

Using the ADuM4136 Isolated Gate Driver and LT3999 DC-to-DC Converter to Drive a 1200 V SiC Power Module

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INTRODUCTION

The success of power developments, such as electric vehicles, renewable energies, and energy storage systems depend on the efficient implementation of electrical power conversion schemes. The core of a power electronic converter contains specialized semiconductor devices and the strategy used to switch these semiconductors on and off, which is achieved with gate drivers.

State-of-the-art wideband devices, such as silicon carbide (SiC) and gallium nitride (GaN) semiconductors feature increased capabilities, such as high voltage ratings from 600 V to 2000 V, low channel impedance, and fast switching speeds up to the megahertz range. These capabilities augment the requirements from gate drivers, for example, shorter propagation delays and improved short-circuit protection via desaturation.

This application note demonstrates the advantages of the ADuM4136 gate driver, a single-channel device with an output drive capability of up to 4 A, a maximum common-mode transient immunity (CMTI) of 150 kV/ μ s, and fast fault management that includes desaturation protection.

A gate driver unit (GDU) for SiC power devices was developed in collaboration with Stercom Power Solutions GmbH showcases the capabilities of the ADuM4136 (see Figure 1). The board is powered with a bipolar, isolated supply based on a push-pull converter that was built with the LT3999 power driver. This monolithic, high voltage, high frequency, dc-to-dc conversion driver features 1 A dual switches with a programmable current limit, frequency synchronization up to 1 MHz, a wide operating range of 2.7 V to 36 V, and a shutdown current of $<1 \mu$ A.

The solution was tested on a SiC metal-oxide semiconductor field-effect transistor (MOSFET) power module (F23MR12W1M1_B11) with a 1200 V drain source breakdown voltage, typical channel resistance of 22.5 m Ω , and pulsed drain current capability of 100 A, with maximum rated gate source voltages of -10 V and $+20$ V.

This application note evaluates the dead time generated by the solution and investigates the total propagation delay introduced by the GDU. Desaturation detection is tested for protection of the SiC devices from overload and short-circuit conditions.

The fast response of the solution is verified by the results of the tests.

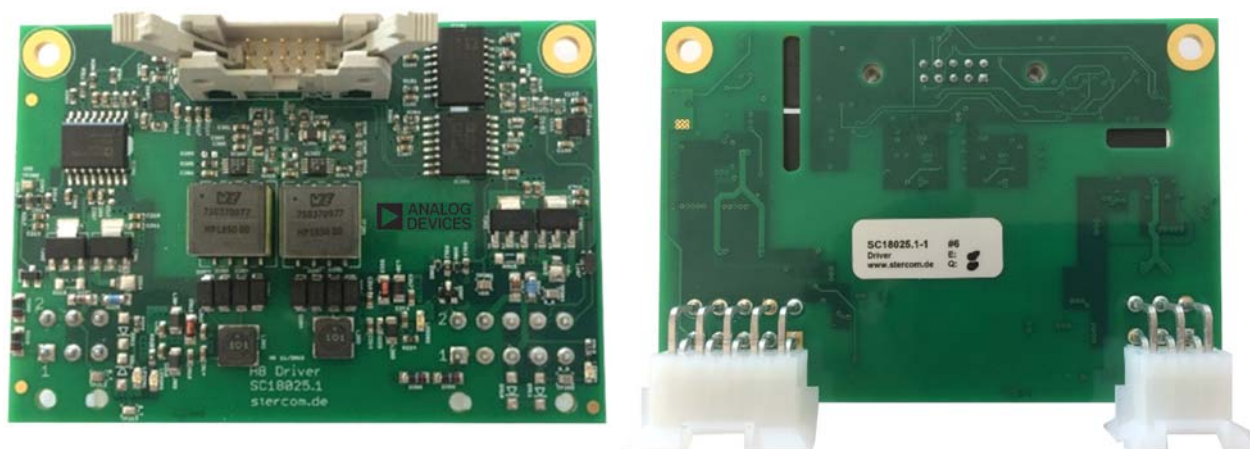


Figure 1. GDU

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REVISION HISTORY

7/2019—Revision 0: Initial Version

TEST SETUP

The full setup used for the reported tests is shown in Figure 2. A high voltage, dc input supply (V1) is placed across the power module. A 1.2 mF, decoupling foil capacitor bank (C1) is added across the input. The output stage is a 38 μ H inductor (L1) that can be connected to the high-side or low-side of the power module during the desaturation protection test. Table 1 summarizes the test setup power components.

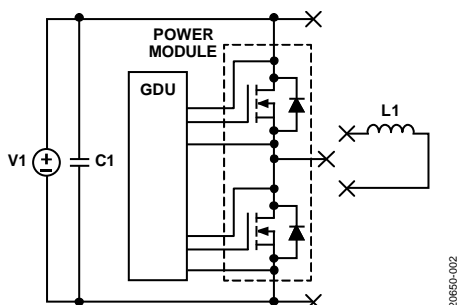


Figure 2. Test Setup Schematic

Table 1. Test Setup Power Components

| Components | Value |
|---|-------------------------------------|
| V1 | 0 V to 1000 V |
| C1 | 1.2 mF |
| SiC Power Module (FF23MR12W1M1_B11) L1 | 1200 V, 23 m Ω 38 μ H |

Table 2. Test Setup Equipment

| Equipment | Manufacturer | Part Number |
|---|-----------------|------------------|
| Oscilloscope | Rohde & Schwarz | HMO3004, 500 MHz |
| DC Power Supply | Komerici | QJE3005EIII |
| Gate Driver Unit (GDU) | Stercom | SC18025.1 PMG02A |
| Pulse Wave Generator | IB Billmann | Fluke 175 |
| Digital Multimeter (DMM) | FLUKE | TT-SI 9010 |
| High Voltage Differential Probe AC Rogowski Current Probe | Testec PEM | CWT mini |

The GDU shown in Figure 4 receives the switching signals from a pulse wave generator. These signals are passed to an integrated dead time generation circuit, implemented with the LT1720 ultra fast, dual-channel comparator, whose output is fed to two ADuM4136 devices. The ADuM4136 gate drivers provide isolated signals to the gate terminals and receive isolated signals from the drain terminals of the two SiC MOSFETs in the power module. The output stages of the gate drivers are supplied with isolated power by a push-pull converter, built with the LT3999 dc-to-dc driver that is fed by an external, 5 V dc power supply. Temperature measurement of the SiC module is implemented with the ADuM4190 high-accuracy isolated amplifier. The ADuM4190 is powered by the LT3080 low dropout (LDO) linear regulator.

Figure 3 shows the experimental setup and Table 2 describes the equipment used in the desaturation protection test.

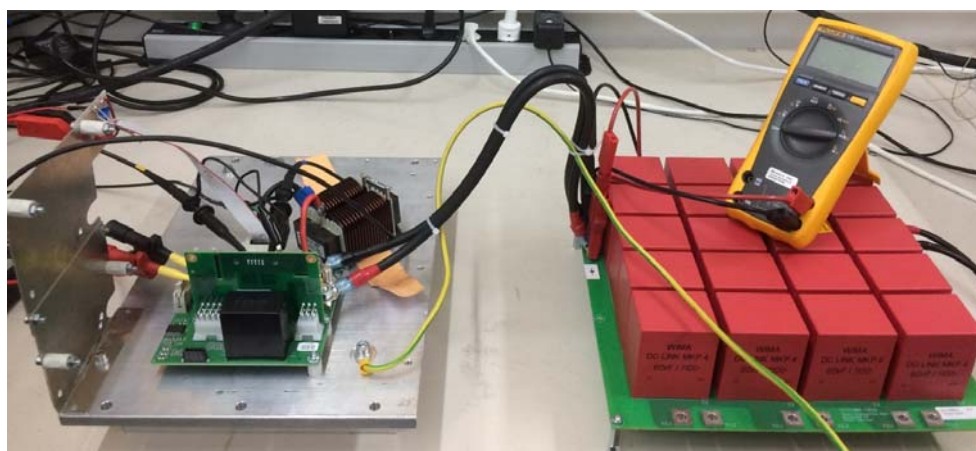


Figure 3. Test Equipment Setup

TEST RESULTS

DEAD TIME AND PROPAGATION DELAY

Hardware dead time is introduced by the GDU to avoid a short circuit in the half-bridge power module, which can occur when the high-side and low-side SiC MOSFETs are turned on or turned off (see Figure 4). Note that the delayed $\overline{\text{PWM_B}}$ signal is indicated within this document as $\overline{\text{PWM_B_D}}$.

In the propagation delay test, dead time is measured on the signal chain of the bottom driver, which is excited by the (active low) input to the GDU $\overline{\text{PWM_B}}$ signal. The dead time generation is realized using resistor-capacitor (RC) filters with the [LT1720](#) ultra fast comparators. Figure 5 to Figure 8 show the results of the propagation delay test. See Table 3 for descriptions of the signals shown in Figure 5 to Figure 8.

Table 3. Oscilloscope Signal Descriptions (Low-Side Driver)

| Symbol | Signal Function | Channel Number |
|-------------------------------|------------------|----------------|
| VGS_B | MOSFET gating | 2 |
| $\overline{\text{PWM_B_D}}$ | After comparator | 3 |
| $\overline{\text{PWM_B}}$ | Input to GDU | 4 |

When the $\overline{\text{PWM_B}}$ input signal is pulled low, the comparator changes its delayed $\overline{\text{PWM_B_D}}$ output state from high to low and the dead time is determined by the RC circuit (~ 160 ns, see Figure 5).

When the SiC MOSFETs are turned off and the $\overline{\text{PWM_B}}$ input signal is pulled high, the $\overline{\text{PWM_B_D}}$ delay time is negligible (~ 20 ns) in comparison to the delay time measured when the SiC MOSFETs are turned on, as shown in Figure 6.

The delay times after the $\overline{\text{PWM_B_D}}$ dead time generation and the VGS_B signals toggle, for both turn on and turn off, are measured as shown in Figure 7 and Figure 8. These short delay times are 66 ns and 68 ns, respectively, and are the delays introduced by the [ADuM4136](#).

The total propagation delay time (dead time plus propagation delay) for turn on is ~ 226 ns, and for turn off is ~ 90 ns. Table 4 gives a summary of the results for propagation delay times.

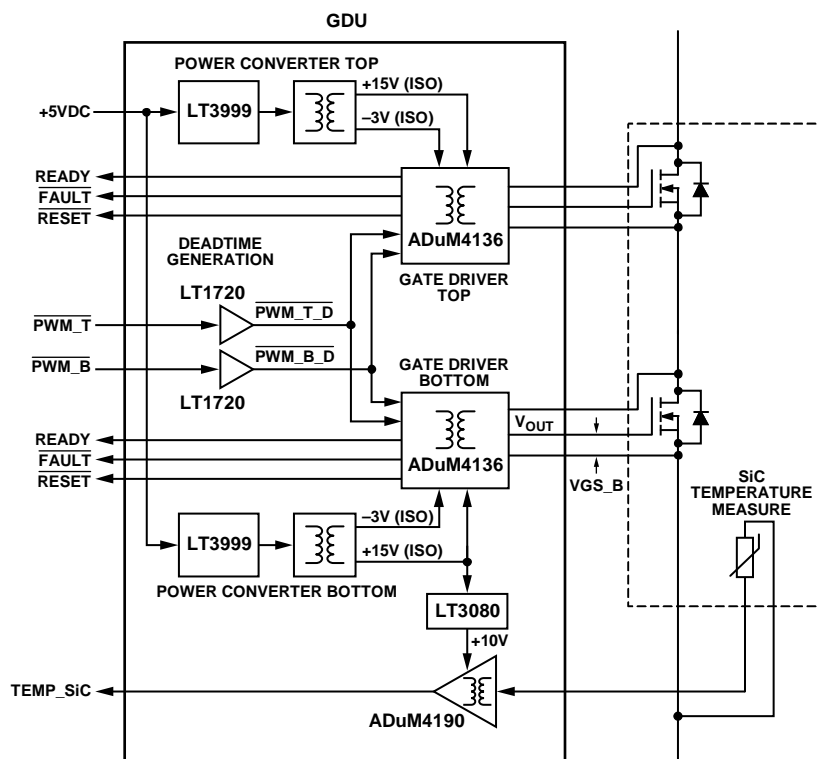


Figure 4. GDU Signal Chain

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Table 4. Propagation Delay Test, Results Summary

| Event | Toggled Signal, High-Low | Toggled Signal, Low-High | Dead Time (ns) | Driver Delay Time (ns) | Total Propagation Delay Time (ns) |
|-------------------|--------------------------|--------------------------|----------------|------------------------|-----------------------------------|
| Device Turned On | PWM_B, PWM_B_D | Gate Signal | 160 | 66 | 226 |
| Device Turned Off | Gate Signal | PWM_B, PWM_B_D | 22 | 68 | 90 |

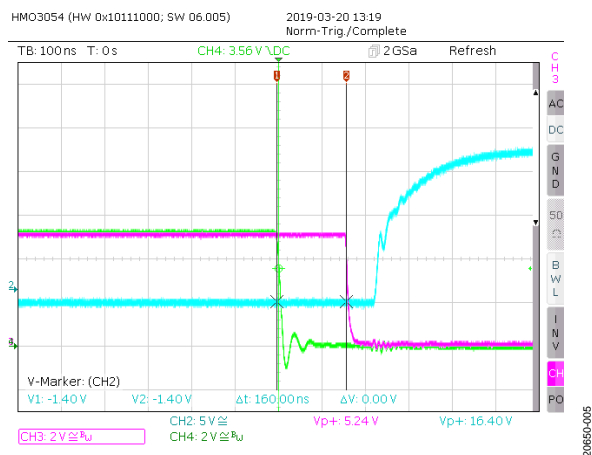


Figure 5. Dead Time Measurement, Device Turned On

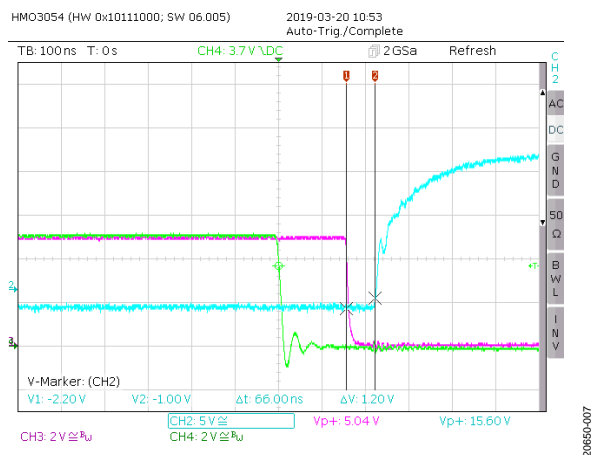


Figure 7. Delay Time Measurement, Device Turned On

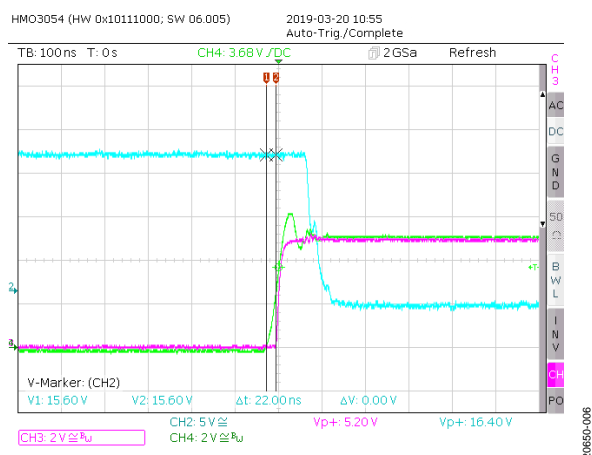


Figure 6. Dead Time Measurement, Device Turned Off

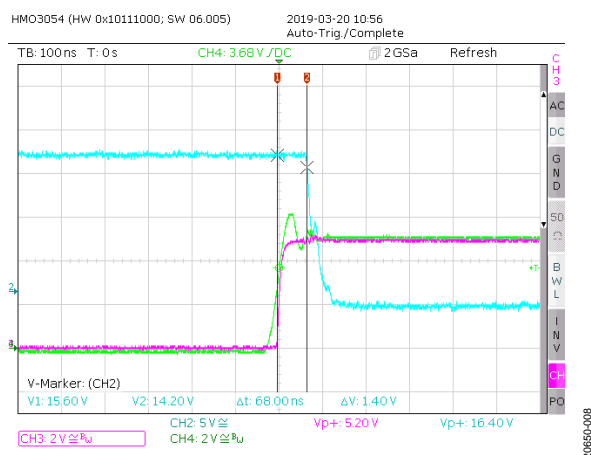


Figure 8. Delay Time Measurement, Device Turned Off

DESATURATION PROTECTION

Desaturation protection against a high voltage short circuit of the driving switch is integrated onto the [ADuM4136](#) IC.

In this application, each gate driver monitors the voltage from the drain to source terminals (V_{DS}) of its MOSFET indirectly, by checking that the voltage at its DESAT pin (V_{DESAT}) does not exceed the reference desaturation voltage level, V_{DESAT_REF} , which varies between 8.66 V and 9.57 V ($V_{DESAT_REF} = 9.2$ V typical). Moreover, the value of V_{DESAT} depends on the MOSFET operation and external circuitry: two high-voltage-protection diodes and a Zener diode (see Table 6 and the Schematics section).

The value of V_{DESAT} can be calculated with the following equation:

$$V_{DESAT} = V_Z + 2 \times V_{DIODE_DROP} + V_{DS}$$

where:

V_Z is the Zener diode breakdown voltage.

V_{DIODE_DROP} is the forward voltage drop of each protection diode.

During turn off, the DESAT pin is pulled low internally and no saturation event is engaged. Additionally, the MOSFET voltage, (V_{MOSFET}) is high and two diodes are reverse-biased, which protects the DESAT pin.

During turn on, the DESAT pin is released after an internal blanking time of 300 ns, the two protection diodes are forward-biased, and the Zener diode breaks down. Here, whether the V_{DESAT} voltage goes above the V_{DESAT_REF} value depends on the value of V_{DS} .

Under normal operation, the V_{DS} and V_{DESAT} voltages remain low. When a high current passes through the MOSFET, the V_{DS} voltage increases and causes the V_{DESAT} voltage level to rise above V_{DESAT_REF} .

In this event, the [ADuM4136](#) gate driver output pin (V_{OUT}) is driven low during 200 ns and desaturates the MOSFET, and a FAULT signal with a delay of $<2 \mu s$ is generated for the gate driver signal (VGS) to immediately lock. These signal can only be unlocked by the RESET pin.

The detection voltage level depends on the value of V_{DS} and can be programmed to any level by choosing the appropriate Zener diode with a breakdown voltage, V_Z . In turn, the MOSFET current (I_D) for desaturation can be estimated based on V_{DS} as described in the MOSFET manufacturer data sheet.

Table 6. Calculated Conditions for Desaturation Protection Tests

| Test | Zener Breakdown Voltage, V_Z (V) | Detection Voltage Level, V_{DS} (V) | Detection Current Level, I_D at 25°C (A) | Detection Current Level, I_D at 125°C (A) |
|-----------|------------------------------------|---------------------------------------|--|---|
| Low-Side | 5.1 | 3.27 | 116 | 95 |
| High-Side | 4.3 | 4.07 | 140 | 110 |

Two desaturation protection tests were performed with gate pulses for both high-side and low-side MOSFETs. Different fault currents were tested in each test by choosing different Zener diodes. The tested current levels are summarized in Table 4, assuming that maximum $V_{DESAT_REF} = 9.57$ V (maximum), and nominal $V_{DIODE_DROP} = 0.6$ V.

Low-Side Test

The low-side desaturation protection test was performed by varying the input voltage (V_1) from 100 V to 800 V at a room temperature of 25°C (see Figure 9).

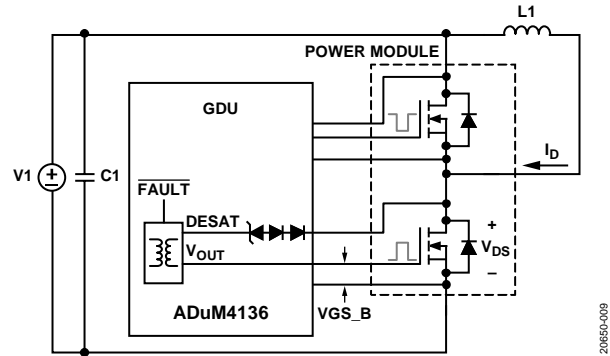


Figure 9. Low-Side Desaturation Protection Test

Figure 10 to Figure 17 show the results of the low-side desaturation protection test. Table 5 describes the signals shown in Figure 10 to Figure 17.

Table 5. Oscilloscope Signal Descriptions (Low-Side Test)

| Channel Number | Signal Name |
|----------------|-------------|
| 1 | FAULT |
| 2 | V_{DS} |
| 3 | I_D |
| 4 | VGS |

In Figure 16 and Figure 17, the desaturation protection was triggered for a current of ~ 125 A at 25°C, and the fault status pin was triggered low after a delay of around 1.34 μs .

Similar tests were run for the high-side of the power module, where the desaturation protection was triggered for a current of ~ 160 A at 25°C, with the fault status pin triggered low after 1.32 μs .

The results for the low-side and high-side tests show that the desaturation detection with current levels close to the ones programmed can be reported by the gate driving solution at a high speed of $<2 \mu s$ (see Table 4).

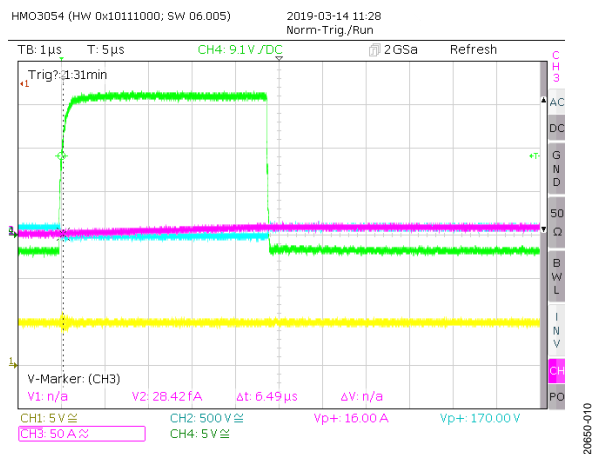


Figure 10. Low-Side Test, V1 = 100 V, No Fault

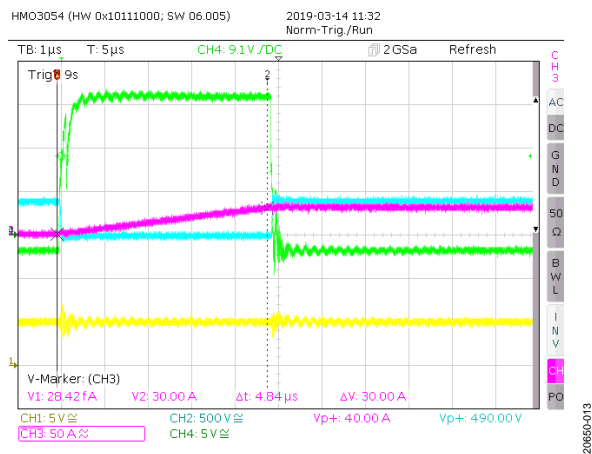


Figure 13. Low-Side Test, V1 = 400 V, No Fault

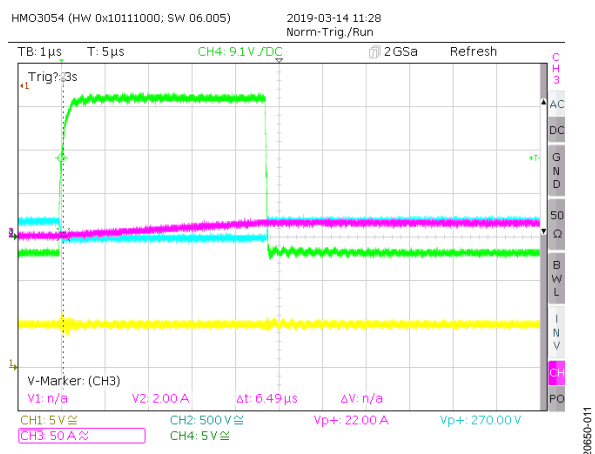


Figure 11. Low-Side Test, V1 = 200 V, No Fault

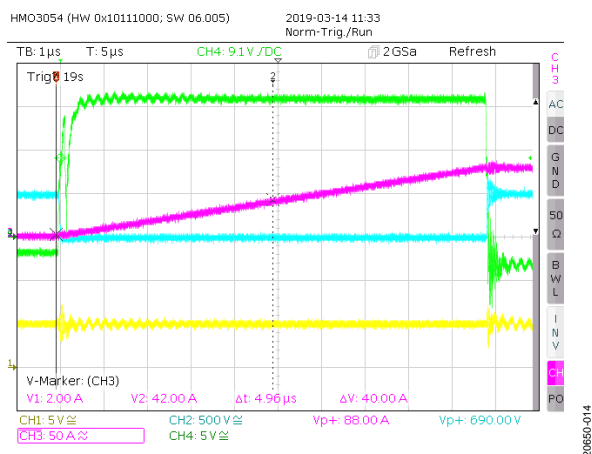


Figure 14. Low-Side Test, V1 = 500 V, No Fault

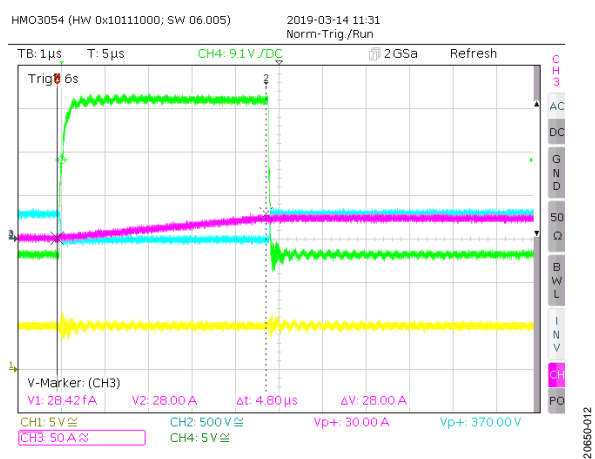


Figure 12. Low-Side Test, V1 = 300 V, No Fault

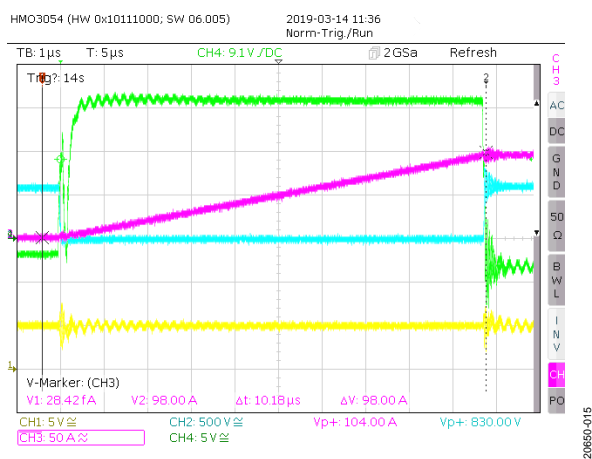
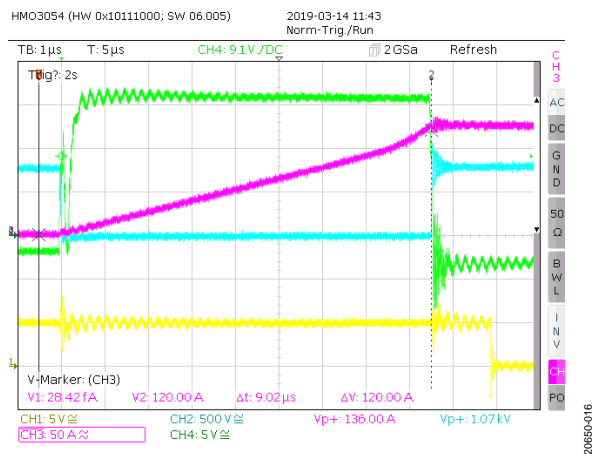
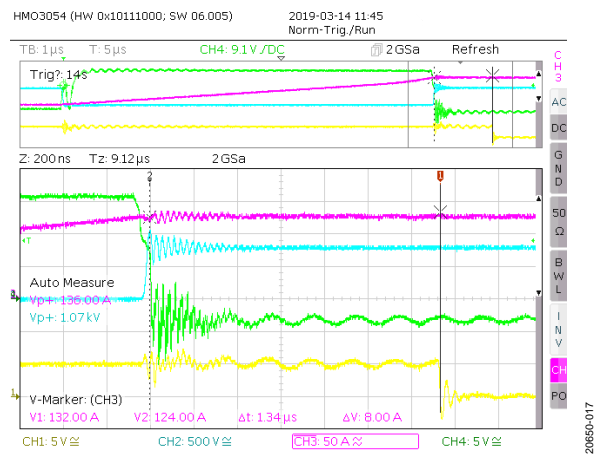


Figure 15. Low-Side Test, V1 = 600 V, No Fault

Figure 16. Low-Side Test, $V_1 = 800$ V, Fault DetectedFigure 17. Low-Side Test, $V_1 = 800$ V, Fault Detected (Zoom In)

SCHEMATICS

Figure 18 to Figure 20 to show the schematics for the **ADuM4136** gate driver board.

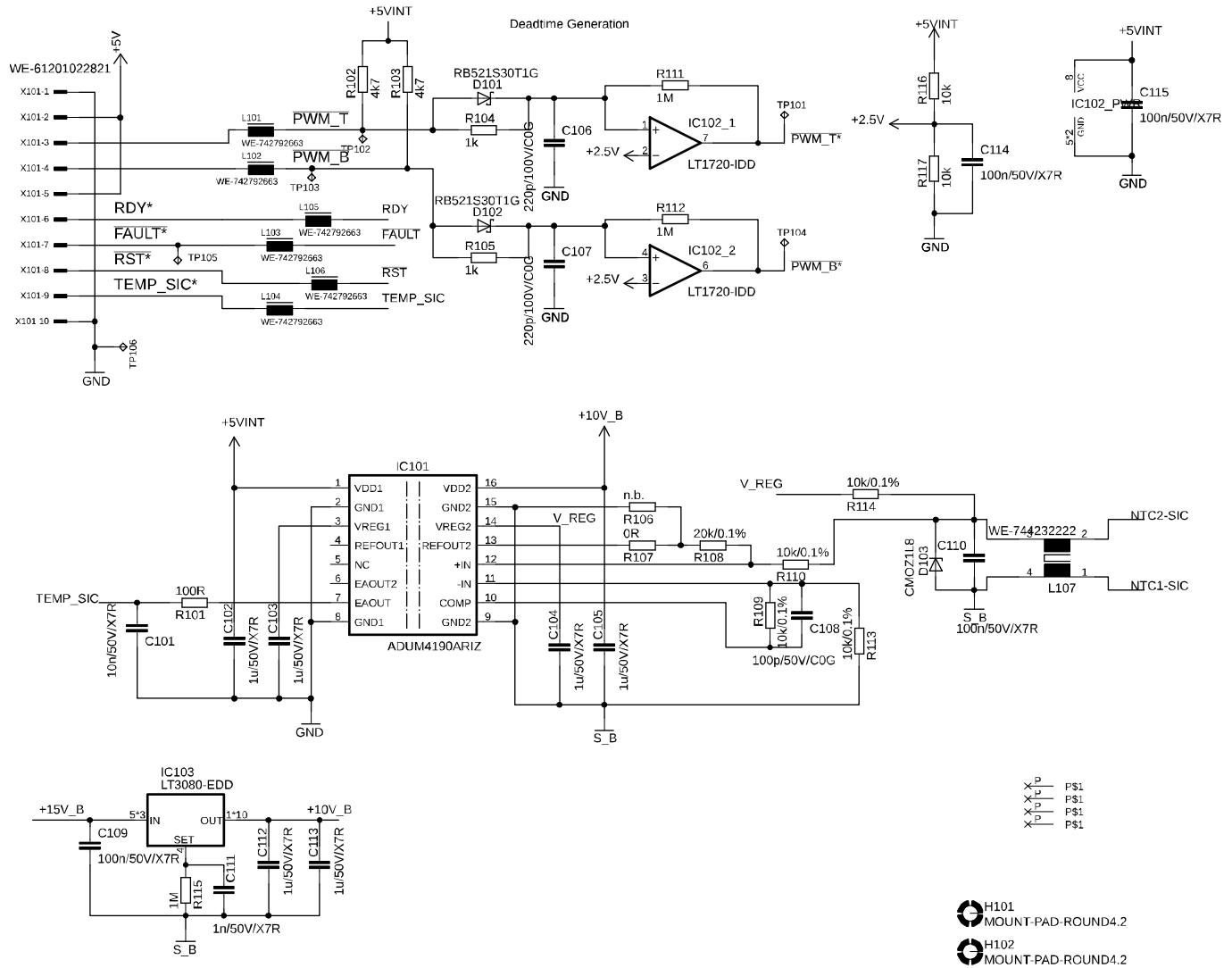


Figure 18. **ADuM4136** Gate Drive Board Schematic (Primary Side)



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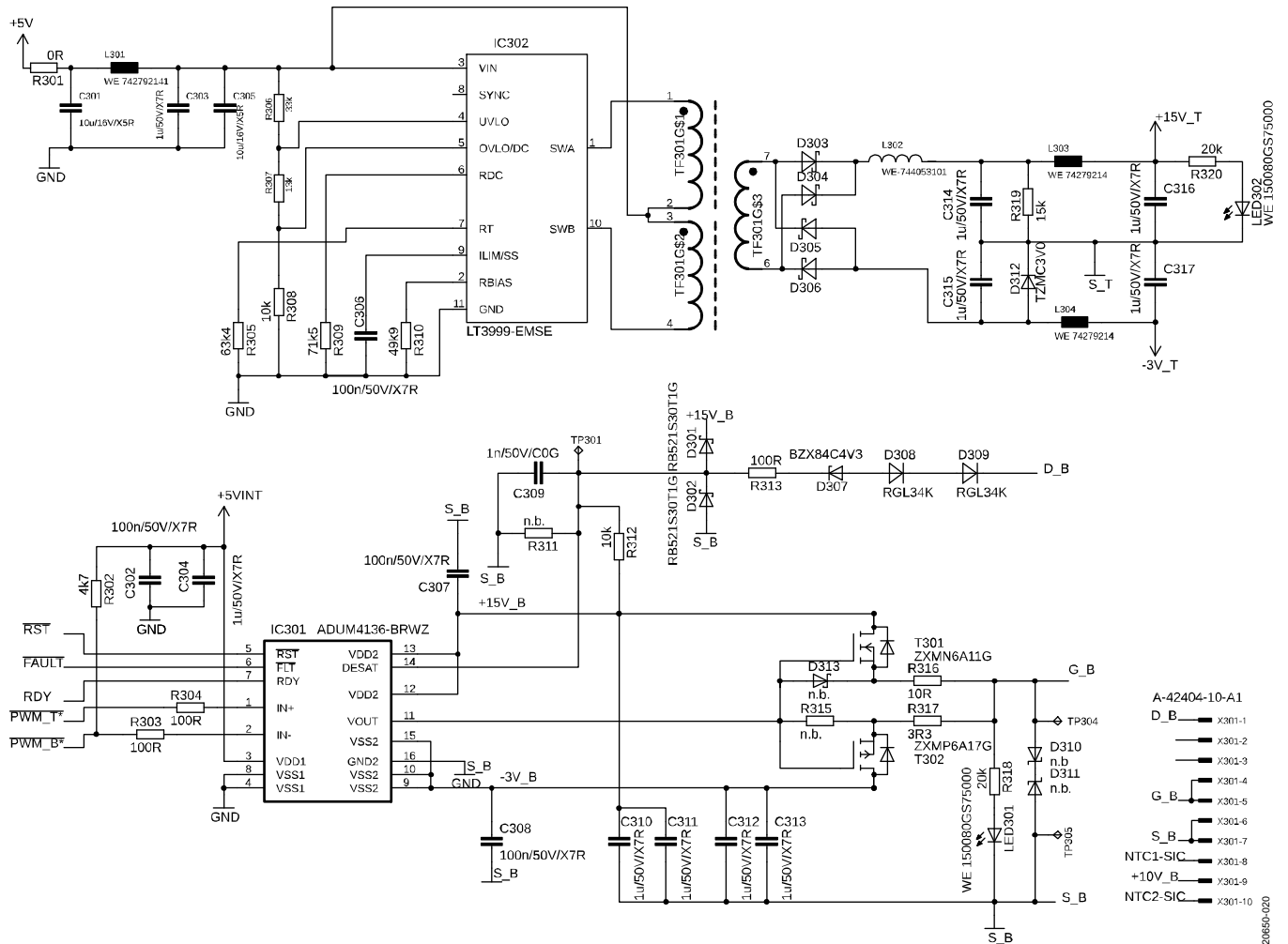


Figure 20. ADuM4136 Gate Drive Board Schematic (Isolated Power and Gate Signal for Low-Side)

CONCLUSION

The [ADuM4136](#) gate driver features short propagation delay and fast overcurrent fault reporting via desaturation protection. These advantages, aligned with adequate external circuitry design, can satisfy the stringent requirements for exploiting the capabilities that state-of-the-art wide-band devices such as SiC and GaN semiconductors can offer.

The test results in this application note provide data from a full gate driving solution for driving a SiC MOSFET module under high voltage, with an ultra fast response, and adequate fault management via desaturation protection. This gate driving solution is powered by a low-noise, compact, power converter built with the [LT3999](#), which provides isolated power of adequate voltage levels with low shutdown currents and soft-start capabilities.