Technical Article

How a High Dynamic Range RF Transceiver Solves the Blocking Challenge for Mission Critical Communications

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Abstract

With limited spectrum and increasing use of commercial/private cellular networks, radio platform development is facing more complex interference scenarios. This article will discuss how the ADRV9002 software-defined radio (SDR), a high dynamic range (DR) RF transceiver, can address the blocking challenge for mission critical communications radios and other high dynamic demanding wireless applications.

Introduction

Mission critical communications systems are essential for our emergency services, utility services, as well as government and military tactical radio systems. Mission critical communications systems are deployed across many operating frequency bands and must coexist with the expanding commercial cellular networks. This places significant challenges on the radio designs as receivers must decipher very low level signals in the presence of large blocking or interfering signals. Furthermore, with many portable and handheld use cases, the size, weight, and power (SWaP) are also major design considerations. An integrated SDR IC is capable of covering the many frequency bands and providing DR to handle the increasing congested operational deployments in small form factor.

To meet these needs, a new family of SDR was designed. The ADRV9002 RF transceiver was designed for the many mission critical comminutions markets and supports narrow-band (NB, low to kHz) and wideband (WB, up to 40 MHz) operation. ADRV9002 is a highly integrated RF-to/from-bit system platform with unified software programmable architecture and incorporates many advance features for mission critical communications including fast frequency hopping (FFH), multichip synchronization (MCS), digital predistortion (DPD), dynamic profile switching (DPS), digital downconverter (DDC), monitor mode (MM), and advanced calibration algorithms that significantly reduce the load on baseband processor. The ADRV9002 offers exceptional DR to provide the best sensitivity and blocker tolerance to handle the challenging deployment and interfering signals.

Blocking Requirements for Receivers

The DR of a receiver is its maximum input signal-to-noise floor, and DR is one of the key factors that determine a receiver's ability to recover low level signals in the presence of blockers (interferers). The minimum detectable signal or sensitivity is determined by the signal bandwidth (BW), the receiver demodulation threshold (SNR_{MIN}), and the receiver's noise figure (NF). It can be denoted by the following equation:

$$Sensitivity = -174\ \text{dBm/Hz} + NF + 10 \times log_{10}(BW) + SNR_{MIN} \quad (1)$$

Because the LO phase noise and reciprocal mixing mechanism are shown in Figure 1, the large blocker energy could spread out to wanted signal and cause the receiver sensitivity degradation; the larger the blocker and the closer it is to the wanted signal, the more sensitivity degradation of the receiver. The large blocker itself may also introduce nonlinearities in the receiver front end and cause the spurious rejection into the wanted signal band. The third-order intermodulation products of two large blockers at equally frequency offsets from the wanted signal will fall in the wanted signal band and cause the receiver performance degradation.

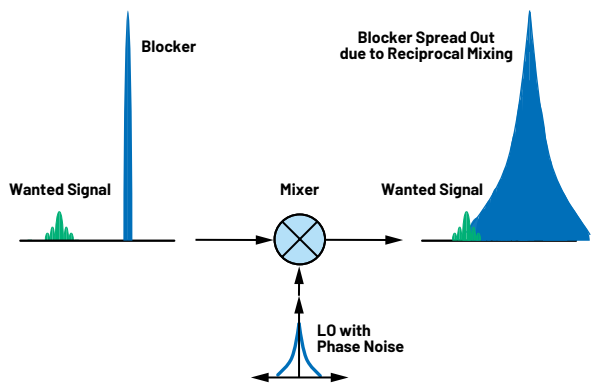

Figure 1. Reciprocal mixing.

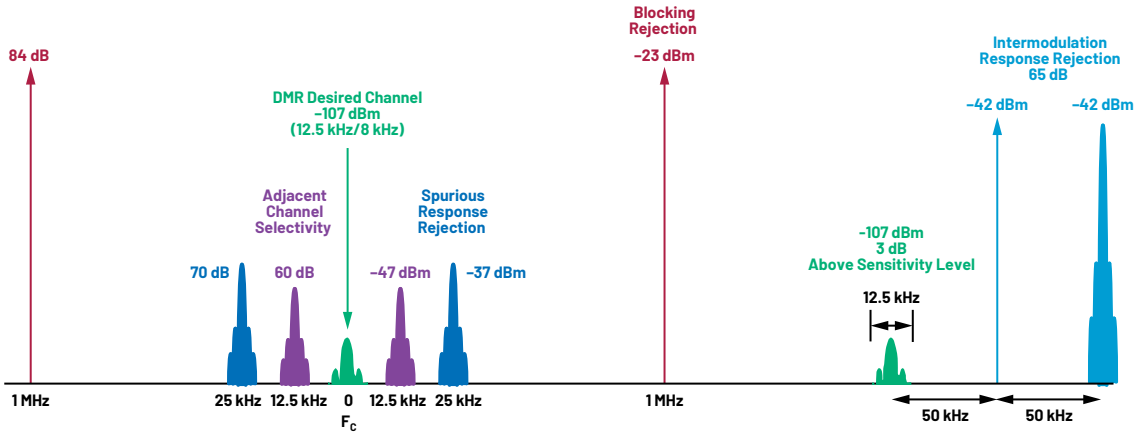

Figure 2. The DMR standard defines the blocking requirements.

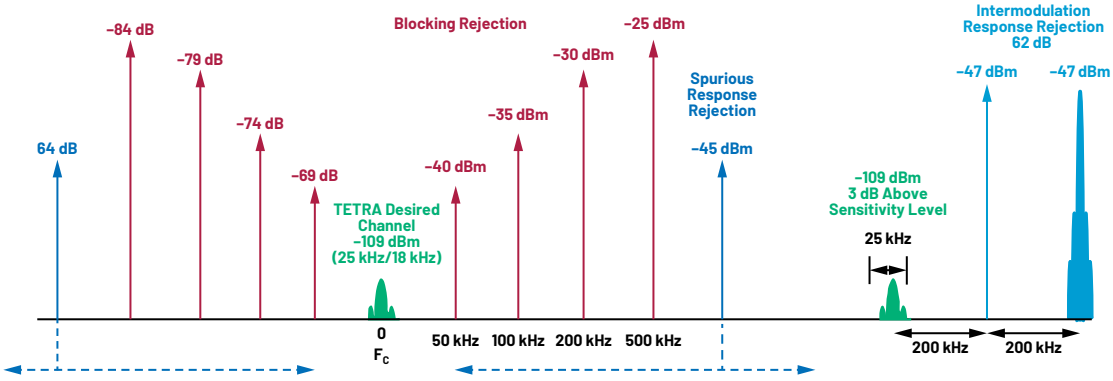

Figure 3. The TETRA standard defines the blocking requirements.

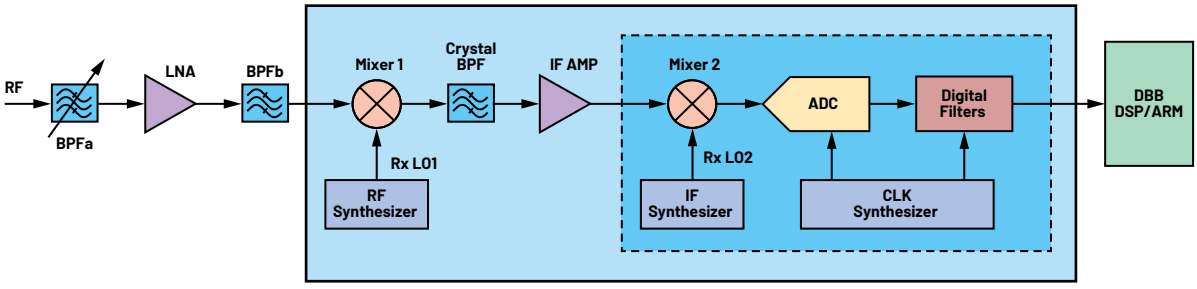

Figure 4. A traditional superheterodyne receiver.

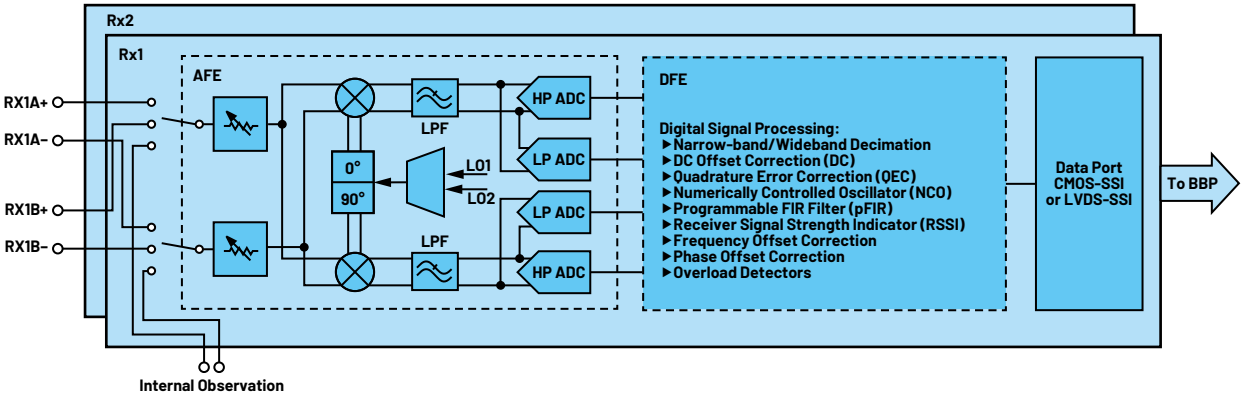

Figure 5. Top level ADRV9002 dual receiver architecture.

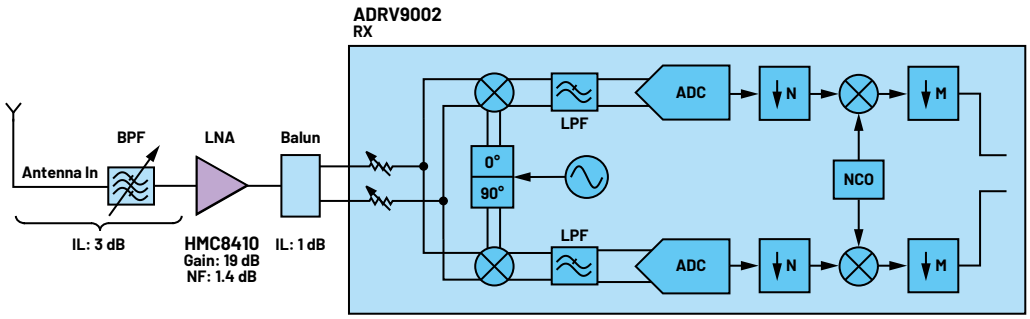

Figure 6. Mission critical communications receiver diagram with ADRV9002.

Figure 2 and Figure 3 show the DMR[1] and TETRA[2] standards that define various interferers and the level requirements for the receiver to tolerate. The standards require the radios to have the capability to handle at least 84 dBc blocking at 1 MHz (DMR) or 500 kHz (TETRA) frequency offset. The radio producers may want 90 dBc or even higher to make their products more competitive. Similarly, for the adjacent channel selectivity, spurious rejection, and intermodulation response rejection, the receiver should have the capability to accommodate all these types of blockings with some margins.

To meet the DMR/TETRA example blocking requirements in Figure 2 and Figure 3, the traditional superheterodyne architecture that is typically utilized in which the RF signal is downconverted to one or two intermediate frequencies (IF), as shown in Figure 4. A pair of tunable BBPs (BPFa, BPFb) is applied to reject out of band blockers as well as the image of Mixer 1 for VHF/UHF band, or a single SAW band filter could be applied for higher frequency band like 800 MHz/900 MHz. The crystal BPF after Mixer 1 has a sharp frequency response to provide channel selectivity and anti-image of Mixer 2. ICs like AD9864 have the integrated functions for the second mixer, IF/CLK synthesizer, ADC, programable decimation filters, etc., which can provide a good in-channel SNR.

The type of superheterodyne architecture shown in Figure 4 highly relies on external BPF (both RF and IF) to filter the in-band and out-of-band blockers and images, with other discrete components for the receiver and transmitter; such architecture limits the ability to lower the radio size, weight, and cost, as well as the multistandard support.

ADRV9002 Receiver Architecture

Figure 5 shows the top level ADRV9002 receiver architecture,[3] which has two identical receivers. The analog front end (AFE) contains the programmable front-end attenuator, matched I and Q mixer, a programmable first-order or second-order low-pass filter (LPF), and two sets of ADCs (high performance (HP) and low power (LP)) per channel. The digital front end (DFE) contains a series of digital signal processing blocks, including decimation filters, DDC, a programmable FIR (PFIR) filter, correction algorithm modules, and so on. ADRV9002 receiver provides flexible NB and WB mode support, automatic or manual gain control, direct conversion, or IF operation. The highly integrated RF-to-bit receiver could replace all the function blocks in the dot rectangle of Figure 4. A much simplified new mission critical communications receiver diagram with ADRV9002 is shown in Figure 6.

Using a set of HPADC and LPADC is the unique design of ADRV9002 receiver, and it provides the maximum linearity (IIP3) and the best power consumption trade-off. HPADC and LPADC have a similar level of noise and DR, with HPADC offering an improved IIP3 performance of around 5 dB compared to LPADC at a price of increased power consumption. The system NF would be expected to be similar between HPADC and LPADC at the antenna input as a result of LNA gain in the front end. Utilizing the fast analog and digital peak detector functions of ADRV9002 receiver, users can dynamically switch the usage of HPADC and LPADC when large blockers are detected or disappeared, so the receiver linearity and power consumption can be well balanced.

The ADC (both HPADC and LPADC) signal transfer function (STF) has a low-pass filter response, which acts as an antialiasing filter and significantly reduces the blockers around the sample rate. It also reduces the antialiasing requirements for the analog LPF before the ADC. Figure 7 shows the ADRV9002 ADC STF and analog LPF frequency response, where the HPADC runs at a 2.2 GHz sample rate and LPF is set to first order with around 20 MHz f1 dB frequency. Benefited from the high DR of the ADCs, ADRV9002 doesn't rely on the analog LPF for the blockers' rejection and channel selectivity; therefore, the analog LPF is designed to a configurable first- or second-order LPF with around 5 MHz to 50 MHz bandwidth. It provides the antialiasing function for ADC and helps attenuate the out of band blockers. The channel filter is done at the end of digital data path by the PFIR filter.

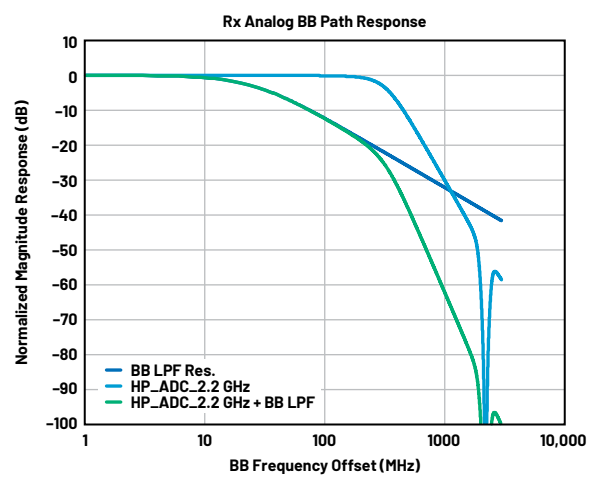

Figure 7. ADRV9002 ADC STF and analog LPF frequency response.

The ADRV9002 receiver can support up to 40 MHz RF bandwidth, and the programmable NCO and DDC allow for digitally downconverting from intermediate frequencies up to ±20 MHz, which works for both NB and WB signals. This provides the flexible direct conversion or IF operation for the receiver. Note that the offset IF plus ½ of the RF signal BW should always be smaller than 20 MHz to make sure the input signal won't be distorted by the digital filters after ADC.

ADRV9002 Receiver Blocking Tolerance

As previously discussed, the maximum blocking tolerance or maximum tolerable blocker power above wanted signal is mainly determined by the following factors:

- Dynamic range (receiver max input signal-to-noise floor)
- Receiver linearity, in scenario where distortion products fall into desired channel
- Image rejection in IF mode, only when interferer is at image frequency
- LO phase noise

Dynamic Range

Receiver must provide enough DR to accommodate the blockers and wanted signal. Unlike the traditional superheterodyne receiver in Figure 4, ADRV9002 receiver doesn't rely on the external BPF to filter the blockers. The ADRV9002 receiver has around 150 dBc/Hz DR, which is enough to accommodate and digitalize both blockers and wanted signal in the analog/RF section of the receiver path, and thanks to that the blocker can be filtered efficiently in the digital domain. Equation 2 shows the calculation of ADRV9002 receiver DR at maximum gain.

$$\begin{aligned} DR\ (\text{dBc/Hz}) &= \textit{Maximum Input Signal Power} - \textit{Noise Floor} \\ &= (-11.4\ \text{dBm}) - (-174\ \text{dBm/Hz} + 12.5\ \text{dB}) \\ &= 150.1\ \text{dBc/Hz} \end{aligned} \tag{2}$$

where -11.4 dBm is the ADRV9002 receiver typical full-scale input power (FSIP) and 12.5 dB is the typical NF of ADRV9002 receiver.

ADRV9002 receiver has around 20 dB maximum gain and 34 dB gain control range set by the attenuators before the mixer, and the more attenuation applied, the less receiver gain. Receiver could provide dB per dB NF and linearity trade-off, and 1 dB gain decrease increases NF by 1 dB and increase IIP3 and IIP2 by 1 dB. Likewise, 1 dB gain decrease increases the FSIP by 1 dB. Figure 8 shows the ADRV9002 receiver NF, IIP2, IIP2, and FSIP at different gain. Based on Equation 2, the ADRV9002 receiver 150 dBc/Hz DR can be maintained in the receiver gain control range.

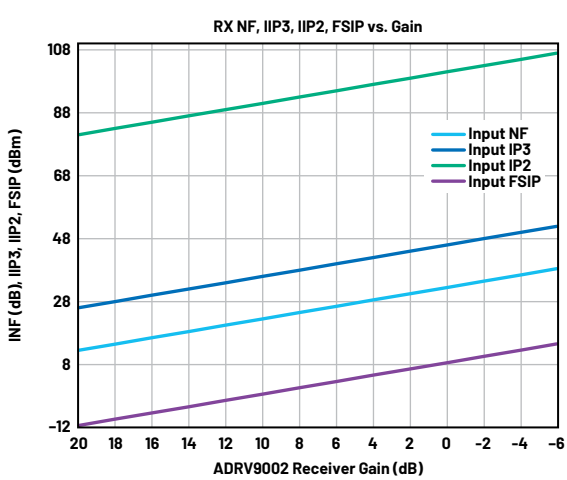

Figure 8. ADRV9002 receiver NF, IIP3, IIP2, and FSIP vs. gain.

Figure 6 shows the receiver, the front-end insertion loss (IL) before LNA as well as LNA gain, and NF dominates the overall system noise floor and consequently to the system DR. The system NF (NF_{SYS}) can be calculated by Equation 3.

$$\begin{aligned} NY_{SYS}(\text{dB}) = 10 \times log10\{&F_{FE} + (F_{LNA} - 1)/A_{FE} \\ &+ (F_{BALUN} - 1)/(A_{FE} \times A_{LNA}) + \\ &+ (F_{TRX} - 1)/(A_{FE} \times A_{LNA} \times A_{BALUN})\} \end{aligned} \tag{3}$$

where:

- F_{FE} is the noise factor of all front end before the LNA
- A_{FE} is the linear insertion loss of FE before the LNA
- F_{LNA} is the LNA noise factor
- A_{LNA} is the linear LNA gain
- F_{BALUN} is the noise factor of the balun
- A_{BALUN} is the balun linear insertion loss
- F_{TRX} is the ADRV9002 noise factor.

For the receiver in Figure 6, there is a 3 dB front-end insertion loss before the LNA. The LNA (HMC8410) has 1.4 dB NF and 19 dB gain. The balun insertion loss is 1 dB, and the ADRV9002 receiver NF is 12.5 dB at maximum gain. From Equation 3, the system NF for this receiver is around 5.1 dB, the total gain from antenna to ADRV9002 input is 15 dB. Using Equation 2, the system DR at antenna input with ADRV9002 maximum gain is around:

$$\begin{aligned} DR_{SYS}(\text{dBc/Hz}) &= (-11.4\ \text{dBm} - 15\ \text{dB}) \\ &\quad -(-174\ \text{dBm/Hz} + 5.1) \\ &= 142.4\ \text{dBc/Hz} \end{aligned} \tag{4}$$

Figure 9 shows the system DR and NF at the antenna input with different ADRV9002 gain, with the ADRV9002 receiver large DR design. The system DR is always limited by the front-end LNA, and this should be carefully designed from a system perspective.

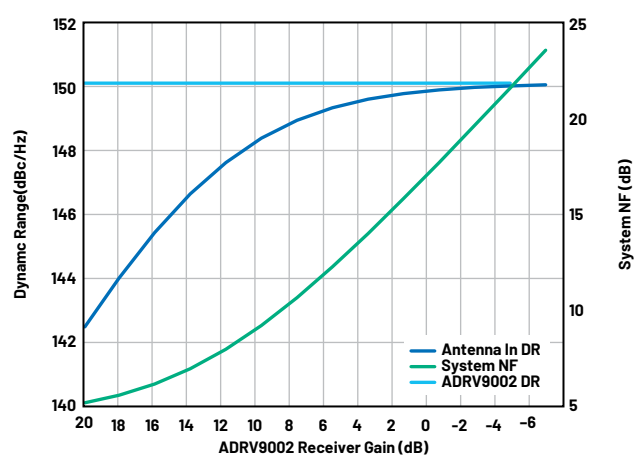

Figure 9. System NF and DR vs. ADRV9002 gain

In radio design practice, Equation 4 can be used to estimate the receiver DR requirement or to estimate the maximum blocker to desired signal tolerable ratio for a given receiver DR. Figure 10 demonstrates the DR estimation diagram for Equation 4.

$$\begin{aligned} DR\ (\text{dBc/Hz}) = P_{BLK\text{-}TO\text{-}DESIRED}\ (\text{dBc}) + PAR_{BLK} + HR \\ + SNR_{MIN} + 10 \times Log\ (BW) \end{aligned} \tag{5}$$

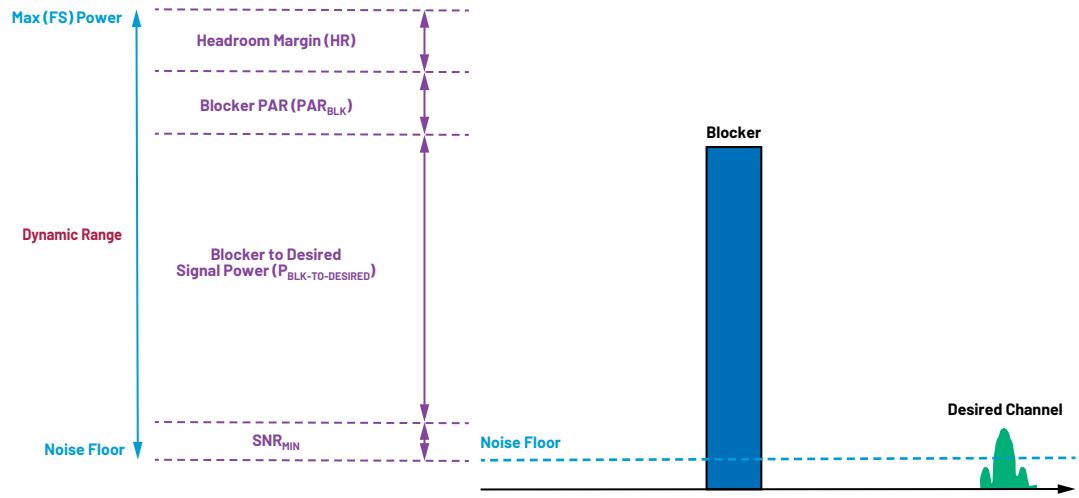

Figure 10. DR requirement analysis diagram.

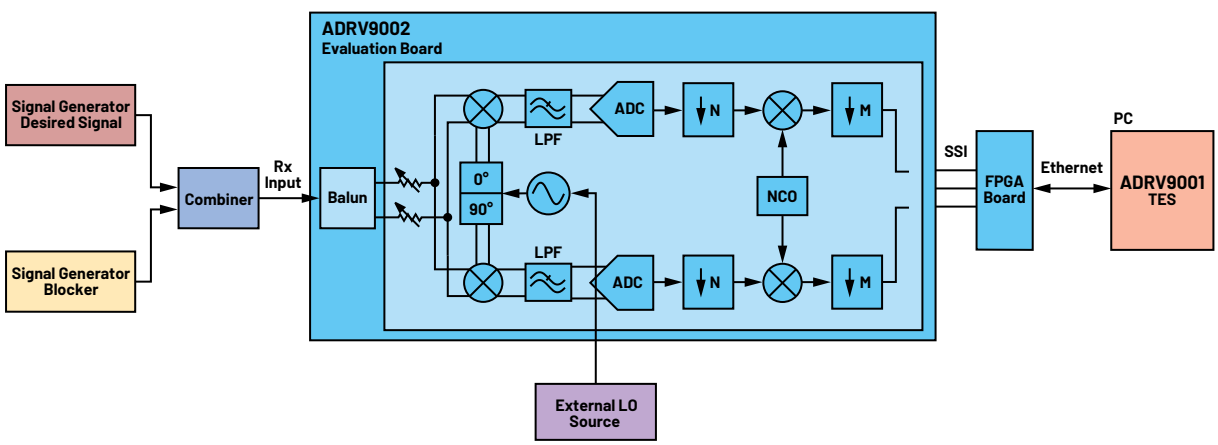

Figure 11. An ADRV9002 blocking test diagram.

Using a typical DMR signal with a CW blocker as an example. Assumed the DMR desired signal BW is 8 kHz, SNR$_{MIN}$ is around 7 dB, 0 dB PAR for CW blocker, and 1 dB for headroom margin. Then based on Equation 4, we can derive that ADRV9002 150 dBc/Hz DR could allow tolerance to a CW blocker as large as 103 dBc above the desired signal with at least 7 dB SNR.

$$\begin{aligned} P_{BLK\text{-}TO\text{-}DESIRED}\ (\text{dBc}) = {} & 150\ \text{dBc/Hz}\ DR - 0\ PAR_{BLK} \\ & -1\ \text{dB}\ HR - 7\ \text{dB}\ SNR_{MIN} \\ & - 10 \times Log(8e3) = 103\ \text{dBc} \end{aligned} \tag{6}$$

Similarly, if the blocker is an LTE10 wideband signal with around 10.3 dB PAR, ADRV9002 150 dBc/Hz DR could allow tolerance to an LTE10 blocker as large as 92.7 dBc.

$$\begin{aligned} P_{BLK\text{-}TO\text{-}DESIRED}\ (\text{dBc}) = {} & 150\ \text{dBc/Hz}\ DR - 10.3\ PAR_{BLK} \\ & -1\ \text{dB}\ HR - 7\ \text{dB}\ SNR_{MIN} \\ & - 10 \times Log(8e3) = 92.7\ \text{dBc} \end{aligned} \tag{7}$$

The above estimation is only for a DR perspective as well as blocker, and LO phase noise performance can degrade the maximum tolerable blocker to a wanted signal. Verifying ADRV9002 receiver's high DR concept for blocking will require high quality signal generator for blocker and external LO. The front-end LNA linearity (IIP3) should not limit the test if the LNA is applied.

Figure 11 shows the ADRV9002 blocking test setup to verify the above analysis and calculation. ADRV9002 is configured to a DMR profile with the IF at 490 kHz, and external LO is applied for the receiver. The desired receiver signal at ARDV9002 receiver input is around -108 dBm, sets the signal generator to different output blocker frequency offset, and increases the blocker level until the wanted signal SNR degrades to SNR$_{MIN}$ in Equation 1 (which is around 7 dB for DMR 8 kHz signal BW). Then, the maximum blocker tolerance at the corresponding frequency offset is noted.

Figure 12 and Figure 13 show the ADRV9002 DMR profile blocking test results with a CW blocker and an LTE10 blocker close to the desired signal.

In the CW blocker test, the desired signal is around 150 MHz. Two signal sources with excellent phase noise are used for the external LO and CW blockers, respectively; therefore, the LO and blocker phase noise basically didn't affect the blocking test. The ADRV9002 CW blocker rejection test results closely match above the 103 dBc estimation except for the blocker at 1 MHz frequency offset, which is around two times the IF frequency and is limited by the image rejection performance.

For another test case, the LTE blocker test, the desired signal is set to 860 MHz, a Keysight N5182B signal generator generates the modulated LTE10 blocker, and ADF5335 PLL is used for the external LO source. The LTE10 blocker rejection test results are very close to the 92.7 dBc estimation results but have about a 3 dB gap. This is mainly the affection of LO and blocker phase noise.

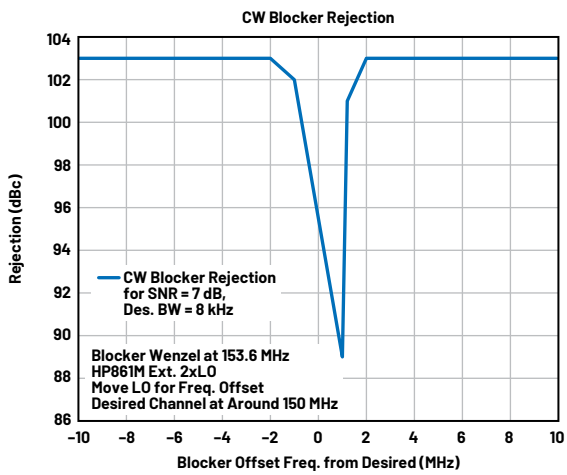

Figure 12. ADRV9002 DMR profile CW blocker tolerance test results.

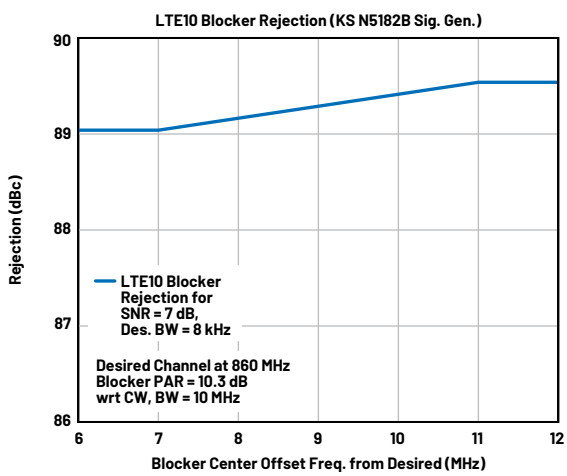

Figure 13. ADRV9002 DMR profile LTE10 blocker tolerance test results.

The above ADRV9002 DMR mode DR estimation and testing results assume there is no filter before the ADC. The ADRV9002 analog LPF can partially attenuate the blocker. This improves the results especially as blockers move to higher offset frequencies—for example, ≥ 5 MHz.

Linearity

The third-order intermodulation products of two large blockers (or the wideband blocker's third nonlinearity components) can fall into the desired signal band and desensitize the receiver. The receiver linearity will limit the overall blocker tolerance below the DR. A simple analysis of third-order nonlinearity distortion can be done by using IP3 (third-order intercept point) concept. Figure 14 shows the wideband blocker nonlinearity products fall into the desired signal band scenario, and a simplified two-tone model can be used for the wideband blocking analysis. The power of each tone is half of the total blocker power (P_{BLK} –3 dB) and spacing equal to the blocker BW and the power of the distortion component (P_{IM}) is equivalent to the total distortion power on each side of the wideband blocker. DMR/TETRA standard intermodulation rejection response in Figure 2 and Figure 3 is validated by an unmodulated interfering signal and a modulated signal, but since the DMR/TETRA modulated signal has a narrow bandwidth, the intermodulation rejection response can also be simplified to the two-tone model in Figure 14, where the BW will be the two interfering signal spacing defined by the DMR/TETRA test specifications.

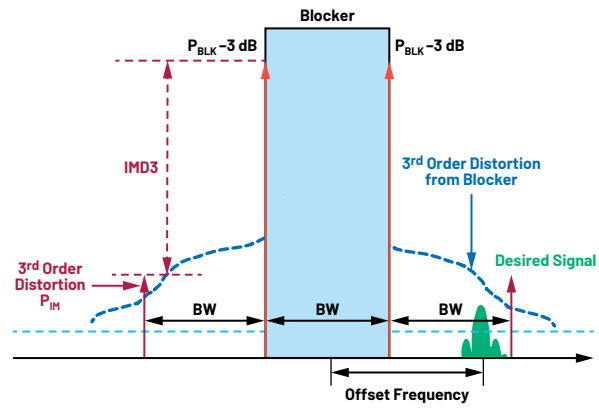

Figure 14. Blocker nonlinearity and analysis.

Receiver IP3 from the two-tone model third-order intermodulation distortion (IMD3) can be denoted by the following equation:

$$IP3\ (\text{dBm}) = P_I\ (\text{dBm}) + [P_I\ (\text{dBm}) - P_{IM}\ (\text{dBm})]/2 \qquad (8)$$

where P_I is the input tone power and P_{IM} is the third-order distortion power.

The ADRV9002 receiver's typical IIP3 is 26 dBm with HPADC. To analyze if the ADRV9002 linearity can meet the DMR intermodulation rejection response requirement, we use the receiver setup in Figure 6. The total FE gain before ADRV9002 is 15 dB. Figure 2 shows –107 dBm desired signal at ADRV9002 input will be –92 dBm and maximum allowable noise caused by third-order distortion or P_{IM} would be –99 dBm at 7 dB SNR_{MIN}. From Equation 5, the maximum allowable P_I at ADRV9002 input can be calculated as –15.7 dBm and would be around –30.7 dBm at the antenna input, which is much higher than the –42 dBm DMR standard requirement. Similarly, ADRV9002 receiver IIP3 is 22 dBm with LPADC. This would allow around –33.3 dBm maximum P_I at antenna input, which still can meet the DMR intermodulation rejection requirement.

Likewise, the interfering blocking requirement in Satellite Earth Stations and Systems (SES)[4] that is compatible with the radio equipment directive (RED) needs the receiver to tolerate up to an 87 dBc LTE 5 MHz blocker with 2.5 dB SNR_{MIN}, as shown in Figure 15. Using the same receiver in Figure 6, the blocker at ADRV9002 input would be –15 dBm with 15 dB FE gain and the desired signal at ADRV9002 input would be –102 dBm. Assuming 7.5 dB PAR for LTE 5 MHz signal and 1 dB margin to ADRV9002 full scale, ADRV9002 receiver needs 5 dB back off from the maximum gain to accommodate the –15 dBm LTE blocking signal, and ADRV9002 IP3 would be 31 dBm at around 15 dB gain in Figure 8.

As shown in Figure 14, the wideband 5 MHz LTE blocker can be simplified to a two-tone approach for IM3 estimation. Each tone power P_i at ADRV9002 input is −18 dBm. From Equation 5, the third-order distortion power P_{IM} is −116 dBm and the distortion power on one side of the blocker is −98 dBc to the blocker, which can meet the RED blocking requirement (−87 dBc blocker to desired power ratio −2.5 dB SNR_{MIN}). Actually, for the wideband blocking, only a portion of the third-order distortion falls in the desired signal band, and the factor is 10 × log10 (156 kHz/7.5 MHz), where 156 kHz is a desired signal BW and 7.5 MHz is the offset from a blocker center to third-order distortion, so the effective distortion power in the desired signal band is much smaller than P_{IM}. The ADRV9002 receiver linearity has lots of margin to meet the RED spec.

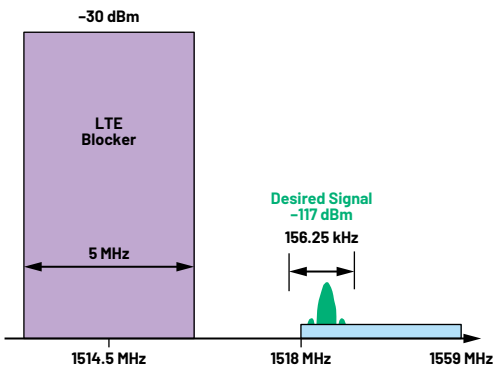

Figure 15. Satellite receiver blocker requirement (compliance with ETSI RED).

Note that these calculations only considered the ADRV9002 receiver third-order distortion. The analysis shows the ADRV9002 receiver linearity has lots of margin to meet the DMR standard blocking intermodulation rejection spec as well as the RED spec. The ADRV9002 receiver provides dB per dB gain and a linearity trade-off, the lesser gain the bigger IIP3, the more margin for above blocking intermodulation rejection. From the system design point of view, the external front-end LNA linearity could limit the overall system linearity. This requires a careful design.

IF Operation and Image Rejection

In IF operation, the blocker at image frequency (desired frequency—2× IF) could be downconverted to the desired signal band after the mixer and could desensitize the receiver. The blocker image must be removed or suppressed to a low enough level to maintain the receiver performance. Figure 15 shows the blocker at the image frequency and rejection requirement. The blocking at the image frequency requirements could be classified to the spurious response rejection of DMR/TETRA standard shown in Figure 2 and Figure 3. For a DMR 70 dBc spurious response rejection and 7 dB SNR_{MIN} example, the receiver image rejection needs to be at least 77 dBc plus extra margins.

The traditional IF operation needs the sharp RF filters (Figure 4, BPFb) to filter the blocker at image frequency before the mixer and/or needs very high IF to be able to use a practical external filter (Figure 4, crystal BPF) to eliminate the blocker image before the second mixer.

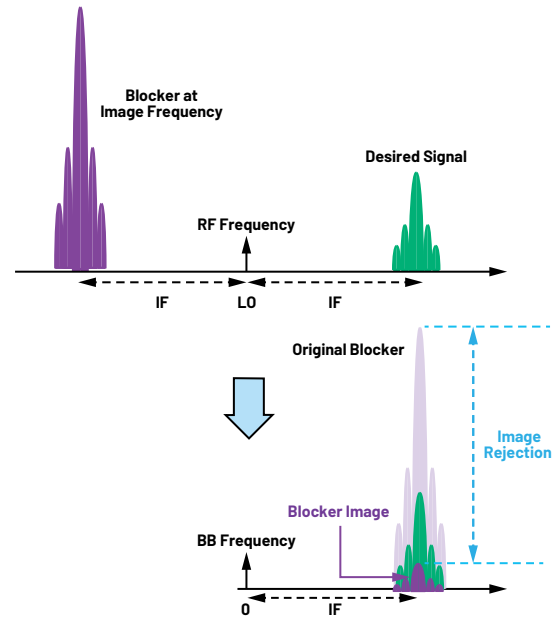

Figure 16. Blocker at image frequency and rejection.

The ADRV9002 image rejection algorithms balance I/Q; therefore, the blockers at image frequency could be removed in digital part of the ADRV9002. ADRV9002 provides around 90 dBc image rejection for NB signals in IF mode. Based on the previous calculation, this leaves a lot of margins to meet the DMR 70 dBc spurious response rejection requirements. At this performance level, the ADRV9002 doesn't necessarily need an external RF BPF (at least with reduced the external RF BPF requirements) for the image rejection. If more image rejection is needed for a system, ADRV9002 can be configured to high IF mode to create maximum space (~40 MHz) between the desired signal and the image; therefore, the external BPF can attenuate the blocker at image frequency. ADRV9002 provides flexible variable IF operation, and users can configure the IF based on their system requirement.

LO Phase Noise

Due to the LO phase noise and reciprocal mixing, the large blocker could degrade the receiver sensitivity. LO phase noise at offset frequency from blocker to desired channel should be low enough so reciprocal mixing components of receiver do not degrade the required SNR in the desired band. For the modulated blocker, the blocker can be modeled with CW tone at the center of the bandwidth and total power of the blocker to simplify the analysis. Figure 16 shows the LO phase noise requirement model. The phase noise requirement can be estimated by the following equation:

$$PN(\text{dBc/Hz at Freq. Offset}) < -P_{BLK\text{-}TO\ DESIRED}\ (\text{dBc}) - SNR_{MIN} - 10 \times Log10\ (BW) \quad (9)$$

where the $P_{BLK\text{-}TO\text{-}DESIRED}$ is a maximum tolerable blocker power above desired signal at given frequency offset.

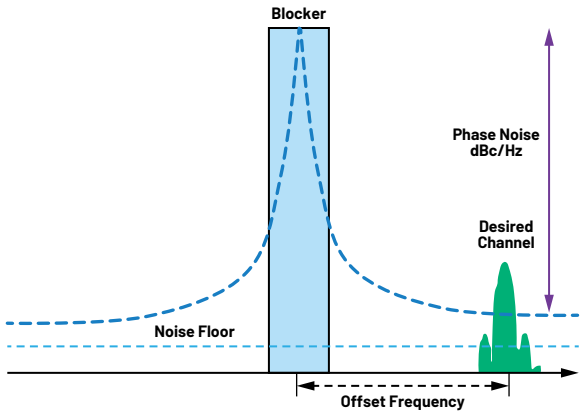

Figure 17. LO phase noise requirement model.

Using DMR as an example (7 dB SNR_{MIN}, 8 kHz BW), the blocker at 1 MHz requirement is 84 dBc. To meet the standard requirement, the LO phase noise at 1 MHz offset should be smaller than –130 dBc/Hz.

ADRV9002 provides integrated RF PLLs and VCOs with improved phase noise performace (see the phase noise plots in ADRV9002 data sheet). The LO phase noise at 1 MHz offset is –141.4 dBc/Hz for 470 MHz LO and –136.5 dBc/Hz for 900 MHz LO. The ADRV9002 internal LO is possible to meet the DMR standard blocking LO phase noise requirements.

ADRV9002 also provides the external LO input for the receiver to allow using external higher performances LOs to get higher blocking performance.

Conclusion

This article has shown how the ADRV9002 system with high DR and linearity design successfully meets challenging blocking needs for mission critical wireless applications. The highly integrated platform covers a wide range of bands and standards. Its least BOMs make it suitable for many uses.

References

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