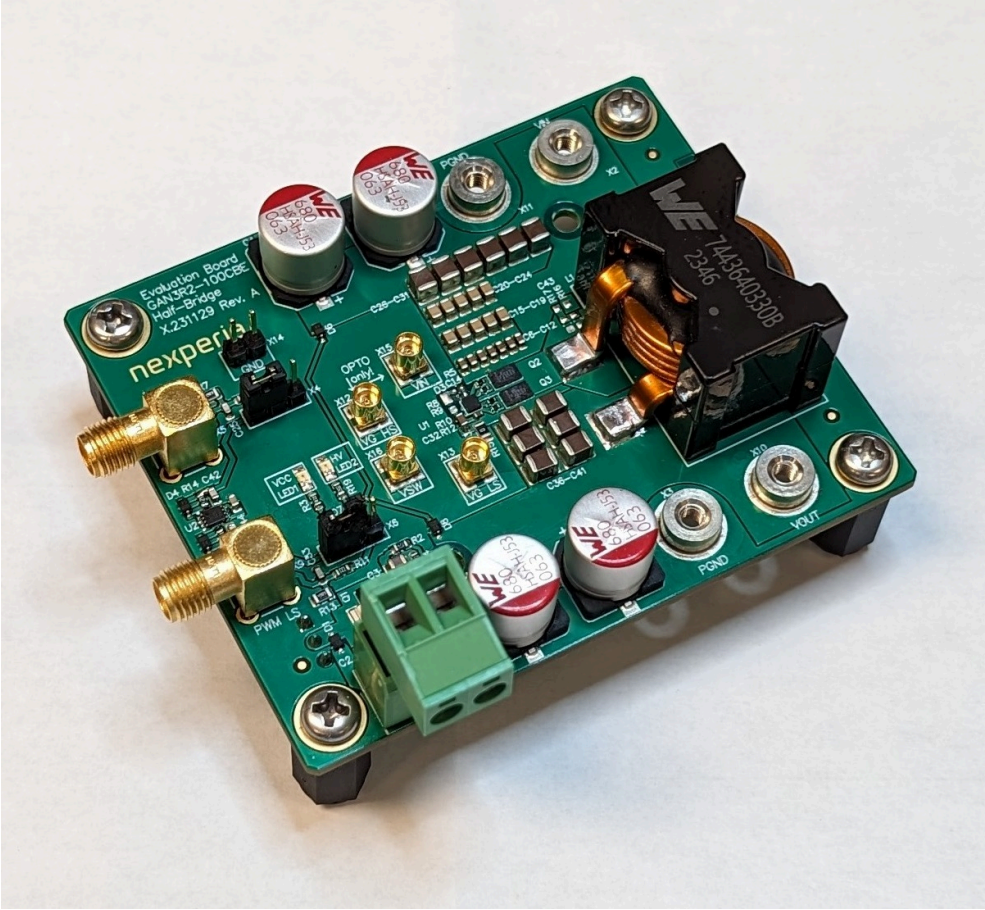
UM90038

Rev. 1.0 — 27 June 2024

User manual

NX-HB-GAN3R2-BSC half-bridge evaluation board



Abstract: The NX-HB-GAN3R2-BSC Evaluation Board is a half-bridge converter circuit using Nexperia power GaN FETs GAN3R2-100CBE. This user manual aims to support laboratory setup of the evaluation board and gives and an overview on testing capabilities and typical results.

Keywords: GaN FET, half-bridge, converter, evaluation board, WLCSP

nexperia

1. EVALUATION BOARD TERMS OF USE

The use of the Evaluation Board is subject to the Evaluation Board Terms of Use, which you can find here. By using this Evaluation Board, you accept these terms.

2. High Voltage Safety Precautions

Read all safety precautions before use!

Please note that this document covers only the NX-HB-GAN3R2-BSC half-bridge evaluation board and its functions. For additional information, please refer to the Product Specification

To ensure safe operation, please carefully read all precautions before handling the evaluation board. Depending on the configuration of the board and voltages used, potentially lethal voltages may be generated. Therefore, please make sure to read and observe all safety precautions described below.

Before Use:

It is recommended that ALL operation and testing of the evaluation board is performed with the board enclosed within a non-conductive enclosure that prevents the High Voltage supply to be switched whilst open and accessible; see Fig. 1.

Fig. 1. Example of a safety enclosure in the Nexperia lab

All probes should be positioned before turning on the High Voltage and should be held in place using a suitable probe positioner e.g. PMK MSA100; see Fig. 2.

Fig. 2. Example of a probe positioner

Always use an oscilloscope with protective earth connected.

When probing High Voltage, ensure that the probes have the correct voltage rating / limit.

Ensure that all scope probes are compensated and de-skewed before use, refer to your oscilloscope or probe manual for instructions on how to do this.

If possible, have a visual indicator of High Voltage located close to the evaluation board (LED bar graph or voltmeter) To show when the Bus Voltage (Vbus) and Outputs are at dangerous levels.

Verify that none of the parts or components are damaged or missing.

Check that there are no conductive foreign objects on the board.

If any soldering or modifications are made or carried out, then please ensure that this is done carefully so that solder splashes and debris are not created. Clean the board with Iso-propyl-alcohol and allow it to dry.

Ensure that there is no condensation or moisture droplets on the circuit board, all testing should be carried out within a dry environment without excessive humidity.

If used under conditions beyond the rated voltage and current specification, this may cause defects, failure and or permanent damage.

NEVER handle the evaluation board during operation under ANY circumstances

After use the Nexperia Evaluation Board contains components which may store high voltage and will take time to discharge. Carefully probe the evaluation board once the power has been removed to check that all capacitors have been discharged. You must do this without touching the board except for the multimeter probes that are being used to check.

This evaluation board is intended for use only in High Voltage Lab environments and should be handled only by qualified personnel familiar with all safety and operating procedures. We recommend carrying out operation and testing in a safe environment that includes restricted access only to trained personnel, the use of High Voltage signage at all entrances, safety interlocks and emergency stops and HV insulated flooring.

It should be noted that this evaluation board is intended to be used ONLY for evaluation purposes and should not be used by consumers or designed into consumer equipment in its current form.

2.1. Warnings

This demo board is intended to demonstrate GaN FET technology. While it provides the main features of a half-bridge converter, it is not intended to be a finished product and does not have all the protection features found in commercial power supplies.

⚠ CAUTION

BE AWARE

There is no specific protection against over-current or over-voltage on this board.

If the on-board pulse generation circuit is used in boost mode, a zero input corresponds to 100% duty cycle for the active low-side switch.

3. Introduction

The NX-HB-GAN3R2-BSC half-bridge evaluation board provides the elements of a simple buck or boost converter, see Fig. 3. This enables the basic study of the switching characteristics and efficiency achievable with Nexperia's 100V E-Mode GaN FETs. The circuit is configured for synchronous rectification, in either buck or boost mode. Selection jumpers allow the use of a single logic input or separate high / low level inputs. The voltage input and output can operate at up to 60 VDC, with a power output > 350 W.

The NX-HB-GAN3R2-BSC is for evaluation purposes only.

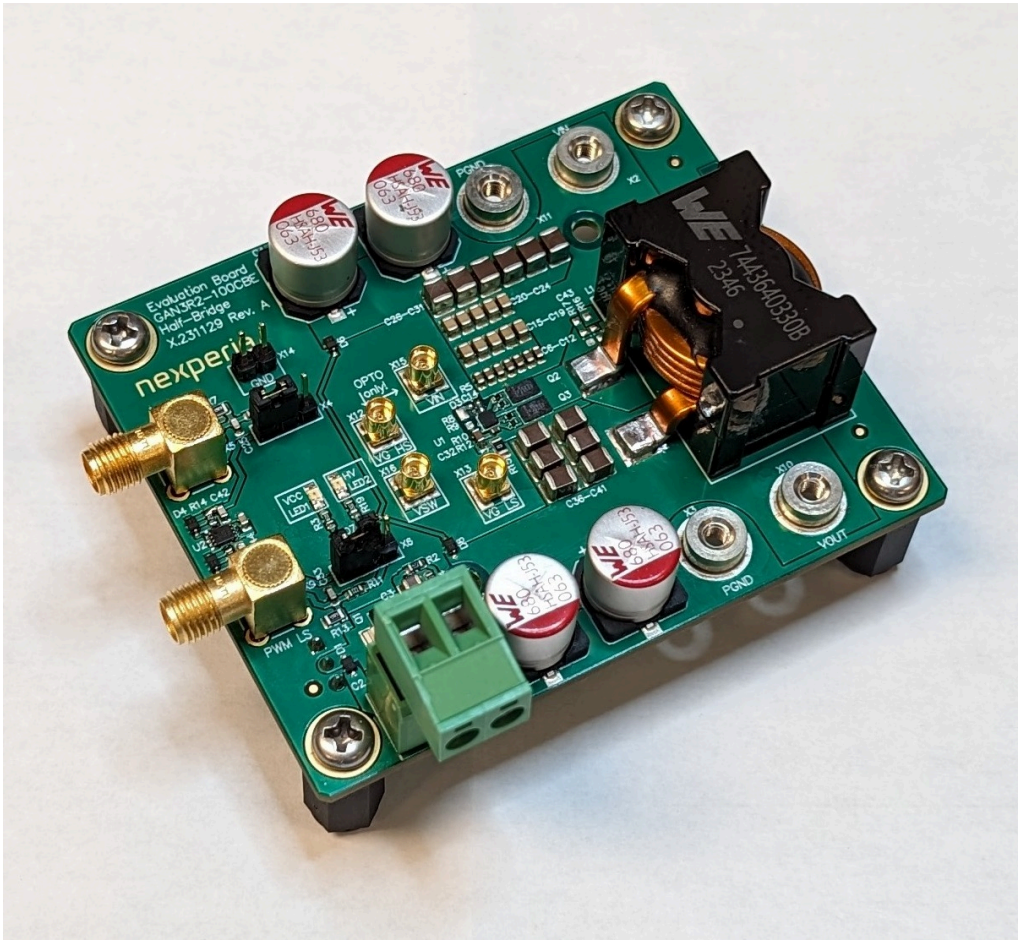


Fig. 3. NX-HB-GAN3R2-BSC half-bridge evaluation board

3.1. Quick reference information

Table 1. NX-HB-GAN3R2-BSC evaluation board Input/Output specifications

Parameter	Value
Input and output voltage	60 VDC max
GAN3R2-100CBE junction temperature	150 °C max
Maximum power	Depends on operation conditions, observe T_{case}
Auxiliary supply	12 VDC nom.; 50 mA
Logic inputs	Nominal 0 - 5 V; 50 Ω terminated SMA
• Pulse-generation circuit	V_{lo} < 1.5 V; V_{hi} > 3.5 V
• Direct connection to gate driver	Dependent on installed gate driver
Switching frequency	Configuration dependent

Power dissipation in the GaN FET is limited by the maximum junction temperature. Refer to the GAN3R2-100CBE data sheet.

4. Circuit description

The circuit comprises a simple half-bridge featuring two GAN3R2-100CBE GaN FETs, as indicated in the block diagram of Fig. 4. Two voltage ports are provided which can serve as either input or output, depending on the configuration: boost or buck. In either case one GaN FET acts as the active power switch while the other carries the freewheeling current. The latter device is enhanced as a synchronous rectifier. With GaN FETs the reverse recovery charge is low and there is no need for additional freewheeling diodes.

Two SMA input connectors are provided which can be connected to sources of logic-level command signals for the hi/lo gate driver. Both inputs may be driven by off-board signal sources, or alternatively, a single signal source may be connected to an on-board pulse-generator circuit which generates the two non-overlapping pulses. Jumpers determine how the input signals are used.

An inductor is provided as a starting point for investigation. This is a 6.8 µH inductor intended to demonstrate a reasonable compromise between size and efficiency at switching frequencies between 250 kHz – 750 kHz. There are alternative connectors available (X7/X8) that allow screw terminals for other inductor configurations and frequencies.

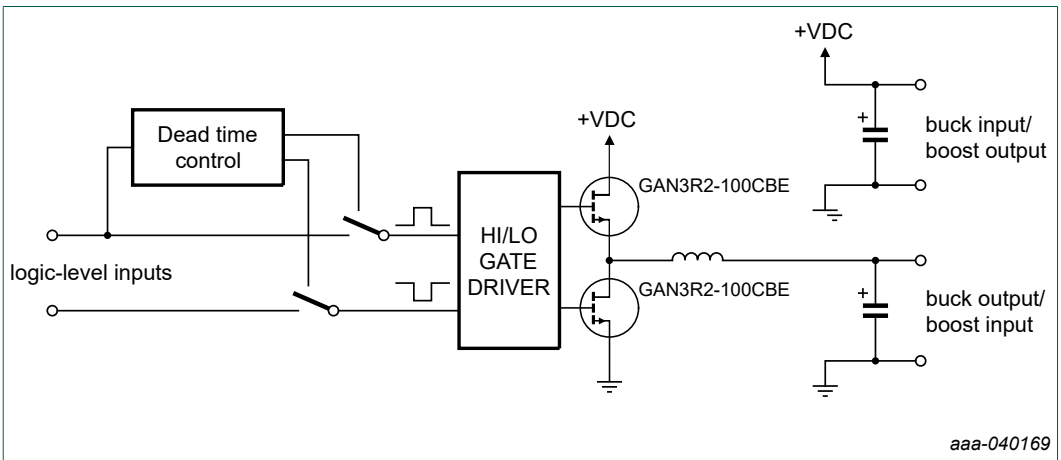
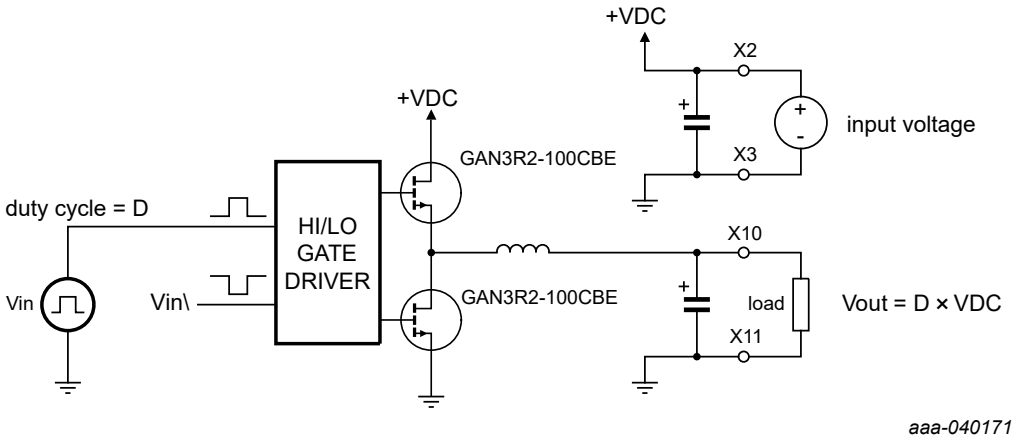


Fig. 4. Functional block diagram

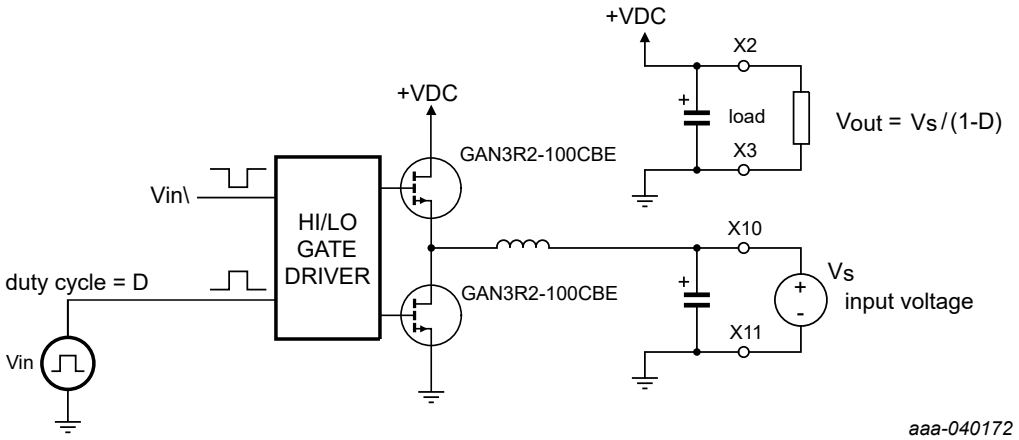
5. Configuration

5.1. Converter configuration

Fig. 5 shows the basic power connections for buck and boost modes. For buck mode, the DC input (terminals X2, X3) is connected to the voltage supply and the output is taken from terminals X10 and X11. For boost mode the connections are reversed.



(a) Buck Mode; see Fig. 6 regarding the complementary input



(b) Boost Mode; see Fig. 6 regarding the complementary input

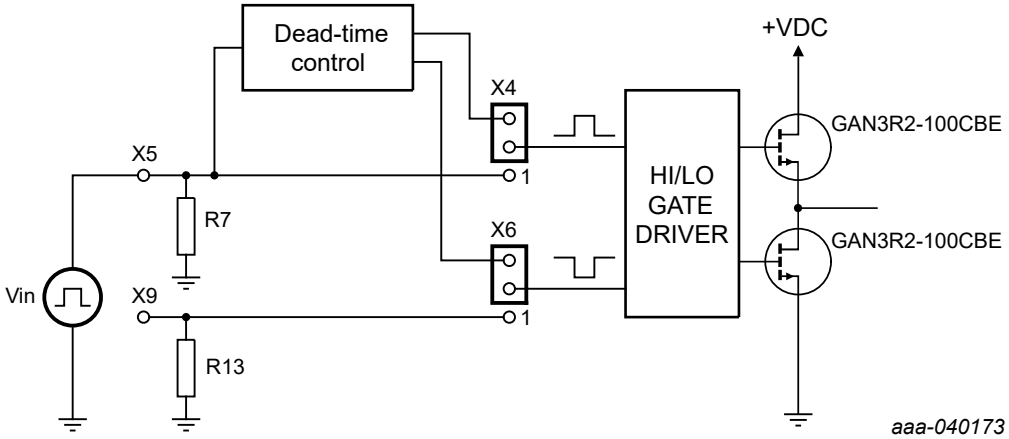
Fig. 5. Supply and load connections for Buck (a) and Boost (b) configurations

5.2. Pulse Width Modulation (PWM) input configuration

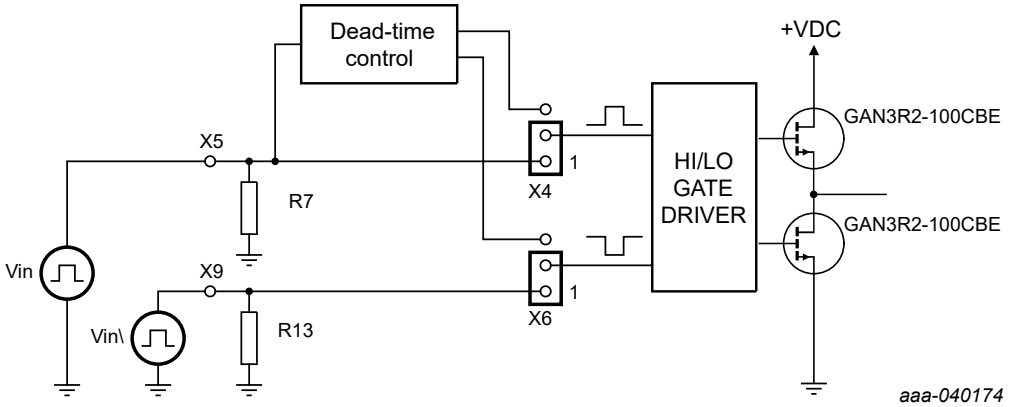
Fig. 6 shows possible configurations for the gate-drive signals. In Fig. 6 (a) a single input from an external signal source is used together with the on-board pulse generation circuit. X5 is used, X9 is left open circuit. Jumpers X4 and X6 are in the top position, as shown. If the high-side transistor is to be the active switch (e.g. buck mode), then the duty cycle of the input source should simply be set to the desired duty cycle (D). If the low-side transistor is to be the active switch (e.g. boost mode) the duty cycle of the input source should be set to (1-D), where D is the desired duty cycle of the low-side switch. This configuration results in synchronous rectification. Fig. 6 (b) shows use of two external signal sources as inputs to the gate driver.

For any configuration an auxiliary supply voltage of 12 V must be supplied at connector X1.

Resistors R7 and R13 are populated with 50 Ω to be used with a 50 Ω signal source. If a high impedance signal source is used, then R7 and R13 should be replaced with higher values (e.g. 10 kΩ).



(a) single signal source



(b) two signal sources

Fig. 6. Input configurations. (a) using a single source for either buck or boost mode (b) using two signal sources

5.3. Dead-time control

The required form of the gate-drive signals is shown in Fig. 7. The times marked A are the dead-times when neither transistor is driven on. The dead-time must be greater than zero to avoid shoot-through currents. The half-bridge GaN driver has no minimum dead-time or shoot-through protection. The on-board dead-time circuit can be adjusted by changing RC time constant of R14/C42 and R18/C45 respectively. The default population with 120 Ω/100 pF results in a dead-time at the gate pins of Q2 and Q3 of about 7 ns.

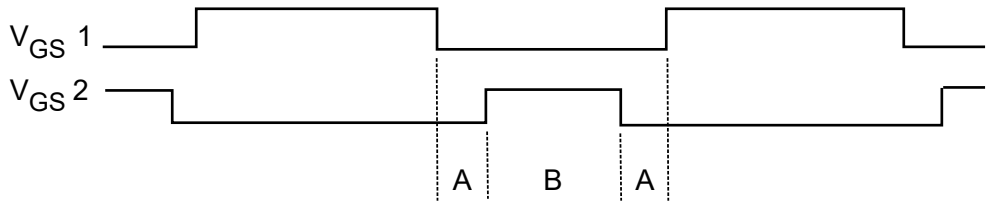


Fig. 7. Non-overlapping gate pulses

6. Probing

MMCX (Micro-Miniature Coaxial) connectors X12 and X13 are provided for probing Gate-Source signals, and X15 – X16 for probing Drain-Source signals for both high-side and low-side GaN FETs. Since X12 and X15 are referenced to the switch node, only isolated probes shall be used for these signals. X13 and X16 are both referenced to PGND and regular high-frequency passive probes can be used.

The probes and the oscilloscope should have a high bandwidth of at least 1 GHz so that all necessary details of the switching transitions can be captured. It is also crucial to take care of a proper de-skewing so that the delay times between different probes are compensated as much as possible.

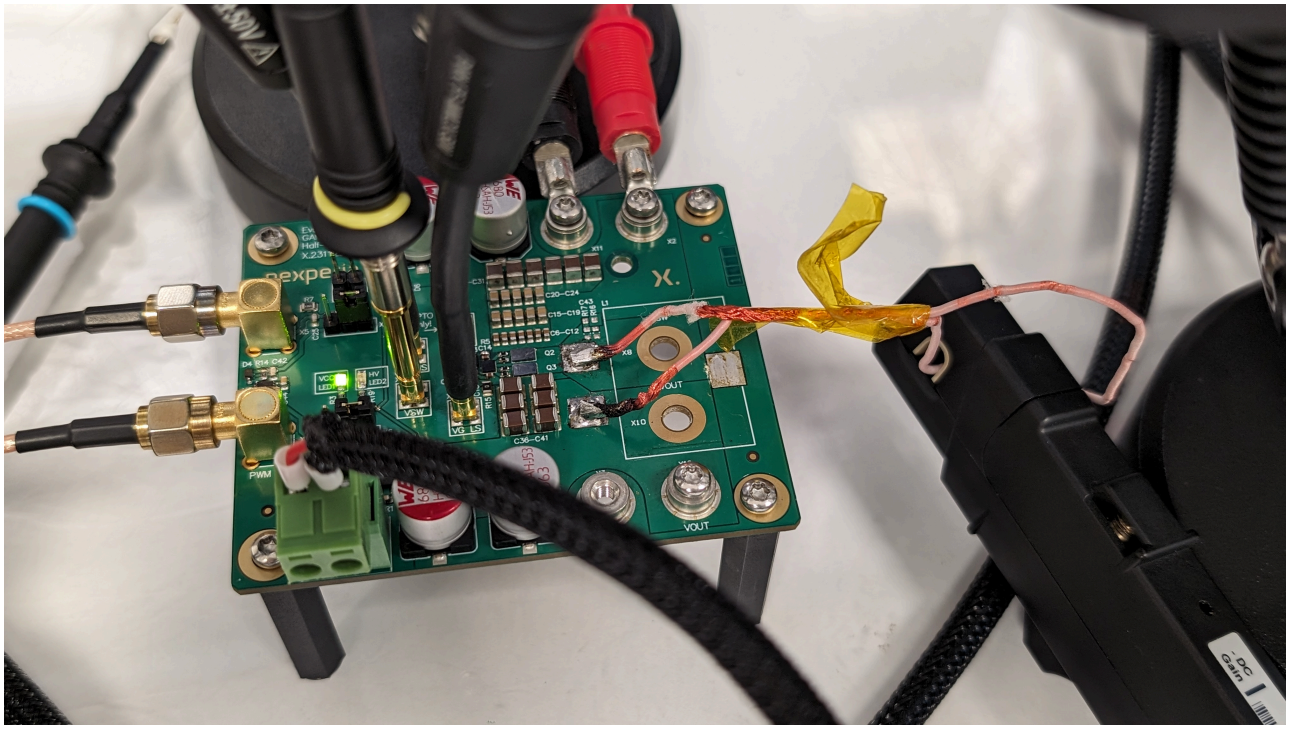


Fig. 8. MMCX connector probing with both passive and isolated probes. The inductor is replaced with a simple litz wire loop for soft switching measurements

7. Typical switching waveforms

7.1. Hard switching

For hard switching the half-bridge is used in a simple buck configuration with the following conditions:

- Load current = 20 A
- VIN = 48 V
- VOUT = 12 V
- f_{sw} = 750 kHz

The switching waveforms in the section below have been captured with passive and isolated probes directly connected to the MMCX connectors. Both have a bandwidth of at least 1 GHz. Fig. 9 and Fig. 10 show typical hard switching waveforms.

It is possible to estimate the commutation inductance of the board by measuring the ringing frequency at the switch node. Fig. 9 shows a ringing frequency immediately after turn on of about 347 MHz. In combination with an estimated total parasitic capacitance at the switch node of 20 pF, the total commutation loop inductance is calculated as:

$$\sum L_{loop} = \frac{1}{(2\pi \cdot f_r)^2 \cdot (C_{oss} + C_{par})} = \frac{1}{(2\pi \cdot 347\ MHz)^2 \cdot (460\ pF + 20\ pF)} \approx 440\ pH \quad (1)$$

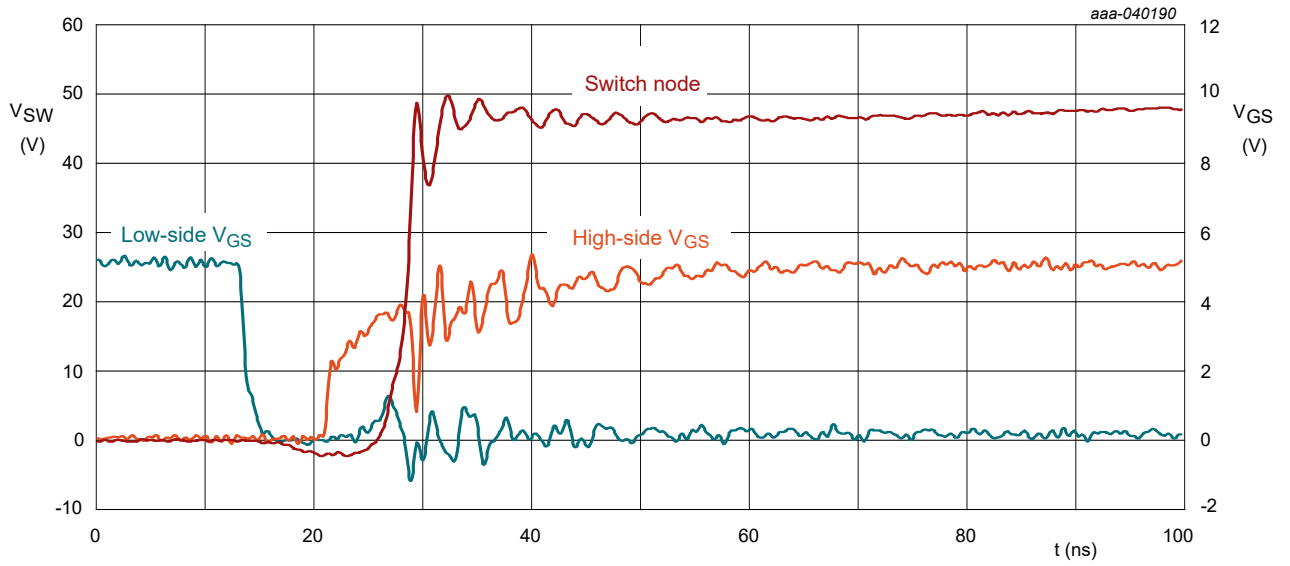


Fig. 9. Low-side turn off, high-side turn on

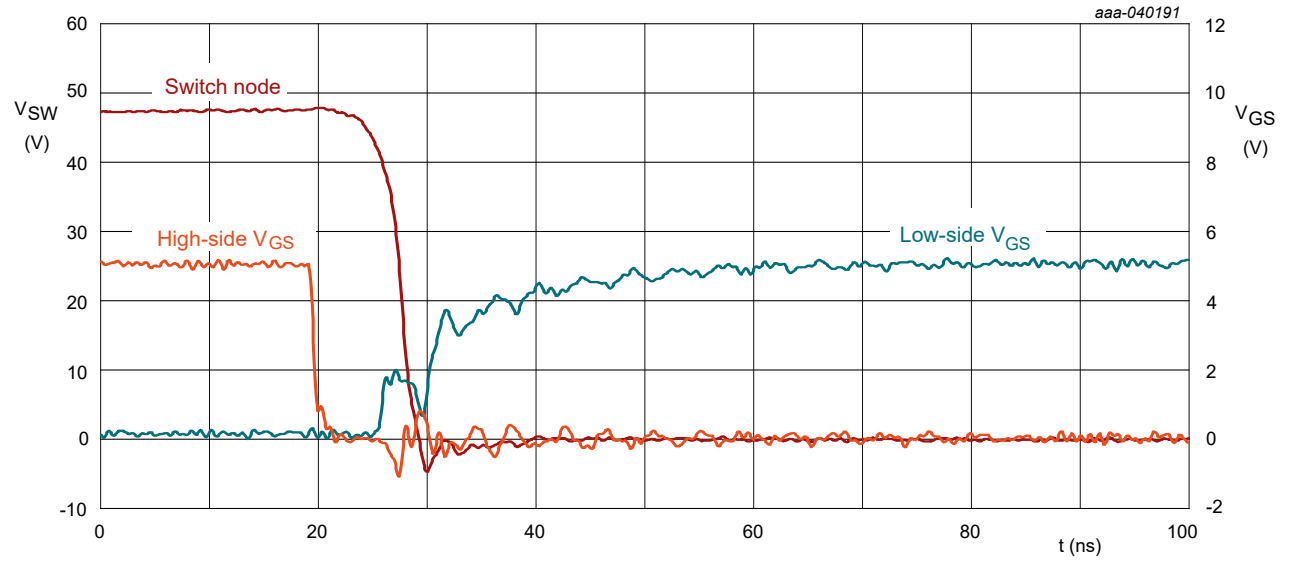


Fig. 10. High-side turn off, low-side turn on

7.2. Soft switching

For this setup, the inductor has been replaced with a simple litz wire loop (as shown in Fig. 8) and the duty cycle adjusted to 50% so that the output voltage is at half the input voltage. The switching frequency is set to 6.78 MHz which is often used for wireless charging.

In order to meet the soft switching criteria, there must be enough time to allow a complete charge/discharge of the output capacitance C_{oss} of the GaN FETs. This time depends on the available peak inductor current during the switching transition:

$$t_{swing} = \frac{2 \cdot Q_{oss}}{I_{pk}} \tag{2}$$

The dead-time between the high-side and low-side GaN FET is ideally the same time or slightly longer:

$$t_{dead} \geq t_{swing} \tag{3}$$

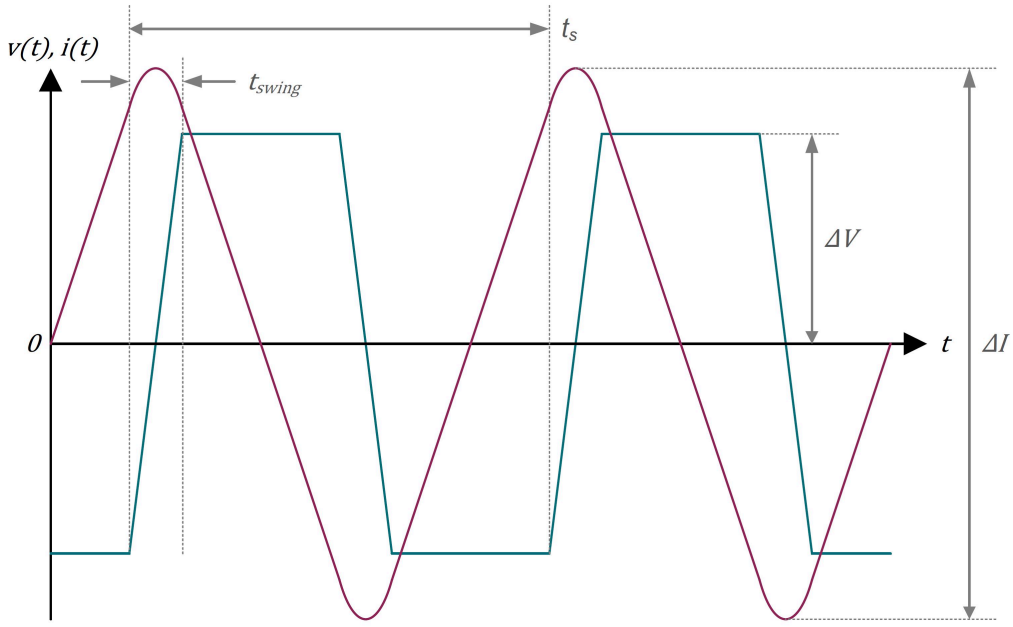


Fig. 11. Voltage and current soft switching waveforms across inductor

With a set dead time of 20 ns the peak inductor current must be at least:

$$I_{pk} = \frac{2 \cdot Q_{oss}}{t_{swing}} = \frac{2 \cdot 50\,nC}{20\ ns} = 5A \tag{4}$$

The relationship between the time-varying voltage *v(t)* across the inductor and the current *i(t)* passing through it is described by the differential equation:

$$v(t) = -L \cdot \frac{di(t)}{dt} \tag{5}$$

By rearranging the formula and with symbols from Fig. 11 the required inductance of the wire loop is:

$$L = \frac{\Delta V \cdot \left(\frac{t_s}{2} - \frac{t_{swing}}{2}\right)}{\Delta I} = \frac{24\ V \cdot \left(\frac{0.5}{6.78\ MHz} - 10\,ns\right)}{10\ A} \approx 150\,nH \tag{6}$$

Fig. 12 shows a typical soft switching waveform at 6.78 MHz.

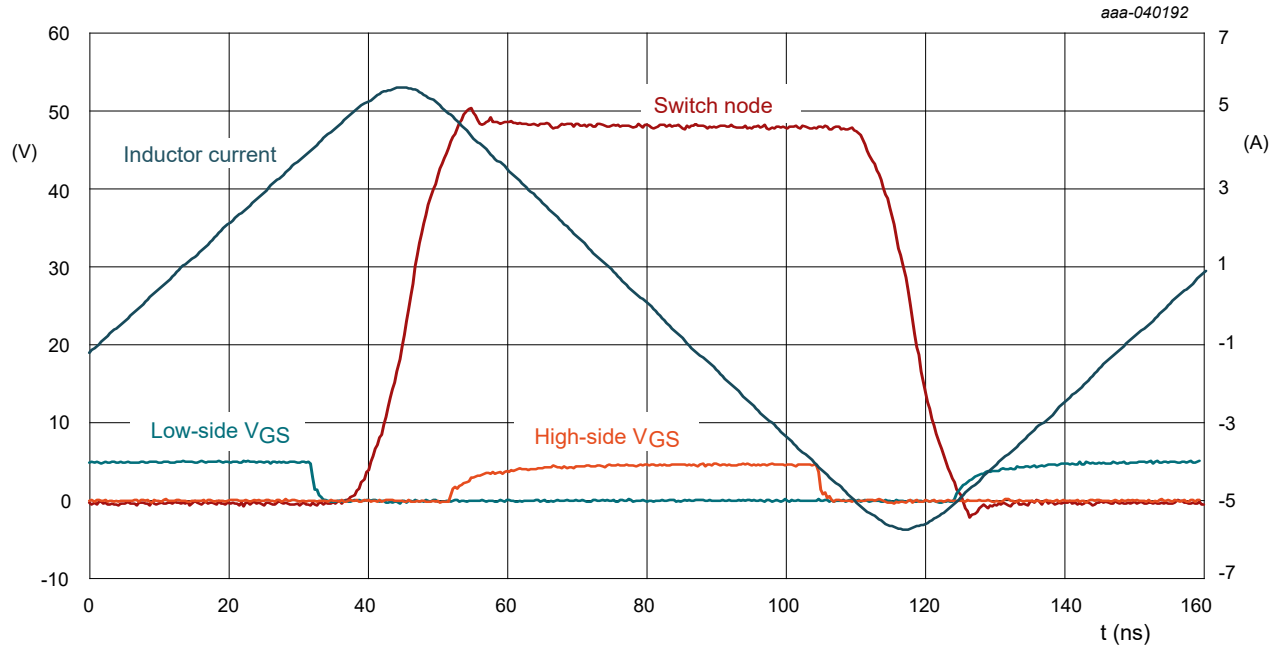


Fig. 12. Soft switching waveform at 6.78 MHz

8. Efficiency sweep

Efficiency has been measured for this circuit in buck mode with a 48 V input and 12 V output at various switching frequencies. To achieve a higher power rating, heatsink MP12 with a 12 V fan is installed. For efficiency measurements, a power analyzer is used, and its voltage sense connections are attached directly to the input and output power connectors of the board.

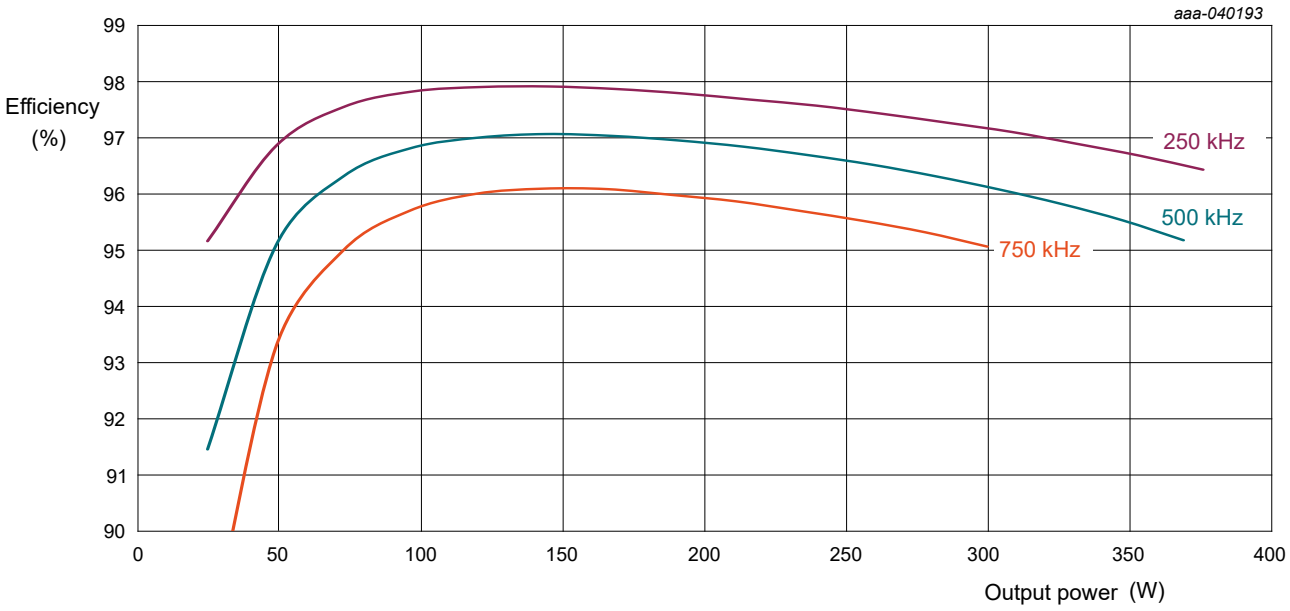


Fig. 13. Efficiency for a buck converter 48 V to 12 V

9. Design details

9.1. Schematic

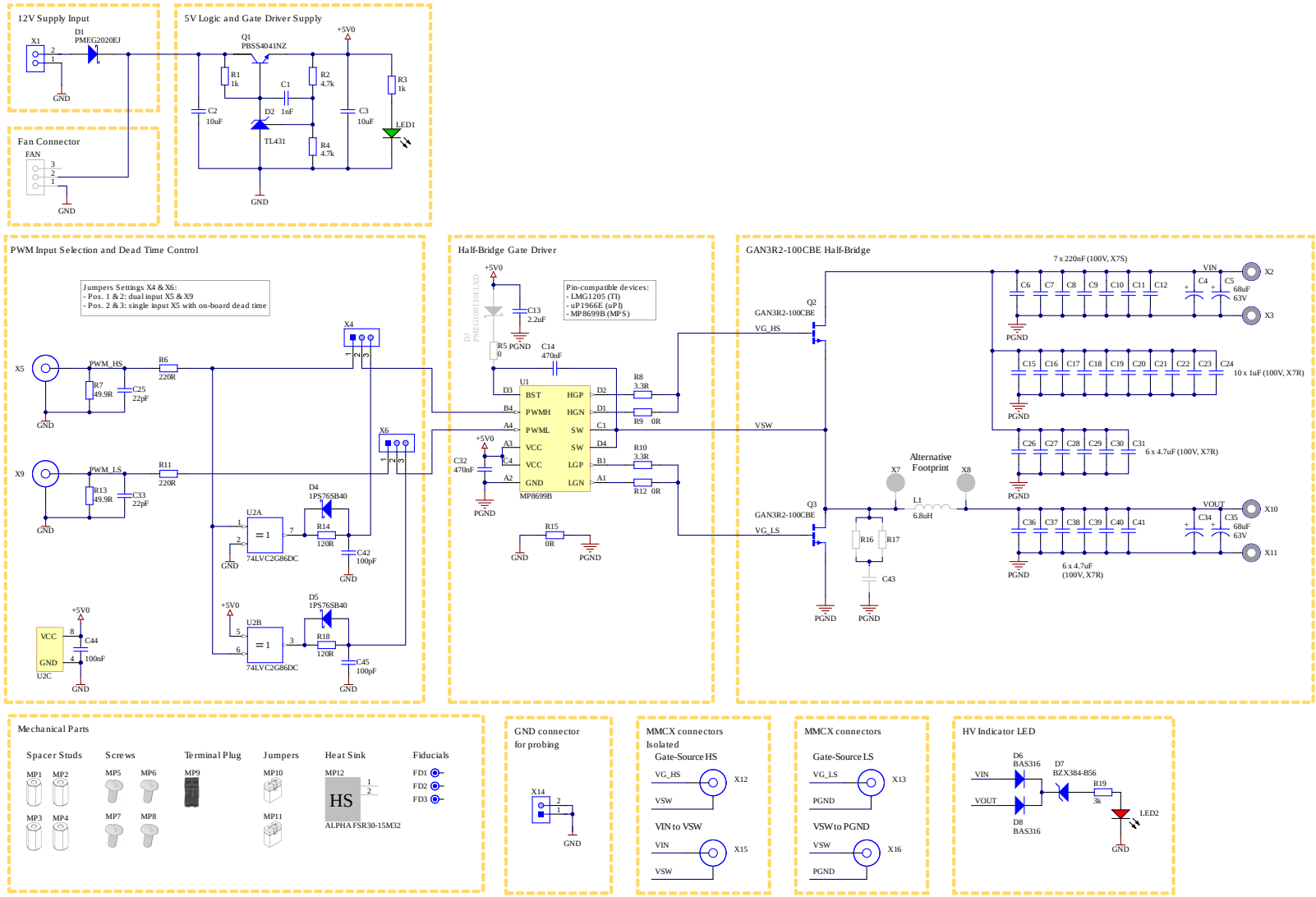


Fig. 14. NX-HB-GAN3R2-BSC schematic

9.2. NX-HB-GAN3R2-BSC PCB Layout

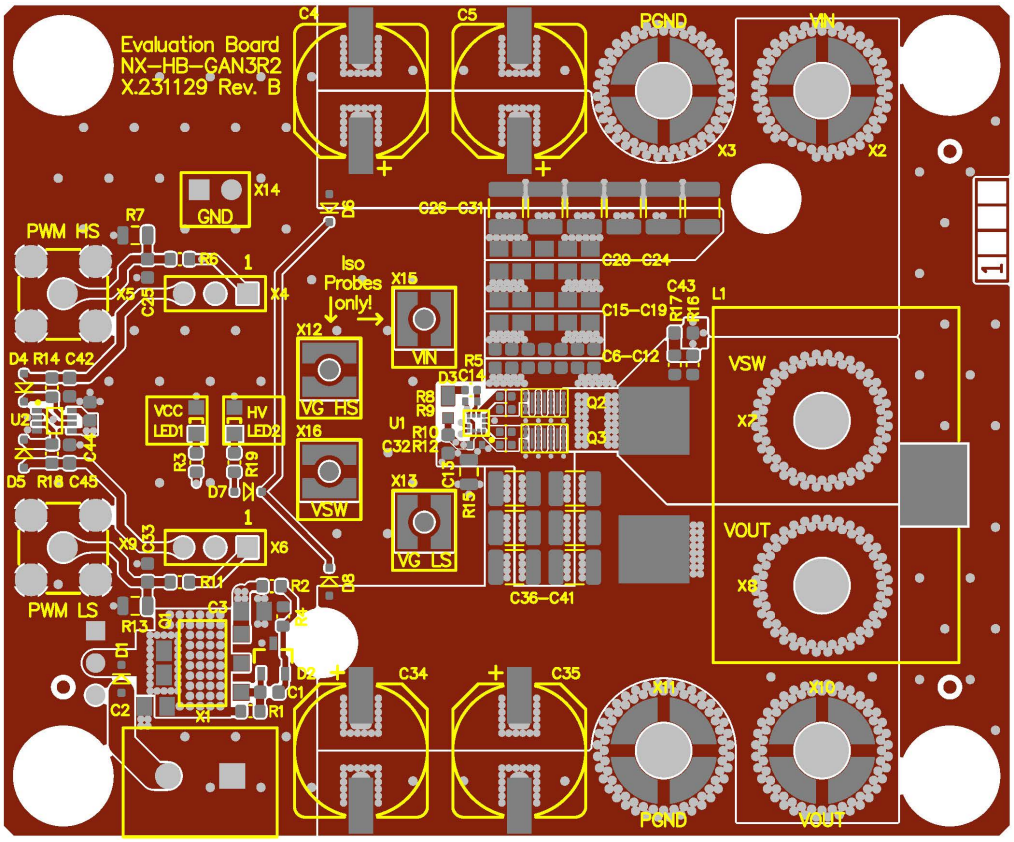


Fig. 15. NX-HB-GAN3R2-BSC PCB top layer

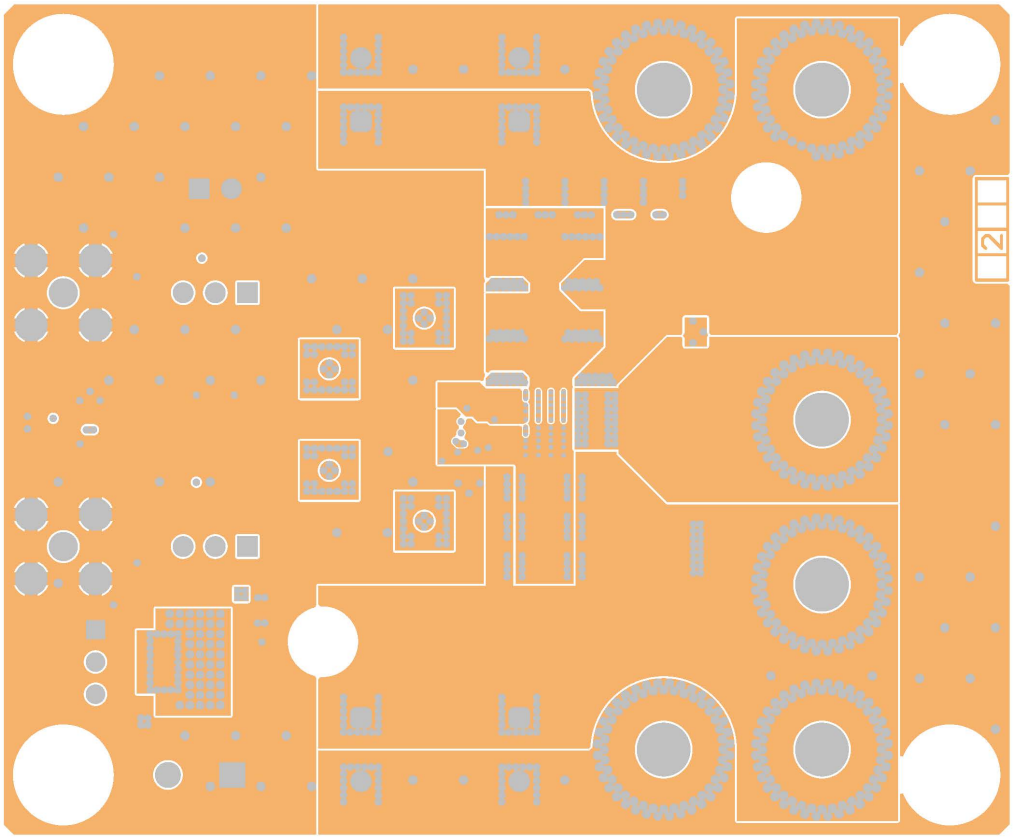


Fig. 16. NX-HB-GAN3R2-BSC PCB inner layer 1

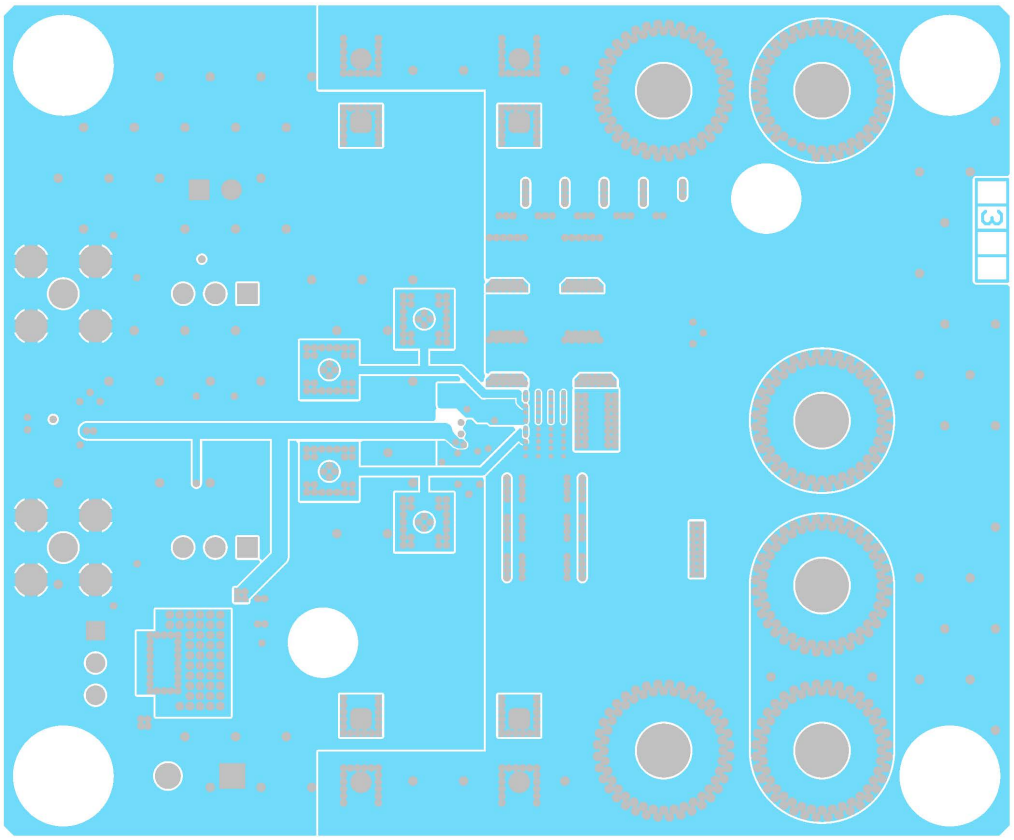


Fig. 17. NX-HB-GAN3R2-BSC PCB inner layer 2

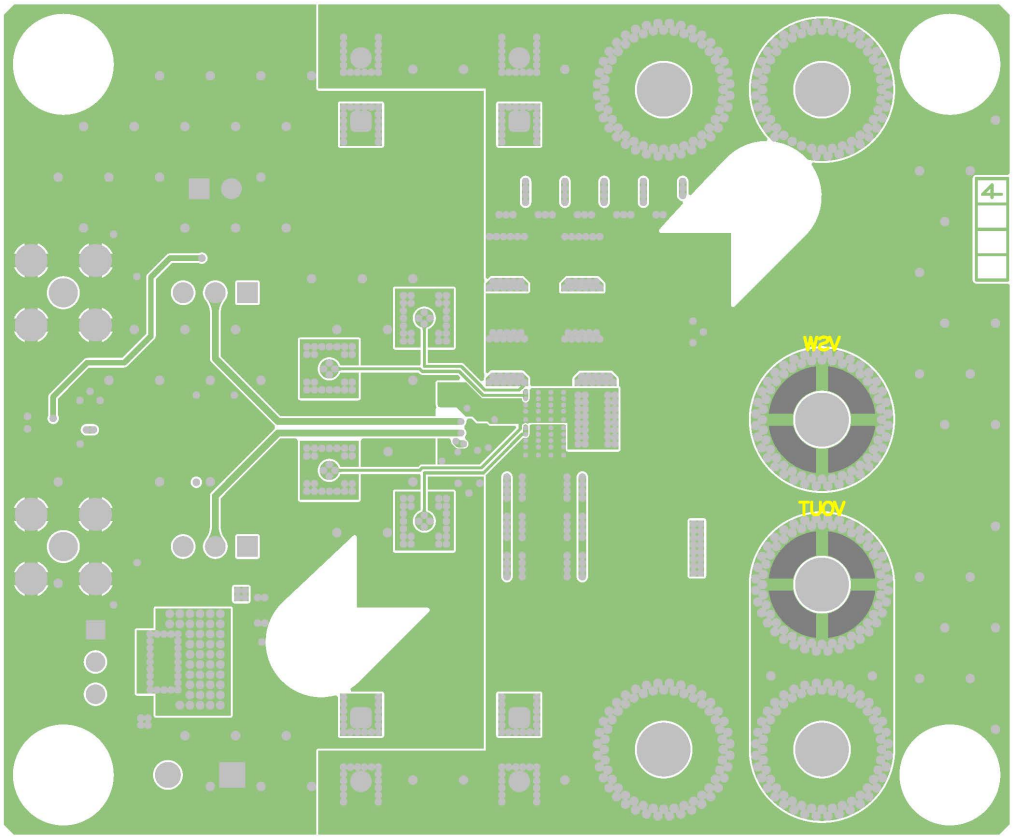


Fig. 18. NX-HB-GAN3R2-BSC PCB bottom layer

9.3. Bill of Materials

Table 2. NX-HB-GAN3R2-BSC evaluation board Bill of Materials

Designator	Qty	Description	Part Number	Manufacturer
C1	1	Ceramic Capacitor 1nF ±20% 50V X7R 0603	885012206083	Wurth Electronics
C2, C3	2	Ceramic Capacitor 10uF ±10% 25V X7S 0805		
C4, C5, C34, C35	4	Aluminum Hybrid Polymer Capacitor 68uF ±20% 63V SMD (10.3mm L x 10.3mm W x 10.5mm H)	875585857007	Wurth Electronics
C6, C7, C8, C9, C10, C11, C12	7	Ceramic Capacitor 220nF ±20% 100V X7S 0603		
C13	1	Ceramic Capacitor 2.2uF ±10% 25V X7S 0603		
C14, C32	2	Ceramic Capacitor 470nF ±10% 10V X7R 0402		
C15, C16, C17, C18, C19, C20, C21, C22, C23, C24	10	Ceramic Capacitor 1uF ±10% 100V X7R 0805		
C25, C33	2	Ceramic Capacitor 22pF ±5% 100V C0G 0603		
C26, C27, C28, C29, C30, C31, C36, C37, C38, C39, C40, C41	12	Ceramic Capacitor 4.7uF ±10% 100V X7R 1210	885012209072	Wurth Electronics
C42, C45	2	Ceramic Capacitor 100pF ±1% 100V C0G 0603	885012006079	Wurth Electronics
C44	1	Ceramic Capacitor 100nF ±20% 50V X7R 0603	885012206095	Wurth Electronics
D1	1	Schottky Diode 20V 2A SOD-323	PMEG2020EJ,115	Nexperia
D2	1	Adjustable Precision Shunt Regulator, 36V 100 mA SOT-23	TL431BFDT,215	Nexperia
D4, D5	2	Schottky Diode 40V 0.12A Low Cap SOD-323	1PS76SB40,115	Nexperia
D6, D8	2	Diode 100V 0.25A SOD-323	BAS316,115	Nexperia
D7	1	Zener Diode 56V SOD-323	BZX384-B56,115	Nexperia
L1	1	Fixed Ind 6.8UH 47.5A 0.968 Mohm	7443640680B	Wurth Electronics
LED1	1	LED Green 2V 20mA 0805	150080VS75000	Wurth Electronics
LED2	1	LED Uni-Color Red 630nm 2-Pin Chip 0805(2012Metric) T/R	150080RS75000	Wurth Electronics
MP1, MP2, MP3, MP4	4	WA-SPAII Plastic Spacer Stud, M4 Thread Internal, 15mm	970150485	Wurth Electronics
MP5, MP6, MP7, MP8	4	M4x0.7 Pan Head Machine Screw Phillips Drive Nylon	50M040070P008	Essentra
MP9	1	2 Position Terminal Block Plug, Female Sockets 0.200" (5.08mm) 180° Free Hanging (In-Line)	691351500002	Wurth Electronics
MP10, MP11	2	2 (1 x 2) Position Shunt Connector Black Open Top 0.100" (2.54mm) Gold	60900213421	Wurth Electronics
MP12	1	Heatsink with fan 30.00mm L X 30.00mm W X 15mm H	FSR30-15M32	Alpha

Designator	Qty	Description	Part Number	Manufacturer
Q1	1	TRANS NPN 60V 7A SOT223	PBSS4041NZ,115	Nexperia
Q2, Q3	2	GaN FET 100V 3R2 mOhm WLCSP (SOT8072)	GAN3R2-100CBEAZ	Nexperia
R1, R3	2	Chip Resistor 1k ±1% 0.1W 0603		
R2, R4	2	Chip Resistor 4.7k ±1% 0.1W 0603		
R6, R11	2	Chip Resistor 220R ±1% 0.1W 0603		
R7, R13	2	Chip Resistor Anti-Surge 49.9R ±1% 0.4W 0805	ESR10EZPF49R9	Rohm
R8, R10	2	Chip Resistor 3R3 ±1% 0.2W 0402	CRCW04023R30FKEDHP	Vishay Dale
R9, R12	2	Chip Resistor 0R Jumper 0402		
R14, R18	2	Resistor 120R ±1% 0.1W 0603		
R15	1	Chip Resistor 0R Jumper 0805		
R19	1	Chip Resistor 3k ±1% 0.1W 0603		
U1	1	Half-Bridge GaN Driver 100V, 1.7A, 5.2A, WLCSP-12 (2.0mm x 2.0mm)	MP8699BGC-CFC7	MPS
U2	1	DUAL 2-IN EX-OR GATE	74LVC2G86DC,125	Nexperia
X1	1	2 Position Terminal Block Header, Male Pins, Shrouded (4 Side) 0.200" (5.08mm) Vertical Through Hole	691311500102	Wurth Electronics
X2, X3, X10, X11	4	TERMINAL REDCUBE M3 SMD	746600330R	Wurth Electronics
X4, X6	2	Connector Header Through Hole 3 position 0.100" (2.54mm)	61300311121	Wurth Electronics
X5, X9	2	SMA Connector Right Angle PCB Jack 50Ohms	60311002111526	Wurth Electronics
X12, X13, X15, X16	4	MMCX Connector Jack, Female Socket 50Ohm Surface Mount Solder	66012102111404	Wurth Electronics
X14	1	Connector Header Through Hole 2 position 0.100" (2.54mm)	61300211121	Wurth Electronics

10. Revision history

Table 3. Revision history

Revision number	Date	Description
1.0	2024-06-27	Initial version.

11. Legal information

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Date of release: 27 June 2024