# Public GMSL3 Hardware Design and Validation Guide

# UG-2208

Rev 2; 8/25

ANALOG DEVICES

# Purpose and Scope

The *GMSL3 Hardware Design and Validation Guide* presents industry standard best practices for designing a high-speed system using GMSL3 products. This guide provides various techniques to optimize high-speed hardware design and guidance for hardware validation. Special consideration is given to schematic design and PCB layout to ensure optimized GMSL3 link performance.

The *GMSL3 Hardware Design and Validation Guide* is not a data sheet. This document describes important system design considerations and should be used as a reference for system development and component evaluation. Specifications for GMSL3 products are only guaranteed by their respective data sheet(s). Contents of this document are subject to change at any time and without notice. Users are responsible for the evaluation and validation of their systems utilizing GMSL3 devices.

# GMSL3 Overview

The GMSL3 devices use Analog Devices, Inc.'s proprietary third-generation Gigabit Multimedia Serial Link (GMSL) technology to transport high-speed serialized data over coax or shielded twisted-pair (STP) cable for automotive camera and display applications.

**Note**: The forward channel is defined as serializer-to-deserializer transmission; the reverse channel is defined as deserializer-to-serializer transmission.

The GMSL3 links operate at fixed data rates: 12Gbps, 6Gbps, or 3Gbps in the forward channel direction and 187Mbps in the reverse channel direction (depending on device capabilities and configuration).

A block diagram of a typical GMSL3 system is shown in *Figure 1*.

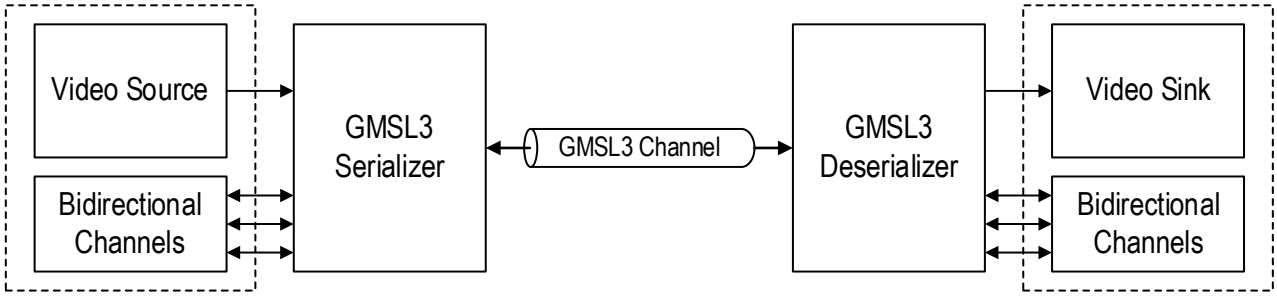



***Figure 1. GMSL3 System Block Diagram***

# Hardware Recommendations and Best Practices

This section provides schematic and layout guidance for designing PCBs with GMSL3 serializers or deserializers.

## Schematic Entry

This section provides schematic design entry guidance.

### Schematic Checklist

- All power pins have the recommended decoupling capacitors with correct voltage tolerance.
- Single-ended links have proper termination on the unused SIO pin. Refer to the data sheet for details.
- Correct series AC coupling capacitor is selected for GMSL3 operation.

- Pull-up resistors on $I^2C$/UART lines are used and appropriately sized.
- GPO pins with open-drain drives have pull-up resistors.
- Crystal or oscillator is properly connected.
- XRES is 402Ω with 1% tolerance (if applicable). Refer to the device data sheet for more information.
- Correct CFG pin resistor-divider values are used for desired power-up mode.
- Input/output video interface is correctly connected.
- Serial-peripheral interface (SPI) and $I^2S$ are correctly connected.
- Check application requirement for AECQ level.
- Use a recommended Power-over-Coax (PoC) circuit or verify a new PoC circuit.
- PoC minimum and maximum voltage need to meet all system requirements.

## AC Coupling and Termination

Any active PHY needs to have both outputs terminated and/or matched to 50Ω (and AC coupled). This is because the output is differential, and if one side is terminated and the other is not, there is a common mode shift that can potentially cause electromagnetic interference (EMI) issues, and link performance degradation. Detailed termination recommendations are shown in the following sections.

For the serializer, in order to minimize the reflection effect, it is recommended to have AC capacitor as close as possible to the pin, usually less than half of a bit rate distance from TX. Note that half UI for 6Gbps signal is approximately a half inch/500mil, which is the maximum distance from the IC that Analog Devices recommends for the AC capacitor placement.

-Coax Application

- In Coax applications, positive SIOP side should usually be used as default path, however this is not true for all devices. Refer to the data sheet for details.
- Use appropriately sized AC capacitors.
- Negative SION side should be terminated with 100nF capacitor and 50Ω to ground.
- Recommended to use 0402 capacitors. Larger capacitors can cause impedance mismatches degrading performance.
- Ensure the AC capacitor is rated above the PoC voltage (including tolerances) to ensure capacitor does not degrade and negatively affect the link integrity.
- See *Figure 2* for coax termination scheme.

-STP Application

- In STP application, both positive SIOP and negative SION pins should be used.
- 100nF AC coupling capacitors should be used on both traces.
- See *Figure 3* for STP termination scheme.

**Table 1. GMSL3 AC Coupling Capacitor Value**

| Configuration | PoC | AC Coupling Capacitor |
|---|---|---|
| **GMSL3** | X | 100nF |

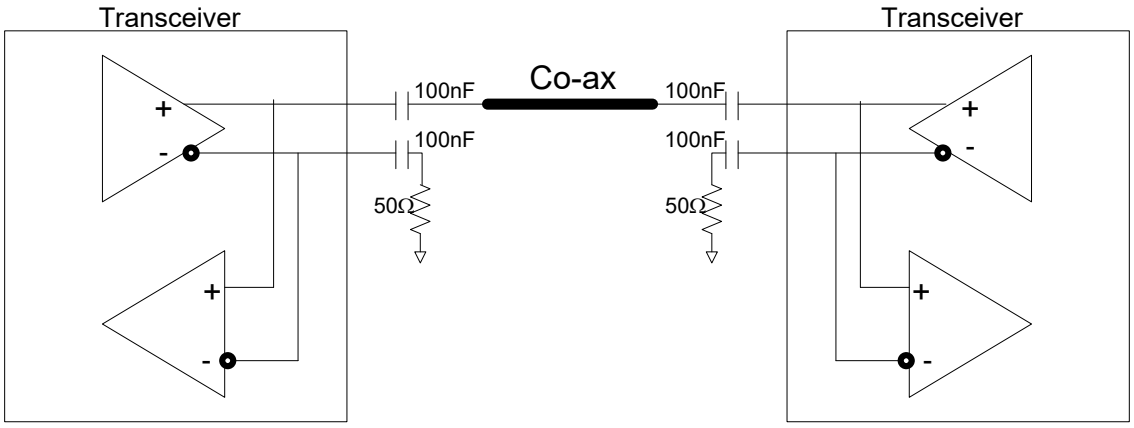



***Figure 2. Typical Coax Termination Scheme ("+" and "–" May be Swapped Depending on the Device)***

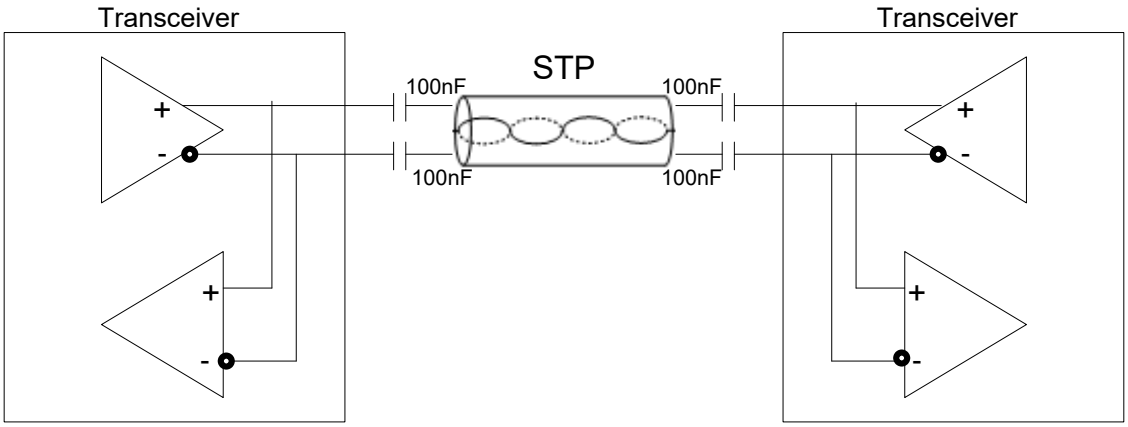



***Figure 3. STP Termination Scheme***

-Unused PHY Termination

If a PHY (SIOA, SIOB, SIOx, etc.) is not being used, it can be left floating only if the PHY is turned off through register settings. Leaving the PHY (SIOA, SIOB, SIOx, etc.) floating reduces BOM content and cost.

If unused PHYs are still enabled through register settings, then PHY pins should be terminated with 100nF capacitor and 50Ω to GND.

## PCB Layout Recommendations

This section provides PCB layout design guidance.

### Key PCB Requirements

- Minimize trace length to pass GMSL3 PCB channel insertion loss specification.
- Minimize impedance discontinuities and the number of components on high-speed traces.
- Use GND cutouts where necessary.
- Simulate and measure PCB performance to ensure a robust link.

- Maintain characteristic impedance.

## Proper Layout Techniques

Proper high-speed printed circuit board (PCB) layout is required to meet the GMSL3 PCB channel specification to ensure robust GMSL3 link operation. The layout of the serial link traces must be carefully designed to provide optimal signal integrity by minimizing impedance discontinuities and noise coupling. The layout of the serial link trace must follow high-speed layout practices:

- Route the serial link trace as a microstrip on the top layer or as a stripline in a middle layer if EMI/electromagnetic compatibility (EMC) is a concern.
- Use 100Ω differential or 50Ω single-ended trace routing with impedance control of ±5%.
- Minimize impedance discontinuities by using proven design and simulation practices.
- Place IC as close as possible to the connectors to minimize trace length.
- Minimize vias. If vias are required, eliminate via stubs by using back drilled vias and add ground transition vias next to signal vias.
- Place AC coupling capacitors on the top layer as close to the IC as possible (within 500mils ensures it is less than 0.5UI from the transmitter). Route signal differentially to the AC coupling capacitors, even in Coax mode. Ensure 100Ω impedance and length matching to the AC capacitors.
- In Coax mode, terminate the SION trace with an AC coupling capacitor and 50Ω resistor to ground.
- In STP mode, ensure length matching and consistent coupling distance between traces.
- Eliminate stubs by placing component pads directly on the high-speed trace, including line fault, PoC, and ESD components.
- Use ground cutouts under the pads of components that are on the high-speed trace.
  - GMSL3 IC SIOP/N pins, PoC and line fault components and ESD devices.
  - The size of these cutouts depends on the specific PCB stackup. For example, the cutouts for Analog Devices EV kits are 1.35x the pad size.
- Follow connector vendor layout footprint recommendations.
- For through-hole connectors, use topside mounting of IC and bottom-side mounting of connector to minimize connector pin stubs to improve return loss.
- Avoid 90-degree bends on high-speed lines.
- Maintain a continuous reference plane under high-speed trace. There should be no split ground or power planes under the serial link trace (except ground cutouts).
- ESD protection should be placed near the RF connector if required for application (and PoC is not used).
- Use an array of ground vias in the exposed ground pad (EP) for thermal management.
- High-speed video interfaces (e.g., HDMI, OLDI, DP, eDP/DP, DSI, CSI C-PHY, CSI D-PHY) and other high-speed interfaces (e.g., SPI) all have their own layout requirements and impedance specifications, length matching tolerances, and maximum trace lengths. Follow the guidance given in each specification.
- Maintain pair-to-pair and signal-to-signal distances for high-speed signals to reduce crosstalk.
- Ensure differential pair-to-pair distance is at least 2x separation away.
- Ensure single-ended signals are at least 3x trace width away or isolate on a different layer.

### Ground Cutout on 50Ω GMSL3 Trace

To avoid ground cutouts, it is recommended to try to select a stackup such that the trace width for the target impedance (50Ω single ended or 100Ω differential) matches the largest component pad size. This would eliminate the need to have ground cuts around the components. In many cases, this is not possible due to certain design constraints, so it is recommended to follow the given guidelines to help minimize impedance mismatches.

When a component's pad is larger than the serial link trace, a ground cutout is needed. The size of the ground cutout depends on the board stackup and the size of the component pad. For example, in the following layout a 0402 component is used with a 1.35X ground cutout and ~0.3mm spacing to the adjacent ground. This design is using a 12mil ~0.305mm trace for a 50Ω match with an adjacent ground layer spaced approximately 6mils from the trace.

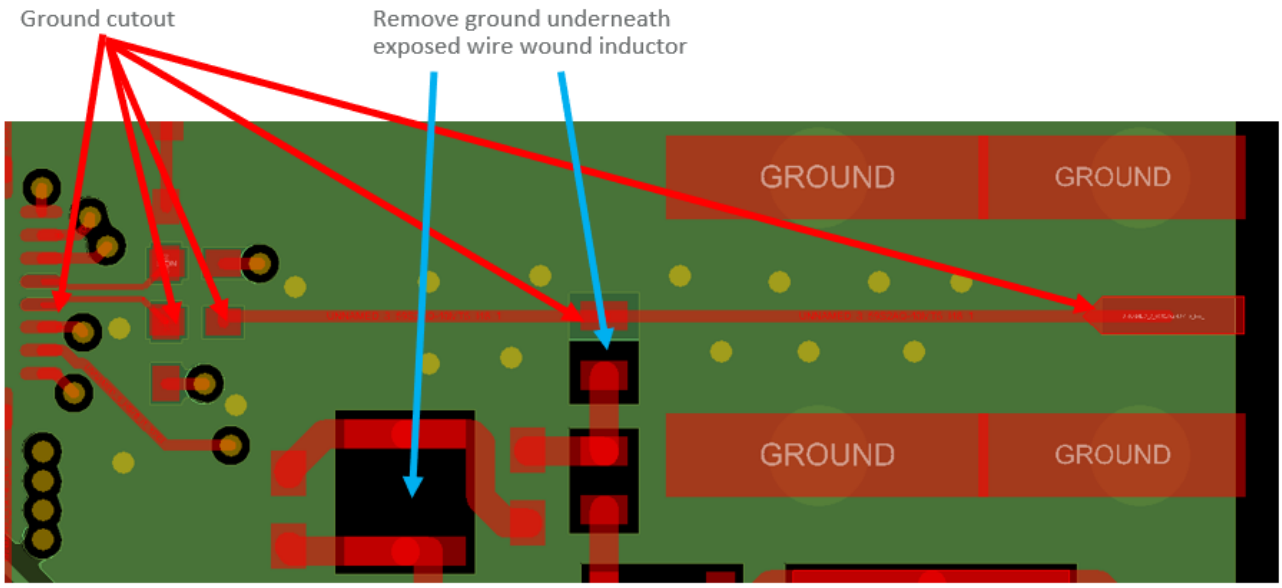



***Figure 4. PoC Layout Example Showing Single-Layer Ground Cutouts under the IC Pad, AC Coupling Cap, First PoC Component, and Fakra Connector Pad. Full Board Cutout is Shown under the Wire-Wound Inductors***

Proper impedance matching requires ground cutouts below components that have a bigger pad size than the matched 50Ω trace. It is highly recommended to perform a high-speed simulation to determine the proper depth and width of the ground cutout for the design.

**Determining Ground Cutout Depth**

When matching a 50Ω trace to a dense PCB stackup, a small trace size is typically needed, which creates a discontinuity when the matched trace reaches the large component pad. To compensate for this mismatch in impedance, it is recommended to remove adjacent ground layers to effectively lower the capacitance below the component pad. To confirm the ideal distance, Analog Devices recommends running a simulation.

## Layout Examples

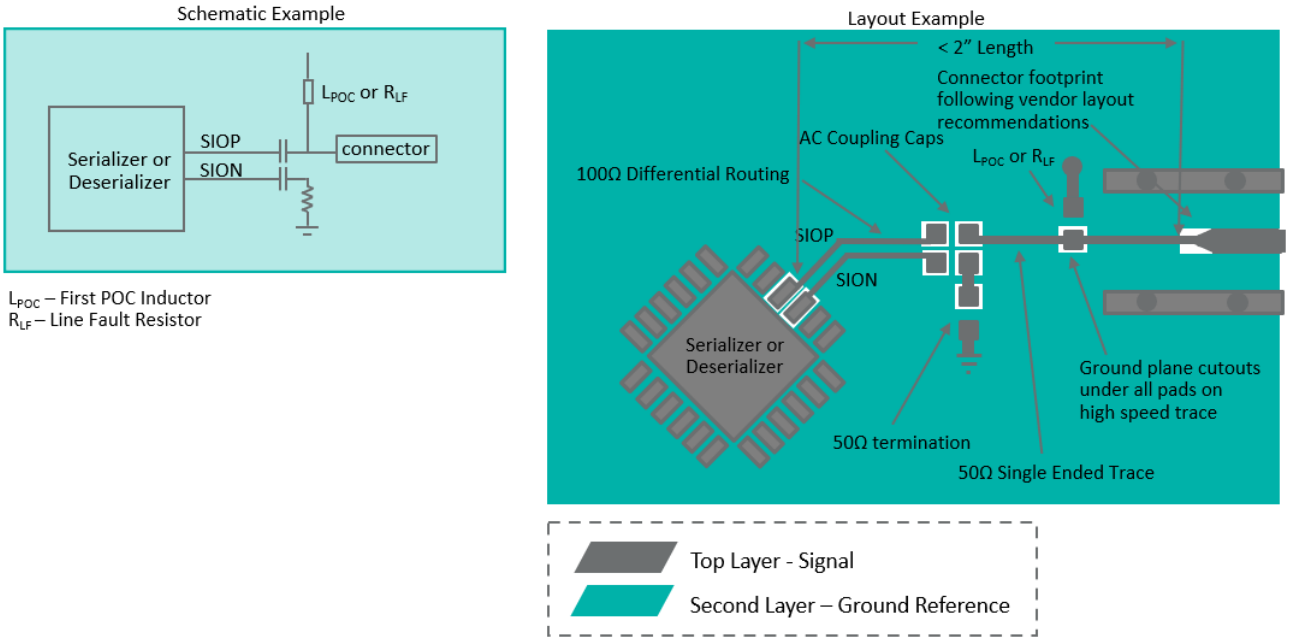



***Figure 5. Schematic and Layout Example for Single-Ended (Coax) Operation***

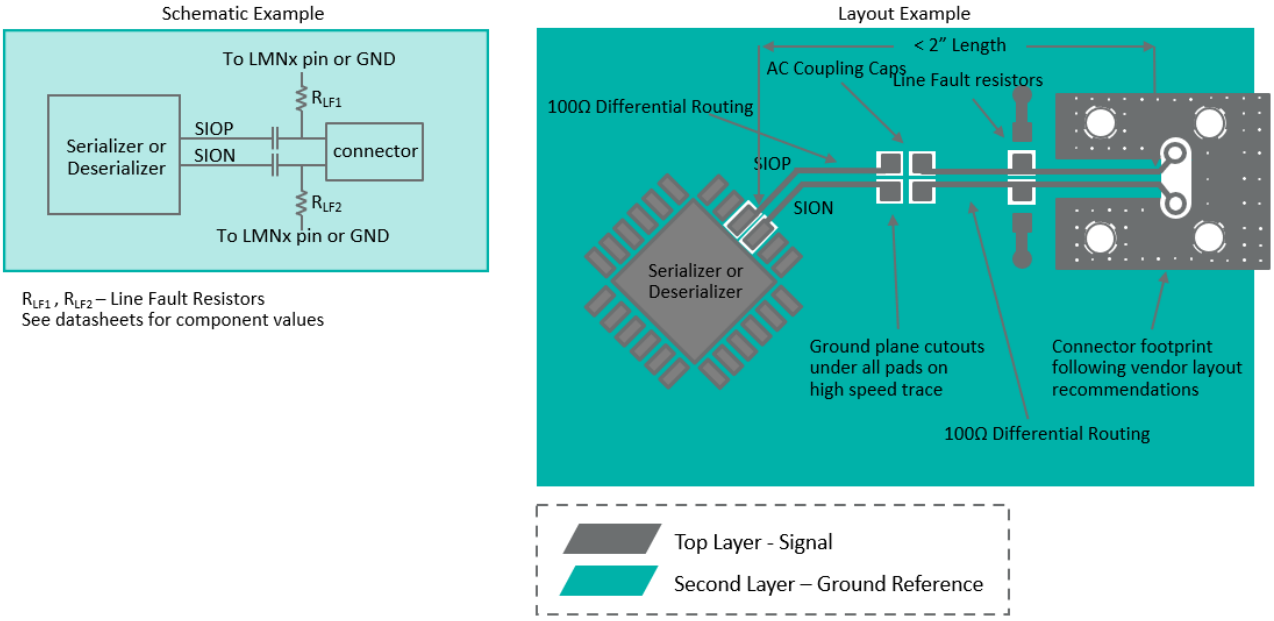



***Figure 6. Schematic and Layout Example for Shielded Twisted-Pair Operation***

## Skew Management

Skew management is a critical part of high-speed signal PCB layout. Propagation delay between differential pair can significantly degrade the signal integrity and increase common mode noise and EMI. Delay skews between clock and data signals need to be carefully controlled for optimal signal integrity. Differential twisted pair GMSL3 links are recommended to have less than ±5mils of skew. Note that for different cables and connectors, there may be intra-pair skews already introduced in the cable and connector, which needs to be taken into consideration when calculating overall channel skew. Check with connector vendor for more details on specific connectors. An example of this can be seen in the HSD footprint recommendation in the *Connectors* section. For video interfaces, such as CSI, eDP/DP, OLDI, HDMI, it is strongly recommended to limit length differences to ±5mils for inter-pairs (between separate differential pairs) and intra-pairs (within a single differential pair).

### Differential EMI Improvements

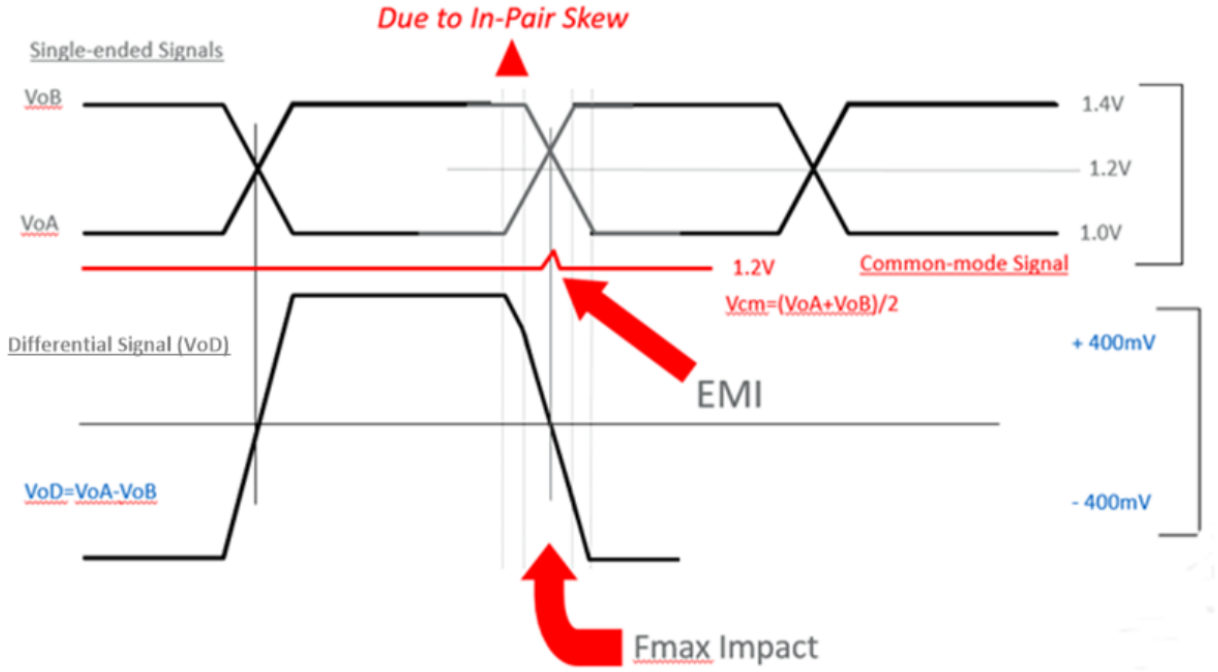



***Figure 7. Maintaining Signal Integrity on Differential Signals***

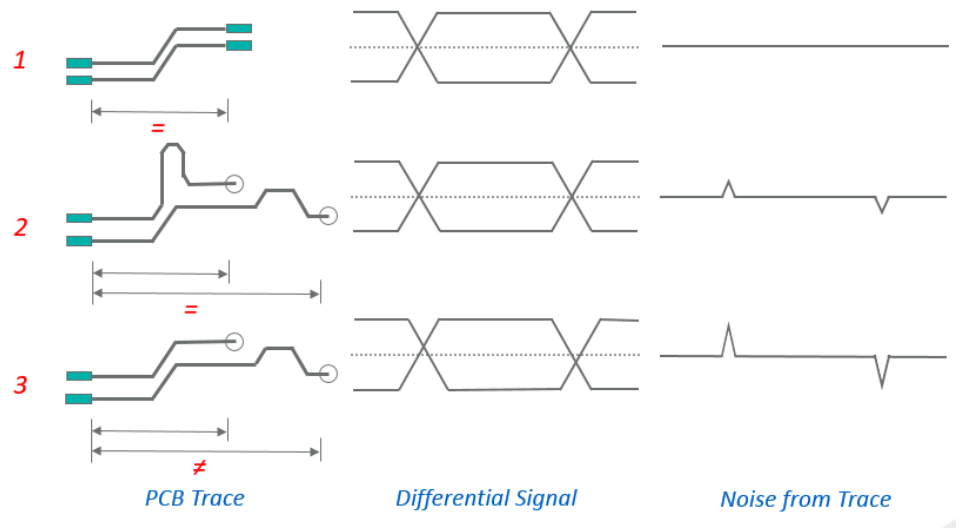



***Figure 8. Connector Skew Effects on Differential Signals***

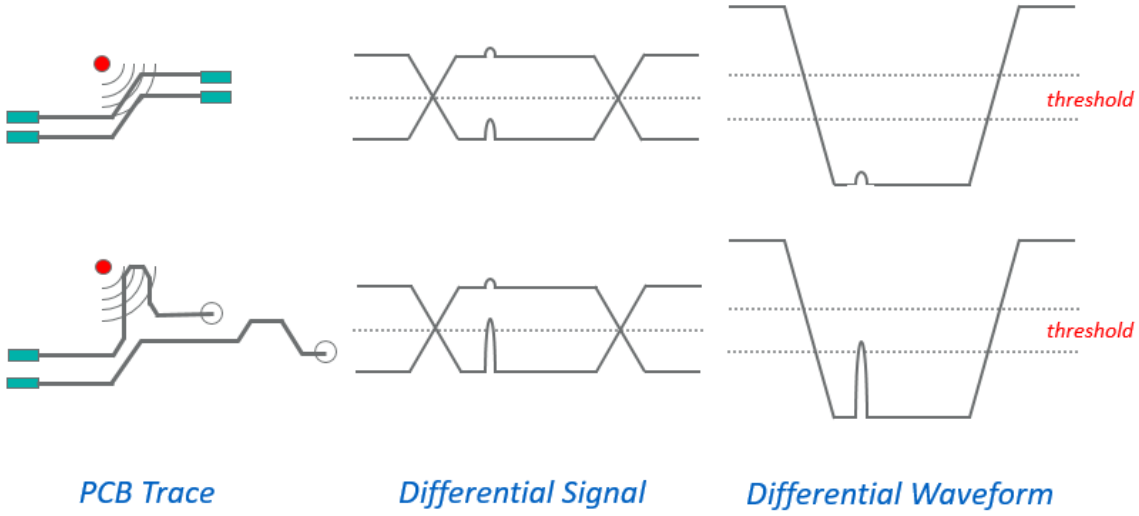



***Figure 9. Signal Coupling and EMI on Differential Signals***

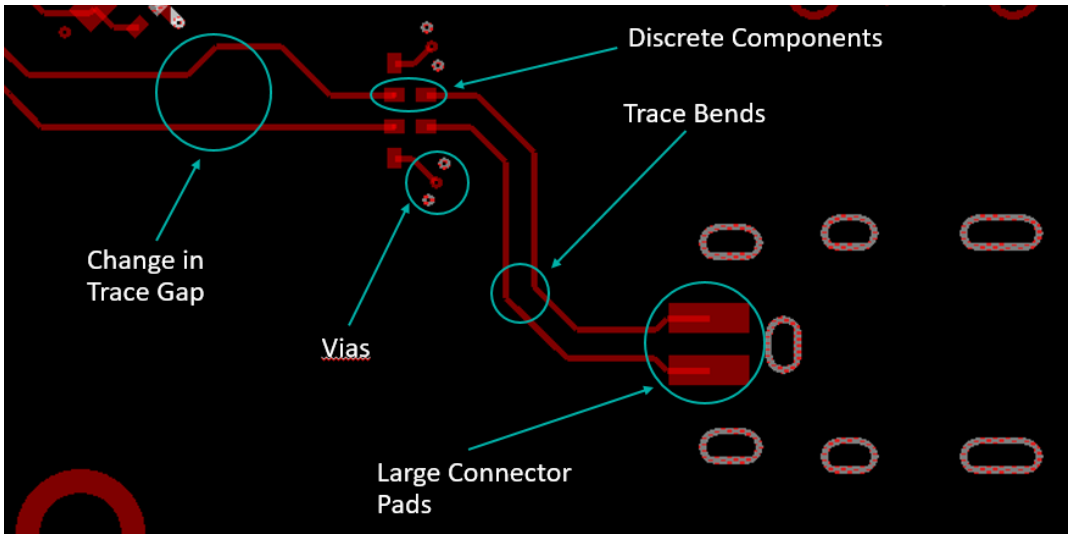



***Figure 10. PCB Layout Impedance Mismatch Examples***

**Tightly Coupled Differential Pair**

- There is better EMI performance.
- Characteristic impedance is highly dependent on gap width.


***Figure 11. Tightly Coupled Differential Signal Pair***

**Loosely Coupled Differential Pair**

- Better S-parameter performance due to impedance not changing with trace spacing.
- This is important for twisted pair connectors that have a wide footprint.

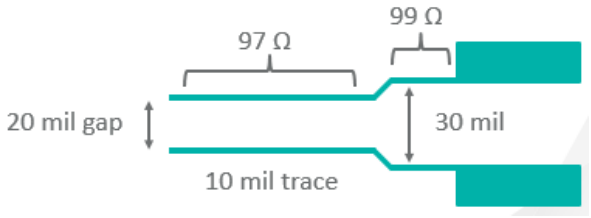



***Figure 12. Loosely Coupled Differential Signal Pair***

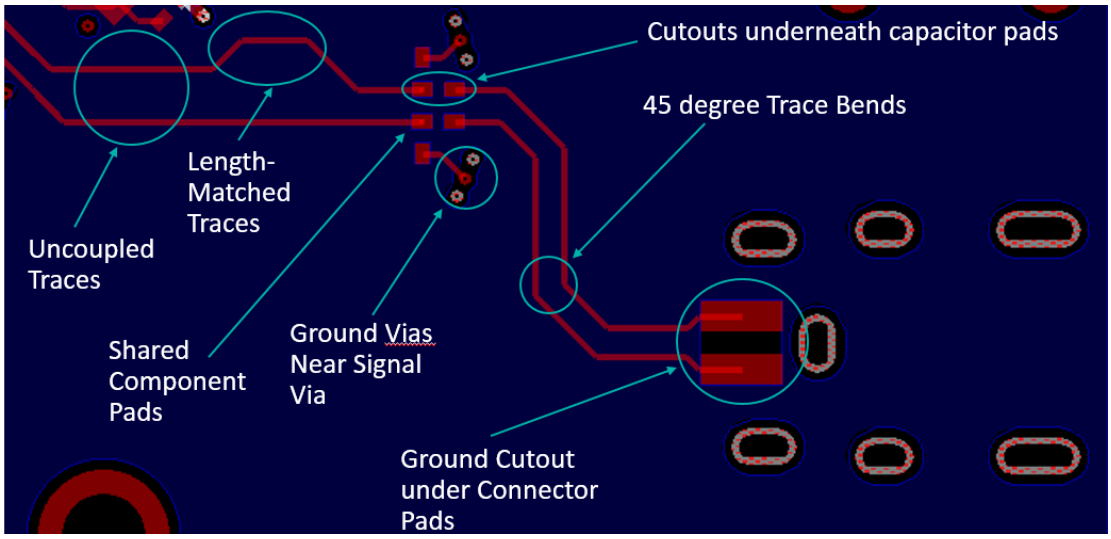



***Figure 13. Optimized PCB Layout for Impedance Matching***

## Layout Recommendations for Other Interfaces

Following are examples of good layout practices for MIPI (C-PHY/D-PHY).

### MIPI PCB Layout Guidelines

#### Recommended PCB Routing for MIPI C-PHY

CSI-2 C-PHY data and clock lines should be routed with best high-speed practices. Unlike D-PHY, there should be little to no coupling between C-PHY lines. C-PHY traces should be impedance-controlled 50Ω single-ended length matched traces corners. Additional information is available from the MIPI Alliance.

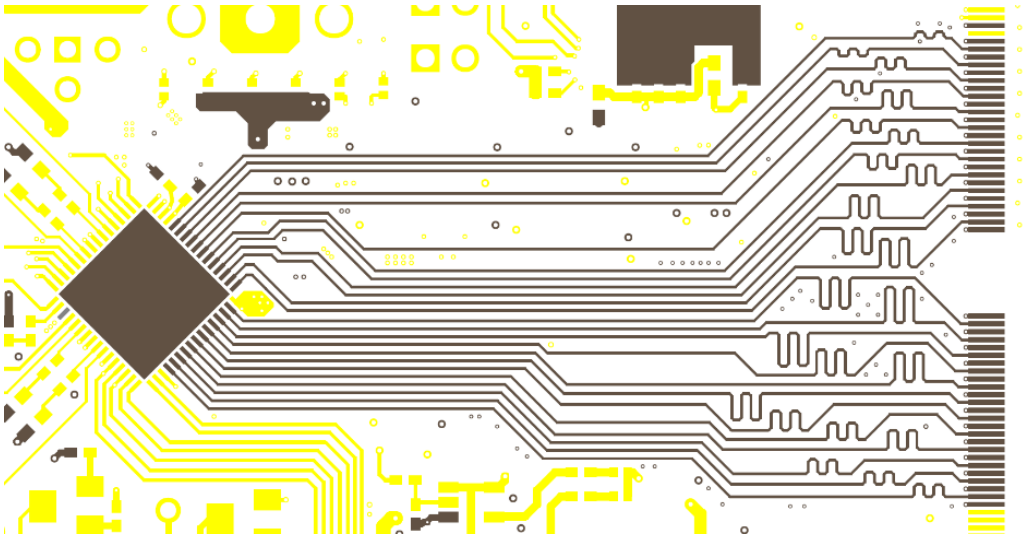


***Figure 14. Example C-PHY Routing Taken from the Analog Devices MAX96712 EV Kits***

**Recommended PCB Routing for MIPI D-PHY**

CSI-2 D-PHY data and clock lines operate up to 1.25GHz (2.5Gbps) and should be routed with best practices. They should be impedance-controlled 100Ω differential length matched traces that avoid any 90-degree corners. Additional information is available from the MIPI Alliance.

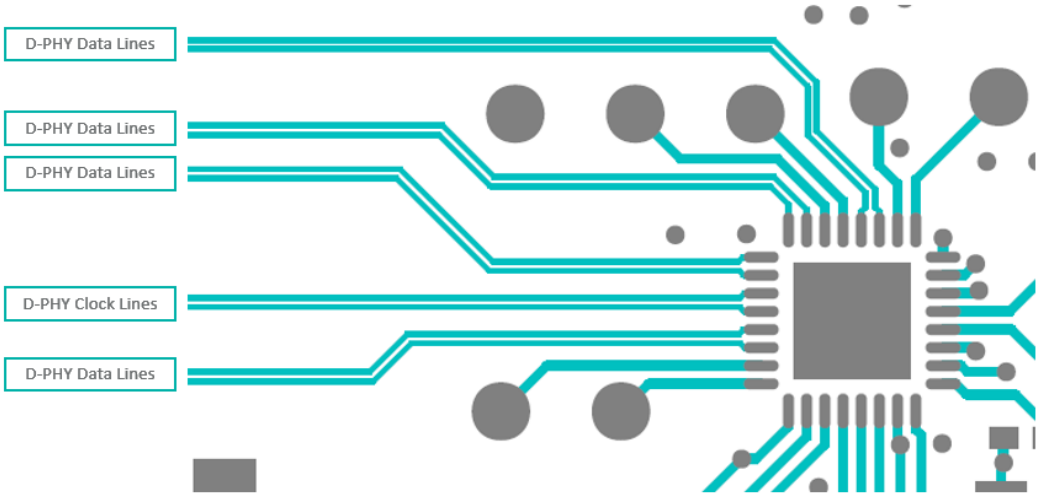



***Figure 15. Example D-PHY Routing Taken from the Analog Devices MAX9295A EV Kits***

**HDMI PCB Layout and TDR Compliance**

Careful consideration must be taken when designing the high-definition multimedia device (HDMI) traces for Analog Devices HDMI serializers to meet HDMI compliance test criteria.

**HDMI Layout Recommendations**

- Maintain differential trace impedance of 100Ω.
- When using an HDMI input connector, place it as close as possible to the chip.
- Keep differential traces together, use as direct as possible routing on differential signals, and route signals through a minimal number of vias.
- In applications that require external ESD protection, place ESD protection diodes near the HDMI connector, as far away from the HDMI serializer as possible. The ESD devices should not be placed over the ground and power plane cutouts near the receiver. The ESD protection diodes should have minimal I/O to I/O capacitance, typical of 0.3pF and low I/O capacitance to GND, 0.7pF typical. Use RClamp0522P as reference.
- Add a resistor footprint with 0Ω resistors to all HDMI differential traces as close to the HDMI serializer as possible.
- Cut out any GND and power copper planes minimum of 45mils below traces at the HDMI receiver (HDMI serializer). See *Figure 16* for dimensions.

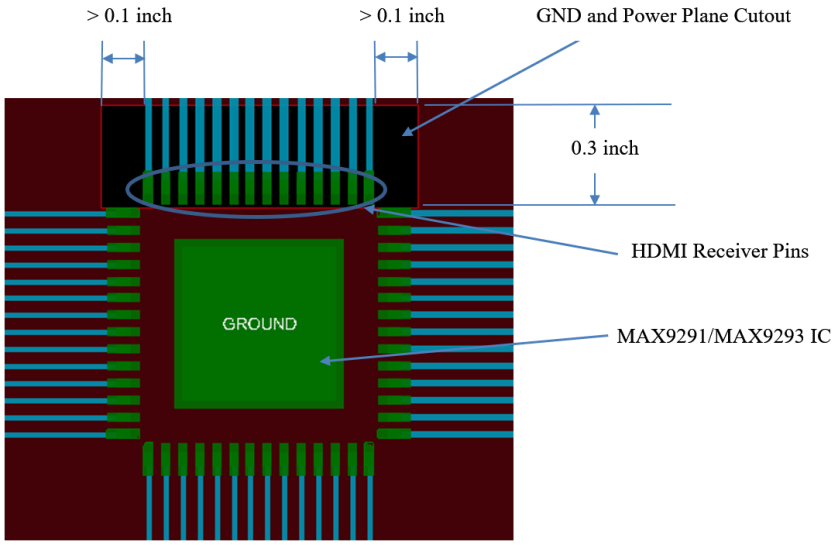



***Figure 16. Ground and Power Plane Cutout***

**HDMI TDR Compliance Test Criteria**

To meet the HDMI TDR compliance test criteria, a time domain reflectometry (TDR) measurement tool is used to measure the differential impedance of the PCB between the HDMI connector, pads of the IC and package.

The differential impedance is ideally 100Ω. The HDMI compliance test limits the variance of the impedance from 100Ω to 25%. This means that the differential impedance measured by the TDR cannot drop below 75Ω or go above 125Ω. Furthermore, if the impedance varies by 15%, meaning the differential impedance drops below 85Ω or rises above 115Ω, it must meet the following stipulations: The duration of the violation is less than 250 pico-seconds and only one excursion can occur during the entire TDR measurement. *Figure 17* shows a TDR measurement that does not pass the HDMI TDR test compliance.

**Test Criteria Summary**

75Ω < Z DIFF < 125Ω

TDR rise time of less than 200psec (10%-90%)

If (Z DIFF_LOW < 85Ω) or (Z DIFF_HI > 115Ω), then it should meet the following two conditions:

1. The duration of violation < 250psec.

2. There is only one excursion—PCB Connector through package IC, TDR Rise time of less than 200psec (10%-90%).

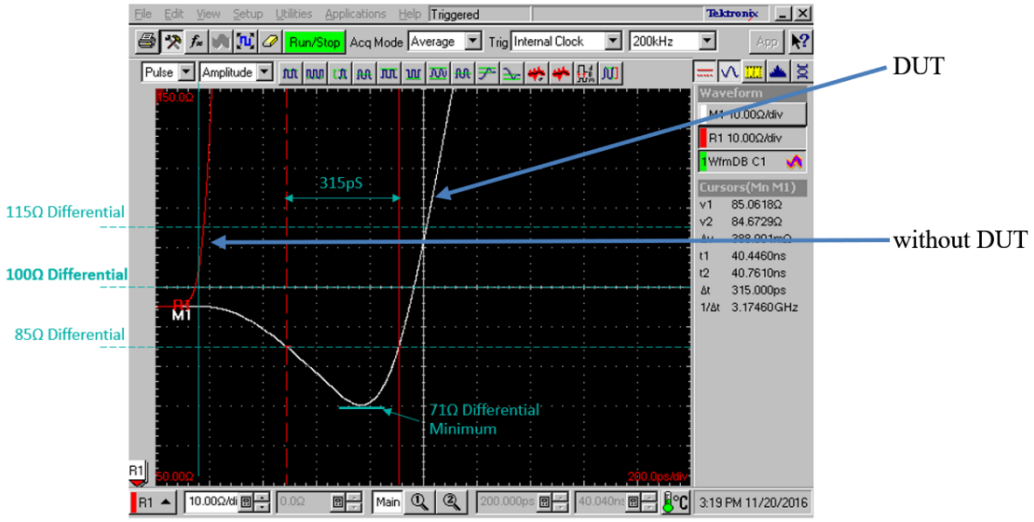



***Figure 17. TDR Measurement Failing Test Criteria***

## Crystal Recommendations

Proper selection of load capacitors is critical to the proper operation of the crystal. A crystal's ESR is an important consideration as it relates to crystal startup time. Crystals that have high ESR may not even start at all because of low margin between negative resistance (see the following sections for details) and the ESR. Other considerations, such as crystal drive level (power dissipation), are important as well. Operation of a crystal outside of the drive level can result in unpredictable change in frequency, ESR, and reliability.

### Crystal Selection

When selecting an automotive grade 25MHz crystal, consider the following parameters.

### Calculate Load Capacitance Needed

The crystal circuit is shown in *Figure 18*. Note that $R_{LIMIT}$ and $R_{FEEDBACK}$ are integrated into the IC and should not be added externally.

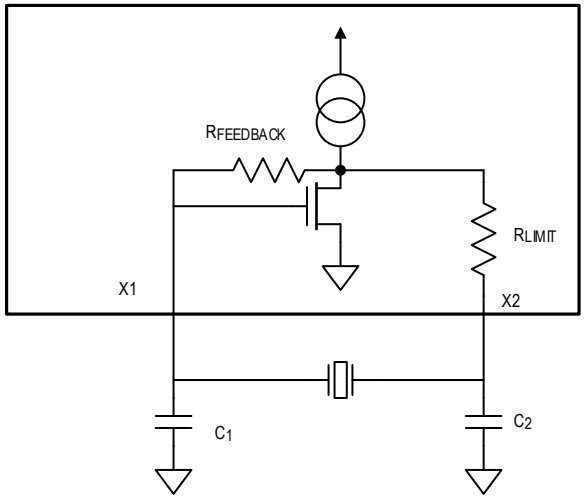


***Figure 18. Recommended Crystal Schematic***

Determine the required load capacitance from the Crystal data sheet. Note that for each leg of the filter, the capacitance seen by the oscillator would be the sum of:

C1 or C2 component value

X1 or X2 pin capacitance value (from GMSL3 data sheet)

X1 or X2 board capacitance value (measured/simulated from layout)

If an example crystal requires 20pF at X1, and the example pin capacitance is 3pF at X1, and the example board capacitance is 8pf at X1, then the example C1 component value must be 9pF.

**Crystal Layout Recommendations**

- Use load capacitors as recommended by the crystal manufacturer. Capacitance seen by the crystal is a summation of:
  - Load capacitor $C_{LOAD}$,
  - PCB trace capacitance, and
  - Input capacitance of the X1 and X2 pins as given in the relevant GMSL3 data sheet.
- Do not add an external feedback resistor or limit resistor; these are internal to GMSL3 devices. The value of the internal feedback resistor and limit resistor is given in the data sheet. On GMSL3, the feedback resistor is built internal to the IC so an external feedback resistor is not required.
- Place crystal as close as possible to X1 and X2 to reduce parasitic capacitance. Length matching of X1 and X2 traces is not required. Trace width is not critical, but it affects capacitance. Fifty ohm traces are not required.
- X1 and X2 traces should be shielded from aggressors such as GMSL3 lines and GPIO. Trace length should be minimal to prevent possibility of aggressor noise.
- If necessary, crystal can be on the board backside, if this is necessary to minimize trace length.
- Ground pour can be used to improve shielding from aggressor noise if space permits.
- Crystal's case ground should be well connected to the ground plane with minimal trace.

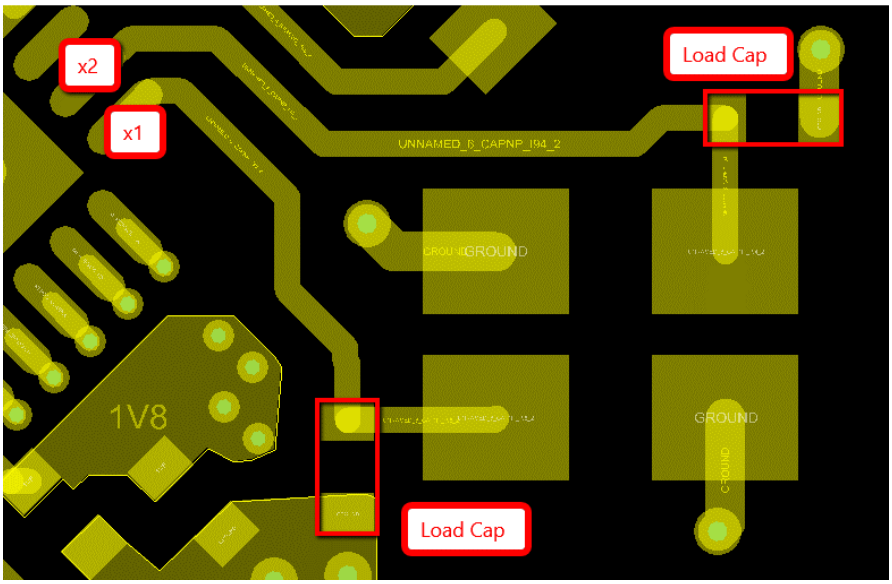



***Figure 19. Example Crystal Layout***

## DC Bypass Capacitors

- Place the smallest capacitor closest to the serialization/deserialization (SerDes) power pin.
- Orientate DC bypass capacitors so that the GND is common, not separate GND islands.

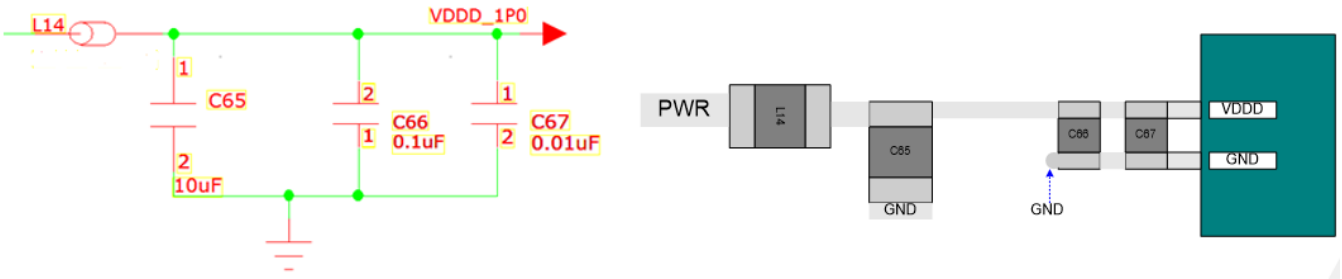



***Figure 20. Bypass Capacitor Placement Example***

## Thermal Considerations

The Analog Devices GMSL3 SerDes products are intended to operate within a specific temperature range measured in the die. Operation outside of this range could result in poor performance or shortened life of the product. Analog Devices recommends a thermal simulation of the system when possible and later, measuring component temperature using on-chip diodes or voltage references.

Board design stackup, proximity to other heat-generating components, airflow, heat sinks, ground planes, etc., all affect the operating temperature of the device.

Temperature parameters for integrated circuits are typically specified in one or more of the following terms:

- TJ (Junction Temperature),
- ΘJC (Thermal Resistance, Junction to Case in degrees C per Watt), or

- ΘJA (Thermal Resistance, Junction to Ambient in degrees C per Watt).

Refer to the Analog Devices Tutorial 4083 for an overview of Thermal Characterization of IC Packages. (*https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html*).

The IC die is attached to the package lead frame with a conductive adhesive and covered in a plastic package. Each has a thermal resistance to the ambient environment.

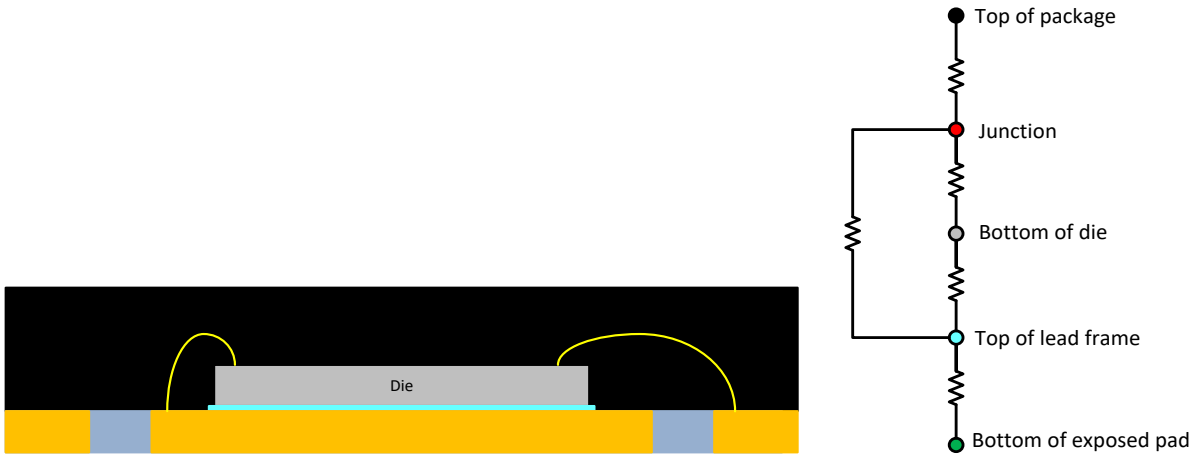



***Figure 21. Die and Package Diagram of Typical Device and Typical Thermal Resistances of IC Packages***

The top of the package can dissipate heat from the die to the surrounding air. The lead frame can dissipate heat to the PCB through a metal pad and, to a much lesser extent, through the package pins.

Thermal specifications for each GMSL3 device are given in their relevant data sheets.

**Layout Recommendations**

To help with thermal performance, Analog Devices recommends an array of vias in the exposed pad (EP). Additional vias close to the high-speed ports are also recommended (this varies depending on package type and pinout). As many vias as possible should be used in the array to maximize thermal performance. See *Figure 22*.

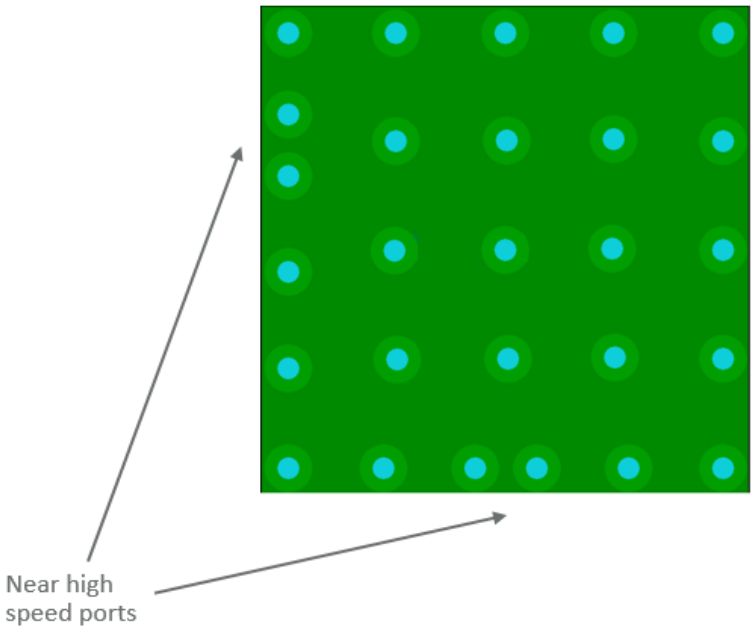



***Figure 22. Thermal Vias in the EP of IC***

### Shielding Recommendations

To optimize the EMI/EMC performance of the design, it is recommended to shield the GMSL device and associated high-speed interconnects and passive components when possible.

## Connectors and Cables

Connectors and cables have different characteristics that play an important role in the GMSL3 channel specification.

### Cabling

Different cables can be utilized for their different properties to best match an application. Cabling with thinner center conductor can be lightweight, more flexible (better bend radius), and be lower cost due to the smaller center conductor (less copper). Cabling with thicker center conductor can have better insertion loss characteristics to allow for longer links.

For example, the areas that are difficult to route to and bend many times throughout the lifespan of a vehicle, such as a trunk or mirrors, can use a short segment of thinner center conductor flexible cable. The segment that uses the longer cable segment can use the thicker center conductor cable with better insertion loss characteristics.

Differential cabling should have 100Ω differential characteristic impedance while Coax cabling should have 50Ω characteristic impedance. Typical DC resistance of the center conductors is approximately 0.1Ω to 0.2Ω per meter.

The STP cabling is differential cabling, which is two conductors that are twisted, wrapped in a single-shielded over-braid. Shielded twisted-quad (STQ) cabling is four center conductors that are twisted together typically in a star-quad configuration and wrapped in a single-shielded over-braid. Star-quad cabling uses the differential output of the GMSL3 PHY and offers a benefit over STP for applications that require a differential pair plus power and GND. It can also be used for dual-link applications. Another type of cabling is shielded parallel pair (SPP). This type of cabling is two center conductors running parallel to each other instead of twisted like STP.

For the price, Coax cabling offers a better insertion loss per meter and often provides the best solution for reliable link performance, flexibility, and weight vs. STP cabling. A Coax cable can often cost less than a comparable STQ cable while offering as much as 50% longer cable runs in a channel.

**Table 2. Cables to Consider**

| Name | Manufacturer | Type | Flexibility |
|---|---|---|---|
| **Dacar 302** | Leoni | Coax | Medium |
| **Dacar 462** | Leoni | Coax | High |
| **1.5DS** | Shikoku | Coax | High |
| **Dacar 686-3** | Leoni | STP | Medium |
| **2Speed 256** | G&G | STP | Medium |
| **Dacar 636** | Leoni | STQ | Low |
| **Quadspeed** | G&G | STQ | Low |

## Connectors

Connector insertion loss is typically less than 0.5dB at 3GHz. Proper layout techniques are required for the connector footprint to minimize signal reflections to obtain good return loss performance. It is strongly recommended to simulate the connector footprint based on board stackup using a 3D simulation tool. Contact connector vendors for simulation models.

**Table 3. Connectors to Consider**

| Name | Manufacturer | Link Configuration |
|---|---|---|
| **FAKRA** | Molex | Single/Dual<br>1x/2x Coax |
| **FAKRA** | Rosenberger | Single/Dual<br>1x/2x Coax |
| **FAKRA** | TE Connectivity | Single/Dual<br>1x/2x Coax |
| **H-MTD** | Rosenberger | Single/Dual/Quad<br>Differential Pairs<br>1x/2x/4x STP |
| **MATE AX** | TE Connectivity | Single/Dual/Quad<br>1x/2x/4x Coax |
| **HFM (FAKRA Mini)** | Rosenberger | Single/Dual/Quad<br>1x/2x/4x Coax |
| **HFM (FAKRA Mini)** | Molex | Single/Dual/Quad<br>1x/2x/4x Coax |

## Connector Modeling

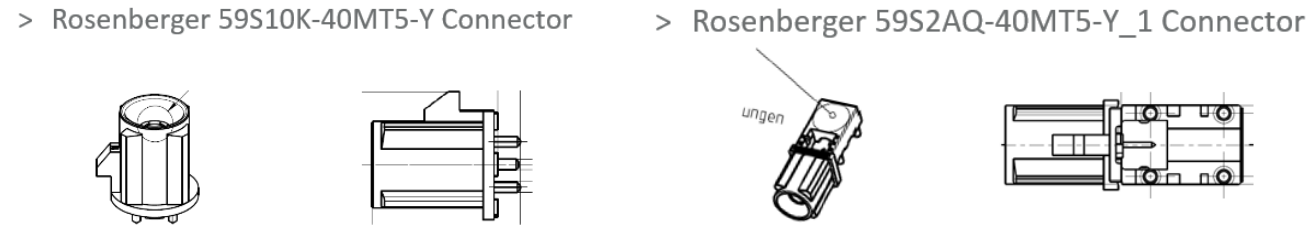



***Figure 23. Straight PCB Plug vs. Right Angle Plug***

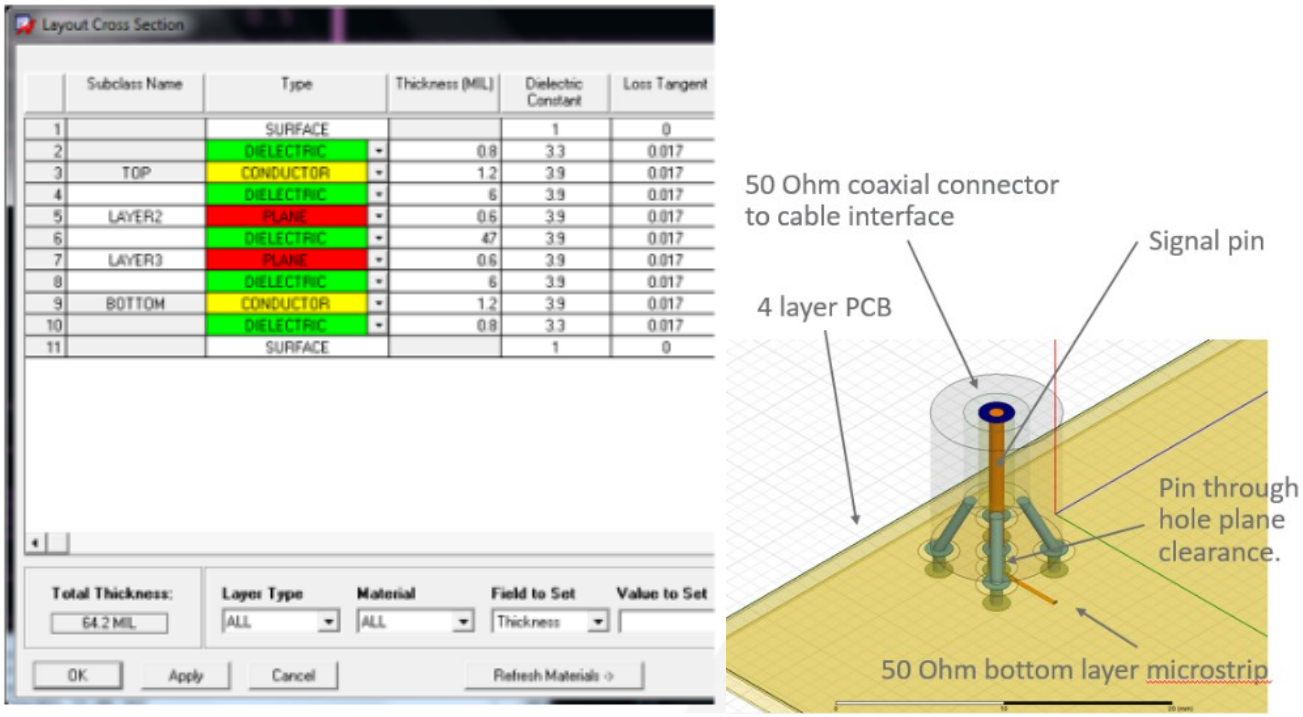



***Figure 24. PCB Construction***

Impedance Match by using

- Clearance_top = 1.4mm
- Clearance_mid1 = 0.8mm
- Clearance_mid2 = 1.4mm

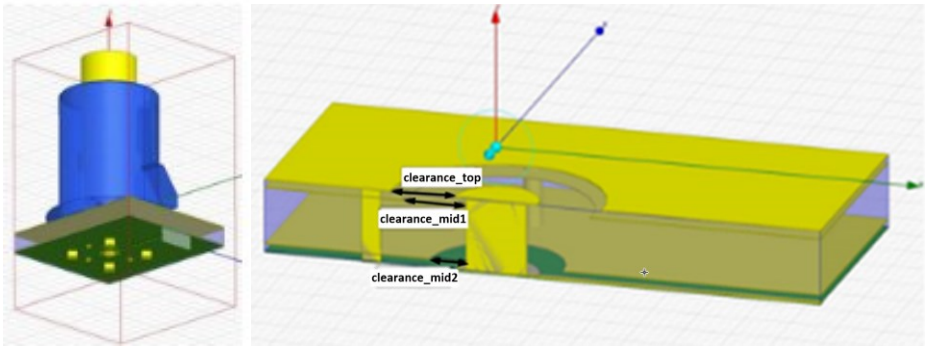



***Figure 25. Clearance Definitions for 59S10K-40MT5Y Connector***

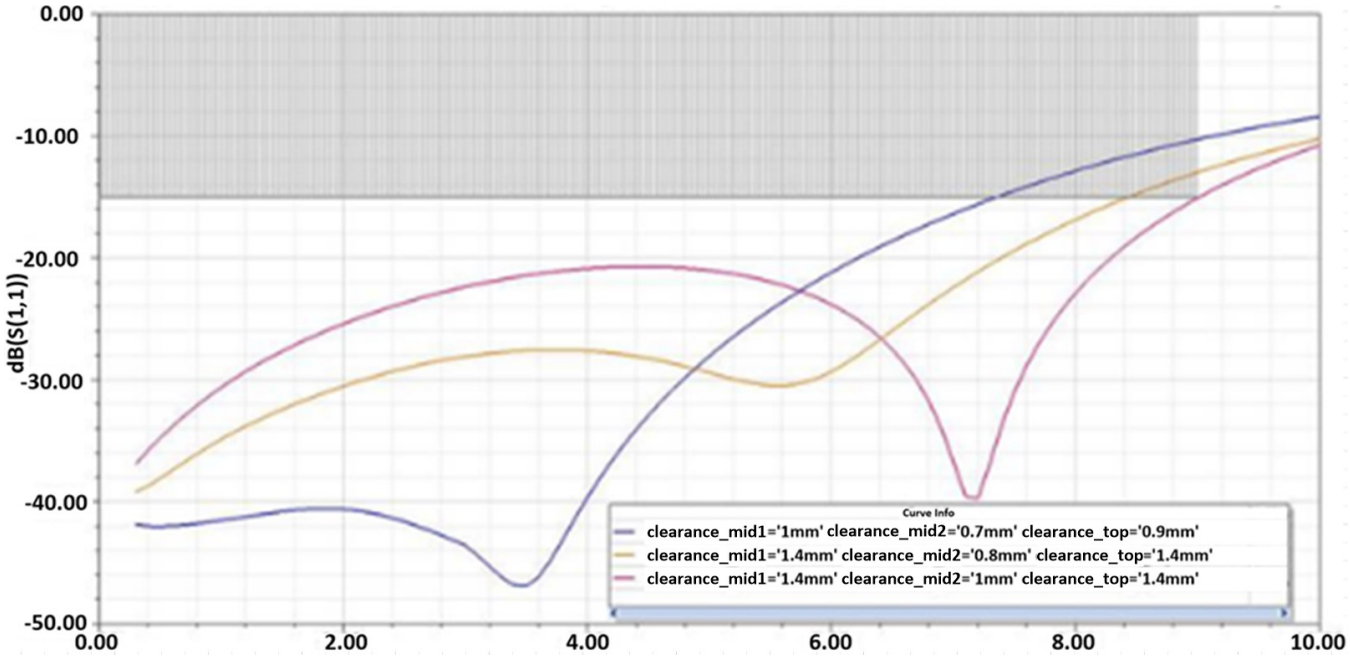



***Figure 26. 59S10K-40MT5Y Connector Return Loss with Varying Clearances***

# Line Fault

## Line Fault Summary

The GMSL3 line fault detection scheme requires only a single external resistor on each end of the serial link to detect various application fault conditions such as:

- Short to battery
- Short to GND
- Open line
- Line-to-line short

**Note**: Line fault cannot be used with PoC as this does not provide accurate line detection measurements.

## Coax Mode (Single-Ended) Hardware Requirements

The local side detecting the line fault requires a single 48.7kΩ connected directly from a Line Fault Monitor X (LMNx) pin to the serial link. The remote side of the serial link requires a 49.9kΩ connected to GND. All line fault resistors should be ±3% accurate or better to ensure proper operation.

**Note**: Line fault detection can be done in the serializer or deserializer, depending on where the microcontroller is located.

*Figure 27* and *Figure 28* show the two options for line fault detection. Configuration Example 1 is typically used for display links. Configuration Example 2 is typically used for camera links; however, either configuration can be used on any device.

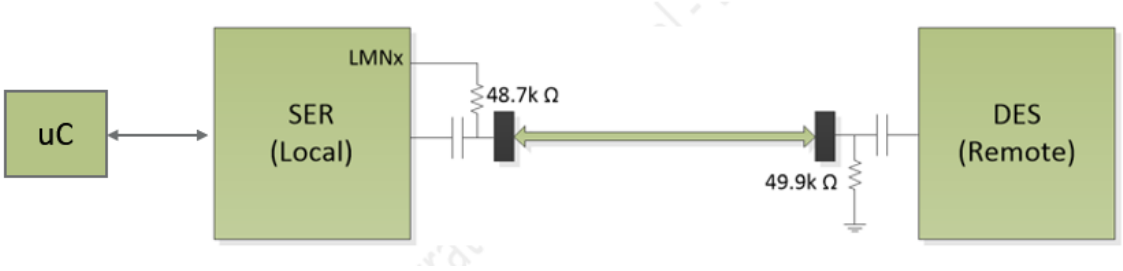



***Figure 27. Coax Line Fault Configuration (Example 1)***

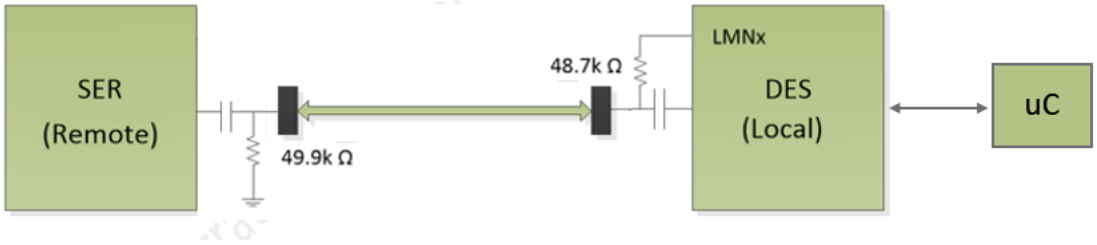



***Figure 28. Coax Line Fault Configuration (Example 2)***

The LMNx pins (LMN0–LMN3) are typically mapped to different multifunctional pins on each unique part and package option. Some parts may have up to four line-fault detectors depending on package and pin availability.

## Twisted Pair Mode (Differential) Hardware Requirements

If operating in twisted pair mode, it is required to connect one line to an even-numbered LMNx pin and the other line to an odd-numbered LMNx pin. The even-numbered pins (LMN0 and LMN2) must be connected using a 42.2kΩ; the odd-numbered pins (LMN1 and LMN3) must use a 48.7kΩ resistor. Line-to-line shorts can only be detected if LMN0 is paired with LMN1 or LMN2 is paired with LMN3. For twisted pair applications, ensure LMN0/1 or LMN2/3 are used for full operation.

The resistor values are critical for reliable line detection in the twisted pair mode and should be ±3% accurate or better.

An example for twisted pair line fault operation is shown as follows:

**Table 4. Line Fault Signals, Pin Pairs, and Resistors in Twisted Pair Mode**

| Signal | SIOA+ | SIOA- |
|---|---|---|
| Ideal Line Fault Pair #1 | LMN0, 42.2kΩ | LMN1, 48.7kΩ |
| Ideal Line Fault Pair #2 | LMN2, 42.2kΩ | LMN3, 48.7kΩ |

*Figure 29* is an example of the twisted pair line monitoring configuration.

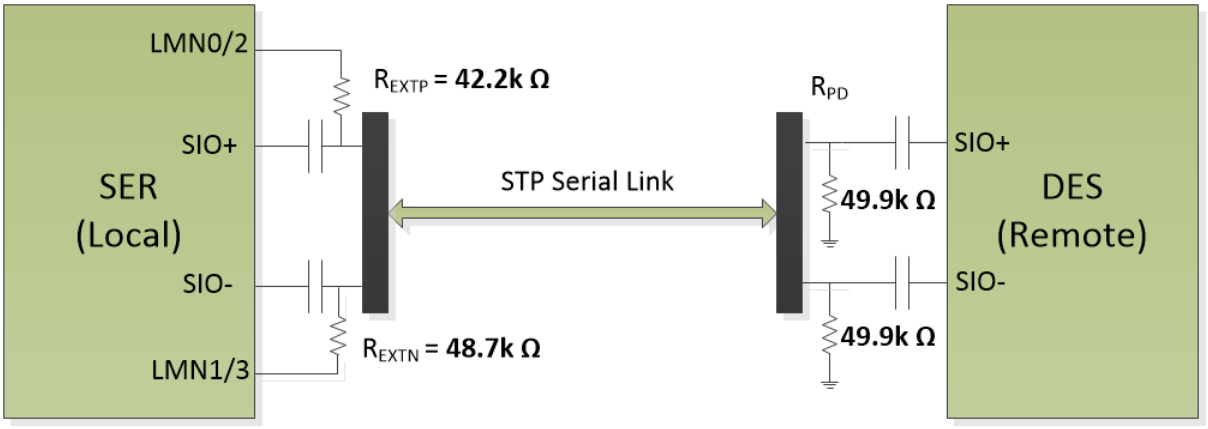



***Figure 29. STP Line Fault Example***

## Simultaneous PoC and Line Fault

Line fault cannot be used simultaneously with PoC.

## Layout for Line Fault

The line fault resistor should be placed with the pad on the high-speed trace such that there is no stub on the serial trace. As described in the PCB layout section, ground cutouts are recommended for impedance matching. *Figure 30* represents a layout for the line fault resistor.

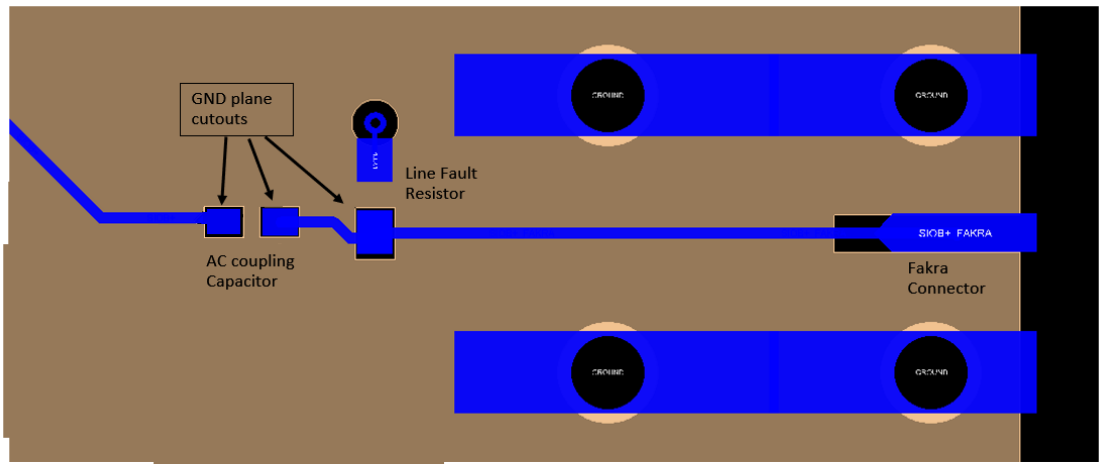



***Figure 30. Line Fault Layout***

## Power-over-Coax

Power-over-Coax is a technique of sending power and data over a single coax cable. This enables the power of remote devices like automotive cameras without the need for extra wiring or power circuitry. PoC is desirable for camera Advance Driver Assistance Systems (ADAS) applications because it reduces cabling in the vehicle.

A well-designed GMSL3 PoC filter should cover the forward and reverse channel frequency band, have great performance at lower frequencies and upper frequencies, and be optimized for size, cost, and current. It is important to verify that the channel is compliant with the addition of PoC, as the PoC filter introduces additional insertion loss and return loss to the channel.

***Figure 31*** shows a block diagram of a SerDes system utilizing PoC.

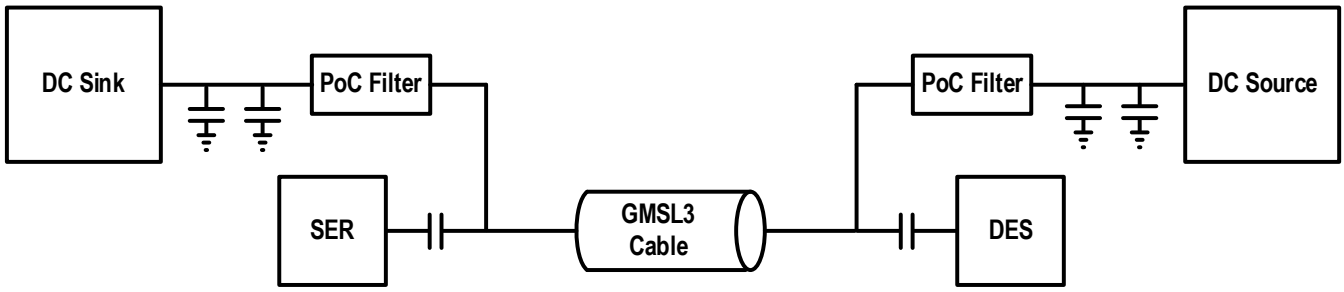



***Figure 31. GMSL3 PoC System Design Block Diagram***

### Theory of Operation

A PoC filter is a notch filter which uses inductors to block the high-frequency signals on the channel from entering the power line while allowing DC current to pass. The AC coupling capacitors in the channel on the serializer and deserializer PCBs allow the high-frequency signals to pass from the transmitter to the receiver, while blocking DC power from entering the device.

*Figure 32* demonstrates the broad frequency band that a PoC filter must attenuate to not influence the high-speed data on the serial link.

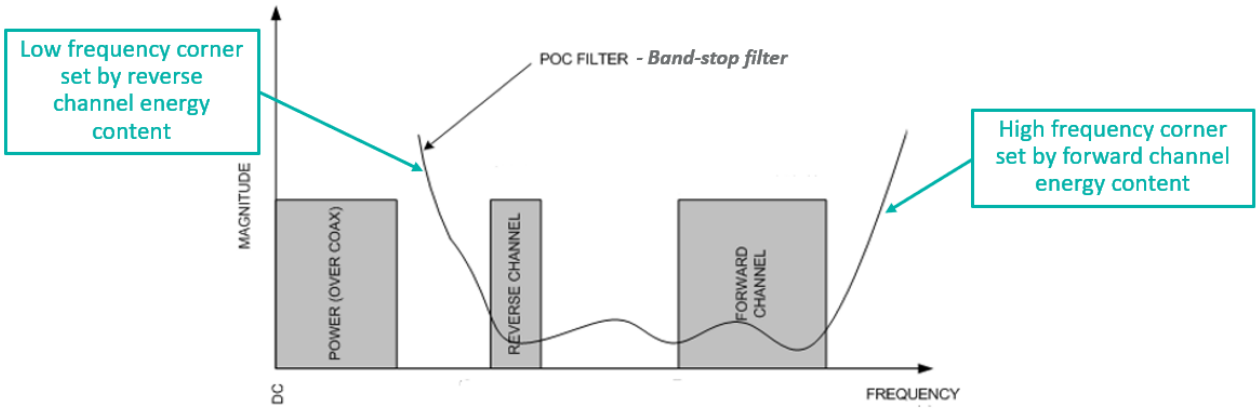



***Figure 32. Transfer Function for PoC Circuit Showing the Frequency Bands of the Power Delivery, Reverse Channel, Forward Channel, and Attenuation of the PoC Filter***

### Self-Resonance Frequency

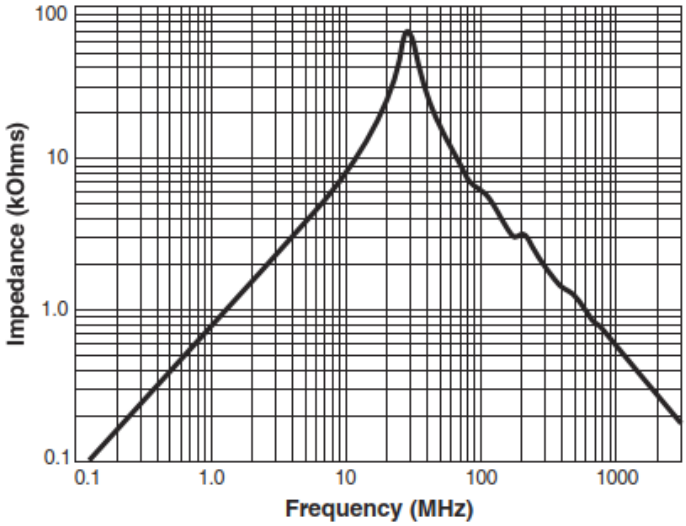



***Figure 33. Inductance vs. Frequency for Typical Chip Inductor Showing Self-Resonant Frequency at 30MHz and Decay Above 30MHz***

The inductors used in a PoC circuit are often wire-wound devices with ferrite compound cores and have high impedance and Q value at the self-resonant frequency. These types of power inductors have higher parasitic capacitance, while non-RF chip inductors have low self-resonant frequencies (SRF). Above the SRF, the inductor begins to act like a capacitor.

$$f_{SRF} = \frac{1}{2\pi\sqrt{LC_{par}}}$$

Equation 1. Self-resonant frequency (Hz) for inductor with inductance L and parasitic capacitance $C_{par}$

A PoC circuit is constructed from a single or multiple inductors used to create a filter that attenuates a large frequency band that covers the full spectrum used by the GMSL3 forward and reverse channels. The inductors must be carefully chosen such that their combined frequency response provides enough attenuation across the full stopband frequency range, as shown in *Figure 34*.

The PoC Network impedance is the sum of the impedances of the individual components. Due to complex impedance of each component, the total impedance may be less than the impedance of an individual component at a particular frequency.

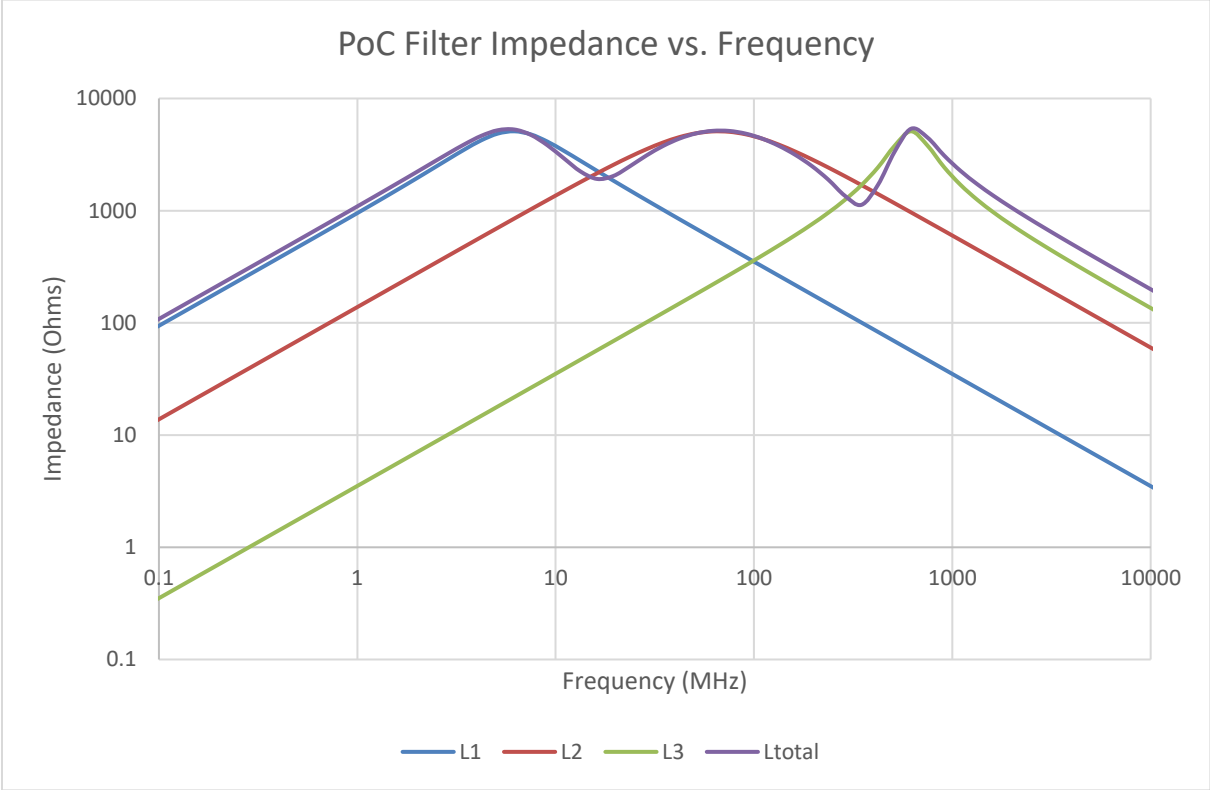



***Figure 34. Frequency Response of a Three-Inductor PoC Network Composed of Inductors L1, L2, and L3 in series. The Purple Line is the Overall PoC Frequency Response.***

**Effect of Bias Current**

The values provided in inductor data sheets of impedance and inductance over frequency are typically measured with no applied DC. The DC bias current substantially affects the performance of inductors. Following are some effects of bias current:

- Increased heat dissipation due to series resistance. Prolonged heating beyond typical values breaks down the inductor.
- Inductors function well in the linear region but above a certain magnetic field, the magnetic flux density saturates. This corresponds to a decrease in effective inductance.
- The ferrite core of the inductor saturates thus decreasing its inductance. Air-core inductors do not saturate but are affected less by added DC.
- In ferrite-core inductors, past a certain current level, the effective inductance of the component becomes negligible.

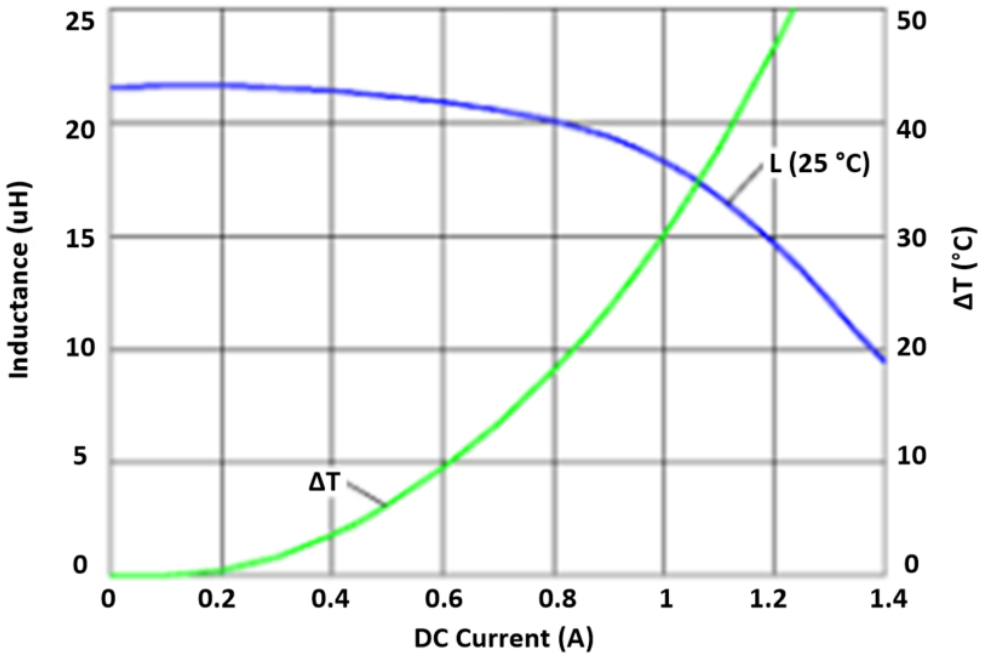



***Figure 35. Effective Inductance of Chip Inductor and Temperature Rise vs. Current***

Due to these effects, the inductance and impedance curves provided in inductor data sheets may not accurately describe how the inductor performs in a PoC network. See *Figure 35*.

In the case of PoC circuits under varying current conditions, the transfer function is not ideal. This is mainly because as current increases the effective inductance increases. In turn, the self-resonant frequency increases (as parasitic capacitance is unaffected). The transfer function shifts right to a higher frequency, and the impedance at a higher frequency is generally lower due to the decreased effective inductance. The shift in the impedance transfer function can be particularly detrimental when trying to filter a relatively narrow band, such as the reverse channel on GMSL3, as the transfer function may be shifted out of the band altogether and stop filtering the reverse channel.

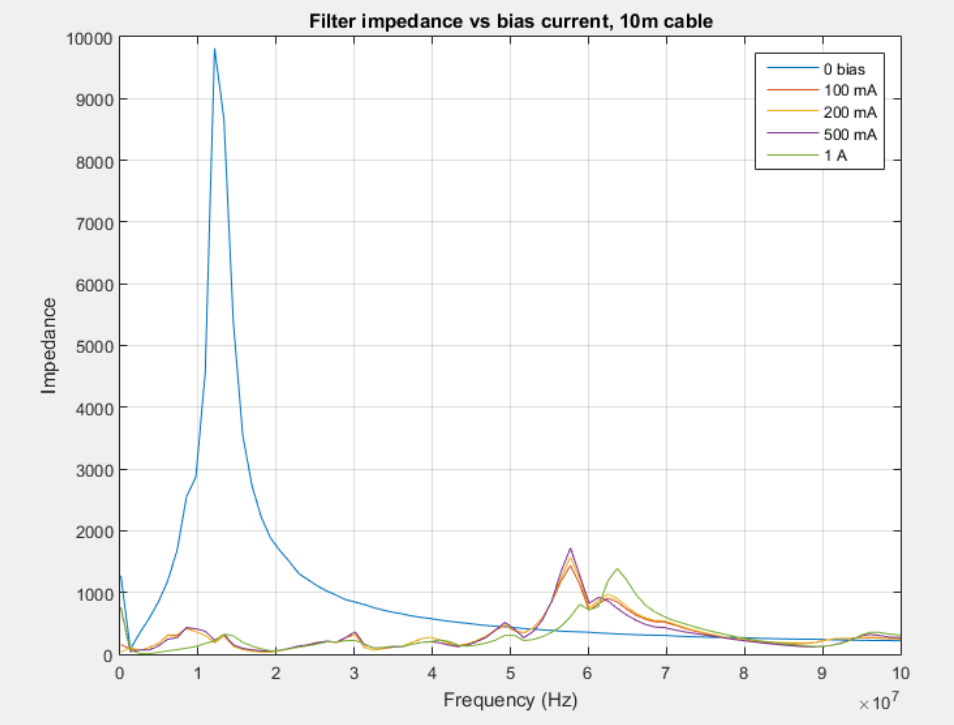



***Figure 36. Impedance of PoC Filter with Applied Bias Currents***

*Figure 36* characterizes the PoC filter with an applied bias current from 0A to 1A. The peak impedance decreases due to a decrease in effective inductance. As the inductor material breaks down with increased current, there is a shift to the right due to change in the self-resonant frequency.

**Note**: Analog Devices is no longer recommending ferrite beads for PoC designs due to their performance sensitivity to increases in temperature and current.

## PoC Design and Validation Process

Analog Devices requires a PoC filter to fully pass GMSL3 Channel Specification insertion and return loss parameters. Maintaining a minimum 1kΩ impedance from 2MHz to 3GHz is recommended. The following outlined sections can be used to validate a PoC filter.

### Component Selection

Following is a list on how to select inductors and AC coupling capacitors.

### Inductors

Select inductors to cover the frequency band stated under the *Theory of Operation* section. Note the following effects:

Inductor Saturation Current

a. Inductance drops as DC increases. This saturation current level is also temperature dependent. A rule of thumb is to have the saturation current affect the inductance by no more than 10% from the zero-current value.

Inductor DC Resistance

b. The DC resistance should be kept low. It affects the PoC circuit in the following two ways:

i. Voltage drop across the filter, which affects power supply headroom and noise rejection.

ii. Power dissipation inside the inductor, which limits load current/operation temperature.

Inductor Q and Parallel Resistances

c. The impedance of an inductor is often very large at one frequency and quickly tapers off away from the self-resonant frequency. Addition of a large parallel resistor increases its Q, which broadens the frequency range of the inductor impedance at the expense of the maximum possible impedance.

**AC Coupling Caps**

GMSL3 uses 0.1µF capacitors to block the PoC voltage from the high-speed GMSL3 pins. Note that DC biasing of the capacitors affects the capacitance value. A general rule is to select capacitors that have a DC voltage rating at 2x-3x the expected DC bias.

**Simulate PoC Filter System**

Simulate the PoC network against the GMSL3 Channel Specification to check performance.

**Obtain Inductor and Cable S-Parameters Models**

Inductor and cable vendors typically supply S-parameters or lumped-element circuit models, so that the system can be simulated with a tool such as Simplis or ADS. This can be useful for initial PoC circuit design; however, there are limitations with using a simulation model. Inductor models may neither reflect worst-case current load nor high temperature; cable models may neither reflect aging characteristics nor high temperature. Contact the component suppliers to get S-parameters for worst-case conditions per use case.

**Simulate PoC Filter Impedance**

Simulate the PoC filter and check for a minimum 1kΩ impedance from 2MHz to 3.5GHz.

See *Figure 37* and *Figure 38* for the example simulation and schematic for PoC impedance.

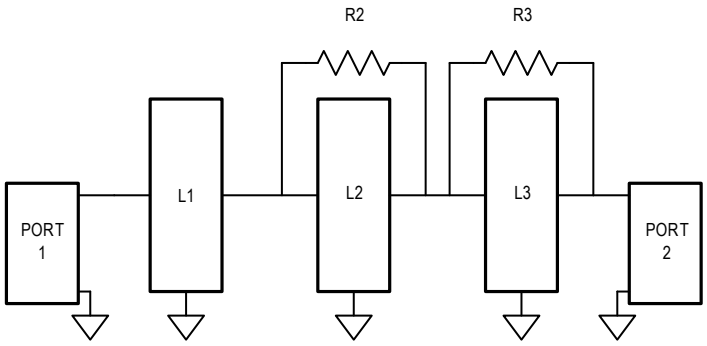



***Figure 37. Example Simulation Schematic for PoC Impedance***

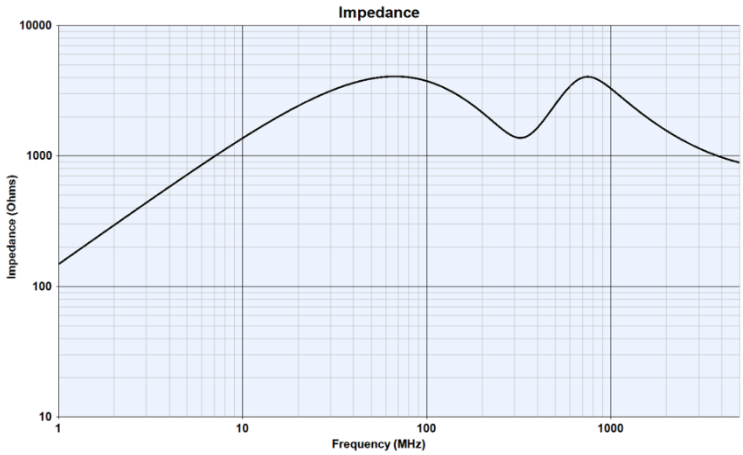



***Figure 38. Example Simulation Result PoC Impedance***

### Obtain PCB S-Parameters Models

Layout the board per high-speed PCB best practices and get an estimate for the S-parameters of the board. Simulation of the PCB differs from inductor components due to the traces/vias and ground planes that are on the board. Inductor modeling is strictly of the component.

### Simulate PCB Board and Cable PoC System

Once all S-parameters (PCB board, cable, inductor(s), capacitor, etc.) are obtained, simulate the PoC system. Ensure that the simulated results pass the GMSL3 Channel Specification. See *Figure 39* for an example setup.

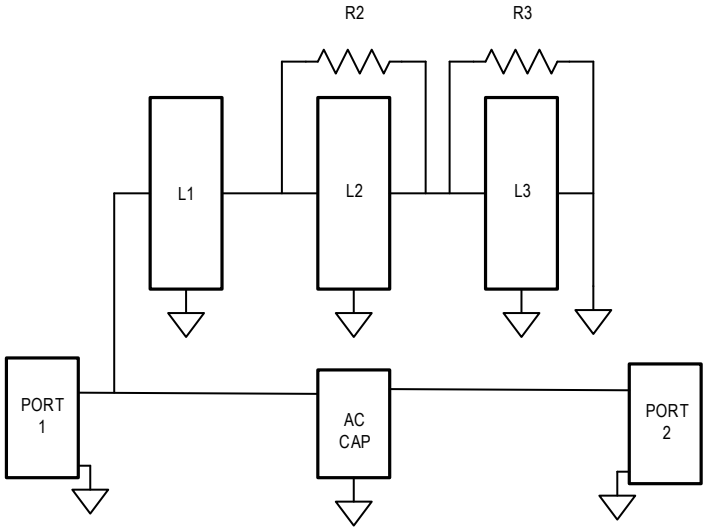



***Figure 39. S-Parameter Simulation Using S-Parameter Data Measured on Each Board***

## PoC Bench Verification

Validate the simulations on the bench of the PoC system (PCB board, cable, inductor(s), capacitor, etc.).

### Pre-Production System Testing

The following sections can be followed to validate PoC in a pre-production environment when the full end-to-end system hardware is not available.

### Measure Cables and Inline Connectors

Use a Vector network analyzer to measure the S-parameters of the cable and inline connectors. These should ideally be tested with “aged cables” to simulate the worst-case cable conditions.

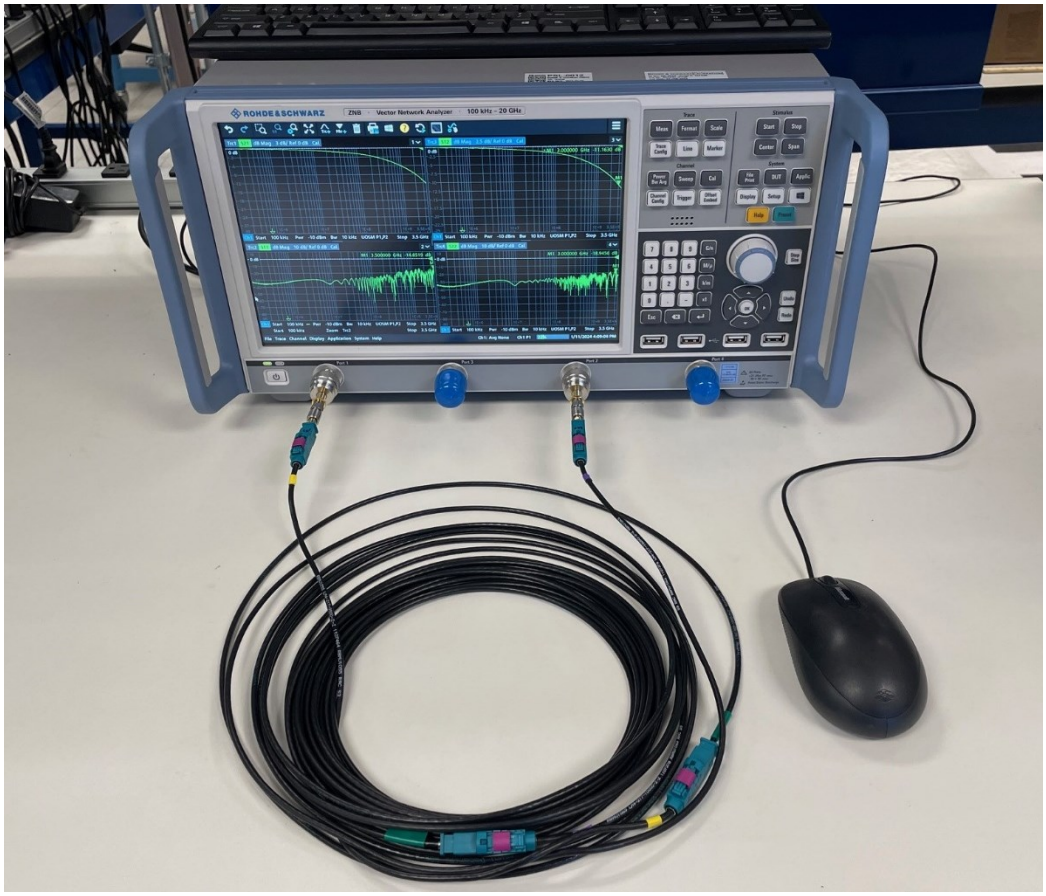



***Figure 40. S-Parameter Measurement of Cable/Inline Connector***

### Measure PoC Circuit S-Parameters

Construct the PoC circuits on small PCB “coupon boards” (*Figure 41*). This allows for quick evaluation of different PoC components with the target cables without the need to layout and build an entire system. It is recommended to use the same board material and stackup as is planned for production design. This allows both the PoC network and the layout to be characterized.

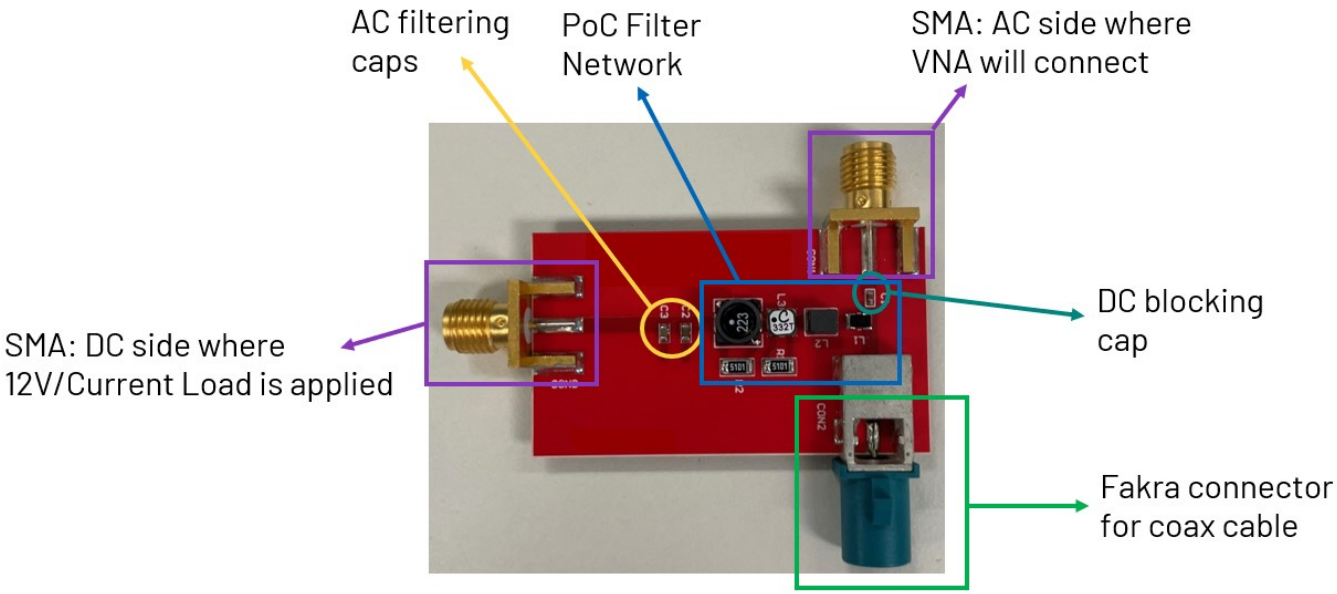



***Figure 41. PoC Coupon Board Comprising DC Bias Input/Output, VNA Port Connection, and a Fakra Connector to Connect a Cable and Second Coupon Board to Evaluate a Complete Link***

To verify the components, use one board to represent the serializer and a second board to represent the deserializer (*Figure 42*). Test the boards over temperature, maximum current, and maximum cable length (*Figure 43*). S-parameters should be captured across system corners and are required to pass the GMSL3 Channel Specification with enough margin to cover additional losses and mismatch of the final PCB boards.

**Note**: Many VNAs do not allow DC bias voltage. A DC block (calibrated out through VNA calibration) may be needed to protect the VNA.

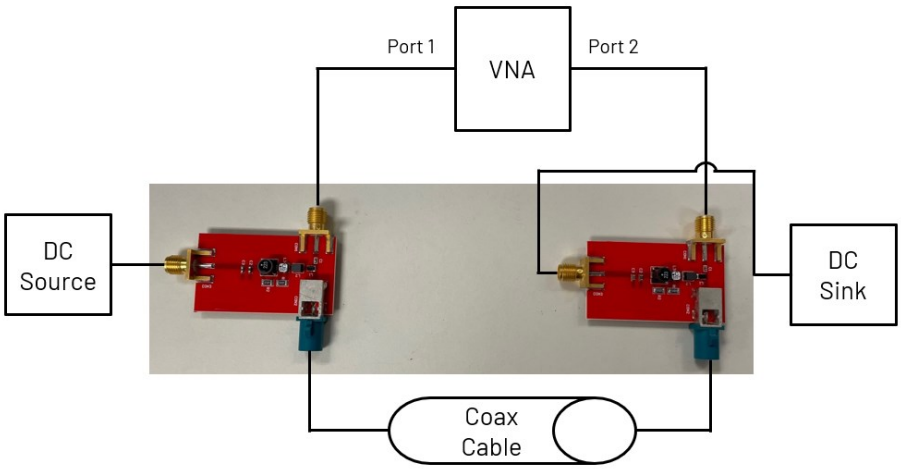
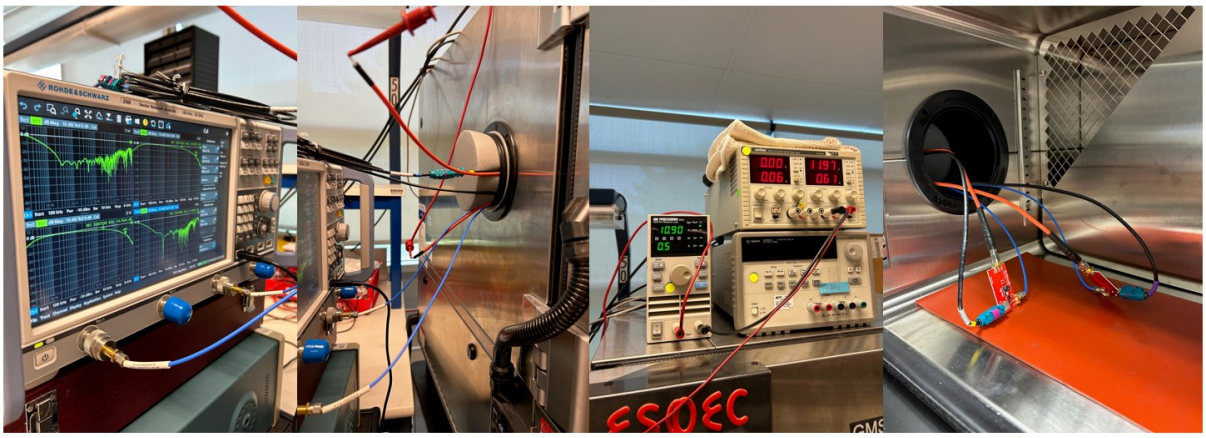



***Figure 42. Block Diagram of PoC Coupon Board S-Parameters Testing with Various Cable Lengths, Current Loads, and Temperatures***



2-port VNA with majority of 15.5M Coax Cable outside of oven

SMA Cables from VNA going into Oven

DC Power Supply and Electronic Load

PoC coupon boards inside oven chamber

***Figure 43. PoC Coupon Board Test Setup***

**Production System Testing**

See *Hardware Channel Measurements* section for more information on testing with Production hardware.

## PoC Layout Recommendations

Following are the PoC component placement, routing, and cutouts to reduce the amount of capacitance:

-Placement and Routing:

- Place all PoC components on the same layer and minimize distance between IC, PoC, and connector.
- If the GMSL3 trace is longer than 2 inches, it is suggested to place the PoC as close as possible to the IC.
- Do not add vias. The added inductance may create unwanted filter response.
- Place lowest inductor value directly on the GMSL3 serial link trace followed by the next highest and so on (see *Figure 44* for a placement example).
- Minimize distance between inductors. Spacing between the first and second inductor is the most critical; ensure that trace is as short as possible.

-Ground Cutouts:

- Remove the ground plane beneath Node 1 and Node 2 to reduce parasitic capacitance to maintain best impedance matching on GMSL3 trace. Full PoC circuit cutout can also be done. But, at minimum, ground plane between Node 1 and Node 2 needs to be removed.

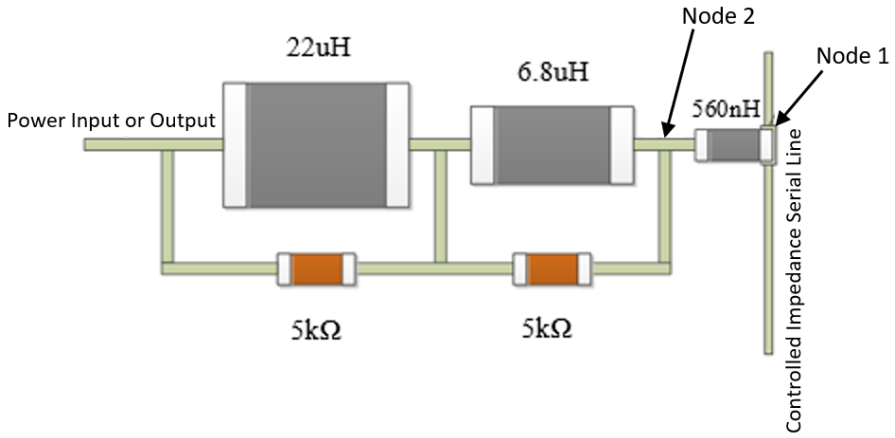



***Figure 44. PoC Placement Strategy***

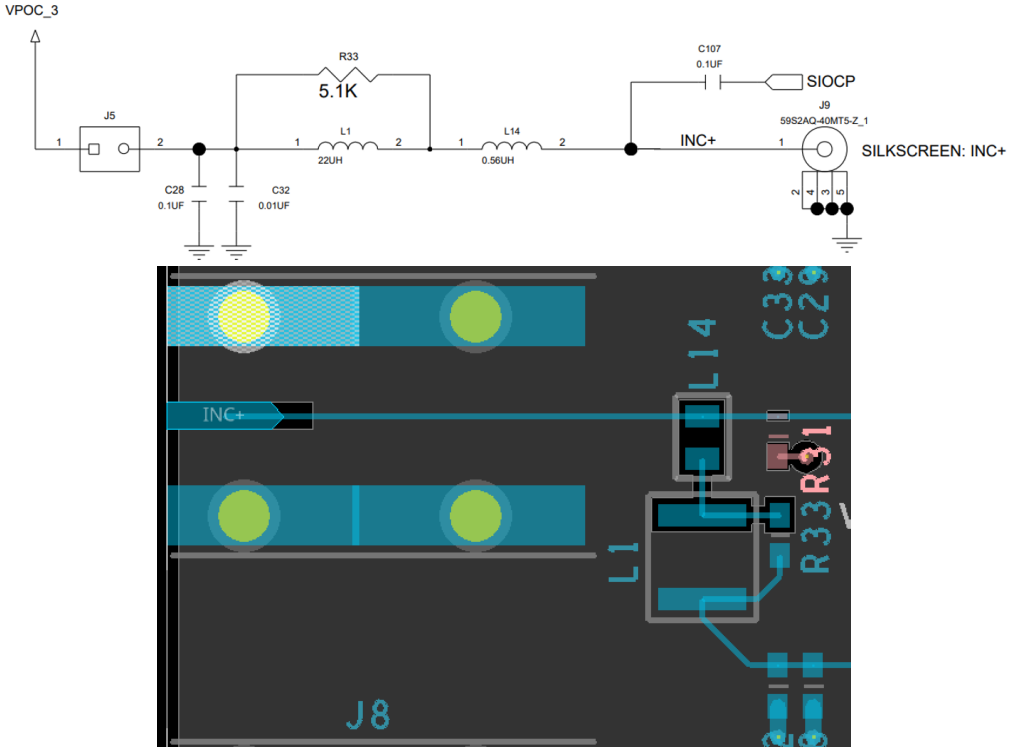



***Figure 45. PoC Layout Example***

## PoC Reference Circuits

Analog Devices works with inductor vendors to come up with the best PoC circuits (performance, size, and cost) that can be used in a GMSL3 system. The following table contains reference PoC circuits that Analog Devices recommends for new designs. They have been evaluated for performance against the GMSL3 Channel Specification but are not guaranteed to meet all customer use cases. Reach out to inductor vendors directly or visit their website for more information.

Customers are still responsible for verifying their chosen PoC circuit (Analog Devices recommended or custom solution) meets the GMSL3 Channel Specification for their given system.

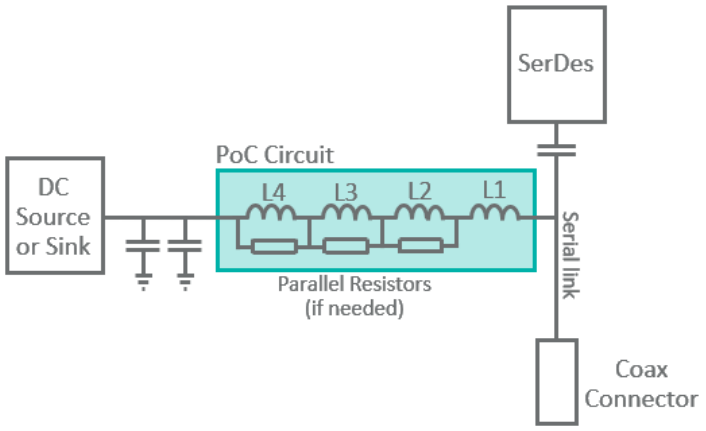



***Figure 46. Schematic for PoC Reference Circuits***

**Table 5. Recommended GMSL3 PoC Solutions for New Designs**

| # | Circuit Name /Manufacturer | Component Part # | Inductance Values | Other Current Ratings | Notes |
|---|---|---|---|---|---|
| **300mA Solutions** | | | | | |
| **1** | C-2L-300-1/Coilcraft | L1: PFL1609-102<br>L2: 1210POCB-223 \|\| 5.1kΩ | L1: 1uH<br>L2: 22uH | 300mA @125C,<br>400mA @105C | |
| **2** | M-1L-300-0/Murata | L1: LQW32FT220M2H | L1: 22uH | | |
| **3** | M-2L-300-0/Murata | L1: LQW21FT2R0M0H<br>L2: LQH3NPH680MME \|\| 1kΩ | L1: 2uH<br>L2: 68uH | | |
| **400mA Solutions** | | | | | |
| **4** | T-1L-400-0/TDK | L1: ADL4524VL-180M-TL000 | L1: 18uH | | |
| **5** | T-2L-400-1/TDK | L1: ADL2012-2R2M-T01<br>L2: VLS3015CX-220M-H \|\| 1kΩ | L1: 2.2uH<br>L2: 22uH | 500mA @85C | |
| **500mA Solutions** | | | | | |
| **6** | C-2L-500-0/Coilcraft | L1: PFL1609-561<br>L2: 1210POC-223 \|\| 5.1kΩ | L1: 560nH<br>L2: 22uH | 400mA @125C,<br>600mA @85C | |
| **7** | T-2L-500-0/TDK | L1: MLJ1608WGCR56NTD25<br>L2: ADL32VHC-220M \|\| 1kΩ | L1: 560nH<br>L2: 22uH | | |
| **600mA Solutions** | | | | | |
| **8** | T-1L-600-0/TDK | L1: ADL8030VA-220M | L1: 22uH | | |
| **9** | T-2L-600-0/TDK | L1: ADL2012-1R5M-T01<br>L2: ADL32VHC-150M \|\| 1.5kΩ | L1: 1.5uH<br>L2: 15uH | | |
| **10** | M-3L-600-01/Murata | L1: LQW21FTR82M0H<br>L2: LQW32FT4R7M0H<br>L3: LQH44PH220MPR \|\| 1kΩ | L1: 0.82uH<br>L2: 4.7uH<br>L3: 22uH | | |
| **800mA Solutions** | | | | | |
| **11** | T-2L-800-0/TDK | L1: ADL3225VF-2R0M-TL000<br>L2: ADL4532VK-160M-TL000 \|\| 1kΩ | L1: 2uH<br>L2: 16uH | | |
| **12** | M-3L-800-0/Murata | L1: LQW32FT2R2M0H | L1: 2.2uH | | |

| # | Circuit Name /Manufacturer | Component Part # | Inductance Values | Other Current Ratings | Notes |
|---|---|---|---|---|---|
| | | L2: LQW32FT2R2M0H<br>L3: LQW43FT180M0H \|\| 1kΩ | L2: 2.2uH<br>L3: 18uH | | |
| **13** | CY-2L-800-0/Cyntec | L1: VCSF20121H-1R5MS2<br>L2: VCSF32253A-150MS5 \|\| 2kΩ | L1: 1.5uH<br>L2: 15uH | 850mA @105C | |
| | | **1000mA Solutions** | | | |
| **14** | M-3L-1000-0/Murata | L1: LQW32FT3R6M8H<br>L2: LQW32FT3R6M8H<br>L3: LQH44PH100MPR | L1: 3.6uH<br>L2: 3.6uH<br>L3: 10uH | | |
| | | **1200mA Solutions** | | | |
| **15** | T-3L-1200-0/TDK | L1: ADL3225VF-2R0M-TL000<br>L2: TFM201210ALMA1R5MTAA \|\| 1.5kΩ<br>L3: VLS5030EX-220M-D \|\| 1.5kΩ | L1: 2uH<br>L2: 1.5uH<br>L3: 22uH | | |
| | | **1300mA Solutions** | | | |
| **16** | M-3L-1300-0/Murata | L1: LQW32FT1R6M8H<br>L2: LQW32FT1R6M8H<br>L3: MDH6045C-220MA \|\| 1kΩ | L1: 1.6uH<br>L2: 1.6uH<br>L3: 22uH | | |

**Note(s)**:

- PoC circuits are validated and approved by Analog Devices at 12V and 105°C. In some cases, additional current/temperature combinations are validated and approved for a given PoC circuit. Additional current/temperature combinations are noted in “Other Current Ratings” column.
- Due to GMSL3 Channel Specification being more stringent than GMSL2, all GMSL3 PoC solutions are approved for GMSL2.

# ESD Guidelines

## Overview

Electrostatic discharge (ESD) is the build of charge which imposes high-current events that can catastrophically damage electronics in a powered or unpowered system. ESD current takes the path of least resistance. ESD protection (internal or external) can be used to divert these currents from important circuitry. The GMSL3 devices contain internal ESD protection devices to help divert high instantaneous currents during an ESD event.

System Level ESD testing (also known as Powered ESD testing) is not the same as chip level unpowered ESD that is referenced in device data sheets. The chip-level unpowered ESD guarantee in the data sheet only guarantees no physical damage for an ESD event per ISO10605 Section 3 and does not guarantee operation during an external ESD discharge event in the system level ESD testing. System level ESD is performed by the Tier 1 or OEM when a completed system is put together. System level ESD is performed typically with a Head Unit (HU) to display in the case of an In Vehicle Infotainment (IVI) system or HU to camera in the case of an ADAS.

The proper design of protecting the IC chips preclude the ESD discharge from ever reaching the IC. If the ESD discharge reaches the IC, the ESD structures short the pins to ground to protect the IC chip from taking all of voltage and current going through the IC. Once it reaches this point, the ESD protection diodes internal to the chip shunt the pin(s) to ground. When this happens, the desired functionality of the chip is disrupted until the ESD event has stopped.

- System Level ESD involves ALL components in the system and the interaction between ALL the components.
- Remember system level ESD testing causes the ESD protection diodes to shunt the discharge to ground.
- It starts with protecting all its components on the PCB board from a direct hit from an external ESD discharge.
- The PCB board, IC components, and enclosure need to be initially designed to redirect the external ESD before it can reach the ICs on the PCB.

*Figure 47* shows basic GMSL3 Deserializer PHY output and internal ESD structure.

*Figure 48* shows basic GMSL3 Serializer PHY output and internal ESD structure.

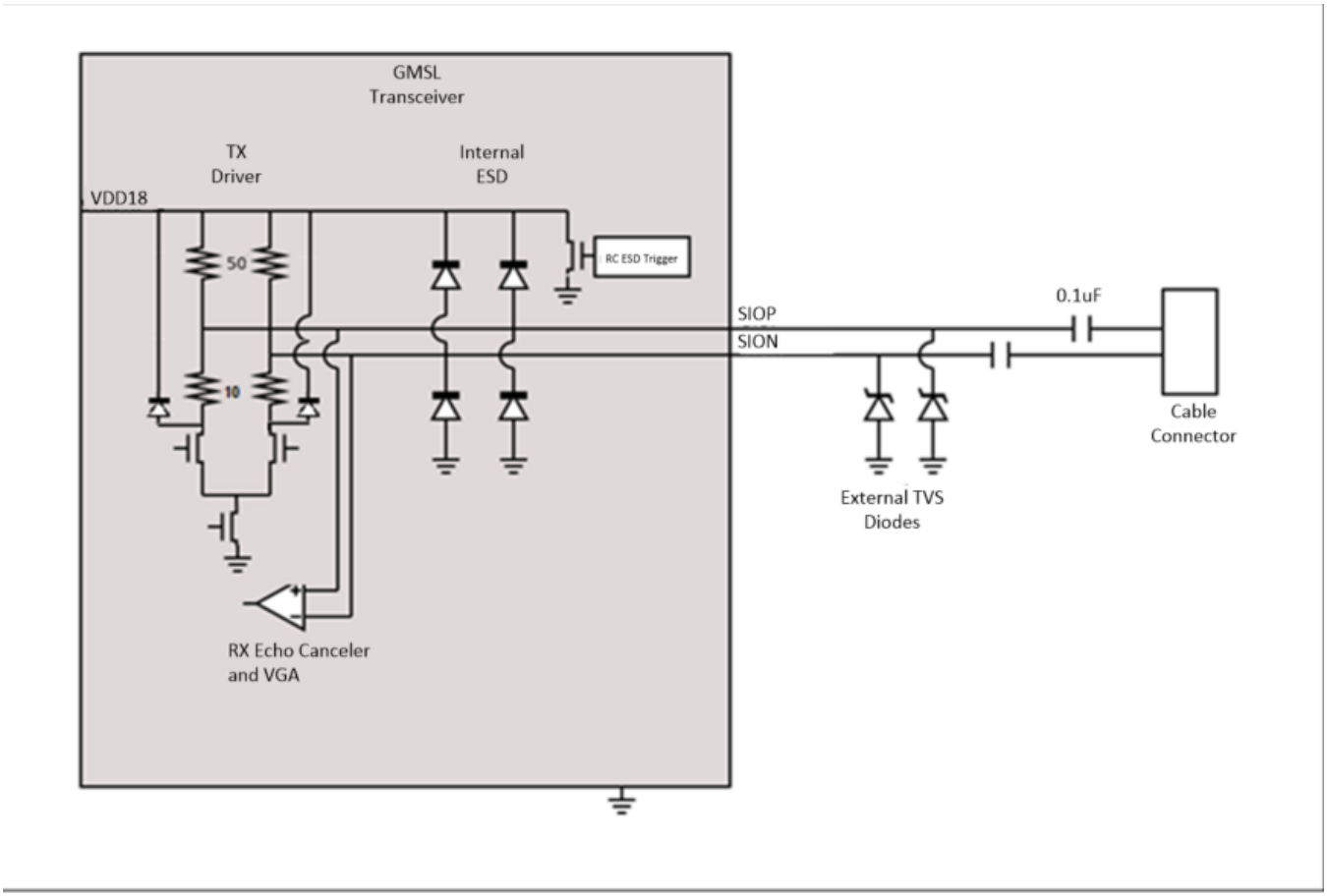



***Figure 47. GMSL3 Deserializer PHY Output Structure with ESD Devices***

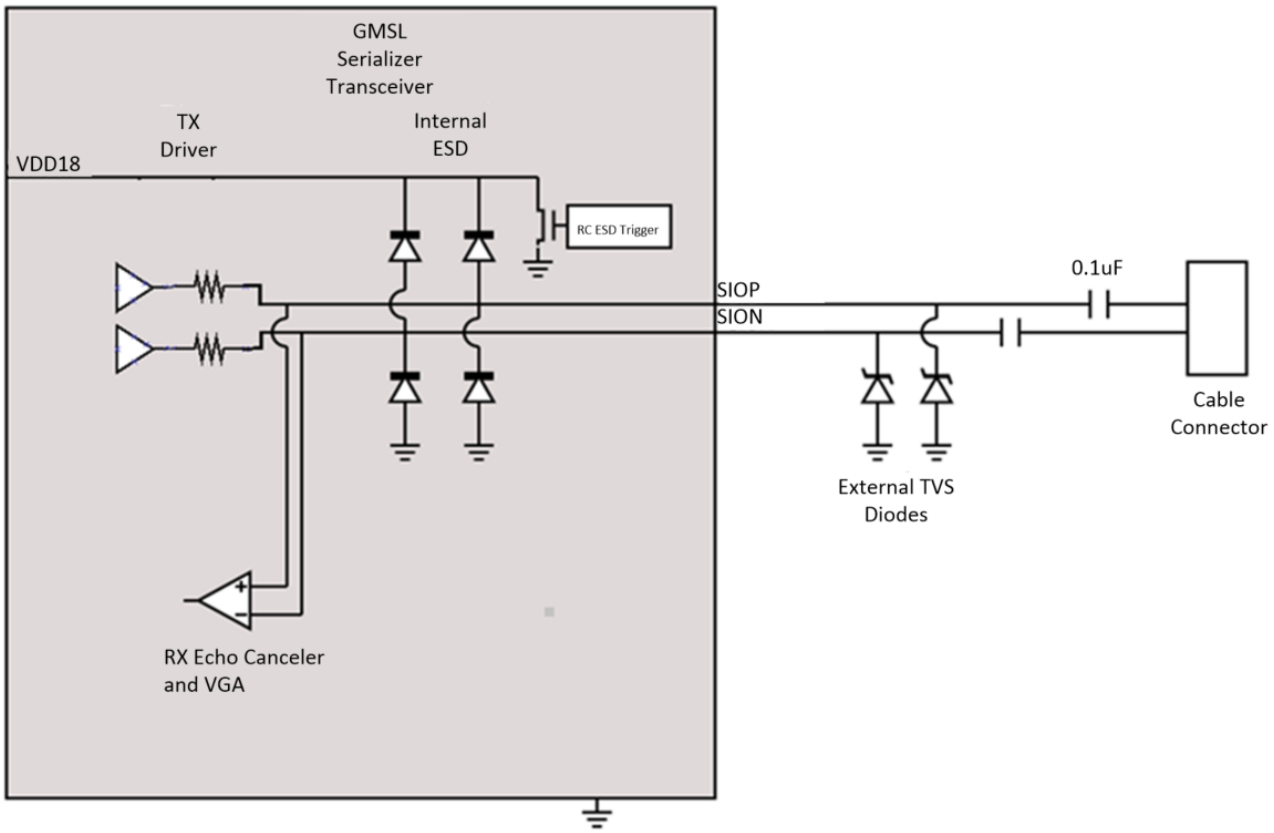



***Figure 48. GMSL3 Serializer PHY Output Structure with ESD Devices***

## Shielding and Grounding Recommendations for ESD and EMI Protection

Simply adding more grounds or placing a shield to fight against ESD/EMI events do not allow for complete ESD/EMI immunity. For this reason, the system level design becomes more important, and the industry best practices must be followed.

While shielding is always recommended, it is important to note there is increased susceptibility on GMSL3 as there is a tradeoff of lower margin for a higher data rate in PAM4 modulation mode.

PAM4 is utilized to achieve higher data rather than NRZ. To achieve 12Gbps rate using NRZ, the fundamental frequency increases two times to 6GHz which increases the signal attenuation through a cable. Cable attenuation at fundamental frequency with a worst-case cable is around 8dB higher for 12G NRZ vs. 12G PAM4 equivalent throughput. While PAM4 may offer lower margin as mentioned, the following tradeoff offers advantages of PAM4 over NRZ.

- PAM4 horizontal eye opening is larger than NRZ at the same bit rate because PAM4 UI is 100% larger.
- PAM4 RX bandwidth can be lower than NRZ, reducing vulnerability to higher frequency interference sources.

Be aware of the additional susceptibility to broadband noise inherent in using the PAM4 protocol as opposed to the NRZ protocol. Any ESD or EMI events that may not have had significant effects (i.e., loss of lock) on a GMSL2 system, can have additional effects on a GMSL3 system because of the lower margin of the additional modulation level.

**Note**: This lower margin can be improved by using differential mode as opposed to single-ended mode. However, robustness is still recommended through good shielding and grounding.

As shown in *Figure 49*, the PAM4 eyes have one-third vertical height of NRZ eye assuming identical peak-peak transmit level. The GMSL transmit level PAM4 is increased to 467mV relative to 410mV for NRZ.

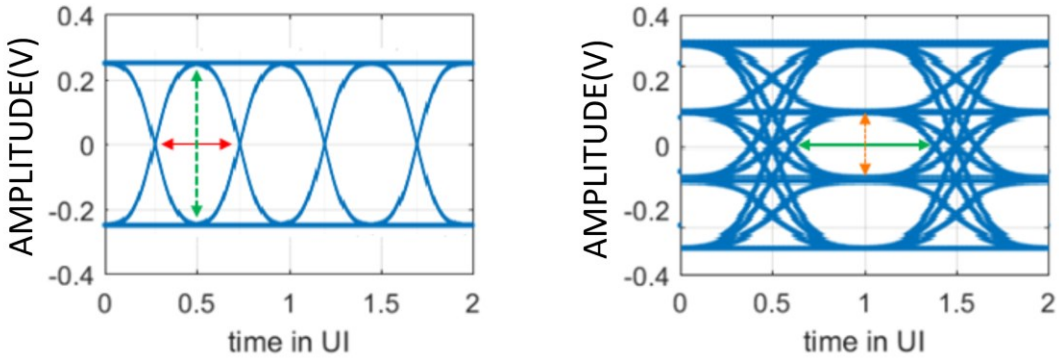



***Figure 49. NRZ and PAM4 Eye Diagrams***

Comparing GMSL PAM4 and NRZ transmit level, vertical eye opening for a given baud rate is approximately 8.4dB smaller for PAM4.

$$\frac{GMSL3\ Eye}{GMSL2\ Eye}[dB] = 20 \times LOG_{10}\left(\frac{467mV/3}{410mV}\right) = -8.4dB$$

Thus, the following guidance is provided to highlight the need for increased system level awareness for the prevention of noise susceptibility. Considering some signal integrity best practices is a great way to easily avoid difficult problems.

The user should design with appropriate shielding and grounding in the following ways:

- PCB
  - Maximize GND Fill and maintain continuity of GND planes.
    - Create board capacitance using equal-sized power plane and ground plane surface area adjacent to each other.
    - Eliminate any floating copper pours or islands by generously stitching to the ground plane.
    - Ground peninsulas should be stitched generously to the ground layer to avoid antenna effects.
  - Use good power supply decoupling. Decoupling values may need to be modified/changed after completed system testing.
  - Optimize PCB to connector interface for optimal ground connectivity and signal quality.
    - When using through hole connectors to connect the high-speed trace, connect at the tip end of the center conductor. Do not make the high-speed trace connection at the housing side of the center conductor. Making the connection at the housing side of the center conductor creates a stub.
    - Do not cut up or isolate the ground plane at the high-speed connector.
  - Reducing high-speed trace impedance discontinuities:
    - Minimize impedance discontinuities.

        - Use one continuous high-speed GMSL trace(s) on one side of board if possible. If not possible, ensure proper transition between layers and removal of any stubs.
        - Impedance discontinuities, if unavoidable, should be lumped together. For the GMSL trace(s), place close to the AC series capacitor. DO NOT have impedance discontinuities in the center of a high-speed trace.
        - Consider using differential stripline construction for the best protection of the high-speed signals.
    - Protect the high-speed traces with adjacent ground and generously stitch to the ground plane.
    - Consider using differential mode with 100Ω differential traces to provide common mode rejection and this also doubles the amplitude as compared with using single-ended mode which uses a single 50Ω trace.
    - Have a continuous ground surrounding the edge of the PCB. Generously stitch the edge ground together.
- Cable
    - Cables with low loss and good shielding provides best performance.
    - Ensure cables have proper shielding for broadband frequency coverage and good connection to end connectors.
    - Connectors with good ground connection and signal transmission characteristics provide the best performance.
- Shield hardware modules when possible.
    - Consider metal enclosure shield options that can help protect sensitive interconnects and connectors from large ground currents and noise pickup.
    - Have a low-impedance connection from system hardware ground to chassis ground to provide a local and low-impedance path to discharge.
- Operation
    - Avoid using GMSL data rates that are unnecessarily high for the application.

All these measures are to prevent a direct strike on any component in the system PCB. It is especially crucial not to allow an ESD strike on any I/Os, as a direct strike causes the internal ESD protection on not only the GMSL SerDes, but on any IC within the system to turn on. When the internal ESD protection diode turns on, it shunts the ESD discharge to ground to protect itself. When the ESD protection diode is on, this shorts the I/O(s) until the ESD event has stopped.

**System-Level ESD Recommendations and References**

The system-level ESD performance level is dependent on the end system design. See the Shielding and Grounding recommendations for optimal design suggestions.

During Powered ESD Tests, it is important to keep in mind that under such stress, the GMSL link may briefly lose link lock and recover. Notice that the data sheet guaranteed value is for the nonpowered ESD testing. In this scenario, Analog Devices guarantees no sustained damage to the IC, and proper operation afterwards.

Consider using GMSL2 over GMSL3 if the throughput is within the bandwidth of the GMSL link. If using GMSL3 mode, use differential mode over single-ended mode for increased noise margin. Differential mode doubles the amplitude over single-ended mode.

$$\frac{GMSL3\ Eye}{GMSL2\ Eye}[dB] = 20 \times LOG_{10}\left(\frac{(467mV/3) \times 2}{410mV}\right) = -2.39dB$$

Forward Error Correction (FEC) is default in GMSL3 mode which adds more robustness to the GMSL3 operation.

Additional shielding and grounding may be required dependent on the system-level ESD level requirement. Higher category levels require even more careful consideration of system design. The ISO 10605:2023 has different severity levels:

Annex C (informative) Function performance status classification (FPSC) section C.2. Per the specification *"It has to be emphasized that, as described in this document, components or systems shall only be tested under the conditions that represent the simulated automotive electromagnetic environments to which the devices would actually be subjected. This will help to ensure a technically and economically optimized design for potentially susceptible components and systems.It should also be noted that this annex is not intended to be a product specification and cannot function as one. It should be used in conjunction with a specific test procedure in this document. Therefore, no specific values for the test signal severity level are included in this annex since they should be determined by the vehicle manufacturers and component suppliers. Nevertheless, using the concepts described in this annex and by careful application and agreement between manufacturer and supplier, this annex can be used to describe the functional status requirements for a specific device. This can then, in fact, be a statement of how a particular device can be expected to perform under the influence of the specified test signals."* [1]

**Table 6. Vehicle Test — Example Severity Levels for Contact Discharge (Test Points Accessible Only from Inside Vehicle) [1]**

| Test Severity Level | | Category 1 | Category 2 | Category 3 |
|---|---|---|---|---|
| **L4i** | | ±6 kV | ±8 kV | ±8 kV |
| **L3i** | | ±4 kV | ±4 kV | ±6 kV |
| **L2i** | | ±2 kV | ±2 kV | ±2 kV |
| **L1i** | | Not Applicable | Not Applicable | Not Applicable |

**Table 7. Vehicle Test — Example Severity Levels for Air Discharge (Test Points Accessible Only from Inside Vehicle) [1]**

| Test Severity Level | Category 1 | Category 2 | Category 3 |
|---|---|---|---|
| **L4i** | ±8 kV | ±15 kV | ±15 kV |
| **L3i** | ±6 kV | ±8 kV | ±8 kV |
| **L2i** | ±4 kV | ±4 kV | ±6 kV |
| **L1i** | ±2 kV | ±2 kV | ±4 kV |

**Table 8. Vehicle Test — Example Severity Levels for Contact Discharge (Test Points Accessible Only from Outside Vehicle) [1]**

| Test Severity Level | Category 1 | Category 2 | Category 3 |
|---|---|---|---|
| **L4i** | ±6 kV | ±8 kV | ±8 kV |
| **L3i** | ±4 kV | ±6 kV | ±6 kV |
| **L2i** | ±2 kV | ±2 kV | ±4 kV |
| **L1i** | Not Applicable | Not Applicable | ±2 kV |

**Table 9. Vehicle Test — Example Severity Levels for Air Discharge (Test Points Accessible Only from Outside Vehicle) [1]**

| Test Severity Level | Category 1 | Category 2 | Category 3 |
|---|---|---|---|
| **L4i** | ±15 kV | ±15 kV | ±25 kV |

| | | | |
|---|---|---|---|
| **L3i** | ±8 kV | ±8 kV | ±15 kV |
| **L2i** | ±4 kV | ±6 kV | ±8 kV |
| **L1i** | ±2 kV | ±4 kV | ±6 kV |

[1]Tables from BS ISO 10605:2023 Road vehicles — Test methods for electrical disturbances from electrostatic discharge and statement of FPSC approach section C.2

## ESD Test Standard

Analog Devices currently specifies system ESD passing levels using the ISO10605 automotive test standard. (*https://www.iso.org/standard/79094.html*).

Analog Devices primarily focuses on the component packaging and handling test method (unpowered test). Within the ISO10605 test standard, the unpowered test section outlines all details of the test, such as the required ESD Gun RC networks, stress points, methods to access stress points, distances between test structures, GND connections, etc.

Refer to the ISO10605 test standard for more details.

## TVS Diode Characteristics

Analog Devices' GMSL3 device data sheets specify nominal ESD passing levels without additional external ESD protection. If the system designer requires better ESD protection, external transient voltage suppression (TVS) diodes can be used. Adding TVS diodes comes as a trade-off as they add additional capacitance and degrade the GMSL3 signal integrity performance.

Ideal external TVS diodes should have the following properties:

- Capacitance of <0.5pF or less to prevent degradation of high-speed GMSL3 signal
- Small package footprint to minimize capacitance
- Low breakdown voltage and low clamping voltage
- Unidirectional, reverse-biased onto the link
- Two-port component to minimize lane-to-lane crosstalk

The external TVS is required to have less than 10V breakdown/clamping voltage due to the internal structure of the ESD diodes. If the external TVS diodes have greater than 10V breakdown/clamping voltage, during an ESD event, then the internal diodes may conduct first and damage the internal circuitry before the external diodes can assist with diverting the high currents.

Unidirectional TVS diodes should be used. External bidirectional diodes are not recommended due to the internal structure of the SerDes ESD protection. While the bidirectional diodes may help with the positive polarity ESD events, most often the protection in the negative polarity does not become active before damaging the internal driver.

### TVS Diode Placement by Use Case

For systems utilizing line fault or PoC, it is recommended to place the unidirectional TVS diode on the chip-side of the AC series coupling capacitor. See *Figure 50*.

For systems that are not using PoC or line fault, TVS diode can be placed on the connector side of the AC series coupling capacitor. See *Figure 51*.

**PoC Use Cases**

To use a TVS diode on the connector side of coupling capacitor while using PoC, the diode would need to have a higher breakdown voltage than the PoC voltage to avoid shorting line to GND.

As example, with a typical 12V PoC system you can use a TVS diode with a 13V breakdown voltage (higher than PoC voltage). When an ESD event occurs, the external TVS diode would not conduct until reaching minimum voltage of 13V. This exposes the internal circuitries of the SerDes devices to ESD event which can lead to damage.

Instead, placing the TVS diode on the chip-side of the coupling capacitor allows TVS breakdown voltage to be independent of the PoC voltage. This is due to the coupling capacitor blocking the PoC DC voltage.

See *Figure 50* for block diagram of TVS diode placement when using PoC.

**Line Fault Use Cases**

A line fault short-to-battery condition may damage the TVS diode depending on the duration of the event. A typical ESD event is on the order of microseconds. Depending on the line fault condition, the external diode might be damaged, unless it was protected by the AC coupling capacitor.

Placing the TVS diodes on the chip-side of the AC series coupling capacitor can allow line fault (no PoC) to be used.

See *Figure 50* for a block diagram of TVS diode placement when using line fault.

**TVS Diode Placement Block Diagrams**

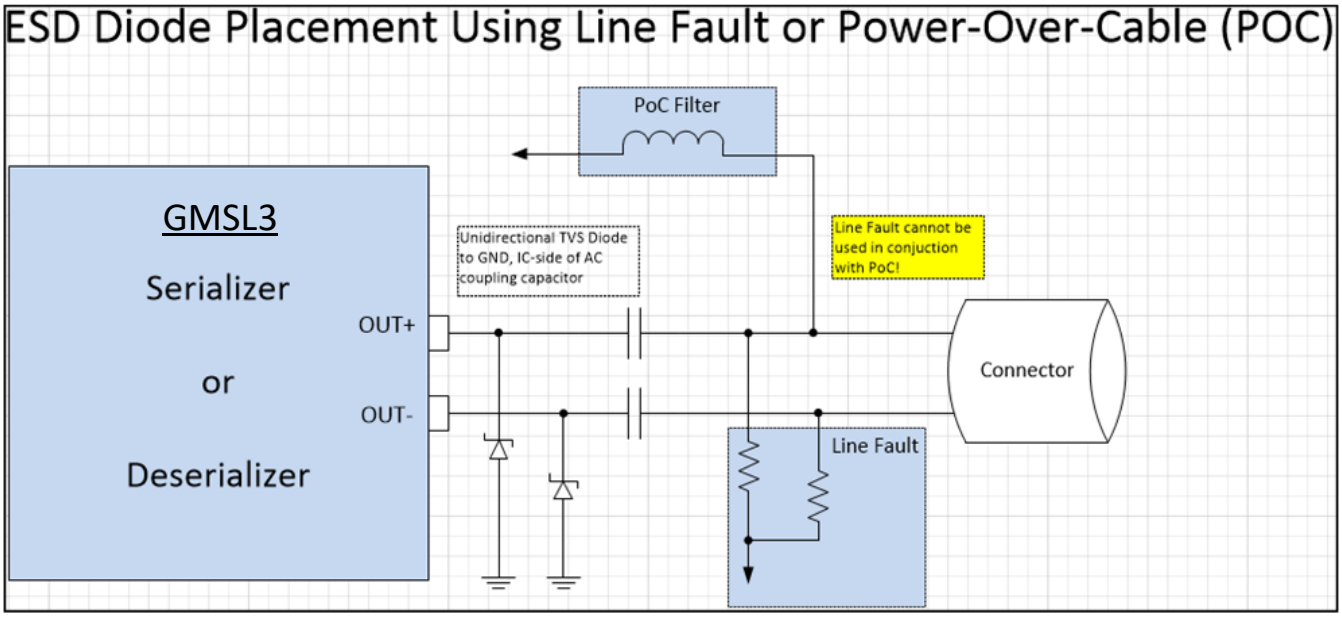



***Figure 50. Recommended ESD Placement with Line Fault or PoC***

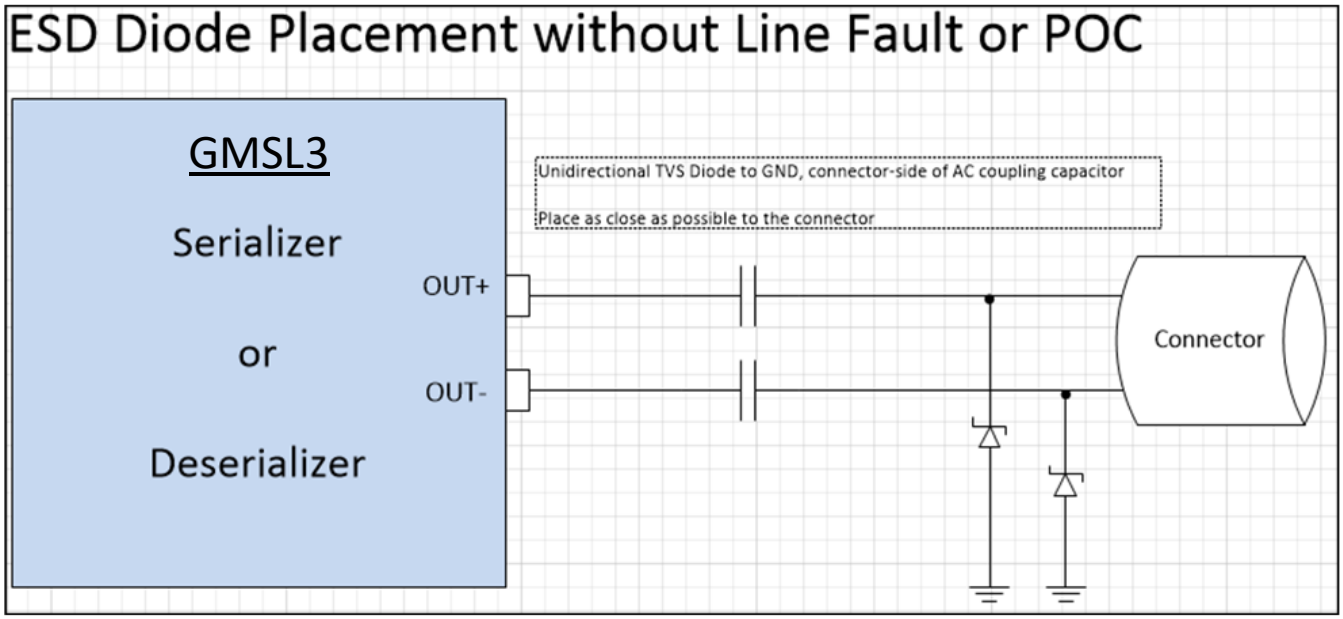



***Figure 51. Recommended ESD Placement without Line Fault or PoC***

**TVS Diode Component Layout**

The TVS diode device should be placed directly onto the serial link trace. There should be no stubs from the serial link trace to any component on the net. A 1.35x GND cutout should be implemented on the pad of the TVS diode. The GND path of the TVS diode should be a low-resistance, large plane, with embedded vias for best ESD performance. See *Figure 52* for an example of this implementation.

General Layout Guidelines

- The IC-to-be-protected should be as far away as possible from the potential ESD event.
- Avoid stubs on the signal path of the TVS diode.
- Minimize inductances between the TVS diode and ground.
- Diodes should connect directly to the ground plane.
- If placing the TVS diode on the connector side of the serial link, place the TVS diode as close as possible to the connector.

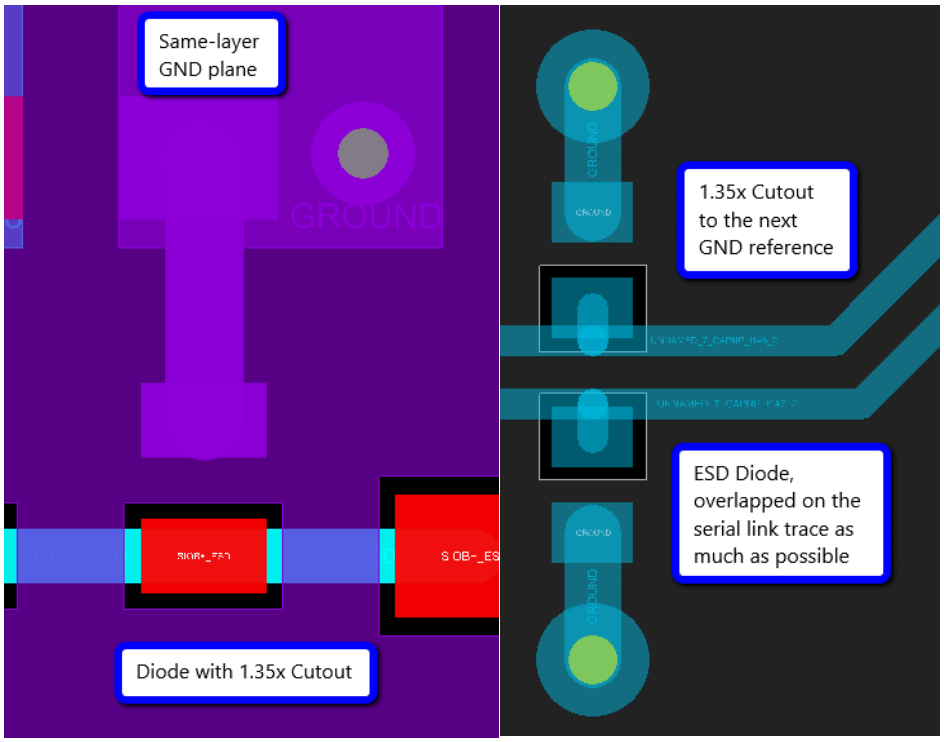



***Figure 52. TVS Diode Layout Placement with Cutout Example***

## Common Mode Filtering

Analog Devices does neither test nor validate common mode filter (CMF)/common mode chokes (CMC) for GMSL3 systems. It does not recommend specific part numbers. If the system designer chooses to add a CMF/CMC, they must verify the system passes the GMSL3 Channel Specification.

## Optimizing Cable Segments for Best Performance

There are many factors that need to be taken into consideration when building a GMSL3 channel. Key items on cable segments are listed as follows:

1) Avoid using cable interconnects as much as possible, as they can be sources of signal reflections. These signal reflections make it more difficult to pass the GMSL3 return loss specification.
2) The deserializer is more sensitive to reflections than the serializer. For this reason, short cable segments are better placed on the serializer side of the link.

# Hardware Validation Tools

The GMSL3 includes on-chip signal integrity tools to assess the quality of the GMSL3 link. These tools are available through the Analog Devices GMSL3 GUI. Alternatively, software support is available for customers who wish to develop their own implementation of these tools in their software. This section begins with a summary of typical results from the tools and explains each tool in detail.

**Table 10. GMSL3 Signal Integrity Tools**

| Tool | Description |
|---|---|
| **Link Margin** | Reduces the transmit amplitude until errors are detected for both the forward and reverse channels. Indicates the voltage margin of the transmitted signal. |
| **Eye Mapper** | Uses the eye-opening monitor (EOM) as an on-chip oscilloscope to display the equalized received signal along with displaying the equalizer coefficients being used. |
| **Forward Error Correction** | Reports FEC input and output BER, including number of blocks processed and number of bits corrected. Only available on GMSL3 products that support FEC. |

## Forward Channel Typical Performance

Typical performance data is provided in this section as a reference to compare the systems' underdevelopment. Systems that fall within these ranges under nominal conditions are operating as expected. The GMSL3 signal integrity tools allow the user to measure each of these parameters for their system.

*Table 7* and *Table 8* are examples of typical forward channel link margin performance on the described GMSL3 SerDes devices that follow. Data was taken on Analog Devices SerDes evaluation boards with nominal voltages and at room temperature.

Typical operating performance is measured for short (0.9m), medium (7m), and long (15.5m) coax cables (Leoni Dacar 302 cable with Rosenburger Fakra edge-launch connectors), with insertion loss as shown in the following figure.

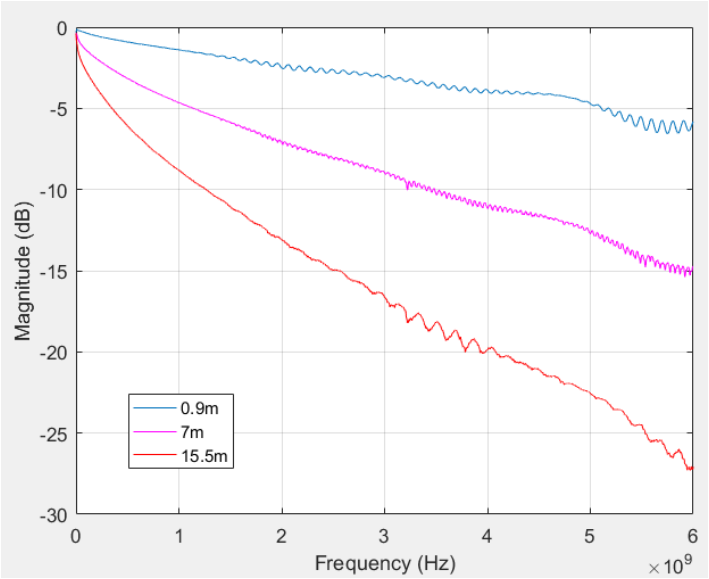



***Figure 53. Insertion Loss of Test Channels***

**Table 11. Typical Forward Channel Performance with MAX96793-MAX96792A**

| MAX96793-MAX96792A Typical Forward Channel Performance | | | | |
|---|---|---|---|---|
| **Data Rate** | **Coax Length (Note 1)** | **S21 (1.5GHz/3GHz) (Note 2)** | **Clock Source** | **Link Margin (Note 3)** |
| 12Gbps/187Mbps | 1m | -3.89/-6.13dB | RoR | 367mV |
| | | | XTAL | 367mV |
| | 7m | -7.58dB/-11.31dB | RoR | 345mV |
| | | | XTAL | 345mV |
| | 13.5m | -13.13/-18.79dB | RoR | 292mV |
| | | | XTAL | 314mV |

**Note(s)**:

- Note 1: m=meter. The 7m cable is composed of 5m and 2m sections. The 13.5m cable is composed of 10m, 3m, and 0.5m sections. STP cable performance is similar to Coax cable performance when the insertion losses (Sdd21 and S21) are equivalent. Note that equivalent performance Coax and STP cables have different lengths due to the difference in loss-per-meter between Coax and STP.
- Note 2: Insertion loss includes the cable, interconnects, and PCB traces on the serializer and deserializer boards.
- Note 3: Link Margin (LM) is the difference between the default transmitter amplitude and the reduced amplitude at which errors are detected. Larger numbers indicate more margin.
- Note 4: Device Revisions Used: MAX96793 dev_rev=0x06, MAX96792A dev_rev=0x06
- Note 5: GUI 6.6.3 used for link margin testing.
- Note 6: Clock Source XTAL=Crystal Mode, RoR=Reference over Reverse Mode; Refer to data sheet and application notes for more information.

## Link Margin Tool

The link margin tool allows quantitative testing of the noise quality of the GMSL3 link. The link margin test starts at the default transmit voltage amplitude for the forward channel and reverse channel. The test decreases the transmit amplitude in 10mV steps, and at each step it performs an FEC input BER check before proceeding to the next amplitude. When FEC input BER > 1e-7 is detected, the test is over. Link margin is reported as the difference between the default transmitter amplitude and the amplitude at which an error was detected. The test can be performed for both forward and reverse channels.

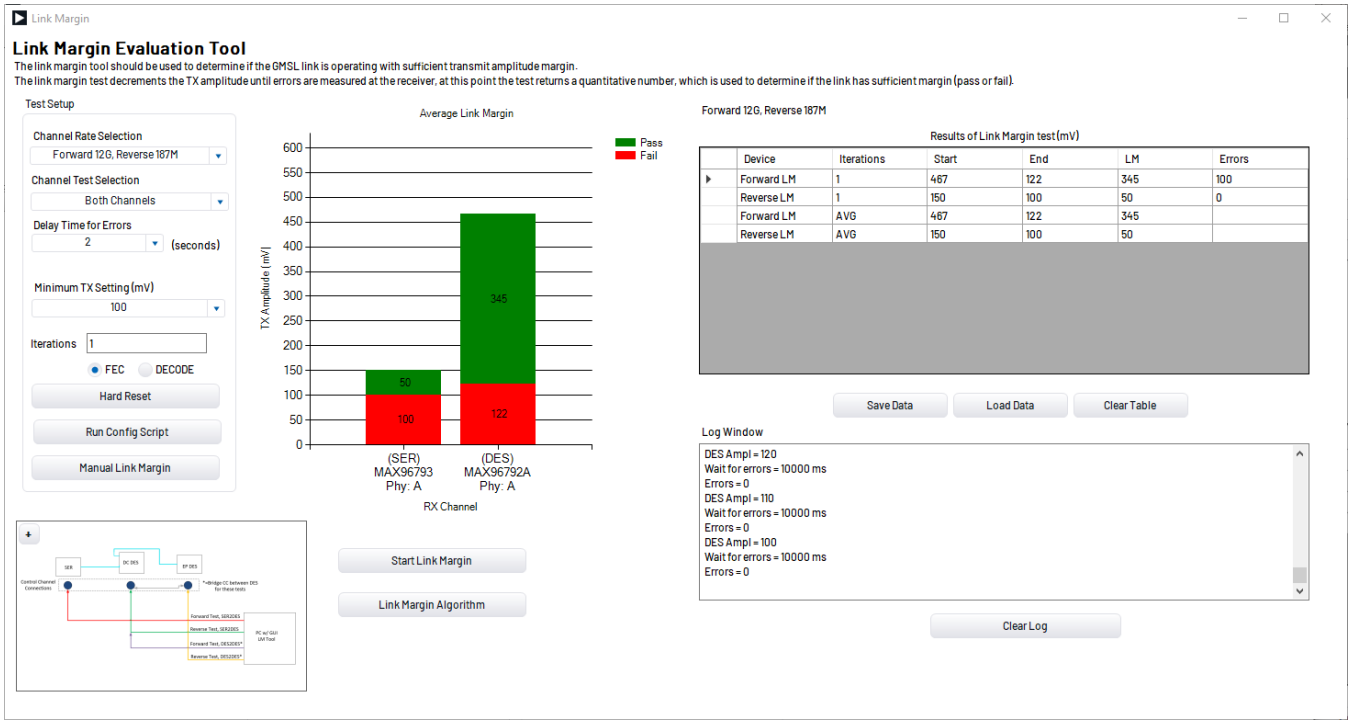



***Figure 54. GMSL3 Link Margin Test (Reverse Channel 50mV Margin, Forward Channel 345mV Margin)***

## Eye Mapper Tool

The Eye Mapper tool uses the on-chip EOM to generate an eye diagram of the equalized received signal. It functions as an on-chip oscilloscope to display the recovered signal and the equalizer coefficients being used. The equalizer automatically adjusts to compensate for loss in the channel and ensures best possible BER.

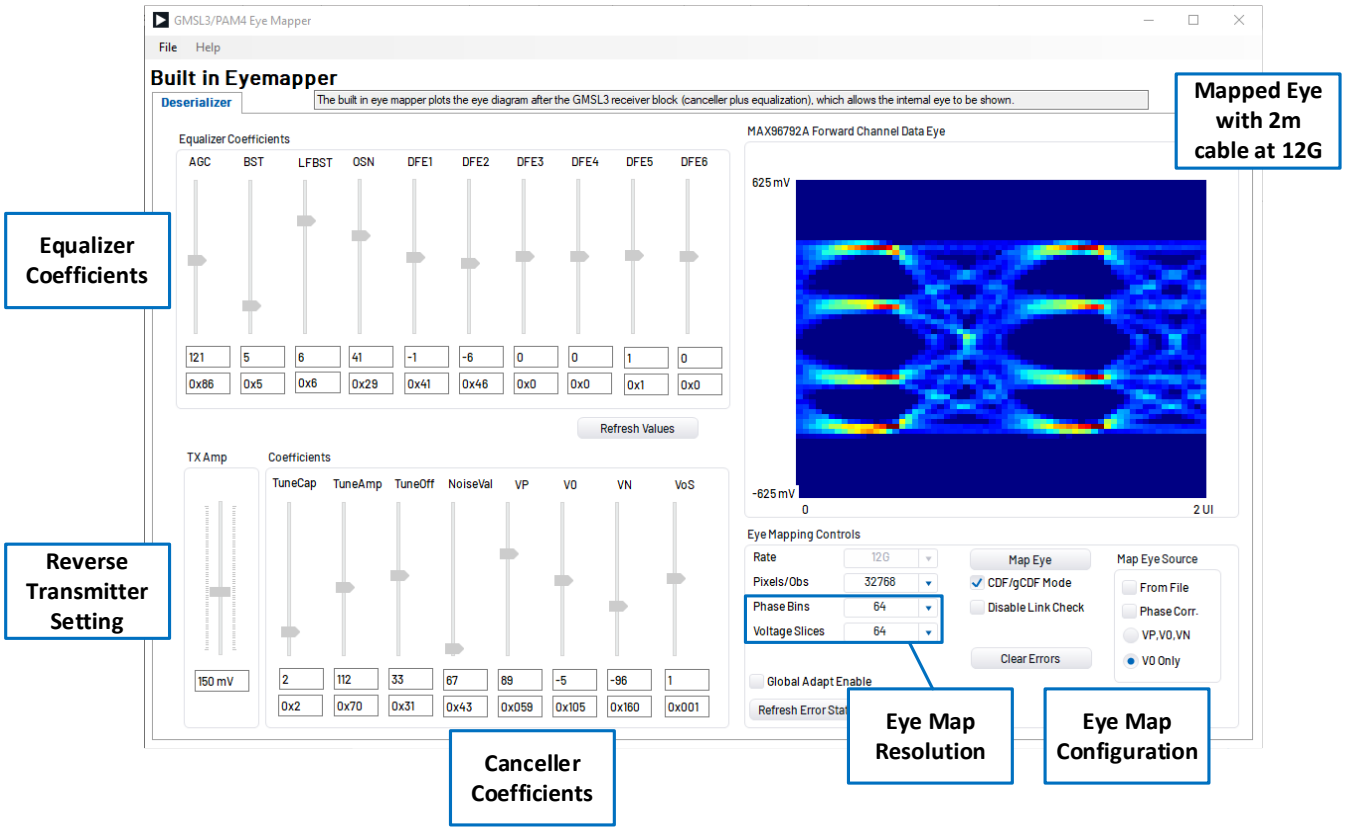



***Figure 55. GMSL3 GUI Eye Mapper Tool, 12Gbps PAM4 Forward***

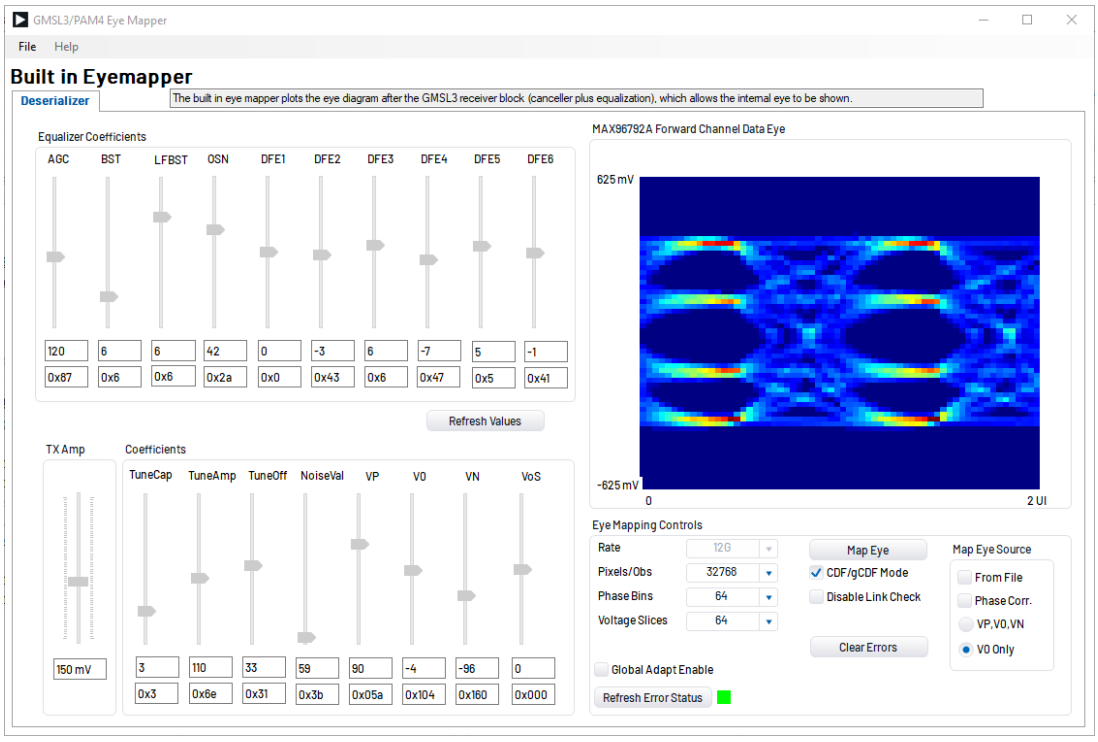



***Figure 56. MAX96793-MAX96792A 12Gbps Eye Mapper; (1M Coax, XTAL with PoC)***

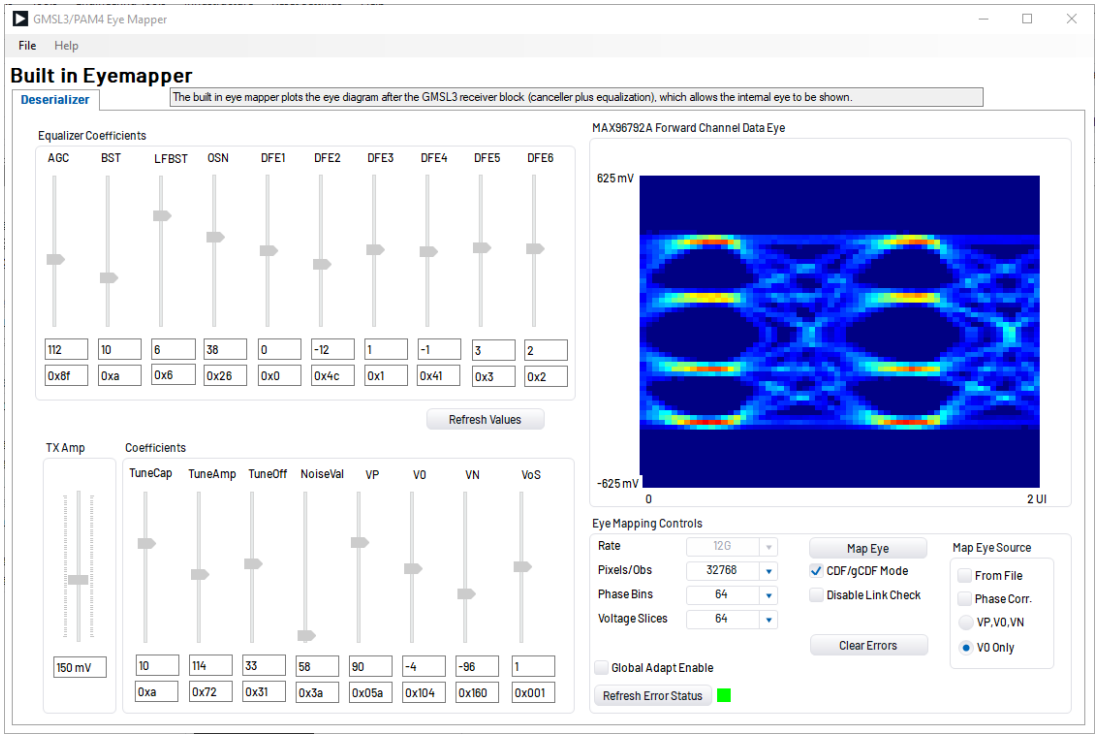



***Figure 57. MAX96793-MAX96792A 12Gbps Eye Mapper; (13.5M Coax, XTAL with PoC)***

## Forward-Error Correction Statistics

The FEC is available on some Analog Devices serializers and deserializers. The GMSL3 GUI reports the FEC status which includes the following:

- Number of blocks processed
- Number of bits corrected
- Number of blocks uncorrected
- Decode errors
- Idle errors
- FEC input BER
- FEC input BER @ 95% confidence level
- FEC output BER

FEC output BER of zero is required for error-free data transmission. The reported FEC input BER confidence level improves with longer observation times.

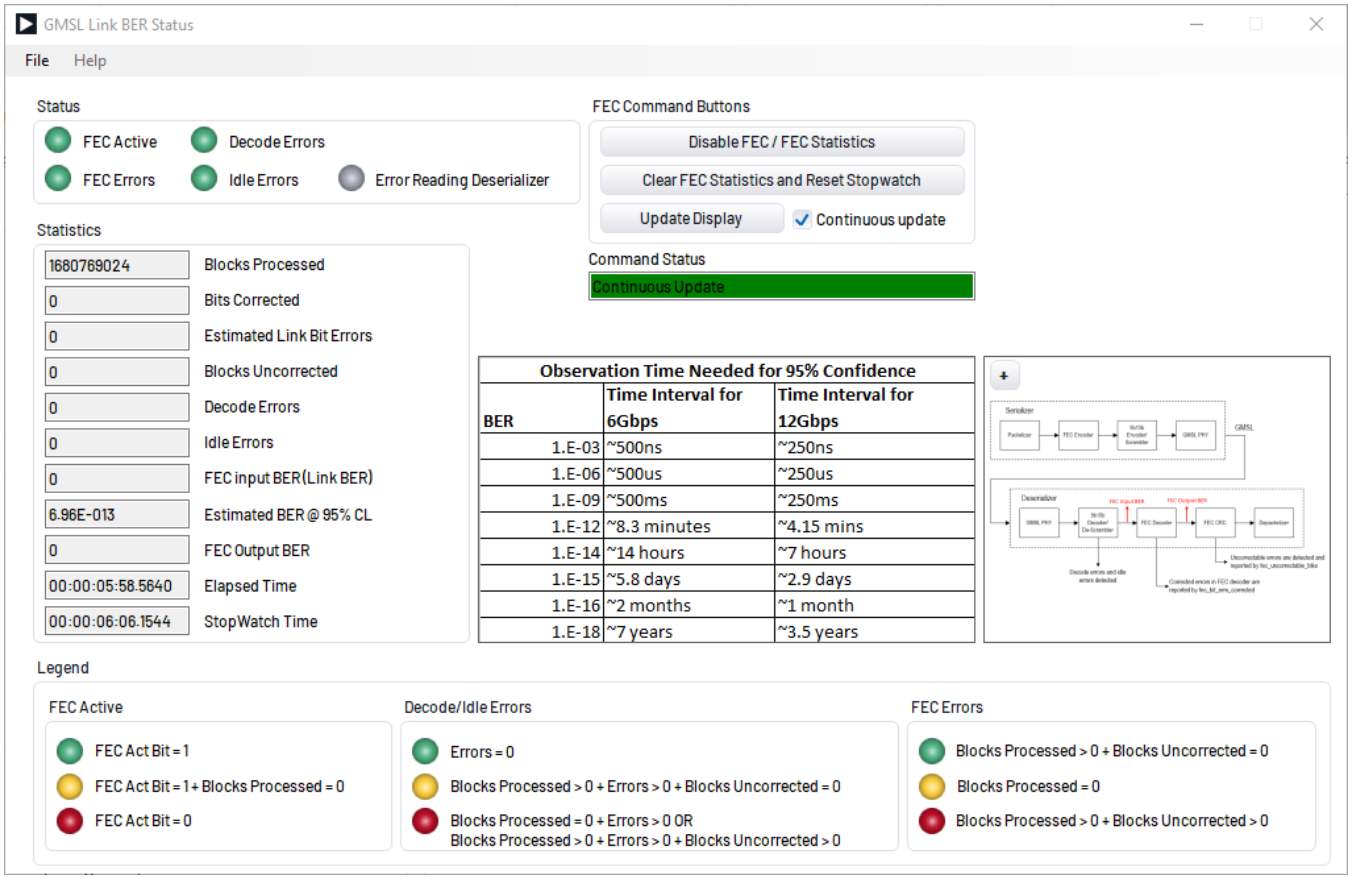



***Figure 58. GMSL3 FEC Status 12Gbps/187Mbps 13.5m Typical; XTAL w/ PoC (MAX96793/MAX96792A)***

## TDR Measurements

While the return loss looks at the impedance matching in the frequency domain, the time-domain-reflectometer (TDR) can evaluate the impedance matching in the time-domain. The TDR is a useful tool to evaluate impedance matching and determine the location of board layout issues.

- TDR: sends out a reflected pulse to measure matching and faults in transmission line
- Y-axis: impedance, x-axis: time (and thus position)
- Pulse rise time determines the frequency (and thus resolution)
- Rule of thumb: $Bandwidth = \frac{0.35}{Rise\ time}$

PCB parasitic inductance increases the magnitude of the impedance while parasitic capacitance lowers the magnitude of the impedance. Using a simulator (such as HFSS), the PCB parasitics can be estimated and layout can be optimized. For example, for the PCB stackup used on Analog Devices EV Kits, a 1.35x GND cutout is used underneath all component pads on the high-speed trace to offset the capacitance added by the component pads. The size of the cutout needed (or the number of layers to cut out) varies with different board stackups and materials.

For GMSL3, Analog Devices' TDR recommends ±5% impedance matching (between 47.5Ω and 52.5Ω single-ended or 95Ω and 105Ω differential) with a 100ps rise time (10%-90%) setting on the TDR.

A faster rise-time setting (between 20ps and 50ps) may also be useful to precisely isolate the location of impedance discontinuities. Slower rise times are less useful as they can mask potential discontinuities that negatively affect channel performance.

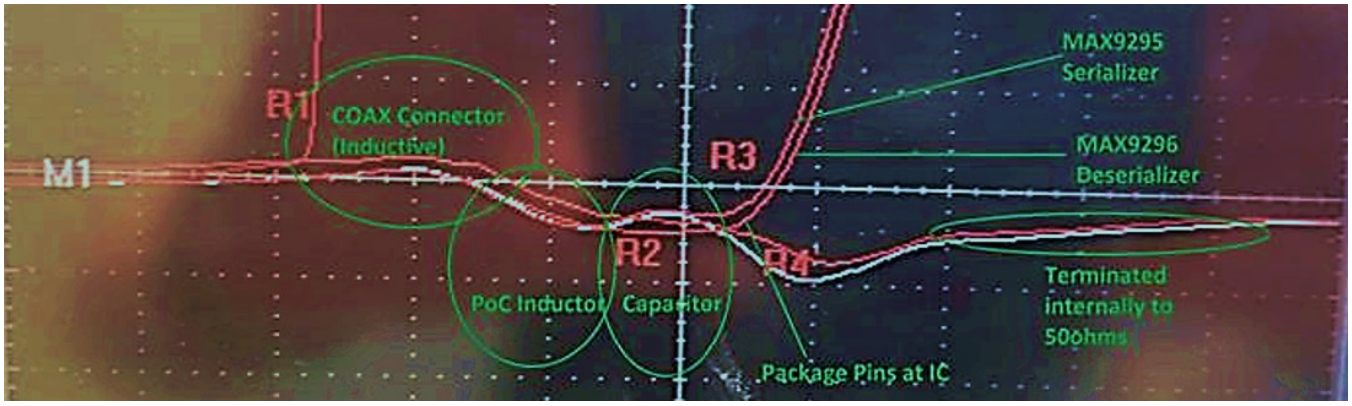



***Figure 59. Example TDR of a PCB that Pass GMSL3 Channel Spec. This is a single-ended measurement (coax system) with rise time = 100ps, x-axis scale = 200ps/div, y-axis scale = 5 ohms/div centered around 50 ohms***

# Hardware Channel Measurements

## Purpose and Scope

The *GMSL3 Channel Measurement Guide* shows example methods to measure the S-parameters and crosstalk of a GMSL3 system to compare against the GMSL3 Channel Specification.

## GMSL3 System Channel Specification Measurements

### Recommended Boards for Channel Measurements

Measurements should be taken with a real system at worst-case conditions to verify that designs are built to GMSL3 specification. There are two preferred methods Analog Devices recommends testing against the GMSL3 Channel Specification.

The first method copies the application PCB (*Figure 60*) and replaces GMSL3 ICs with high-quality SMA connectors (*Figure 61*). This ensures that any losses or discontinuities due to layout or components are preserved.

Second method involves the use of a coupon board (*Figure 62*) to model the GMSL3 channel. Keep the following parameters the same as the production PCB when making a coupon board:

- Passive components (including connectors, filters, capacitors)
- Electrical length between components (including vias)
- Board stackup

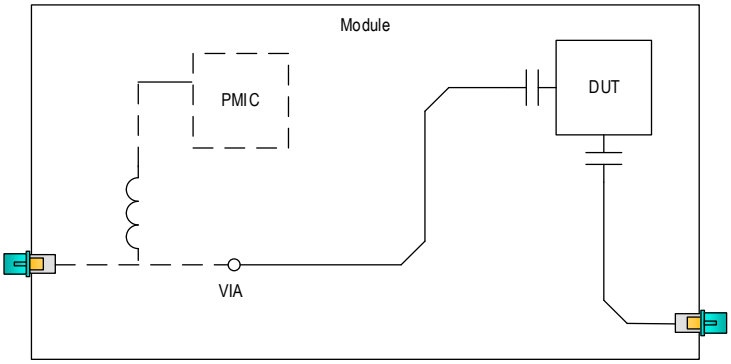



***Figure 60. GMSL3 Production PCB Design***

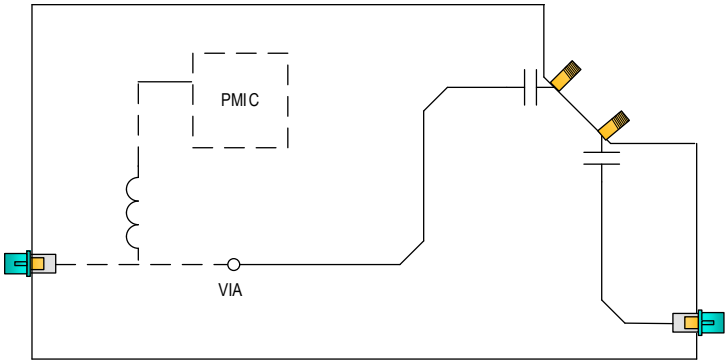



***Figure 61. GMSL3 S-Parameter Measurement Board (Nonproduction)***

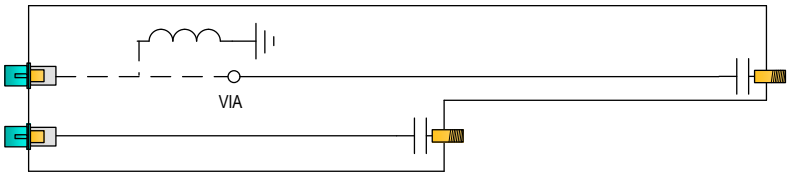



***Figure 62. Example of GMSL3 Coupon Board***

## GMSL3 Pin-to-Pin Channel Measurements

The forward channel is defined as serializer-to-deserializer transmission; the reverse channel is defined as deserializer-to-serializer transmission.

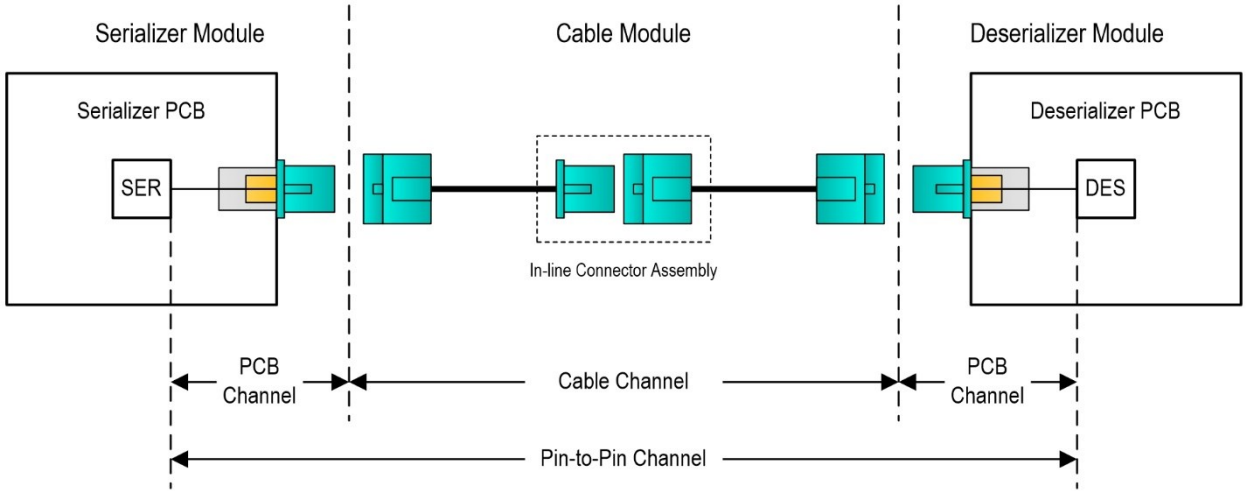



***Figure 63. GMSL3 Channel Definition***

**Note**: AC-coupling capacitors and optional PoC or line-fault components are not depicted in *Figure 63*.

**Note**: The PCB and cable channels comprising a compliant GMSL system channel may not meet the standards required for GMSL module compliance. Modules must be independently evaluated for module compliance. See the *GMSL3 Module Channel Specifications* section for additional information.

**Measurements for Insertion Loss and Return Loss**

Full 2-port S-parameters should be taken from the serializer SIO_ pin to the deserializer SIO_ pin. Start with a replica system consisting of the cable and two replica boards. Connect both ends to a vector network analyzer/VNA. Coax systems should use a 2-port VNA, while STP applications should use a 4-port VNA. For insertion loss, select $S_{21}/S_{DD21}$ and/or $S_{12}/S_{DD12}$ depending on the direction being measured. For return loss, select $S_{11}/S_{DD11}$ and/or $S_{22}/S_{DD22}$ depending on the port being measured.

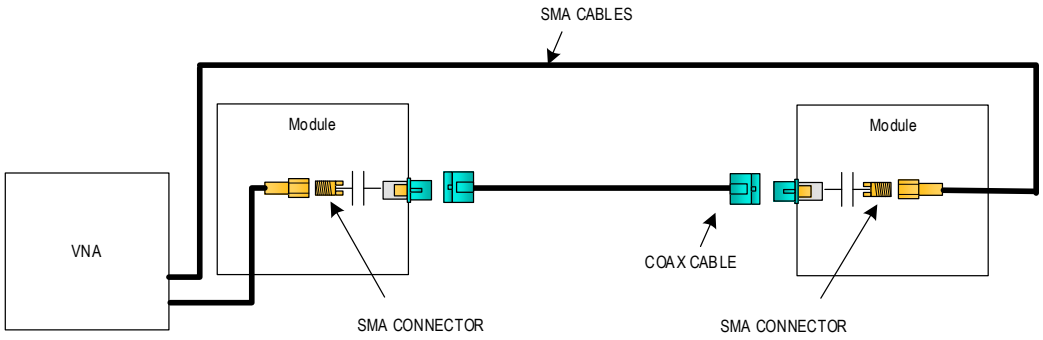



***Figure 64. Coax 2-Port VNA Connection***

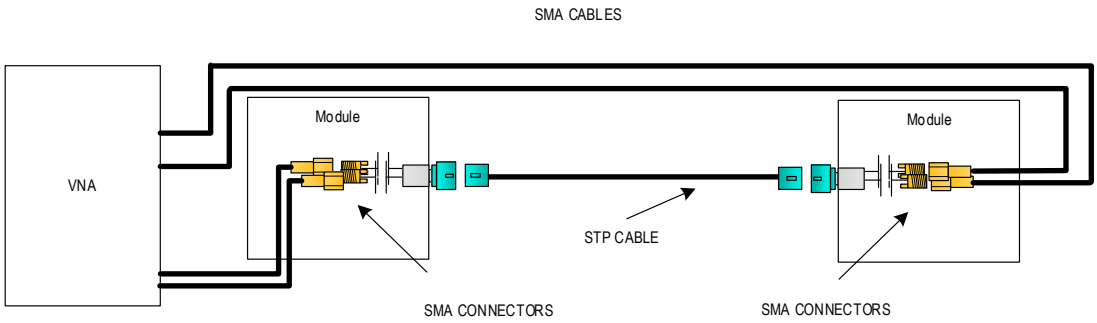



***Figure 65. STP 4-Port VNA Connection***

Set up the VNA with the following parameters:

- Start Frequency: 2MHz or lower
- Stop Frequency: 3.5GHz or higher
- Step size: 1MHz
- Sweep: Linear sweep
- Power Level: 0dBm

**Note**: STP cables for differential measurements must be phased matched.

**GMSL3 Crosstalk at Device Under Test**
Crosstalk is specified at a module level. See the following module measurement guidelines.

## GMSL3 Module Channel Specifications

The GMSL3 Module Channels are defined as the individual subchannels within the GMSL System Channel. See the *GMSL3 Module Channel Specifications* section for additional information.

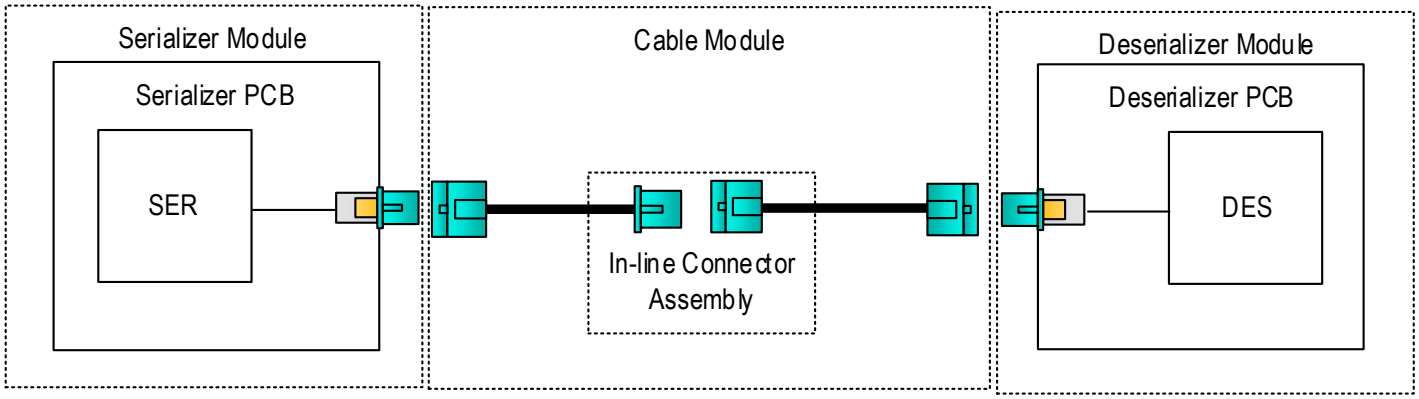



***Figure 66. GMSL3 Module Channels***

**Measurements for Insertion and Return Loss (PCB Channel)**

Using a replica/coupon board, connect the vector network analyzer to the SMA connector, and the GMSL module connector through an adapter (contact the connector manufacturer regarding adapters). Be sure to calibrate out losses of the SMA cables and adapters.

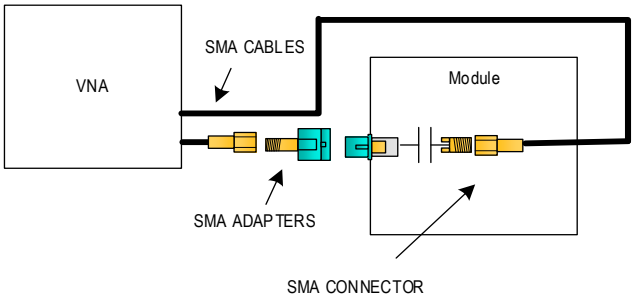



***Figure 67. Coax VNA Connection***

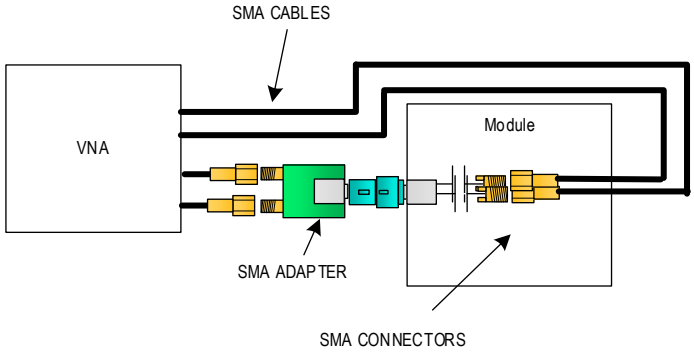



***Figure 68. STP VNA Connection***

Set up the VNA with the following parameters:

- Start Frequency: 2MHz or lower
- Stop Frequency: 3.5GHz or higher
- Step size: 1MHz
- Sweep: Linear sweep
- Power Level: 0dBm

**Measurements for Insertion and Return Loss (Cable Channel)**
Connect the VNA to both ends of the cable with adapters (if necessary).

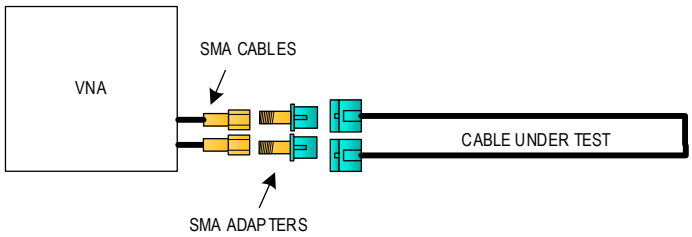



***Figure 69. Coax VNA Connection***

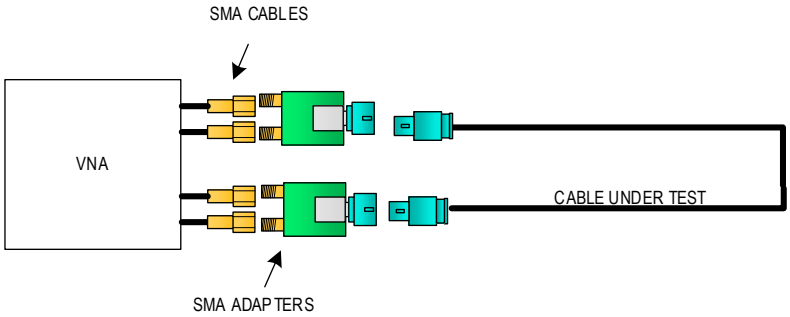



***Figure 70. STP VNA Connection***

Set up the VNA with the following parameters:

- Start Frequency: 100kHz or lower
- Stop Frequency: 3.5GHz or higher
- Step size: 1MHz
- Sweep: Linear sweep
- Power Level: 0dBm

**Measurements for Crosstalk (PCB Channel)**

**Crosstalk from GMSL or Other Broadband Signals**
The setup shown in *Figure 71* and *Figure 72* is used to measure crosstalk between the different ports (connectors) on a PCB. The data traffic causing interference is running on ports 1..N, and crosstalk is measured on Port M of the PCB.

The worst-case crosstalk condition occurs with channels (ports 1..N) with minimum insertion loss. This maximizes the received signal power on port M. Crosstalk is measured as peak amplitude on Port M using an oscilloscope. The GMSL device on Port M should be in Squelch mode. Scopes with enough bandwidth (4GHz min) generally have a low enough noise floor to not require additional gain stages. If a gain stage is needed, use a broadband, AC-coupled gain block to increase the noise signal to a measurable level. Gain should be high enough that the noise level falls within an acceptable input level for the scope.

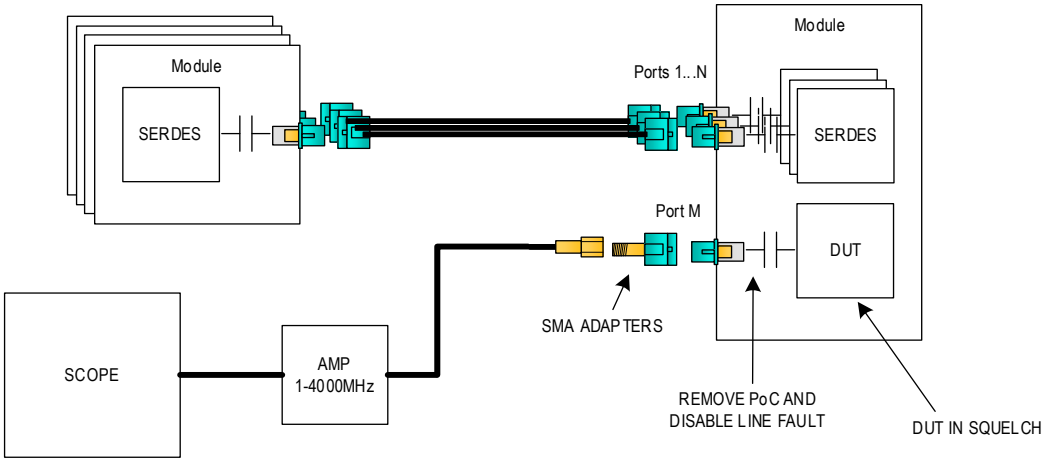



***Figure 71. Broadband Crosstalk Characterization Method (Coax)***

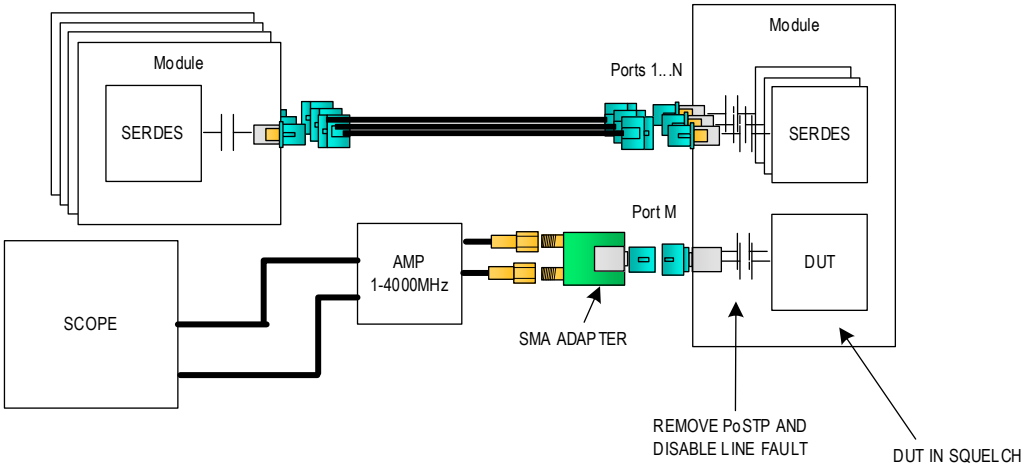



***Figure 72. Broadband Crosstalk Characterization Method (STP)***

**Note**: Removal of PoC, PoSTP, and Line Fault may be required if equipment requires 0V DC inputs.

### Crosstalk from Narrowband Signals

Connect the system as shown in *Figure 73* or *Figure 74*. The device under test is in Squelch mode. All other links 1..N are operating normally. A spectrum analyzer separates out noise sources so the user can measure the narrowband power of a single noise source. Measure the total power of the noise source (not just dBm level of the peak). Use a

balun if measuring a twisted pair system to match the DUT with the analyzer input. Make sure to account for the Balun's insertion loss. Alternatively, the noise level can be measured with an oscilloscope. In contrast to the broadband crosstalk measurement, a band-pass filter and a low-noise amplifier is used to measure narrowband signals individually. The gain needs to be large enough that the noise can be measured by the scope. The filters need to be selective enough to isolate frequencies. These vary depending on the system, but in general, lab grade devices should suffice.

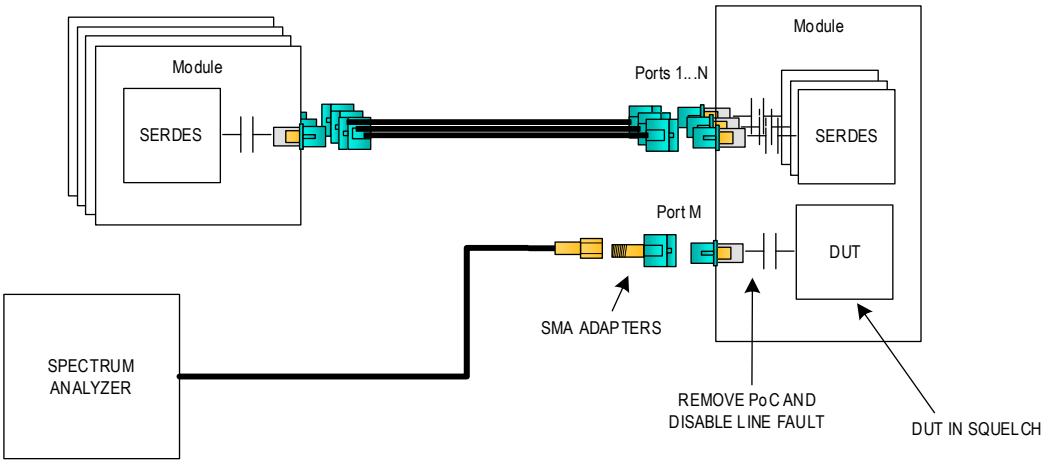



***Figure 73. Measurement Setup for Narrowband Crosstalk (Coax) using a Spectrum Analyzer***

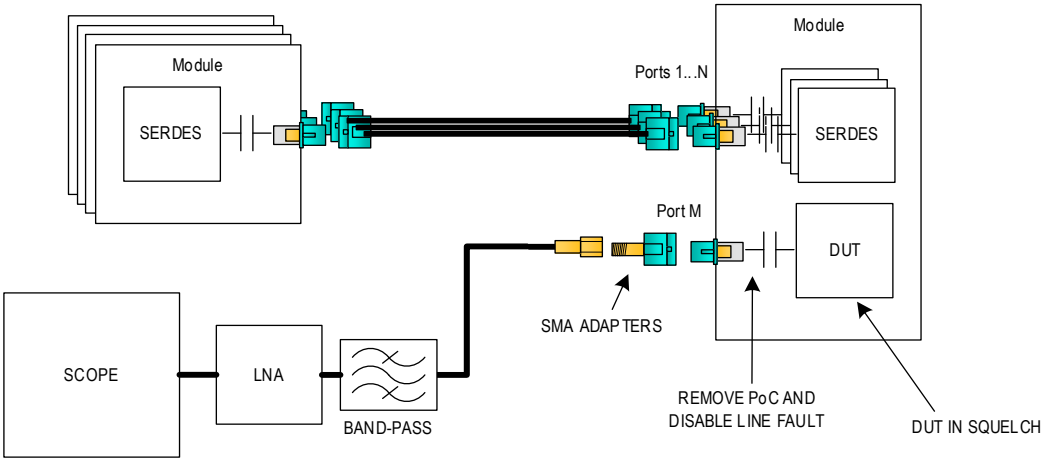



***Figure 74. Measurement Setup for Narrowband Crosstalk (Coax) using a Scope***

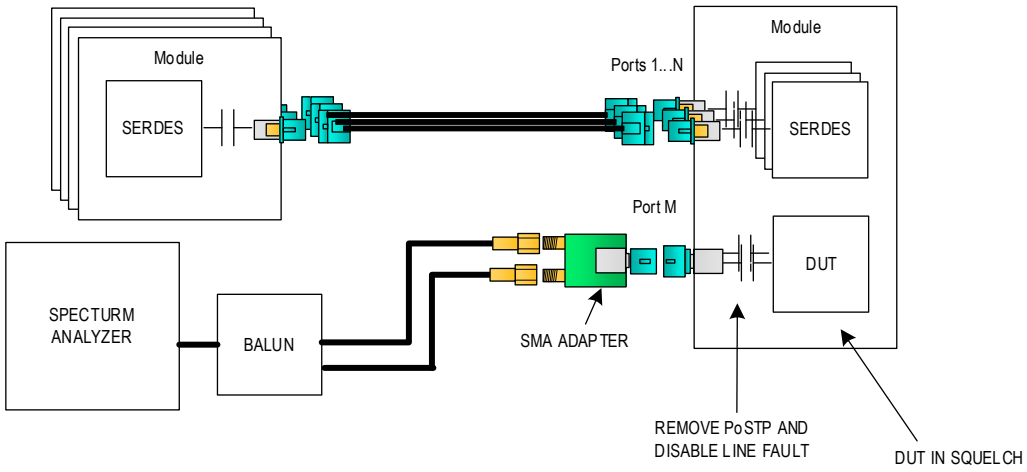



***Figure 75. Measurement Setup for Narrowband Crosstalk (STP) using a Spectrum Analyzer***

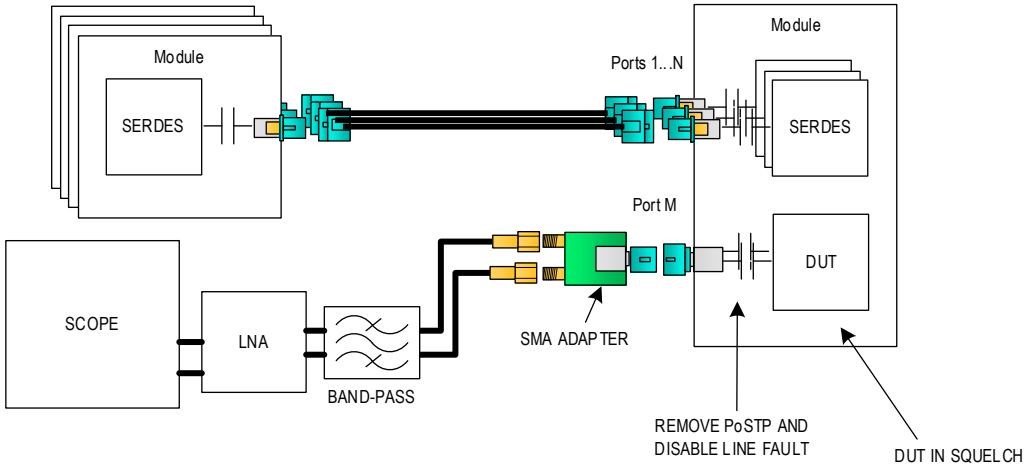



***Figure 76. Measurement Setup for Narrowband Crosstalk (STP) using a Scope***

**Note**: Removal of PoC, PoSTP, and line fault may be required if equipment requires 0V DC inputs.

### Measurements for Crosstalk (Cable Bundles)

### Far-End Cable Bundle Crosstalk

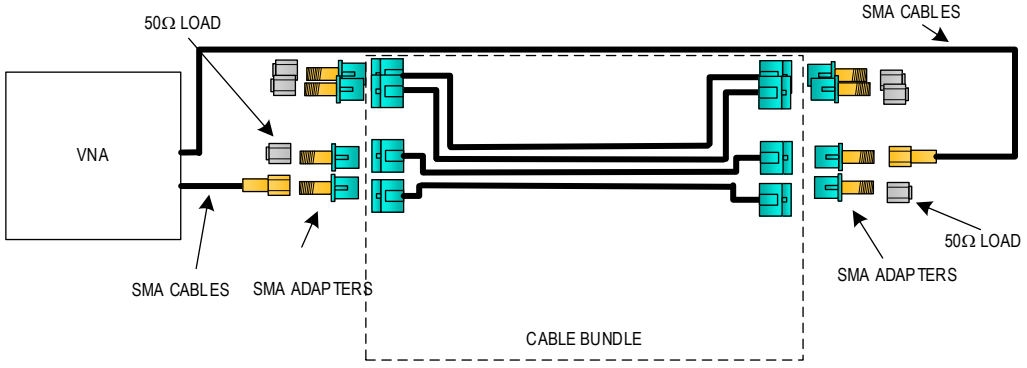


*Figure 77. Far-End Crosstalk (FEXT) Coax*

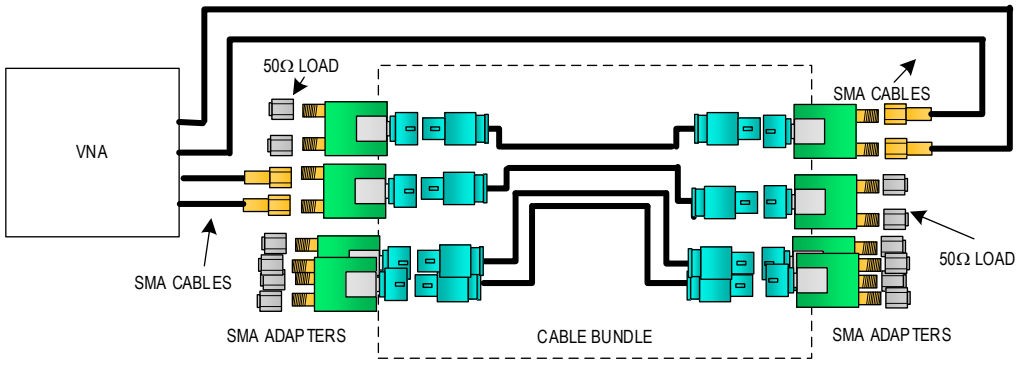



*Figure 78. Far-End Crosstalk (FEXT) STP*

Far-end crosstalk/FEXT is a measure of the crosstalk received at the far end of the cable with the disturbance applied at the near-end of the cable (*Figure 87*).

**Note**: During measurement, all unused ports must be terminated in 50Ω for coax or 100Ω for STP.

### Near-End Cable Bundle Crosstalk

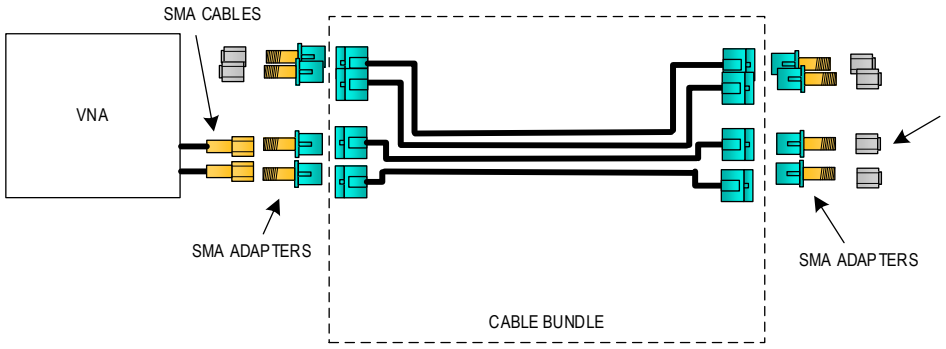



*Figure 79. Near-End Crosstalk (NEXT) Coax*

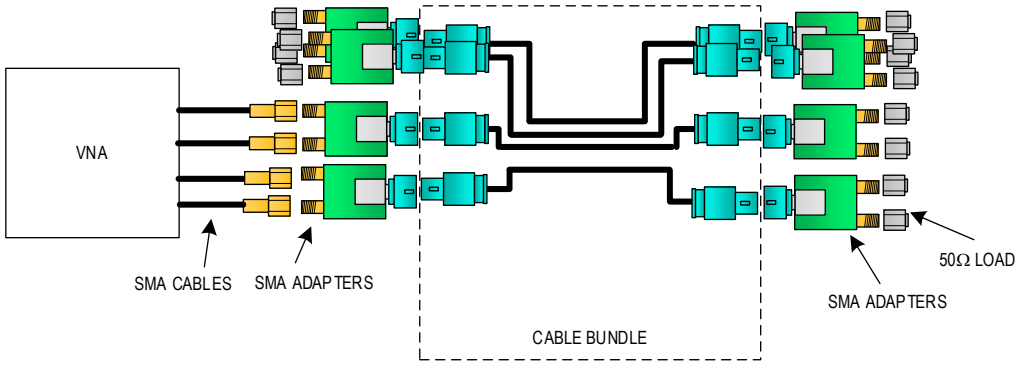



*Figure 80. Near-End Crosstalk (NEXT) STP*

The near-end crosstalk/NEXT is usually dominant. NEXT is based on the injection and measurement ports shown in *Figure 79* and *Figure 80*.

The NEXT measurement is performed as a sequence of multiport S-parameter measurements using a vector network analyzer/VNA. The transfer functions from injection port to measurement port are added in the power domain.

**Note**: During measurement, all unused ports must be terminated in 50Ω for coax or 100Ω for STP.

**Squelch Mode**

Many measurements taken on PCB modules (TDR, S-parameters, noise measurements) are taken with the GMSL3 device in system. To ensure proper termination of the output transmitter without sending data, the device needs to be placed in Squelch mode. Set the following parameters before making measurements. Note that if both ends of the link are connected (e.g., serializer module connected to deserializer module), both ends need to be put into Squelch mode by their respective local uCs.

**Table 12. GMSL3 Squelch Mode Register Settings**

| Step # | Command | Register/Setting | Notes |
|---|---|---|---|
| 1 | Set the GMSL3 bit rate. | Refer to data sheet for register settings. | Step is only needed if default bitrate is not being set by CFG pins. |
| 2 | Turn on the GMSL3 correct link. | Refer to data sheet for register settings. | Manually turn on the desired link. |
| 3 | Set the correct GMSL3 transmitter to Squelch mode. | RLMSA8=0xE0<br>RLMSA9=0xA8 | Registers 0xXXA8 and 0xXXA9 in the relevant block per GMSL3 link. Each GMSL3 link has its own register set. |

# Appendix

## Appendix A: Legacy Recommendations

The following sections are for legacy approved Analog Devices system components. Each section provides more detail.

### Legacy Recommended ESD TVS Didoes

*Table 13* lists legacy recommended ESD TVS diodes. Part numbers, passing levels, and notes are included.

Due to ESD TVS diode vendors continuously releasing new TVS diodes and Analog Devices not testing out solutions on hardware, Analog Devices no longer recommends specific TVS diode part numbers. Legacy-recommended ESD TVS diodes are still valid for GMSL3 systems as long as they pass the GMSL3 Channel Specification.

For new designs, Analog Devices recommends reviewing *TVS Diode Characteristics* section and/or contacting TVS diode vendors directly for the best solution available.

**Table 13. Legacy-Recommended External TVS Diodes**

| MFG | Part Number | Automotive Qualified? | ESD Passing Level Contact/Air | Tested by Analog Devices? | Note |
|---|---|---|---|---|---|
| **Littelfuse** | SESD0201X1UN | Yes | >8kV/15kV | Yes | 0201 package, 2-pin device |
| **Littelfuse** | SESD0402X1UN | Yes | >8kV/15kV | Yes | 0402, larger package than above |
| **ON Semi** | ESD7004MUTAG | No | >8kV/15kV | Yes | 10-pin device |
| **ON Semi** | SZESD7004MUTAG | Yes | -- | No | Automotive-qualified version of above, results should be similar |
| **ON Semi** | SZESD9101P2T5G | Yes | >8kV/15kV | Yes | 2-pin device |

**Note(s)**

- Analog Devices does not guarantee passing levels for these devices.
- Recommendations based on ideal characteristics stated in *TVS Diode Characteristics* section.

# Appendix B: Crystal Calculations

## Calculate Oscillator Negative Resistance

Calculate the circuit's negative resistance. Generally, to allow sufficient margin to component variation, it is desirable that negative resistance magnitude is greater than ~5x ESR.

Calculate the oscillator's negative resistance as follows:

$$R_{OSC}(\Omega) = -\frac{g_M \times C_1 \times C_2}{\omega^2 \times (C_1 \times C_2 + C_1 \times C_{SHUNT} + C_2 \times C_{SHUNT})^2 + (g_M \times C_{SHUNT})^2}$$

where:

$$C_1, C_2 = Total\ load\ capacitance\ at\ X1, X2\ in\ Farad\ (Calculated)$$

$$g_M = Crystal\ Oscillator\ Transconductance\ in\ A/V\ (GMSL\ Datasheet)$$

$$C_{SHUNT} = Crystal\ Shunt\ Capacitance\ in\ Farad\ (Crystal\ Datasheet)$$

$$\omega = angular\ frequency\ = 2\pi * 25{,}000{,}000\ Hz$$

As an example, with $C_1, C_2 = 20pF, g_M = 28mA/V, C_{SHUNT} = 7pF$

$$R_{OSC}(\Omega) = -\frac{28E-3 \times 20E-12 \times 20E-12}{(2\pi * 25E6)^2 \times (20E-12 \times 20E-12 + 20E-12 \times 7E-12 + 20E-12 \times 7E-12)^2 + (28E-3 \times 7E-12)^2}$$

$$R_{OSC}(\Omega) = -225\Omega$$

$|R_{OSC}|$ should be greater than 5x ESER. Thus, ESR should be 45Ω or less.

### Calculate Crystal Drive Level

Next, calculate the power dissipated in the crystal (crystal drive level) to check if it is within the limits of the crystal data sheet.

- Power dissipated by the crystal is: $P_{DRIVE} = \left(I_{DRIVE(RMS)}\right)^2 \times ESR$. This can be found by measuring the crystal current through a current probe.
- If a current measurement cannot be done, the crystal current can be calculated ≈ current through C1 (current through pin X1 is negligible).

  Current through C1 is: $I_{DRIVE(RMS)} = I_{C1(RMS)} = |\frac{V_{C1(RMS)}}{Z_{C1}}| = V_{C1(RMS)} \times 2\pi f \times C_1$
- Power dissipated by the crystal is now: $P_{DRIVE} = \left(V_{C1(RMS)} \times 2\pi f \times C_1\right)^2 \times ESR$

If $V_{C1}$ is a sine wave, then $P_{DRIVE} = \frac{1}{2}\left(V_{C1(P-P)} \times 2\pi f \times C_1\right)^2 \times ESR$

For example, a measured 600mVpp sine wave at 25MHz and ESR = 40Ω and C1 = 20pF:

$$P_{DRIVE} = \frac{1}{2}(0.6 \times 2\pi * 25E6 \times 20E-12)^2 \times 40 = 71\mu W$$

## Appendix C: Single-Ended and Differential S-Parameters

S-parameters (scattering parameters or scattering matrix) are used to characterize the Analog Devices GMSL Channel Specification requirement. S-parameters are used to quantify how RF energy propagates through a multiport network. For Coax mode, which uses single-ended signaling, the channel is characterized as a two-port, single-ended network (*Figure 89*). These networks have one input port and one output port. Signals on the input and output ports are referenced to ground. Measurements should be made using a vector network analyzer.

**Note**: The GMSL3 Channel Specifications apply to the componentry and cabling from the pin(s) of the transmitter to the pin(s) of the receiver.

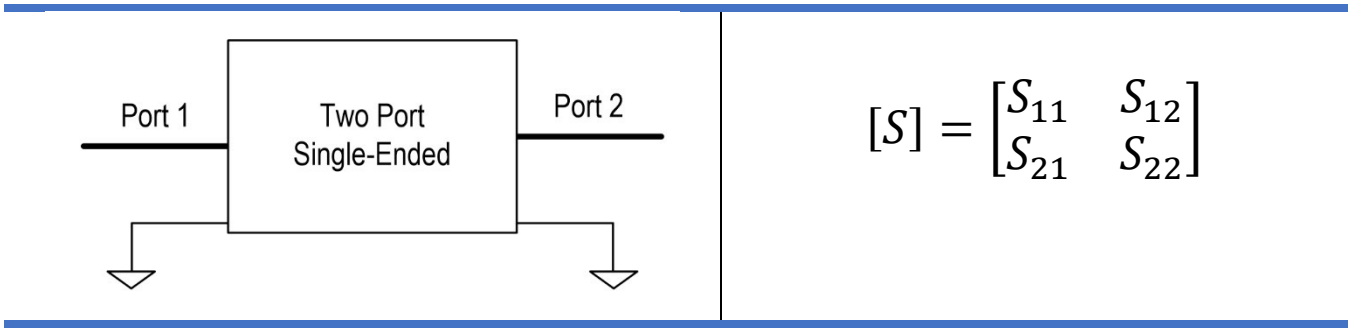
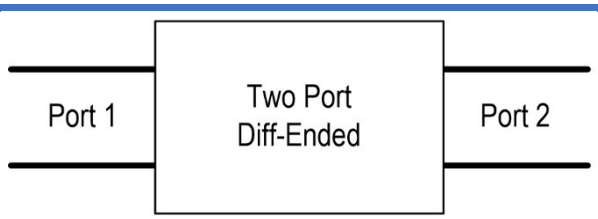


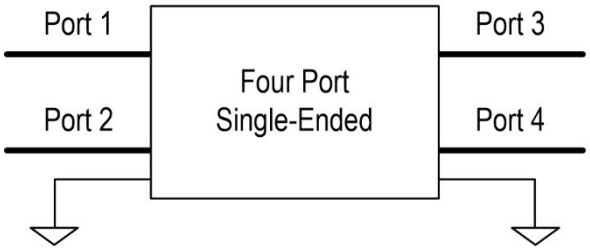

***Figure 81. Two-Port, Single-Ended Network***

STP mode requires the use of differential S-parameters (Sdd) to evaluate the network. In real-world application, balanced measurements may not be possible (or preferred). Instead, the two-port, differential network (*Figure 82*) can be considered along with a four-port, single-ended network (*Figure 83*).




$$[S_{dd}] = \begin{bmatrix} S_{dd11} & S_{dd12} \\ S_{dd21} & S_{dd22} \end{bmatrix}$$

***Figure 82. Two-Port, Differential-Ended Network***




$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix}$$

***Figure 83. Four-Port, Single-Ended Network***

Mixed-mode S-parameters can be extracted from S4P files (or four-port, single-ended S-matrix) with the standard formula or professional tools.

## Revision History

| Revision Number | Revision Date | Change(s) |
|---|---|---|
| 0 | 7/24 | Initial release |
| 1 | 1/25 | Wording changes to and refinement of *Shielding and Grounding Recommendations for ESD and EMI Protection* section |
| 2 | 8/25 | Updated Table 5 with additional PoC solutions. |