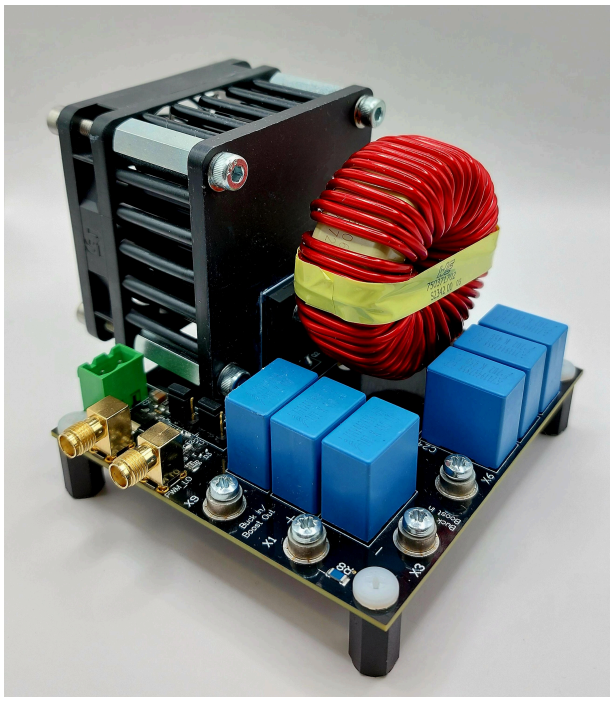
UM90045

Rev. 2.0 — 10 February 2025

User manual

NX-HB-GAN111UL 2.0 kW half-bridge evaluation board user guide



Abstract: The NX-HB-GAN111UL evaluation board is a half-bridge converter circuit using Nexperia GAN111-650WSB power GaN FETs.

Keywords: GaN FET, half-bridge, converter, evaluation board, NX-HB-GAN111UL, GAN111-650WSB

nexperia

1. EVALUATION BOARD TERMS OF USE

The use of the Evaluation Board is subject to the Evaluation Board Terms of Use, which you can find here. By using this Evaluation Board, you accept these terms.

2. High Voltage Safety Precautions

Read all safety precautions before use!

Please note that this document covers only the NX-HB-GAN111UL 2.0 kW half-bridge evaluation board and its functions. For additional information, please refer to the Product Specification

To ensure safe operation, please carefully read all precautions before handling the evaluation board. Depending on the configuration of the board and voltages used, potentially lethal voltages may be generated. Therefore, please make sure to read and observe all safety precautions described below.

Before Use:

It is recommended that ALL operation and testing of the evaluation board is performed with the board enclosed within a non-conductive enclosure that prevents the High Voltage supply to be switched whilst open and accessible; see Fig. 1.

Fig. 1. Example of a safety enclosure in the Nexperia lab

All probes should be position before turning on the High Voltage and should be held in place using a suitable probe positioner e.g. PMK MSA100; see Fig. 2.

Fig. 2. Example of a probe positioner

Always use an oscilloscope with protective earth connected.

When probing High Voltage, ensure that the probes have the correct voltage rating / limit.

Ensure that all scope probes are compensated and de-skewed before use, refer to your oscilloscope or probe manual for instructions on how to do this.

If possible, have a visual indicator of High Voltage located close to the evaluation board (LED bar graph or voltmeter) To show when the Bus Voltage (Vbus) and Outputs are at dangerous levels.

Verify that none of the parts or components are damaged or missing.

Check that there are no conductive foreign objects on the board.

If any soldering or modifications are made or carried out, then please ensure that this is done carefully so that solder splashes and debris are not created. Clean the board with Iso-propyl-alcohol and allow it to dry.

Ensure that there is no condensation or moisture droplets on the circuit board, all testing should be carried out within a dry environment without excessive humidity.

If used under conditions beyond the rated voltage and current specification, this may cause defects, failure and or permanent damage.

NEVER handle the evaluation board during operation under ANY circumstances

After use the Nexperia Evaluation Board contains components which may store high voltage and will take time to discharge. Carefully probe the evaluation board once the power has been removed to check that all capacitors have been discharged. You must do this without touching the board except for the multimeter probes that are being used to check.

This evaluation board is intended for use only in High Voltage Lab environments and should be handled only by qualified personnel familiar with all safety and operating procedures. We recommend carrying out operation and testing in a safe environment that includes restricted access only to trained personnel, the use of High Voltage signage at all entrances, safety interlocks and emergency stops and HV insulated flooring.

It should be noted that this evaluation board is intended to be used ONLY for evaluation purposes and should not be used by consumers or designed into consumer equipment in its current form.

3. Introduction

The NX-HB-GAN111UL half-bridge evaluation board provides the elements of a simple buck or boost converter using GAN111-650WSB GaN FET. It enables the basic study of the switching characteristics and efficiency achievable with Nexperia's 650 V GaN FETs. The circuit can be configured for synchronous rectification, in either buck or boost mode. Selection jumpers allow the use of a single logic input or separate high / low level inputs. The high-voltage input and output can operate at up to 400 V DC, with a power output of up to 2.0 kW. The inductor provided is intended for efficient operation at 100 kHz, however, other inductors and frequencies may be used.

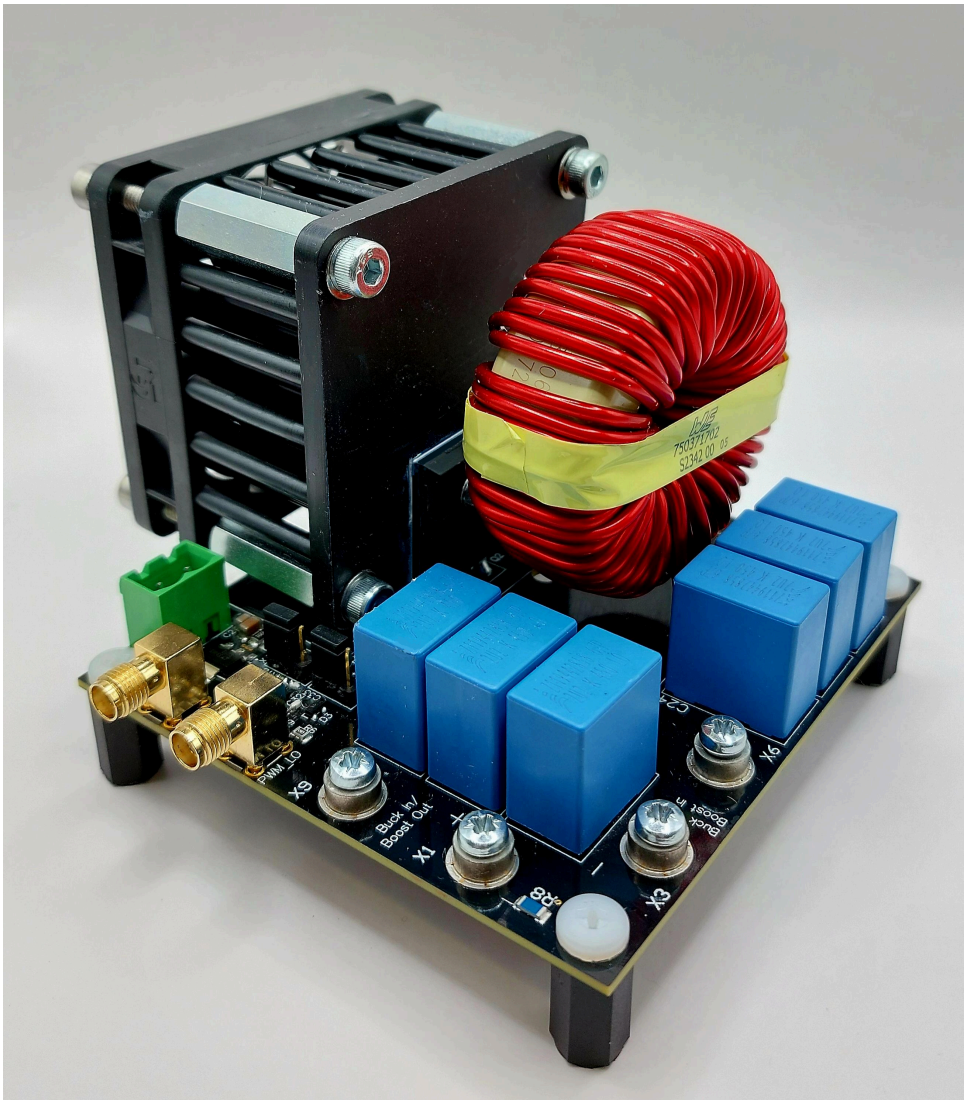


Fig. 3. NX-HB-GAN111UL half-bridge evaluation board

3.1. Quick reference information

Table 1. NX-HB-GAN111UL Input/Output specifications

Parameter	
High-voltage input/output	400 VDC max
Auxiliary supply (J1)	10 V min, 18 V max
Logic inputs	nominal 0-5 V

Parameter	
• for the pulse-generation circuit	V_{lo} < 1.5 V, V_{hi} > 3.0 V
• for direct connection to gate driver	V_{lo} < 0.8 V, V_{hi} > 2.0 V
SMA coaxial connectors	
Switching frequency	configuration dependent
• lower limit	determined by peak inductor current
• upper limit	determined by desired dead time and power dissipation

Power dissipation in the GaN FETs is limited by maximum junction temperature. Refer to the GAN111-650WSB data sheet.

4. Warnings

This demo board is intended to demonstrate GaN FET technology. While it provides the main features of a half-bridge converter, it is not intended to be a finished product and does not have all the protection features found in commercial power supplies.

There is no specific protection against over-current or over-voltage on this board.

If the on-board pulse generation circuit is used in boost mode, a zero input corresponds to 100% duty cycle for the active low-side switch.

5. Circuit description

The circuit comprises a simple half-bridge featuring two GAN111-650WSB GaN FETs, as indicated in the block diagram of Fig. 4. Two high-voltage ports are provided which can serve as either input or output, depending on the configuration: boost or buck. In either case one GaN FET acts as the active power switch while the other carries the freewheeling current. The latter device may be enhanced, as a synchronous rectifier, or not. With GaN FETs the reverse recovery charge is low and there is no need for additional freewheeling diodes. Two input connectors are provided which can be connected to sources of logic-level command signals for the hi/lo gate driver. Both inputs may be driven by off-board signal sources, or alternatively, a single signal source may be connected to an on-board pulse-generator circuit which generates the two non-overlapping pulses. Jumpers determine how the input signals are used.

An inductor is provided as a starting point for investigation. This is a 330 µH toroid intended to demonstrate a reasonable compromise between size and efficiency for power up to 2.0 kW at a switching frequency of 100 kHz.

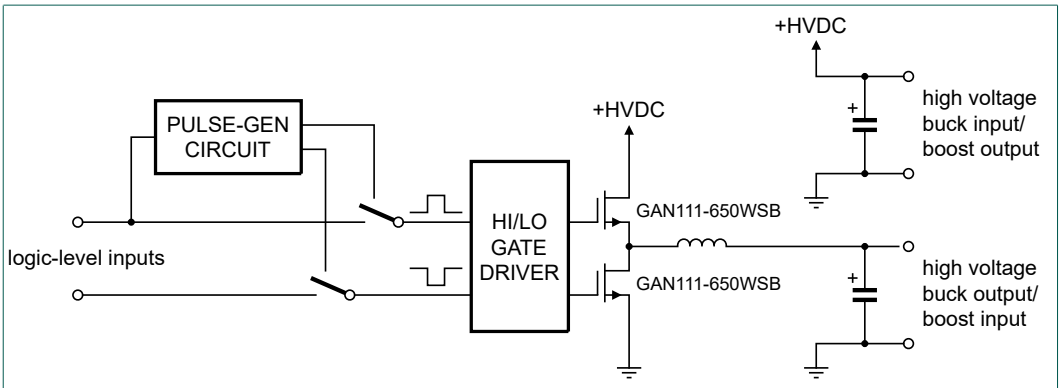
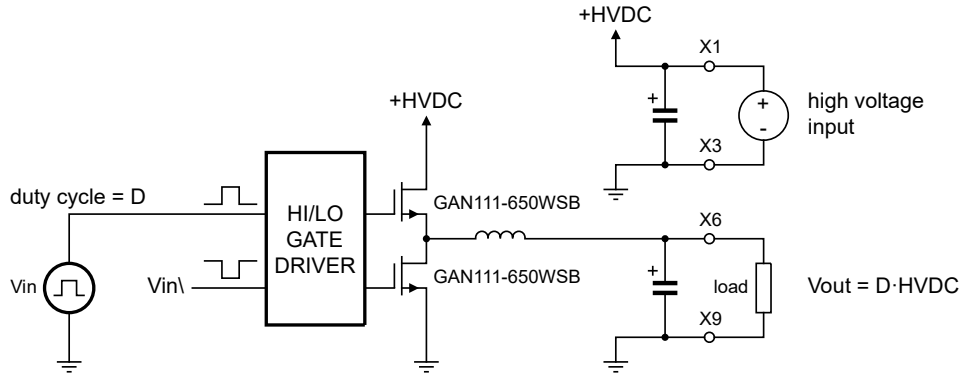


Fig. 4. Functional Block Diagram

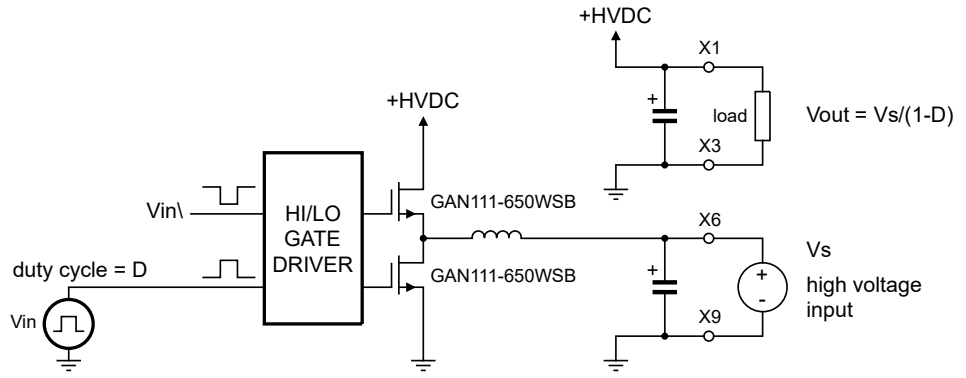
6. Configuration

Fig. 5 shows the basic power connections for buck and boost modes. For buck mode, the HVDC input (terminals X1, X3) is connected to the high-voltage supply and the output is taken from terminals X6 and X9. For boost mode the connections are reversed.

Note that in boost mode a load must be connected. The load current affects the output voltage up to the transition from DCM to CCM. In buck mode the load may be an open circuit. In the latter case – buck mode, no load – the ripple current in the inductor is symmetric about zero, and the soft switching behavior of the GaN FETs may be studied.



(a) Buck Mode; See regarding the complementary input



(b) Boost Mode; See regarding the complementary input

Fig. 5. Supply and load connections for Buck (a) and Boost (b) configurations

Fig. 6 shows possible configurations for the gate-drive signals. In Fig. 6 (a) a single input from an external signal source is used together with the on-board pulse generation circuit. X5 is used, (see Fig. 7), X8 is left open circuit. Jumpers X4 and X7 are in the top position, as shown in Fig. 7. If the high-side transistor is to be the active switch (e.g. buck mode), then the duty cycle of the input source should simply be set to the desired duty cycle (D). If the low-side transistor is to be the active switch (e.g. boost mode) the duty cycle of the input source should be set to (1-D), where D is the desired duty cycle of the low-side switch. This configuration results in synchronous rectification. If it is desired to let the device carrying the freewheeling current act as a diode, then the appropriate jumper should be placed so that the pull-down resistor is connected to the driver. Fig. 6 (b) shows a buck-mode configuration where the low-side device is not enhanced. Finally, Fig. 6 (c) shows use of two external signal sources as inputs to the gate driver. This can be done by linking pins 1 and 2 on the respective jumper X4 or X7.

For any configuration an auxiliary supply voltage of 10 V-18 V must be supplied at connector X2.

Pull-down resistors R5 and R6 have a value of 49.9 Ω. If a 50 Ω signal source is used and 50 Ω termination is desired, then R5 and R6 may be replaced (or paralleled) with 1206 size 50 Ω resistors.

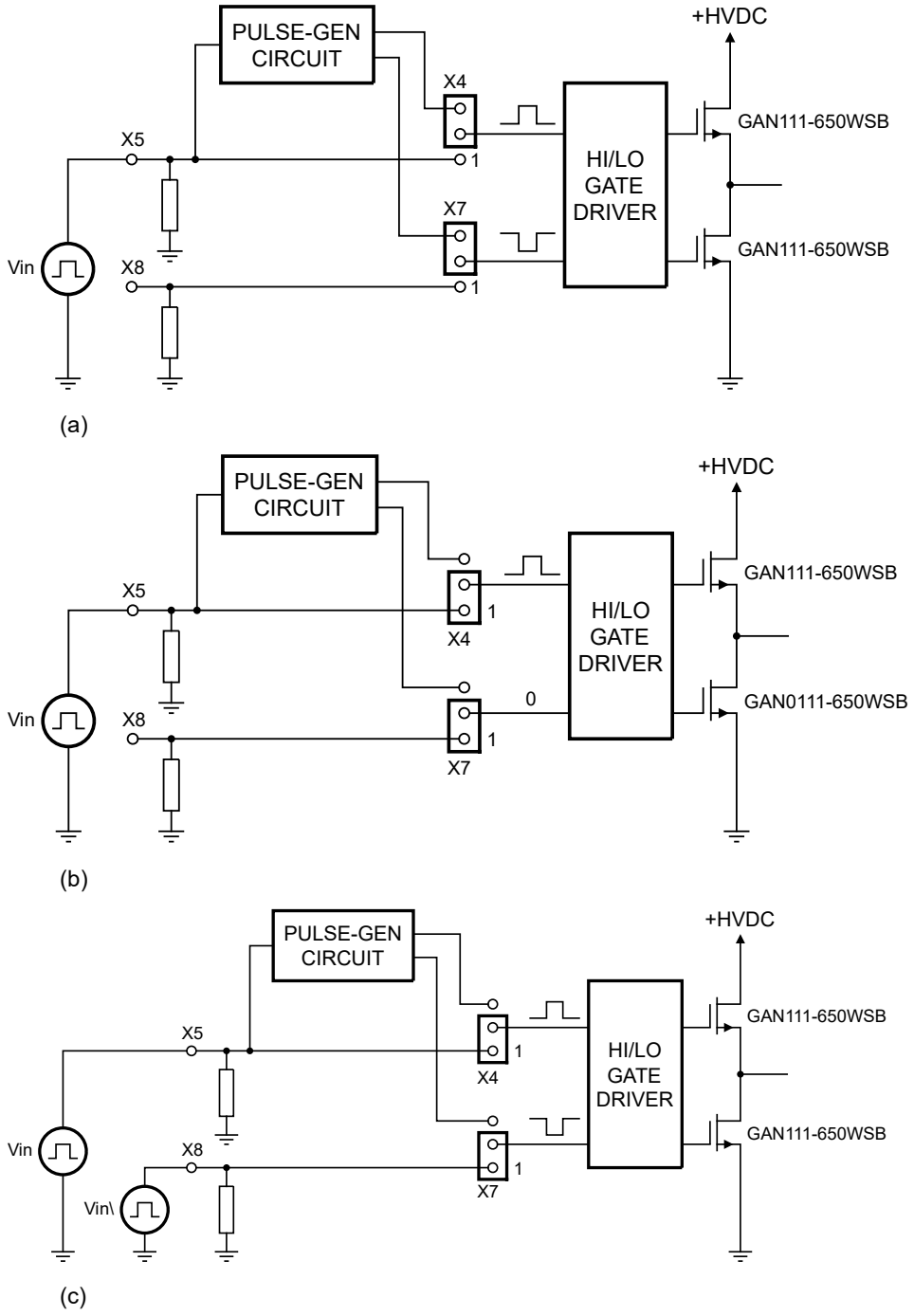


Fig. 6. Input configurations. (a) using a single source for either buck or boost mode (b) buck mode without synchronous rectification (c) using two signal sources

Caution: If the on-board pulse-generation circuit is used for boost mode, be aware that a steady state zero input (or disconnected signal source) will result in the low-side FET being turned on continuously. Ensure that high voltage is not applied to X1 until the input is switching. This configuration results in synchronous rectification. If it is desired to let the device carrying the freewheeling current act as a diode, then the appropriate jumper should be placed so that the pulldown resistor is connected to the driver. Fig. 6 (b) shows a buck-mode configuration where the low-side device is not enhanced. Finally, Fig. 6 (c) shows use of two external signal sources as inputs to the gate driver. This can be done by linking pins 1 and 2 on the respective jumper X4 or X7.

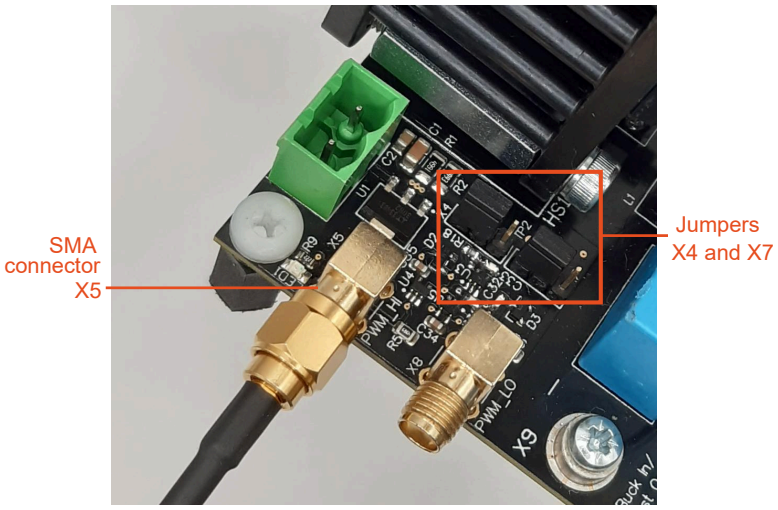


Fig. 7. SMA connector X5, jumpers X4 and X7 locations

7. Design details

For this evaluation board, the half-bridge converter circuit has been implemented on a 4-layer PCB and uses two Nexperia GAN111-650WSB GaN FETs

The circuit schematic, PCB layout and bill of materials for the NX-HB-GAN111UL evaluation board are shown in the next sections.

7.1. NX-HB-GAN111UL schematic

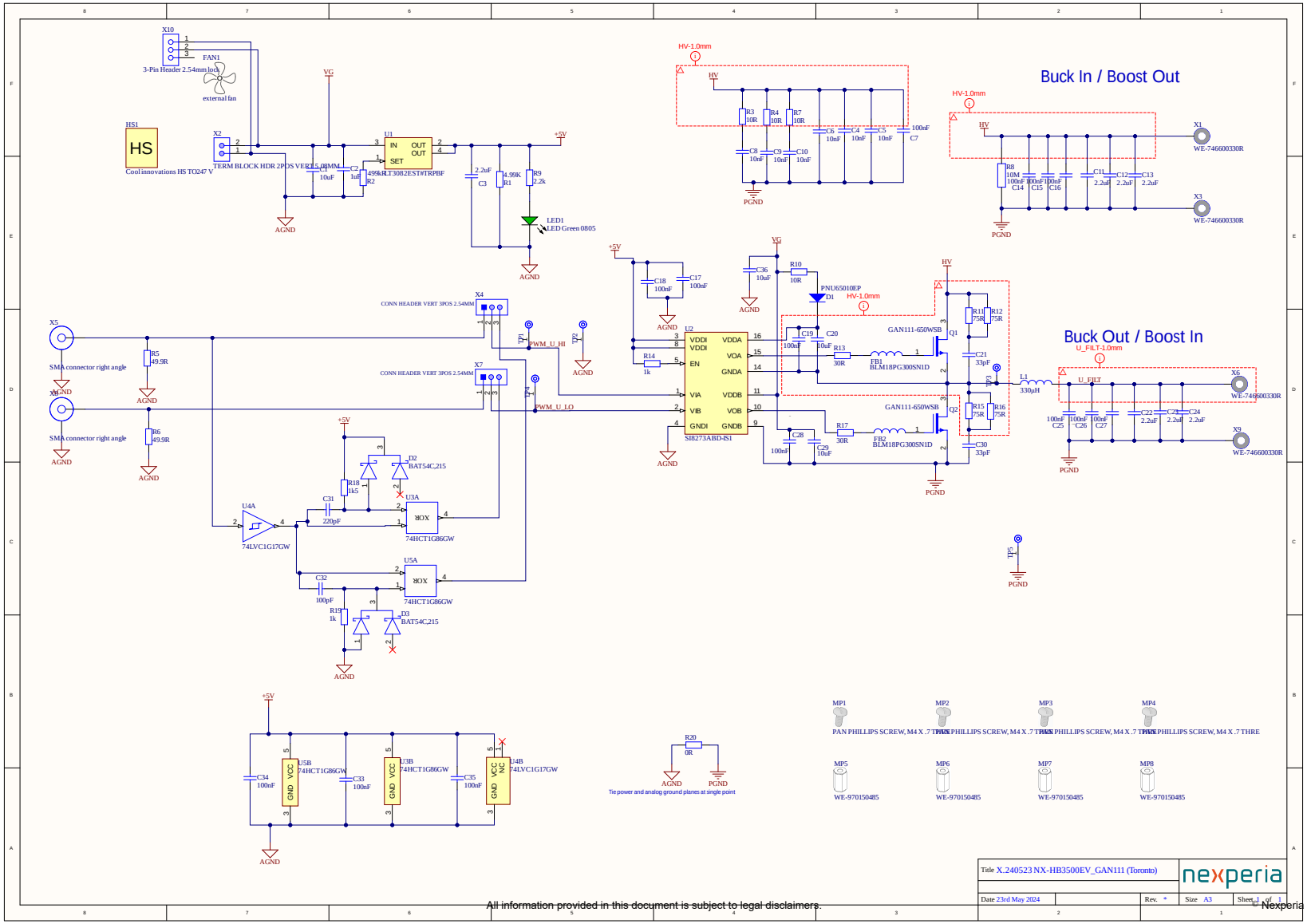


Fig. 8. Schematic

7.2. NX-HB-GAN111UL evaluation board PCB layout

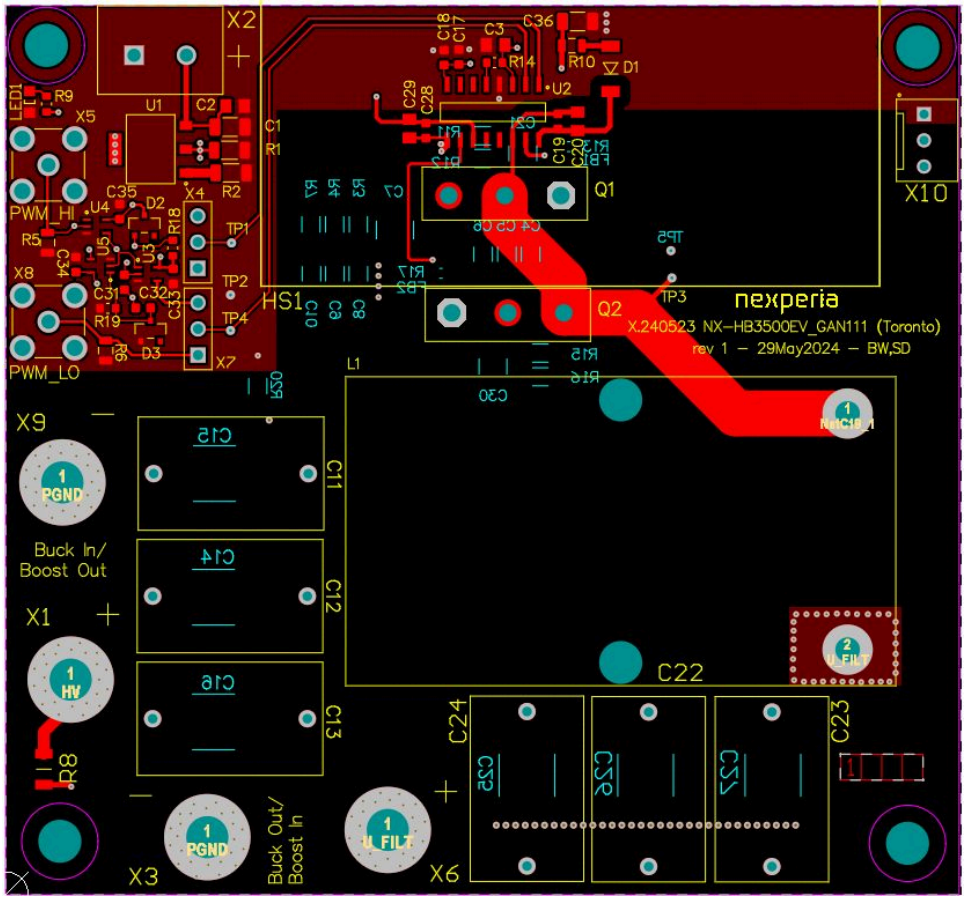


Fig. 9. PCB top layer

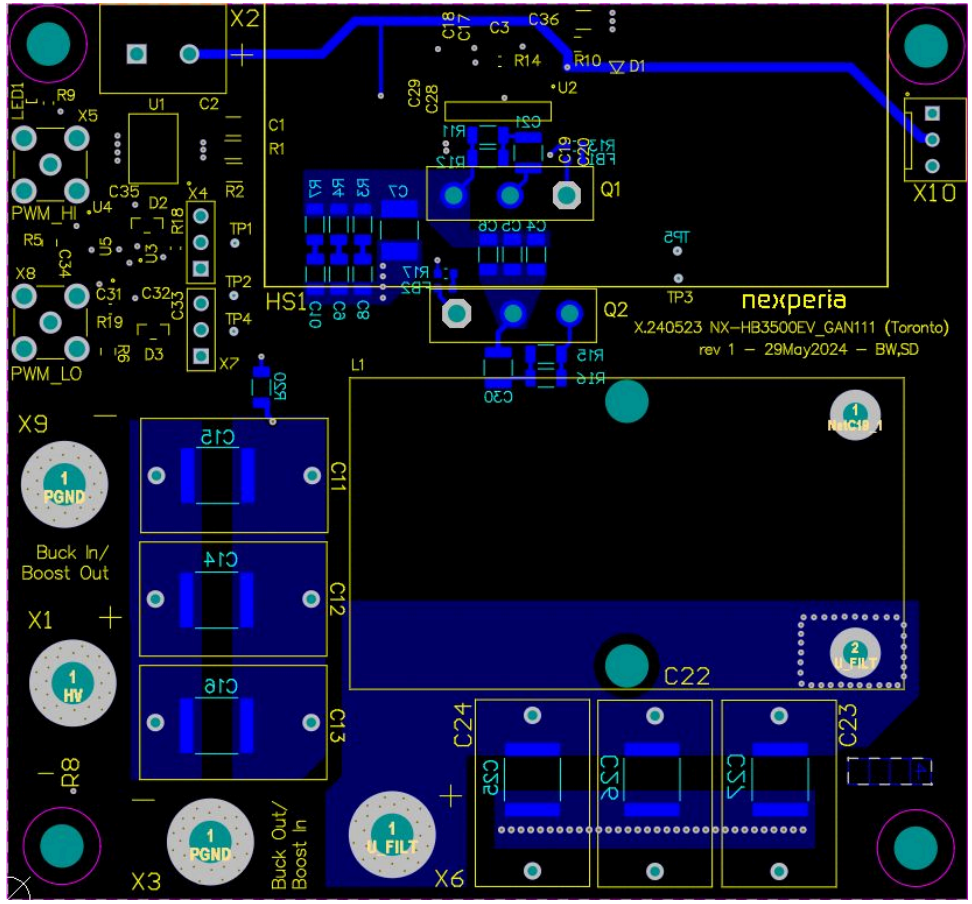


Fig. 10. PCB bottom layer

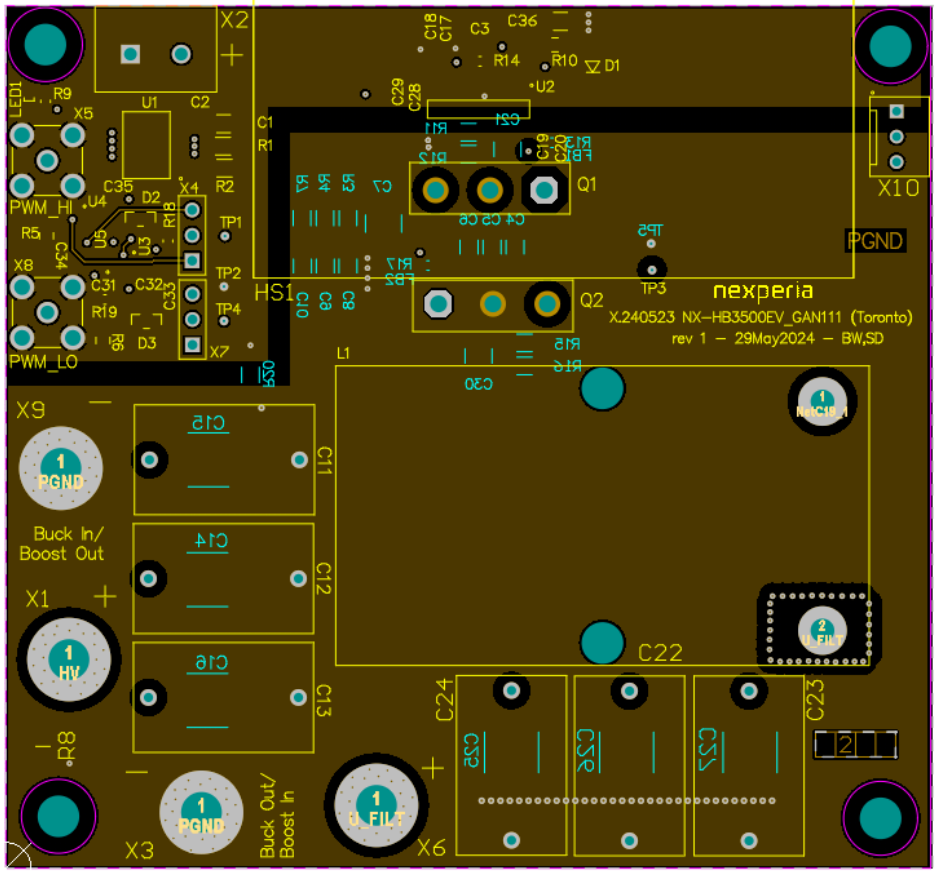


Fig. 11. PCB inner layer 2, ground plane

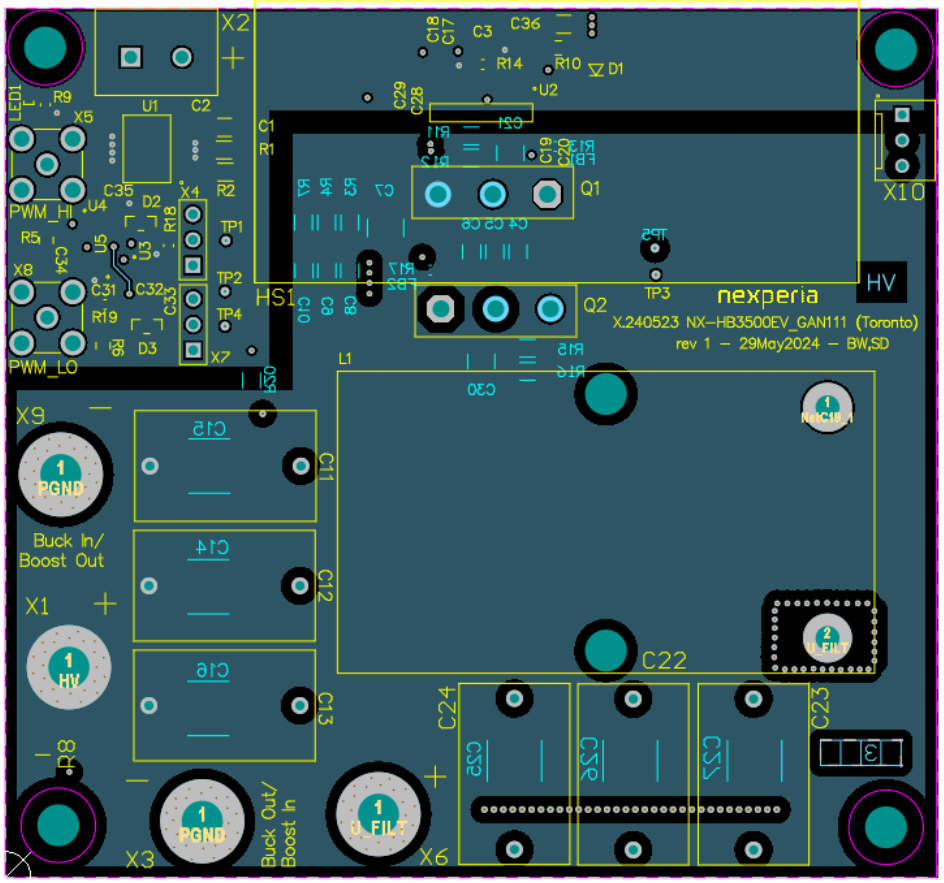


Fig. 12. PCB inner layer 3, power plane

7.3. NX-HB-GAN111UL evaluation board Bill of Materials (BOM)

Table 2. NX-HB-GAN111UL Bill of Materials

Name	Description	Designator	Qty	Manufacturer	Part number
CAP CER 10uF Â±10% 50V X5R 1206	Ceramic Capacitor 10uF Â±10% 50V X5R 1206	C1, C36	2	Wurth Electronics	885012108022
CAP CER 1uF Â±10% 50V X7R 0805	Ceramic Capacitor 1uF Â±10% 50V X7R 0805	C2	1	Wurth Electronics	885012207103
CAP CER 2u2 20% 25V X7R 0805	0805 2.2 uF 25 V Â±10 % Tolerance X7R Surface Mount Multilayer Ceramic Capacitor	C3	1	Wurth Electronics	885012207079
CAP CER 10nF Â±10% 1kV X7R 1206	Ceramic Capacitor 10nF Â±10% 1kV X7R 1206	C4, C5, C6, C8, C9, C10	6	Wurth Electronics	885342208021
CAP 100n 10% 1000V 1812	Cap Ceramic 0.1uF 1000V X7R 10% Pad SMD 1812	C7	1	KEMET	C1812C104KDRACAUTO
B32672P4225K000	Film Capacitor MKP 2.2uF Â±5% 450V Radial	C11, C12, C13, C22, C23, C24	6	TDK EPCOS	B32672P4225K000
CAP CER 0.1uF Â±10% 1KV X7R 2220	Ceramic Capacitor 0.1uF Â±10% 1KV X7R 2220	C14, C15, C16, C25, C26, C27	6	Wurth Electronics	885342214173
CAP CER 100nF Â±20% 50V X7R 0603	Ceramic Capacitor 100nF Â±20% 50V X7R 0603	C17, C18, C19, C28, C33, C34, C35	7	Wurth Electronics	885012206095
CAP CER 10uF Â±10% 25V X7S 0805	Ceramic Capacitor 10uF Â±10% 25V X7S 0805	C20, C29	2		
CAP CER 33pF Â±10% 1kV C0G 1210	Ceramic Capacitor 33pF Â±10% 1kV C0G 1210	C21, C30	2	Kyocera AVX	VJ1210A330KBGAT4X
CAP CER 100pF Â±1% 100V C0G 0603	Ceramic Capacitor 100pF Â±1% 100V C0G 0603	C32	1	Wurth Electronics	885012006079
PNU65010EP	Ultrafast recovery rectifier, 650V, 1A, CFP5 (SOD128)	D1	1	Nexperia	PNU65010EPX
BAT54C,215	BAT54 Series 30V 2 uA Surface Mount Schottky Barrier Diode - SOT-23	D2, D3	2	Nexperia	BAT54C,215
Cooling fan	60 x 60 x 15 mm 12 V 5400 RPM 30.4 CFM Vapo Bearing DC Fan	FAN1	1	Sunon	MF60151VX-1000U-A99

Name	Description	Designator	Qty	Manufacturer	Part number
BLM18PG300SN1D	Ferrite Bead 30Ohm 1A 0603	FB1, FB2	2	Murata	BLM18PG300SN1D
Cool innovations HS TO247 V	Cool innovations HS TO247 Vertical heatsink + Fan	HS1	1	Cool Innovations	3-242411 MS73377
330uH PFC Inductor TH PADS	Custom 330uH PFC Inductor	L1	1	Wurth Electronics	750371702
LED Green 0805	LED Green 2V 20mA 0805	LED1	1	Dialight	598-8160-107F
GAN111-650WSB	GaN FET 650V 97mOhm TO-247-3	Q1, Q2	2	Nexperia	GAN111-650WSB
RES SMD 4.99K 1% 1/4W 1206	Res Thick Film 1206 4.99K Ohm 1% 1/4W	R1	1	Bourns	CR1206-FX-4991ELF
RESISTOR SMD 499K 1% 1/W 1206	Res Thick Film 1206 499K Ohm 1% 1/4W SMD	R2	1	Vishay	CRCW1206499KFKEA
RES SMD 10R 1% 0.25W 1206	Chip Resistor 10R Â±1% 0.25W 1206	R3, R4, R7	3	Panasonic	ERJ-8ENF10R0V
ESR10EZPF49R9	Chip Resistor Anti-Surge 49.9R Â±1% 0.4W 0805	R5, R6	2	Rohm	ESR10EZPF49R9
RES SMD 10M .5% 1/4W 1206	Thick Film Resistors - SMD 1/4W 10Mohm .5% CRCW120610M0DHEAP	R8	1	Vishay Dale	CRCW120610M0DHEAP
RES SMD 2.2k 1% 0.1W 0603	Chip Resistor 2.2k Â±1% 0.1W 0603	R9	1	Vishay Dale	CRCW06032K20FKEB
ERJUP6F10R0V	Chip Resistor Anti-Surge 10R Â±1% 0.5W 0805	R10	1	Panasonic	ERJ-UP6F10R0V
RES 75R 1% 1206 1/4 W	Res Thick Film 1206 75R 1% 1/4W	R11, R12, R15, R16	4	Panasonic	CRCW120675R0FKEA
RES SMD 30R 1% 0.1W 0603 anti-surge	SMD Chip Resistor, 30 Ohm, Â± 1%, 250 mW, 0603, Thick Film, Anti-Surge	R13, R17	2	Panasonic	ERJ-PA3F30R0V
RES SMD 1k 0.1% 0.1W 0603	Chip Resistor 1k Â±0.1% 0.1W 0603	R14	1	Yageo	RT0603BRE071KL
RES SMD 1k 1% 0.1W 0603	Chip Resistor 1k Â±1% 0.1W 0603	R19	1		
RES SMD 0R JUMPER 1206	Chip Resistor 0R Jumper 1206	R20	1	Yageo	RC1206FR-070RL
LT3082EST#TRPBF	LDO Regulator Pos 0V to 40V 0.2A Automotive 4-Pin(3+Tab) SOT-223 T/R	U1	1	Analog Devices / Linear Technology	LT3082EST#TRPBF
SI8273ABD-IS1	Isolated Gate Driver 2.5KV	U2	1	Skyworks Solutions	SI8273ABD-IS1R
74HCT1G86GW	74HCT SINGLE GATE, SMD, 74HCT1G86, Logic Family / Base Number: 74HCT1G86, Logic Type: XOR, Output Current: 2mA, No....	U3, U5	2	Nexperia	74HCT1G86GW

Name	Description	Designator	Qty	Manufacturer	Part number
74LVC1G17GW	Schmitt Trigger Buffer 1-CH Non-Inverting CMOS 5-Pin TSSOP	U4	1	Nexperia	74LVC1G17GW
WE-746600330R	TERMINAL REDCUBE M3 SMD	X1, X3, X6, X9	4	Wurth Electronics	746600330R
CONN HEADER VERT 3POS 2.54MM	Connector Header Through Hole 3 position 0.100\ (2.54mm)"	X4, X7	2	Wurth Electronics	61300311121
SMA connector right angle	SMA Connector Right Angle PCB Jack 50Ohms	X5, X8	2	TE Connectivity	5-1814400-2
PAN PHILLIPS SCREW, M4 X .7 THRE	M4x0.7 Pan Head Machine Screw Phillips Drive Nylon	MP1, MP2, MP3, MP4	4	Essentra	50M040070P008
WE-970150485	WA-SPAII Plastic Spacer Stud, M4 Thread Internal, 15mm	MP5, MP6, MP7, MP8	4	Wurth Electronics	970150485
TERM BLOCK HDR 2POS VERT 5.08MM	2 Position Terminal Block Header, Male Pins, Shrouded (4 Side) 0.200\ (5.08mm) Vertical Through Hole"	X2	1	Wurth Electronics	691311500102
3-Pin Header 2.54mm lock	3 pin male Locking Header, THT, Vertical, pitch 2.54 mm, 1 x 3 position	X10	1	Wurth Electronics	61900311121
CAP CER 220pF Â±1% 50V C0G 0603	Ceramic Capacitor 220pF Â±1% 50V C0G 0603	C31	1	Wurth Electronics	885012006059
RES SMD 1.5k 1% 0.1W 0603	Chip Resistor 1.5k Â±1% 0.1W 0603	R18	1	Panasonic	ERJ-3EKF1501V
KK 254 crimp terminal	Contact, KK® 254, KK 254 2759, Socket, Crimp, 22 AWG, Tin Plated Contacts		2	Molex	08-50-0113
Housing connector	Molex, KK 254 Female Connector Housing, 2.54mm Pitch, 3 Way, 1 Row		1	Molex	22/01/3037
Alumina insulator	Placed on Q1 highside		1	Aavid	4169G
Heatsink paste			1	ELECTROLUBE	HTSP50T
60mmx60mm Metal Fan Guard			1		
M3 Plain nut			1		
M3 Plain Washer			2		
M3x20 Pan Head Pozi			1		
M4 Nuts	Nuts for heatsink		4		
M4x50 Pan Head Pozi	Cooling fan screw		4		

Name	Description	Designator	Qty	Manufacturer	Part number
M3x6 Pan head Pozi	Screws for X1, X3, X6, X9		4		
JUMPER W/TEST PNT 1X2PINS 2.54MM	Jumpers for X4, X7		2		

8. Using the board

The board can be used for evaluation of basic switching functionality in a variety of circuit configurations. It is not a complete circuit, but rather a building block. It can be used in steady-state DC/DC converter mode with output power up to 2.0 kW.

9. Dead-time control

The required form of the gate-drive signals is shown in Fig. 13. The times marked A are the dead-times when neither transistor is driven on. The dead-time must be greater than zero to avoid shoot-through currents. The Si8273ABD gate driver ICs does NOT have integrated dead-time functionality. The on-board pulse generator circuit, for example, creates dead-times of about 60 ns. The resulting dead-time at the gate pins of Q1 and Q2 is about 120 ns. IF gate drive signals are provided on X5 and X8 SMA connectors and X4 and X7 have jumpers to link pins 1 and 2, then the signals MUST have dead-time between them implemented by the user.

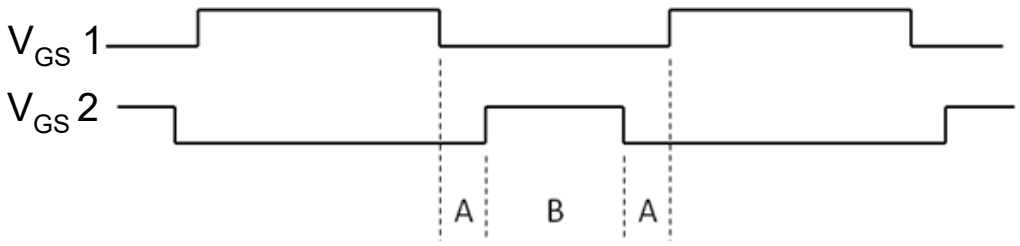


Fig. 13. Non-overlapping gate pulses

10. Probing

Test points TP3 and TP5, (SW NODE and PGND respectively), are provided for probing the switching waveform. In order to minimize inductance during measurement, the tip and the ground of the probe should be directly attached to the sensing points to minimize the sensing loop. Coiled bus wire can be effectively used to make these connections, as indicated in Fig. 14.

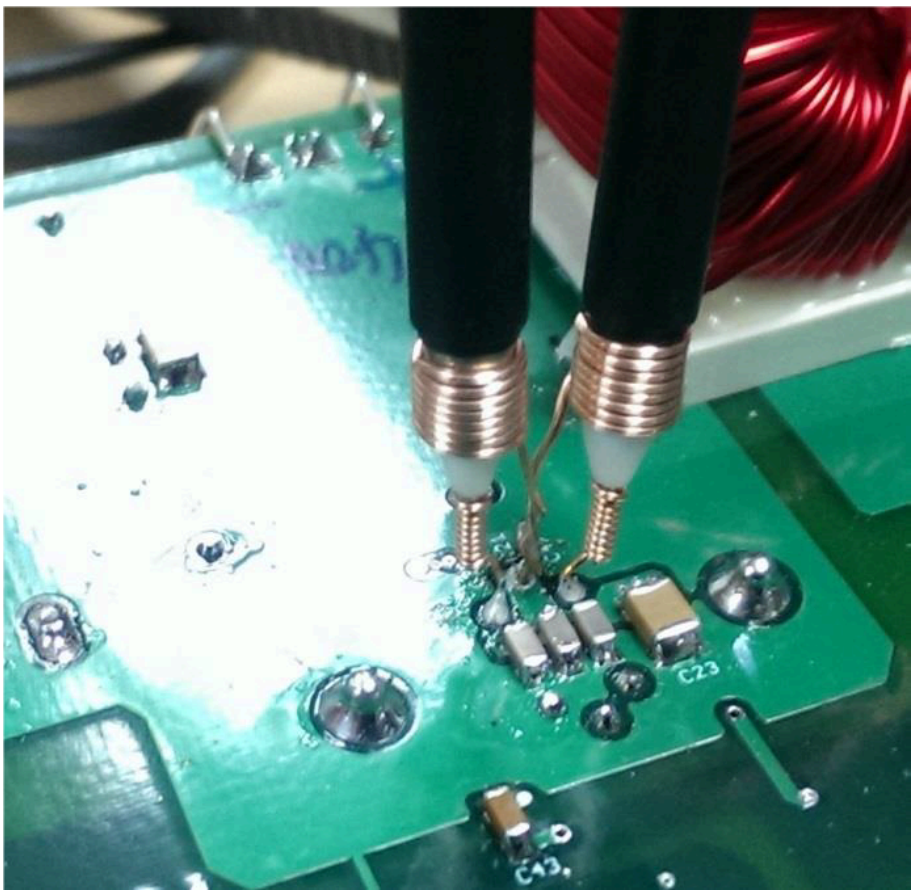


Fig. 14. Low-inductance probing of fast, high-voltage signals

11. Typical switching waveforms

Fig. 15, Fig. 16 and Fig. 17 show the typical switching waveforms with conditions:

- Load current = 9 A
- V_{supply} = 400 VDC
- V_{out} = 230 VDC

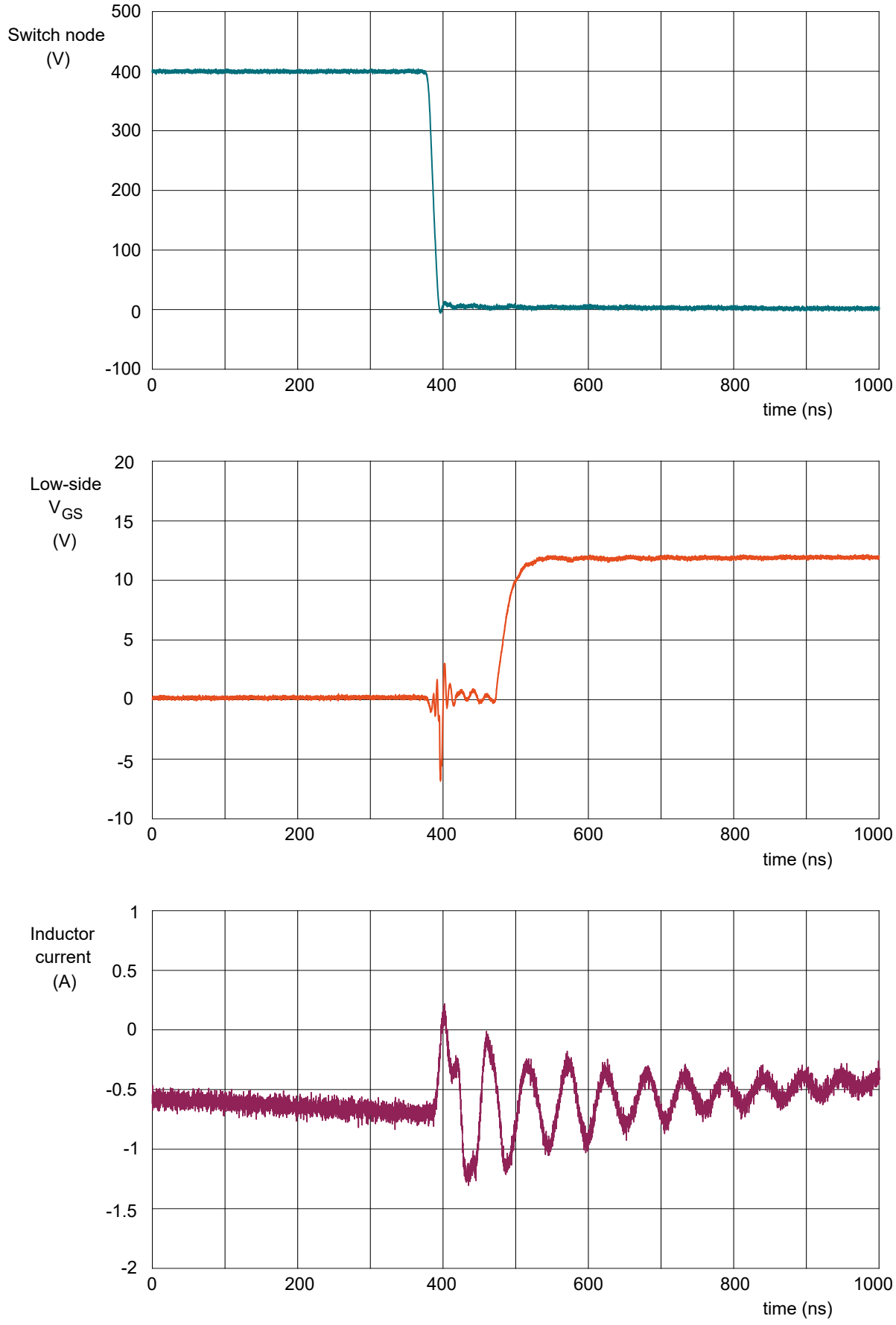


Fig. 15. Low-side turn ON

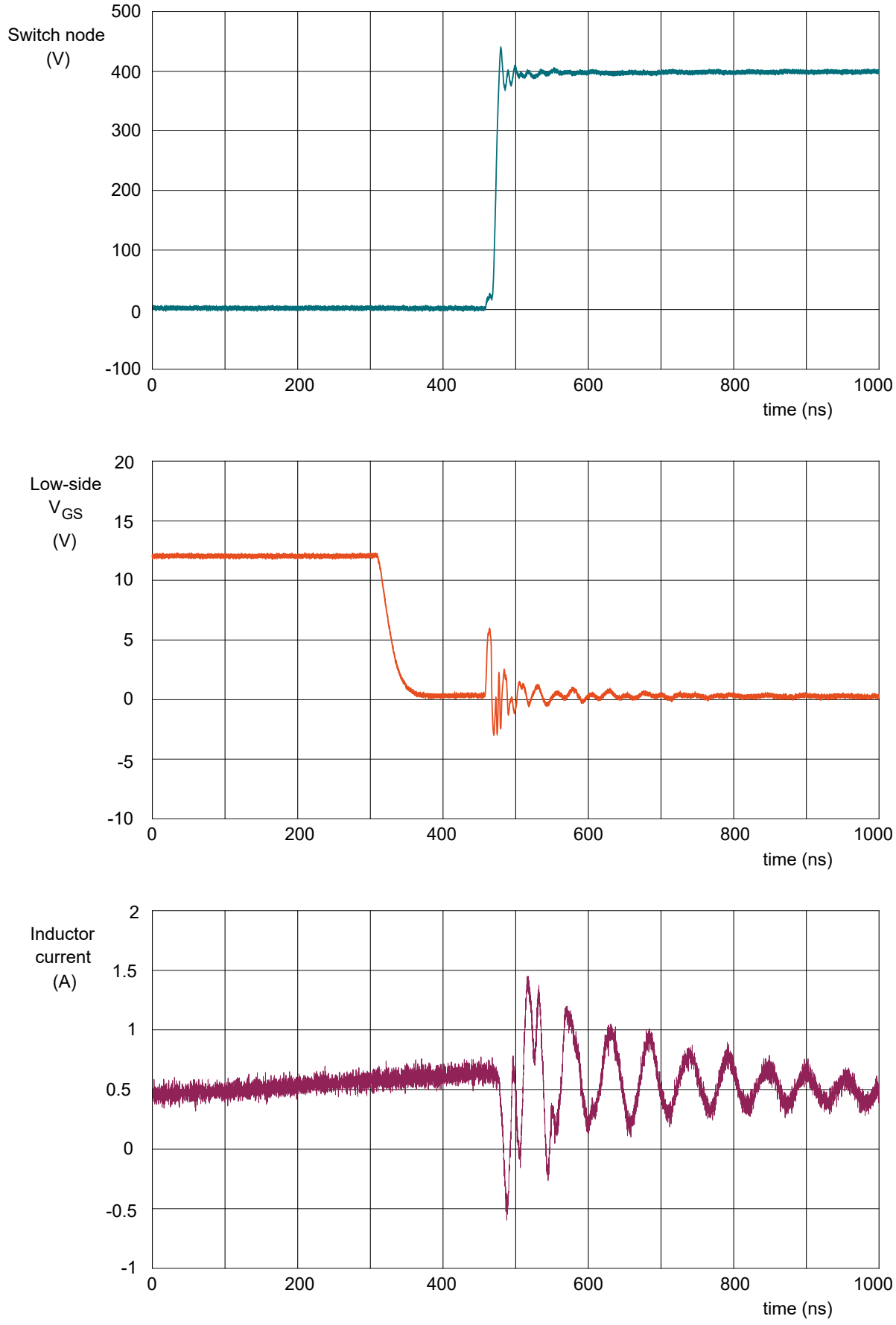


Fig. 16. Low-side turn OFF

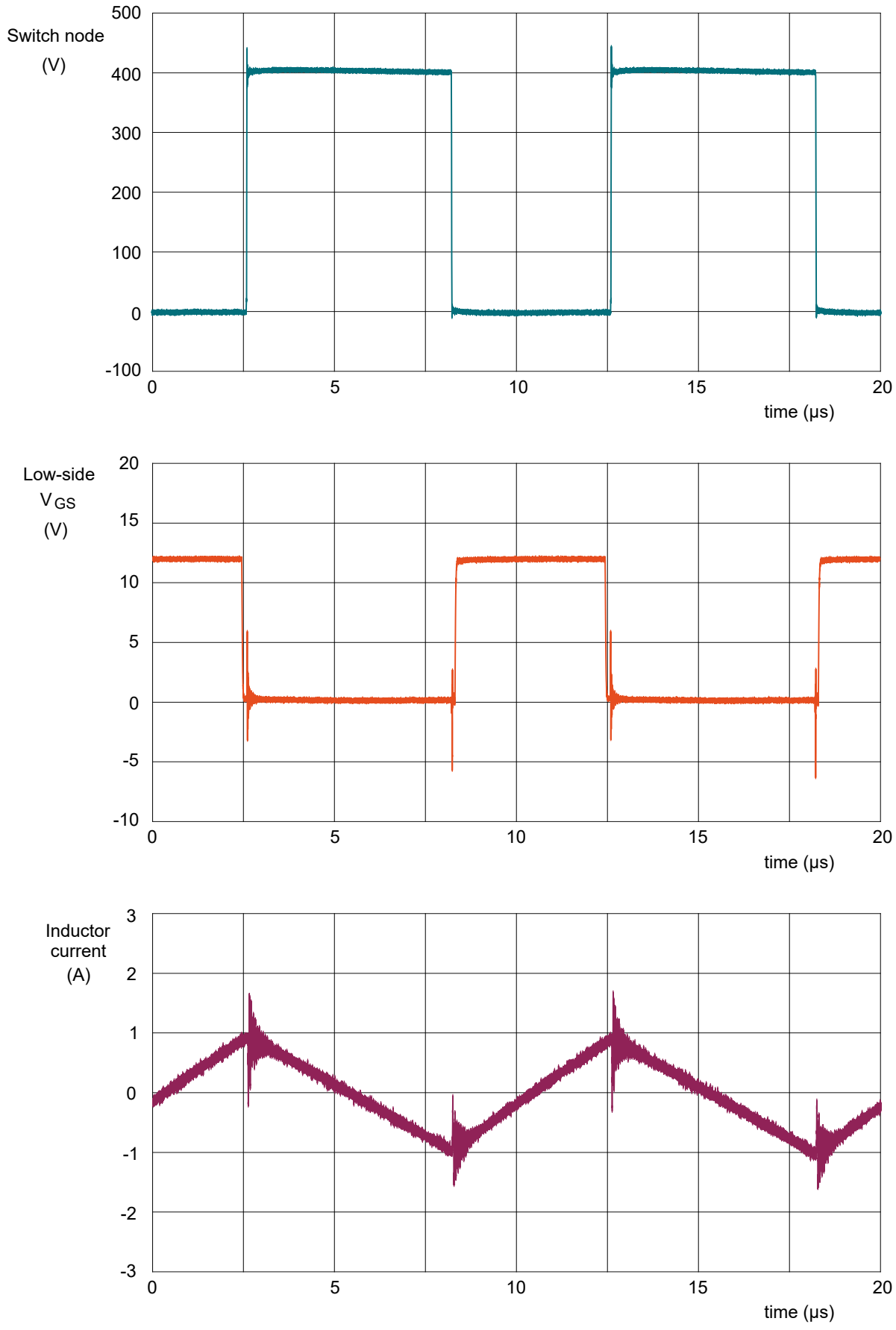
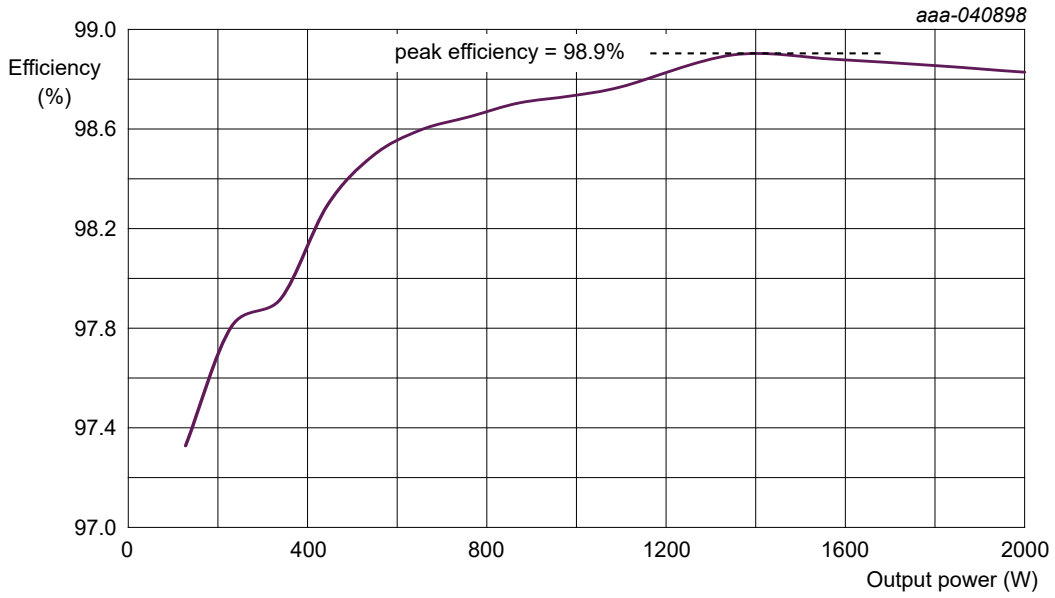


Fig. 17. Switching cycle

12. Efficiency sweep

Efficiency has been measured for this circuit in buck mode with a 400 VDC input and 230 VDC output, switching at 100 kHz.



R_G= 30 Ω; GFB = 30 Ω @ 100 MHz; snubber 33 pF, 37R5

Fig. 18. Efficiency for a buck converter 400 V: 230 V

13. Revision history

Table 3. Revision history

Revision number	Date	Description
2.0	2025-02-10	Update of section 7.3
1.0	2024-06-09	Initial version

14. Legal information

Definitions

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