



## DESCRIPTION

The MP8017 is an integrated, IEEE 802.3af-compliant, power over Ethernet (PoE) powered device (PD) with a flyback power converter. It is targeted for small-sized, 13W, isolated PoE applications.

The PD interface has all the functions of IEEE 802.3af, including detection, classification, inrush current limit, operation current limit, and a 100V hot-swap MOSFET.

The flyback converter is specifically designed for active-clamp primary-side regulation (PSR) flyback topologies. PSR provides a small-sized solution. The MP8017 can also be set to a secondary-side regulation (SSR) active-clamp flyback topology. SSR optimizes regulation through the optocoupler from the secondary side.

The MP8017 can support a front-end solution for PoE PD applications with a minimal number of external components. It is available in a QFN-19 (3mmx4mm) package.

## FEATURES

- IEEE 802.3af-Compliant
- 100V, 0.5Ω Powered Device (PD) Input MOSFET
- Active-Clamp Primary-Side Regulation (PSR) Flyback without Auxiliary Winding
- Active-Clamp Secondary-Side Regulation (SSR) Flyback through Optocoupler
- 0.37Ω and 0.75Ω Integrated Flyback MOSFETs
- Configurable Frequency Up to 650kHz
- 1.5A Switching Current Limit
- Output Diode Compensation in PSR Mode
- Configurable Soft-Start Time
- EMI Reduction with Frequency Dithering
- Overload Protection (OLP), Over-Voltage Protection (OVP), and Over-Temperature Protection (OTP) with Hiccup Mode
- Available in QFN-19 (3mmx4mm) Package



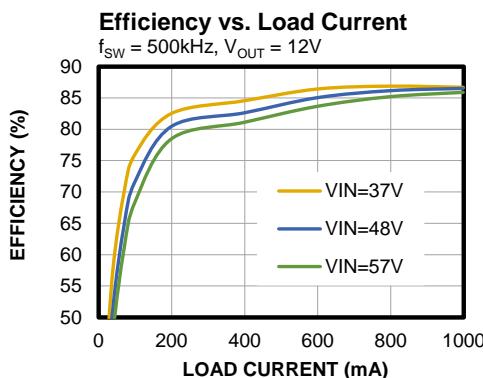
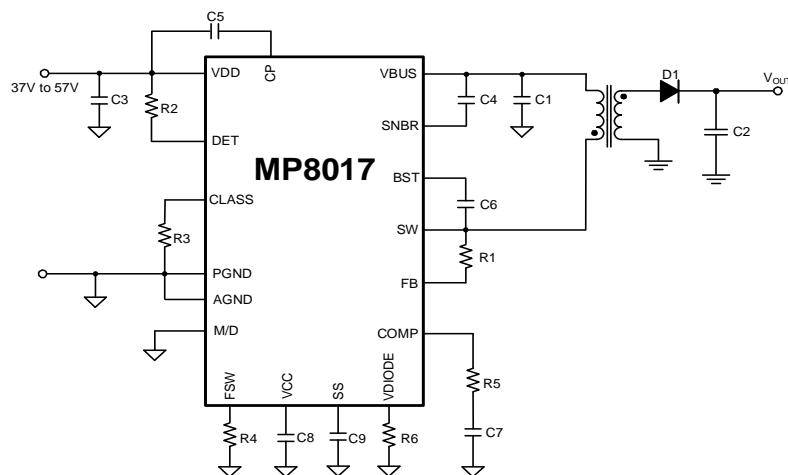
Optimized Performance with  
MPS Inductor MPL-AT Series

## APPLICATIONS

- IEEE 802.3af-Compliant Devices
- Security Cameras
- VoIP Phones
- Wireless Local Area Network (WLAN) Access Points)
- Internet of Things (IoT) Devices

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## TYPICAL APPLICATION



## ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8017GL	QFN-19(3mmx4mm)	See Below	1

\*For Tape & Reel, add suffix -Z (e.g. MP8017GL-Z).

## TOP MARKING

**MPYW**  
**8017**  
**LLL**

MP: MPS prefix

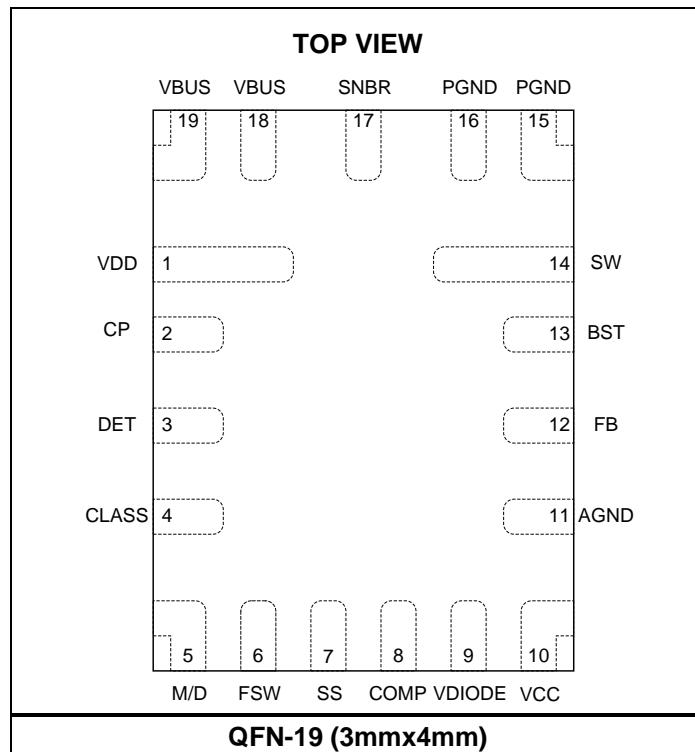
Y: Year code

W: Week code

8017: First four digits of the part number

LLL: Lot number

## PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	Description
1	VDD	<b>Positive power supply terminal from the PoE input power rail.</b>
2	CP	<b>Charge pump output for hot-swap FET driver power supply.</b> Connect a 0.01 $\mu$ F to 0.22 $\mu$ F capacitor from CP to VDD.
3	DET	<b>Powered device (PD) detection and power enable pin.</b> Connect a 24.9k $\Omega$ resistor between VDD and DET for PoE detection. Pull DET low to disable the class function, hot-swap MOSFET, and flyback converter.
4	CLASS	<b>Classification pin.</b> Connect a resistor from CLASS to AGND to configure the classification current.
5	M/D	<b>Feedback MODE and dither function selection pin.</b> See Table 2 on page 21 for the detailed function setting.
6	FSW	<b>Switching Frequency setting pin.</b> Connect an external resistor from the FSW pin to AGND to set the switching frequency ( $f_{sw}$ ).
7	SS	<b>Soft start and hiccup period control pin.</b> Connect one capacitor between the SS pin and AGND. SS controls the FB ramping slew rate in primary-side regulation (PSR) mode and controls the COMP ramp slew rate in secondary-side regulation (SSR) mode. The SS pin also controls the hiccup mode protection time period.
8	COMP	<b>Feedback loop control pin.</b> COMP is the FB error amplifier (EA) output pin for PSR mode and the feedback pin for SSR mode.
9	VDIODE	<b>Output rectifier diode voltage drop compensation pin.</b> A resistor connected from the VDIODE pin to AGND compensates the output voltage for different switching currents.
10	VCC	<b>DC/DC converter internal circuit power supply pin.</b> The VCC pin is powered through the internal LDO from VBUS. Connect a minimum 2.2 $\mu$ F capacitor from VCC to AGND to bypass the internal regulator. VCC also can be powered from external power to reduce internal LDO loss, but the external voltage should be clamped below 6.5V.
11	AGND	<b>Analog signal power ground.</b>
12	FB	<b>Output voltage feedback in PSR mode, and PSR\SSR OVP pin.</b> In PSR mode, connect one resistor from the SW pin to the FB pin to regulate the output voltage ( $V_{out}$ ). In SSR mode, the internal EA is disabled and the output voltage signal is fed back from the COMP pin. Connect one resistor from FB to SW to set the over-voltage protection (OVP) threshold, or float the FB pin if OVP is not required.
13	BST	<b>Bootstrap power pin for the high-side MOSFET driver.</b> Connect one 0.22 $\mu$ F capacitor between BST and SW.
14	SW	<b>Drain of the converter's main switching MOSFET.</b>
15, 16	PGND	<b>Power ground of the flyback converter.</b>
17	SNBR	<b>Active clamp snubber capacitor connection pin.</b> The SNBR pin is connected to the drain of the internal SYNC FET.
18, 19	VBUS	<b>Source of the PD hot-swap MOSFET.</b> The VBUS pin supplies power for the flyback converter.

**ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

VDD, VBUS, DET, SW, SNBR.....	-0.3V to +105V
SW (<20ns) .....	-3V to +110V
FB.....	$V_{BUS}$ - 0.5V to $V_{BUS}$ +0.2V
CP to VDD, BST to SW.....	-0.3V to +7V
All other pins .....	-0.3V to +7V
FB max source current.....	2mA <sup>(2)</sup>
FB max sink current .....	200 $\mu$ A <sup>(2)</sup>
Continuos power dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(3) (5)</sup> .....	2.5W
Junction temperature .....	150°C
Lead temperature .....	260°C
Operating temperature .....	-65°C to +150°C

**Recommended Operating Conditions <sup>(4)</sup>**

Supply voltage ( $V_{DD}$ ) .....	0V to 57V
FB max source current.....	1mA <sup>(2)</sup>
FB sink current.....	100 $\mu$ A <sup>(2)</sup>
Operating junction temp ( $T_J$ ) ....	-40°C to +125°C

**Thermal Resistance  $\theta_{JA}$   $\theta_{JC}$** 

QFN-19 (3mmx4mm)	
EVL8017-L-00A <sup>(5)</sup> .....	50.....4.....°C/W
JESD51-7 <sup>(6)</sup> .....	45.....5.2....°C/W

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The FB maximum sink/source current should be limited. See the FB Maximum Sink/Source Current Setting section on page 23 for more details.
- 3) The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J$  (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) = ( $T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 4) The device is not guaranteed to function outside of its operating conditions.
- 5) Measured on EVL8017-L-00A (2-layer, 42mmx60mm) PCB.
- 6) The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

$V_{DD} = 48\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  <sup>(7)</sup>, typical values are tested at  $T_J = 25^\circ\text{C}$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Detection</b>						
Detection on	$V_{DET-ON}$	$V_{DD}$ rising		1.2	1.5	V
Detection off	$V_{DET-OFF}$	$V_{DD}$ rising	10.1	11		V
DET leakage current	$V_{DET-LK}$	$V_{DET} = V_{DD} = 57\text{V}$ , measure $I_{DET}$		0.1	5	$\mu\text{A}$
Bias current	$V_{DET-BIAS}$	$V_{DD} = 10.1\text{V}$ , float DET pin, not in mark event, measure $I_{SUPPLY}$			12	$\mu\text{A}$
Detection current	$I_{DET}$	$V_{DD} = 2\text{V}$ , measure $I_{SUPPLY}$ , $R_{DET} = 24.9\text{k}\Omega$	80	82.5	85	$\mu\text{A}$
		$V_{DD} = 10.1\text{V}$ , measure $I_{SUPPLY}$ , $R_{DET} = 24.9\text{k}\Omega$	400	410	420	$\mu\text{A}$
DET disable threshold	$V_{DET-SD}$	Disable functions except detection, DET falling edge	2.9	3.2	3.5	V
DET disable threshold hysteresis	$V_{DET-SD-HYS}$			0.5		V
<b>Classification</b>						
Classification stability time				0.25		ms
CLASS output voltage	$V_{CLASS}$	$13\text{V} < V_{DD} < 21\text{V}$ , $1\text{mA} < I_{CLASS} < 44\text{mA}$	1.11	1.16	1.21	V
Classification current	$I_{CLASS}$	$13 \leq V_{VDD} \leq 21\text{V}$ , guaranteed by $V_{CLASS}$				
		$R_{CLASS} = 578\Omega$ , $13\text{V} \leq V_{DD} \leq 21\text{V}$	1.8	2	2.4	mA
		$R_{CLASS} = 110\Omega$ , $13\text{V} \leq V_{DD} \leq 21\text{V}$	9.9	10.55	11.3	
		$R_{CLASS} = 62\Omega$ , $13\text{V} \leq V_{DD} \leq 21\text{V}$	17.7	18.7	19.8	
		$R_{CLASS} = 41.2\Omega$ , $13\text{V} \leq V_{DD} \leq 21\text{V}$	26.6	28.15	29.7	
		$R_{CLASS} = 28.7\Omega$ , $13\text{V} \leq V_{DD} \leq 21\text{V}$	38.2	40.4	42.6	
Classification lower threshold	$V_{CL-ON}$	Regulator turns on, $V_{DD}$ rising	12	12.6	13.2	V
Classification lower threshold hysteresis	$V_{CL-L-HYS}$	Lower threshold hysteresis	1.3	1.5	1.7	V
Classification upper threshold	$V_{CL-OFF}$	Regulator turns off, $V_{DD}$ rising	21.2	22.2	23.2	V
Classification upper threshold hysteresis	$V_{CL-U-HYS}$	Upper threshold hysteresis		0.5		V
Mark event reset threshold	$V_{MARK-L}$		4.5	5	5.5	V
Max mark event voltage	$V_{MARK-H}$		10.4	11.1	11.8	V
Mark event current	$I_{MARK}$		1.5	2	2.5	mA
Mark event resistance	$R_{MARK}$	2-point measurement at 5.5V and 10.1V, $\Delta V/\Delta I$	45			$\text{k}\Omega$
IC supply current during classification	$I_{IN-CLASS}$	$V_{DD} = 17.5\text{V}$ , CLASS floating		120	200	$\mu\text{A}$
Class leakage current	$I_{LEAKAGE}$	$V_{CLASS} = 0\text{V}$ , $V_{DD} = 57\text{V}$			1	$\mu\text{A}$

## ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = 48\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ <sup>(7)</sup>, typical values are tested at  $T_J = 25^\circ\text{C}$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>PD Under-Voltage Lockout (UVLO)</b>						
VDD turn-on threshold	$V_{DD-R}$	$V_{DD}$ rising	35	37.5	40	V
VDD turn-off threshold	$V_{DD-F}$	$V_{DD}$ falling	30	32	34	V
VDD UVLO hysteresis	$V_{DD-HYS}$		5	5.5		V
Input leakage current	$V_{DD-LK}$	$V_{DD} = 29.5\text{V}$			50	$\mu\text{A}$
IC supply current during operation	$I_Q$	No load, $f_{SW} = 500\text{kHz}$		3.5	4.0	mA
<b>Pass Device and Current Limit</b>						
PD MOSFET on resistance	$R_{ON-PD}$	360mA load on $V_{BUS}$		0.5		$\Omega$
CP regulation voltage	$V_{CP}$			5.5		V
PD current limit	$I_{PD-LIMT}$	$V_{BUS}$ drop from $V_{DD}$ , $V_{DD} - V_{BUS} = 1\text{V}$	390	420		mA
Inrush current limit	$I_{INRUSH}$	$V_{BUS}$ ramps up from low to high, $V_{DD} - V_{BUS} = 1\text{V}$		120		mA
Inrush current termination	$I_{TERM}$	$V_{BUS}$ rising, $I_{TERM}$		96		mA
Inrush to operation mode delay	$t_{DELAY}$		80	100		ms
Current foldback threshold	$V_{BUS-FOLD}$	$V_{BUS}$ falling, $V_{DD} - V_{BUS}$		10		V
Foldback deglitch time	$t_{BUS-FOLD}$	$V_{BUS}$ falling to inrush current		1		ms
<b><math>V_{BUS}</math> Over-Voltage Protection (OVP)</b>						
$V_{BUS}$ maximum regulated voltage	$V_{BUS-CLAMP}$		58	61	64	V
<b>Converter Power Supply</b>						
Converter $V_{BUS}$ UVLO rising threshold	$V_{BUS-R}$	$V_{BUS}$ start charge $V_{CC}$		10		V
Converter $V_{BUS}$ UVLO falling threshold	$V_{BUS-F}$	$V_{BUS}$ stop charge $V_{CC}$		8		V
$V_{CC}$ regulation	$V_{CC}$	Load = 0mA to 10mA	5.2	5.5	5.8	V
$V_{CC}$ UVLO rising threshold	$V_{CC-R}$	$V_{DD}$ exceeds the UVLO threshold, $V_{CC}$ rising	4.4	4.6	4.8	V
$V_{CC}$ UVLO falling threshold	$V_{CC-F}$	$V_{DD}$ exceeds the UVLO threshold, $V_{CC}$ falling	4.2	4.4	4.6	V
SNBR discharge threshold before switching		$V_{SNBR} - V_{BUS}$		1.5		V
SNBR discharge current		Discharge to $V_{BUS}$		1.2		mA
<b>Feedback (FB) Voltage</b>						
FB regulation current	$I_{FB-REG}$	$V_{BUS} = 37\text{V} - 57\text{V}$ , $T_J = 25^\circ\text{C}$	99	100	101	$\mu\text{A}$
		$V_{BUS} = 37\text{V} - 57\text{V}$ , $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$	98	100	102	$\mu\text{A}$
FB to $V_{BUS}$ offset voltage	$V_{FB-OFFSET}$	$V_{FB} - V_{BUS}$ , 100 $\mu\text{A}$ pull up on FB	-50	0	+50	mV
FB feedback OVP threshold	$I_{FB-OVP}$		115	125	135	$\mu\text{A}$

## ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = 48 \text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$  <sup>(7)</sup>, typical values are tested at  $T_J = 25^\circ\text{C}$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Error Amplifier (EA)</b>						
Error amplifier gain		PSR mode, $I_{FB}$ is $\pm 5\mu\text{A}$ from $I_{FB-REG}$ , $V_{COMP} = 1.5\text{V}$		12		$\mu\text{A}/\mu\text{A}$
Amplifier maximum source current	$I_{EA-SOURCE}$	PSR mode, $V_{COMP} = 1.5\text{V}$ , $I_{FB} = 90\mu\text{A}$		-110		$\mu\text{A}$
Amplifier maximum sink current	$I_{EA-SINK}$	PSR MODE, $V_{COMP} = 1.5\text{V}$ , $I_{FB} = 110\mu\text{A}$		110		$\mu\text{A}$
COMP high voltage	$V_{COMP\_H}$	PSR mode, $I_{FB} = 90\mu\text{A}$		3.2		V
		SSR mode, float COMP		3.5		V
COMP pull-up resistors	$R_{COMP}$	SSR mode	9	10	11	$\text{k}\Omega$
COMP pull-up bias current	$I_{COMP-BIAS}$	SSR mode	90	105	120	$\mu\text{A}$
<b>PSR Mode Regulation Compensation</b>						
$V_{OUT}$ compensation gain		LS-FET current to $V_{DIODE}$ voltage gain		1		V/A
<b>Switching MOSFET</b>						
Low-side MOSFET (LS-FET) on resistance	$R_{ON-LS}$			0.37		$\Omega$
High-side MOSFET (HS-FET) on resistance	$R_{ON-HS}$			0.75		$\Omega$
LS-FET leakage current	$I_{LS-LK}$	SW - PGND = 100V		0.1	10	$\mu\text{A}$
HS-LET leakage current	$H_{LS-LK}$	$V_{BUS}$ - SW = 100V		0.1	10	$\mu\text{A}$
<b>M/D Pin Setting</b>						
M/D pin detection current	$I_{M/D}$		90	107	124	$\mu\text{A}$
M/D detection period	$t_{M/D}$			250		$\mu\text{s}$
M/D pin detection threshold voltage <sup>(8)</sup>	$V_{M/D}$	Voltage level 1 range			0.1	V
		Voltage level 2 range	0.5		0.95	V
		Voltage level 3 range	1.15		1.95	V
		Voltage level 4 range	2.15			V
<b>Frequency Dither</b>						
Dither frequency range <sup>(9)</sup>				$\pm 6\%$		$f_{SW}$
Dither injection frequency <sup>(9)</sup>				9		kHz
<b>Overload Protection (OLP), Short-Circuit Protection (SCP), Over-Voltage Protection (OVP)</b>						
LS-FET switching current limit	$I_{LS-LIM}$		1.3	1.5	1.65	A
SCP limit	$I_{LS-SCP}$			2.1		A
HS-FET and LS-FET zero-current detection (ZCD)	$I_{ZCD}$			0		mA
HS-FET negative current limit	$I_{HS\_LIM}$	SNBR to SW	-0.9	-0.8	-0.7	A

## ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = 48\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ <sup>(7)</sup>, typical values are tested at  $T_J = 25^\circ\text{C}$ , unless otherwise noted.

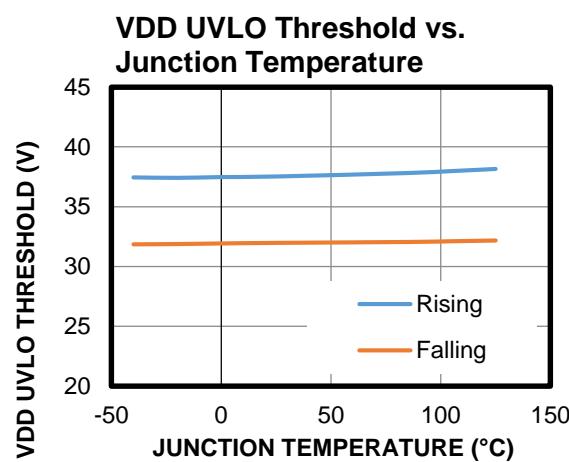
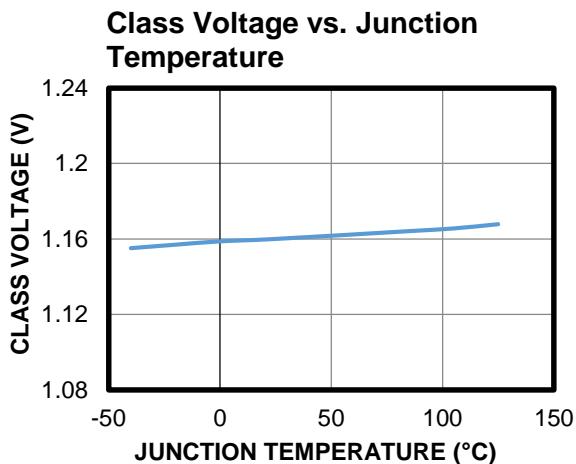
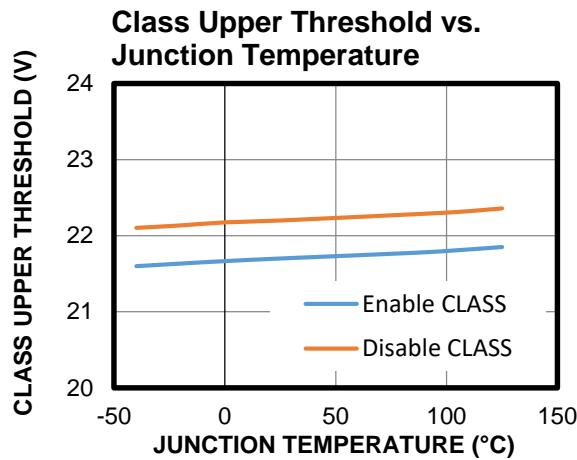
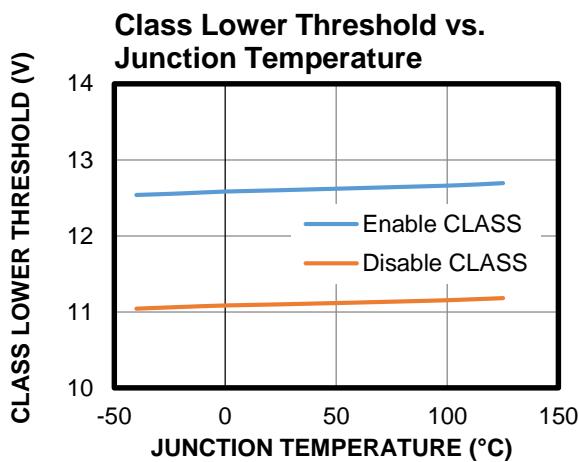
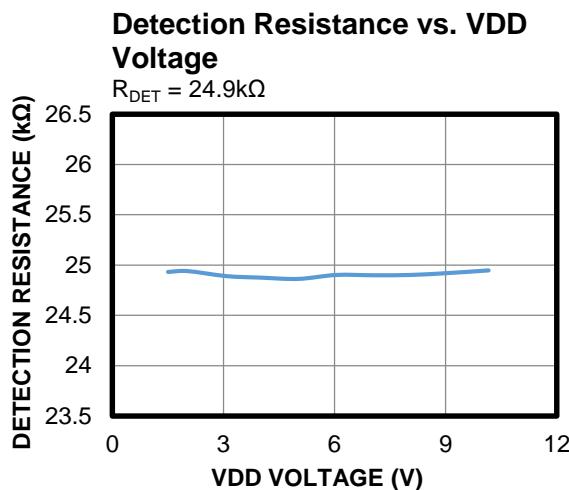
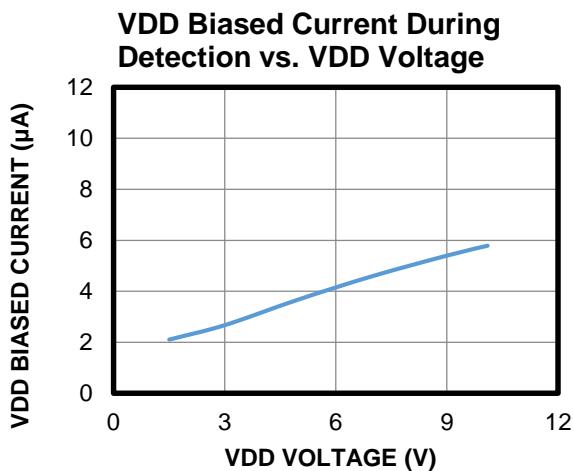
Parameter	Symbol	Condition	Min	Typ	Max	Units
SS charge current	$I_{SS}$			50		$\mu\text{A}$
Overload detection SS discharge current				20		$\mu\text{A}$
SS discharge current during protection				2		$\mu\text{A}$
SS charged threshold voltage	$V_{SS}$			3.5		V
Overload shutdown threshold voltage	$V_{SS-P}$			3		V
Protection reset threshold voltage	$V_{SS-RESET}$			0.2		V
SNBR pin over-voltage (OV) threshold	$V_{SNBR\_OVP}$			105		V
<b>Switching Frequency</b>						
Switching frequency	$f_{SW}$	$R_{FREQ} = 9.31\text{k}\Omega$	450	500	550	kHz
		$R_{FREQ} = 18.7\text{k}\Omega$	215	250	285	kHz
Foldback frequency	$f_{SW-FOLD}$	SS = 0V or FB = 0V		80		kHz
Minimum on time	$t_{MIN-ON}$			200		ns
Minimum off time	$t_{MIN-OFF}$		700	800	900	ns
Maximum duty cycle	$D_{MAX}$			75		%
<b>Thermal Protection</b>						
Thermal shutdown temperature	$T_{SD}$			150		$^\circ\text{C}$
Thermal shutdown hysteresis	$T_{HYS}$			20		$^\circ\text{C}$
Over-temperature protection (OTP) cool down timer	$t_{SD-COOL}$		80	100		ms

### Notes:

- 7) Not tested in production. Guaranteed by over-temperature correlation.
- 8) See Table 2 on page 21 to configure different voltage levels.
- 9) Guaranteed by sample characterization. Not tested in production.

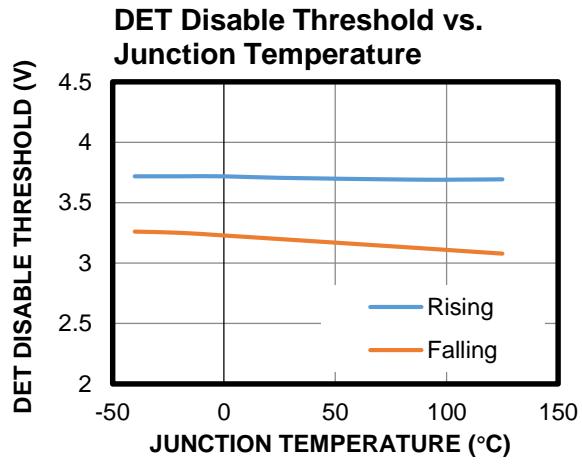
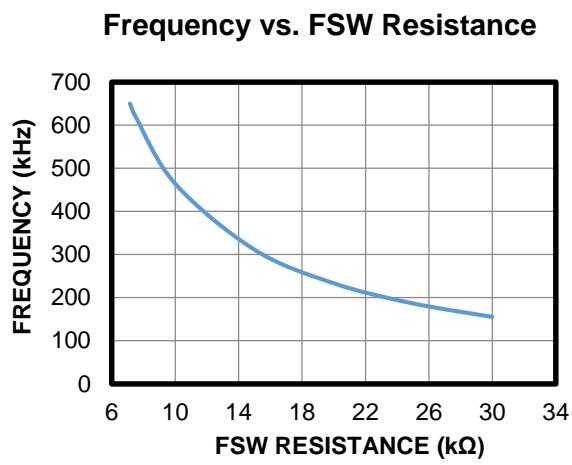
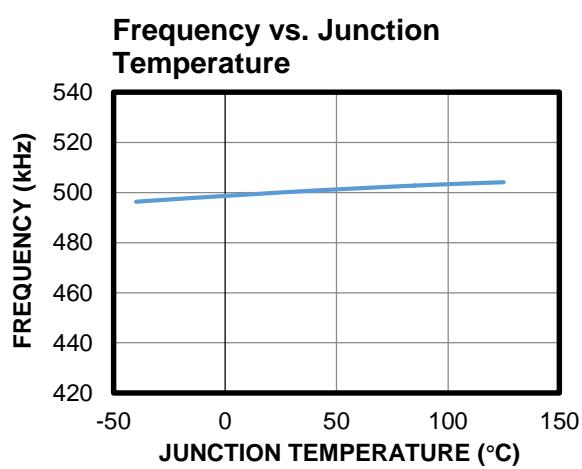
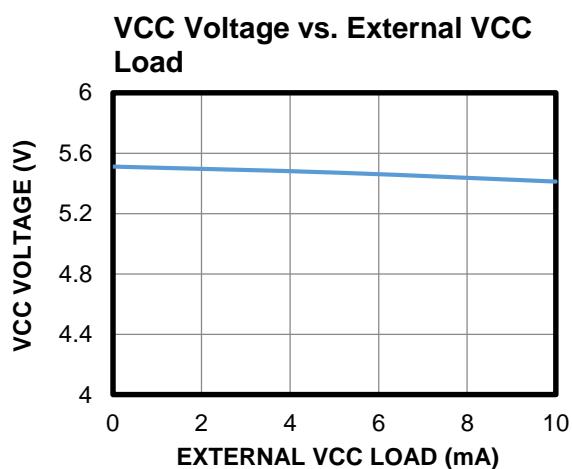
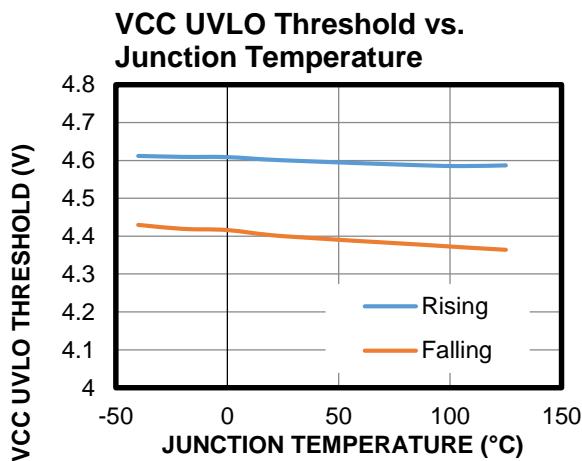
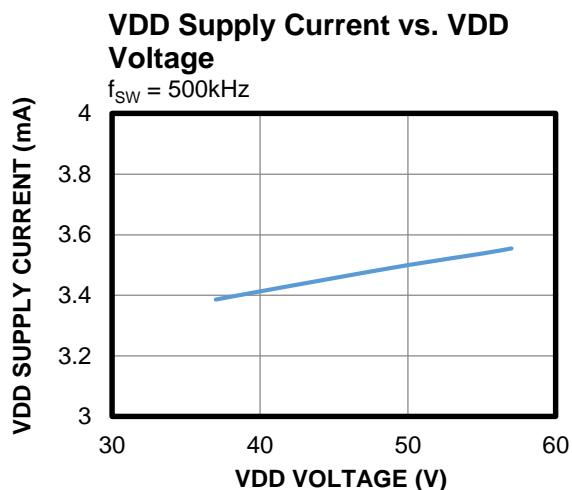
## TYPICAL CHARACTERISTICS

$V_{DD} = 48V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



## TYPICAL CHARACTERISTICS (continued)

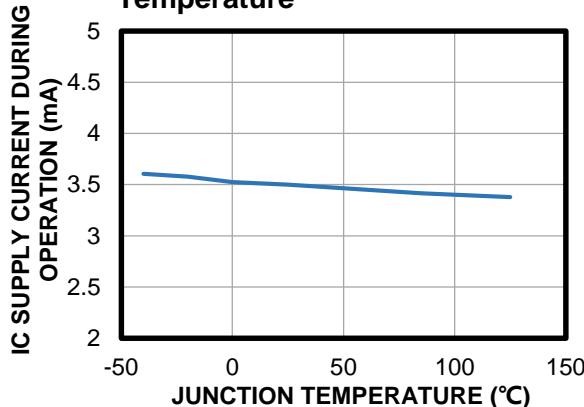
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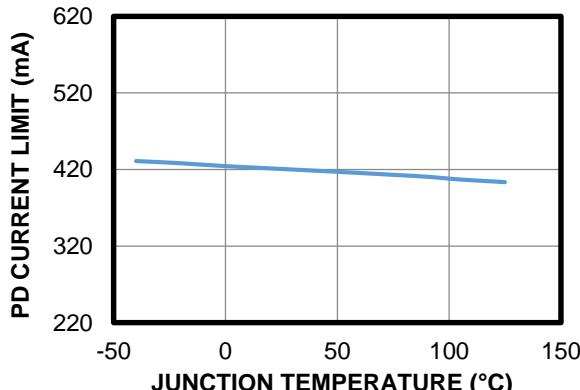
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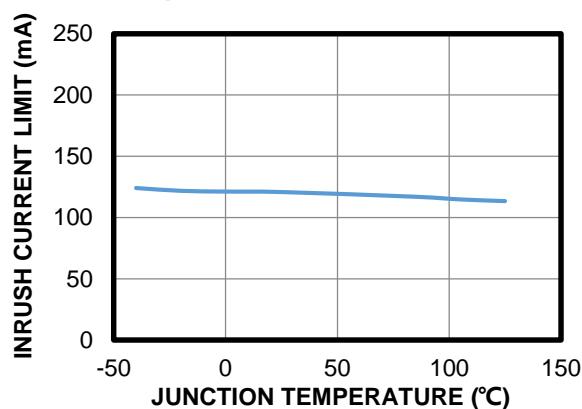
**IC Supply Current during Operation vs. Junction Temperature**



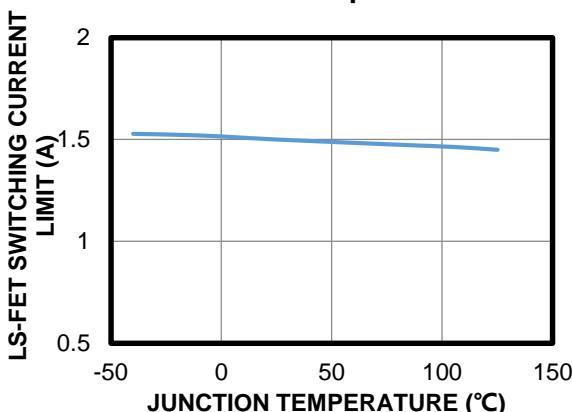
**PD Current Limit vs. Junction Temperature**



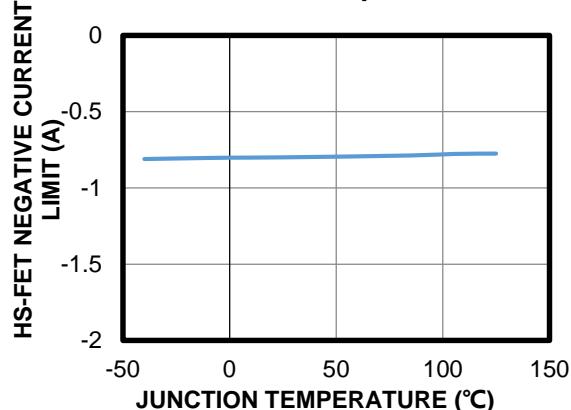
**Inrush Current Limit vs. Junction Temperature**



**LS-FET Switching Current Limit vs. Junction Temperature**

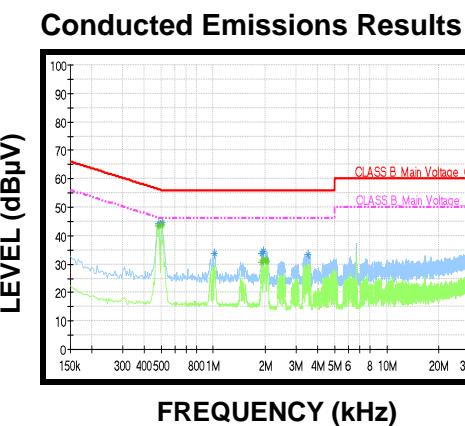
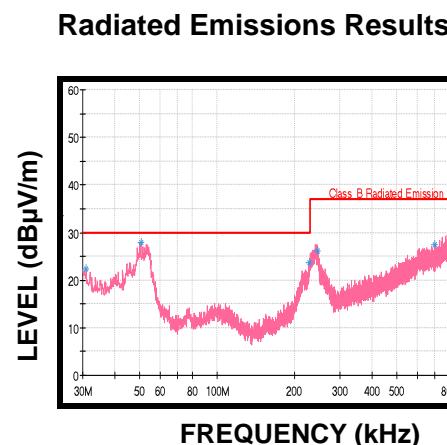
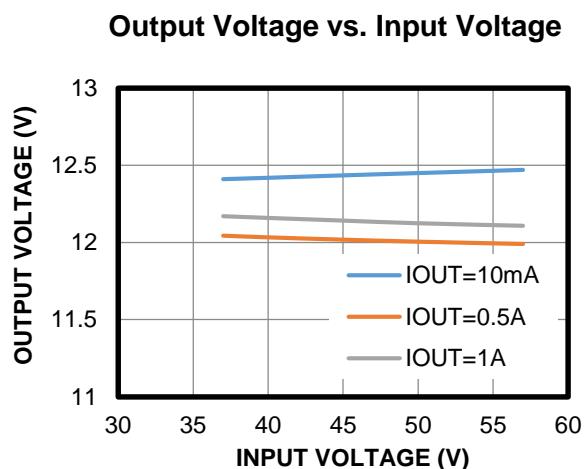
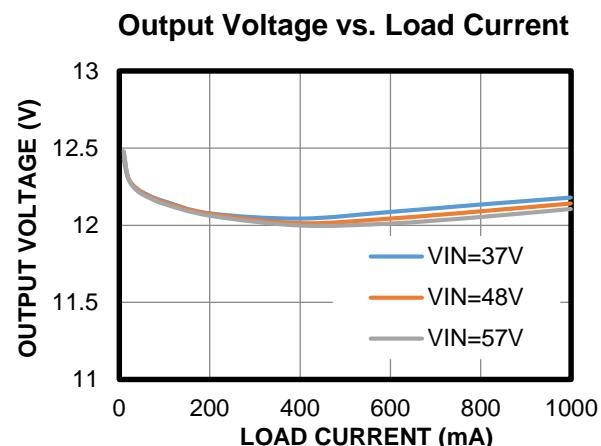
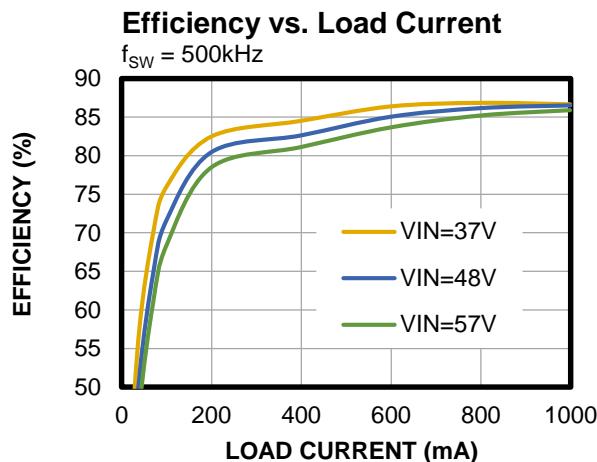


**HS-FET Negative Current Limit vs. Junction Temperature**



## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 48V$ ,  $V_{OUT} = 12V$ , load = 1A, PSR flyback mode,  $T_A = 25^\circ C$ , unless otherwise noted.

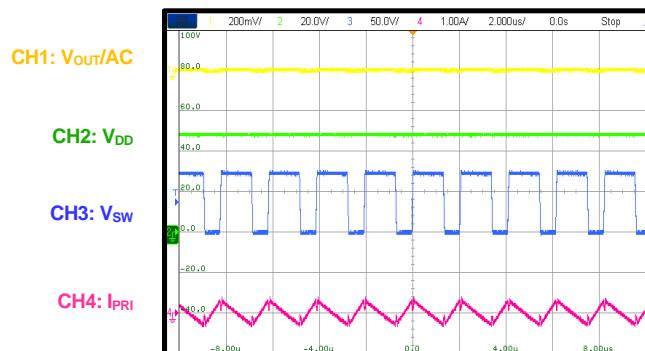


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{DD} = 48V$ ,  $V_{OUT} = 12V$ , load = 1A, PSR flyback mode,  $T_A = 25^\circ C$ , unless otherwise noted.

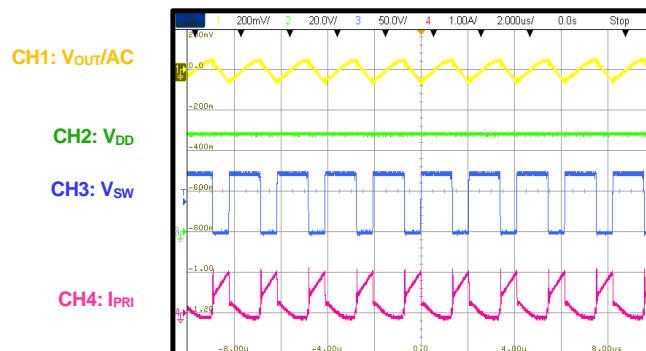
### Steady State

$I_{OUT} = 0A$



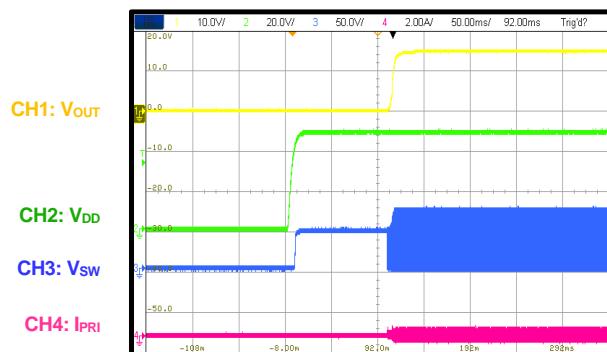
### Steady State

$I_{OUT} = 1A$



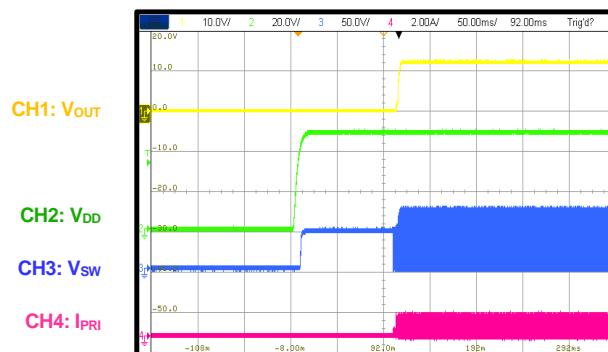
### Start-Up through VDD

$I_{OUT} = 0A$



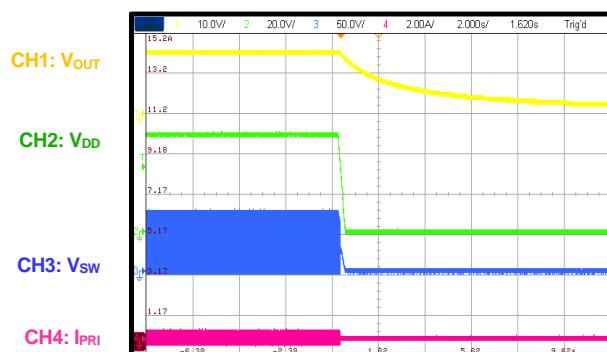
### Start-Up through VDD

$I_{OUT} = 1A$



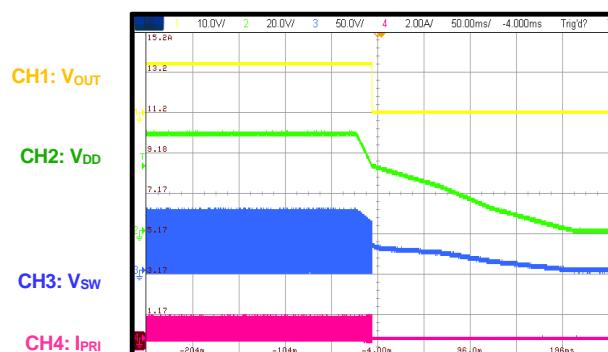
### Shutdown through VDD

$I_{OUT} = 0A$



### Shutdown through VDD

$I_{OUT} = 1A$

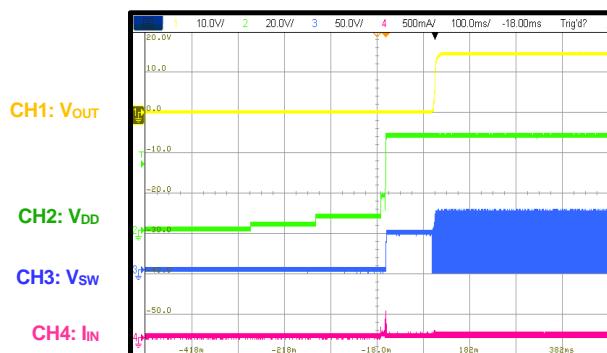


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{DD} = 48V$ ,  $V_{OUT} = 12V$ , load = 1A, PSR flyback mode,  $T_A = 25^\circ C$ , unless otherwise noted.

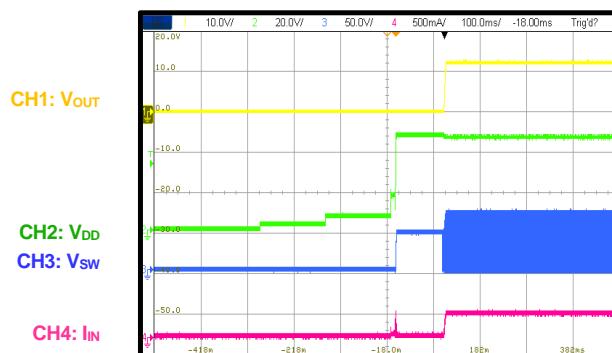
### Start-Up through PSE

$I_{OUT} = 0A$



### Start-Up through PSE

$I_{OUT} = 1A$



### Load Transient Response

$I_{OUT} = 10mA$  to  $0.5A$ ,  $I_{RAMP} = 25mA/\mu s$



### Load Transient Response

$I_{OUT} = 0.5A$  to  $1A$ ,  $I_{RAMP} = 25mA/\mu s$



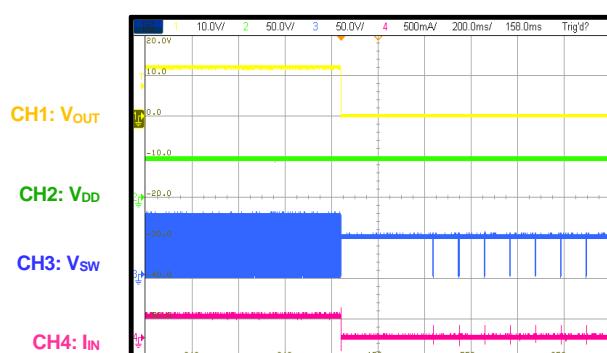
### SCP Entry

$I_{OUT} = 0A$  to short



### SCP Entry

$I_{OUT} = 1A$  to short

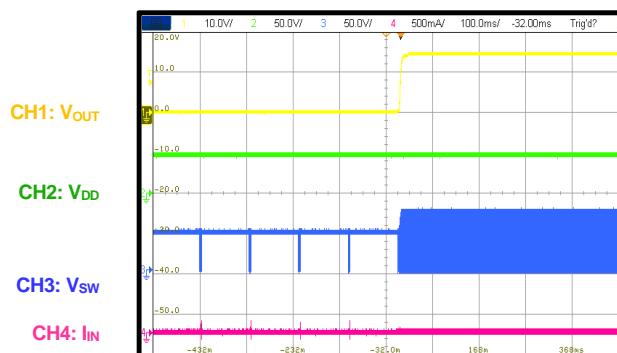


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{DD} = 48V$ ,  $V_{OUT} = 12V$ , load = 1A, PSR flyback mode,  $T_A = 25^\circ C$ , unless otherwise noted.

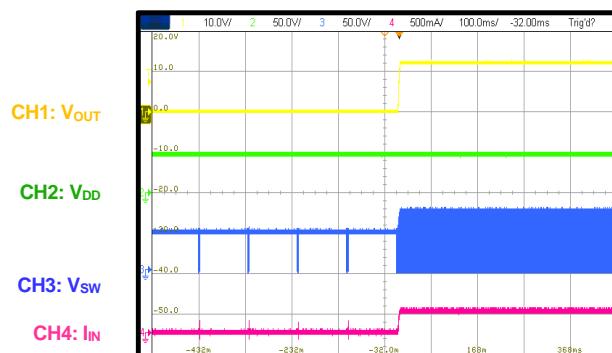
### SCP Recovery

$I_{OUT}$  = Short to 0A



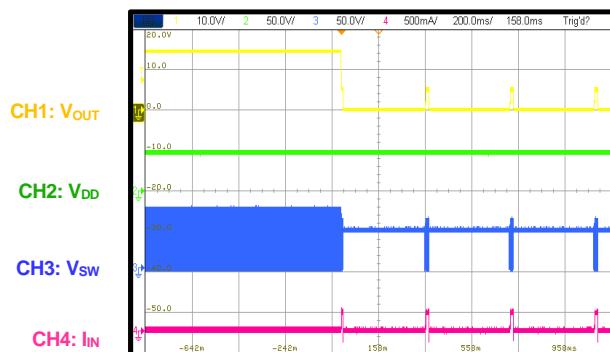
### SCP Recovery

$I_{OUT}$  = Short to 1A



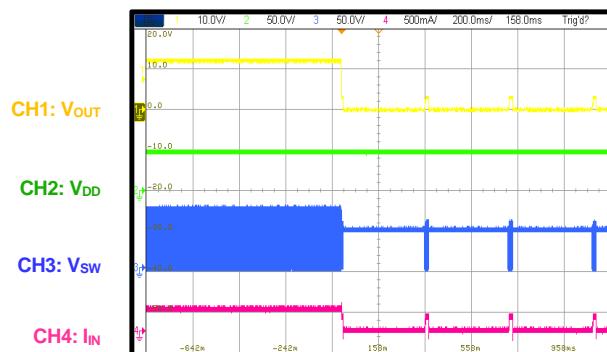
### OCP Entry

$I_{OUT}$  = 0A to overload



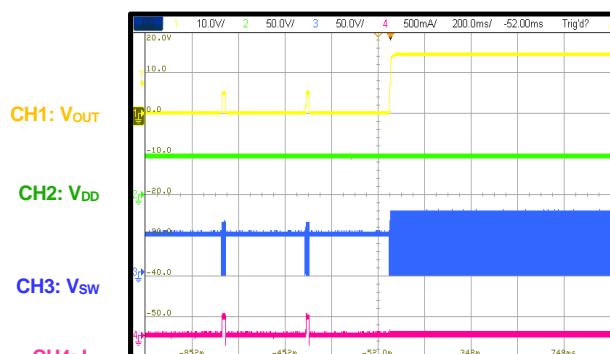
### OCP Entry

$I_{OUT}$  = 1A to overload



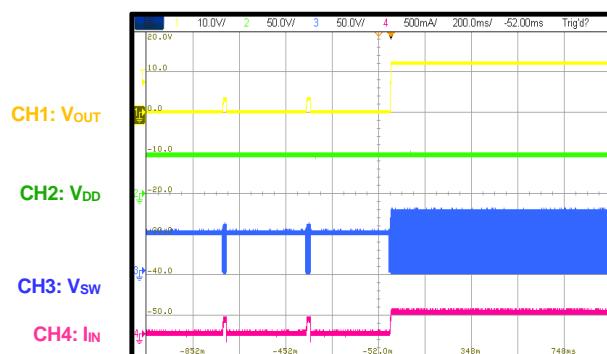
### OCP Recovery

$I_{OUT}$  = overload to 0A



### OCP Recovery

$I_{OUT}$  = overload to 1A



## FUNCTIONAL BLOCK DIAGRAM

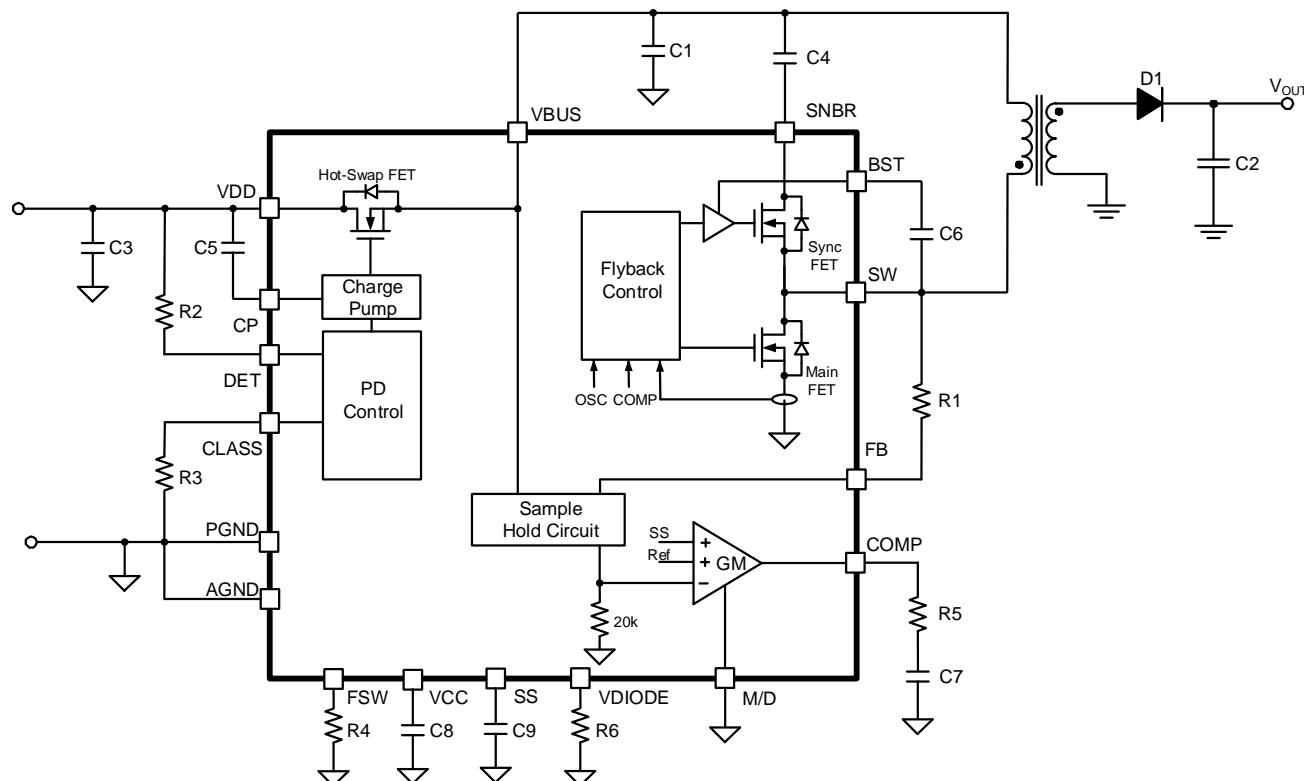


Figure 1: Functional Block Diagram

## OPERATION

The MP8017 is an integrated, IEEE 802.3af-compliant, Power over Ethernet (PoE) powered device (PD) with a PD interface and flyback power converter. The power converter can be set to active-clamp primary-side regulation (PSR) flyback mode and active-clamp secondary-side regulation (SSR) flyback mode. It is targeted for small-sized, 13W, isolated PoE applications. The PD can also respond to IEEE802.3at power-sourcing equipment (PSE) at a class 4 level. Figure 1 on page 17 shows the internal block diagram.

### Detection (DET)

The DET pin supports PoE detection. In detection mode, a resistor connected between DET and VDD presents as a load to the PSE. To determine the load resistance, the PSE applies two safe voltages (between 2.7V and 10.1V) while measuring the change in how much current is drawn. A 24.9k $\Omega$  resistor between VDD and DET is recommended to present a correct signature, and the valid signature resistance from the power interface (PI) is between 23.7k $\Omega$  and 26.3k $\Omega$ .

DET controls the MP8017's enable function, except for detection. By pulling DET low, the MP8017 disables classification, the input MOSFET, and flyback switching. This function can disable the flyback converter when adapter power is available on an output terminal.

### Classification

Classification mode specifies to the PSE the expected load range of the device under power (e.g. the MP8017). This allows the PSE to intelligently distribute power to as many loads as possible within its maximum current capability. IEEE802.3af classification mode is active between 14.5V and 20.5V. The MP8017 presents a current in classification mode (see Table 1).

Table 1: CLASS Resistor Selection

Class	Max. Power to PD (W)	Classification Current (mA)	R <sub>CLASS</sub> ( $\Omega$ )
0	12.95	2	578
1	3.84	10.55	110
2	6.49	18.7	62
3	12.95	28.15	41.2
4	25.5	40.4	28.7

### PD Under-Voltage Lockout (UVLO) and Current Limiting

When the PD is powered by the PSE and V<sub>DD</sub> exceeds the turn-on threshold, the input MOSFET starts to pass a limited current (I<sub>INRUSH</sub>) to charge the bulk capacitor on V<sub>BUS</sub>.

The inrush current limit function works until the working current drops below 80% of the inrush current limit. Then the current limit changes to the normal operation current limit threshold.

After a delay (t<sub>DELAY</sub>) from when under-voltage lockout (UVLO) begins, the MP8017 asserts an internal enable (EN) signal. After the inrush period, the MP8017 goes from start-up mode to running mode. The internal EN signal can enable the flyback converter internally (see Figure 2).

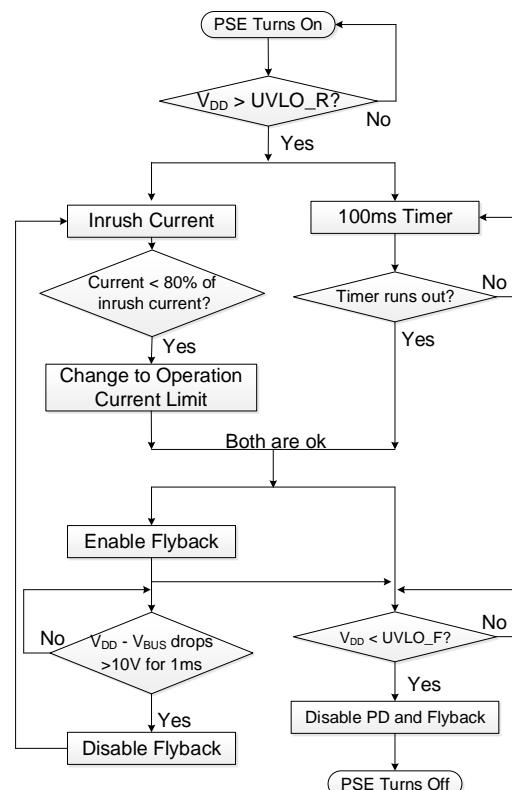


Figure 2: Start-Up Sequence

If V<sub>DD</sub> drops below its falling UVLO threshold, the input MOSFET and DC/DC converter are both disabled.

If the output current (I<sub>OUT</sub>) overloads on the input MOSFET, the current limit works and V<sub>BUS</sub> drops.

If  $V_{DD} - V_{BUS}$  drops by more than  $V_{BUS-FOLD}$  for longer than  $t_{BUS-FOLD}$ , or  $V_{BUS}$  drops to 15V, the current limit reverts to the inrush limit value. Meanwhile, the internal EN pulls down to disable DC/DC switching. Then the device operates in a new inrush cycle; in this scenario, the internal EN signal does not have a delay.

Figure 2 on page 18 shows the sequences for the current limit and internal EN signal during start-up from the PSE's power supply.

### **VBUS Over-Voltage (OV) Clamp**

In addition to the current limit function, the PD input MOSFET can also protect VBUS from the surge voltage from VDD. If  $V_{BUS}$  exceeds  $V_{BUS-CLAMP}$ , the input MOSFET is regulated to keep  $V_{BUS}$  at  $V_{BUS-CLAMP}$ .

### **DC/DC Converter Start-Up and Power Supply**

The MP8017's DC/DC converter has an internal start-up circuit. When  $V_{BUS}$  exceeds its UVLO rising threshold, the capacitor at VCC is charged through the internal LDO. Typically, VCC is regulated at 5.5V. VCC has a UVLO rising threshold, and the internal reference circuit is enabled once VCC is ready.

The DC/DC converter starts switching and regulates the isolated output when the following conditions are met:

- Both  $V_{BUS}$  and  $V_{CC}$  are high
- The SNBR voltage is almost equal to  $V_{BUS}$
- The internal EN signal from the PD is ready

### **Flyback Working Mode Detection**

The MP8017 supports active-clamp flyback control in both PSR mode and SSR mode. See Table 2 on page 21 and the Frequency Dither Function section on page 20 for more details.

After start-up, the MP8017's work mode is latched and cannot change until the flyback converter is disabled by VCC UVLO.

In PSR mode, the  $V_{OUT}$  feedback signal is detected from the SW voltage through the FB pin without an optocoupler or auxiliary winding. In SSR mode, the  $V_{OUT}$  feedback signal is directly detected through the COMP pin by an external diode (TL431) and optocoupler. In both modes, the frequency is constant and does not run in sleep mode under light-load conditions,

which can prevent audible noise issues from the transformer.

### **Pulse-Width Modulation (PWM) Operation**

The MP8017 integrates two MOSFETs for the active-clamp flyback design.

At the beginning of each cycle, the low-side MOSFET (LS-FET) turns on, forcing the current in the transformer to increase. The current through the LS-FET is sensed. When the sum of the current signal and the slope compensation signal rises above the voltage set by the COMP pin, the LS-FET turns off. The transformer current then transmits energy from primary-side winding to secondary-side winding, and the transformer charges the output capacitor through the Schottky diode.

At the same time, the high-side MOSFET (HS-FET) turns on after LS-FET turns off, which provides a clamp loop for the energy in the transformer leakage inductance. While the HS-FET is on, the energy in the transformer leakage inductance can be absorbed by the snubber capacitor on the SNBR pin. The capacitor energy can be discharged back to the output through the transformer within the same cycle, which balances the snubber capacitor's voltage in each cycle.

The transformer's primary-side current is controlled by the COMP voltage, which itself is controlled by the feedback output voltage. This means that  $V_{OUT}$  controls the transformer current to satisfy the load.

It is recommended to place a 4.7 $\mu$ F capacitor on SNBR to clamp the transformer leakage inductance energy; otherwise, the SW and SNBR voltages may become too high.

If the MP8017 stops switching due to ULVO or a protection, both the HS-FET and LS-FET stay off. There is a zero-current detection (ZCD) circuit on both the HS-FET and LS-FET to ensure that they turn off when the current is low.

### **Voltage Control**

#### **Primary-Side Regulation (PSR) Mode**

Unlike a traditional flyback with opto-isolator feedback, the MP8017 can detect the transformer's primary winding voltage ( $V_{SW} - V_{BUS}$ ) from the FB pin during the secondary-side's output diode conduction period.

Assume that the secondary winding is the master, and the primary winding is the slave. When the secondary-side diode conducts, the primary winding voltage can be calculated with Equation (1):

$$V_{\text{PRI}} = \frac{N_p \times (V_{\text{OUT}} + V_{\text{DOF}})}{N_s} \quad (1)$$

Where  $V_{\text{DOF}}$  is the output diode's forward-drop voltage,  $V_{\text{OUT}}$  is the output voltage,  $V_{\text{PRI}}$  is transformer's primary winding voltage, and  $N_p$  and  $N_s$  are the turns of the primary winding and output winding, respectively.

The MP8017 senses the primary-side winding voltage through the FB pin, which generates a feedback current ( $I_{\text{FB}}$ ) through the resistor.  $I_{\text{FB}}$  can be estimated with Equation (2):

$$I_{\text{FB}} = \frac{V_{\text{PRI}}}{R_{\text{FB}}} \quad (2)$$

Where  $I_{\text{FB}}$  is the feedback current (100 $\mu$ A), and  $R_{\text{FB}}$  is the resistor from SW pin to FB pin.

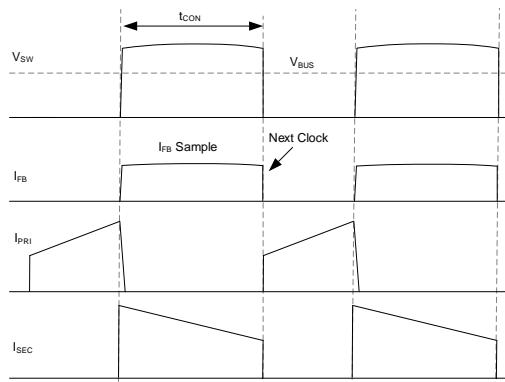


Figure 3: FB Feedback Control

The MP8017 samples the primary-side winding voltage after the LS-FET turns off. A blanking time is added so that SW's rising edge is not affected. To guarantee a sufficiently long FB sampling period, the MP8017 has a minimum LS-FET off time, which also limits the maximum duty cycle ( $D_{\text{MAX}}$ ) when the frequency is high.

During the FB sensing period, the FB signal is sent into the EA's negative input. This value is held after the sensing time window elapses.

### Secondary-Side Regulation (SSR) Mode

The MP8017 can also be set to SSR flyback mode. In SSR mode, the  $V_{\text{OUT}}$  signal is fed back to the COMP pin through one optocoupler and TL431, the FB to COMP error amplifier is disabled, and the FB pin is only used for overvoltage protection (OVP).

### Output Voltage ( $V_{\text{OUT}}$ ) Compensation

In PSR mode, the primary-side winding waveform reflects the secondary-side winding voltage with the transformer turns ratio, but  $V_{\text{OUT}}$  differs from output winding voltage due to output diode voltage drop, as well as the power winding resistance. The dropout voltage varies when the conducted current changes. The MP8017 has a VDIODE pin, which can be used to compensate for the dropout voltage across current variations.

The MP8017 senses the LS-FET current when it is on, and then holds the current signal when the LS-FET is off. By filtering the current signal, the MP8017 controls FB's sink current on the sensed LS-FET current in each cycle. A different resistor on the VDIODE pin sets the sink current ( $I_{\text{FBCOMP}}$ ) from the FB pin, calculated with Equation (3):

$$I_{\text{FBCOMP}} = \frac{I_{\text{IN}} \times (1-n)}{D \times R_{\text{VDIODE}}} \quad (3)$$

Where  $I_{\text{FBCOMP}}$  is the expected compensation current,  $D$  is the duty cycle,  $n$  is the current ripple ratio,  $I_{\text{IN}}$  is the input current, and  $R_{\text{VDIODE}}$  is the VDIODE resistor.

FB's sink current leads to a voltage drop on the feedback resistor between the SW and FB pins, which compensates for  $V_{\text{OUT}}$  when the load varies.

In SSR flyback mode, this voltage compensation function is disabled.

### Frequency Dither Function

The MP8017 supports frequency dithering by setting the M/D pin. During start-up, the MP8017 outputs a current ( $I_{\text{M/D}}$ ) current to M/D pin to detect the resistor setting after  $V_{\text{CC}}$  is ready (see Table 2 on page 21).

**Table 2: M/D Pin Configuration Options**

M/D Resistance (kΩ)			MODE	Dither Function?
Min	Typ (1%)	Max		
0	0	0.68	PSR	Yes
6.2	6.8	7.5	PSR	No
13.7	15	15.4	SSR	No
24.9	Float	Float	SSR	Yes

The M/D pin's detection current lasts for a certain time ( $t_{M/D}$ ). Typically, it is sufficient to connect one resistor from the M/D pin to AGND. In noisy environments, a capacitor can be connected from the M/D pin to AGND to provide filtering. The capacitance should be below 100pF so that the M/D pin voltage can rise to a steady state before MP8017 detects this voltage.

Frequency dithering is fixed at  $\pm 6\%$  of the switching frequency ( $f_{sw}$ ), and the modulation frequency is about 9kHz.

### Overload Protection (OLP)

The MP8017 senses the LS-FET current during each switching cycle. If the LS-FET current exceeds the current-limit threshold, the MP8017 turns off the LS-FET for that cycle. The LS-FET does not turn on again until the internal oscillator starts the next cycle, and then the current is sensed again. The MP8017 has cycle-by-cycle over current protection (OCP).

If the load continues increasing after triggering OCP,  $V_{OUT}$  drops and the peak current triggers the switching limit every cycle. The MP8017 sets overload protection (OLP) by continuing to monitor the LS-FET current.

Once the SS voltage ( $V_{SS}$ ) is charged to 3.5V after soft start is complete, OLP is enabled. If an OCP signal is detected, the SS charging current is disabled. Then the OC discharge source is enabled, and  $V_{SS}$  drops with the rate of a 20 $\mu$ A current. At the same time, the 50 $\mu$ s one-shot timer is activated, and it remains active for 50 $\mu$ s after the OCP condition is removed. The 20 $\mu$ A discharge source cannot turn off until the one-shot timer becomes inactive.

If the OC condition disappears before the 50 $\mu$ s time elapses, and before the SS capacitor discharges to 3V, the MP8017 returns to normal operation, and the SS capacitor charges to 3.5V with a rate of 50 $\mu$ A.

If the SS capacitor discharges to 3V, the MP8017 detects an overload condition and turns off the switching MOSFETs until the next restart cycle. At the same time, the 20 $\mu$ A discharge current is disabled and the 2 $\mu$ A overload discharge source is enabled. After  $V_{SS}$  discharges to 0.2V, the MP8017 restarts with a new soft-start cycle. This is called hiccup mode protection.

The OLP detection function is disabled when  $V_{SS}$  drops below 3V; it is enabled when  $V_{SS}$  rises to 3.5V. This means that OLP only occurs after soft start completes.

### Short-Circuit Protection (SCP)

When the output is shorted to the ground, the part works in OCP mode and the current is limited cycle by cycle; in this scenario, OLP may be triggered. However, if the peak current cannot be limited by the cycle-by-cycle limit due to the minimum on time, the current may become too high, and the transformer may become saturated. If the monitored LS-FET current reaches the SCP threshold, the MP8017 turns off the switching FETs and runs into hiccup mode immediately by discharging the SS capacitor with a 2 $\mu$ A current. The MP8017 restarts once  $V_{SS}$  discharges to 0.2V.

If the LS-FET current does not reach the SCP threshold during SCP, but the HS-FET's negative current exceeds the negative current limit, the MP8017 initiates hiccup mode and discharges the SS capacitor with a 2 $\mu$ A current until  $V_{SS}$  reaches 0.2V.

### Over-Voltage Protection (OVP)

The MP8017 includes FB pin over-voltage protection (OVP) in both PSR and SSR mode. If the feedback current on the FB pin exceeds 125% of  $I_{REF}$ , the MP8017 stops switching, and it enters hiccup mode immediately by discharging the SS capacitor with a 2 $\mu$ A current. The MP8017 restarts once  $V_{SS}$  discharges to 0.2V

To avoid a mistriggering due to the oscillation of the leakage inductance and the parasitic capacitance, the OVP sampling has a blanking time ( $t_{ovps}$ ).

The MP8017 also monitors the SNBR pin for maximum OVP. If the SNBR voltage exceeds 105V, the MP8017 stops all switching and enters hiccup mode.

### Soft Start (SS)

The MP8017 provides soft start by charging the SS pin's capacitor with a current source. During soft start, the SS signal ramps up slowly. The SS capacitor discharges completely in the event of a commanded shutdown, thermal shutdown, or a protection condition.

In PSR mode, the SS signal clamps the internal FB voltage until it reaches the reference voltage. In SSR mode, the SS signal clamps the COMP voltage until it reaches the level set by the switching current. The SS time is controlled by the SS capacitor.

During SS,  $f_{sw}$  folds back when  $V_{ss}$  is low. See the Switching Frequency section below for more details.

Figure 4 shows the hiccup protection logic.

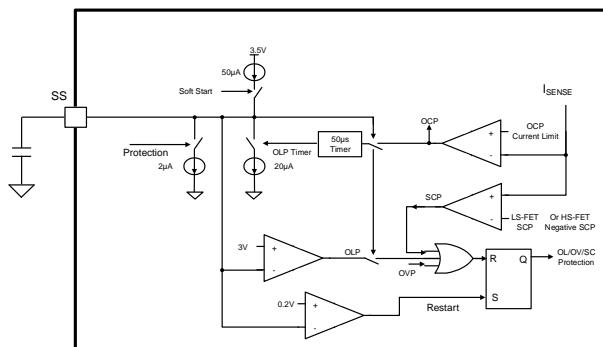


Figure 4: Hiccup Protection Logic

### Switching Frequency ( $f_{sw}$ )

The MP8017's oscillating frequency is set by an external resistor connected from the FSW pin to AGND. The value of resistor can be estimated with Equation (4):

$$R_{sw} = \frac{4650}{f_{sw}} \quad (4)$$

Where  $R_{sw}$  is the frequency setting resistor, and  $f_{sw}$  is the switching frequency.

The MP8017 works with this frequency across the full load range, and this frequency does not

drop, even if the circuit operates with no load. Typically, the MP8017 is set to be between 80kHz and 650kHz in application.

The MP8017 has a frequency foldback function during soft start that prevents transformer saturation when the MP8017 triggers the LS-FET's switching minimum on time. When  $V_{ss} < 0.2V$ , the foldback frequency exceeds either 80KHz or 1/4 of  $f_{sw}$ . And it ramps up slowly to normal frequency with SS voltage's rising. After SS finishes, the function is disabled.

### BST Power Supply

The MP8017 integrates both an LS-FET and HS-FET for an active-clamp topology. The HS-FET is supplied by the BST pin while the HS-FET turns on. During start-up, the BST pin is charged by the internal charge pump from the CP pin. During steady state switching mode, the BST capacitor can be charged up by  $V_{cc}$  when the LS-FET turns on.

### Minimum on Time ( $t_{min-on}$ ) and Minimum off Time ( $t_{min-off}$ )

The transformer's parasitic capacitance induces a current spike on the LS-FET when the LS-FET turns on. The MP8017 includes a leading edge blanking period to avoid falsely terminating the switching pulse. During this blanking period, the current-sense comparator is disabled, and the switching power FET cannot switch off.

The MP8017 also limits the minimum off time to ensure optimal function for the primary-side's feedback loop.

### Over-Temperature Protection (OTP)

Thermal shutdown is implemented to prevent the chip from thermal runaway. When the silicon die temperature exceeds its upper threshold, the die shuts down the whole chip, including the PD section and flyback section.

When the temperature drops below its lower threshold, the OTP cool down timer runs out, and SNBR is discharged to be almost equal to  $V_{bus}$ , the chip is enabled again with a new start-up cycle.

## APPLICATION INFORMATION

### Selecting the Detection Resistor

In detection mode, a resistor must be connected between the DET and VDD pins to act as a load for the PSE. The resistance is calculated as a  $\Delta V/\Delta I$ , with an acceptable resistance between 23.7k $\Omega$  and 26.3k $\Omega$ . Typically, use a 24.9k $\Omega$  detection resistor.

### Selecting the Classification Resistor

For the PSE to distribute power to as many loads as possible, there is a resistor between the CLASS and AGND pins. This resistor classifies the PD power level, which draws a fixed current set by the classification resistor. The power supplied to PD is set by the classification resistor (see Table 1 on page 18). The typical voltage on the CLASS pin is low, so this voltage leads to a small amount of power loss on the class resistor, even within the class 4 range.

### Selecting the Protection TVS Diode

To limit the input transient voltage within the absolute maximum ratings, a transient voltage suppression (TVS) diode must be placed across the input voltage (VDD to PGND). A SMAJ58A (or equivalent) diode is recommended for general indoor applications. Outdoor transient levels or special applications require additional protection.

### Selecting the PD Input Capacitor

A 0.05 $\mu$ F to 0.12 $\mu$ F input bypass capacitor should be placed from VDD to PGND for the IEEE 802.3af standard specification. Typically, a 0.1 $\mu$ F, 100V ceramic capacitor is used.

### Output Voltage ( $V_{OUT}$ ) Setting

The MP8017 has two feedback modes: PSR mode and SSR mode.

In PSR mode, the MP8017 senses the primary-side winding voltage through FB pin, and  $V_{OUT}$  can be calculated with Equation (5):

$$V_{OUT} = \frac{I_{FB} \times R_{FB}}{N_p} \times N_s - V_{DOF} \quad (5)$$

Where  $V_{OUT}$  is the output voltage,  $R_{FB}$  is the SW to FB resistance,  $I_{FB}$  is the feedback current (100 $\mu$ A),  $V_{DOF}$  is the output diode's forward-drop voltage, and  $N_p$  and  $N_s$  are the turns of the primary winding and output winding,

respectively.

In SSR mode,  $V_{OUT}$  is set by an external reference voltage regulator (TL431). If the TL431's reference voltage is 2.5V, and the expected  $V_{OUT}$  is 12V, the upper and lower divider's resistor ratio is 3.8. Then TL431 generates an amplified signal and controls the MP8017's COMP pin through an optocoupler (e.g. PC357). COMP controls the current, and  $V_{OUT}$  is regulated based on the feedback signal.

### FB Maximum Sink/Source Current Setting

The FB resistor is connected between the FB pin and SW pin to regulate  $V_{OUT}$ . The FB voltage is almost equal to  $V_{BUS}$  during switching.

While the primary MOSFET turns off, the SW voltage exceeds the FB voltage, so current flows into FB. During normal operation, the MP8017 regulates the sink current at 100 $\mu$ A; during OVP, the FB maximum sink current is typically 125 $\mu$ A.

While the primary MOSFET turns on, the SW voltage is 0V, so current flows out of the FB pin. FB's maximum output current should be limited below 1mA by the FB resistance.

### Work Mode/Frequency Dithering Setting

Once the MP8017 is enabled, the M/D pin's current ( $I_{M/D}$ ) detects the M/D resistance. See Table 2 on page 21 for more details.

### Selecting the Transformer

A transformer is critical for a flyback converter since it determines the duty cycle, peak current, efficiency, MOSFET, and output diode rating.

The transformer winding ratio determines the duty cycle. Estimate the duty cycle with Equation (6):

$$D = \frac{N \times V_{OUT}}{N \times V_{OUT} + V_{IN}} \quad (6)$$

Where  $V_{IN}$  is the input voltage, D is the duty cycle, and N is the transformer primary winding to output winding ratio.

For the MP8017, it is recommended to select a 2:1 ratio for a 12V output, as this matches the SW voltage rating.

The primary-side inductance affects the input current ripple's ratio factor. A high inductance results in a larger transformer size and higher cost; a low inductance results in a high switching peak current and RMS current, which reduces efficiency. Choose a primary-side inductance to make the current ripple ratio factor to be about 30% to 50%.

$L_P$  is the primary inductance. Calculate  $L_P$  based on the minimum input voltage condition and  $f_{SW}$ , as calculated with Equation (7):

$$L_P = \frac{V_{IN} \times D^2}{2 \times n \times I_{IN} \times f_{SW}} \quad (7)$$

Where  $n$  is the current ripple ratio, and  $I_{IN}$  is the input current.

The transformer should have a high saturation current to support the switching peak current; otherwise, the transformer inductance may sharply decrease.

The current rating counts the maximum RMS current, which allows current to flow through each winding. The current density should be controlled; otherwise, it can cause a high resistive power loss.

#### Output Voltage ( $V_{OUT}$ ) Compensation Setting

The MP8017 senses the LS-FET current when the LS-FET is on, and controls a sink current from the FB pin based on the sensed LS-FET current in each cycle. Different resistors on the VDIODE pin set FB's sink current (see the Output Voltage ( $V_{OUT}$ ) Compensation section on page 20 for more details).

The  $V_{OUT}$  compensation function is only enabled in PSR mode.

#### Selecting the Output Diode

The flyback output rectifier diode supplies current to the output capacitor when the primary-side MOSFET is off. Use a Schottky diode to reduce losses from the diode's forward voltage and recovery time. The diode should be rated for a reverse voltage 1.5 times greater than  $V_{DIODE}$ , which can be estimated with Equation (8):

$$V_{DIODE} = \frac{V_{IN}}{N} + V_{OUT} \quad (8)$$

Where  $V_{DIODE}$  is the output diode's reverse voltage.

The average current rating must exceed the maximum expected load current, and the peak current rating must exceed the output winding peak current.

It is recommended to use an RC snubber circuit for the output diode

#### Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor while limiting noise at the input source. A low-ESR capacitor is required to minimize the noise to the IC. Ceramic capacitors are recommended, but tantalum or low-ESR electrolytic capacitors may be sufficient. For ceramic capacitors, the capacitance dominates the input voltage ripple at the switching frequency. The input voltage ripple can be calculated with Equation (9):

$$\Delta V_{IN} = I_{IN} \times \frac{V_{IN}}{f_{SW} \times C_{IN} \times (N \times V_{OUT} + V_{IN})} \quad (9)$$

Where  $\Delta V_{IN}$  is the input voltage ripple, and  $C_{IN}$  is the input capacitor.

#### Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. For the best results, use ceramic capacitors or low-ESR capacitors to minimize the output voltage ripple. For ceramic capacitors, the capacitance dominates the output ripple at the switching frequency. The output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{N \times V_{OUT}}{(V_{IN} + N \times V_{OUT}) \times f_{SW}} \times \frac{I_{OUT}}{C_{OUT}} \quad (10)$$

Where  $\Delta V_{OUT}$  is the output voltage ripple,  $C_{OUT}$  is the output capacitor, and  $I_{OUT}$  is the output current.

#### Design Example

Table 3 shows a PSR topology flyback design example following specific application guidelines.

Table 3: PSR Flyback Design Example

$V_{IN}$	37V to 57V
$V_{OUT}$	12V
$I_{OUT}$	1A

Figure 6 on page 26 shows the detailed application schematic. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section starting on page 13. For more device applications, refer to the related evaluation board datasheet.

### PCB Layout Guidelines

Efficient layout of the PoE front-end and high-frequency switching power supply is critical for stable operation. A poor layout may result in reduced performance, excessive EMI, resistive loss, and system instability. For the best results, refer Figure 5 and follow the guidelines below:

1. Keep the input switching loop between the flyback input capacitor, transformer, SW pin, and PGND as short as possible.
2. Keep the output loop between the rectifier diode, output capacitor, and transformer as short as possible.
3. Keep the active clamp loop between the active clamp capacitor, transformer, SW pin, and SNBR pin as short as possible.
4. Keep the input hot-swap loop between the PD input capacitor, VDD pin, VBUS pin, and VBUS capacitor as short as possible.
5. Place the VCC capacitor close to the VCC pin for optimal decoupling.

6. Ensure that the feedback trace is short and routed far away from noisy sources, such as SW.
7. Keep other signal leads (e.g. DET, CLASS, COMP, VDIODE, SS, and FSW) as short as possible.
8. Shorten the CP loop and BST loop for excellent hot-swap and HS-FET driver function.
9. Use a single-point connection between power GND and signal GND.
10. Place copper and vias under the MP8017 package for excellent thermal sinking.

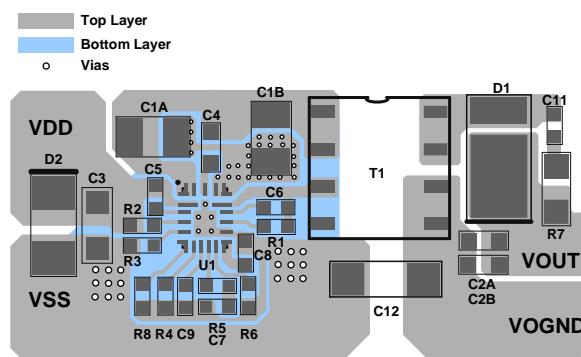


Figure 5: Recommended PCB Layout

Figure 5 refers to Figure 6 on page 26. For more information, refer to the related evaluation board datasheet.

## TYPICAL APPLICATION CIRCUITS

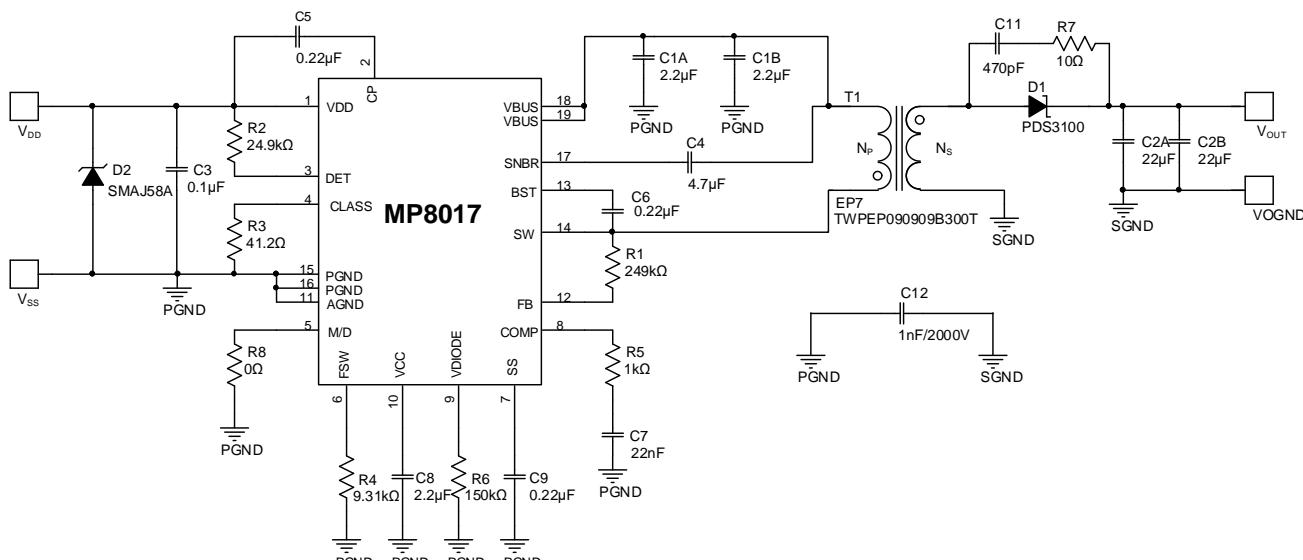


Figure 6: Typical Application Circuit for Active-Clamp PSR Flyback ( $V_{DD}$  = 37V to 57V,  $V_{OUT}$  = 12V at 12W)

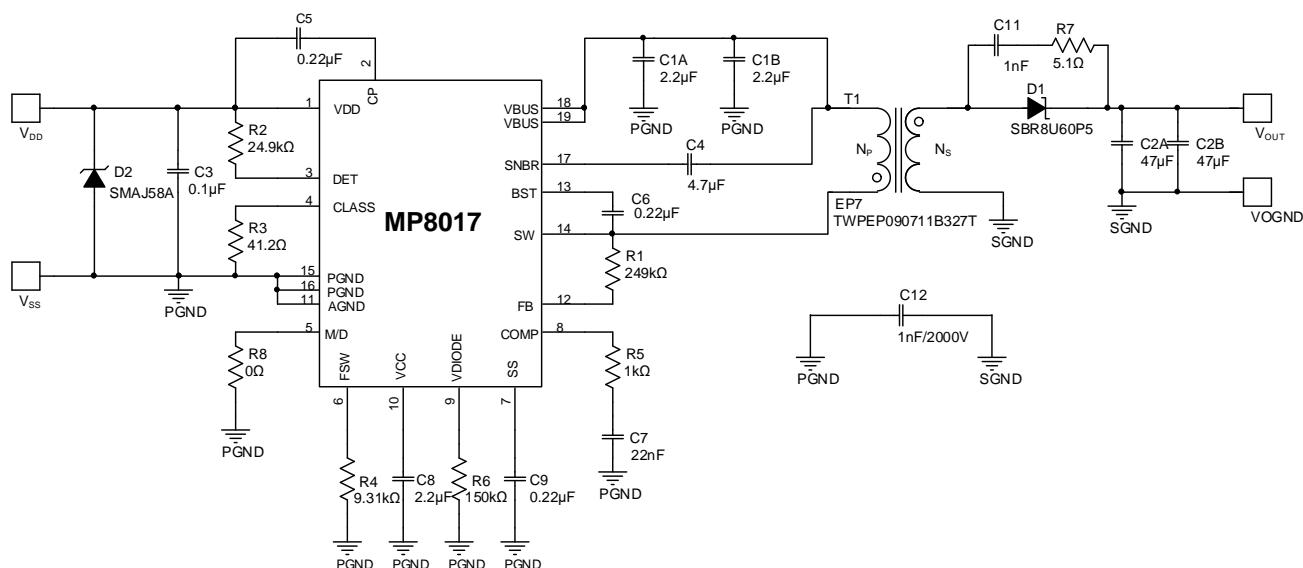


Figure 7: Typical Application Circuit for Active-Clamp PSR Flyback ( $V_{DD}$  = 37V to 57V,  $V_{OUT}$  = 5V at 12W)

## TYPICAL APPLICATION CIRCUITS (continued)

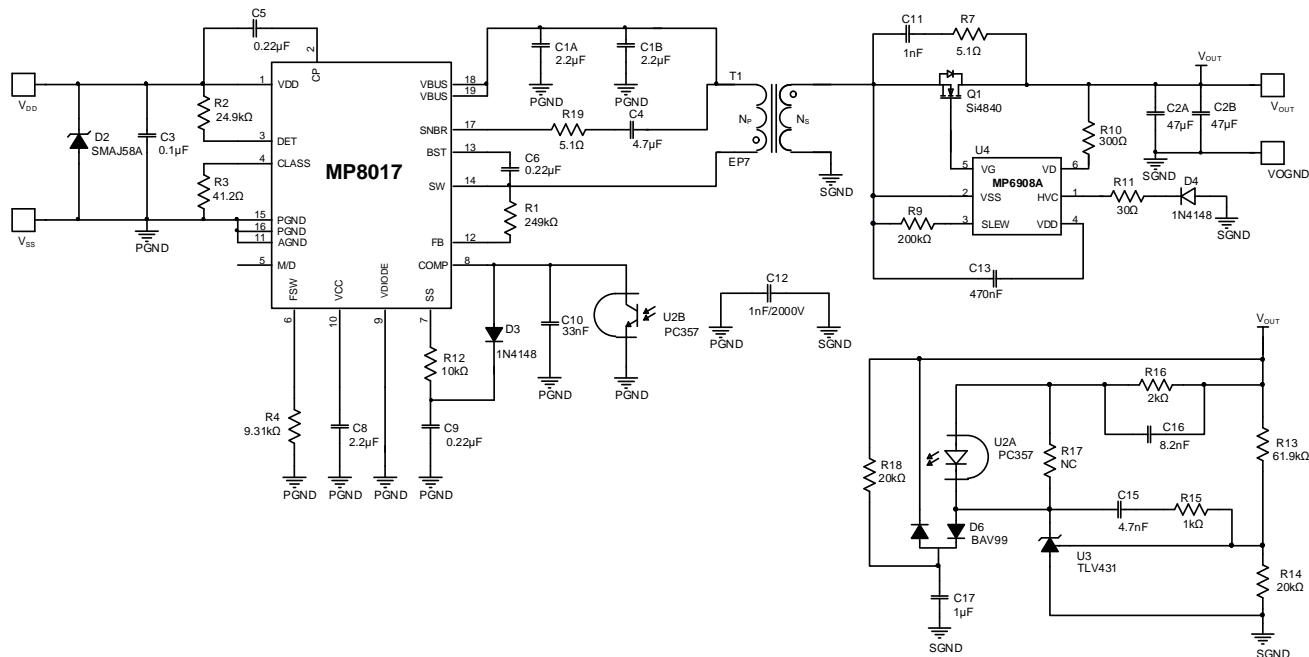
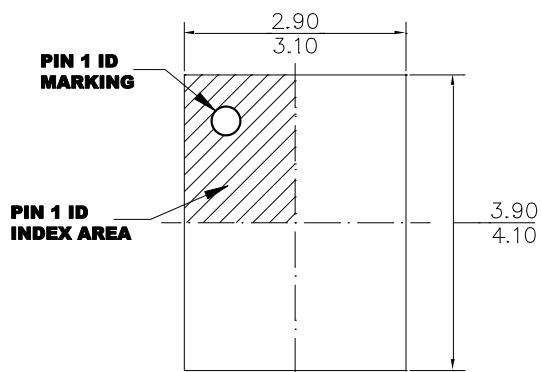


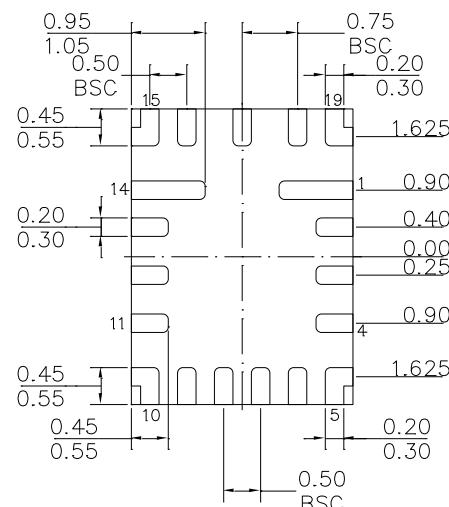
Figure 8: Typical Application Circuit for Active Clamp and MP6908A SYNC SSR Flyback ( $V_{DD} = 37V$  to  $57V$ ,  $V_{OUT} = 5V$  at  $12W$ )

## PACKAGE INFORMATION

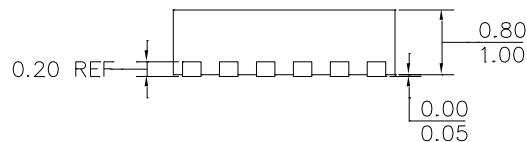
### QFN-19 (3mmx4mm)



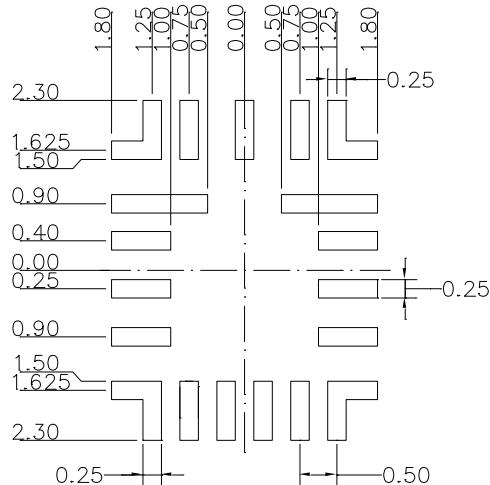
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**

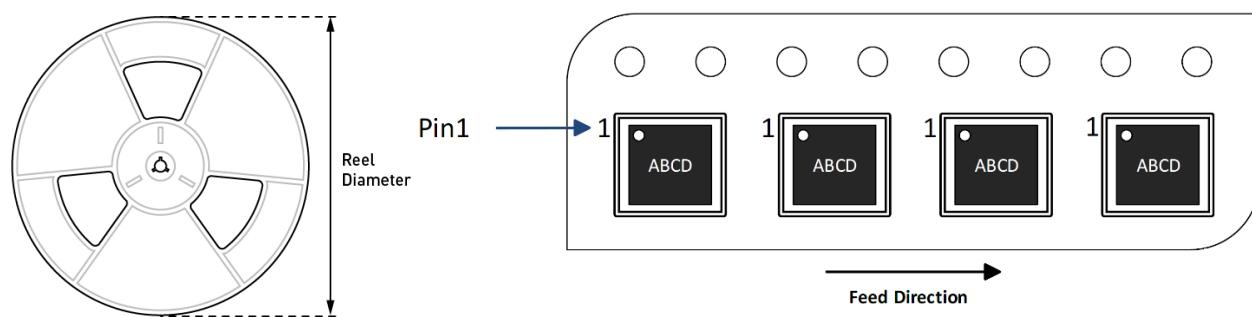


**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-220.
- 4) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Quantity/Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8017GL-Z	QFN-19 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/21/2023	Initial Release	-

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