25CSM01

1-Mbit SPI Serial EEPROM with 128-Bit Serial Number and Enhanced Write Protection

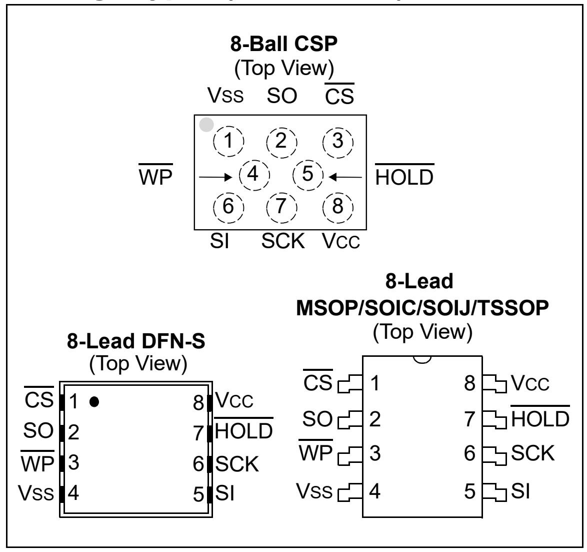
Features

- 1-Mbit Serial EEPROM:
  - 131,072 x 8 organization
  - Page size of 256 bytes
  - Byte or sequential reads
  - Byte or page writes
  - Self-timed write cycle (4 ms maximum)
- Security Register:
  - Preprogrammed 128-bit serial number
  - User-programmable, lockable 256-byte ID page
- Built-in Error Correction Code (ECC) Logic:
  - ECC Status bit via the STATUS register
- JEDEC® SPI Manufacturer Read ID Support
- High-Speed Clock Frequency:
  - 20 MHz at $V_{CC} \geq 4.5V$
  - 10 MHz at $V_{CC} \geq 2.5V$
  - 5 MHz at $V_{CC} \geq 1.7V$
- Legacy Write Protection Mode:
  - Block protection functionality (quarter, half or entire memory array)
- Enhanced Write Protection Mode:
  - User-definable memory partitions
  - Each partition can be set independently and have unique protection behavior
- Low-Power CMOS Technology:
  - Voltage range: 1.7V to 5.5V
  - Write current: 3.0 mA at 5.5V
  - Read current: 3.0 mA at 4.5V, 10 MHz
  - Standby current: 2.0 µA at 2.5V
- High Reliability:
  - More than one million erase/write cycles
  - Built-in ECC logic for increased reliability
  - Data retention: > 200 years
  - ESD protection: > 4000V
- Available Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C

Packages

- 8-Ball CSP, 8-Lead DFN, 8-Lead MSOP, 8-Lead SOIC, 8-Lead SOIJ, and 8-Lead TSSOP

Package Types (not to scale)



Pin Function Table

Name	Function
$\overline{\text{CS}}$	Chip Select Input
SO	Serial Data Output
$\overline{\text{WP}}$	Write-Protect Pin
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{\text{HOLD}}$	Hold Input
V_{CC}	Supply Voltage

General Description

The Microchip Technology Inc. 25CSM01 provides 1-Mbit of Serial EEPROM utilizing the Serial Peripheral Interface (SPI) compatible bus. The device is organized as 131,072 bytes of 8 bits each (128 Kbytes) and is optimized for use in consumer and industrial applications where reliable and dependable nonvolatile memory storage is essential. The 25CSM01 is capable of operation across a broad voltage range (1.7V to 5.5V).

The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{CS}$) input. Communication to the device can be paused via the $\overline{HOLD}$ pin. While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

The 25CSM01 features a nonvolatile Security register independent of the 1 Mbit main memory array. The first half of the Security register is read-only and contains a factory-programmed, globally unique 128-bit serial number in the first 16 bytes. The 128-bit serial number is unique across the entire CS series of Serial EEPROM products and eliminates the time-consuming step of performing and ensuring serialization of a product on a manufacturing line. The 128-bit read-only serial number is followed by an additional 256 bytes of user-programmable EEPROM.

The user-programmable section of the Security register can later be permanently write-protected via a software sequence.

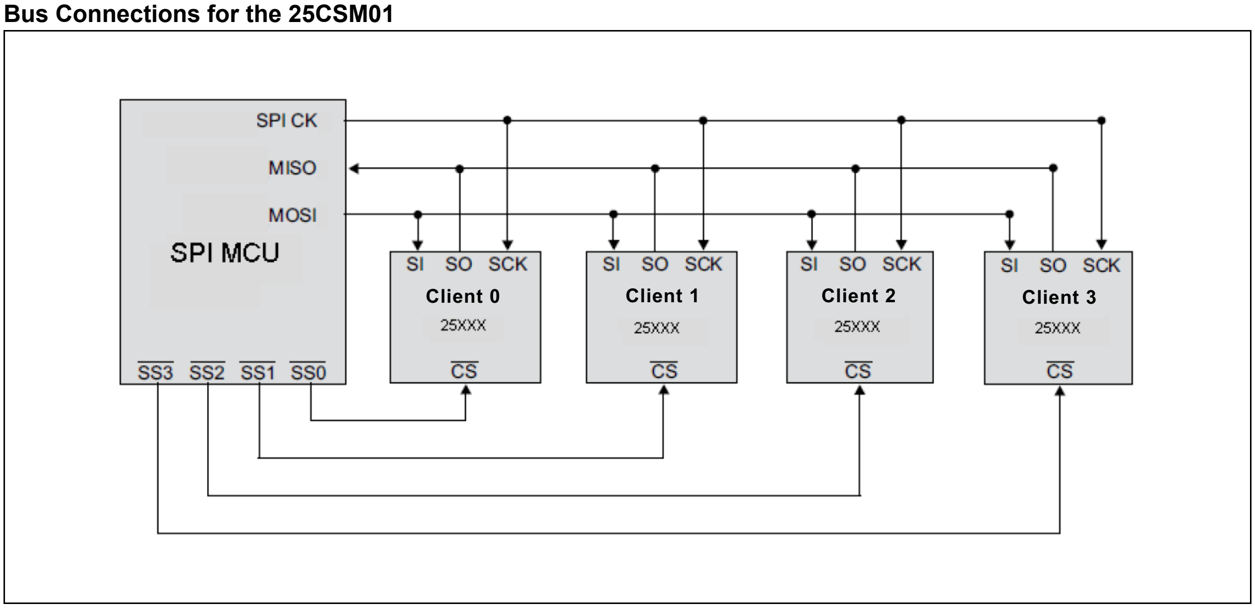
The 25CSM01 features a configurable write protection scheme that allows the user to select Legacy Write Protection mode or Enhanced Write Protection mode. Legacy Write Protection mode enables the Block Protection function via the STATUS register. Enhanced Write Protection mode segments the memory into independent partitions. Each partition can be configured to inhibit writing based on the status of the Memory Partition register setting.

To protect against brown-out events, an undervoltage lockout detection circuit inhibits all write sequences when the VCC supply voltage drops below the set voltage level. The voltage level is configurable via the Undervoltage Lockout Detection (UVLO) register.

For added reliability, the 25CSM01 uses a built-in Error Correction Code (ECC) scheme. This scheme can correct up to one incorrectly read bit within four bytes read out. Additionally, the 25CSM01 includes a flag in the STATUS register to report if any errors were detected and corrected in the most recent memory array read sequence.

The 25CSM01 features an identification register that contains identification information that can be read from the device. This enables the application to electronically query and identify the 25CSM01 while it is in the system. The identification method and the instruction opcode comply with the JEDEC standard for “Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices”. The type of information that can be read from the device includes the JEDEC-defined Manufacturer ID, the vendor-specific Device ID, and the vendor-specific Extended Device Information (EDI).

Bus Connections for the 25CSM01



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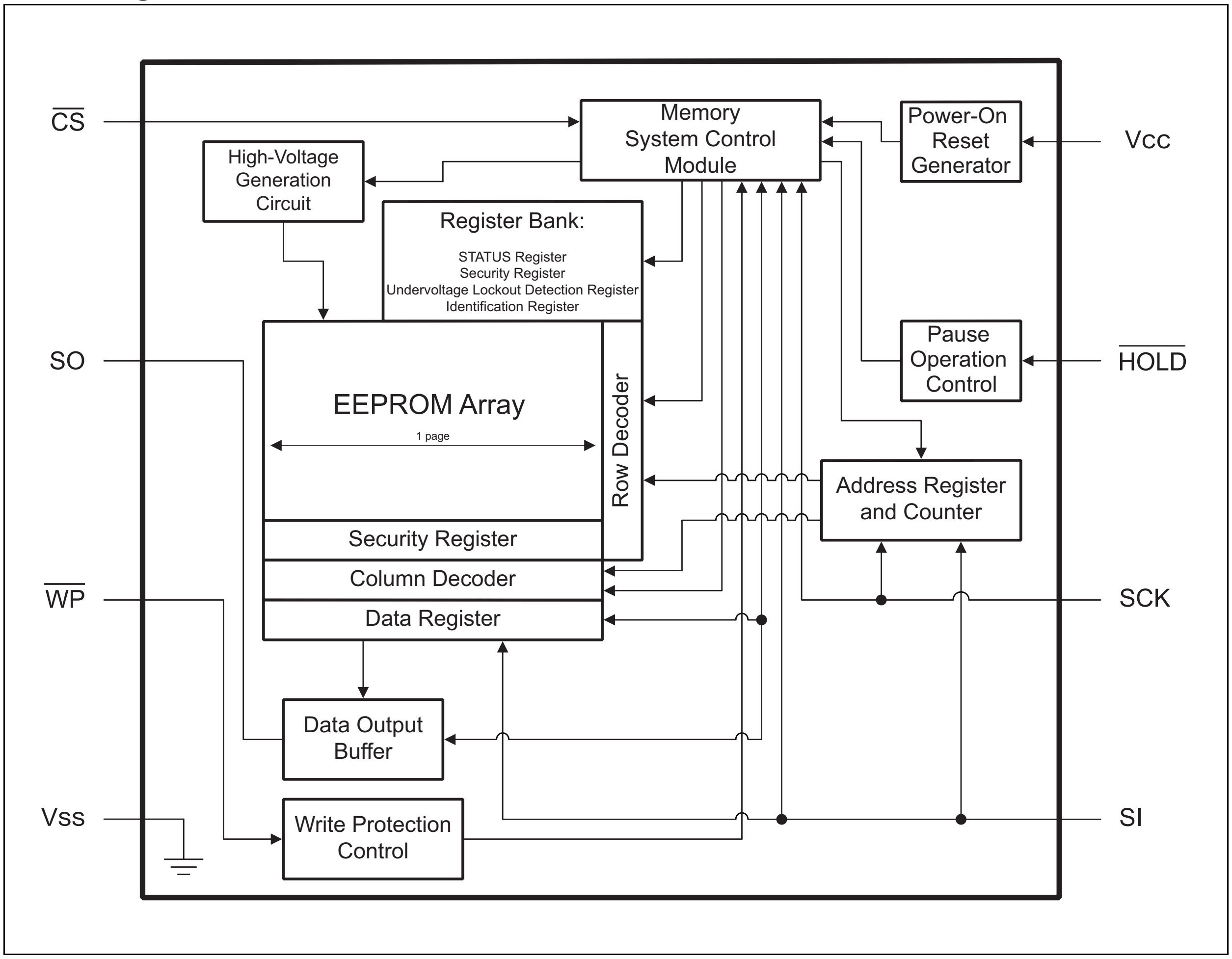
Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

V_{CC} 6.25V

All inputs and outputs w.r.t. V_{SS} .... 0.6V to V_{CC} +1.0V

Storage temperature .... -65°C to +155°C

Ambient temperature under bias .... -40°C to +125°C

ESD protection on all pins .... 4 kV

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics: Industrial (I): T_{AMB} = -40°C to +85°C V_{CC} = 1.7V to 5.5V Extended (E): T_{AMB} = -40°C to +125°C V_{CC} = 1.8V to 5.5V				
Param. No.	Symbol	Characteristic	Min.	Typical	Max.	Units	Test Conditions
D001	V_{IH}	High-Level Input Voltage	V_{CC} x 0.7	—	V_{CC} + 1	V	
D002	V_{IL}	Low-Level Input Voltage	-0.3	—	V_{CC} x 0.3	V	$V_{CC} \geq 2.5V$
D003	V_{OL}	Low-Level Output Voltage	—	—	0.4	V	I_{OL} = 3.0 mA, $V_{CC} \geq 2.5V$
			—	—	0.2	V	I_{OL} = 1.0 mA, V_{CC} < 2.5V
D004	V_{OH}	High-Level Output Voltage	V_{CC} - 0.5	—	—	V	I_{OH} = -100 µA
D005	I_{LI}	Input Leakage Current	—	—	±1.0	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}
D006	I_{LO}	Output Leakage Current	—	—	±1.0	µA	$\overline{CS}$ = V_{CC}, V_{OUT} = V_{SS} or V_{CC}
D007	C_{INT}	Internal Capacitance (all inputs and outputs)	—	—	6.0	pF	T_{AMB} = +25°C, F_{CLK} = 1.0 MHz, V_{CC} = 5.0V (**Note 1**)
D008	I_{CCREAD}	Operating Current	—	—	5.0	mA	V_{CC} = 5.5V, F_{CLK} = 10 MHz, SO = Open
			—	—	3.0	mA	V_{CC} = 4.5V, SCK =10 MHz, SO = Open
			—	—	2.0	mA	V_{CC} = 2.5V, SCK = 5 MHz, SO = Open
D009	$I_{CCWRITE}$	Operating Current	—	—	3.0	mA	V_{CC} = 5.5V
			—	—	2.0	mA	V_{CC} = 2.5V

Note 1: This parameter is not tested but ensured by characterization.

TABLE 1-1: DC CHARACTERISTICS (CONTINUED)

DC CHARACTERISTICS (Continued)			Electrical Characteristics: Industrial (I): TAMB = -40°C to +85°C VCC = 1.7V to 5.5V Extended (E): TAMB = -40°C to +125°C VCC = 1.8V to 5.5V				
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typical**	**Max.**	**Units**	**Test Conditions**
D010	ICCS	Standby Current	—	—	5.0	µA	VCC = 5.5V, $\overline{\text{CS}}$ = VCC, E-Temp. Inputs tied to VCC or VSS
			—	—	3.0	µA	VCC = 2.5V, $\overline{\text{CS}}$ = VCC, E-Temp. Inputs tied to VIN = VCC or VSS
			—	—	2.0	µA	VCC = 5.5V, $\overline{\text{CS}}$ = VCC, I-Temp. Inputs tied to VIN = VCC or VSS
			—	—	1.5	µA	VCC = 2.5V, $\overline{\text{CS}}$ = VCC, I-Temp. Inputs tied to VIN = VCC or VSS
D011	VUVL	Undervoltage Lockout Level (Note 1)	1.7	1.8	1.9	V	VUVL[4:0] = 00011
			1.8	1.9	2.0	V	VUVL[4:0] = 00100
			1.9	2.0	2.1	V	VUVL[4:0] = 00101
			2.0	2.1	2.2	V	VUVL[4:0] = 00110
			2.1	2.2	2.3	V	VUVL[4:0] = 00111
			2.2	2.3	2.4	V	VUVL[4:0] = 01000
			2.3	2.4	2.5	V	VUVL[4:0] = 01001
			2.4	2.5	2.6	V	VUVL[4:0] = 01010
			2.5	2.6	2.7	V	VUVL[4:0] = 01011
			2.5	2.7	2.9	V	VUVL[4:0] = 01100
			2.6	2.8	3.0	V	VUVL[4:0] = 01101
			2.7	2.9	3.1	V	VUVL[4:0] = 01110
			2.8	3.0	3.2	V	VUVL[4:0] = 01111
			2.9	3.1	3.3	V	VUVL[4:0] = 10000
			3.0	3.2	3.4	V	VUVL[4:0] = 10001
			3.1	3.3	3.5	V	VUVL[4:0] = 10010
			3.2	3.4	3.6	V	VUVL[4:0] = 10011
			3.3	3.5	3.7	V	VUVL[4:0] = 10100
			3.4	3.6	3.8	V	VUVL[4:0] = 10101
			3.5	3.7	3.9	V	VUVL[4:0] = 10110
			3.6	3.8	4.0	V	VUVL[4:0] = 10111
			3.7	3.9	4.1	V	VUVL[4:0] = 11000
			3.8	4.0	4.2	V	VUVL[4:0] = 11001
			3.9	4.1	4.3	V	VUVL[4:0] = 11010
			4.0	4.2	4.4	V	VUVL[4:0] = 11011
			4.1	4.3	4.5	V	VUVL[4:0] = 11100
			4.2	4.4	4.6	V	VUVL[4:0] = 11101
			4.3	4.5	4.7	V	VUVL[4:0] = 11110
			4.4	4.6	4.8	V	VUVL[4:0] = 11111

Note 1: This parameter is not tested but ensured by characterization.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): TAMB = -40°C to +85°C VCC = 1.7V to 5.5V Extended (E): TAMB = -40°C to +125°C VCC = 1.8V to 5.5V			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
1	FCLK	Clock Frequency	—	20	MHz	VCC ≥ 4.5V
			—	10	MHz	VCC ≥ 2.5V
			—	5	MHz	VCC ≥ 1.7V
2	TCSS	$\overline{CS}$ Setup Time	15	—	ns	VCC ≥ 4.5V
			30	—	ns	VCC ≥ 2.5V
			60	—	ns	VCC ≥ 1.7V
3	TCSH	$\overline{CS}$ Hold Time	15	—	ns	VCC ≥ 4.5V
			30	—	ns	VCC ≥ 2.5V
			60	—	ns	VCC ≥ 1.7V
4	TCSD	$\overline{CS}$ Disable Time	15		ns	VCC ≥ 4.5V
			30	—	ns	VCC ≥ 1.7V
5	TSU	Data Setup Time	5	—	ns	VCC ≥ 4.5V
			10	—	ns	VCC ≥ 2.5V
			20	—	ns	VCC ≥ 1.7V
6	THD	Data Hold Time	5	—	ns	VCC ≥ 4.5V
			10	—	ns	VCC ≥ 2.5V
			20	—	ns	VCC ≥ 1.7V
7	TR	CLK Rise Time	—	2	µs	**Note 1**
8	TF	CLK Fall Time	—	2	µs	**Note 1**
9	THI	Clock High Time	20	—	ns	VCC ≥ 4.5V
			40	—	ns	VCC ≥ 2.5V
			80	—	ns	VCC ≥ 1.7V
10	TLO	Clock Low Time	20	—	ns	VCC ≥ 4.5V
			40	—	ns	VCC ≥ 2.5V
			80	—	ns	VCC ≥ 1.7V
11	TCLD	Clock Delay Time	50	—	ns	
12	TCLE	Clock Enable Time	50	—	ns	
13	TV	Output Valid from Clock Low	—	20	ns	VCC ≥ 4.5V
			—	40	ns	VCC ≥ 2.5V
			—	80	ns	VCC ≥ 1.7V
14	THO	Output Hold Time	0	—	ns	**Note 1**
15	TDIS	Output Disable Time	—	20	ns	VCC ≥ 4.5V (**Note 1**)
			—	40	ns	VCC ≥ 2.5V (**Note 1**)
			—	80	ns	VCC ≥ 1.7V (**Note 1**)
16	THS	$\overline{HOLD}$ Setup Time	5	—	ns	VCC ≥ 4.5V
			10	—	ns	VCC ≥ 2.5V
			20	—	ns	VCC ≥ 1.7V

Note 1: This parameter is not 100% tested but is ensured by characterization.

2: TWC begins on the rising edge of $\overline{CS}$ after a valid write sequence and ends when the internal write cycle is complete.

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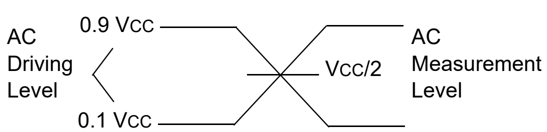
TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): T_{AMB} = -40°C to +85°C V_{CC} = 1.7V to 5.5V Extended (E): T_{AMB} = -40°C to +125°C V_{CC} = 1.8V to 5.5V			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
17	T_{HH}	$\overline{\text{HOLD}}$ Hold Time	5	—	ns	$V_{CC} \geq 4.5V$
			10	—	ns	$V_{CC} \geq 2.5V$
			20	—	ns	$V_{CC} \geq 1.7V$
18	T_{HZ}	$\overline{\text{HOLD}}$ Low to Output High Z	—	20	ns	$V_{CC} \geq 4.5V$ (Note 1)
			—	40	ns	$V_{CC} \geq 2.5V$ (Note 1)
			—	80	ns	$V_{CC} \geq 1.7V$ (Note 1)
19	T_{HV}	$\overline{\text{HOLD}}$ High to Output Valid	—	20	ns	$V_{CC} \geq 4.5V$
			—	40	ns	$V_{CC} \geq 2.5V$
			—	80	ns	$V_{CC} \geq 1.7V$
20	T_{UVL}	UVLO Detection Time	60	—	µs	
21	T_{WC}	Internal Write Cycle Time	—	4	ms	Note 2

Note 1: This parameter is not 100% tested but is ensured by characterization.

2: T_{WC} begins on the rising edge of $\overline{\text{CS}}$ after a valid write sequence and ends when the internal write cycle is complete.

FIGURE 1-1: INPUT TEST WAVEFORMS AND MEASUREMENT LEVELS



Note: t_R, t_F < 2 ns (10% to 90%)

FIGURE 1-2: OUTPUT TEST LOAD

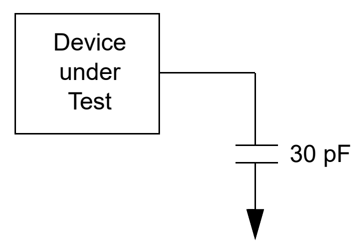


FIGURE 1-3: SERIAL INPUT TIMING

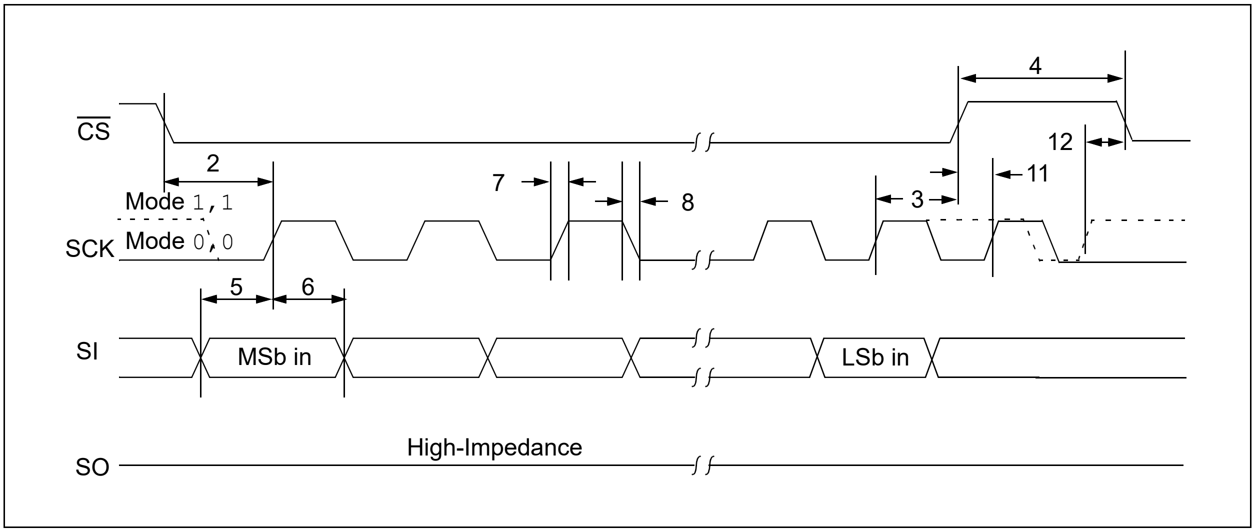


FIGURE 1-4: SERIAL OUTPUT TIMING

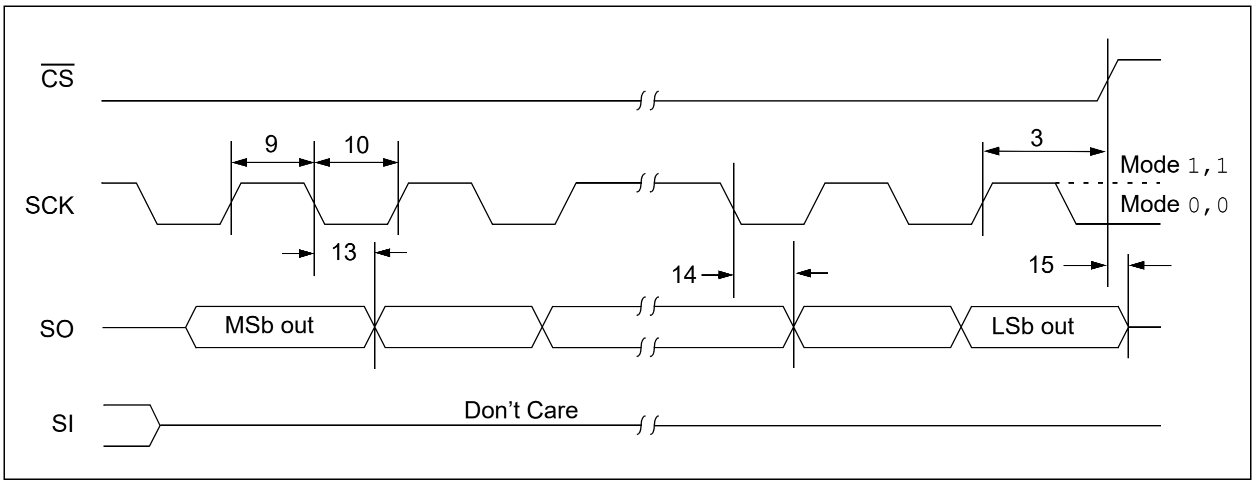


FIGURE 1-5: HOLD TIMING

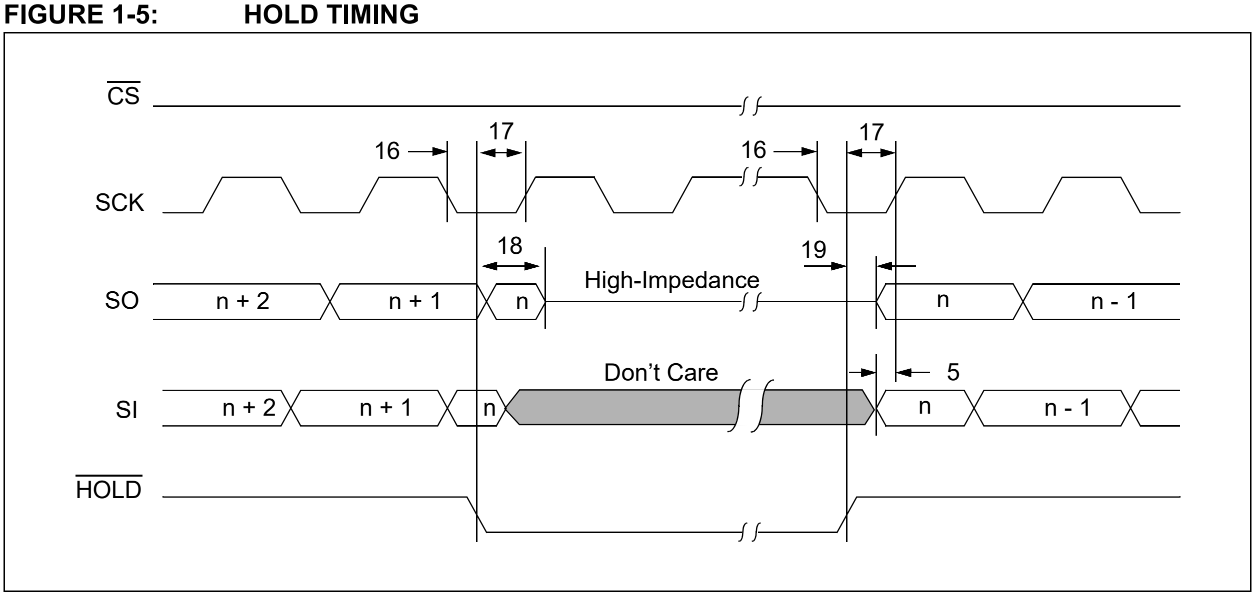


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TABLE 1-3: EEPROM CELL PERFORMANCE CHARACTERISTICS

Operation	Test Condition	Minimum	Maximum	Units
Write Endurance[1,2]	T_A = +25°C, 1.7V ≤ V_{CC} ≤ 5.5V	1,000,000	—	Write Cycles
Data Retention[1]	T_A = +55°C	200	—	Years

Note 1: Performance is determined through characterization and the qualification process.

2: Due to the memory array architecture, the write cycle endurance is specified for write sequences in groups of four data bytes. The beginning of any 4-byte boundaries can be determined by multiplying any integer (N) by four (i.e., 4*N). The end address can be found by adding three to the beginning value (i.e., 4*N+3). See **Section 8.2 "Error Correction Code (ECC) Architecture"** for more details on this implementation.

1.1 Power-Up Requirements and Default Conditions

During a power-up sequence, the VCC supplied to the 25CSM01 should monotonically rise from VSS to the minimum VCC level, as specified in Table 1-1, with a slew rate no faster than 0.1 V/µs.

1.1.1 DEVICE POWER-ON RESET

TABLE 1-4: POWER-UP CONDITIONS

Symbol	Parameter	Minimum	Maximum	Units
TVCSL	Minimum VCC to Chip Select Low Time	100	—	µs
VPOR	Power-on Reset Threshold Voltage	—	1.5	V
TPOFF	Minimum time at VCC = 0V between power cycles	1	—	ms

To prevent spurious events from happening during a power-up sequence, the 25CSM01 includes a Power-on Reset (POR) circuit. Upon power-up, the device will not respond to any instructions until the VCC level crosses the internal voltage threshold (VPOR) that brings the device out of Reset and into Standby mode.

Microchip recommends that $\overline{CS}$ follows the rise of VCC at power-up through the use of a pull-up resistor. The system designer must ensure that no instruction is sent to the device and that $\overline{CS}$ is driven high until the VCC supply reaches a stable value greater than the minimum VCC level. Once VCC has surpassed the minimum level, the SPI host must wait at least TVCSL before asserting the $\overline{CS}$ pin. See Table 1-4 for the values associated with these power-up parameters.

If an event occurs in the system where the VCC level supplied to the 25CSM01 drops below the maximum VPOR level specified, it is recommended that a full power cycle sequence be performed by first driving the VCC pin to VSS, waiting at least the minimum TPOFF time, and then performing a new power-up sequence in compliance with the requirements defined in this section.

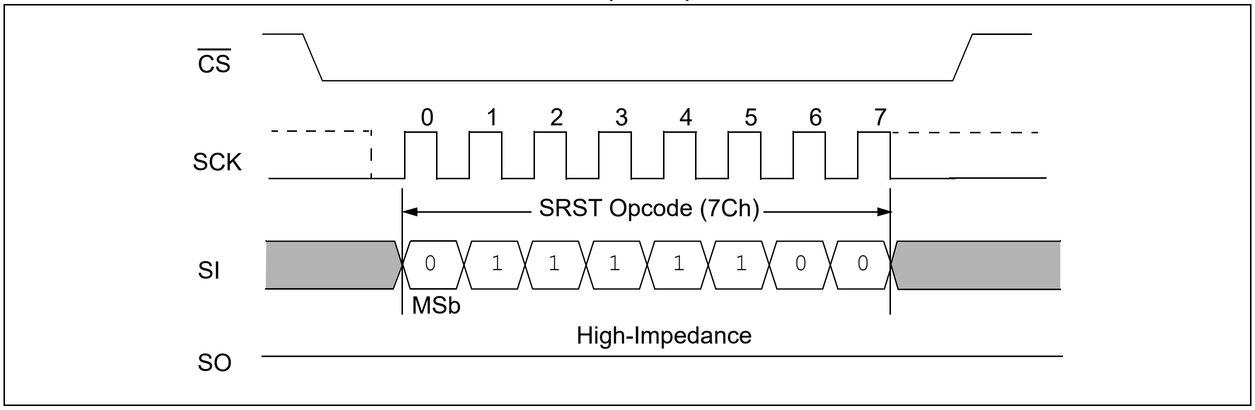
1.1.2 SOFTWARE RESET

The 25CSM01 includes a Software Device Reset (SRST) instruction that gives the user the opportunity to reset the device to its power-on default behavior (**Section 1.2 "Device Default State"**) without the need to power cycle the device. To execute this Reset, first, the $\overline{\text{CS}}$ pin must be driven low to select the device, and then a 7Ch opcode is clocked in on the SI pin.

Then the $\overline{\text{CS}}$ pin can be driven high, and the Reset mechanism will engage. The Reset will have internally completed by the time the minimum TCSD time is satisfied.

Note:	The SRST instruction cannot interrupt the device while it is in a Busy state (**Section 6.1.4 "Ready/Busy Status Latch"**).

FIGURE 1-6: SOFTWARE DEVICE RESET (SRST) INSTRUCTION



1.2 Device Default State

1.2.1 POWER-UP DEFAULT STATE

The 25CSM01 default state upon power-up consists of:

- Standby mode ($\overline{CS}$ = HIGH)
- A high-to-low level transition on $\overline{CS}$ is required to enter the active state
- Write Enable Latch (WEL) bit in the STATUS register = 0
- Error Correction State Latch (ECS) bit in the STATUS register = 0
- Partition Register Write Enable Latch (PREL) bit in the STATUS register = 0
- Ready/Busy ($\overline{RDY}$/BUSY) bit in the STATUS register = 0, indicating the device is ready to accept a new instruction

1.2.2 DEVICE FACTORY DEFAULT CONDITION

The 25CSM01 is shipped to the customer with the EEPROM array set to an all FFh data pattern (logic '1' state).

The Security register contains a preprogrammed 128-bit serial number in the lower 16 bytes. The user-programmable portion (lockable ID page) is unlocked and set to logic '1', resulting in 256 bytes of FFh data. In the various device registers, the following nonvolatile bits are set:

- Write Protection Enable (WPEN) bit in the STATUS register is set to logic '0', allowing writing to the STATUS register. (See Table 1-5).
- Block Write-Protect (BP[1:0] bits in the STATUS register are logic '0', indicating no write protection set when in Legacy mode. (See Table 1-5).
- Write Protection Mode (WPM) bit in the STATUS register is set to logic '0', indicating the device is set for Legacy Write Protection mode. (See Table 1-6).
- Freeze Memory Protection Configuration (FMPC) bit in the STATUS register is set to logic '0', indicating the Memory Partition Registers (MPRs) and the Write Protection Mode (WPM) bit are not locked and can be changed. (See Table 1-6).
- Protect Address Boundary Protection (PABP) bit in the STATUS register is set to logic '0', indicating the partition endpoint address value in each MPR can be modified. (See Table 1-6).
- Memory Partition Registers (MPR0-MPR3) are set to 00h, indicating that the entire 1 Mbit memory can be written. (See Table 1-7).
- Undervoltage Lockout Detection (UVLO) register is set to 00h, indicating that the UVLO function is not enabled and the undervoltage lockout detection level (VUVL) is set to the minimum level (See Table 1-8).

TABLE 1-5: STATUS REGISTER BITS – BYTE 0 (FACTORY DEFAULT)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	Reserved	Reserved	Reserved	BP1	BP0	WEL(1)	$\overline{RDY}$/BUSY(1)
0	0	0	0	0	0	0	0

Note 1: These bits are volatile and reset to this value upon power-up.

TABLE 1-6: STATUS REGISTER BITS – BYTE 1 (FACTORY DEFAULT)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPM	ECS(1)	FMPC	PREL(1)	PABP	Reserved	Reserved	$\overline{RDY}$/BUSY(1)
0	0	0	0	0	0	0	0

Note 1: These bits are volatile and reset to this value upon power-up.

TABLE 1-7: MEMORY PARTITION REGISTERS (FACTORY DEFAULT)

MPR No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Partition Behavior		Partition Endpoint Address					
	PB1	PB0	A16	A15	A14	A13	A12	A11
MPR0	0	0	0	0	0	0	0	0
MPR1	0	0	0	0	0	0	0	0
MPR2	0	0	0	0	0	0	0	0
MPR3	0	0	0	0	0	0	0	0

TABLE 1-8: UNDERVOLTAGE LOCKOUT DETECTION REGISTER (FACTORY DEFAULT)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	UVLOEN	VUVL4	VUVL3	VUVL2	VUVL1	VUVL0
0	0	0	0	0	0	0	0

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	8-Ball CSP	8-Lead DFN	8-Lead MSOP	8-Lead SOIC	8-Lead SOIJ	8-Lead TSSOP	Function
$\overline{\text{CS}}$	A5	1	1	1	1	1	Chip Select Input
SO	A3	2	2	2	2	2	Serial Data Output
$\overline{\text{WP}}$	B2	3	3	3	3	3	Write-Protect
Vss	A1	4	4	4	4	4	Ground
SI	C1	5	5	5	5	5	Serial Data Input
SCK	C3	6	6	6	6	6	Serial Clock Input
$\overline{\text{HOLD}}$	B4	7	7	7	7	7	Hold Input
Vcc	C5	8	8	8	8	8	Device Power Supply

2.1 Chip Select ($\overline{\text{CS}}$)

Asserting the $\overline{\text{CS}}$ pin selects the device. When the $\overline{\text{CS}}$ pin is deasserted, the device will be deselected and placed in Standby mode, and the SO pin will be in a high-impedance state. When the device is deselected, data will not be accepted on the SI pin.

A high-to-low transition on the $\overline{\text{CS}}$ pin is required to start a sequence, and a low-to-high transition is required to end a sequence. For write sequences, the device will not enter Standby mode until the completion of the self-timed internal write cycle.

2.2 Serial Data Output (SO)

The SO pin is used to shift data out from the device. Data on the SO pin are always clocked out on the falling edge of SCK. The SO pin is in a high-impedance state whenever the device is deselected ($\overline{\text{CS}}$ is deasserted) as well as when the Hold function is engaged.

2.3 Write-Protect Pin ($\overline{\text{WP}}$)

The Write-Protect ($\overline{\text{WP}}$) pin can be used to protect the STATUS register and memory array contents via the Block Protection modes when Legacy Write Protection mode is enabled.

When Enhanced Write Protection mode is enabled, the $\overline{\text{WP}}$ pin can be used to protect any memory zone in accordance with how its corresponding Memory Partition registers are programmed.

2.4 Serial Data Input (SI)

Instructions, addresses and data are latched by the 25CSM01 on the rising edge of the Serial Clock (SCK) line via the Serial Data Input (SI) pin.

2.5 Serial Clock (SCK)

The Serial Clock (SCK) pin is used to provide a clock signal to the device and is used to synchronize the flow of data to and from the device. Instructions, addresses and data present on SI pin are always latched in on the rising edge of SCK, while output data on the SO pin are always clocked out on the falling edge of SCK.

2.6 Hold ($\overline{\text{HOLD}}$)

When the device is selected and a serial communication sequence is underway, $\overline{\text{HOLD}}$ can be used to pause the communication with the host device without resetting the serial sequence.

3.0 MEMORY ORGANIZATION

3.1 EEPROM Organization

The 25CSM01 is internally organized as 512 pages of 256 bytes each.

3.2 Device Registers

The 25CSM01 contains four types of registers that modulate device operation and/or report on the current status of the device. These registers are:

- STATUS register
- Security register
- Memory Partition registers (four total)
- Identification register

3.2.1 STATUS REGISTER

The STATUS register is a 16-bit combination of volatile and nonvolatile bits. It is used to modify the write protection functions as well as store various aspects of the current status of the device. Details about the STATUS register are covered in **Section 6.0 “STATUS Register”**.

3.2.2 SECURITY REGISTER

The Security register is split into a read-only section and a user-programmable lockable ID page section. The read-only section contains a preprogrammed, globally unique, 128-bit serial number.

The user-programmable (lockable ID page) section of the Security register is ideal for applications that need to irreversibly protect critical or sensitive application data from ever being altered. See **Section 9.0 “Security Register”** for more details.

3.2.3 MEMORY PARTITION REGISTERS

The 25CSM01 is equipped with four Memory Partition registers. Each register is an 8-bit nonvolatile register that can be programmed with an ending address for the partition as well as determine the behavior of that partition. The partition protection can be set to one of four levels:

- Unprotected
- Software write-protected
- Hardware write-protected by the $\overline{\text{WP}}$ pin
- Software write-protected with locked memory partition register

A complete description of the Memory Partition register function can be found in **Section 10.0 “Memory Partition Functionality”**.

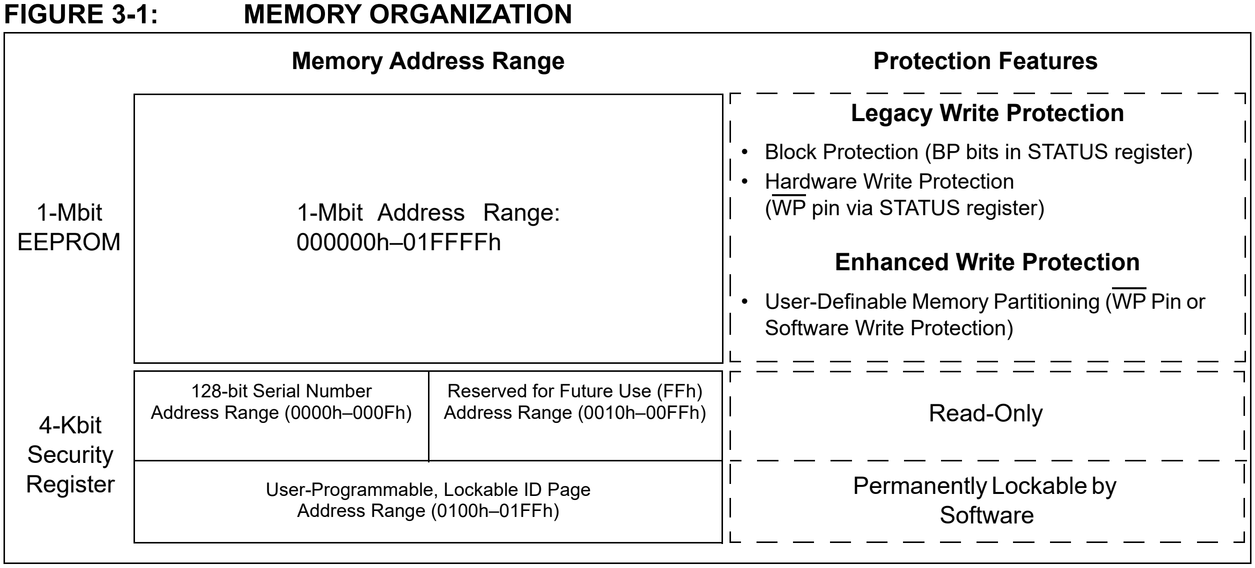
3.2.4 3.2.4 UNDERVOLTAGE LOCKOUT REGISTER

The Undervoltage Lockout Detection (UVLO) register is an 8-bit nonvolatile register that can be used to modify the threshold of the undervoltage detection circuit. Information on this function can be found in **Section 11.0 “Programmable UnderVoltage Lockout”**.

3.2.5 IDENTIFICATION REGISTER

The Identification register is a 40-bit nonvolatile, read-only register that contains device identification data in compliance with the JEDEC standard for “Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices.” The contents and format of the Identification register can be reviewed in **Section 12.0 “Identification Register”**.

FIGURE 3-1: MEMORY ORGANIZATION



4.0 FUNCTIONAL DESCRIPTION

4.1 Device Operation

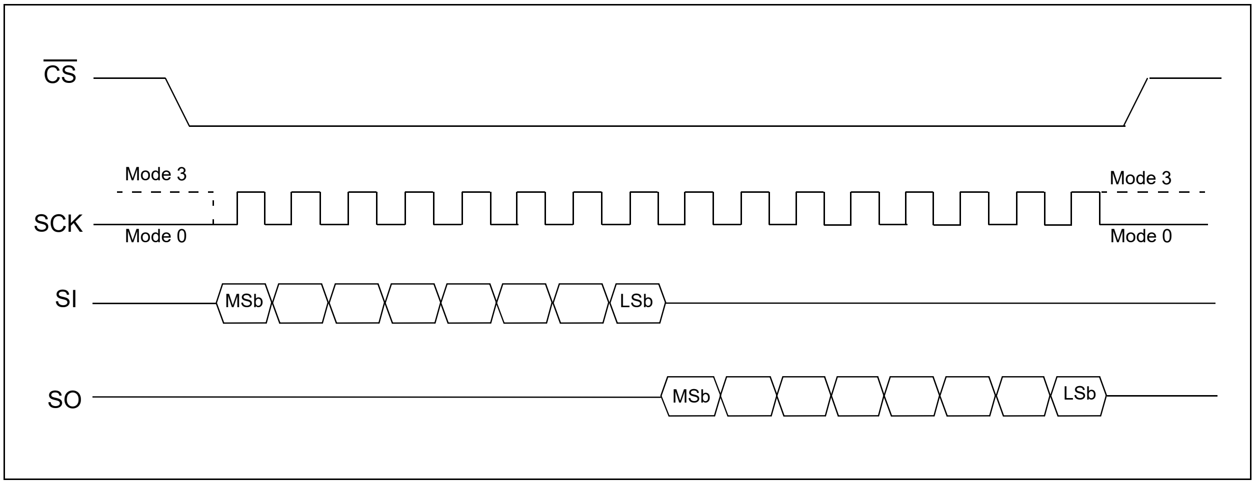
The 25CSM01 is controlled by a set of instructions that are sent from a host controller, commonly referred to as the SPI host. The SPI host communicates with the 25CSM01 via the SPI bus, which is comprised of four signal lines:

- Chip Select ($\overline{CS}$)
- Serial Clock (SCK)
- Serial Input (SI)
- Serial Output (SO)

The SPI protocol defines a total of four modes of operation (Mode 0, 1, 2, or 3), with each mode differing in respect to the SCK polarity and phase and how the polarity and phase control the flow of data on the SPI bus. The 25CSM01 supports the two most common modes, SPI Mode 0 and 3. With SPI Modes 0 and 3, data are always latched in on the rising edge of SCK and always output on the falling edge of SCK. The only difference between SPI Modes 0 and 3 is the polarity of the SCK signal when in the inactive state (when the SPI host is in Standby mode and not transferring any data). SPI Mode 0 is defined as a low SCK while $\overline{CS}$ is not asserted (high), and SPI Mode 3 has SCK high in the inactive state. The SCK Idle state must match when the $\overline{CS}$ is deasserted both before and after the communication sequence in SPI Mode 0 and 3.

The figures in this document depict Mode 0 with a solid line on SCK while $\overline{CS}$ is inactive and Mode 3 with a dotted line.

FIGURE 4-1: SPI MODE 0 AND MODE 3



4.2 Interfacing the 25CSM01 on the SPI Bus

Communication to and from the 25CSM01 must be initiated by the SPI host device. The SPI host device must generate the serial clock for the 25CSM01 on the SCK pin. The 25CSM01 always operates as a client due to the fact that the Serial Clock pin (SCK) is always an input.

4.2.1 SELECTING THE DEVICE

The 25CSM01 is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the SO pin will remain in a high-impedance state.

4.2.2 SENDING DATA TO THE DEVICE

The 25CSM01 uses the Serial Data Input (SI) pin to receive information. All instructions, addresses and data input bytes are clocked into the device with the Most Significant bit (MSb) first. The SI pin begins sampling on the first rising edge of the SCK line after the $\overline{CS}$ has been asserted.

4.2.3 RECEIVING DATA FROM THE DEVICE

Data output from the device is transmitted on the Serial Data Output (SO) pin with the MSb output first. The SO data are latched on the falling edge of the first SCK clock cycle after the instruction and address bytes, if necessary, have been clocked into the device.

4.3 Device Opcodes

4.3.1 SERIAL OPCODE

After the device is selected by driving $\overline{CS}$ low, the first byte sent must be the opcode that defines the sequence to be performed.

The 25CSM01 utilizes an 8-bit instruction register. The list of instructions and their operation opcodes are contained in Table 4-1. All instructions, addresses and data are transferred with the MSb first and are initiated with a high-to-low $\overline{CS}$ transition.

TABLE 4-1: INSTRUCTION SET FOR 25CSM01

Instruction	Instruction Description	Opcode		Address Bytes	Data Bytes	Reference Section
STATUS Register Instructions						
RDSR	Read STATUS Register	05h	0000 0101	0	1 or 2	6.2
WRBP	Write Ready/Busy Poll	08h	0000 1000	0	1	6.1.4.1
WREN	Set Write Enable Latch (WEL)	06h	0000 0110	0	0	5.1
WRDI	Reset Write Enable Latch (WEL)	04h	0000 0100	0	0	5.2
WRSR	Write STATUS Register	01h	0000 0001	0	1 or 2	6.3
EEPROM and Security Register Instructions						
READ	Read from EEPROM Array	03h	0000 0011	3	1+	7.1
WRITE	Write to EEPROM Array (1 to 256 bytes)	02h	0000 0010	3	1+	8.0
RDEX	Read from the Security Register	83h	1000 0011	3	1+	9.1
WREX	Write to the Security Register	82h	1000 0010	3	1+	9.2
LOCK	Lock the Security Register (permanent)	82h	1000 0010	3	1	9.2.1
CHLK	Check Lock Status of Security Register	83h	1000 0011	3	1	9.2.2
Memory Partition Register Instructions						
RMPR	Read Contents of Memory Partition Registers	31h	0011 0001	3	1	10.3
PRWE	Set Memory Partition Write Enable Latch	07h	0000 0111	0	0	10.2.1
PRWD	Reset Memory Partition Write Enable Latch	0Ah	0000 1010	0	0	10.2.2
WMPR	Write Memory Partition Registers	32h	0011 0010	3	1	10.2.3
PPAB	Protect Partition Address Boundaries	34h	0011 0100	3	1	10.1.3
FRZR	Freeze Memory Protection Configuration (permanent)	37h	0011 0111	3	1	10.4
Identification Register Instructions						
SPID	Read the SPI Manufacturer ID Data	9Fh	1001 1111	0	5	12.1
Undervoltage Lockout Register Instructions						
RUVL	Read the Undervoltage Lockout Register	15h	0001 0101	0	1	11.2.1
WUVL	Write Undervoltage Lockout Register	11h	0001 0001	0	1	11.2.2
Device Reset Instruction						
SRST	Software Device Reset	7Ch	0111 1100	0	0	1.1.2

4.4 Hold Function

The HOLD pin is used to pause the serial communication with the device without having to stop or reset the clock sequence. Hold mode, however, does not have an effect on the internal write cycle. Therefore, if a write cycle is in progress, asserting the HOLD pin will not pause the sequence, and the write cycle will continue until it is finished.

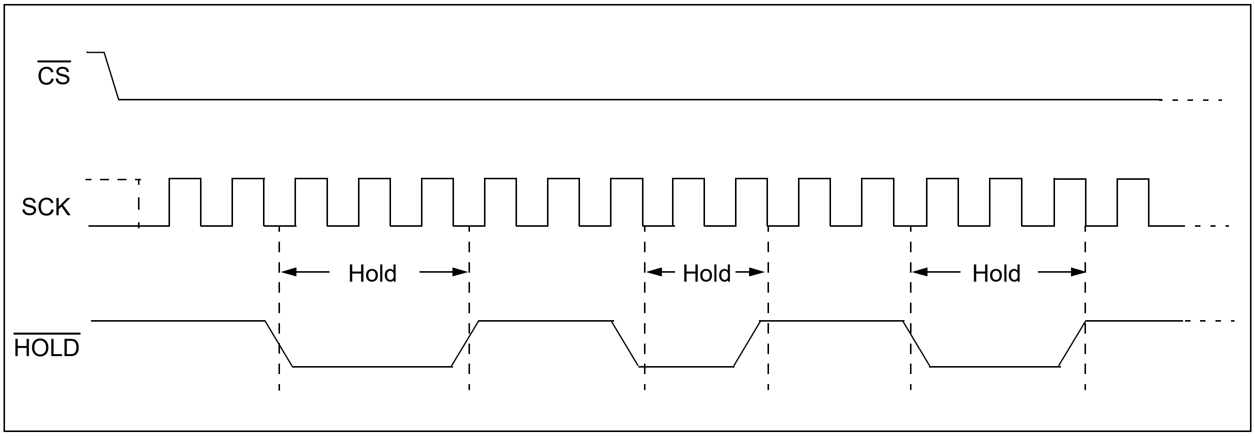
Hold mode can only be entered while the CS pin is asserted. Hold mode is activated by asserting the HOLD pin during the SCK low pulse. If the HOLD pin is asserted during the SCK high pulse, then Hold mode will not be started until the beginning of the next SCK low pulse. The device will remain in the Hold mode as long as the HOLD pin and CS pin are asserted.

While in Hold mode, the SO pin will be in a high-impedance state. In addition, both the SI pin and the SCK pin will be ignored. The WP pin, however, can still be asserted or deasserted while in Hold mode.

To end Hold mode and resume serial communication, the HOLD pin must be deasserted during the SCK low pulse. If the HOLD pin is deasserted during the SCK high pulse, then the Hold mode will not end until the beginning of the next SCK low pulse.

If the CS pin is deasserted while the HOLD pin is still asserted, then any sequence that may have been started will be aborted.

FIGURE 4-2: HOLD MODE



4.5 Write Protection

The 25CSM01 write protection schemes are first controlled by the state of the Write Protection Mode (WPM) bit in the STATUS register (bit 7, byte 1). The device can be set for either Legacy Write Protection mode or Enhanced Write Protection mode by the state of the WPM bit.

The Write Protection mode can be made permanent by executing the `FRZR` instruction. This can be done in *both* Legacy Write Protection mode and Enhanced Write Protection mode. Refer to **Section 10.4 "Freeze Memory Protection Configuration (FRZR)"** for details.

4.5.1 LEGACY WRITE PROTECTION MODE

In Legacy Write Protection mode, the EEPROM array can only be programmed in accordance with how the Block Protect bits in the STATUS register are programmed. Refer to **Section 6.1.2 "Block Write-Protect Bits"** for details.

Additionally, the contents of the STATUS register can be protected by enabling the Write-Protect Enable (WPEN) bit in the STATUS register.

When the WPEN function is enabled, the STATUS register contents will be protected when the WP pin is asserted (low). Details about the WPEN function are provided in **Section 6.1.1 "Write-Protect Enable Bit"**.

4.5.2 ENHANCED WRITE PROTECTION MODE

In Enhanced Write Protection mode, the EEPROM protection is determined by the contents of the Memory Partition Registers (MPR). Each MPR can be programmed to specify the ending address of a given partition as well as to set the desired protection behavior of that partition.

Full details about the Memory Partition registers can be found in **Section 10.0 "Memory Partition Functionality"**.

Note:	If Enhanced Write Protection mode is disabled, the MPRs will be ignored regardless of their configured behavior.

4.5.3 WRITE-PROTECT PIN FUNCTION

While in both Legacy Write Protection mode and Enhanced Write Protection mode, writing to the STATUS register and the Memory Partition registers can be inhibited by enabling the WPEN bit in the STATUS register. When the WPEN function is enabled, the contents of these registers will be protected when the $\overline{\text{WP}}$ pin is asserted (low). In order for these registers to be protected, the $\overline{\text{WP}}$ pin must be asserted for the entire $\overline{\text{CS}}$ valid time. Details about the WPEN function are provided in **Section 6.1.1 "Write-Protect Enable Bit"**.

If the internal write cycle has already been initiated, the $\overline{\text{WP}}$ pin going low will have no effect on any write sequence.

The $\overline{\text{WP}}$ pin function is blocked when the WPEN bit in the STATUS register is a logic '0'. This will allow the user to install the 25CSM01 device in a system with the $\overline{\text{WP}}$ pin tied to VSS and still be able to write to the STATUS register. All $\overline{\text{WP}}$ pin functions are enabled when the WPEN bit is set to a logic '1'.

5.0 WRITE ENABLE AND DISABLE

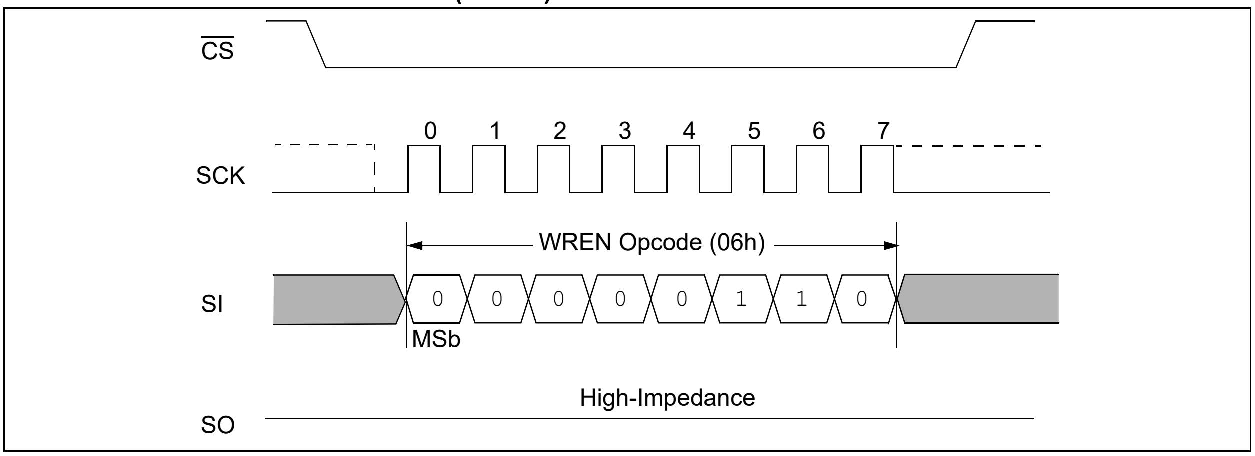
5.1 Write Enable Instruction (WREN)

The Write Enable Latch (WEL) bit of the STATUS register must be set to a logic '1' prior to each WRSR, WRITE, WREX, LOCK, PPWE, WMPR, PPAB and FRZR instruction. Some of these sequences need further instructions prior to being executed and are noted in their corresponding sections. The WEL bit is set to a logic '1' by sending a WREN (06h) instruction to the 25CSM01. First, the CS pin is driven low to select the device, and then a 06h instruction is clocked in on the SI pin. Then the CS pin is driven high. The WEL bit will be immediately updated in the STATUS register to a logic '1'.

The WEL bit will be reset to a logic '0' in the following circumstances:

- Upon power-up as the power-on default condition is the Write Disable state (**Section 1.2.2 "Device Factory Default Condition"**)
- Upon successful completion of any write sequence (WRITE, WRSR, WREX, LOCK, WMPR, PPAB, FRZR)
- When a Write Disable (WRDI) instruction is executed (**Section 5.2 "Write Disable Instruction (WRDI)"**)
- When a Software Device Reset (SRST) instruction is executed

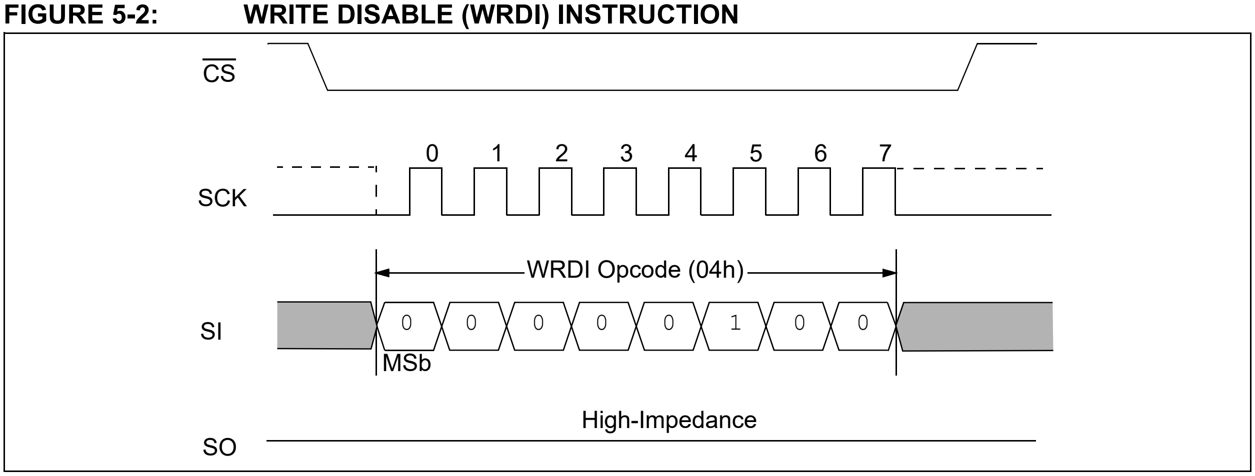
FIGURE 5-1: WRITE ENABLE (WREN) INSTRUCTION



5.2 Write Disable Instruction (WRDI)

To protect the device against inadvertent write sequences, the Write Disable (04h) instruction disables all programming modes by setting the WEL bit to a logic '0'. The WRDI instruction is independent of the WP pin state.

FIGURE 5-2: WRITE DISABLE (WRDI) INSTRUCTION



6.0 STATUS REGISTER

6.1 Status Register Bit Definition

The 25CSM01 includes a 2-byte STATUS register which is a combination of six nonvolatile bits of EEPROM and five volatile latches. The STATUS register bits modulate various features of the device, as shown in Register 6-1 and Register . These bits can be read or modified by specific instructions that are detailed in the subsequent sections.

REGISTER 6-1: STATUS REGISTER (BYTE 0)

R/W	U-0	U-0	U-0	R/W	R/W	R-0	R-0
WPEN	—	—	—	BP1	BP0	WEL	$\overline{\text{RDY}}$/BSY
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **WPEN:** Write-Protect Enable bit
1 = Write-Protect pin is enabled
0 = Write-Protect pin is ignored

bit 6-4 **Unimplemented:** Read as ‘0’

bit 3-2 **BP[1:0]:** Block Protection bits (see Table 6-2)
00 = No array write protection
01 = Upper quarter memory array protection
10 = Upper half memory array protection
11 = Entire memory array protection

bit 1 **WEL:** Write Enable Latch bit
1 = WREN has been executed and device is enabled for writing
0 = Device is not write-enabled

bit 0 **$\overline{\text{RDY}}$/BSY:** $\overline{\text{Ready}}$/Busy Status Latch bit
1 = Device is busy with an internal write cycle
0 = Device is ready for a new sequence

STATUS REGISTER (BYTE 1)

R/W-1	R-0	R	R-0	R	R	U-0	R-0
WPM	ECS	FMPC	PREL	PABP	WLS	—	$\overline{\text{RDY}}$/BSY
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **WPM:** Write Protection Mode bit[(1)]
1 = Enhanced Write Protection mode selected
0 = Legacy Write Protection mode selected

bit 6 **ECS:** Error Correction State Latch bit
1 = The previously executed read sequence did require the Error Correction Code (ECC)
0 = The previous executed read sequence did not require the Error Correction Code (ECC)

bit 5 **FMPC:** Freeze Memory Protection Configuration bit[(2)]
1 = Memory Partition registers and write protection mode are permanently frozen and cannot be modified
0 = Memory Partition registers and write protection mode are not frozen and are modifiable

bit 4 **PREL:** Partition Register Write Enable Latch bit
1 = PRWE has been executed and WMPR, FRZR and PPAB instructions are enabled
0 = WMPR, FRZR and PPAB instructions are disabled

bit 3 **PABP:** Partition Address Boundary Protection bit
1 = Partition Address Endpoints set in Memory Partition registers cannot be modified
0 = Partition Address Endpoints set in Memory Partition registers are modifiable

bit 2 **WLS:** Write Lockout State
1 = The previous nonvolatile write sequence was blocked by the UVLO
0 = The previous nonvolatile write sequence was not blocked by the UVLO

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **$\overline{\text{RDY}}$/BSY:** Ready/Busy Status Latch
1 = Device is busy with an internal write cycle
0 = Device is ready for a new sequence

Note 1: If the FMPC bit is set to a logic ‘1’, the WPM bit is read-only.
2: Once the FMPC bit has been set, it cannot be cleared.

6.1.1 WRITE-PROTECT ENABLE BIT

The Write-Protect Enable (WPEN) bit in the STATUS register (byte 0, bit 7) can be used in conjunction with the $\overline{\text{WP}}$ pin to inhibit writing to the various registers within the device.

The device is hardware write-protected when *both* the $\overline{\text{WP}}$ pin is low and the WPEN bit has been set to a logic ‘1’. The affected registers depend on the write protection mode selected.

The write protection mode is determined by the WPM bit in the STATUS register (bit 7, byte 1). Hardware write protection is disabled when *either* the $\overline{\text{WP}}$ pin is deasserted (high) or the WPEN bit is a logic ‘0’.

Table 6-1 describes which registers will be protected from being modified. The $\overline{\text{WP}}$ pin must be asserted (low) to enable any protection capabilities.

 Preliminary

TABLE 6-1: REGISTER BEHAVIOR IN LEGACY WRITE PROTECTION AND ENHANCED WRITE PROTECTION MODES

Write Protection Mode	$\overline{\text{WP}}$ Pin	WPEN Bit	STATUS Register	Memory Partition Registers
Legacy or Enhanced	Low	0	Not Protected	Not Protected
	Low	1	Protected	Protected
	High	x	Not Protected	Not Protected

Note: When the WPEN bit is a logic '1', it cannot be changed back to a logic '0', as long as the $\overline{\text{WP}}$ pin is asserted (low).

When the device is hardware write-protected, the nonvolatile bits of the STATUS register (WPEN, BP1, BP0, WPM, FMPC, PABP) become read-only and the Write STATUS Register (WRSR), Freeze Memory Protection Configuration (FRZR) and Protect Partition Address Boundaries (PPAB), Write Memory Partition Registers (WMPR) and Lock the Security Register (LOCK) instructions will not be accepted.

6.1.2 BLOCK WRITE-PROTECT BITS

The 25CSM01 contains four levels of EEPROM write protection using the Block Protection function. The nonvolatile Block Write-Protect bits (BP1, BP0) are located in bits three and two of the first STATUS register byte and define the region of the EEPROM and Security register that are to be treated as read-only. These values are only valid if the device has been set to Legacy Write Protection mode via the WPM STATUS register bit (byte 1, bit 7).

The four levels of array protection are as follows:

- **Level 0** – No portion of the EEPROM is protected, while the lower 256 bytes of the Security register are read-only.
- **Level 1** – The upper quarter address range is write-protected, meaning the highest order 1 Mbits in the EEPROM are read-only. The lower 256 bytes of the Security register are read-only.
- **Level 2** – The upper half address range is write-protected, meaning the highest order 2 Mbits in the EEPROM are read-only. The lower 256 bytes of the Security register are read-only.
- **Level 3** – Both the EEPROM and Security register are write-protected, meaning all addresses are read-only.

The address ranges that are protected for each Block Write Protection level and corresponding STATUS register control bits are shown in Table 6-2.

TABLE 6-2: BLOCK WRITE-PROTECT BITS

Level	STATUS Register Byte 0 Bits [3:2]		Protected Address Range	
	BP1	BP0	Memory Region	25CSM01
0	0	0	EEPROM	None
			Security Register	00000h-000FFh
1	0	1	EEPROM	180000h-1FFFFh
			Security Register	00000h-000FFh
2	1	0	EEPROM	10000h-1FFFFh
			Security Register	00000h-000FFh
3	1	1	EEPROM	00000h-1FFFFh
			Security Register	00000h-001FFh

Note: The Block Protection mechanism will only function with the WPM bit of the STATUS register (bit 7, byte 1) set to a logic '0', indicating Legacy Write Protection mode. If the WPM is set to logic '1', the device will respond in accordance with the Enhanced Write Protection mode. For more details on the Enhanced Write Protection mode, refer to **Section 10.1 "Enhanced Write Protection Mode"**.

6.1.3 WRITE ENABLE LATCH

Enabling and disabling writing to any nonvolatile register, the EEPROM array, and the Security register is accomplished through the Write Enable instruction (`WREN`) as shown in **Section 5.1 "Write Enable Instruction (WREN)"** and the Write Disable instruction (`WRDI`) as shown in **Section 5.2 "Write Disable Instruction (WRDI)"**. These functions change the state of the Write Enable Latch (WEL) bit (byte 0, bit 1) in the STATUS register.

6.1.4 READY/BUSY STATUS LATCH

The Ready/Busy Status Latch (RDY/BSY) is used to indicate whether the device is currently active in a nonvolatile write sequence. This bit is read-only and automatically updated by the device. This bit is provided in bit 0 of both STATUS register bytes.

A logic '`1`' bit indicates that the device is currently busy performing a nonvolatile write sequence. During this time, only the Read STATUS Register (`RDSR`) and the Write Ready/Busy Poll (`WRBP`) instructions will be executed by the device.

A logic '`0`' bit in this position indicates the device is ready to accept new instructions.

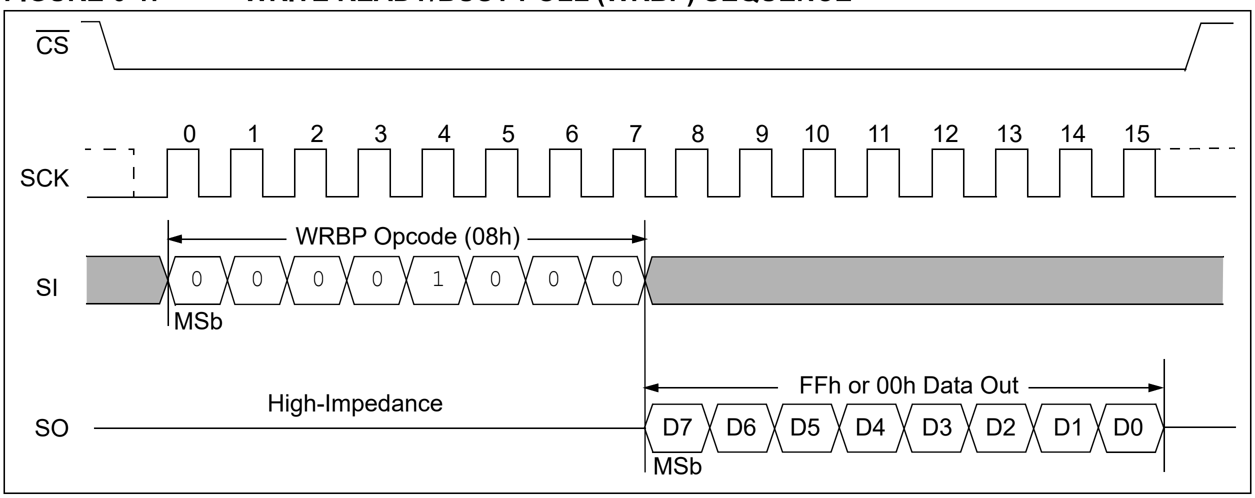
6.1.4.1 Write Ready/Busy Poll

The Write Ready/Busy Poll (`WRBP`) instruction provides direct access to the Ready/Busy STATUS register bit in an 8-bit format. The `WRBP` instruction can be used after any nonvolatile write sequence as a means to check if the device has completed its internal write cycle.

This instruction will return an FFh value when the device is still busy completing the write cycle or a 00h value if the device is no longer in a write cycle.

Refer to **Section 8.3 "Polling Routine"** for a description on implementing a polling routine. Continuous reading of the WRBP state is supported, and the value output by the device will be updated every eight bits.

FIGURE 6-1: WRITE READY/BUSY POLL (WRBP) SEQUENCE



6.1.5 WRITE PROTECTION MODE BIT

The 25CSM01 write protection behavior is controlled by the nonvolatile Write Protection Mode (WPM) bit in the STATUS register. This bit is located in bit 7, byte 1 of the STATUS register. A logic '`0`' indicates the device is in Legacy Write Protection mode, whereas a logic '`1`' indicates the device is in Enhanced Write Protection mode.

The write protection modes control how the contents of the EEPROM and Security register, as well as the various nonvolatile registers in the device, can be inhibited from writing. An overview of the two protection modes can be found in **Section 4.5 "Write Protection"**. Details on which nonvolatile registers are protected, in conjunction with the WP pin, can be found in **Section 6.1.1 "Write-Protect Enable Bit"**.

The WPM bit in the STATUS register can only be modified using the `WRSR` instruction as described in **Section 6.3 "Write STATUS Register (WRSR)"**.

Write protection mode can be made permanent by executing the `FRZR` instruction. This can be done in *both* Legacy Write Protection mode and Enhanced Write Protection mode. Refer to **Section 10.4 "Freeze Memory Protection Configuration (FRZR)"** for additional information.

6.1.6 ERROR CORRECTION STATE LATCH

The Error Correction State (ECS) bit is located in byte 1, bit 6 of the STATUS register. This bit indicates whether the on-chip Error Correction Code (ECC) logic scheme was invoked during the previous read sequence. For more information related to ECC, refer to **Section 8.2 "Error Correction Code (ECC) Architecture"**.

The ECS bit will be set to logic '0' unless the previously executed read sequence required the use of the ECC logic scheme. When this occurs the ECS bit will set to logic '1'.

The ECS bit will continue to read a logic '1' until another read sequence occurs where the use of the ECC logic scheme is not required, a Power-on Reset (POR) event occurs, or a Software Device Reset (SRST) instruction is sent to the 25CSM04.

6.1.7 FREEZE MEMORY PROTECTION CONFIGURATION BIT

The Freeze Memory Protection Configuration (FMPC) bit resides in byte 1, bit 5 of the STATUS register. This bit is nonvolatile and One-Time-Programmable (OTP) with a factory default value of logic '0'.

This bit can only be set to a logic '1' as a result of the Freeze Memory Protection Configuration (FRZR) instruction (**Section 10.4 "Freeze Memory Protection Configuration (FRZR)"**). This bit cannot be modified with a Write STATUS Register (WRSR) instruction. Once this bit has been permanently set to a logic '1', the memory configuration cannot be changed.

6.1.8 PARTITION WRITE ENABLE LATCH

In addition to the WEL bit, enabling and disabling writing to the Memory Partition register is done by issuing the Set Memory Partition Write Enable Latch (PRWE) as shown in Figure 10-3 and the Reset Memory Partition Write Enable Latch (PRWD) as shown in Figure 10-4. These functions change the status of the PREL bit (byte 1, bit 4). in the STATUS register.

Note:	The WEL bit must first be set before issuing the PRWE instruction; otherwise, it is ignored.

6.1.9 PARTITION ADDRESS BOUNDARY PROTECTION BIT

The Partition Address Boundary Protection (PABP) bit is located in byte 1, bit 3 of the STATUS register. This bit can be read through an RDSR instruction but can only be set or cleared through a Protect Partition Address Boundary sequence (see **Section 10.1.3 "Protecting the Partition Endpoint Addresses"**). When programmed to a logic '1', the address range bits in the Memory Partition registers are read-only and cannot be modified, but the behavior bits can still be modified.

If the Freeze Memory Protection Configuration bit has been programmed to a logic '1', the address range and behavior bits are permanently read-only and cannot be modified regardless of the state of the PABP bit.

6.1.10 WRITE LOCKOUT STATE BIT

The Write Lockout State (WLS) bit is located in byte 1, bit 2 of the STATUS register. This bit indicates whether the last write sequence was inhibited by the UVLO detection circuit (see **Section 11.0 "Programmable UnderVoltage Lockout"**). A logic '1' in this bit position indicates the previous write sequence was inhibited by UVLO. A logic '0' indicates the previous write sequence was not inhibited by UVLO.

The WLS bit will continue to read out a logic '1' until one of the following events occurs:

- A Power-on Reset (POR) event (**Section 1.1.1 "Device Power-On Reset"**)
- A nonvolatile write op-code is sent to the device (WRITE, WRSR, WREX, LOCK, WMPR, PPAB, FRZR, WUVL)
- A Software Device Reset (SRST) instruction is executed

Note:	The Write Lockout State (WLS) bit is only valid if the undervoltage lockout function is enabled.

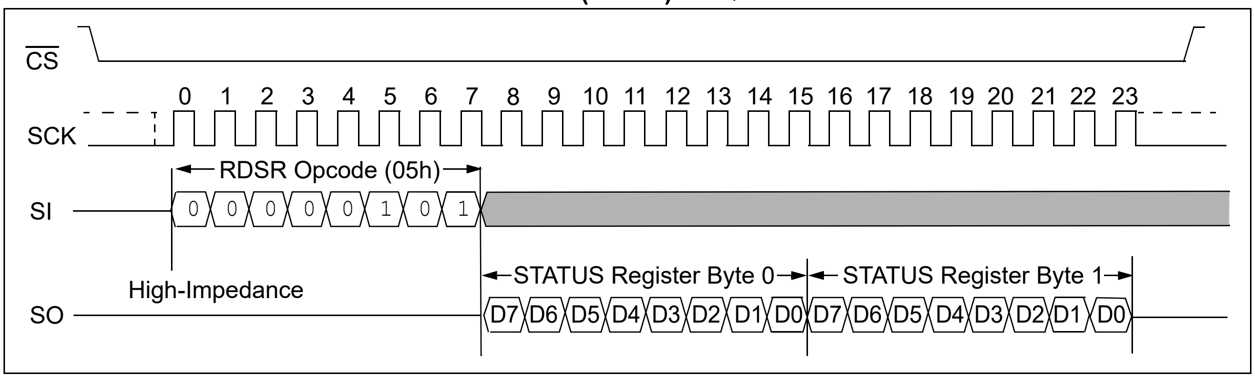
6.2 Read STATUS Register (RDSR)

The Read STATUS Register (`RDSR`) instruction provides access to the contents of the STATUS register. The STATUS register is read by asserting the CS pin, followed by sending a 05h opcode. The device will return the 16-bit STATUS register value on the SO pin.

The STATUS register can be continuously read for data by continuing to read beyond the first 16-bit value returned. The 25CSM01 will update the value of the volatile bits (RDY/BSY, WEL and PREL) in the STATUS register at byte boundaries, thereby allowing new STATUS register volatile bit values to be read without having to issue a new `RDSR` instruction.

A new `RDSR` instruction needs to be initiated in order for the nonvolatile bits (WPEN, BP0, BP1 and WPM) in the STATUS register to be updated.

FIGURE 6-2: READ STATUS REGISTER (RDSR) SEQUENCE



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6.3 Write STATUS Register (WRSR)

The Write STATUS Register (`WRSR`) instruction enables the SPI host to change selected bits of the STATUS register. Before a WRSR sequence can be initiated, a `WREN` instruction must be executed to set the WEL bit to logic ‘`1`’. Upon completion of a `WREN` instruction, a WRSR sequence can be executed.

The `WRSR` instruction will only modify:

- Byte 0: bit 7, bit 3 and bit 2
- Byte 1: bit 7

These modifiable bits are the Write-Protect Enable (WPEN) bit, the Block Protect (BP1, BP0) bits and the Write Protection Mode (WPM) bit.

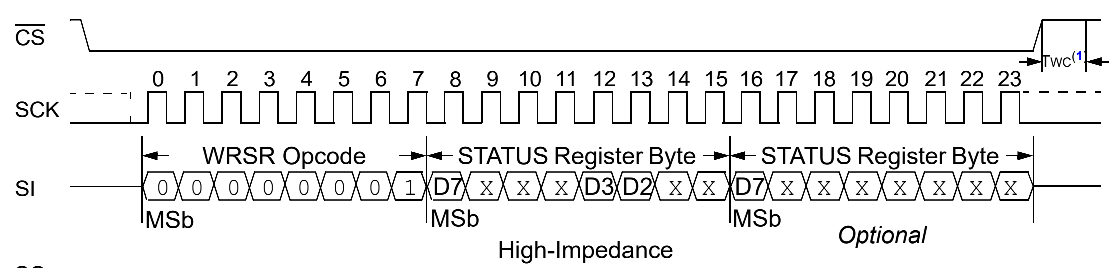
These four bits are nonvolatile cells that have the same properties and functions as regular EEPROM cells. Their values are retained while power is removed from the device. While FMPC (byte 1, bit 5) and PABP (byte 1, bit 3) of the STATUS register are also nonvolatile bits, they are modified through dedicated instructions. Refer to **Section 6.1.7 “Freeze Memory Protection Configuration Bit”** and **Section 10.1.3 “Protecting the Partition Endpoint Addresses”** for more details about these requirements.

When writing to the STATUS register, byte 0 must always be written. Byte 1 can optionally be written to utilize Enhanced Write Protection mode.

Note:	If the $\overline{CS}$ pin is deasserted somewhere other than at the end of an 8-bit byte boundary, the sequence will be aborted, and no write cycle will take place.

The 25CSM01 will not respond to instructions other than a `RDSR` or a `WRBP` after a WRSR sequence until the self-timed internal write cycle has completed. When the write cycle has completed, the WEL bit in the STATUS register is reset to a logic ‘`0`’.

FIGURE 6-3: WRITE STATUS REGISTER (WRSR) SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

7.0 READ SEQUENCES

7.1 Reading from the EEPROM

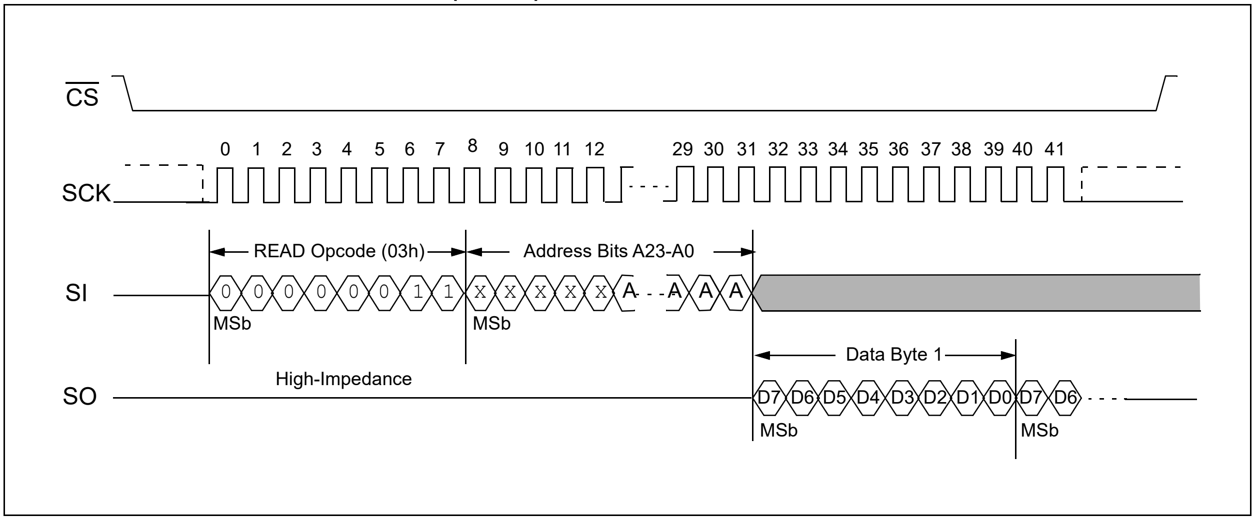
Reading the EEPROM contents can be done whenever the device is not in an internal write cycle, as indicated by the Ready/Busy bit of the STATUS register. To read the EEPROM, first, the CS line is pulled low to select the device, and the `READ` (03h) instruction is transmitted via the SI line followed by the 24-bit address to be read. Address bits A23 through A17 are “don’t care” bits because they do not fall within the addressable memory range.

Upon completion of the 24-bit address, any data on the SI line will be ignored. The data (D7–D0) at the specified address are then shifted out onto the SO line. If only one byte is to be read, the CS line should be driven high after the data are clocked out.

The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address (00000h), allowing the entire memory to be read in one continuous read cycle regardless of the starting address.

The read sequence can be terminated at any point in the sequence by driving CS high.

FIGURE 7-1: READ EEPROM (READ) SEQUENCE



8.0 WRITE SEQUENCES

In order to program the EEPROM in the 25CSM01, the device must be write-enabled via the Write Enable instruction (`WREN`). If the device is not write-enabled, it will ignore the `WRITE` instruction and return to the Standby state when $\overline{CS}$ is brought high. The address of the memory location(s) to be programmed must be outside the protected address range(s) selected by the Block Write Protection level or the contents of the various Memory Partition registers. During an internal write cycle, all instructions will be ignored except the `RDSR` and the `WRBP` instructions.

8.1 Write Instruction Sequences

8.1.1 BYTE WRITE

Once a `WREN` instruction has been completed, a byte write sequence can be performed as shown in Figure 8-1. After the $\overline{CS}$ line is pulled low to select the device, the `WRITE` (02h) instruction is transmitted via the SI line, followed by the 24-bit address and the data (D7-D0) to be programmed.

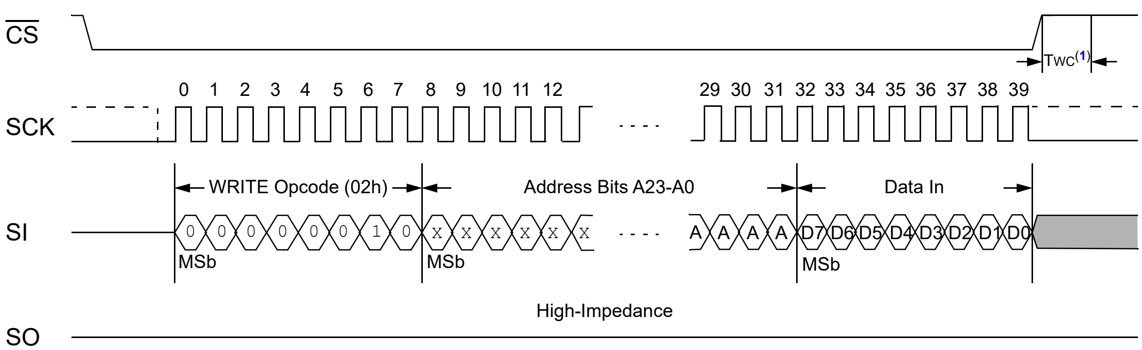
Address bits A23 through A17 are "don't care" bits because they do not fall within the addressable memory range.

Programming will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low time (mode 0) and SCK high time (mode 3) immediately after clocking in the D0 (LSB) data bit.

Note:	If the $\overline{CS}$ pin is deasserted somewhere other than at the end of an 8-bit byte boundary, the sequence will be aborted, and no write cycle will take place.

The 25CSM01 is automatically returned to the Write Disable state (STATUS register bit WEL = `0`) at the completion of a write cycle.

FIGURE 8-1: BYTE WRITE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

8.1.2 PAGE WRITE

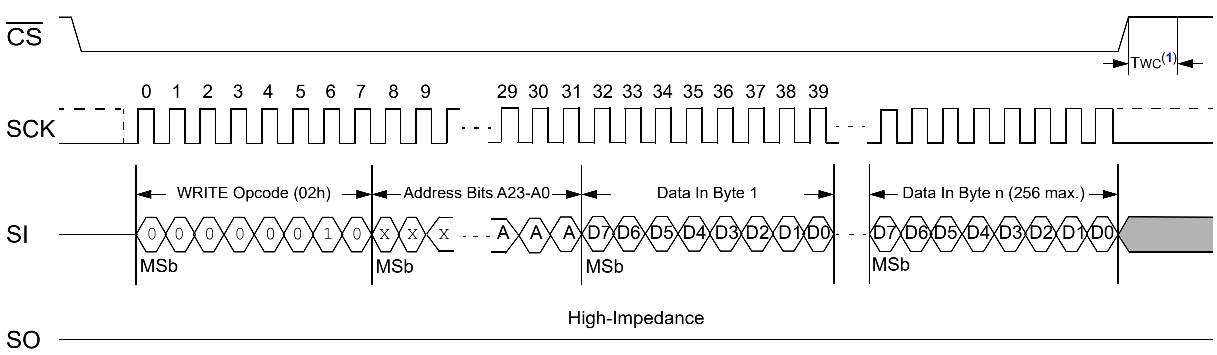
A page write sequence is the same as a byte write, however allowing up to 256 bytes to be written in the same write cycle, provided that all bytes are in the same page of the memory array (where addresses A16 through A8 are the same). Partial page writes of less than 256 bytes are allowed. After each byte of data is received, the eight lowest order address bits are internally incremented by one, and the remaining address bits will remain constant.

If more bytes of data are transmitted than what will fit at the end of that memory page, the address counter will roll over to the beginning of the same page, and only the last 256 bytes of data received will be written to the device.

Upon completion of a write cycle, the 25CSM01 automatically returns to the Write Disable state (STATUS register bit WEL = `0`).

Note:	If the $\overline{CS}$ pin is deasserted somewhere other than at the end of an 8-bit byte boundary, the sequence will be aborted, and no write cycle will take place.

FIGURE 8-2: PAGE WRITE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

8.2 Error Correction Code (ECC) Architecture

The 25CSM01 incorporates a built-in Error Correction Code (ECC) logic scheme. The EEPROM array is internally organized as a group of four connected bytes plus an additional six ECC parity bits of EEPROM. These 38 bits are referred to as the internal physical data word. During a read sequence, the ECC logic compares each 4-byte physical data word with its corresponding six ECC parity bits. If a single bit out of the 4-byte region happens to read incorrectly, the ECC logic will detect the bad bit and replace it with a correct value before the data is serially clocked out. This architecture significantly improves the reliability of the 25CSM01 compared to a device that does not utilize ECC.

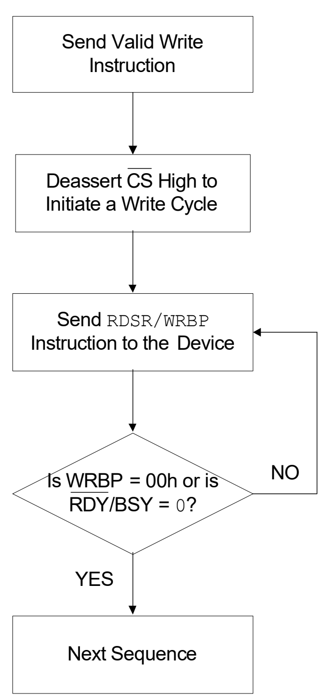
It is important to note that data are always physically written to the part at the internal physical data word level, regardless of the number of bytes written. Writing single bytes is still possible with the byte write sequence, but internally, the other three bytes within the 4-byte location where the single byte was written, along with the six ECC parity bits will be updated. Due to this architecture, the 25CSM01 EEPROM write endurance is rated at the internal physical data word level (4-byte word). The system designer needs to optimize the application writing algorithms to observe these internal word boundaries in order to maximize the endurance.

8.3 Polling Routine

A polling routine can be implemented to optimize time sensitive applications that would not prefer to wait the fixed maximum write cycle time (TWC). This method allows the application to query whether the Serial EEPROM has completed the write sequence. This polling routine should be initiated once the internally timed write sequence has begun.

The polling routine repeatedly sends Read STATUS Register (`RDSR`) or Write Ready/Busy Poll (`WRBP`) instructions to determine if the device has completed its self-timed internal write cycle (see Figure 8-3). If the RDY/$\overline{BSY}$ bit = `1` from `RDSR` or FFh from `WRBP`, the write cycle is still in progress. If the RDY/$\overline{BSY}$ bit = `0` from `RDSR` or 00h from `WRBP`, this indicates the write cycle has ended. If the device is still in a busy state, repeated `RDSR` or `WRBP` instructions can be executed until the RDY/$\overline{BSY}$ bit = `0` or the `WRBP` instruction returns a 00h, signaling that the device is ready to execute a new instruction. Only the `RDSR` and `WRBP` instructions are enabled during the write cycle.

FIGURE 8-3: POLLING FLOW



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9.0 SECURITY REGISTER

The Security register is segmented into one 256-byte read-only page and one 256-byte user-programmable, lockable ID page. The user-programmable, lockable ID page supports both byte write and page write sequences. The user-programmable lockable ID page may be permanently locked at any time with the `LOCK` instruction. The Security register lock state can be verified at any time with `CHLK` instruction.

TABLE 9-1: SECURITY REGISTER ORGANIZATION

Security Register Byte Number									
0	1	...	254	255	256	257	...	510	511
Factory-Programmed (Read-only) 0-15: Device Serial Number 16-255: Reserved for Future Use					User-Programmable (Lockable)				

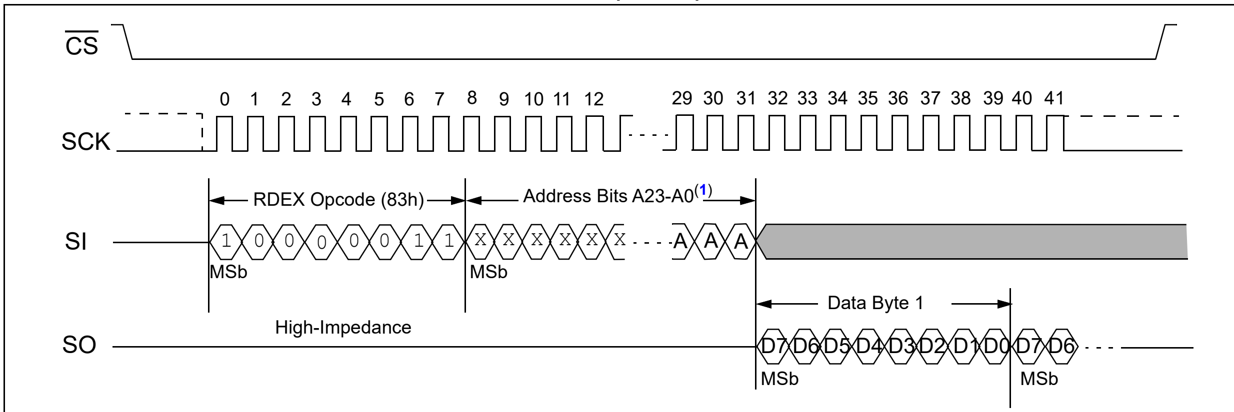
9.1 Reading from the Security Register

Reading the Security register contents from 25CSM01 follows a similar sequence to reading the EEPROM, but a different opcode and specific address data are required. To read the Security register, first drive the $\overline{CS}$ low to select the device, then send the `RDEX` (83h) instruction via the SI line, followed by the 24-bit address to be read.

Note:	Address bits A23 through A9 are “don’t care” bits, except A10 which must be a logic ‘`0`’.

Upon completion of the 24-bit address, any data on the SI line will be ignored. The data (D7 – D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached (0001FFh), the address counter will roll over to the lowest address (0000h), allowing the entire Security register to be read in one continuous read cycle regardless of the starting address.

FIGURE 9-1: READ SECURITY REGISTER (RDEX) SEQUENCE



Note 1: Address bit A10 must be ‘`0`’ to read the Security register.

9.1.1 READING THE FACTORY-PROGRAMMED 128-BIT SERIAL NUMBER

The Security register contains a factory-programmed, globally unique, read-only 128-bit serial number. This serial number is unique across all varieties of Microchip CS series EEPROM, and it is located in the lower 16 bytes of the Security register (bytes 0h-Fh). Reading the serial number is accomplished in the same way as reading any other data in the Security register.

Note:	To ensure a unique number, the 128-bit serial number must be read from the starting address. Additionally, the entire serial number must be read to obtain a completely unique value.

9.2 Writing to the Security Register

Executing a write sequence to the Security register is identical to the EEPROM as described in **Section 8.1.1 "Byte Write"** and **Section 8.1.2 "Page Write"**, with the exception that the `WREX` (82h) instruction is used, and A10 must be a logic '`0`' and A8 must be a logic '`1`' to write the user-programmable, lockable ID page. In Legacy Write Protection mode, the Security register is write-protected when the BP [1:0] bits (byte 0, bits 3-2) of the STATUS register = 11. There is no dependency on the WPEN bit (byte 0, bit 7) of the STATUS register or the $\overline{\text{WP}}$ pin.

The user-programmable, lockable ID page of the Security register can also be permanently locked such that its contents also become read-only. This is accomplished with `LOCK` instruction. Determining if the device has previously been locked can be done with the `CHLK` instruction. If the Security register is locked, any subsequent `WREX` instructions will be ignored.

Note:	If the $\overline{\text{CS}}$ pin is deasserted somewhere other than at the end of an 8-bit byte boundary, the sequence will be aborted, and no write cycle will take place.

9.2.1 LOCKING THE SECURITY REGISTER

The upper 256 bytes of the Security register are shipped by Microchip in a user-programmable state. Once the desired data is written, the user-programmable, lockable ID page of the Security register can be permanently write-protected with the `LOCK` instruction.

Note:	The `LOCK` instruction will be ignored if the WPEN bit (byte 0, bit 7) of the STATUS register is set to a logic '`1`' and the WP pin is asserted.

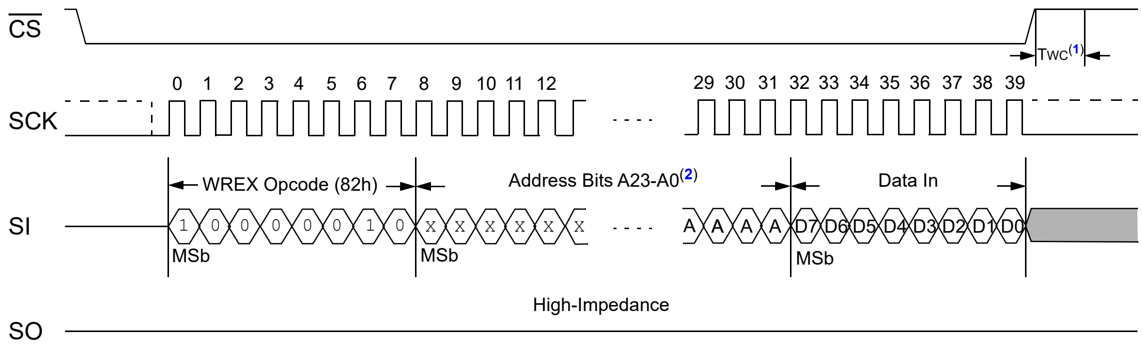
The `LOCK` instruction is irreversible and will permanently prevent all future write sequences to the upper 256 bytes of the Security register on the 25CSM01, thereby rendering the entire 512-byte Security register read-only.

Note:	Once the Security register has been locked, *it is not possible to unlock it.*

The `LOCK` instruction emulates a write sequence in that a `WREN` instruction must first be sent to set the WEL bit in the STATUS register to logic '`1`'. As shown in Figure 9-4, the `LOCK` (82h) instruction is clocked in on the SI line, followed by a dummy address where bits A23 through A0 are "don't care" bits with the exception that bit A10 must be set to '`1`'. Finally, a confirmation data byte of `xxxxxx1xb` is sent, and the self-timed internal write cycle will begin once the $\overline{\text{CS}}$ pin is driven high.

Note:	If the $\overline{\text{CS}}$ pin is deasserted before the end of the 40-bit sequence, the sequence will be aborted, and no write cycle will take place.

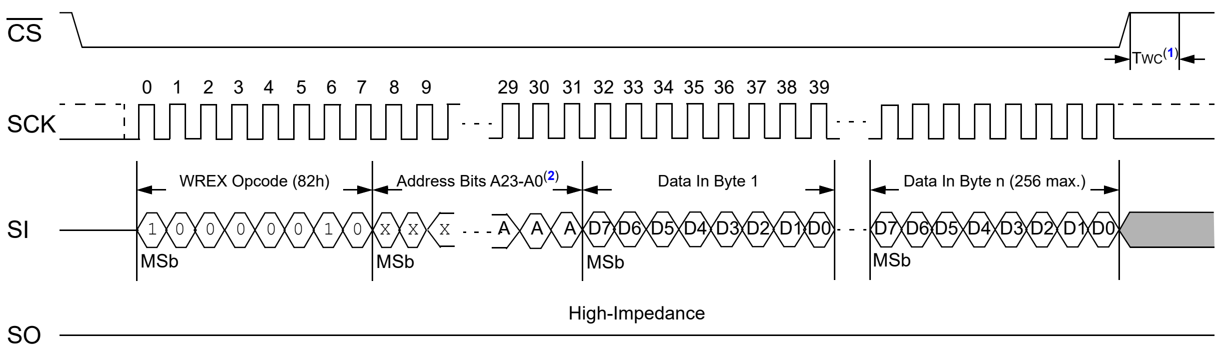
FIGURE 9-2: WRITE SECURITY REGISTER (WREX) BYTE WRITE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

2: A23 through A9 are "don't care" bits, except A10 which must be a logic '0' and A8 which must be a logic '1' to address the second Security register byte that is user programmable.

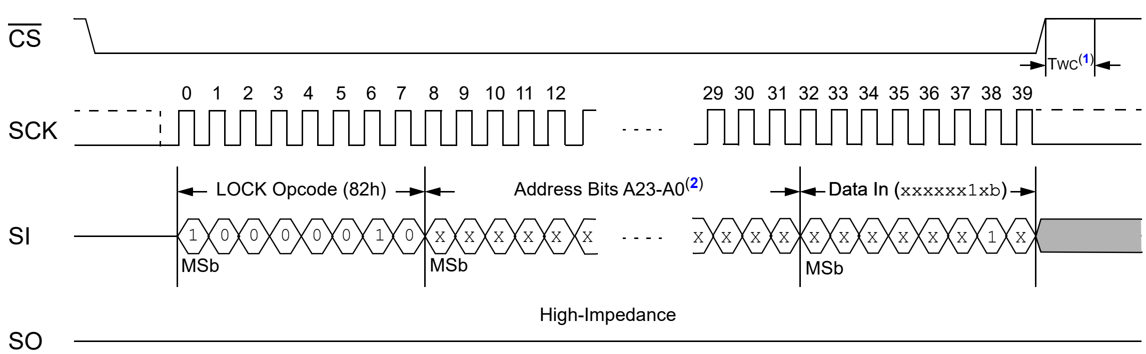
FIGURE 9-3: WRITE SECURITY REGISTER (WREX) PAGE WRITE SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

2: A23 through A9 are "don't care" bits, except A10 which must be a logic '0' and A8 which must be a logic '1' to address the second Security register byte that is user programmable.

FIGURE 9-4: LOCK SECURITY REGISTER (LOCK) SEQUENCE



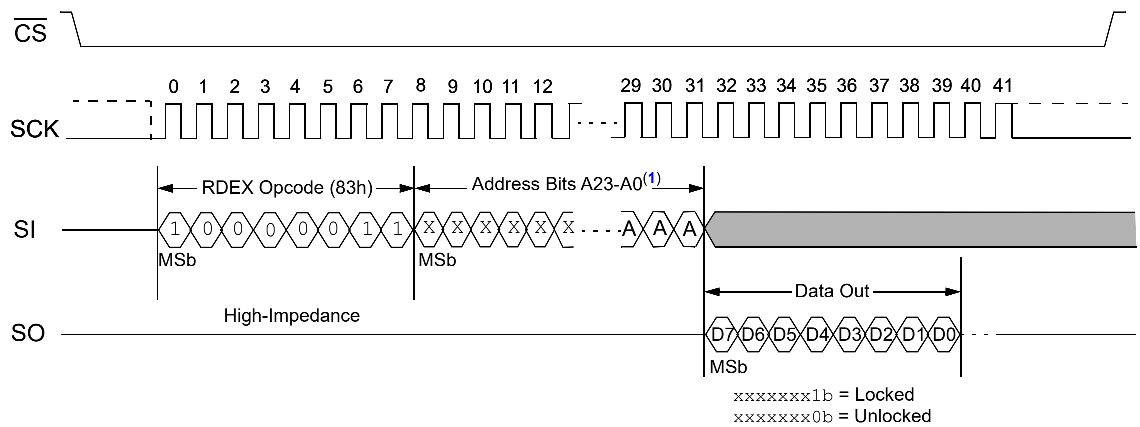
Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

2: A23 through A0 are "don't care" bits, except A10 which must be a logic '1'.

9.2.2 DETERMINING THE LOCK STATE OF THE SECURITY REGISTER

To determine whether or not the user-programmable, lockable ID page of the Security register is locked, the 25CSM01 includes a `CHLK` instruction to check the lock state. To determine the lock status, the opcode 83h must be clocked into the device on the SI line. The address bit A10 must be equal to logic '1' while the other address bits are "don't care". Data bit 0 of the data byte clocked out on the SO line determines the lock state; the other bits of the data byte are "don't care" bits. A data response of `xxxxxxx1b` indicates the region is locked, while a `xxxxxxx0b` response indicates that the region is not locked.

FIGURE 9-5: CHECK SECURITY REGISTER LOCK (CHLK) SEQUENCE



Note 1: A23 through A0 are "don't care" bits, except A10 which must be a logic '1'.

10.0 MEMORY PARTITION FUNCTIONALITY

The write-protect functionality of the 25CSM01 can be configured for Legacy Write Protection mode or Enhanced Write Protection mode with the WPM bit of the STATUS register (see **Section 6.1.5 "Write Protection Mode Bit"**). Changing this bit is accomplished with a WRSR sequence. If WPM is set to a logic '0', then the device is set for Legacy Write Protection mode. If WPM is a logic '1', Enhanced Write Protection mode is enabled.

Note:	The write protection mode can be made permanent by executing the FRZR instruction. This can be done in *both* Legacy Write Protection mode and Enhanced Write Protection mode. Refer to **Section 10.4 "Freeze Memory Protection Configuration (FRZR)"** for additional information.

When the device is set for Legacy Write Protection mode, the EEPROM and Security register are protected based upon the Block Protection bits in the STATUS register. This functionality is described in **Section 6.1.2 "Block Write-Protect Bits"**.

10.1 Enhanced Write Protection Mode

The device incorporates an Enhanced Write Protection mode, which is enabled by setting the WPM bit of the STATUS register (byte 1, bit 7) to a logic '1'. When the device is set to Enhanced Write Protection mode, the STATUS register and Memory Partition registers are protected from any modification when the WPEN bit is set to a logic '1' and the $\overline{WP}$ pin is asserted.

Setting the 25CSM01 for Enhanced Write Protection mode enables its four Memory Partition Registers (MPR0 through MPR3). These are 8-bit registers that control the memory organization in terms of writable address ranges and the type of protection behavior.

10.1.1 MEMORY PARTITIONING OVERVIEW

Through the use of the device's four MPRs, the EEPROM array can be divided into as many as five partitions. Each MPR specifies one of four types of protection behaviors for its corresponding partition.

The Memory Partition register contents specify the six Most Significant bits of the memory array address (A16 through A11) corresponding to the endpoint of a given partition where A10 through A0 are a logic '1'. This creates an available partition size in 8-page (2-Kbyte) increments, meaning the partition can be set as small as 16-Kbit (2^{11} x 8). However, each partition can be uniquely sized to fit the application requirements. Figure 10-1 provides a map of the available partition points.

Note:	If Enhanced Write Protection mode is disabled, the MPRs will be ignored regardless of their configured behavior.

FIGURE 10-1: 25CSM01 MEMORY PARTITION MAP

	1-Mbit (128-Kbyte) EEPROM (256 bytes per page x 512 pages)	Beginning Address	Ending Address	
Available Partition Point: A16:A11 [000000b]	8 Pages	000000h	0007FFh	16-Kbit
Available Partition Point: A16:A11 [000001b]	8 Pages	000800h	000FFFh	16-Kbit
Available Partition Point: A16:A11 [000010b]	8 Pages	001000h	0017FFh	16-Kbit
Available Partition Point: A16:A11 [000011b]	8 Pages	001800h	001FFFh	16-Kbit
	- - - -	- - - -	- - - -	
Available Partition Point: A16:A11 [111110b]	8 Pages	01F000h	01F7FFh	16-Kbit
Available Partition Point: A16:A11 [111111b]	8 Pages	01F800h	01FFFFh	16-Kbit

10.1.2 MEMORY PARTITION REGISTER ORGANIZATION

Each MPR is an 8-bit nonvolatile register. The MPR organization is shown in Register 10-1. The four types of protection behavior are defined by the contents of bit 7 and bit 6 of each MPR (see Register 10-1). Each partition can have a unique behavior.

Bit 5 though bit 0 contain the Partition Endpoint Address of A16:A11, where A10:A0 are set to logic '1'. For example, if the first partition of the memory array is intended to stop after 16 Kbits of memory, the endpoint address would be 00FFFh. Consequently, the corresponding A16:A11 address bits to be loaded into MPR0 would be 000001b.

The four MPRs are each decoded sequentially by the device, starting with MPR0. Each MPR should be set to a Partition Endpoint Address greater than the ending address of the previous MPR. If a higher order MPR sets a Partition Endpoint Address less than or equal to the ending address of a lower-order MPR, that higher order MPR is ignored and no protection is set by its contents.

An example use case is provided in Table 10-1.

Note:	When the Partition Behavior bits are written to 11b, that MPR will become permanently read-only (ROM), and its contents cannot be changed (see Register 10-1).

REGISTER 10-1: MEMORY PARTITION REGISTERS

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PB1	PB0	A16	A15	A14	A13	A12	A11
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **PB[1:0]:** Partition Behavior bits[(1)]

`00` = Partition is open and writing is permitted.
`01` = Partition is always write-protected but can be reversed at a later time (software write-protected).
`10` = Partition is write-protected only when $\overline{WP}$ pin is asserted (hardware write-protected).
`11` = Partition is software write-protected and Memory Partition register is permanently locked.

bit 5-0 **A[16:11]:** Partition Endpoint Address bits[(1, 2)]

`000000` = Endpoint address of partition is set to 0007FFh.
`000001` = Endpoint address of partition is set to 000FFFh.
•
•
•
`111110` = Endpoint address of partition is set to 01F7FFh.
`111111` = Endpoint address of partition is set to 01FFFFh.

Note 1: The Memory Partition registers cannot be written if the FMPC bit has been set.
2: The Partition Endpoint Address bits cannot be written if the PABP bit has been set.

TABLE 10-1: EXAMPLE USE OF MEMORY PARTITION REGISTERS

Register	Content	Partition Behavior Bits (Bit 7-6)	Partition Protection	Register Protection	Partition Ending Address Bits (Bit 5-0)	Partition Ending Memory Address	Partition Size and Address Range
MPR0	43h	`01b`	Software Protection	Unlocked	`000011b`	001FFFh	64-Kbit partition 000000h-001FFFh
MPR1	C4h	`11b`	Software Protection	Locked	`000100b`	0027FFh	16-Kbit partition 002000h-0027FFh
MPR2[(1)]	03h	`00b`	Unprotected	Unlocked	`000011b`	001FFFh	Register ignored
MPR3	8Fh	`10b`	Hardware Protection	Unlocked	`001111b`	007FFFh	176-Kbit partition 002800h-007FFFh

Note 1: In this example, MPR2 is ignored because its Partition Endpoint Address was not greater than the ending address specified by MPR1.

10.1.3 PROTECTING THE PARTITION ENDPOINT ADDRESSES

The 25CSM01 device includes the ability to protect the Partition Endpoint Addresses specified in the device's four MPRs from being modified. When the protection is enabled, the Partition Behavior bits of the MPR can still be modified. As shown in Table 10-2, this function becomes redundant if the FMPC bit in the STATUS register (bit 5, byte 1) is a logic '`1`' as a result of a FRZR sequence (see **Section 10.4 "Freeze Memory Protection Configuration (FRZR)"**) since the FRZR sequence locks all Partition Endpoint Addresses and Partition Behavior bits.

> **Note:** The `PPAB` instruction will be ignored if the WPEN bit (byte 0, bit 7) of the STATUS register is set to logic '`1`' and the $\overline{WP}$ pin is asserted.

Once the Partition Endpoint Addresses are programmed to the desired values, it is recommended that addresses be protected to prevent unintentional modification. This is accomplished by executing the Protect Partition Address Boundary (`PPAB`) instruction which will modify the PABP bit in the STATUS register (bit 3, byte 1).

> **Note:** The starting address of each partition is determined by the endpoint address boundary of the previous partition (00000h for MPR0). Changing the address boundary of an MPR can affect the assigned write-protection behavior for individual array locations by reassigning their associated partition.

TABLE 10-2: MEMORY PARTITION REGISTER PROTECTION MATRIX

FMPC	PABP	Partition Behavior Bits	Partition Endpoint Address Bits
0	0	Writable	Writable
0	1	Writable	Protected
1	x	Permanently-Protected	Permanently-Protected

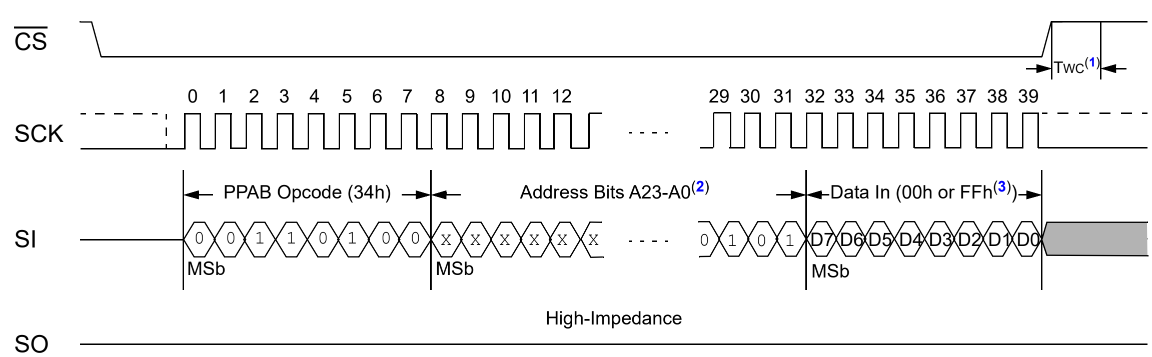
To execute the `PPAB` instruction, first, a `WREN` instruction and then a `PRWE` instruction must be sent to enable write sequences (see **Section 10.2 "Writing to the Memory Partition Registers"**). This will set the WEL and PREL bits to a logic '1'.

Next, as shown in Figure 10-2, the `PPAB` (34h) instruction is clocked in on the SI line, followed by any 24-bit address that ends with CC55h in the Least Significant 16 bits. Finally, a data byte of 00h or FFh is sent, and the self-timed internal write cycle will begin once the $\overline{CS}$ pin is driven high.

Using a data byte of FFh will protect the Partition Endpoint Addresses from being changed by setting the PABP bit in the STATUS register to logic '1'. Sending a data byte of 00h will unprotect these addresses by clearing the PABP bit in the STATUS register to logic '0'.

> **Note:** If the $\overline{CS}$ pin is deasserted before the end of the 40-bit sequence, the sequence will be aborted, and no write cycle will take place.

FIGURE 10-2: PROTECT PARTITION ADDRESS BOUNDARIES (PPAB) SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

2: Address bits A23-A16 are ignored. Address bits A15-A0 must be set to CC55h.

3: A data byte of FFh will set the PABP bit, while a data byte of 00h will clear the PABP bit.

10.1.4 ADDRESS LOCATION OF THE MEMORY PARTITION REGISTERS

When attempting to access any of the device's four MPRs, the address of each MPR is embedded in bit position A16:A15 of the 24-bit address sent to the device.

The remaining 22 address bits (A23-A17 and A14-A0) are ignored. Table 10-3 depicts the values needed to be sent in the A16 through A15 positions.

TABLE 10-3: MEMORY PARTITION REGISTER ADDRESS LOCATION

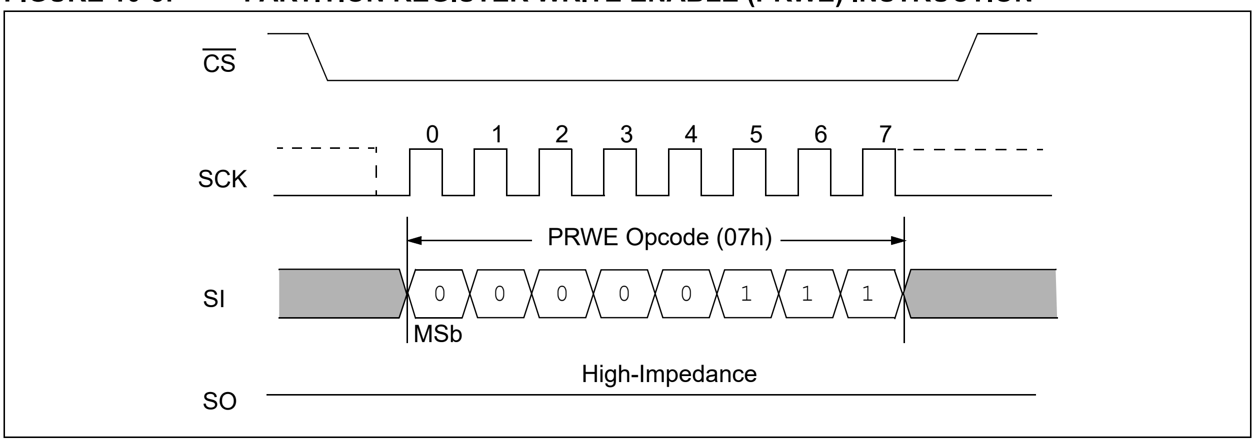
Memory Partition Register Number	A16	A15
MPR0	0	0
MPR1	0	1
MPR2	1	0
MPR3	1	1

10.2 Writing to the Memory Partition Registers

10.2.1 MEMORY PARTITION REGISTER WRITE ENABLE (PRWE)

Prior to any write sequence to protect an address boundary, or `FRZR` instruction, the WEL and PREL bits in the STATUS register must be set to '1'. This is accomplished by first sending a `WREN` (06h) instruction, (see **Section 6.1.3 "Write Enable Latch"**) followed by a `PRWE` (07h) instruction, as shown in Figure 10-3. Once both bits are set to '1', the MPRs can be programmed with the `WMPR` instruction, the Partition Endpoint Addresses can be set with the `PPAB` instruction, or the contents of all MPRs can be permanently locked with the `FRZR` instruction. Upon completion of any of these instructions, the PREL and WEL bits are automatically reset to logic '0'.

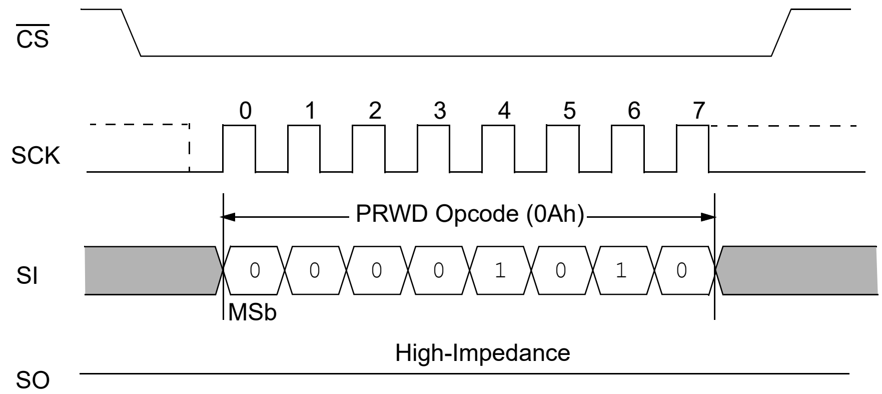
FIGURE 10-3: PARTITION REGISTER WRITE ENABLE (PRWE) INSTRUCTION



10.2.2 MEMORY PARTITION REGISTER WRITE DISABLE (PRWD)

A Partition Register Write Disable (PRWD) instruction is also available (opcode 0Ah), which will reset the PREL bit in the STATUS register to a logic '0' state.

FIGURE 10-4: PARTITION REGISTER WRITE DISABLE (PRWD) INSTRUCTION



10.2.3 WRITING TO THE MEMORY PARTITION REGISTERS

Once the WEL and PREL bits in the STATUS register have been set to '1', the Memory Partition registers can be programmed provided that the FMPC bit in the STATUS register has not already been set to a logic '1' by executing the FRZR sequence (**Section 10.4 "Freeze Memory Protection Configuration (FRZR)"**).

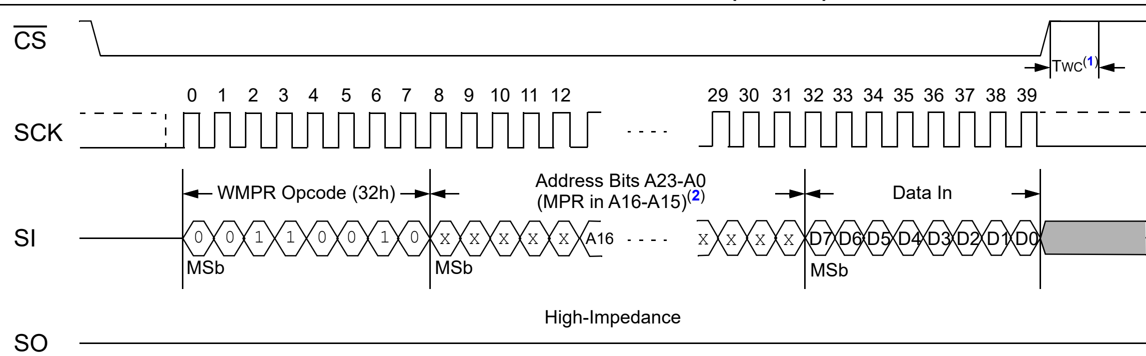
Writing to the MPRs uses the WMPR instruction. To issue the WMPR instruction, the $\overline{CS}$ pin must first be asserted, and then the opcode 32h must be clocked into the device on the SI line, followed by three address bytes containing the Memory Partition register address that corresponds with the desired Memory Partition register number embedded in bits A16 and A15 (Table 10-3).

Following the address information, a data byte using the register definition shown in Register 10-1 must be sent to the device, followed by deasserting the $\overline{CS}$ line. The device will enter an internal write cycle, and once complete, the WEL and PREL STATUS register bits are automatically reset to logic '0'.

Any additional data clocked into the device after the first byte of data will cause the instruction to be ignored, as only one MPR can be programmed at a time. If the sequence is terminated at any point other than an 8-bit boundary, the instruction will be ignored. This sequence is illustrated in Figure 10-5.

The MPR Partition Endpoint Address values must be loaded sequentially in each register as the four MPRs are decoded sequentially by the device, starting with MPR0. If a higher-order MPR sets a Partition Endpoint Address that is less than or equal to the ending address of a lower-order MPR, the higher order MPR is ignored and no behavior is set by its contents.

FIGURE 10-5: WRITE MEMORY PARTITION REGISTERS (WMPR) SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

2: Address bits A23-A17 and A14-A0 are ignored.

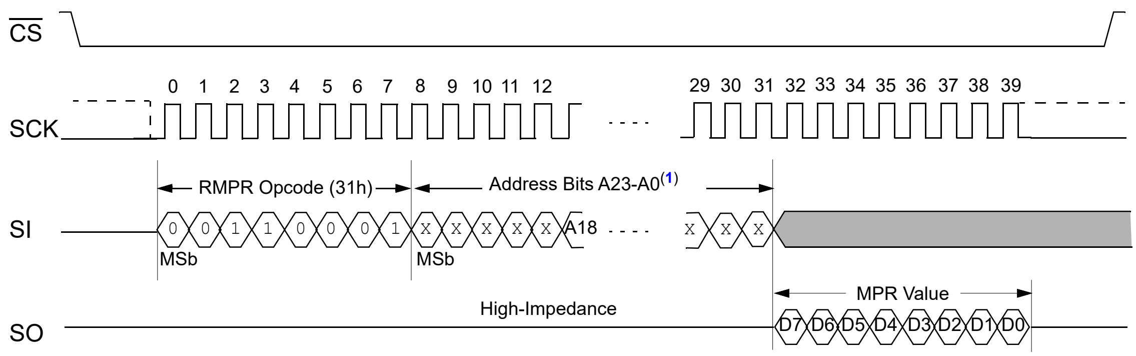
 Preliminary

10.3 Reading the Memory Partition Registers

The contents of the Memory Partition registers can be read with the Read Memory Partition Register (RMPR) instruction. Their contents can be read irrespective of the FMPC bit in the STATUS register.

To determine the MPR contents, the device must first be selected with the CS line, and then the opcode 31h must be clocked into the device on the SI line, followed by the 24-bit Memory Partition register address. The address for each Memory Partition register is embedded into the first address byte sent to the device, in bit positions A16 through A15 (see Table 10-3). The device will then begin to clock data out on the SO line. Only one MPR can be read at a time. This sequence is depicted in Figure 10-6.

FIGURE 10-6: READ MEMORY PARTITION REGISTER (RMPR) SEQUENCE



Note 1: Address bits A23-A17 and A14-A0 are ignored.

10.4 Freeze Memory Protection Configuration (FRZR)

The current state of the Memory Partition registers and Write Protection mode can be permanently frozen so that no further modification of their contents is possible. This is accomplished by the use of the Freeze Memory Protection Configuration (`FRZR`) instruction. For additional information on the Memory Partition registers, refer to **Section 10.0 "Memory Partition Functionality"**.

> **Note:** The Write-Protect Enable (WPEN) and Block Protection (BP[1:0]) bits are not affected by the `FRZR` instruction.

Before a `FRZR` instruction can be issued, first a `WREN` instruction must be issued to set the WEL bit in the STATUS register to a logic '`1`', followed by a `PRWE` instruction to set the PREL bit to a logic '`1`' as well. Once these two steps are complete, the `FRZR` instruction can be sent to the device.

> **Note:** The `FRZR` instruction will be ignored if the WPEN Bit (byte 0, bit 7) of the STATUS register is set to a logic '`1`' and the $\overline{WP}$ pin is asserted.

To freeze the state of the Memory Protection Configuration with the `FRZR` instruction, the CS pin must be driven low, followed by sending an opcode of 37h to the device on the SI line.

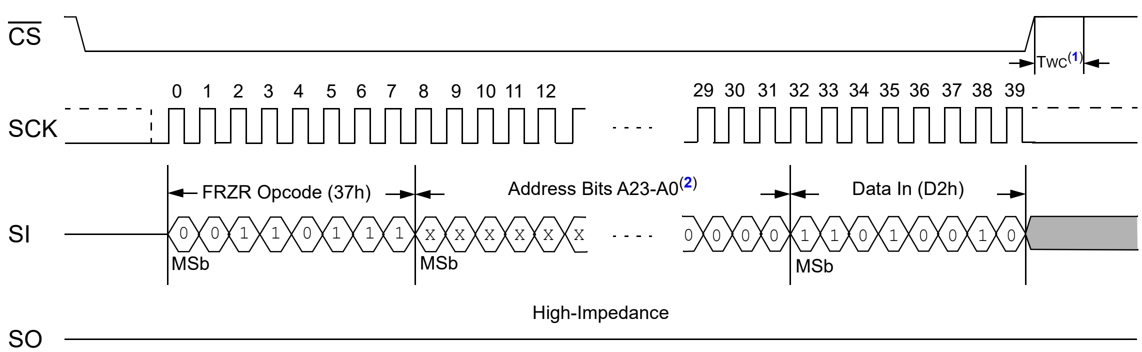
Next, an address of AA40h is sent, followed by a confirmation data byte of D2h. Upon deasserting the $\overline{CS}$ pin, the device will begin a self-timed internal write cycle to set the FMPC bit, freeze all four Memory Partition registers, and the Write Protection Mode (WPM) bit in the STATUS register.

> **Note:** Once the Memory Partition Registers and WPM bit have been frozen, their state cannot be altered.

Once the write cycle is completed, the PREL bit and WEL bit in the STATUS register will be reset back to the logic '`0`' state, the WPM STATUS register bit (bit 7, byte 1) will be permanently set to its current state and the FMPC STATUS register bit (bit 5, byte 1) will be permanently set to a logic '`1`' to indicate that the Memory Protection Configuration has been frozen. If the registers and WPM bit have already been frozen, any attempt to issue the `FRZR` instruction will be ignored. The device will return to the Idle state once the $\overline{CS}$ pin has been deasserted.

> **Note:** If the $\overline{CS}$ pin is deasserted before the end of the 40-bit sequence, the instruction will be aborted, and no write cycle will take place.

FIGURE 10-7: FREEZE MEMORY PROTECTION CONFIGURATION (FRZR) SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

2: Address bits A23-A16 are ignored. Address bits A15-A0 must be set to AA40h.

11.0 PROGRAMMABLE UNDERVOLTAGE LOCKOUT

The 25CSM01 is equipped with an undervoltage lockout detection circuit, which looks for brown-out events or device VCC power supply levels deemed too low for a given application.

To prevent spurious application events that could negatively affect the EEPROM contents of the device, the 25CSM01 employs a circuit that monitors the VCC line voltage. Because the safe power supply voltage level will vary by application, the threshold that defines a brown-out event can be modified in the device from the default level.

11.1 Undervoltage Lockout Detection Register

The 25CSM01 contains a nonvolatile, 8-bit Undervoltage Lockout Detection (UVLO) register that can be modified to change the undervoltage detection threshold (VUVL). When the detector is enabled (bit 5 must be set to logic '1'), the device will sample the VCC supply level upon the detection of the $\overline{\text{CS}}$ pin going high (which starts the internal write cycle) and compare it to VUVL. If VCC remains below VUVL for the minimum UVLO detection time (TUVL) after the CS goes high, the UVLO detection circuit will inhibit the write operation. The WLS bit in the STATUS register can be checked to determine if the previous write sequence was inhibited. If the WLS bit is a logic '1', VCC was less than VUVL and the previous write sequence was inhibited. The WLS bit is only valid if the UVLO function is enabled. See **Section 6.0 "STATUS Register"** for more details.

The instructions that will be inhibited include the following:

- WRITE, WRSR, WREX, LOCK, WMPR, PPAB, FRZR, WUVL

The UVLO register has one bit (UVLOEN) that controls whether the undervoltage detection function is enabled. Five other bits (VUVL[4:0]) determine the undervoltage threshold level. Refer to Table 1-1 for the specific threshold levels.

The STATUS register contains a volatile bit called Write Lockout State (WLS, byte 1, bit 2). If a write sequence to nonvolatile memory is inhibited by the undervoltage lockout detector circuit, the WLS bit will read out as a logic '1'.

The WLS bit will continue to read out a logic '1' until one of the following occurs:

- A Power-on Reset (POR) event occurs (**Section 1.1.1 "Device Power-On Reset"**)
- A nonvolatile write op-code is sent to the device (WRITE, WRSR, WREX, LOCK, WMPR, PPAB, FRZR, WUVL)
- A Software Device Reset (SRST) instruction is executed

The organization of the register is depicted in Register 11-1.

Note:	If the STATUS register is read during the UVLO detection time (TUVL), the device will report a busy state, indicated by RDY/BSY = 1. If the write is inhibited due to the UVLO, the RDY/BSY bit will be cleared, and the WLS bit will be set.

Note:	Setting the undervoltage detection threshold (VUVL) above VCC will cause all write sequences to be ignored. VCC must be above VUVL to reprogram the VUVL.

REGISTER 11-1: UNDERVOLTAGE LOCKOUT DETECTOR REGISTER

U-0	U-0	R/W	R/W	R/W	R/W	R/W	R/W
—	—	UVLOEN	VUVL4	VUVL3	VUVL2	VUVL1	VUVL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **UVLOEN:** Enable Undervoltage Lockout Function
1 = UVLO is enabled
0 = UVLO is not enabled

bit 4-0 **VUVL[4:0]:** Undervoltage Lockout Detection Level[(1)]
00000 = Minimum
•
•
•
11111 = Maximum

Note 1: For specific UVLO levels, refer to Table 1-1.

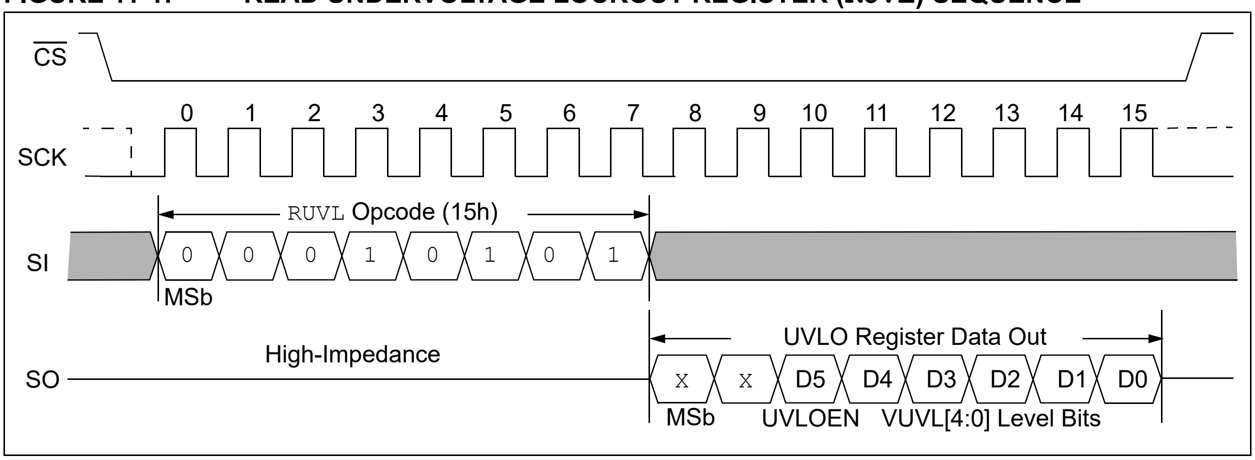
11.2 Accessing the Undervoltage Lockout Register

11.2.1 READING THE UNDERVOLTAGE LOCKOUT DETECTOR REGISTER

Reading the Undervoltage Lockout (UVLO) register is accomplished in a manner similar to reading the STATUS register.

To read the UVLO register, assert the $\overline{CS}$ pin and send the 15h opcode, which corresponds to the RUVL instruction, on the SI pin. Upon completion of the opcode, the device will return the 8-bit register value on the SO pin. The input conditions of the RUVL instruction are illustrated in Figure 11-1.

FIGURE 11-1: READ UNDERVOLTAGE LOCKOUT REGISTER (RUVL) SEQUENCE



11.2.2 WRITING THE UNDERVOLTAGE LOCKOUT DETECTOR REGISTER

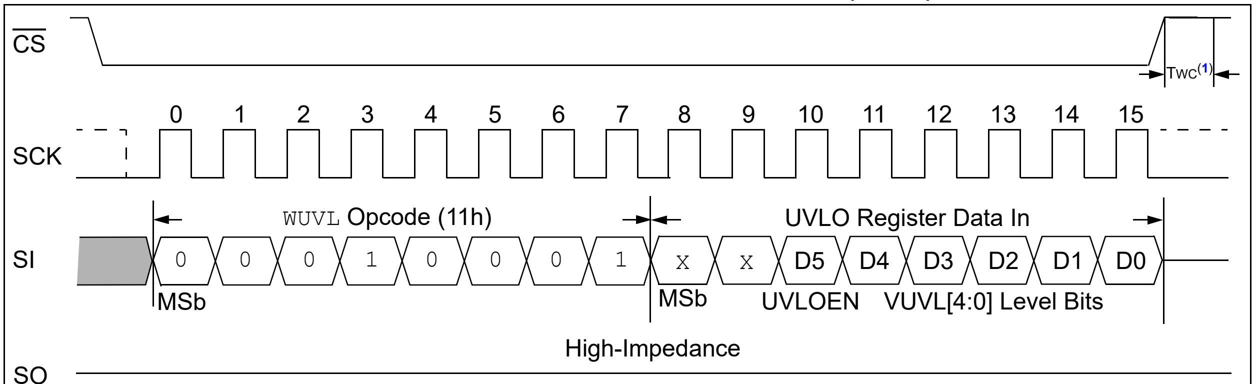
Writing to the UVLO register can be done by using the `WUVL` instruction. However, before a `WUVL` instruction can be initiated, a `WREN` instruction must be executed to set the WEL bit to logic '`1`' (see **Section 8.1.1 "Byte Write"**). The `WUVL` instruction is prevented if WPEN = `1` and $\overline{WP}$ is asserted. Upon completion of a `WREN` sequence, a `WUVL` instruction can be executed.

This begins by driving the $\overline{CS}$ pin low, followed by sending an 11h opcode on the SI pin. Then continue by sending the desired 8-bit UVLO register value.

Note that bits 7 through bit 6 have no function, as shown in Register 11-1. The 25CSM01 will only respond to a `RDSR` or `WRBP` instruction after a `WUVL` sequence until the self-timed internal write cycle has completed, as the UVLO is a nonvolatile register. When the write cycle is completed, the WEL bit in the STATUS register is reset to logic '`0`'. The `WUVL` sequence is depicted in Figure 11-2.

> **Note:** If the $\overline{CS}$ pin is deasserted before the end of the 16-bit sequence, the sequence will be aborted, and no write cycle will take place.

FIGURE 11-2: WRITE UNDERVOLTAGE LOCKOUT REGISTER (`WUVL`) SEQUENCE



Note 1: This sequence initiates a self-timed internal write cycle on the rising edge of $\overline{CS}$ after a valid sequence.

12.0 IDENTIFICATION REGISTER

The Identification register contains identification information that can be read from the device to enable systems to electronically query and identify the 25CSM01 while it is in system.

The identification method and the instruction opcode comply with the JEDEC standard for "Manufacturer and Device ID Read Methodology for SPI Compatible Serial Interface Memory Devices". The type of information that can be read from the device includes the JEDEC-defined Manufacturer ID, the vendor-specific Device ID, and the vendor-specific Extended Device Information (EDI).

12.1 Reading the Identification Register

To read the identification information, the CS pin must first be asserted, and the 9Fh opcode (SPID) must be clocked into the device. After the opcode has been clocked in, the device will begin outputting the identification data on the SO pin during the subsequent clock cycles. The first byte output will be the Manufacturer ID, followed by two bytes of Device ID information.

The fourth byte output will be the Extended Device Information (EDI) String Length which, for the 25CSM01, will be 01h indicating one byte of EDI data follows.

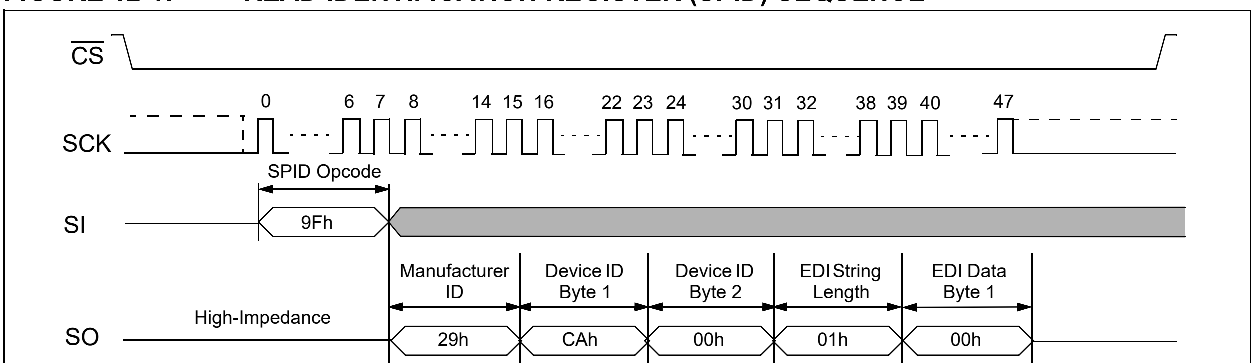
After one byte of EDI data is output, the SO pin will go into a high-impedance state; therefore, additional clock cycles will have no effect on the SO pin, and no data will be output. As indicated in the JEDEC standard, reading the EDI String Length and any subsequent data is optional.

Deasserting the CS pin will terminate the Manufacturer and Device ID read sequence and put the SO pin into a high-impedance state. The CS pin can be deasserted at any time and does not require that a full byte of data be read. This sequence is depicted in Figure 12-1.

MANUFACTURER AND DEVICE ID DETAILS

Data Type	Byte No.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex Value	Details
Manufacturer ID	1	JEDEC® Assigned Code								29h	JEDEC® Code: `0010 1001` (29h for Microchip)
		0	0	1	0	1	0	0	1		
Device ID (Part 1)	2	Family Code			Density Code						
		1	1	0	0	1	0	1	0	CAh	1-Mbit Density Code
Device ID (Part 2)	3	Sub Code			Product Variant						
		0	0	0	0	0	0	0	0	00h	Reserved for Future Use
EDI Length	4	0	0	0	0	0	0	0	1	01h	Indicates one EDI byte
EDI Byte 1 Device Revision	5	0	0	0	0	0	0	0	0	00h	First generation, SPI 1-Mbit device

FIGURE 12-1: READ IDENTIFICATION REGISTER (SPID) SEQUENCE



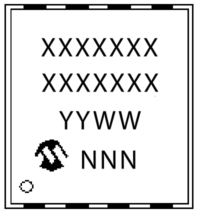
Note: Each transition shown for SI and SO represents one byte (8 bits).

 Preliminary

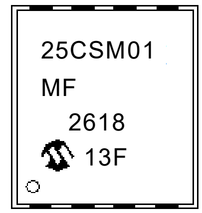
13.0 PACKAGING INFORMATION

13.1 Package Marking Information

8-Lead DFN-S



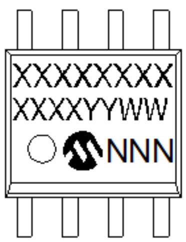
Example



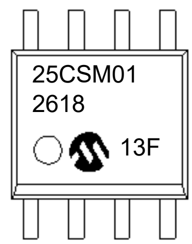
8-Lead MSOP

Example

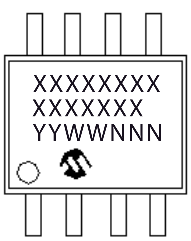
8-Lead SOIC (3.90 mm)



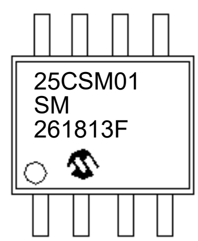
Example



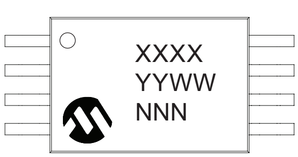
8-Lead SOIJ



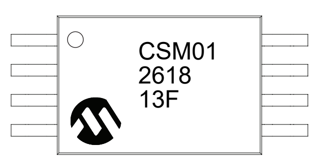
Example



8-Lead TSSOP



Example



Part Number	1st Line Marking Codes				
	DFN-S	MSOP	SOIC	SOIJ	TSSOP
25CSM01	25CSM01	5CSM01	25CSM01	25CSM01	CSM01

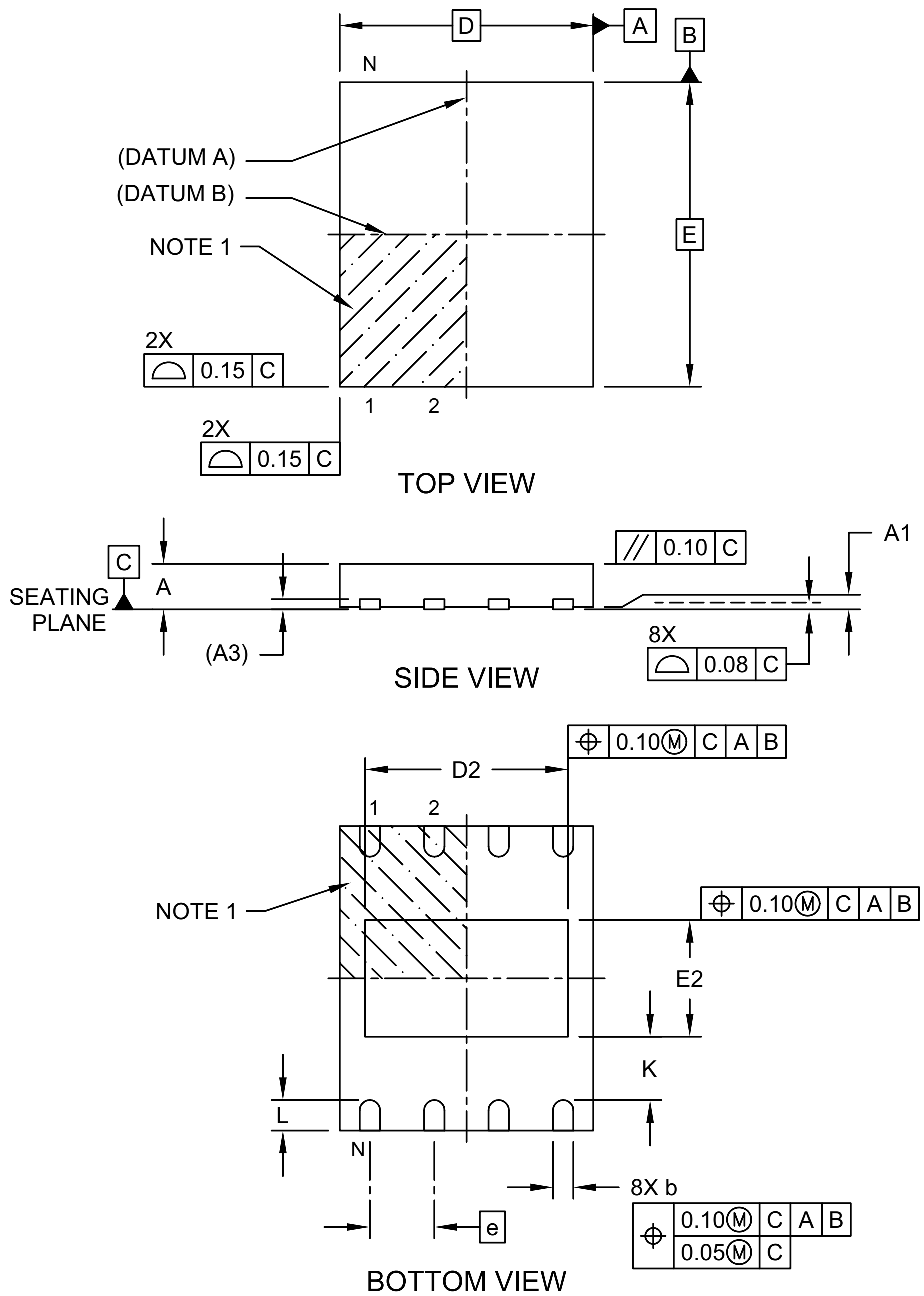
Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code
*	This package is RoHs compliant. The JEDEC® designator can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

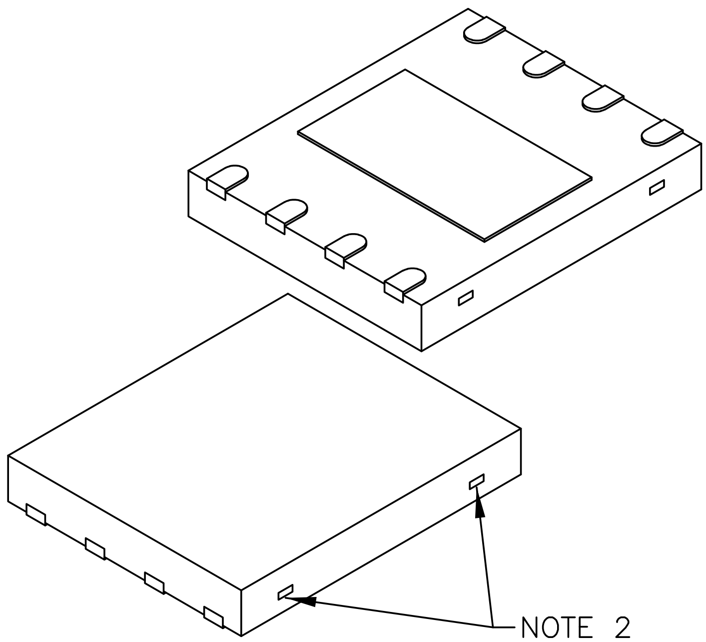
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-122 Rev D Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.90	4.00	4.10
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	2.20	2.30	2.40
Terminal Width	b	0.30	0.40	0.50
Terminal Length	L	0.50	0.60	0.75
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one ore more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

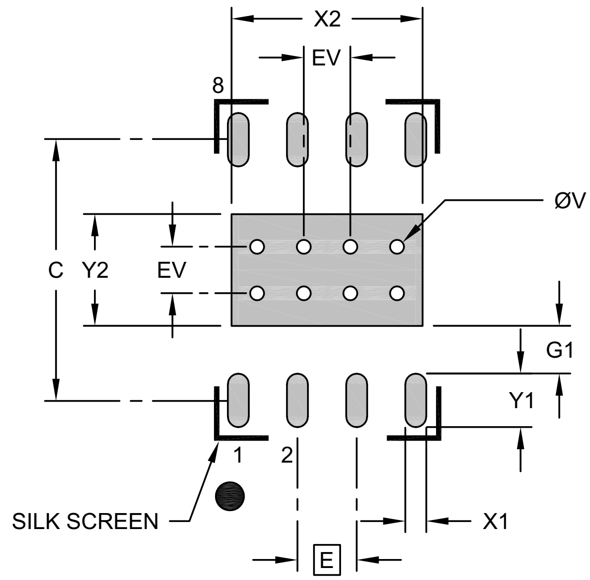
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-122 Rev D Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S] Saw Singulated

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

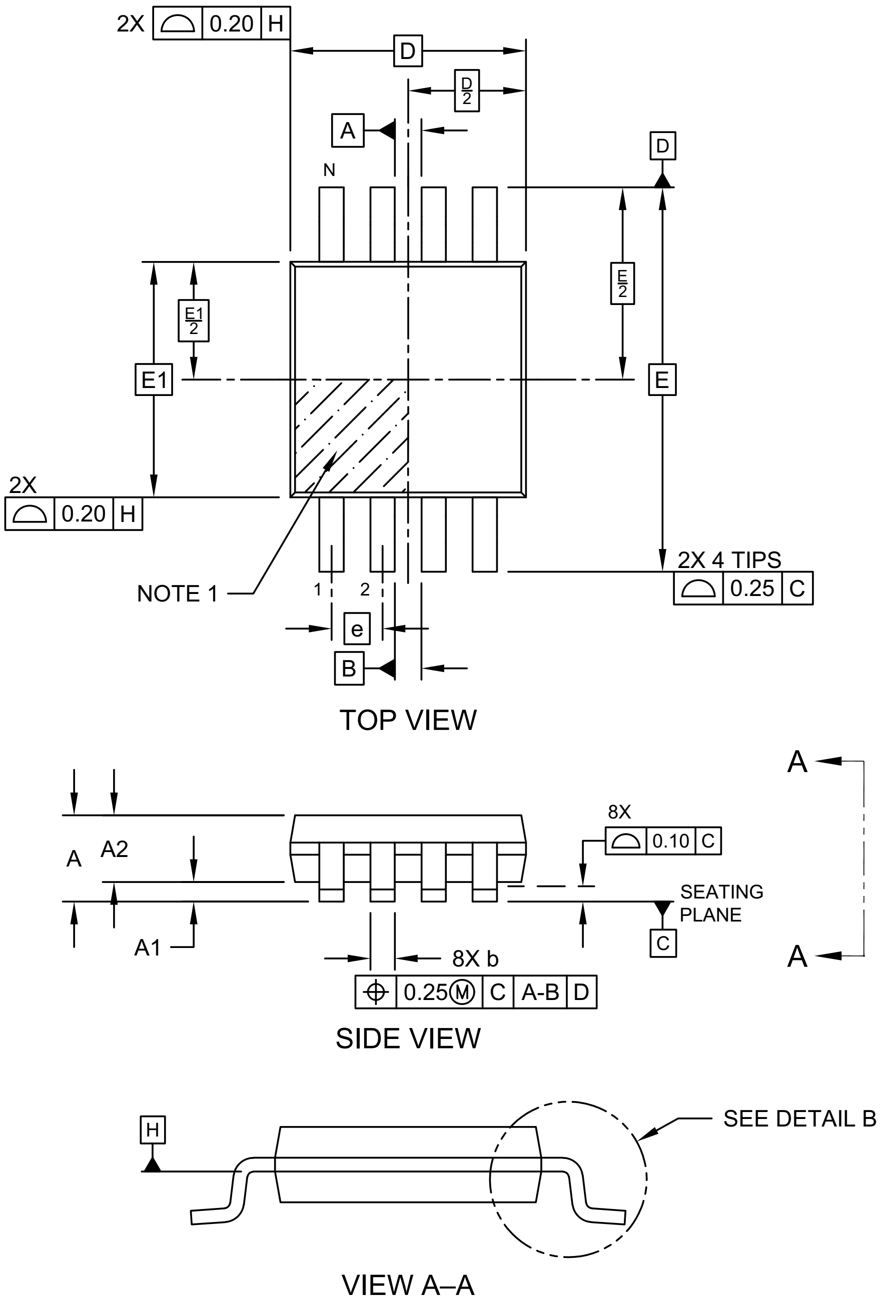
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Length	X2			4.10
Optional Center Pad Width	Y2			2.40
Contact Pad Spacing	C		5.60	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.15
Contact Pad to Center Pad (X20)	G1	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2122 Rev D

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

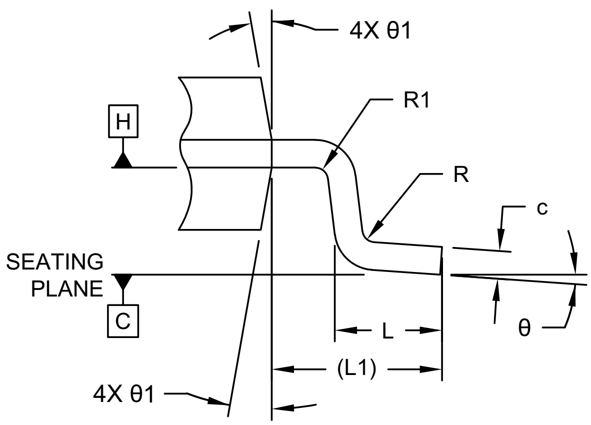
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



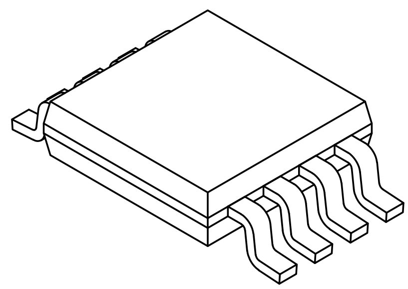
Microchip Technology Drawing C04-111-MS Rev F Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B



		Units	MILLIMETERS	
		Dimension Limits		
		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D		3.00 BSC	
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Terminal Width	b	0.22	–	0.40
Terminal Thickness	c	0.08	–	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

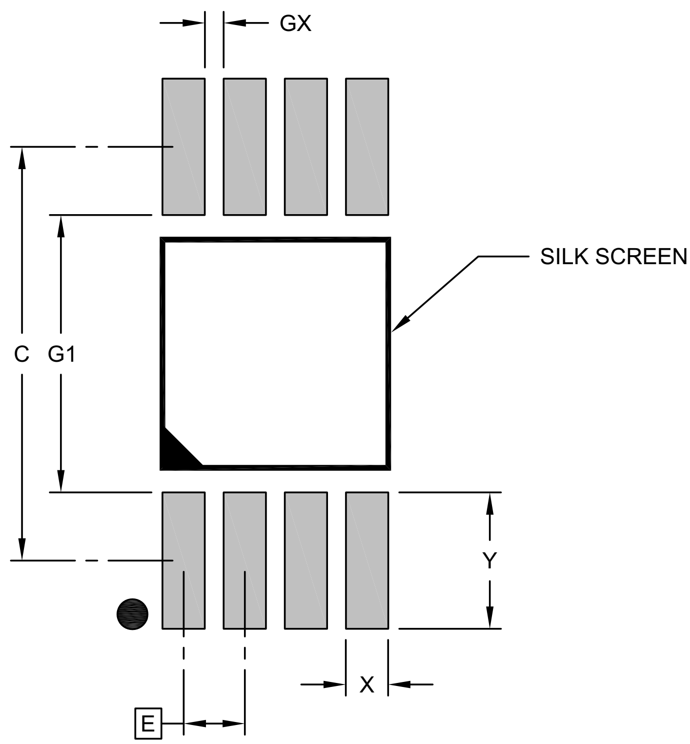
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-MS Rev F Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Contact Pad Width (X8)	X			0.45
Contact Pad Length (X8)	Y			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

Notes:

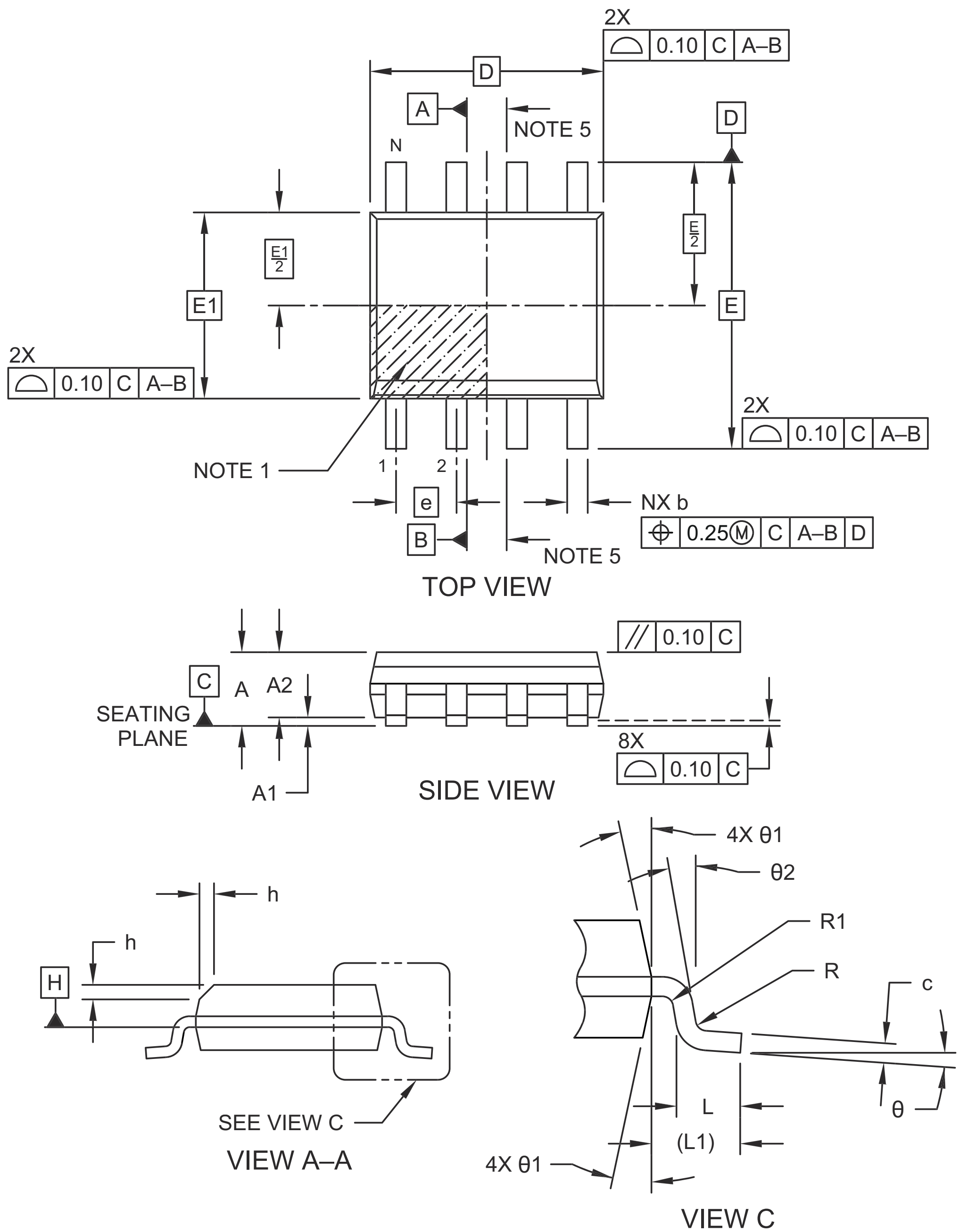
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2111-MS Rev F

 Preliminary

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

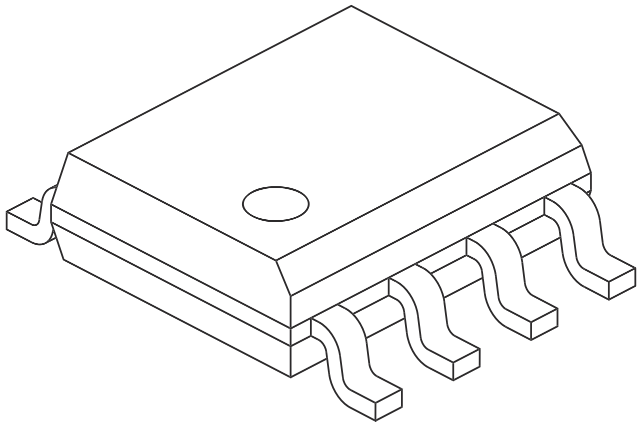
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

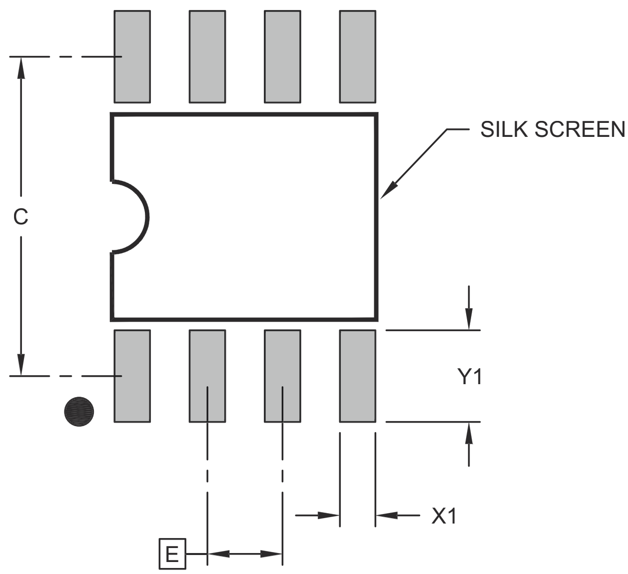
Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

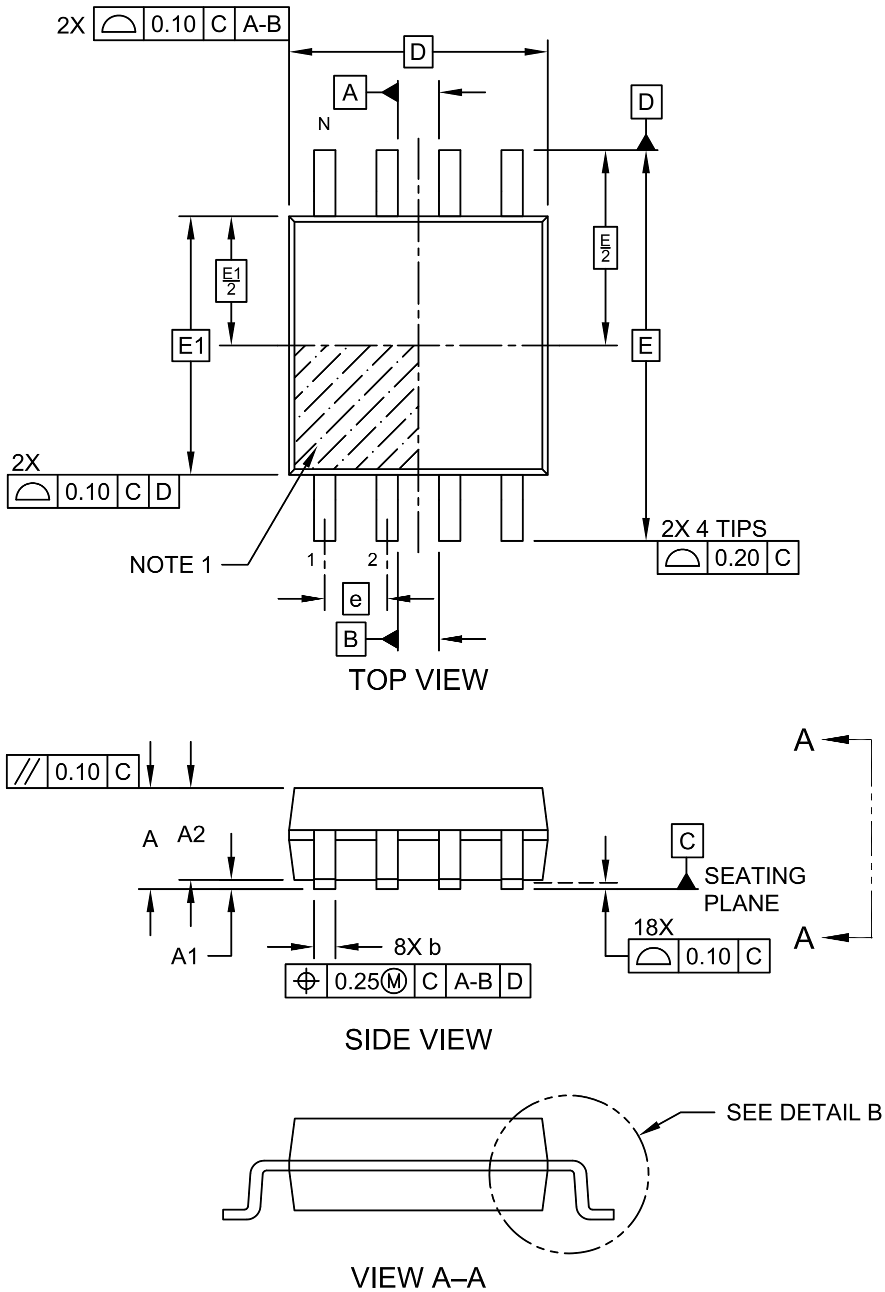
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-02057-SN Rev L

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

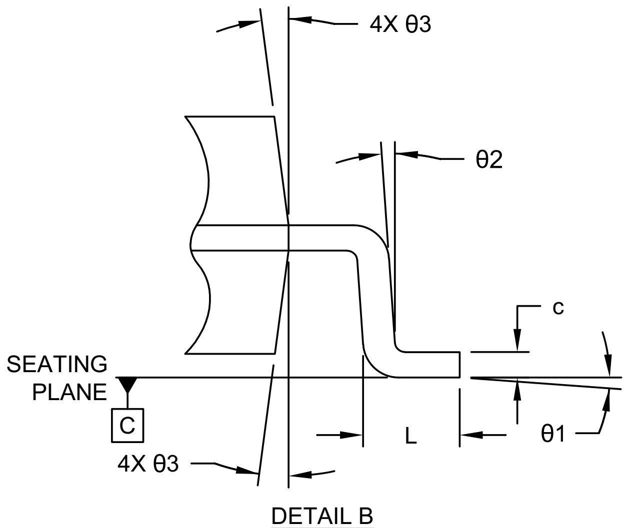


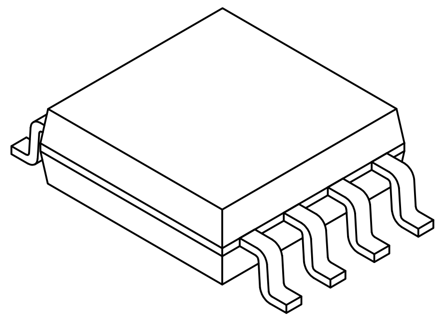
Microchip Technology Drawing C04-056 Rev E Sheet 1 of 2

 Preliminary

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	1.77	–	2.03
Standoff §	A1	0.05	–	0.25
Molded Package Thickness	A2	1.75	–	1.98
Overall Length	D	5.26 BSC		
Overall Width	E	7.94 BSC		
Molded Package Width	E1	5.25 BSC		
Terminal Width	b	0.36	–	0.51
Terminal Thickness	c	0.15	–	0.25
Terminal Length	L	0.51	–	0.76
Foot Angle	θ1	0°	–	8°
Lead Angle	θ2	0°	–	–
Mold Draft Angle	θ3	–	–	15°

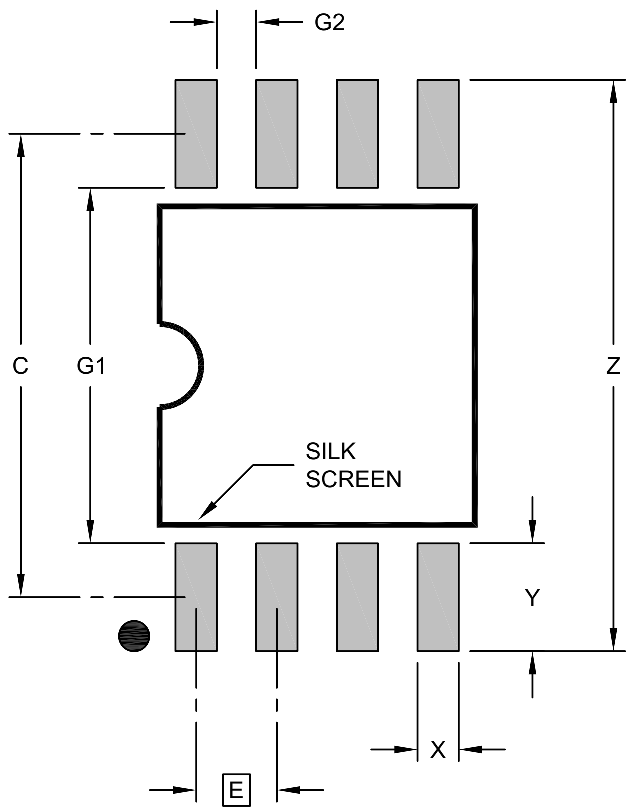
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. SOIJ – JEITA/EIAJ Standard, Formerly called SOIC
3. § – Significant Characteristic
4. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
5. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-056 Rev E Sheet 2 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm (.208 Inch) Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Overall Width	Z			9.00
Contact Pad Spacing	C		7.30	
Contact Pad Width (X8)	X			0.65
Contact Pad Length (X8)	Y			1.70
Contact Pad to Contact Pad (X4)	G1	5.60		
Contact Pad to Contact Pad (X6)	G2	0.62		

Notes:

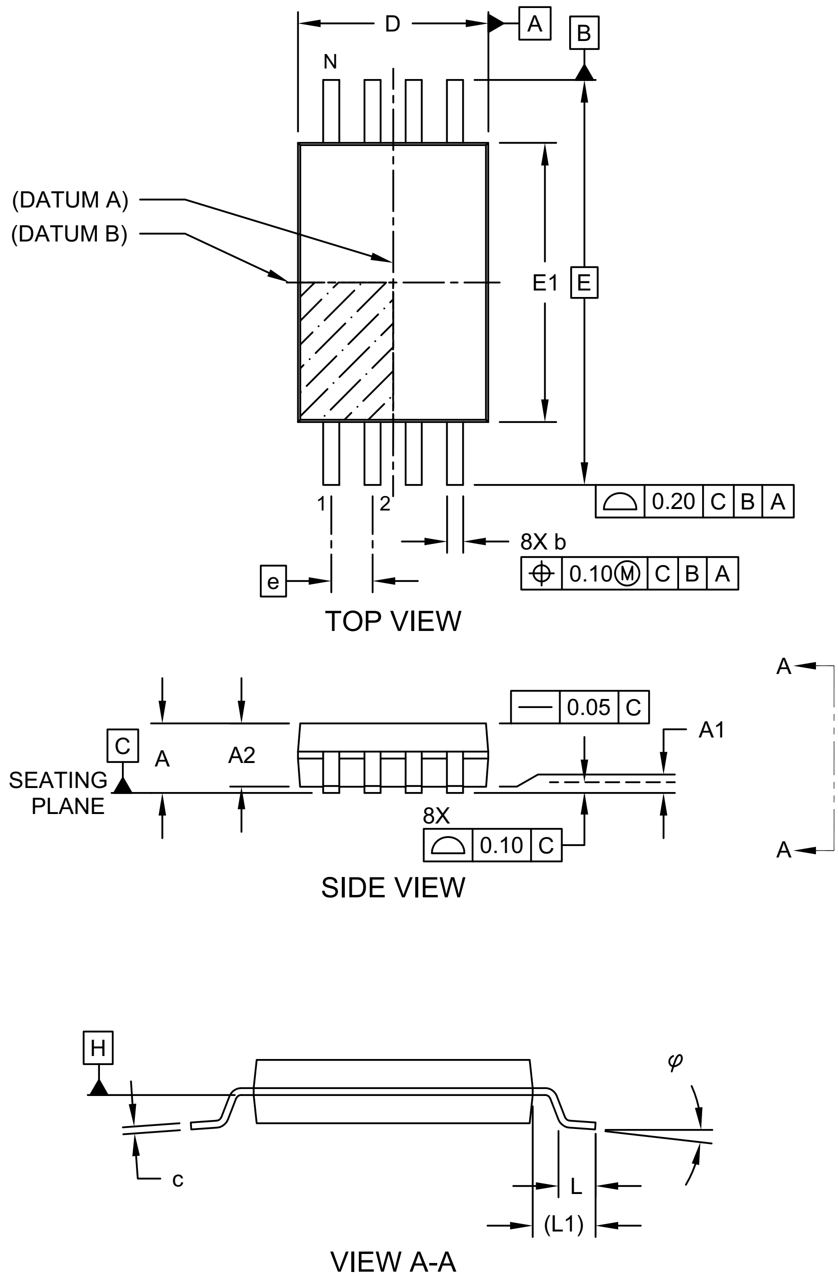
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2056 Rev E

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

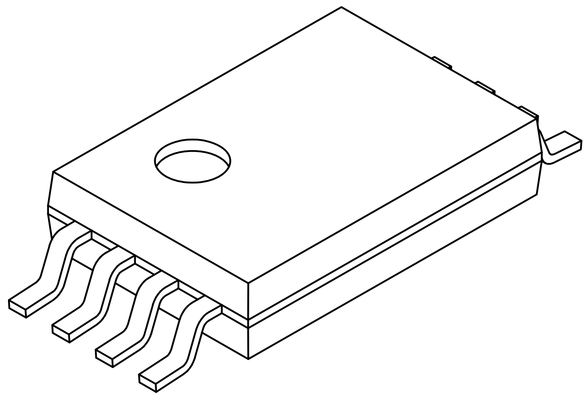
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-086 Rev C Sheet 1 of 2

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	-
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Overall Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Thickness	c	0.09	-	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

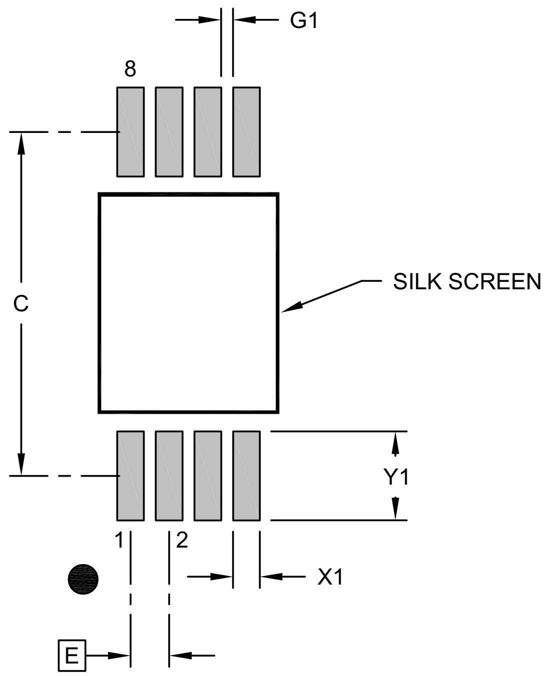
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086 Rev C Sheet 2 of 2

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.80	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.50
Contact Pad to Center Pad (X6)	G1	0.20		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2086 Rev B

APPENDIX A: REVISION HISTORY

Revision B (06/2026)

Removed low voltage UVLO settings; Updated UVLO AC spec.; Minor editorial updates.

Revision A (08/2025)

Initial release of this document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X][(1)]	X	/XX
Device	Tape and Reel Option	Temperature Range	Package

Device:	25CSM01 = 1-Mbit SPI Serial EEPROM with Security Register		
Tape and Reel Option[(1)]:	Blank	=	Standard packaging (tube or tray)
	T	=	Tape and Reel[(1)]
Temperature Range:	I	=	-40°C to +85°C (Industrial)
	E	=	-40°C to +125°C (Extended)
Package:	MF	=	8-Lead Plastic Dual Flat, 6x5 mm No Lead Package (DFN-S)
	MS	=	8-Lead Plastic Micro Small Outline Package, (MSOP)
	SN	=	8-Lead Plastic Small Outline – Narrow 3.90 mm Body (SOIC)
	SM	=	8-Lead Plastic Small Outline Package - Medium 5.28 mm Body (SOIJ)
	ST	=	8-Lead Plastic Thin Shrink Small Outline – 4.4 mm Body (TSSOP)

Examples:

a) 25CSM01T-I/SN: 1-Mbit, 1.7V-5.5V, Tape and Reel, Industrial Temp., SOIC package.

b) 25CSM01-E/SN: 1-Mbit, 1.8V-5.5V, Extended Temp., SOIC package.

c) 25CSM01T-I/MS: 1-Mbit, 1.7V-5.5V, Tape and reel, Industrial Temp., MSOP package.

d) 25CSM01T-E/ST: 1-Mbit, 1.8V-5.5V, Tape and reel, Extended Temp., TSSOP package.

e) 25CSM01-I/SM: 1-Mbit, 1.7V-5.5V, Industrial Temp., SOIJ package.

f) 25CSM01-E/MF: 1-Mbit,1.7V-5.5V, Extended Temp., DFN-S package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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