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156.25MHz Ultra-Low RMS Jitter XOs

Performance Study

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Introduction

Over time, system clock jitter requirements have become stringent. Most require an upper limit of 200fs maximum RMS jitter over 12kHz to 20MHz bandwidth at 156.25MHz carrier. Recognizing this ever-increasing market demand for ultra-low RMS jitter clocking solutions, Abracon continues its quest of enhancing the performance characteristics of its solutions while simultaneously reducing form factors.

There are four fundamental ways to design a 156.25MHz clock oscillator:

A. Quartz oscillator utilizing an inverted mesa quartz blank as the resonator element
B. Quartz oscillator utilizing a third overtone quartz blank as the resonator element
C. Oscillator loop based on a sub-50MHz third overtone / fundamental mode quartz blank or a sub-50MHz temperature-compensated crystal oscillator mated with an integer or fractional mode phase-locked-loop [PLL] IC
D. Sub-50MHz MEMS resonator-based oscillator loop mated with an integer or fractional mode phase-locked loop [PLL] IC

Option A neither yields the best RMS jitter performance nor is the lowest cost solution. The MEMS resonator-approach [Option D] does not meet the primary performance criteria of 200fs maximum RMS jitter. Option B utilizes an optimally designed third overtone quartz blank with considerations given to the geometry of the electrodes and the optimization of the angle of cut, which provides the best convergence in cost, performance and size.

Abracon's AK2, AX3, AK5 and AK7 ClearClock™ crystal oscillator (XO) solutions are designed with third overtone, high-Q quartz blanks using a specific angle of cut to satisfy the stringent frequency stability requirements over the extended operating temperature range of -40^{0}C to +85^{0}C. These solutions offer superior RMS jitter performance – predominantly exceeding system-level requirements.

Additionally, Abracon investigated, analyzed, designed and produced its ASGTX5 series of temperature-compensated crystal oscillator (TCXO) devices utilizing Option C to address both over-temperature and long-term stability requirements of Stratum-IV architectures.

Third Overtone ClearClock™ XO Series

The ClearClock™ family of crystal oscillators is particularly suited for optical transceivers and data center architectures, which predominantly employ a 156.25MHz local oscillator with superior phase noise and RMS jitter performance as the system clock in 10G, 40G, 100G and upcoming 400G systems.

Abracon recently introduced its AK2 series of ClearClock™ oscillators, which are housed in a miniature ceramic package that measures a mere 2.5 x 2.0 x 1.0 mm. With the addition of the AK2 series to the ClearClock™ family, Abracon now offers a full line of superior jitter performance quartz oscillator solutions in the industry standard 5.0 x 7.0, 5.0 x 3.2, 3.0 x 2.5 and 2.5 x 2.0 mm package sizes. See Table 1.

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Series	Package Size (mm)	Standard Available Frequencies (MHz)	Typ / Max RMS Jitter @ 156.25 MHz	OTR	Stability Over OTR
AK2	2.5 x 2.0 x 1.0	100, 125, 148.5, 156.25, 200	< 110 / 200 fs (LVPECL & LVDS, +2.5V)	-40°C to +85°C	±30 ppm
AX3	3.2 x 2.5 x 1.0	100, 114.285, 122.88, 125, 148.5, 150, 155.52, 156.25, 200, 212.5	< 75 / 150 fs, (LVECL, +3.3V) < 110 / 150 fs, (LVDS, +3.3V)	-40°C to +85°C	±20 ppm
AK5	5.0 x 3.2 x 1.3	100, 122.88, 125, 148.5, 156.25, 200	< 75 / 100 fs, (LVECL, +3.3V) < 90 / 115 fs, (LVDS, +3.3V)	-40°C to +85°C	±20 ppm
AK7	5.0 x 7.0 x 1.8	100, 122.88, 125, 148.5, 156.25, 200, 212.5	< 75 / 100 fs, (LVPECL & LVDS +3.3V)	-40°C to +85°C	±20 ppm

Table (1)

These third overtone ClearClock™ solutions are designed with a specific angle of cut to satisfy the stringent frequency stability requirements over the extended operating temperature range of -40°C to +85°C. Figures 1- 4 below outline the performance of AK2, AX3, AK5 and AK7 devices at the 156.25MHz resonant frequency over temperature.

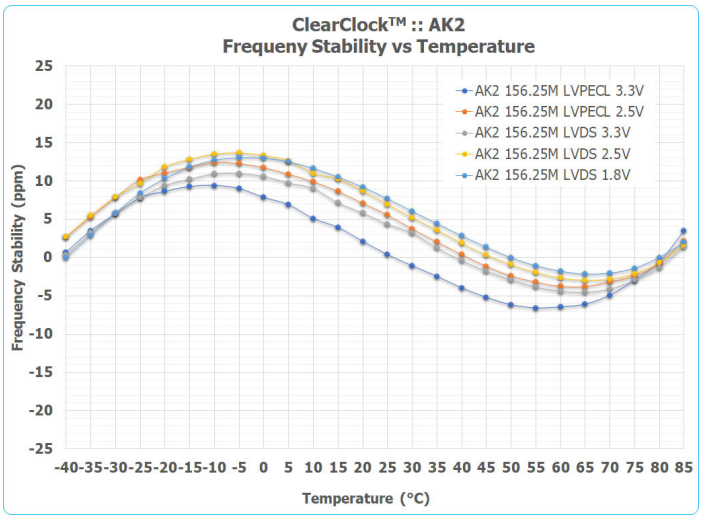

Figure (1)

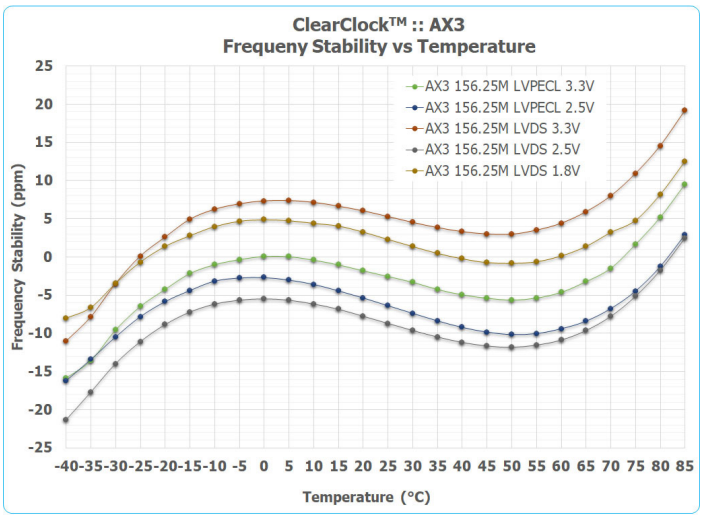

Figure (2)

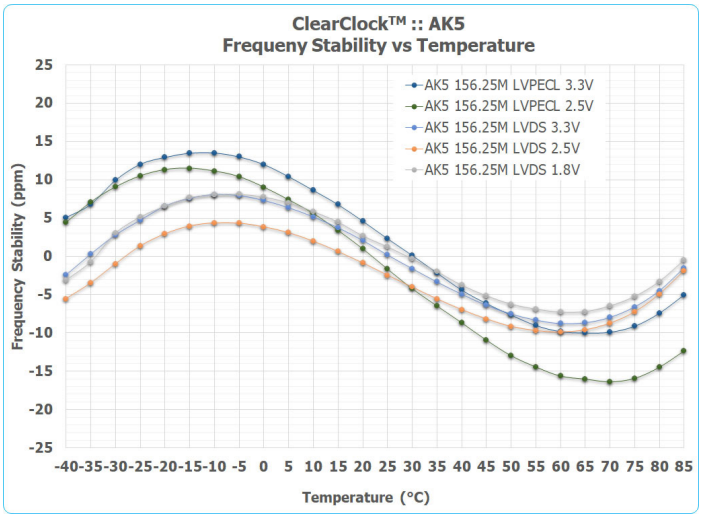

Figure (3)

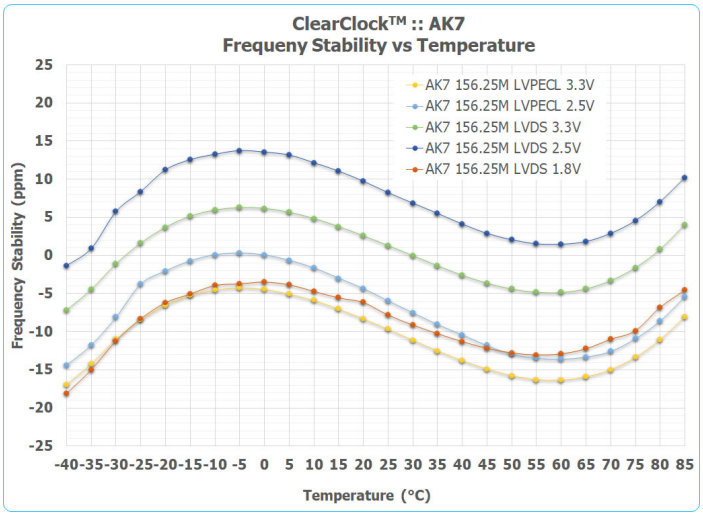

Figure (4)

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Single sideband phase noise characteristics and the associated RMS jitter provide the ClearClock™ family's key performance advantage. In Figure 5, the typical AK2 [2.5 x 2.0 x 1.0 mm] phase noise performance is outlined with both the LVPECL and the LVDS output formats at all available V_{dd} levels.

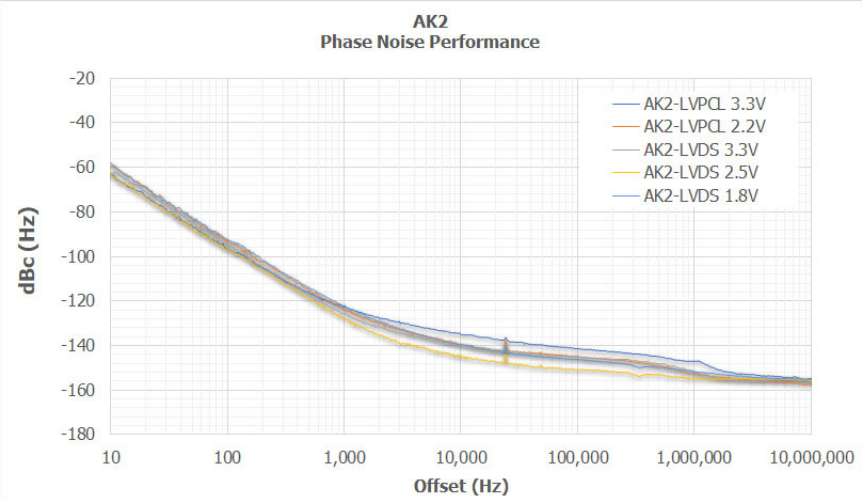

Figure (5)

Figures 6 summarizes the typical phase noise performance of an AX3 [3.2 x 2.5 x 1.0 mm] device with both the LVPECL and the LVDS output formats at all available V_{dd} levels.

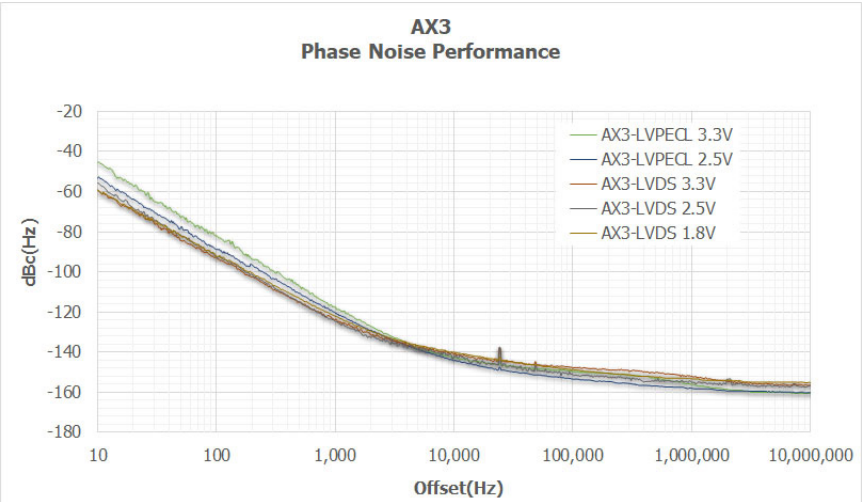

Figure (6)

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Figures 7 summarizes the typical phase noise performance of an AK5 [5.0 x 3.2 x 1.3 mm] device with both the LVPECL and the LVDS output formats at all available V_{dd} levels.

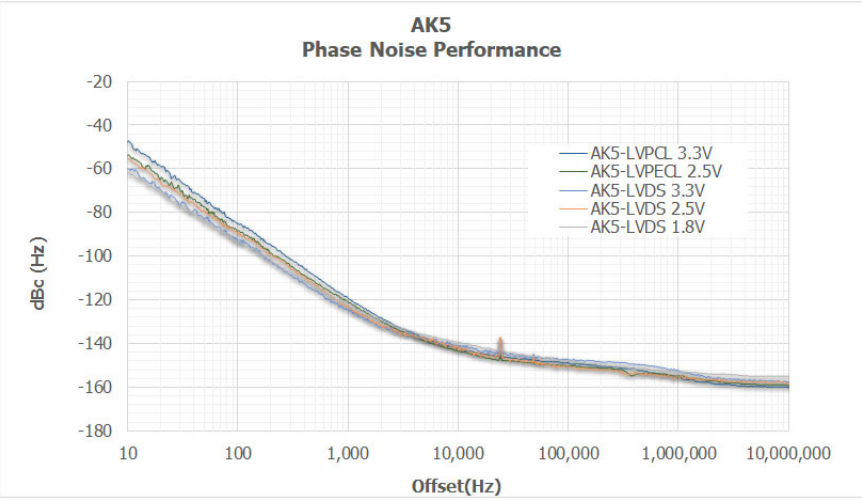

Figure (7)

Figure 8 summarizes the typical phase noise performance of an AK7 [5.0 x 7.0 x 1.8 mm] device with both the LVPECL and the LVDS output formats at all available V_{dd} levels.

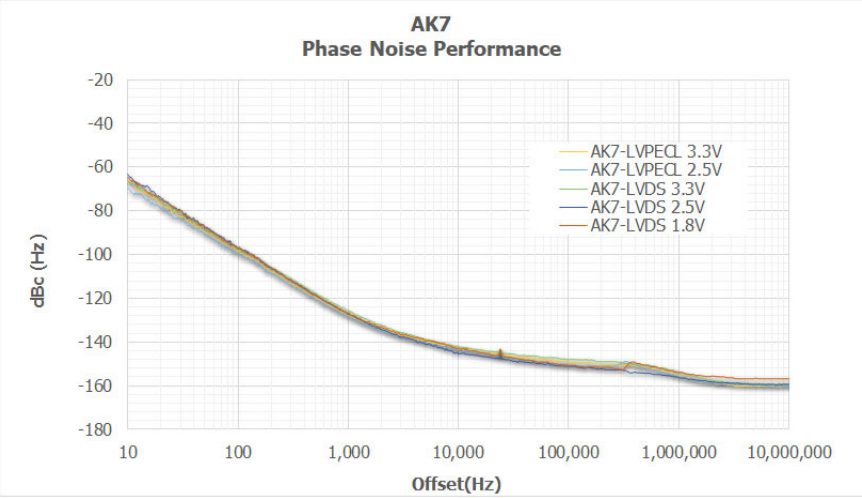

Figure (8)

Table 2 summarizes the typical RMS jitter performance of the four primary offerings within the ClearClock™ family at the 156.25MHz carrier. As evident below, this family of devices is optimally designed to meet the challenging RMS jitter requirements of today's optical transceivers, data centers,

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instrumentation applications and other precision verticals requiring data rates of 10, 40, 100, 200 and 400Gbps.

	Typical RMS jitter (fs) over 12kHz to 20MHz BW: 156.25MHz Carrier				
	LVDS			LVPECL	
Series	+1.80V	+2.5V	+3.3V	+2.5V	+3.3V
AK2	135.379	104.137	126.152	106.429	140.932
AX3	115.788	92.354	109.192	63.377	69.487
AK5	119.051	105.294	87.761	77.743	72.598
AK7	124.294	74.518	81.710	74.129	74.457

Table (2)

The AK2, AX3, AK5 and AK7 solutions offer superior RMS jitter performance that is well below the typical system-level maximum requirement of 200fs.

For systems that require guaranteed RMS jitter performance of 100fs maximum, both the AK5 and the AK7 solutions meet this requirement with either the LVDS or the LVPECL output format when biased at +3.3V.

ASGTX5 TCXO Series

In addition to the standard frequency [non-factory-configurable] ClearClock™ solutions, Abracon has developed the ASGTX5 series to address the Stratum-IV clocking systems that have an all-inclusive total stability requirement of ±32ppm maximum. This requirement is inclusive of initial set-tolerance, shift through reflow, frequency pulling and pushing, frequency stability over -40°C to +85°C, and long-term aging (20 years).

The ASGTX5 temperature-compensated crystal oscillator (TCXO) solution meets this stringent requirement at any carrier frequency between 15.0MHz and 2.1GHz. However, to achieve that precision, this solution has slightly worse RMS jitter than its third overtone ClearClock™ counterparts. For instance, it exhibits < 350fs typical RMS jitter at 156.25MHz carrier.

The ASGTX5 is available with CML differential output format in addition to the standard LVDS, LVPECL and HCSL offerings. System architectures requiring a CML output type can certainly benefit from the ASGTX5 series.

Series	Package Size (mm)	Standard Available Frequencies (MHz)	Typ / Max RMS Jitter @ 156.25 MHz	OTR	Stability Over OTR
ASGTX5	5.0 x 3.2 x 1.5	Any frequency between 15.0 MHz and 2.1 GHz (factory programmable)	< 350 fs typcial @ +3.3V (LVDS/LVPECL/HCSL/CML)	-40°C to +85°C	±3 ppm

Table (3)

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Although specified for a guaranteed maximum error of ±3.0 ppm over -40°C to +85°C, the ASGTX5 devices typically hold better than ±1.0 ppm accuracy over this extended operating temperature range. Figure 9 below outlines the stability over temperature performance of ASGTX5 devices at 156.25MHz carrier.

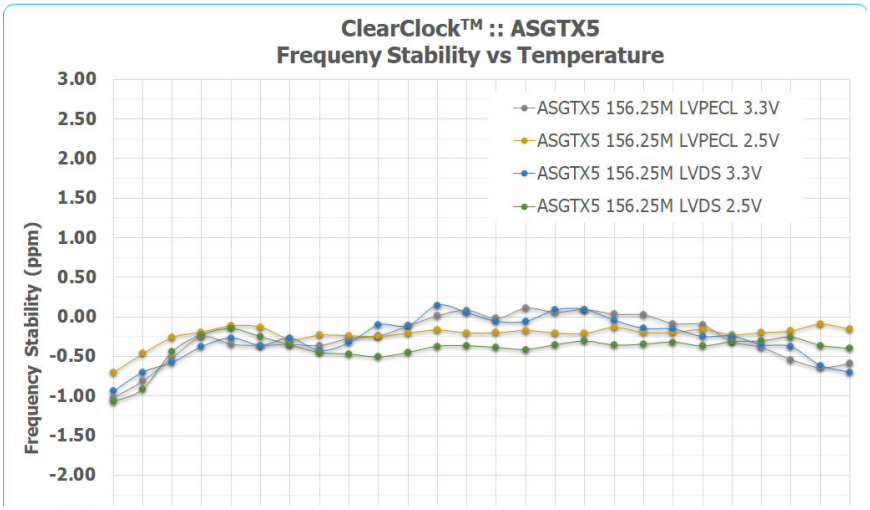

Figure (9)

Figures 10 summarizes the typical phase noise performance of an ASGTX5 TCXO [5.0 x 3.2 x 1.5 mm] device with both the LVPECL and the LVDS output formats at all available V_{dd} levels.

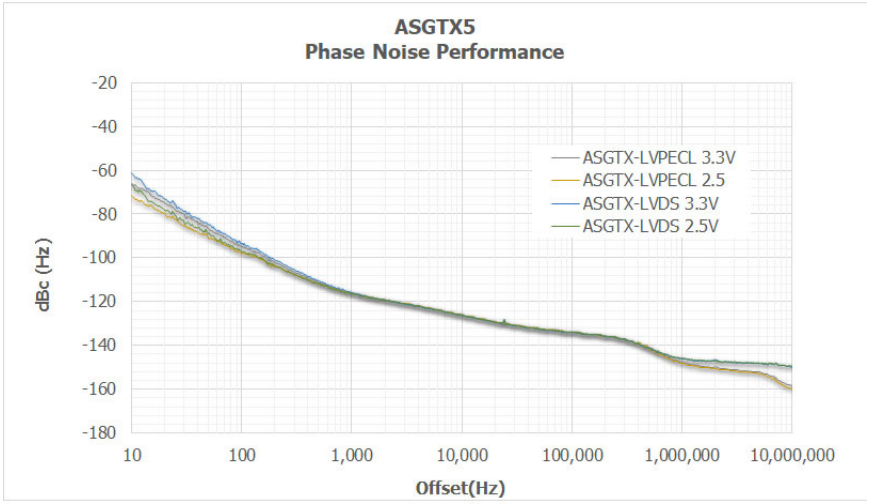

Figure (10)

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Although the ASGTX5 is a temperature-compensated solution, Abracon has instituted specific design techniques to maintain superior RMS jitter performance, as outined in Table 4 below.

	Typical RMS jitter (fs) over 12kHz to 20MHz BW: 156.25MHz Carrier				
	LVDS			LVPECL	
Series	+1.80V	+2.5V	+3.3V	+2.5V	+3.3V
ASGTX5		298.075	295.860	199.548	212.306

Table (4)

Summary

Table 5 reviews the RMS jitter performance characteristics of the Abracon solutions discussed in this whiter paper.

	Typical RMS jitter (fs) over 12kHz to 20MHz BW: 156.25MHz Carrier				
	LVDS			LVPECL	
Series	+1.80V	+2.5V	+3.3V	+2.5V	+3.3V
AK2	135.379	104.137	126.152	106.429	140.932
AX3	115.788	92.354	109.192	63.377	69.487
ASGTX5		298.075	295.860	199.548	212.306
AK5	119.051	105.294	87.761	77.743	72.598
AK7	124.294	74.518	81.710	74.129	74.457

Table (5)

As evident, these devices are optimally designed to meet the challenging RMS jitter requirements of today's precision applications requiring data rates of 10, 40, 100, 200 and 400Gbps.

In continuation of Abracon's long-standing strategy of offering performance-differentiated solutions, specifically addressing ultra-low RMS jitter clocking requirements, the devices discussed in this white paper cover all popular packaging options and RF output formats.

The AK5 and AK7 solutions are optimal for systems requiring a guaranteed RMS jitter of 100fs maximum at the 156.25MHz carrier when biased at +3.3V. These solutions are available in 5.0 x 3.2 mm and 5.0 x 7.0 mm packages, respectively. If a design has real estate challenges, then either the AX3 [3.2 x 2.5 x 1.0 mm] or the AK2 [2.5 x 2.0 x 1.0 mm] make ideal choices, offering a maximum RMS jitter performance of 150fs and 200fs, respectively. The AK2, AX3, AK5 and AK7 devices are all available in standard industry output formats of LVDS, LVPECL or HCSL.

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The ASGTX5 series is available in a 5.0 x 3.2 x 1.8 mm SMT package, which exceeds the Stratum-IV requirements of ±32 ppm all-inclusive stability. Even with built-in temperature compensation, this series of devices exhibits a typical RMS jitter performance of <350fs at the 156.25MHz carrier. Additionally, the ASGTX5 is available in all four standard differential output formats (LVDS, LVPECL or CML) at any carrier frequency between 15MHz and 2.1GHz as well as up to 700MHz in the HCSL format. This series is ideally suited for systems that either require stringent frequency accuracy, high carrier frequency [such as 1.00GHz] or CML differential output.

All five offerings detailed in this white paper are in stock and available via Abracon's global distribution network.

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