MICROCHIP

AN2587

EMI, EMC, EFT, and ESD Circuit Design Consideration for 32-bit Microcontrollers

Introduction

This application note is intended to provide recommendations concerning incorporation of circuit protection devices and PCB layout guidelines to enhance an application's immunity in electrically noisy environments and survivability of EMI, EMC, EFT, and ESD events as described in the International Electrotechnical Commission (IEC) standards: IEC 61000-4-2, IEC 61000-4-4, and IEC 61000-4-5.

We will begin with:

1. A brief review of EMI, EFT, and ESD specifications.
2. Key ESD protection device specifications definitions.
3. A quick summary of EMI, EFT, and ESD protection strategies.
4. Capacitor filter selection and characteristics.
5. PCB Hardware design best practices and layout considerations checklists:
   - Standard PCB design/layout practices
   - Special Ethernet layout considerations
   - Special DDR Layout considerations
6. Software protection techniques.
7. Microcontroller reference circuit schematics with protection examples:
   - RS-232
   - USB
   - CAN FD and LIN
   - Ethernet
   - Audio and mechanical switches
   - LCD
   - Power supplies
   - Reset and ICSP programming interface
   - SD memory card
   - I^2C

Reference Designs Note:

Cost pressure is a constant consideration in any design. All of the circuit components in support of the CPU were selected based on the lowest cost and availability, which met the threat protection requirements. A user should carefully consider any substitutions. It is also highly recommended that the user consider designing in the protection elements in their layout, and then depopulate with zero ohm resistors as they think necessary, based on ESD, EMI, and EFT prototype board testing. This will save significant board redesign time to market in the final product.

Increasingly, application design requirements call for robust reliable operation in electrically noisy environments and immunity to high-voltage discharge events to meet IEC 61000-4-2, IEC 61000-4-4, and IEC 61000-4-5 requirements. As a result, many consumer, most commercial and all life/mission critical applications typically require conformance to one or more of the IEC 61000-4-2, IEC 61000-4-4, and IEC 61000-4-5 standards related to ESD, EFT, and EMI testing. The task is sometimes made more challenging because designers must contend not just with obvious external events, but in some cases, the forgotten sources from components within their own design. Increasing levels of silicon density/integration coupled with very high operating speeds can create conditions such that the components themselves become sources of conducted and radiated noise, putting additional demands on the application, which affects circuit reliability and interference. Furthermore, an unsuspecting designer can be misled by component manufacturer claims that a particular device meets IEC61000-4-2 specifications, which will be discussed in a subsequent section.

Table of Contents

1. IEC 61000-4-2, IEC 61000-4-4, and IEC 61000-4-5 Definitions

The following table lists and describes each International Electrotechnical Commission (IEC) standard. Refer to the following website for more information: http://www.iec.ch/emc/basic_emc/basic_61000.htm.

Table 1-1. IEC 61000-4-2, IEC 61000-4-4, and IEC 61000-4-5 Standard Definitions

Standard	Description
IEC 61000-4-2	Electrostatic Discharge (ESD) Immunity Test
IEC 61000-4-4	Electrical Fast Transient (EFT) Burst Immunity Test
IEC 61000-4-5	Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC) Lightning/ Surge Immunity Test

There are five categories of failure modes for ICs as specified in IEC 62132-1 and shown in Table 1-2. The classification is determined by the performance of the IC in the presence of the ESD or EFT. This performance is dependent on the type of IC, and its functional behavior as defined in its data sheet.

Table 1-2. Classification of IC Performance Degradation

CLASS	Description
A	All functions of the IC perform as designed during and after exposure to a disturbance.
B	All functions of the IC perform as designed during exposure; however, one or more of them may go beyond the specified tolerance. All functions return automatically to within normal limits after the disturbance is removed. Memory functions shall remain Class A.
C	A function of the IC does not function as designed during exposure but returns automatically to normal operation after the disturbance is removed.
D	A function of the IC does not function as designed during exposure and does not return to normal operation until the disturbance is removed and the IC is reset by simple operator action.
E	One or more functions of the IC do not perform as designed during and after exposure and cannot be returned to normal operation.

2. Electrostatic Discharge (ESD) IEC 61000-4-2

Most digital non-interface components and microcontrollers are only warranted for 2 kV Human Body Model (HBM). This is acceptable in most cases for interconnected signals between ICs on the same printed circuit board (PCB) that share the same ground. High risk exceptions are microcontroller peripheral pins with either direct external PCB connections, mechanical connectors, and/or remote cabled communications, such as USB, LCD, SD, etc. Off-chip microcontroller transceivers ICs, such as CAN and TCP/IP have much higher native ESD HBM protection than the parent microcontroller, but again in some cases, they do not rise to the level to meet all IEC 61000-4-2 standards. They should be reviewed as needed for the appropriate HBM or IEC 61000-4-2 requirements based on the application. Unless the target silicon specifically states it is tested to IEC 61000-4-2, users should assume its standard HBM or contact the manufacturer for clarification. Again, even though some device manufactures may claim they meet IEC 61000-4-2 voltage level specification, they may not meet both voltage and current requirements, as described in Table 2-2.

Table 2-1. IEC 61000-4-2 Voltage Severity Test Levels

Level	Relative Humidity	Anti-static Material	Synthetic Material	Test Voltage (Contact Discharge)	Test Voltage (Air Discharge)
1	35 %	X	–	2 kV	2 kV
2	10 %	X	–	4 kV	4 kV
3	50 %	–	X	6 kV	8 kV
4	10 %	–	X	8 kV	15 kV

Table 2-2. IEC 61000-4-2 Contact Discharge Amperage Severity Test Levels

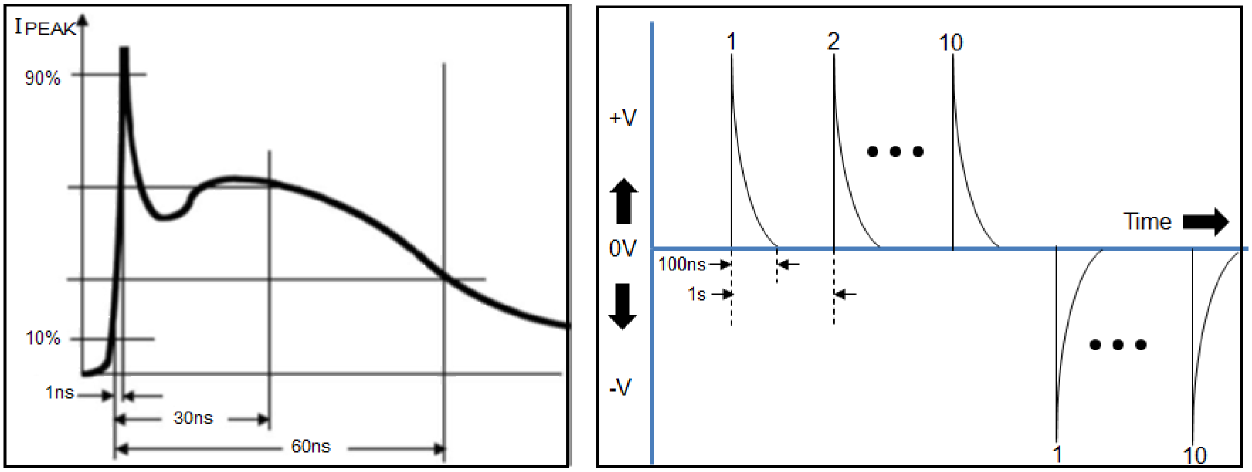
LEVEL	Contact Discharge Voltage	First Peak Current of Discharge ±10%	ESD Pulse Rise Time (tr)	Current ±30% @ 30 ns	Current ±30% @ 60 ns
1	2 kV	7.5 A	0.7 to 1 ns	4 A	2 A
2	4 kV	15 A	0.7 to 1 ns	8 A	4 A
3	6 kV	22.5 A	0.7 to 1 ns	12 A	6 A
4	8 kV	30 A	0.7 to 1 ns	16 A	8 A

Table 2-3. Common Static Voltages

Static Voltages as a Function of Relative Humidity	20% RH (kV)	80% RH (kV)
Walking across a vinyl floor	12	0.25
Walking across a synthetic carpet	35	1.5
Arising from a foam cushion	18	1.5
Picking up a polyethylene bag	20	0.6
Sliding a styrene box on a carpet	18	1.5
Removing mylar tape from a PC board	12	1.5

Static Voltages as a Function of Relative Humidity	20% RH (kV)	80% RH (kV)
Shrinkable film on a PC board	16	3.0
Triggering a vacuum solder remover	8	1.0
Aerosol circuit freeze spray	15	5.0

Figure 2-1. IEC 61000-4-2 ESD Amperage Discharge Test Waveform



When a prominent semiconductor manufacturer was contacted with questions concerning language in one of their component data sheets about ESD protection and their claims that it met IEC61000-4-2 level 4 requirements, their reply was "Yes, it met level 4 requirements". When asked about the max discharge current, their response was that the "IEC61000-4-2 only specifies a maximum voltage that their component met". However, as you will discover in this application note, it is ultimately all about power, (i.e., I * E), which means that it is not sufficient for the component to meet just the voltage specification, but the peak currents associated with a particular IEC 61000-4-2 test, as well.

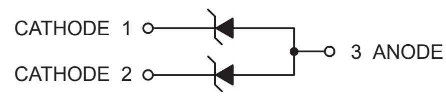
As a general rule:

1. If the manufacturer as an example states the component meets 8 kV discharge, but no mention of IEC 61000, this may indicate that it is compliant to the HBM, which is the lesser specification, and the component is not IEC 61000-4-2 compliant (see Table 10-1).
2. Even when a manufacturer states that they comply with IEC61000-4-2 level 4, but only mentions voltage, but not current, this could indicate that they may or may not comply with all aspects of IEC61000-4-2. If in doubt, contact the manufacturer for clarification. It is always recommended to design in the respective required protection components based on the level of protection needed. This at least gives the user the option to populate (or not) based on IEC 61000-4-2, IEC 610004-4, and IEC 61000-4-5 testing results. These false and exaggerated claims may also apply to the protection devices themselves.
   For example, compare the highlighted feature claim for a Transient Voltage Suppressor (TVS) manufacturer in Figure 2-2, and their electrical characteristics specifications with IEC 61000-4-2 in Table 4. Note that the max IPP, (i.e., Peak Pulse Current), data sheet current versus the 30A IPP specified in IEC 61000-4-2 level 4. Despite the manufacturer's misleading claim, this component does not meet all aspects of IEC 61000-4-2 level 4 requirements.
3. Generally, a TVS should have a rating of 250-400 peak surge watts to meet Level 3 or 4 requirements for IEC61000-4-2 contact discharge.

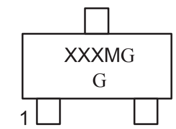
Figure 2-2. Misleading IEC 61000-4-2 Level 4 TVS Data Sheet Example

Features

- SOT−23 Package Allows Either Two Separate Unidirectional Configurations or a Single Bidirectional Configuration
- Working Peak Reverse Voltage Range − 3 V to 26 V
- Standard Zener Breakdown Voltage Range − 5.6 V to 47 V
- Peak Power − 24 or 40 W @ 1.0 ms (Unidirectional)
- ESD Rating:
  - − Class 3B (> 16 kV) per the Human Body Model
  - − Class C (> 400 V) per the Machine Model
- ESD Rating of IEC61000−4−2 Level 4, ±30 kV Contact Discharge
- Maximum Clamping Voltage @ Peak Pulse Current
- Low Leakage < 5.0 mA
- Flammability Rating UL 94 V−0
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant



MARKING DIAGRAM



XXX = Specific Device Code
M = Date Code
G = Pb−Free Package
(Microdot may be in either location)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)
UNIDIRECTIONAL (Circuit tied to Pins 1 and 3 or Pins 2 and 3)
(V_F = 0.9 V Max @ I_F = 10 mA) (5% Tolerance) **24 WATTS**

				Breakdown Voltage				Max Zener Impedance			V_C @ I_{PP}		
	Device	V_{RWM}	I_R @ V_{RWM}	V_{BR} (V)			@ I_T	Z_{ZT} @ I_{ZT}	Z_{ZK} @ I_{ZK}		V_C	I_{PP}	QV_{BR}
Device	Marking	Volts	mA	Min	Nom	Max	mA	W	W	mA	V	A	mV/5C
XXXXXXXXXX1	XX1	3.0	5.0	5.32	5.6	5.88	20	11	1600	0.25	8.0	3.0	1.26
XXXXXXXXXX2	XX2	3.0	0.5	5.89	6.2	6.51	1.0	–	–	–	8.7	2.76	2.80
XXXXXXXXXX3	XX3	4.5	0.5	6.46	6.8	7.14	1.0	–	–	–	9.6	2.5	3.4
XXXXXXXXXX4	XX4	6.0	0.3	8.65	9.1	9.56	1.0	–	–	–	14	1.7	7.5

Note: The component data sheet claims it meets IEC-61000-4-2 Level 4; however, after a quick look at the electricals, it is revealed that the Peak Pulse Current (IPP), falls well short of Level 4 requirements (see Table 2-2). Far too often this is the case, and unsuspecting circuit designers learn too late and become a victim of this tactic. Also, note that it is only rated at 24 watts, which reflects the low IPP specifications.

2.1 Effective ESD Deterrent Strategies

- Transient Voltage Suppressors (TVS)
- PCB design
- Ferrite beads
- RC, LC, and C filters

3. Electrical Fast Transient (EFT) Immunity IEC 61000-4-4

The IEC 61000-4-4 is an IEC standard designed to test fast transient or burst immunity at the system level. In EFT tests, waveforms are coupled into signal, control lines, power, and earth connections to simulate the coupling of transient noise onto these lines.

Common Causes of EFT

- Inductive loads, such as relays, switch contactors, or heavy-duty motors when de-energized, produce bursts of narrow high-frequency transients on the power distribution system
- Fast transients produced when the utility provider switches in or out the power factor correction equipment.
- Sparking that occurs whenever an AC power cord is plugged in, equipment is switched on/off, or when circuit breakers are opened or closed
- Lightning strikes also produce EFT events. EFT transients are coupled to end equipment typically over power lines.
- Subway trains and electric buses impose large EFT surges onto the power grid and subsequently AC mains with their constant arcing
- A common mistake in switching power supply layout is to have a big loop on the SMPS high-switching current paths. This path must be heavy and as short as possible.

Note: The sensitive output resistor divider feedback net of an SMPS should not be routed parallel to a vibrant EFT source like the inductor, which should always be a shielded type and mounted such that a sufficient air gap (at least 2 mm) must be reserved around to evacuate the heat.

Key Points

- A word about EFT and EMI. Obviously, it is not the only priority, but the first priority in a design should be to insure that EFT and EMI cannot enter or exit your design. It is much harder to contain and deal with electrical disturbances once they have spread out and infected dozens of circuits within your design. Therefore, your first mission objective should be to focus on primary power entry (i.e., power supply) and external PCB interfaces for the biggest bang for the buck which is what the reference schematics at the end of the application note focus's on.
- Typically, transformer less power supply and Switch Mode Power Supply (SMPS)-based systems face more EFT issues compared to iron core transformer based systems (see ESD, EMI, and EFT Hardware Circuit Schematic Protection Examples).

Embedded controllers are designed to generate and act on signals that have timing specifications comparable to that of transient-induced noise. Therefore, transient-induced noise is likely to interfere with these signals. In a broad classification, the following blocks are most influenced by transient-induced noise:

- Power and ground signals
- Reset circuits
- Edge-sensitive triggers
- High-impedance signals
- Analog signals
- External communication blocks, such as I2C, SPI, UART, etc.
- CPU
- RAM

EFT Resets

EFT transient-induced noise can generally affect one or more of these blocks if the user does not design their application for EFT from the beginning. If not, the following types of system failures can occur and most commonly in this priority order:

- CPU or system reset
- Latch-up
- Communication errors or failure
- Memory corruption

By far, the most common reaction to an EFT (i.e., transient-induced noise) event due to an ineffective design, is one of the following types of resets:

- External reset
- Power-on Reset (POR)
- Low-voltage Detect (LVD)-based reset
- Brown-out Reset (BOR)
- Software reset

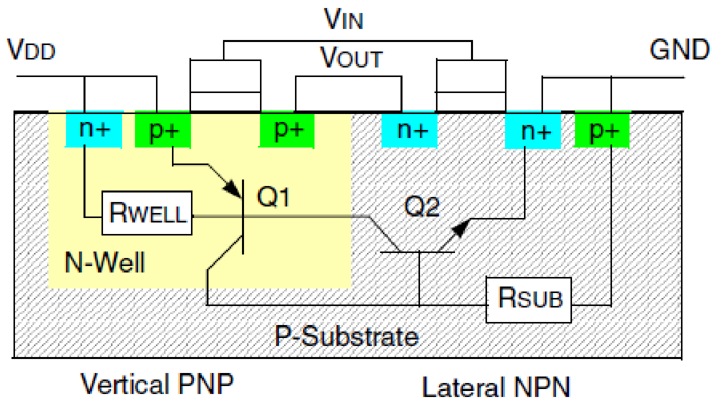
Resets due to POR, LVD, and BOR typically occur in the following cases:

- Transient-induced noise pulls down the supply voltage
- Transient-induced noise shifts the ground reference
- Negative transient-induced noise triggers the ESD clamp circuits on I/Os so that the effective supply voltage seen by the device dips triggering a BOR
- POR/BOR occurs if the effective supply voltage is below the device operating voltage range. When brown-out and LVD-based reset are enabled in the controller, these events can occur when the effective supply voltage is below the trip voltage and stays there beyond the minimum time.
- A software reset occurs if the master device wants to reset the slave upon detecting abnormal behavior in the system such as when the master receives incorrect data due to the loss of signal integrity. A software reset can also occur if the code execution is not normal and enters an exception. This abnormal code execution can be due to a corrupted state in the CPU, clock, Flash, or RAM.

EFT Latch-up

EFT-induced transients can also cause latch-up. All CMOS logic devices will latch-up when exposed to a strong enough voltage transient on either an input pin or a supply pin. Before addressing possible preventative measures to latch-up, it is important to understand how it occurs. A cross-section of a CMOS logic inverter is shown in Figure 3-1, which also shows the pair of parasitic bipolar (BJT) transistors that are formed.

Figure 3-1. Cross-sectional View of an Inverter



The equivalent circuit that is formed by the parasitic BJTs is shown in Figure 3-1. Thus, the transistors form a parasitic Silicon Controlled Rectifier (SCR). A SCR turns ON when triggered, and stays ON until the current flow is reduced to a value below the minimum holding current. Triggering can occur when sufficient current is forced to flow through either the N-well or substrate impedance to cause a voltage drop of about 0.6 volts or greater with the appropriate polarity. The triggered SCR or latch-up condition thus forms a self-sustaining low impedance path between VDD and ground, which can lead to the destruction of the device due to overcurrent if not power cycles in time.

The EFT pulse waveform shown in Figure 5-1, has a high amplitude (0.5 - 4 kV), short rise time, high repetition rate, and a low energy content. IEC 61000-4-4 also defines test levels based on the amplitude of the pulse waveform, as shown in Table 3-1. It consists generally of a burst of 75 pulses repeated every 300 milliseconds for a duration of 1 minute. Both positive and negative polarity EFT pulses are injected during testing

Table 3-1. IEC 61000-4-4 Electrical Fast Transient Test Levels

Level	I/O Signals/Data Terminals		Power Supply Terminal	Environment	Repetition Rate (kHz)
	Peak Voltage	Repetition Rate (kHz)	Peak Voltage		
1	0.25 kV	5 or 100	0.5 kV	5 or 100	Well Protected Environment
2	0.5 kV	5 or 100	1 kV	5 or 100	Protected Shielded System *(i.e., Home Appliances)*
3	1.0 kV	5 or 100	2 kV	5 or 100	Typical Industrial
4	2.0 kV	5 or 100	4 kV	5 or 100	Severe Industrial

Typically, transformerless power supply and Switch Mode Power Supply (SMPS)-based systems face more EFT issues compared to iron core transformer based systems (see Figure 12-10).

Power Supply Coupling Modes	
L+	Positive pulses on power line
L-	Negative pulses on power line

Power Supply Coupling Modes	
N+	Positive pulses on Neutral
N-	Negative pulses on Neutral
LN+	Differential mode, positive pulses across Line and Neutral
LN-	Differential mode, negative pulses across Line and Neutral

Like ESD, EFT can be especially fatal on data and I/O lines. The fast rise time of the EFT pulses demands a suppression element with the same characteristics as that which are required for suppression of an ESD pulse. Again, TVS diodes offer the best solution for suppressing the expected transient energy while keeping clamping voltages across the protected elements to a minimum. Additionally, the extremely fast response time of TVS diodes is essential for responding to the 5 ns rise time of the EFT pulse.

3.1 Effective EFT Deterrent Strategies

- Power Suppressors: Metal Oxide Varistor (MOV), Transient Voltage Suppressors (TVS)
- Common mode chokes
- Ferrite beads
- PCB design
- Capacitive filters
- Twisted pair power lines

Figure 3-2. Twisted Pair Power Lines

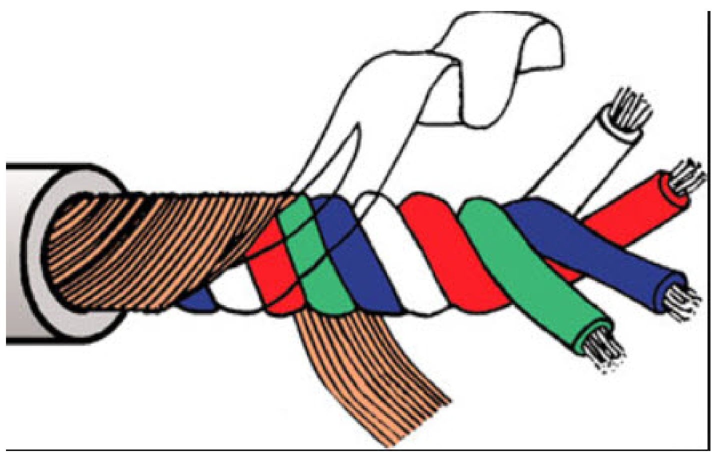
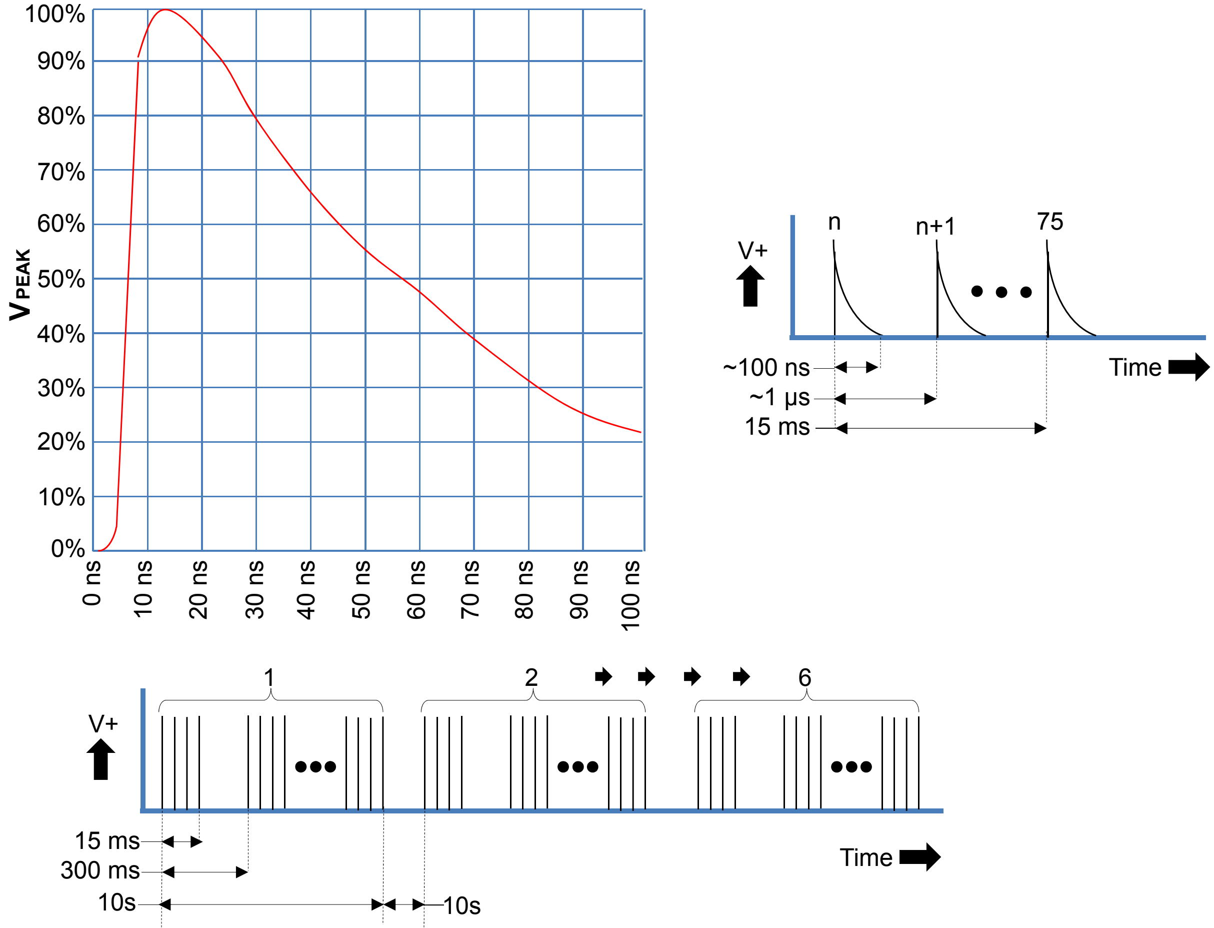


Figure 3-3. EFT Test Waveforms



4. Filter Capacitor Selection

A brief word about capacitors as EFT/EMI filters. EFT testing frequencies tend to be in the 100-200 MHz range, (~5 ns rise time). When selecting capacitors as noise filters, users should always consider two important characteristics of the capacitor: maximum frequency limitation and self-resonance. The maximum frequency limitation of various types of capacitors is shown in Table 4-1. Self-resonance is the frequency at which a capacitor no longer behaves like a capacitor and instead becomes more like an inductor.

Table 4-1. Capacitor Frequency Limits

Capacitor Type	Frequency Limitation
Aluminum Electrolytic	100 kHz
Ceramic	1 GHz
Mica	500 MHz
Mylar	10 MHz
Paper	5 MHz
Polystyrene	500 MHz
Tantalum Electrolytic	1 MHz

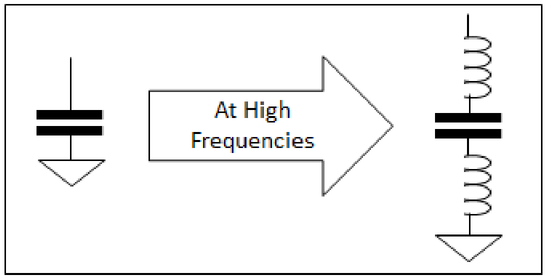
Ensure that the type of capacitor you are using to filter out noise has a higher self-resonance frequency than that of the noise you are trying to filter out. Table 4-2 lists typical self-resonance frequencies of various values of capacitance.

Table 4-2. Capactior Self-resonance Frequencies

Capacitor Value	Leaded	Surface Mount
1 µF	2.5 MHz	5 MHz
0.1 µF	8 MHz	16 MHz
0.01 µF	25 MHz	50 MHz
1000 pF	80 MHz	160 MHz
100 pF	250 MHz	500 MHz
10 pF	800 MHz	1.6 GHz

Capacitor self-resonance frequency is the frequency at which resonance occur due to the capacitor’s own capacitance and residual inductance. It is the frequency at which the impedance of the capacitor becomes zero. The insertion loss of capacitors increase until the frequency reaches the self-resonance frequency, and then decrease due to residual inductance of the lead wires and the capacitor's electrode pattern existing in series with the capacitance. Since noise is prevented from going through the bypass capacitor to the GND due to the residual inductance becoming dominate, the capacitors insertion loss begins to decrease with increasing frequency. The frequency at which the insertion loss begins to decrease is called self-resonance frequency.

Figure 4-1. Self-resonance Frequency



Some surprising facts about capacitors to keep in mind that apply to ceramic XR5, as well as XR7. It is common knowledge that a given capacitors' tolerance degrades with temperature. Here are some not so well-known facts that a designer may not be aware of.

Key Points

- For a given capacitance of a ceramic capacitor, as the package size increases, the capacitance variation with an applied DC voltage decreases substantially
- For a given capacitance of a ceramic capacitor, as the package size increases, the capacitance variation decreases
- For a given capacitance of a ceramic capacitor among different package sizes, the lower voltage rated packages have less capacitance variation compared to higher rated voltage packages, but not within the same package size families

Ceramic capacitor type designations, such as X7R and Y5V, imply nothing about voltage coefficients,but only temperature coefficients. For example, a 4.7 μF 16V-rated capacitor with a 12V bias would typically provide only 1.5 μF of capacitance, but just increasing the package size from 0805 (2012 Metric) to 1206 (3216 Metric), the typical capacitance under a 12V bias would be 3.4 μF.

Note:

1. Both the Murata and TDK websites have tools that allow you to plot the variations of capacitors over different electrical and environmental conditions.
2. Another useful tool from AVX, for comparing capacitor impedance versus frequency as a function of package size, dielectric, voltage rating, and working voltage can be found at: http://www.avx.com/design-tools/.

5. Electromagnetic Interference (EMI/EMC) IEC 61000-4-5

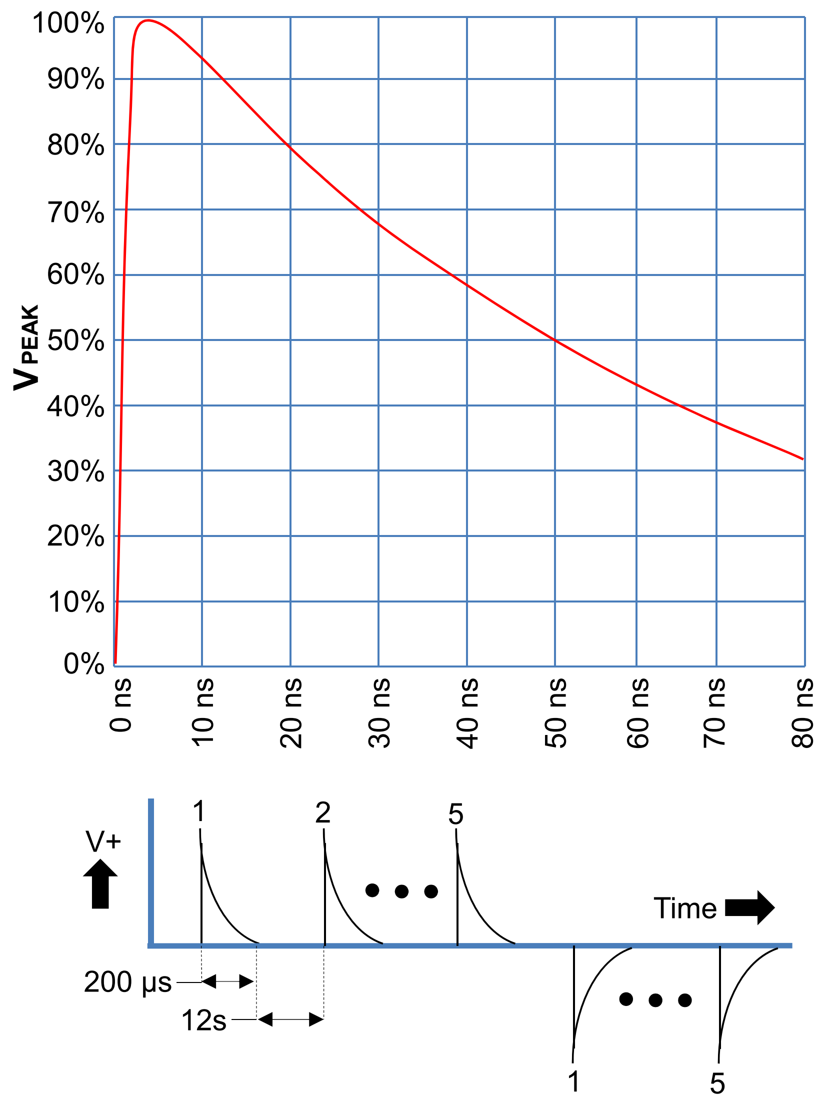
Electromagnetic Interference (EMI), is a disturbance generated by an internal or external source that affects an electrical circuit by electromagnetic induction, electrostatic coupling, or conduction. Electromagnetic Compatibility (EMC) is concerned with the unintentional generation, propagation and reception of electromagnetic energy, which may cause unwanted effects such as EMI or even physical damage in operational equipment.

EMI/EMC regulatory compliance testing is mandatory for medical device manufacturing per the appropriate FDA Reviewer Guidance document or the European IEC 60601-1-2 standards. In the European Union, all medical devices must have CE marking, which requires both immunity and emissions testing per IEC 60601-1-2. MIL-STD-461 contains stringent electromagnetic compatibility requirements. Consumer goods, such as microwave ovens, cellular phones, laptops, and satellite TV dishes all must undergo EMC/EMI testing to ensure they do not cause harmful interference and accept interference without causing undesired operation.

Table 5-1. IEC 61000-4-5 Electrical Electromagnetic Interference Test Levels

LEVEL	VOLTAGE
0	25V
1	0.5 kV
2	1 kV
3	2 kV
4	4 kV

Figure 5-1. IEC 61000-4-5 EMI Test Waveforms



5.1 Types of EMI

5.1.1 Radiated EMI

This type of EMI coupling that is normally experienced when the source and victim are separated by a distance, which is typically more than a wavelength. The source radiates a signal which may be wanted or unwanted, and the victim receives it in a way that disrupts its performance.

Most Effective Radiated EMI Deterrents:

- Proper PCB design
- Shielding
- Differential signals, such as CAN, USB, and Ethernet are particularly resistant to this form of interference due to common mode noise cancellation
- Twisted pairs
- RC filters

- Ferrite beads

Common Causes of Radiated EMI:

- Magnetic fields, such as those radiating from electrical wires, unshielded power transformers, inductors
- Electromagnetic surges due to a lightning strike
- Electrostatic discharges associated with static electricity
- High-speed signal impedance mismatches (signal reflections)
- High-density silicon devices with high-speed clocks and instantaneous current / power demands

Every functioning electrical circuit radiates EMI. The amount of radiated EMI depends on frequency, current, signal current loop area and inductance. Every current loop that carries a switching current source is also a radiator, and therefore, a loop antenna. Consequently, every circuit radiates radio frequency energy, EMI.

PCB Circuit Radiated EMI Factors:

- Antenna current loop area
- Inductance (load)
- Frequency
- Switching current

Figure 5-2. Radiated EMI Circuit Comparisons

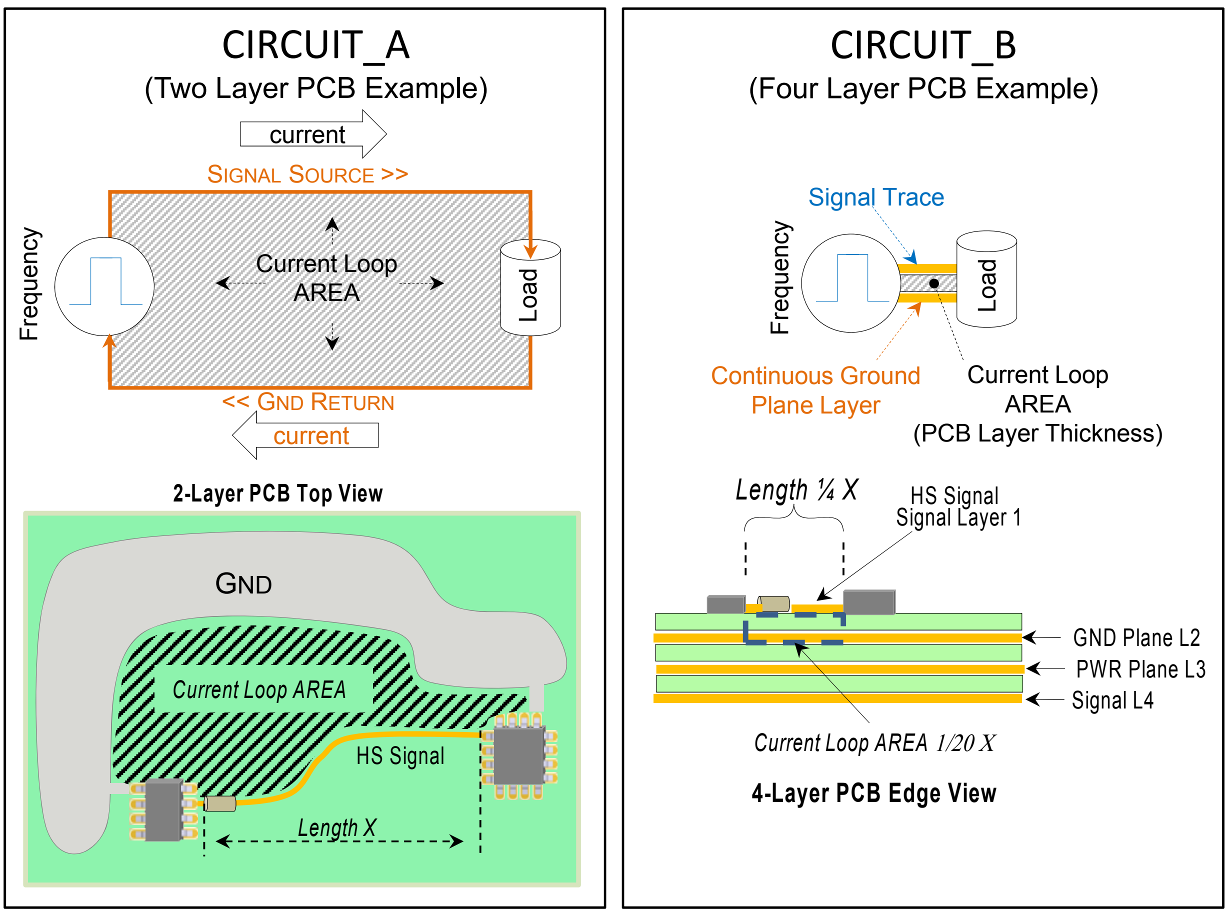


Table 5-2. Radiated EMI Circuit Comparisons

Circuit Example	Current Loop Area	INDUCTANCE	FREQUENCY	SWITCHING CURRENT
CIRCUIT_A	Very Large	Large	Same	Same
CIRCUIT_B	Very Small	Small	Same	Same

Referring to Figure 5-2, the Table 5-2 applies.

5.1.1.1 Signal Current Loop Area

EMI radiated energy is a function of the current loop area, which is the single most important factor of all contributors. On a two layer PCB it is impossible to have a continuous uninterrupted ground trace next to every signal on the board, as this can create large antenna loop areas. The larger the antenna, the larger the radiated emissions become, particularly with high-speed signals.

Key Point: Radiated energy is a cubic function of area. This means if you reduce the area enclosed by your loop by a factor of 2, you reduce the radiated power by a factor of 8. Going to a 4-layer PCB with a dedicated continuous ground plane effectively, as shown in Circuit_B of Figure 5-2, reduces one of the most import parameters of the area to just the thickness between the PCB layers resulting generally in a substantial reduction of radiated EMI in complex high density design layouts as depicted in the circuit “A” and “B” comparison. In conjunction to reducing the trace length by locating critical components in proximity, both the loop area and inductance is reduced for a double bonus.

5.1.1.2 Inductance

Inductance is dependent on wire length and is less dependent on width and height. Inductance of a PCB trace is equal to:

L(inductance) = 2.0 x 10^{-3} * Len [ln{(2.0 * Len) / (Width + Thickness)} + 0.5 + 0.2235{Width + Thickness) / Len}]µH

where Len, Width, and Thickness are in centimeters.

Key Point: Minimizing the PCB trace lengths, as shown in Circuit_B of Figure 5-2, particularly on high-frequency signals, will reduce the inductance reducing radiated EMI. Simply move critical circuits closer together in your floor planning to minimize trace length as in the Circuit “A” and “B” comparison.

5.1.1.3 Frequency

As the frequency and transition rate of change of the signal current increase, so does the radiated energy. It is not always possible on high-frequency signals to mute this due to speed timing requirements of the particular protocol, such as USB and Ethernet, except to insure that they have controlled impedance matching networks.

Key Point: One thing a user can do on synchronous protocols like SPI, for example, is to reduce the clock rate to achieve the minimum data rate needed by the application, rather than run at full-speed, which will also surrender more bandwidth to the CPU. Also, use series resistors on signals greatern than 8 MHz depending on the circuit capacitance to attenuate signal transition rates where possible.

5.1.1.4 Switching Current

In general, there is not much a user can adjust with regards to switching current, as signals loads are usually fixed by the design requirements. This would need to be evaluated on case-by-case circuit basis by the user for reduction opportunities.

Key Point: Radiated power = I^2 * R, which means if a user can reduce the loop switching current by 50%, in turn, the EMI radiated power would be reduced by 75%.

5.1.2 Conducted EMI

Conducted emissions occur when there is a conduction route along which the signals can travel. This can be along power cables or other interconnection cabling. The conduction may be in one of two modes:

- Common mode: This type of EMI coupling occurs when the noise appears in the same phase on two conductors, (i.e. outputs and return for signals, or + and - for power lines).
- Differential mode: This occurs when the noise is out of phase on two conductors.

Most Effective Conducted EMI Deterrent Strategies:

- PCB design
- Common mode chokes
- Ferrite beads (signal and AC power cord)
- RC, LC, and C filters

Common Causes of Conducted EMI:

- Magnetic fields, such as those radiating from electrical wires
- Voltage drops due to a brownout, blackouts or other power interruption
- Power voltage surges, sages, dips or spikes.
- Electromagnetic surges due to a lightning strike
- Electrostatic discharges associated with static electricity
- Fast transients caused by electrical switches, motors and relays, fluorescent lamp ballasts.
- EFT and ESD events.

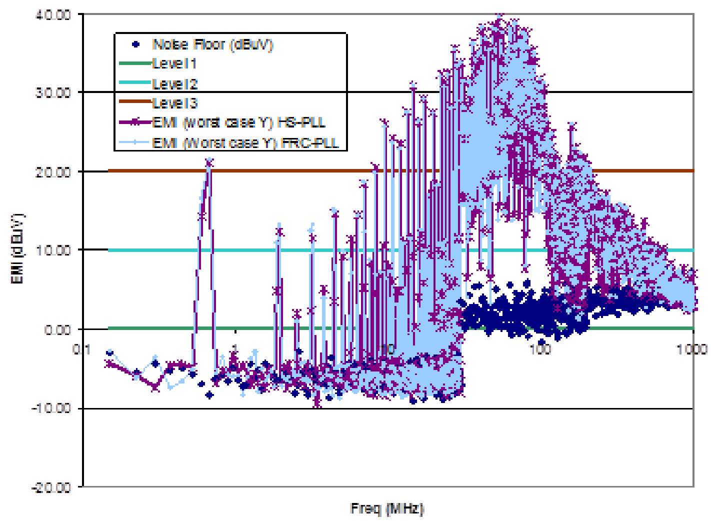
Filtering Techniques

The filtering techniques required for EMI will vary according to the type of EMI coupling experienced.

- *Inductive coupling:* This occurs due to magnetic induction.
- *Capacitive coupling:* This occurs when a changing voltage from the source capacitively transfers a charge to victim circuitry.
- *Magnetic coupling:* This type of EMI coupling exists when a varying magnetic field exists between the source and victim, which may occur when two conductors run close together (less than λ apart). This induces a current in the victim circuitry, thereby transferring the signal from source to victim.

5.1.3 Radiated EMI From Within an Application

Figure 5-3. Typical CPU Run Mode EMI Emissions (PLL and All Clocks Active)



Note: 80 MHz CPU clock with 160 MHz PLL with all I/O pins toggling at 630 kHz. Both “X” and “Y” EMI emissions are roughly the same for the same CPU configuration.

Even if the application is enclosed in a metal enclosure it will not isolate the circuit from internal radiated EMI sources or conducted EMI from external AC mains from power sources and I/O cabling. Various power supply filtering and/or shielding techniques may be required (refer to ESD, EMI, and EFT Hardware Circuit Schematic Protection Examples).

In particular, EMI shielding may be required for sensitive analog an RF Wi-Fi™ wireless circuits with high gain, low noise amplifier receiver front ends, (i.e., LNA). In many cases the CPU with so many internal high frequencies and harmonics is a strong source of radiated EMI and in some circumstances, may require an RF shield to prevent interference with on-board PCB wireless components. When employing an RF shield it is highly recommended that the user chooses shields large enough to not only encompass the CPU but the power pins Pi and T Filter networks as shown in the reference designs but also the CPU crystal oscillator circuit.

Note: Ensure that the RF shield has at least 3 mm clearance from any signal trace to protect against 8 kV Level 4 IEC61000-4-2 contact discharge.

Figure 5-4. EMI RF Shielding

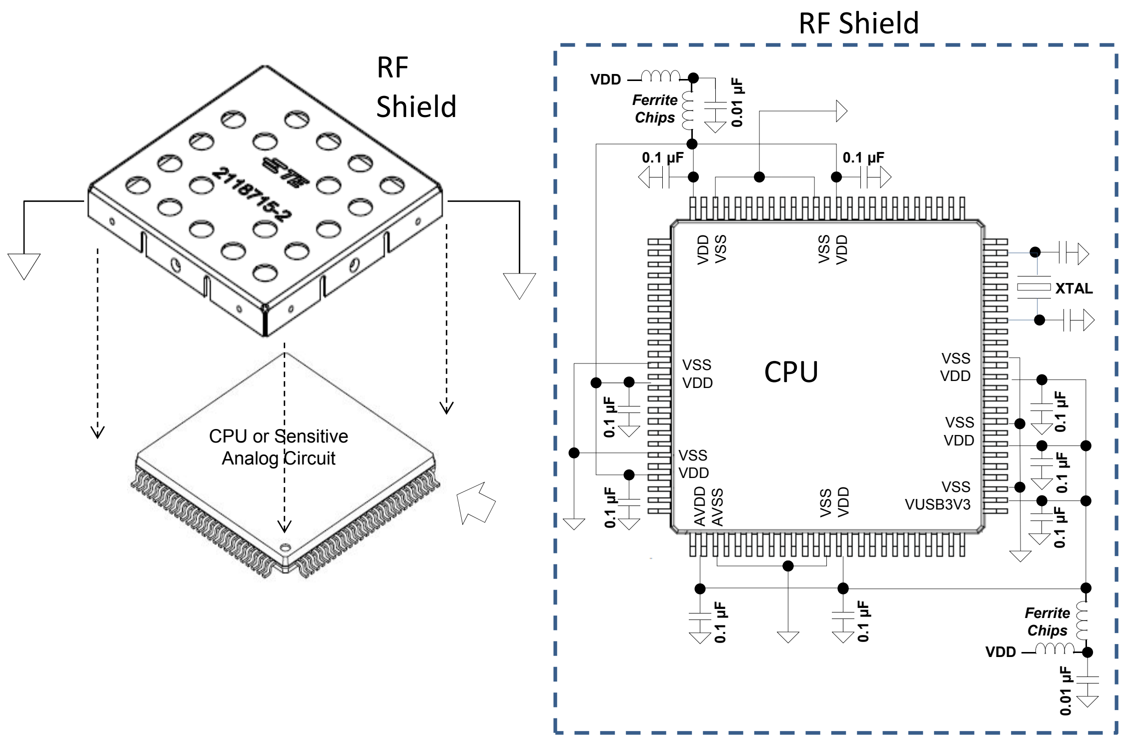


Table 5-3. EMI RF Shield Part Numbers

Manufacturer	Digi-Key / Manufacturer Part #	Dimensions (mm)
Leader Tech Inc.	1798-1176-ND / SMS-201C	13.26 x 13.26
TE Connectivity	A126120-ND / 2118715-2	16.90 x 16.90
Leader Tech Inc.	1798-1178-ND / SMS-202C	17.07 x 17.07
Leader Tech Inc.	1798-1182-ND / SMS-203-M-C	26.77 x 26.77

Note: Average cost in 1000 unit quantities: ~ $0.17 each.

Another source of internal application EMI can be from the CPU primary oscillator, particularly if the crystal is being over driven. Refer to the following of crystal application notes for reference.
Note: Check the target CPU for any primary oscillator errata that may take preference to the following references.

- AN826 - Crystal Oscillator Basics and Crystal Selection (http://ww1.microchip.com/downloads/en/appnotes/00826a.pdf)
- AN588 - Oscillator Design Guide (http://ww1.microchip.com/downloads/en/AppNotes/00588b.pdf)
- AN849 - Basic PICmicro® Oscillator Design (http://ww1.microchip.com/downloads/en/AppNotes/00849a.pdf)

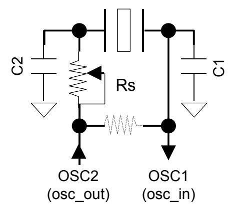
Important: None of the application note references previously listed, as well as either of the two crystal calibration methods that follow are relevant if the target CPU utilizes an internal crystal AGC design.

Methods to Ensure a Crystal is Not Overdriven

Figure 5-5. Method 1

Primary Oscillator: Method 1 of 2 (Ballpark Method)

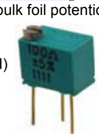
1) Set Rs = 0 Ohms
2) Start the CPU.
3) Toggle I/O pin and monitor with oscilloscope.
4) Using non-conductive adjustment tool, (i.e., non-metallic), very slowly increase Rs until I/O pin stops toggling.
5) Very slowly reduce Rs until I/O pin resumes toggling consistently.
6) Remove power.
7) Remove and measure Rs with an ohm meter.
8) Replace potentiometer with closest standard fixed value resistor less 10-15%



Potentiometer: 0-5K Ohm, Part# Y40535K00000J0L no substitutions allowed. Specialty required bulk foil potentiometer

High-Frequency Characteristics

- Rise time = 1.0 ns without ringing
- Inductance = 0.08 µH typical (i.e. 80nH)
- Capacitance = 0.5 pF typical



Primary Oscillator Crystal Load Capacitor Calculation

- C_{IN} = PIC oscillator input pin capacitance = 3.5-4 pF
- C_{OUT} = PIC oscillator output pin capacitance = 3.5-4 pF
- PCB stray capacitance (i.e., 12 mm length) = 2.5 pF
- C1 and C2 = Loading capacitors to use on your crystal circuit design to guarantee that the effective capacitance as seen by the crystal in circuit meets the crystal manufacturer C_{LOAD} specification

MFG Crystal Data Sheet CLOAD spec:
C_{LOAD} = {([C_{IN} + C1] * [C_{OUT} + C2]) / [CIN + C1 + C2 + C_{OUT}] } + oscillator PCB stray capacitance

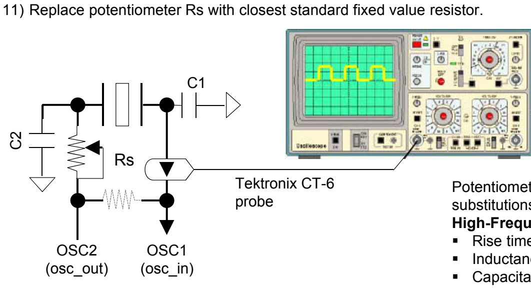
Assuming C1 = C2 and PIC C_{IN} = C_{OUT}, the formula can be further simplified and restated to solve for C1 and C2 by:

EQUATION 1:
C1 = C2 = ((2 * MFG C_{LOAD} spec) - C_{IN} - (2 * PCB capacitance))

Figure 5-6. Method 2

Primary Oscillator Method 2 of 2 (Traditional Method)

1) Set Rs = 0 ohms.
2) Place current probe in series on OSC1 (i.e., CPU Osc_in) side of crystal. Set oscilloscope to display RMS current.
3) Start up the CPU.
4) Measure oscilloscope IRMS current.
5) Calculate crystal power using Equation 3 below.
6) If power in watts is ~75% of crystal rated power drive specification, go to step 9.
7) Using non-conductive adjustment tool, (i.e., non-metallic), very slowly increase Rs by 1 turn, ~250 ohms.
8) Go to step 4 and repeat.
9) Disable CPU power.
10) Remove and measure Rs with ohm meter.
11) Replace potentiometer Rs with closest standard fixed value resistor.



Potentiometer Rs 0-5K Ohm, Part# Y40535K00000J0L no substitutions allowed. Specialty required bulk foil potentiometer

High-Frequency Characteristics

- Rise time = 1.0 ns without ringing
- Inductance = 0.08 µH typical (i.e. 80nH)
- Capacitance = 0.5 pF typical

Example:
Crystal = ABLSG-4.194304MHZ-D2Y-T (Mfg. specifications)

- Co = Shunt capacitance = 7 pF
- Cload = 18 pF
- ERS = Equivalent Series Resistance = 180 ohms
- PD = Power Drive = 1mW(max)

EQUATION 2:
$I_{RMS} = (I_{PKPK} / (2\sqrt{2})$

EQUATION 3:
Crystal Circuit Power = I_{RMS}^2 * ERS((1+Co / Cload)^2)

Note: If using a series resonance crystal, C_L goes to infinity; therefore, power is: (*Crystal Power = IRMS^2 * Motional Resistance*)

6. ESD, EMI, and EFT Circuit Protection Selection Strategy Summary

The goal of selecting a protection device is to insure it can survive the surge in the case of EFT and ESD event and to protect the equipment by limiting the surge voltage (VCL) below the maximum admissible voltage of the equipment/circuit. In the case of EMI, it is limit and attenuates both internal and external radiated and conducted energy. Table 6-1 lists the most common and effective forms of circuit protection based on the threat.

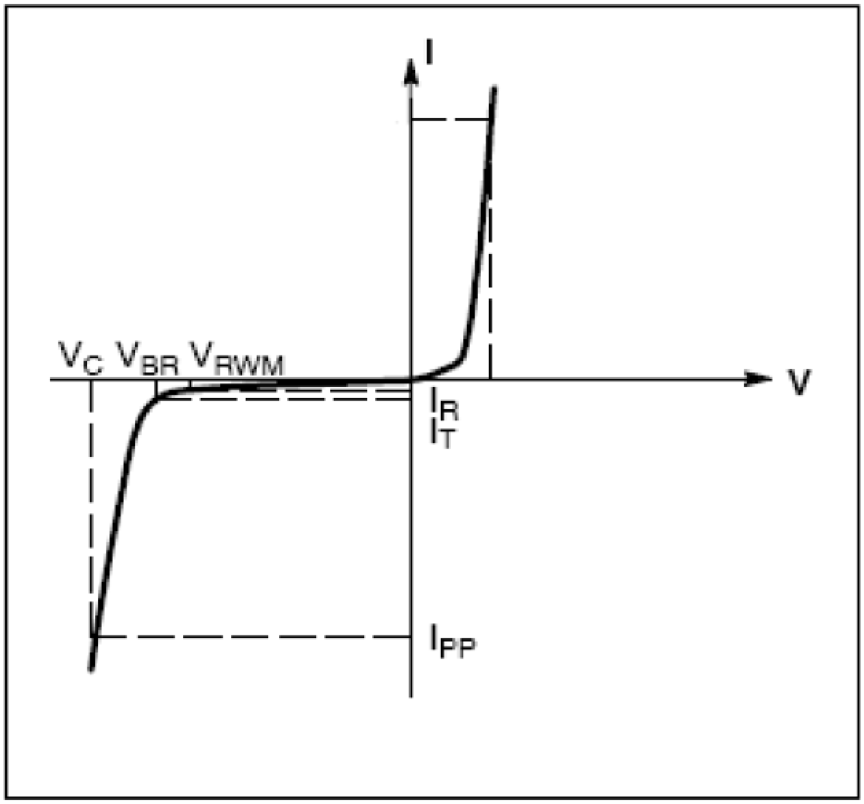
Table 6-1. Most Common Forms of Circuit Protection Based on the Threat

Type	Metal-Oxide Varistor (MOV)	TVS	RC Filter	LC Filter	Ferrite Bead/ Inductor	Common Mode Choke	PCB Layout/ Design	RF Shields
Conducted EMI	–	–	X	X	X	X	X	–
Radiated EMI	–	–	X	X	–	–	X	X
ESD	X	X	X	–	–	–	X	–
EFT	X	X	X	X	X	X	X	–

6.1 ESD Transient Voltage Suppressor (TVS) Selection Considerations

Using a unidirectional device is safer, as clamping voltage will be limited to VCL in one direction, and to a forward voltage on the other direction. A bidirectional device must be used only if the application requires accepting a reverse plug-in (on DC power lines) or if located on AC lines.

Figure 6-1. I/V Characteristics of a Unidirectional Clamping Device



Key Transient Voltage Suppressors (TVS), DC Parameters:

- VBR = Reverse Breakdown Voltage @ IT
- VRWM = Reverse Working Voltage @ IR (VRWM
- IPP = Maximum Reverse Peak Pulse Current (typically specified with either the 8 x 20 μs or 10 x 1000 μs Surge Pulse)
- VC = Clamping Voltage @ IPP

Reverse Working Voltage, VRWM: Maximum nominal working voltage for which the ESD device is intended for use. At this voltage, the ESD diode will appear in the “off” state as a high impedance element that will have very low leakage current. This spec must be greater than the intended peak operating voltage of the signal being protected.

Peak Pulse Current, IPP: Maximum surge current which the device can withstand without damage.

This parameter is very important for high-power transient voltage suppression (TVS) applications, such as IEC61000-4-2 level 4 contact discharge events.

Clamping Voltage, VC: Clamping voltage determines the voltage that the IC signal being protected will get exposed to. This is one of the most important parameters to consider in the selection of a Transient Voltage Suppressor in addition to IPP.

Capacitance, C: TVS capacitance is a parameter that becomes a concern for applications that operate at high data rates. High capacitance will degrade signals, compromising high-speed signal integrity. A device with low bulk capacitance is required for high-speed signals such as Ethernet, High-Speed USB, etc., which is typically less than 5 pF. Interesting in medium/low-speed signals that require protection, higher TVS capacitance devices can actually be a benefit and help provide a dual purpose. The higher capacitance acts also as a filter for EMI. Not only shunting conducted EMI but limiting the signal slew rate to reduce radiated signal EMI as well.

Reverse Breakdown Voltage, VBR: At this voltage, the ESD diode starts to conduct, or turn “on”. VBR is specified as a minimum value for ESD applications and usually is 10% to 15% above the VRWM. This spec is always higher than VRWM and lower than VC.

7. Printed Circuit Board (PCB) Layout and Design Considerations for EMC, EFT, and ESD

The initial primary focus of many designers is on insuring the functionality of their design with little consideration for EMI/EMC/EFT/ESD. EMI test fees and repeated board turns can add up quickly. Reportedly 90% of the products tested at one EMC/EMI test lab fail the first time through. If that is true, circuit design and PCB layout considerations for EMI/EMC/EFT/ESD are as important as functionality given that EMI compliance test fees can range from $5,000 to $50,000. Therefore, it's probably worthwhile to consider EMI/EMC/EFT/ESD in your initial PCB design. If not for certification requirements, then for application reliability.

There are tools, such as Near field scanners that allow users to see emissions all over a board and even zoom in and magnify hot spots to isolate potential layout issues. That is hard to do with a single probe. There are several EMI/EMC scanners on the market today, such as those from EMSCAN, DETECTUS, and API, among others. A scanner is essentially a series of near-field probes placed in a grid. Therefore, it can produce an image of a board's emissions that is more consistent and repetitive than you can get by manually scanning a board with a single probe. The EMxpert scanner from EMSCAN is one such scanner to consider. Click the EMxpert link to watch a demonstration video. EMxpert is a very useful tool, which allows you to quickly analyze and compare design iterations and optimize hardware design in real-time so that you are far more likely to pass the expensive certification lab testing, thereby saving valuable time to market for your product.

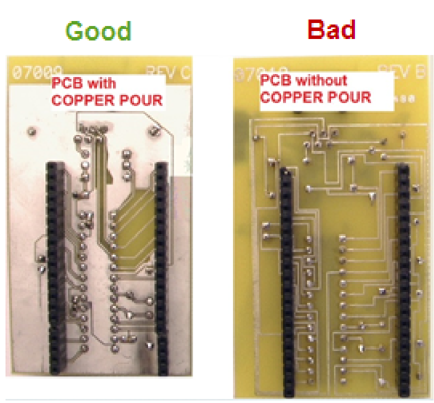
In the following sections, a series of "best known" methods (or practices) recommendations for PCB layout are provided to assist with meeting EMI/EMC/EFT/ESD concerns.

7.1 PCB Layout "Best Practices" Recommendations

Note: If your design requires EMC/EMI/EFT/ESD testing and certification, and after following as many of the following recommendations as possible, it is recommend that you make early contact with the targeted compliance lab and have a predesign meeting with the principals, such that their wisdom can be learned and applied to the early design effort. These principals have a wealth of experience on what does and does not work.

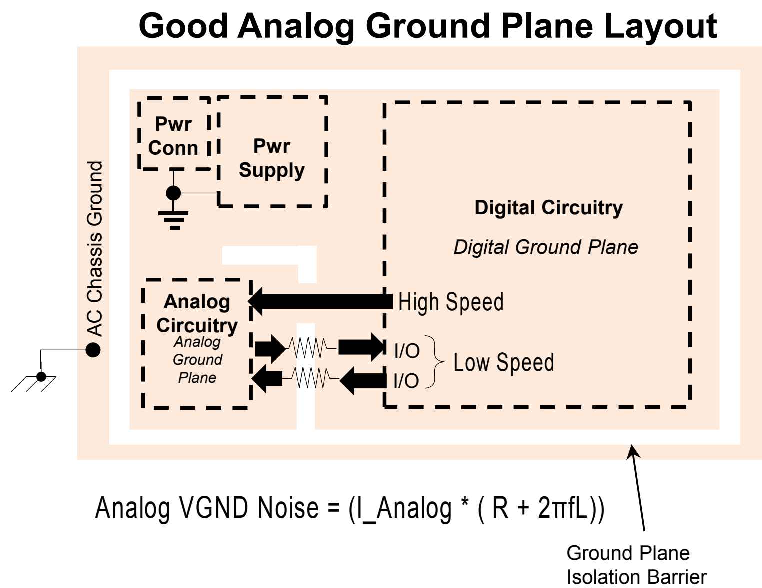
1. Layout differential and high-speed traces first maintaining differential impedance matching on PCB layer 1 adjacent to ground plane layer.
2. Ensure that all clock and high-speed signal traces have an unbroken reference ground plane with no gaps or voids beneath them and also that they are routed on layer 1.
3. Copper pour all voids on signal layers with signal ground.

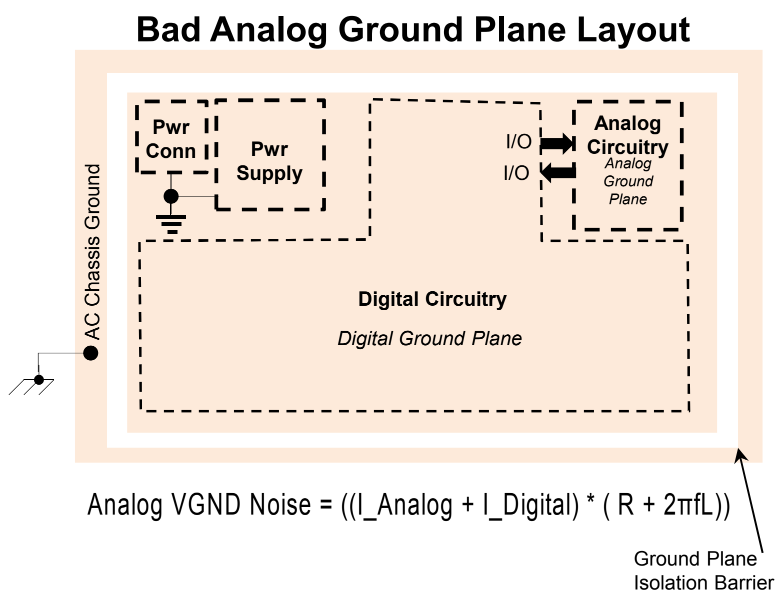
Figure 7-1. Copper Ground Pour in PCB Voids



4. Use separate digital and analog grounds when appropriate, and do not connect the ground planes together except at power ground, (i.e., closest to the respective input power regulator).

Figure 7-2. Analog Versus Digital Ground Layout Placement

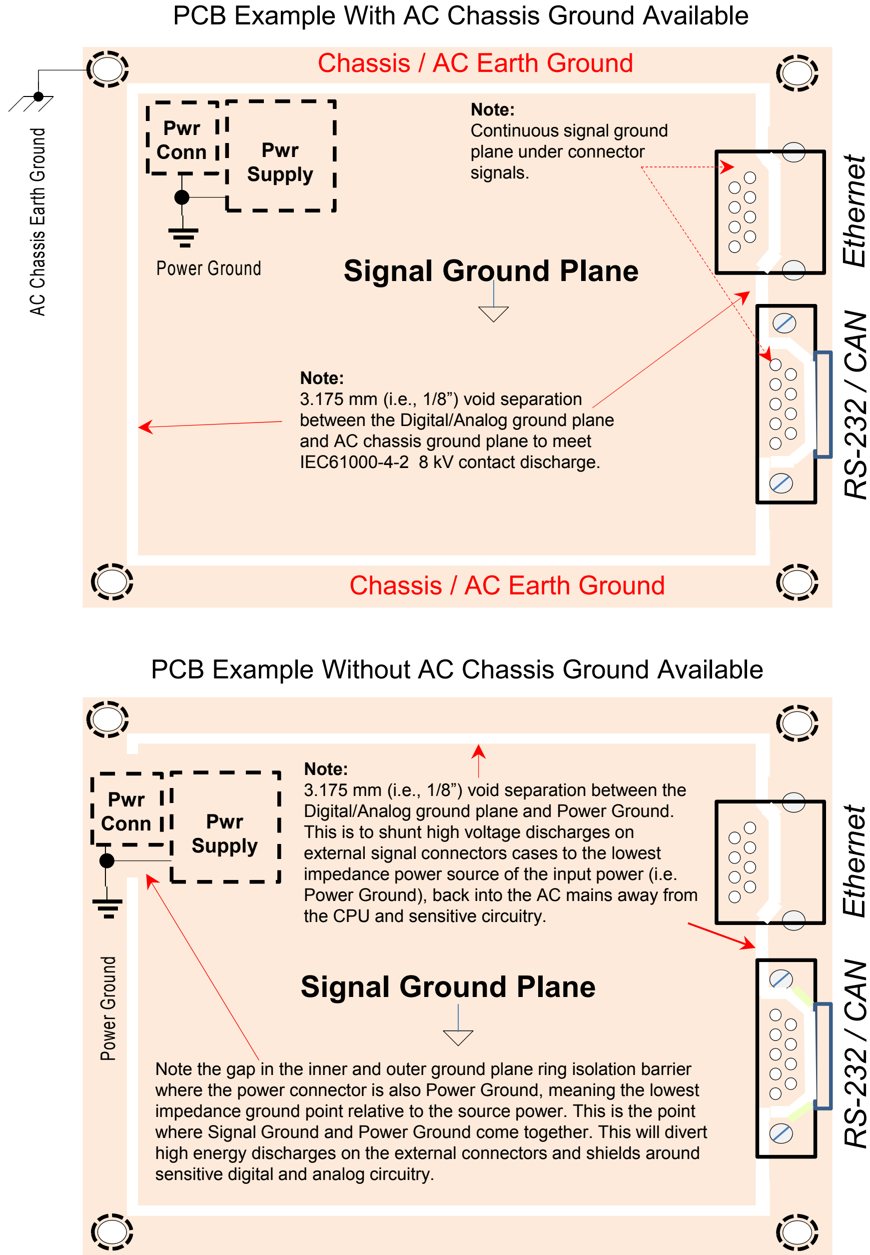




5. Digital noise and current is generally much larger than that of the analog circuitry. As a result, choose a layout strategy where analog ground current has a separate and not additive digital ground current and noise as depicted above. Use ground isolation barriers to steer and contain digital noise/current away from analog circuitry. Remember that high-frequency noise will seek the path of least inductance which is generally the shortest distance on a ground plane. When required to route low-speed digital signals to bridge analog and digital domain logic over ground voids (i.e., moat), use 1k to 5k series resistors, as shown in the Good Analog Ground Plane Layout in Figure 7-2. In cases where high-speed signals from digital to analog domain is required, such as audio codec master clock, do not route over ground voids, use an isolation barrier bridge, as shown in the first example, as well as a ~ 50 ohms termination resistor at the clock source.

6. Do not run sensitive analogue signals in parallel over or near fast digital transit signals. If necessary, insure they cross at right angles to minimize the capacitive cross section of the traces.
7. The lengths of traces carrying high-speed digital signals or clocks should be minimized. High-speed digital signals and clocks are often the strongest noise sources. The longer these traces are, the more opportunities there will be to couple energy away from these traces. In addition, remember that the loop area is generally more important than the trace length. Ensure that there is a good high-frequency current return path very near each trace.
8. The lengths of traces attached directly to connectors (I/O traces) should be minimized. Traces attached directly to connectors are likely paths for EMC, EMI, and EFT energy to be coupled on or off the board. The use of TVS and ferrite beads and/or common mode chokes as required are recommended on all external connector I/O pins (refer to ESD, EMI, and EFT Hardware Circuit Schematic Protection Examples).
9. In general, it is a good PCB design rule practice to not run any traces in between any surface mount pads (resistors, capacitors, ferrite beads, etc.).
10. PCB traces should be designed with the proper width for the amount of current they are expected to supply. The use of mini-planes in a local area on either the top or bottom layers will ensure proper current supply.
11. Partition the layout into functional blocks and position all components with critical signals adjacent to each other.
12. All component leads to any power plane or ground plane should be as short as possible. The best solutions are plane connection vias inside the surface mount pads. When using vias outside the surface mount pads, pad-to-via connections should be less than 5 to 10 millimeters in length. Trace connections should be as wide as possible to lower inductance. This will include any power ferrite beads feeding power planes, fuses feeding power planes, etc.
13. Signals with high-frequency content should not be routed beneath components used for board I/O. Traces routed under a component can capacitive or inductively couple energy to that component.
14. Whenever possible, all connectors should be located on one edge or on one corner of a board. Connectors represent the most efficient EMC/EMI antenna parts in most designs. Locating them on the same edge of the board makes it much easier to control the common-mode voltage that may drive one connector relative to another.

Figure 7-3. Grounding Recommendations for External Connectors



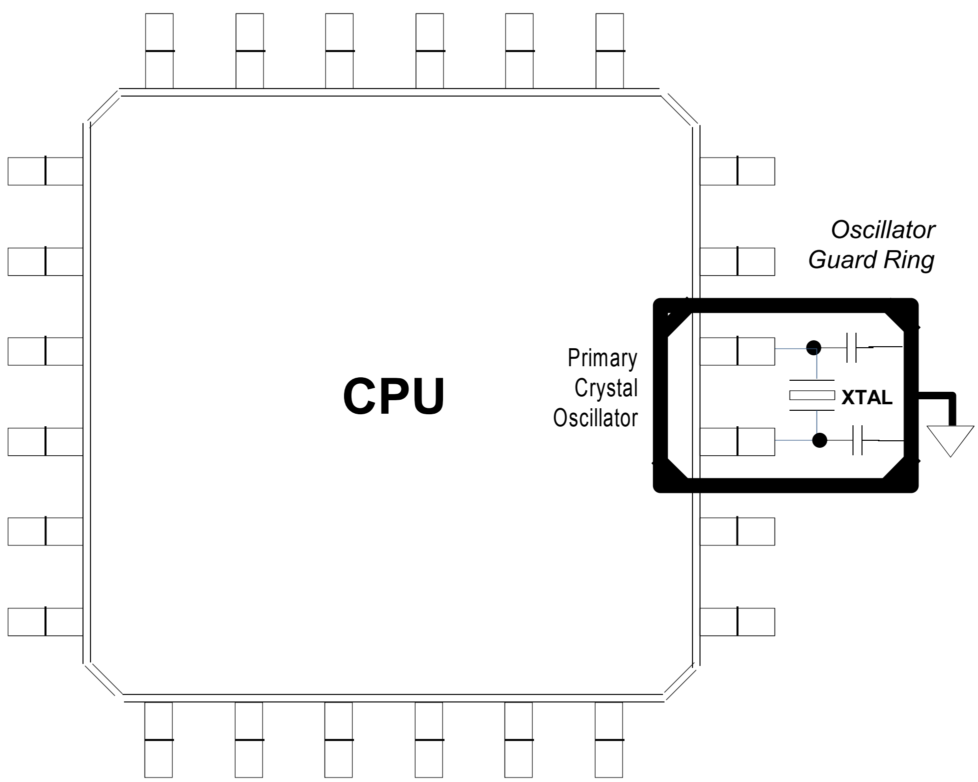
15. In applications where an AC chassis ground is available, as shown in the first in Figure 7-3, it is strongly recommended that digital signal ground and AC chassis ground NOT be connected and separated by at least 3.175 mm (i.e., 0.125 inches), for 11-12 kV spark gap isolation to meet IEC61000-4-2 Level-4 8 kV contact discharge.
   Peripherals like - USB, Ethernet, SD memory card holders, RS232 and CAN, the connector cases are electrically isolated from signal ground. The case should be connected to AC chassis ground whenever available, (i.e. Earth Ground), to shunt high-voltage discharges to earth ground harmlessly and NOT into the digital or analog ground circuitry. Note that in the figures the ground plane is always continuous under all the high-speed signal connections of the peripheral connector but the connector case is isolated to the outer AC chassis plane.
   Note: Not all connectors like audio metal input/output jacks cases are isolated. They are in fact the signal ground. In situations like this they should NOT be mounted to an isolated AC chassis

ground, but instead to the digital/analog ground as appropriate through a ferrite bead (see Audio Headphone and Microphone Schematic Protection). The user should determine whether or not the external peripheral connector in use has an isolated or non-isolated case to signal ground. For isolated connectors, connect only the connector case to AC chassis ground; otherwise, connect to signal ground through an appropriate ferrite bead.

On the second example in Figure 7-3, where there is no AC chassis ground (i.e., Earth Ground) available, the best strategy is to still have an isolation barrier and join the inner and other planes at the lowest impedance point in the circuit relative to the power source at the power inlet and regulator otherwise called power ground. This will divert high-energy discharges on the external connectors and shields around sensitive digital and analog circuitry to be dissipated through the power source and coupled to the AC mains.

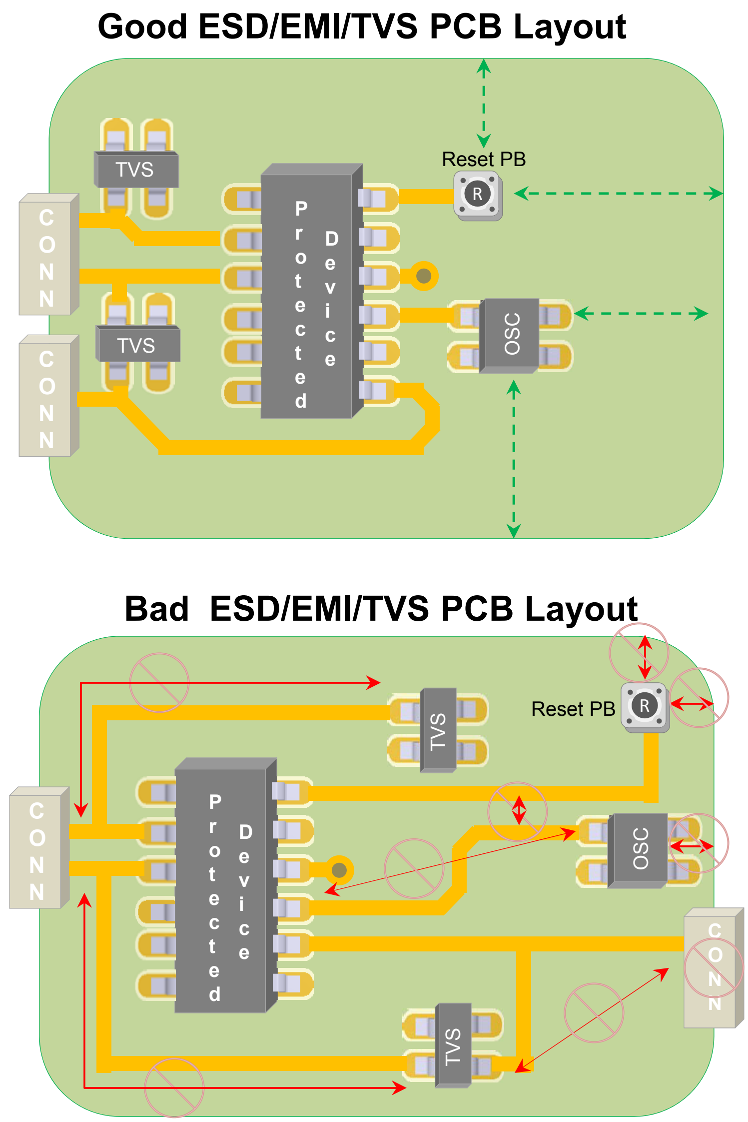
16. No high-speed circuitry should be located between I/O connectors. Even if two connectors are on the same edge of the board, high-speed circuitry located between them can induce enough common-mode voltage to drive one connector relative to the other resulting in significant radiated emissions.
17. Unused I/O pins should not be allowed to float as inputs. They should be tied to ground through a 1k to 10k resistor.
18. The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins as possible, not to exceed (12 mm). The load capacitors should be placed immediately next to the oscillator itself, on the same side of the board. Use a grounded copper pour, guard ring (see lkdf) around the oscillator circuit to isolate it from surrounding circuits. On a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Figure 7-4. Oscillator Guard Ring



19. When possible, critical signal or clock traces should be buried between power/ground planes. Routing a trace on a layer between two solid planes does an excellent job of containing the fields from these traces and prevents unwanted coupling.
20. Select active digital components that have maximum acceptable off-chip transition times. If the transition times of a digital waveform are faster than they need to be, the power in the upper harmonics can be much higher than necessary. If the transitions times of the logic employed are faster than they need to be, they can usually be slowed using series resistors or ferrites.
21. All off-board communication from a single device should be routed through the same connector. Many components (especially large VLSI devices) generate a significant amount of common-mode noise between different I/O pins. If one of these devices is connected to more than one connector, this common-mode noise will potentially drive a good antenna. (The device will also be more susceptible to radiated noise brought in on this antenna.)
22. Locate TVS as close to external signal connectors as possible, with TVS ground connections directly to ground plane the avoid ground trace connections.
23. High-speed or susceptible analog/digital traces should be routed at least 2x from the board edge, where 'x' is the distance between the trace and its return current path. The electric and magnetic field lines associated with traces very near the edge of a board are less well contained. Crosstalk and coupling to and from antennas tends to be greater from these traces and makes them more susceptible to ESD, EMI, and EFT events.
24. Susceptible components/circuits should be kept away from the PCB edge. Preferably, place them in the center of the board. If this is not possible, try to place them at a distance greater than 12 mm from the edge if no exterior AC chassis ground ring is used because in high-voltage discharge events, high-frequency energy collects on exterior edges particularly at the right angle corners of the PCB body (use rounded PCB corners), as depicted in Figure 7-5.

Figure 7-5. PCB Layout Examples



25. Differential signal trace pairs should be routed together and maintain the same distance from any solid planes. Differential signals are less susceptible to noise and less likely to generate radiated emissions if they are balanced (i.e., if they have the same length and maintain the same impedance relative to other conductors). These, and other high-speed signals should be routed on layer 1, directly above the ground plane layer to minimize current loops and radiated EMI.
26. All power (voltage) planes that are referenced to the same power return (ground) plane, should be routed on the same layer. For example, if a board employs three voltages, 3.3 volts, 3.3 volts analog, and 1.8 volt, it is generally desirable to minimize the high-frequency coupling between these planes. Putting the voltage planes on the same layer will ensure that there is no overlap. It will also help to promote an efficient layout, since the active devices are unlikely to require two different voltages at any one position on the board.
27. The separation between any two power planes on a given layer should be at least 3 mm (i.e., 11 kV isolation). If two planes get too close to each other on the same layer, significant high-frequency coupling may occur. Under adverse conditions, arcing or shorts may also be a problem if the planes are too closely spaced.

28. On a board with power and ground planes, no traces should be used to connect to power or ground. Connections should be made using a via adjacent to the power or ground pad of the component. Traces on a connection to a plane located on a different layer take up space and add inductance to the connection. If high-frequency impedance is an issue, as it is with power bus decoupling connections, this inductance can significantly degrade the performance of the connection. In the case of devices like CPUs with multiple power pins that may require EMI/EFT filtering local power and ground islands.
29. If the design has more than one ground plane layer, any connection to ground at a given position should be made to all ground layers at that position. The overall guiding principle here is that high-frequency currents will take the most beneficial (lowest inductance) path if allowed to. Do not try to direct the flow of these currents by only connecting to specific planes.
30. Ideally, there should be no gaps or slots in the ground plane unless user has sensitive analog logic they are attempting to isolate (see Figure 7-3). It is usually best to have a solid ground (signal return) plane and a layer devoted to this plane. Any additional power or signal current returns that must be DC isolated from the ground plane should be routed on layers other than the layer devoted to the ground plane.
31. Be certain to review the entire PCB design for any high-speed signal traces crossing over any reference plane cuts. This will more than likely create an EMC occurrence, so be sure to avoid this.
32. All power or ground conductors on the board that make contact with (or couple to) the chassis, cables, or other good "antenna parts", should be bonded together at high frequencies. Unanticipated voltages between different conductors, nominally called "ground", are a primary source of radiated emission and susceptibility problems.
33. Components that interface with the external world should be kept close to the PCB edge. The remaining components should be kept away from PCB edge to reduce environmental effect (i.e., ESD).
34. If filters (i.e., RC or Ferrite bead) are used to filter external signals, they should be placed at the location of their entry to the PCB. If a Ferrite bead is used to suppress noise, then it should be kept towards the noise source rather than a susceptible device. Always try to suppress noise at the source. If noise spreads, it becomes more difficult to control.
35. If common mode choke or transient suppressor devices (i.e., TVS, MOV) are used for power filtering, they should be placed at the entry of the PCB. In circuits protected by TVS circuits, external signals from the connector should be routed to the TVS first, and then to the ferrites or common mode chokes, and then to the protected component.
36. The differential signals including mains power (L and N) should come from adjacent pins on the same connector.
37. PCB traces should be routed using 45 degree corners when changing directions; whereas, 90 degree corners should *never* be used.
38. All component leads to any power plane or ground plane should be as short as possible. The best solutions are plane connection vias inside the surface mount pads. When using vias outside the surface mount pads, pad-to-via connections should be less than 5 to 10 millimeters in length. Trace connections should be as wide as possible to lower inductance. This will include any power ferrite beads feeding power planes, fuses feeding power planes, etc.

7.2 PCB Bypassing

1. Bypass capacitors should be placed near all power entry points on the PCB. These caps will allow unwanted high-frequency noise from entering the design; the noise will simply be shunted to ground.

2. Multiple bypass capacitors, in x10 or x100 decade values, should be utilized on all IC power supply connections and all voltage regulators in the design.
3. All bypass capacitor leads should be as short as possible. The best solutions are plane connection vias inside the capacitor surface mount pads. When using vias outside the surface mount pads, pad-to-via connections should be less than 5 – 10 millimeters in length. Trace connections should be as wide as possible to lower inductance.
4. IC decoupling capacitors and ferrite beads should be placed as close to the IC power pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. Ideally there should be two bypass caps, 0.1 µF and 0.001 µF, in parallel. Run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum thereby reducing PCB trace inductance.
5. The use of a bulk capacitors distributed over the area of the power plane in the design is recommended to improve power supply stability particularly around large current consumption devices. Typical values range from 4.7 µF to 47 µF. Place the bulk capacitors close to the location where current demand is the highest. At a minimum, one per functional block and maybe more in close proximity where instantaneous current demand is high like the CPU.

7.3 PCB Layer Strategy

1. *4-Layer PCB Example:*
   - Layer 1 component plus signal side (short traces)
   - Layer 2 ground plane
   - Layer 3 power plane
   - Layer 4 signal

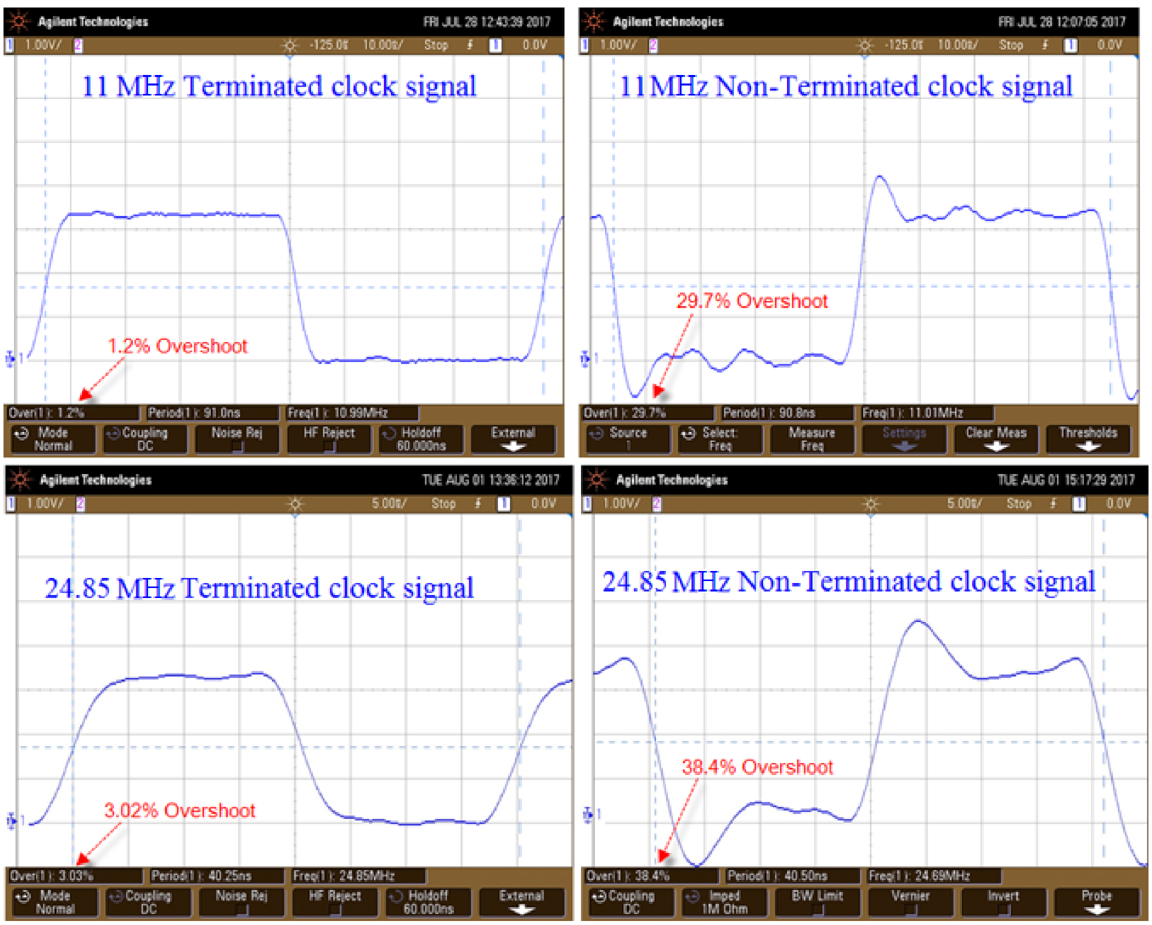
   Note: Strongly recommended for all high-speed Ethernet LAN designs and minimum requirements to meet most EMC, EMI and EFT requirements.
2. *6-Layer PCB Example:*
   - Layer 1 component plus signal side (short traces)
   - Layer 2 ground plane
   - Layer 3 signal
   - Layer 4 signal
   - Layer 5 power plane
   - Layer 6 signal

   Note: Layer 1 on either 4- or 6-layer PCBs is considered the prime layer for critical routes and components because of the solid digital ground plane directly beneath it and Layer 1 also requires no vias to connect components located on Layer 1.
3. All PCB traces (especially high-speed and critical signal traces), should be routed on Layer 1 next to the solid, contiguous ground plane layer. These traces must have a continuous reference plane for their entire length of travel. This will improve EMC performance and signal integrity issues.
4. The implementation of an Ethernet chassis ground plane separate from the digital ground plane is required.
5. Avoid creating ground loops in the PCB design and the system design. To facilitate routing and minimize signal crosstalk issues, adjacent layers in a multi-layer design should be routed orthogonal.

7.4 PCB Signal Integrity Concerns

1. If required to cross a ground plane void (i.e. moats, slot, barrier) for slow-speed I/O to traverse digital to analog sections, do so with resistors or ferrites with a high DCR to help slow down signal edge transitions to minimize radiated EMI. As an alternative, many CPUs, such as the PIC32MZXXEFXX, PIC32MZXXDAXX and PIC32MKXX families, have I/O with user programmable slew rate control for the same purpose (refer to the specific device family data sheet for details). Never cross a ground plane void with high-speed signals or clock lines.
2. Provide AC terminations for all high-speed switching signals and clock lines with very long length traces on the PCB if unavoidable. Locate these terminations at the load end of the trace. In general, use a 50 ohm series resistor with a 50k parallel load to ground.
3. Provide impedance matching 50 ohm series terminations to minimize ringing overshoot and undershoot on critical and high-speed signals. These series terminations should be located at the driver end of the trace as opposed to the load end of the trace. Unterminated signal frequencies in the 35-45 MHz range can experience over/under shoot in the 50% range. Unterminated high-speed signals can be a significant contributor to the radiated EMI/EMC signature and crosstalk.

Figure 7-6. Terminated Versus Non-Terminated Clock Signals



4. Avoid via usage and branches in high-speed signals, differential, and clock lines.
5. Minimize the use of vias throughout the design on high-speed signals, as vias add capacitance to signal traces.

6. In general, review all signal crosstalk design rules to avoid crosstalk problems. Use the 3-W rule to provide enough trace separation to avoid crosstalk problems. Guard traces may also be utilized to minimize crosstalk problems on high-speed signals.
7. For impedance matching consider SMT resistor arrays for large busses.
8. It can be tricky to determine up front the correct termination resistor value, as most vendors do not specify output rise/fall times and driver impedance. This can be fine-tuned on the bench with the first prototypes. It is commonly reported that a 22 to 50Ω resistor is adequate.

Note: As an alternative, most manufacturers post an IC's IBIS models on-line. In the IBIS text file you can find the V/I and output impedance values for the output driver pin(s) to determine the correct impedance.

8. Ethernet 10/100 Base-T Design Guidelines

8.1 Ethernet TX± and RX± Differential Pair Considerations

1. Both RX± and TX± pairs should be routed as differential pairs. This includes the entire length of travel of the traces from the RJ-45 connector to the LAN device.
2. RX± and TX± differential pairs should be routed as close together as possible. Typically, when beginning the impedance calculation, the smallest trace space (4 to 5 mils) is selected. The trace width is then adjusted to achieve the necessary 100 ohm impedance.
3. Differential pairs should be constructed as 100 ohm, controlled impedance pairs.
4. Designs employing common mode chokes for EMI isolation must be 100 ohm.
5. Differential pairs should be routed away from all other traces with a clearance of at least three times the trace width.
6. Each trace of the differential pair should be matched in length. The matched lengths of each positive and negative pair should be within 20 mils of each other.
7. The differential pairs should be as short in length as possible.
8. The use of vias is not recommended. If vias are used, keep to a minimum and always match vias so the differential pairs are balanced.
9. Layer changes are also not recommended. Keep the differential pairs referenced to the same power/ground plane whenever possible.
10. For optimum immunity, route Transmit pairs and Receive pairs as far away from each other as possible.
11. Always reference any Transmit terminations to the same reference plane that the Transmit routes are referenced to. Likewise, always reference any Receive terminations to the same reference plane that the Receive routes are referenced to.
12. Precedence should be given to the differential pair routing. Terminations should be added after the routing is determined. The terminations should simply be “dropped” onto the differential routing.
13. All resistive terminations in the Ethernet front end should have values with 1.0% tolerances.
14. All capacitive terminations in the Ethernet front end should have tight tolerances and high-quality dielectrics (NPO).
15. For optimum separation, experimentation can be explored with inserting a ground plane island between the Transmit pair and the Receive pair. A separation from this ground plane from any of the traces of 3 to 5 times the dielectric distance should be maintained.
16. This same technique can be used to separate different Ethernet ports if port cross talk is an issue. A ground plane can be inserted between Ethernet channels. The separation space between the two channels should be as wide as possible. Again, a separation from this ground plane from any of the traces of 3 to 5 times the dielectric distance should be maintained.
17. The length difference between the TX data and TXCK lanes should not exceed 300 mils.
18. The length difference between the RX data and RXCK lanes should not exceed 300 mils.
19. The impedance of any single-end signal trace should be 50 ± 10% Ω.

8.2 Unused Ethernet Cable Pairs

The unused cable pairs (pins 4, 5, 7, and 8 on the RJ-45 connector) should be properly terminated for common mode considerations. These terminations should be routed with heavy, short traces and as close as possible to the RJ-45 connector.

If not using an RJ-45 connector with internal termination for unused cable pairs, terminate with 75 ohm resistors to a proper chassis ground plane through a high voltage (2 kV) capacitor.

8.3 Ethernet RJ-45 Connector

1. A shielded, metal enclosed RJ-45 connector is recommended.
2. The metal shield should be connected directly to a proper chassis ground plane.
3. Another ESD enhancement may be to use of an RJ-45 connector with surface mount contacts. This may simplify routing and allow greater separation in the Ethernet front end to enhance ESD/ susceptibility performance.

8.4 Ethernet Magnetics

1. There are many different types and configurations of magnetics available for use with any particular LAN device. Different packages, orientations, sizes are all factors that need to be considered when selecting magnetics.

Table 8-1. Ethernet Magnetics Selection Criteria

Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	–
Open-circuit inductance (minimum)	300 µH	100 mV, 100 kHz, 8 mA
Insertion loss (typical)	-1.1 dB	100 kHz to 100 MHz
HIPOT (minimum	1500 Vrms	–

2. The magnetics should be placed as close as possible to the RJ-45 connector.
3. Depending upon which style of magnetic selected (North/South or East/West) will determine the orientation of the magnetics as related to the RJ-45 connector. Be certain that the network side of the magnetics faces the RJ-45 connector and the device side of the magnetics faces the LAN device. This will ensure that the high-voltage barrier through the middle of the magnetics can be correctly routed and designed on the PCB.
4. Ideally, the LAN device should then be placed as close as possible to the magnetics. If this is not possible, the RJ-45 connector and magnetics must remain in close proximity. The LAN device then can be located somewhat remotely from the RJ-45/magnetics area.

9. DDR Design Guidelines

1. In each data lane the length difference between each signal and the respective DQS/DQSn signal should not exceed 50 mils.
2. It is recommended to route all signals of the same data lane on the same layer.
3. The DQS/DQSN signal pairs should be routed as differential traces. The length difference between the differential traces should not exceed 20 mils, with a controlled impedance of 100 ± 10% Ω.
4. The length difference between the data lane and the CK signal should not exceed 400 mils.
5. The impedance of any single-end signal trace should be 50 ± 10% Ω.
6. The length difference between the ADDR/CMD/CTL signal and the CK signal should not exceed 200 mils and recommended to route all of these signals on the same layer.
7. CK/CKn signals should be routed as differential traces. The length difference between the differential traces should not exceed 20 mils, with a controlled impedance of 100 ± 10% Ω.
8. To minize crosstalk signals in the same data lane: 8 to 12 mils.
9. Data lane signal to other signals: Greater than 20 mils.
10. ADDR/CMD/CTL/CK to other signals: Greater than 20 mils.
11. Place the microcontroller and DDR memories as a first-level priority. The traces should be as short as possible with a minimal number of vias.

10. Human Body Model (HBM) Versus ESD IEC 61000-4-2

There are several differences between the HBM and IEC 61000-4-2 standard, which must be factored into your decision to use external ESD protection logic. The differences are:

- Amount of current and the resulting power released during a voltage strike
- Rise time of the voltage strike
- Number of voltage strikes in a test

The difference in current/power is critical to whether or not a target will survive the ESD strike. Because high current levels can cause junction failures and metallization traces to melt, it is possible that a chip protected to 10 kV HBM can be destroyed by a 2 kV IEC 61000-4-2 strike. The problem is sometimes exacerbated by advanced technology with smaller silicon geometry devices, because it generally makes them more susceptible.

Table 10-1. Human Body Model (HBM) Versus IEC 61000-4-2 Contact Discharge Peak Current

Applied Voltage	Peak Current HBM	Peak Current IEC 610000-4-2
2 kV	1.33 Amps	7.5 Amps
4 kV	2.67 Amps	15.0 Amps
6 kV	4.00 Amps	22.5 Amps
8 kV	5.33 Amps	30.0 Amps
10 kV	6.67 Amps	37.5 Amps

The most important difference to note in Table 10-1 is the peak current level associated with a strike, which should be a consideration for TVS component selection, if required. Although most silicon is warranted to survive some level of contact with ESD HBM peak currents, they generally are not warranted to survive 5.5x higher IEC 61000-4-2 peak surge currents without external ESD protection logic. The ratings that are used for protecting ICs in the manufacturing environment, such as HBM and CDM, are not equivalent to system level ESD tests in IEC 61000-4-2.

The HBM model specifies a rise time of 25 ns. An IEC pulse has a rise time of less than 1 ns and dissipates most of its energy in the first 30 ns. If it takes 25 ns for most target silicon internal protection logic to respond, devices rated using the HBM specification can be destroyed if subjected to IEC 61000-4-2 tests. Unless the data sheet for the target silicon specifically states it is tested to IEC 61000-4-2, users should assume its HBM, or contact the manufacturer for clarification.

Another difference is the number of strikes used during testing. The IEC 61000-4-2 test requires 10 positive strikes and 10 negative strikes; however, the HBM standard requires only a single positive and single negative strike to be tested. It is possible for a device to survive a single strike, but fail on subsequent strikes due to damage sustained during the initial strike.

11. Software EFT Protection Techniques

As discussed previously in Electrical Fast Transient (EFT) Immunity IEC 61000-4-4, the most common issues resulting from a poorly protected and/or designed circuit to an EFT event are:

- CPU or system reset (*most common*)
- Communication errors or failure
- Latch-up
- Memory corruption

On a poorly protected design, the most common result of an EFT event is a CPU reset. Most CPUs have multiple reset mechanisms, such as an external hardware reset, a Brown-out Reset (BOR), low-voltage detect (LVD) resets on some devices, and Power-on Reset (POR). The trigger conditions for each of these resets vary, but the challenge for the application software is determining whether the reset in question was a normal occurrence, such as in a typical routine power-up or from an EFT event. There are no absolutes when it comes to software protection, but following are a few common sense "best practices" to be considered. At the end of this section is a firmware technique to enable the users application to determine if a POR or BOR was caused by an EFT event or just a normal power-up sequence.

11.1 Runaway Code Protection

Watchdog Timer (WDT)

The WDT can be used to indicate and recover from a runaway code event, such as what could occur due to an EFT event.

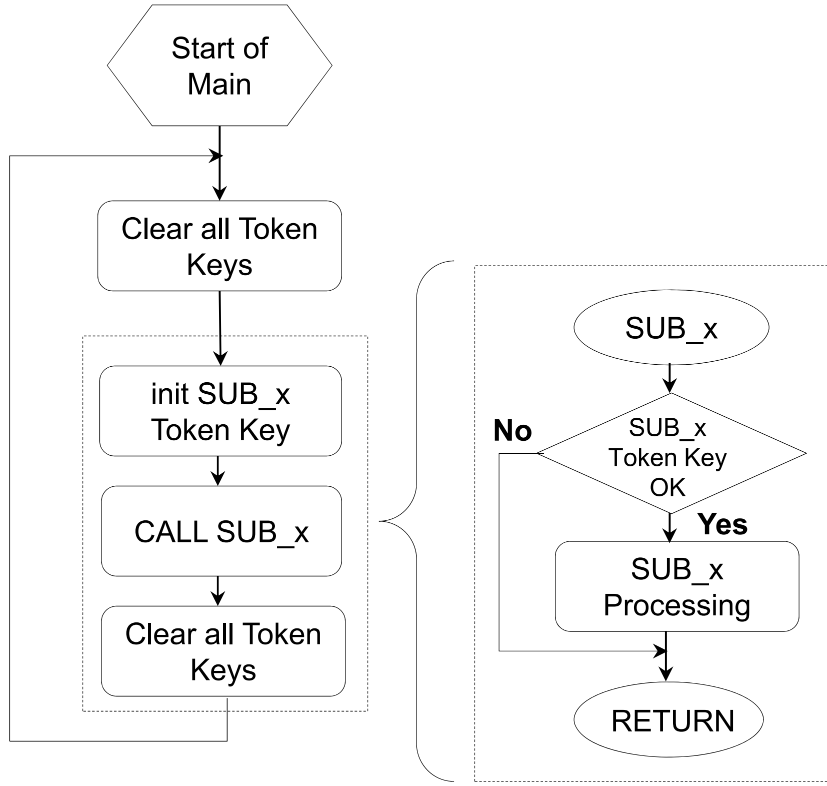
1. Use the shortest WDT time-out period possible to ensure that a runaway condition will not last very long.
2. Use only one WDT refresh operation within the main loop, not interrupt service routines, unless main loop execution period is greater than the WDT time-out, in which case WDT refreshes should be placed at approximately equal intervals in the main loop.
3. Use multiple RAM challenge token keys to decide whether or not to refresh the WDT, and not just a single bit.

Token Keys

Protect crucial subroutines and WDT refresh from a runaway code event by using challenge RAM persistent token keys, which will help guard against arrant runaway code execution.

Note: A persistent variable is a variable that does not get initialized automatically at reset by the compiler run-time initialization routine. The compiler run-time initialization routine is a routine that the linker appends as a prefix to the users object and hex file, which is not visible in the user's source code. The advantage of this variable type is that is is not preinitialized by a reset event. It allows the user code to evaluate and decide if and when at run-time the variable should be initialized; for example, based on an EFT-induced reset, versus a typical start-up reset.

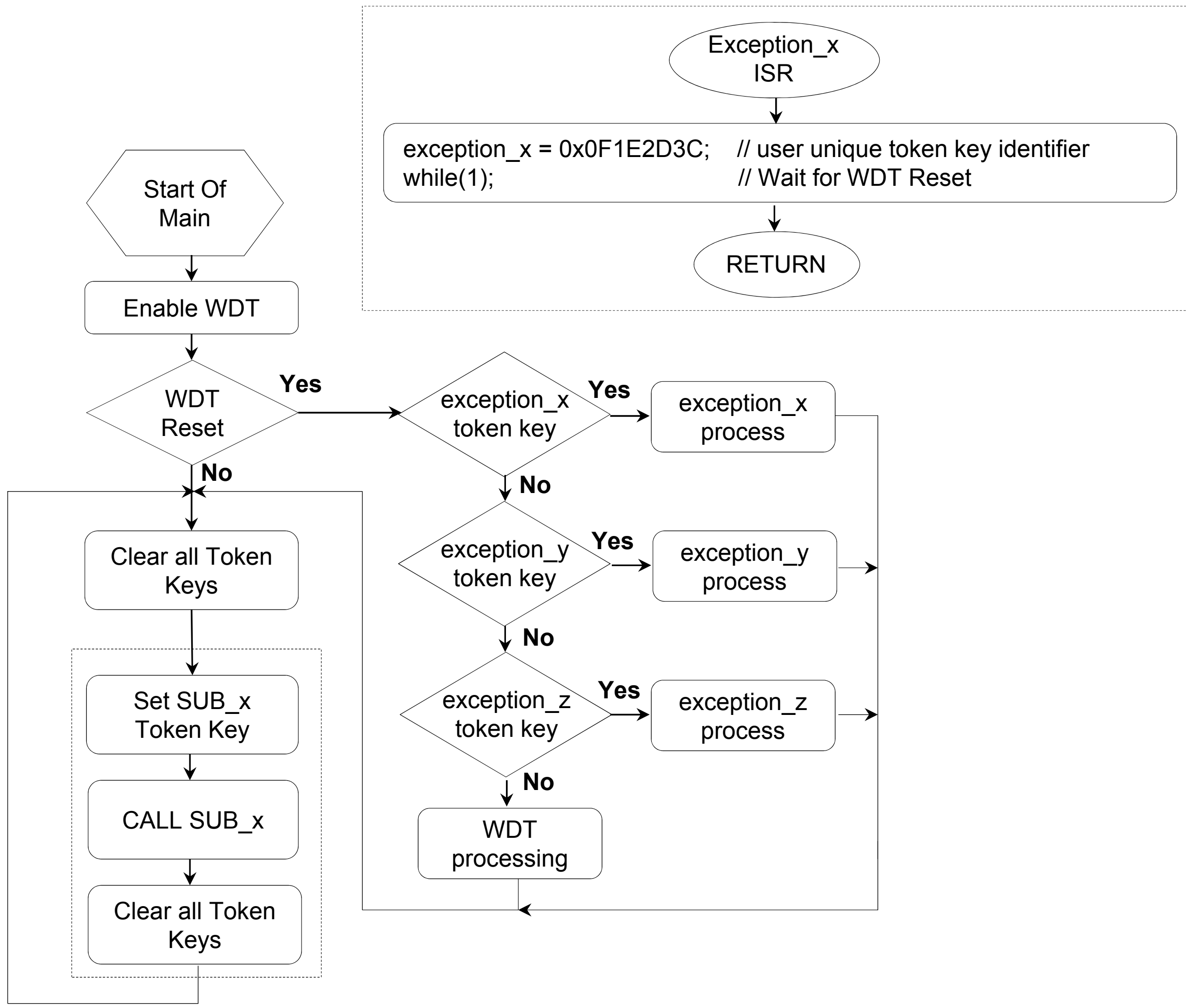
The following figure shows an example for `_persistent unsigned int token_sub_x, token_sub_y, token_sub_z;`.



Exception Handlers

1. Create ISR's for all exception errors like illegal opcode, misaligned address, invalid memory address, etc.
2. Create persistent variables for each type of exception and upon entry into exception ISR initialize persistent variable with a user selected unique value. In the MPLAB XC32 C/C++ Compiler for PIC32 devices, the compiler automatically populates all user undefined exceptions with `while(1)`.
   Note: In most CPUs, the exception ID register is a persistent hardware register and is not cleared on any reset. Check the respective CPU data sheet or software user's guide for clarification. If your CPU has a persistent hardware exception ID register, ignore using the software exception RAM token key portion of the example as depicted below.
3. On a WDT CPU reset, check to see if any exceptions occurred as a possible EFT event, and handle as appropriate.

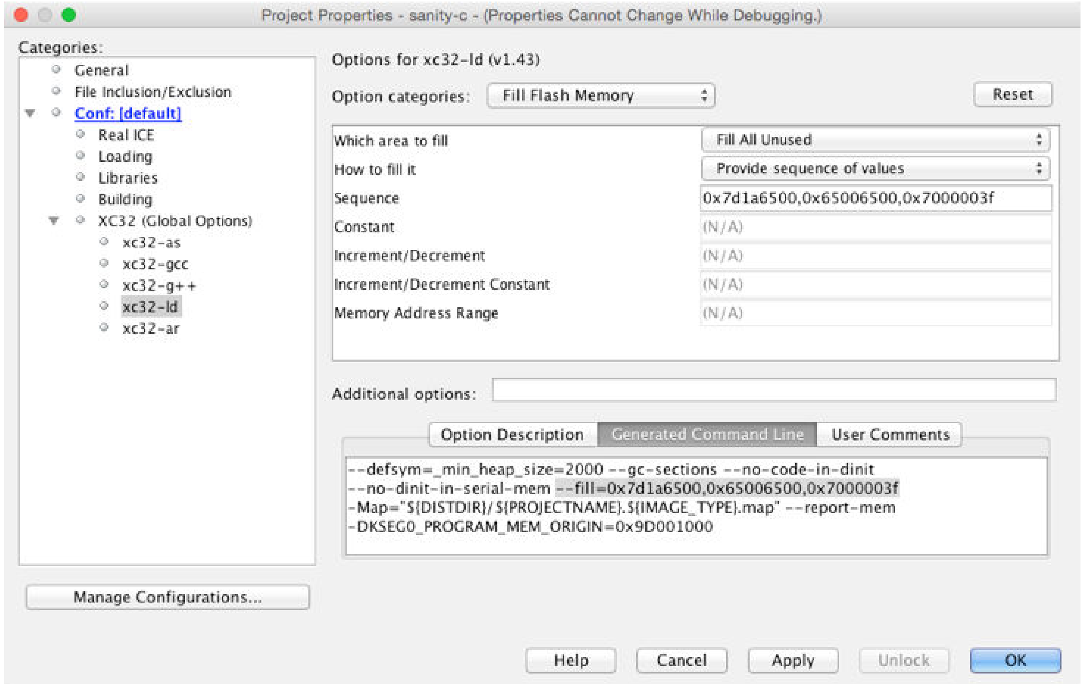
Figure 11-1. Exception Example _persistent unsigned int exception_x, exception_y, exception_z;



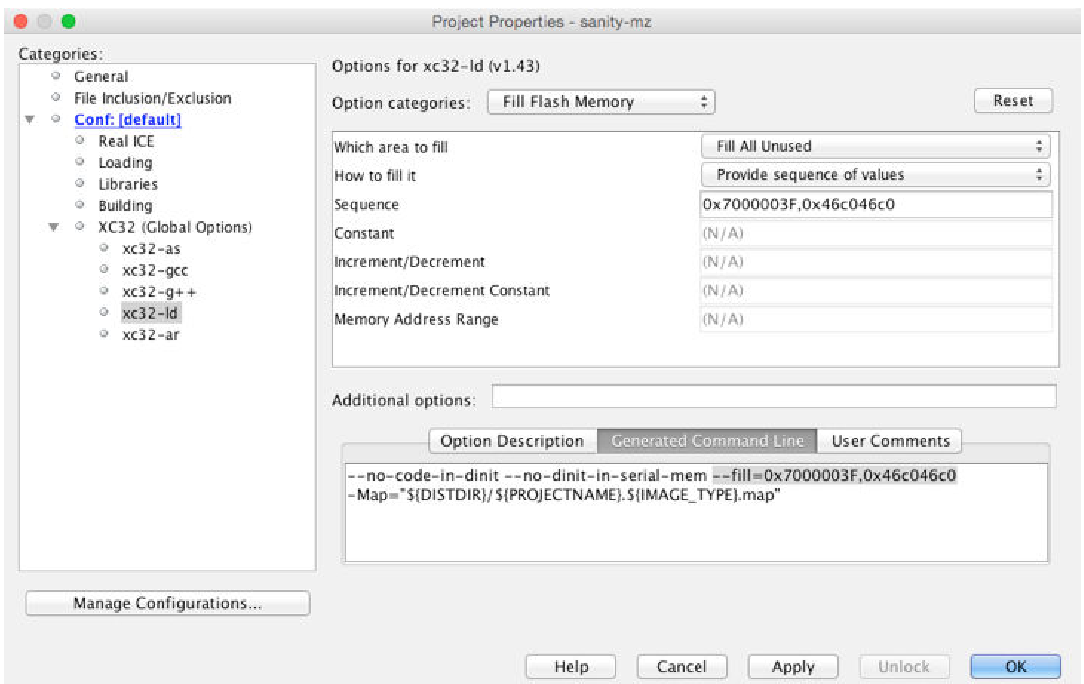
Filling Unused Program Memory

1. In a situation where the CPU execution goes awry and enters into unused program memory space due to an EFT event, the user should consider filling unused program memory with a trap instruction sequence to stop the runaway code, and to allow a WDT time-out and reset. There are various means to do this, and as a suggestion, consult your development tools manual or compiler user manual for cases where there may be a compiler macro available. The following example describes a method using MPLAB® X IDE.

   1.1. For PIC32MX Devices (MIPS32 and MIPS16e)



1.2. For PIC32MZ and PIC32MK Devices (MIPS32 and microMIPS)



11.2 Program Memory and System Integrity Verification

In a poorly protected circuit design, a severe EFT event can compromise the integrity of the Flash memory and hence the application code. One method to protect the application is to insure the Flash content integrity using a checksum approach.

1. Write a Flash program memory checksum function, as shown in the following PIC32 code example. The function should calculate a checksum on all program memory locations from location zero, up to but not including, the last four PM words where the user checksum could be stored.
2. If the user implemented the EFT detector circuit (see Figure 11-2) the user software could optionally elect to:
   2.1. Perform a Flash program memory verification on an EFT-detected event and not on normal power-up resets.
   2.2. Run Class B Safety Library tests on an EFT-detected event and not every reset.

Components Covered by the Class B Safety Software Library

MCU Circuit Component Fault/Error:

1. CPU registers stuck
2. Program counter stuck
3. Interrupt handling and execution: No interrupts or too many interrupts
4. Clock frequency: Clock failure or incorrect frequency
5. Memory testing (Flash/EEPROM): All single bit faults
6. Memory testing (RAM) DC fault

Most CPU manufactures offer free Class B libraries (refer to http://www.microchip.com/design-centers/home-appliance/class-b-safety-software).

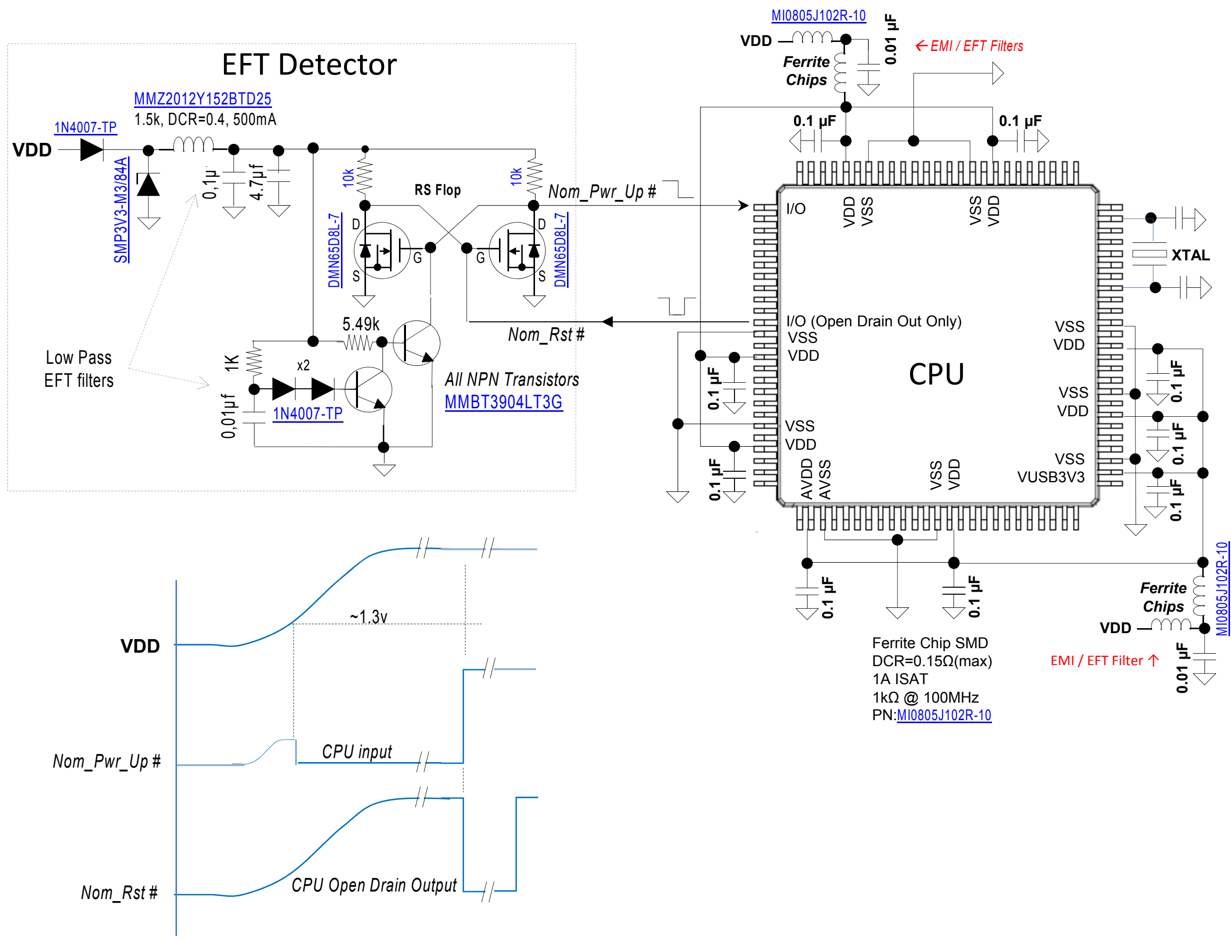
```
PIC32 EXAMPLE ONLY:
//*************************************************
// For compile, user must define:
// Class_B_Tests() user defined function
// PM_Error() user defined function
// Err_Rpt() user defined function
//*************************************************
  #include <string.h>
  #include <stdint.h> // Defines uint32_t
  #include <xc.h>     // Defines __KSEG0_PROGRAM_MEM_BASE &
                      // __KSEG0_PROGRAM_MEM_LENGTH for PIC32M

//***********************************************************
// These are predefined XC32 product header file defines
//
// __KSEG0_PROGRAM_MEM_BASE
// __KSEG0_PROGRAM_MEM_LENGTH
//***********************************************************
// The starting address of the last 4 words in program memory are:
  #define CHECKSUM ((__KSEG0_PROGRAM_MEM_BASE + __KSEG0_PROGRAM_MEM_LENGTH)-16)
  #define EFT                        //Comment out if no EFT detector circuit
  #define PORTCbits.RC12 Nom_Pwr_Up //Example only

  extern const uint32_t __attribute__((address(CHECKSUM))) inputData[4];

main(void)
{
    uint32_t EFT_err=0;

    if(RCONbits.POR || RCONbits.BOR)
    {
        RCONbits.POR = 0;
        RCONbits.BOR = 0;

        #ifdef EFT //If EFT hardware detector circuit present
        if (Nom_Pwr_Up) //If EFT reset event detected
        {
            if (!PM_Checksum_Calc)   //If PM chksum fails
            {
                PM_Error(); //PM integrity compromised, Report
                            //error & go to safe condition
                EFT_err = (EFT_err | 0x1);
            }
            if (!Class_B_Tests())
```

```
            {
                Err_Rpt();   //Report Class_B failure
                EFT_err = (EFT_err | 0x2);
            }
            while (EFT_err);  //If Chksum or Class_B error wait forever
        }
        #else
        {
            if (!PM_Checksum_Calc())
            {
                PM_Error(); //PM integrity compromised
                EFT_err = (EFT_err | 0x1);
                while (EFT_err);  //If Chksum err wait forever
            }
        }
        #endif
    }

    //*********************************
    //USER APPLICATION CODE HERE
    //*********************************

} //END MAIN

//************************************************************************************
// Program Memory Code Integrity Verification Function
// Call this function in case of a possible EFT, Electrical Fast Transient,
// event where the Flash content may have been compromised.
// NOTE: This algorithm should provide ~100,000 to 1 chance that a random
// Flash pattern would match the user checksum.
//************************************************************************************
int PM_Checksum_Calc (void)
{
    uint32_t *checksum_ptr;
    uint32_t checksum_array[4], carry, loop_cnt, start_addr=__KSEG0_PROGRAM_MEM_BASE;
    uint64_t sum;
    for (loop_cnt=0; loop_cnt < 4; start_addr+= 4, loop_cnt++)
    {
        sum=0;
        carry = 0;
        checksum_ptr = (uint32_t *) start_addr;
        while ( (uint32_t)checksum_ptr < CHECKSUM)
        {
            sum = (sum + *checksum_ptr );
            sum = (sum * 2);
            if (sum > 0xFFFFFFFF)
            {
                carry++;
                sum = (sum & 0xFFFFFFFF);
            }
            checksum_ptr += 4;
        }
        checksum_array[loop_cnt] = (uint32_t) (sum + carry);
    }

    //**********************************************************************
    // Place user breakpoint here for very first time only to read checksum values
    // from “checksum_array” for insertion into “inputData” Flash constant data
    // section in Flash memory, then reprogram device.
    //**********************************************************************
    Nop(); //One time user Breakpoint after code development 100% complete.
           //Code "checksum_array[4]" values into Flash "inputData[4]" constant
           //Flash data array and then reprogram device for final release.

    return !memcmp(inputData, checksum_array, 16); //return 1 if match
}

//**********************************************************************
// Define the last 4 words of Program memory to contain the user
// program memory checksum words.
//
// Populate these Flash words with the program memory checksum
// from “checksum_array” inside the “PM_Checksum_Calc” function
// at the indicated debug breakpoint then reprogram device.
//**********************************************************************
const uint32_t __attribute__((address(CHECKSUM))) inputData[4] =
{
    0x00000000, //Checksum 0, user populates these values from
```



```
                    // the PM_Checksum_Calc() breakpoint
    0x00000000, //Checksum 1, then recompiles and reprogram with Checksum 0-3 with values.
    0x00000000, //Checksum 2
    0x00000000  //Checksum 3
};
```

Figure 11-2. EFT Detector Circuit



POR Status Bit	BOR Status Bit	"Nom_Pwr_Up#" Input Pin Logic Level	Type of Event	User Action
1	1	0	Non-EFT	Toggle "Nom_Rst" (1 µs min)
0	1	0	Non-EFT	Toggle "Nom_Rst" (1 µs min)
1	1	1	EFT	Run Code/system Verification
0	1	1	EFT	Run Code/system Verification

11.2.1 EFT Circuit Theory of Operation

A more appropriate name for the EFT detector circuit (see Figure 11-2) is a non-EFT detector. A power or ground EFT event lasts from 1 ns to100 ns, which is far faster than a normal 200 µs to 8 ms power supply power-up sequence. It is much easier to develop a forgiving low-speed detection circuit rather, than the one required to respond to a typical 1 to 5 ns rise time EFT spike. Therefore, the circuit in Figure 11-2, only detects normal non-EFT POR and BOR events. The low-pass filters will insure that an EFT event will not trigger the transistor RS flip-flop and clear the “Nom_Pwr_Up” signal; however, a normal power-up sequence will.

The CPU POR/BOR logic circuits cannot distinguish an EFT from normal power-up or power-down, and therefore, neither can the user's software. Either type of event will trigger the CPU POR/BOR. However, by adding the “non-EFT” detector circuit that will respond only to normal Power-up sequences, there is another status that can break the tie. Since the most common CPU reaction to an EFT event is a reset, the user software can by virtue of interrogating the BOR, POR reset status register and the “Nom_Pwr_Up” I/O input signal, determine if it was an EFT event reset or a normal power up or brown-out reset.

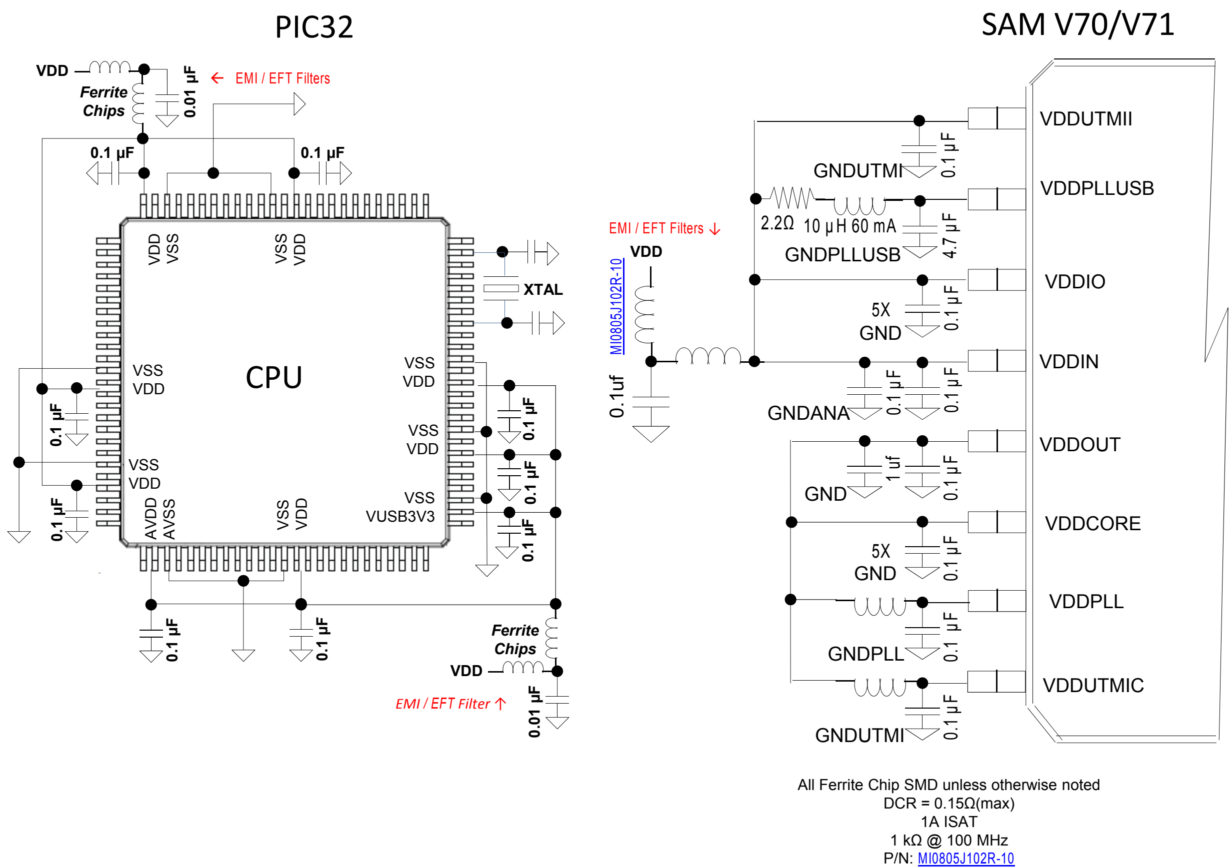
After a normal power-up reset the “Nom_Pwr_Up” output from the transistor RS flip-flop is reset to a logic low. The user's code would then immediately set the RS flip-flop by writing a momentary logic '0' followed by writing a logic '1' to the open drain output pin that is signal “Nom_Rst”, which will set “Nom_Pwr_Up” to a logic '1'. Recall that only a normal POR/BOR CPU reset will clear “Nom_Pwr_Up” to a logic '0'. Therefore, on any subsequent reset by virtue of a return to the beginning of “main” and/or interrogation of the reset status register, if “Nom_Pwr_Up” signal is still a logic '1', the CPU was reset by an EFT event, conversely if “Nom_Pwr_Up” is a logic '0' it was a normal reset. The users code therefore after a potential damaging EFT event can opt to do code and system integrity checks and on any failures can put the application in a safe state and report the error (i.e., run-time program memory code checksums and Class B Library verification tests).

There is a steering diode, TVS, a low-pass LC filter, and large enough caps to insure the operating voltage of the EFT detector, which remains valid even during the EFT power disruption.

12. ESD, EMI, and EFT Hardware Circuit Schematic Protection Examples

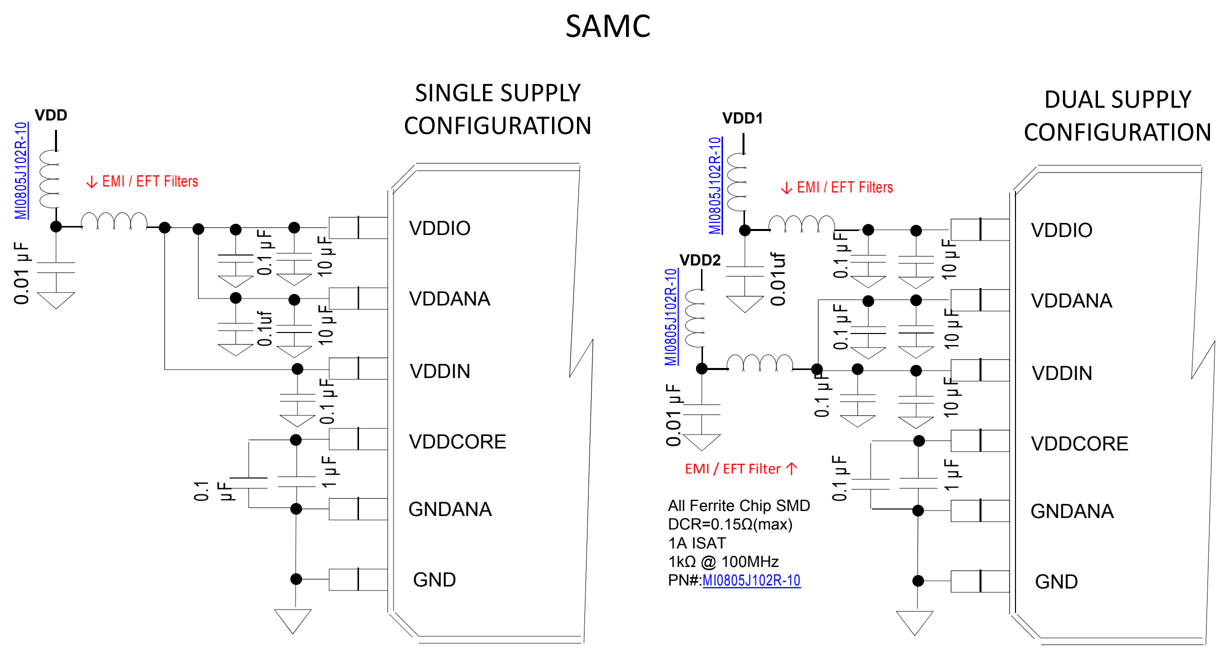
12.1 CPU Protection

Figure 12-1. PIC32 and SAMV70/V71 Circuit Protection Example



Note: All CPU AVSS/VSS and filter bypass capacitor ground connections should be directly connected to the ground plane and not through a trace to ground, and on same side of board as the CPU. Bypass and filter caps must be placed as close as possible to pins.

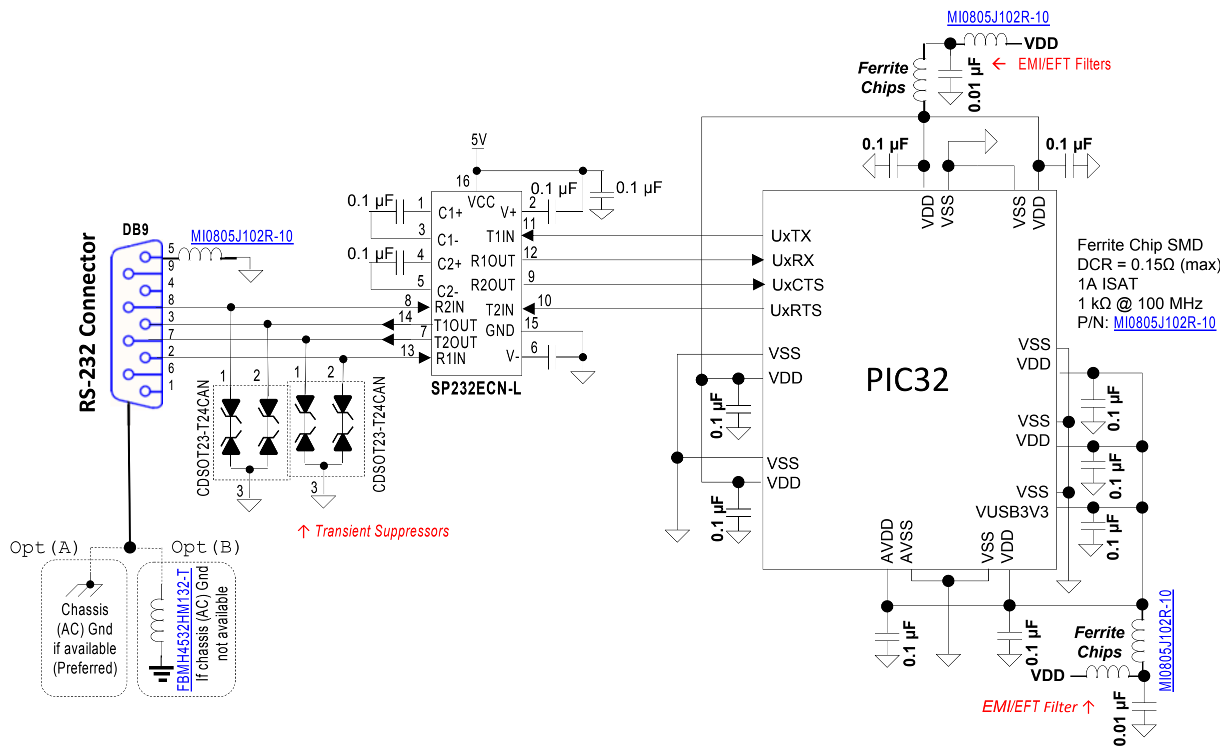
Figure 12-2. SAMC CPU Protection Example



Note: All CPU AVSS/VSS and filter bypass capacitor ground connections should be directly connected to the ground plane and not through a trace to ground, and on same side of board as the CPU. Bypass and filter caps must be placed as close as possible to pins.

12.2 UART RS-232 Schematic Protection

Figure 12-3. UART RS-232 Schematic Protection Example

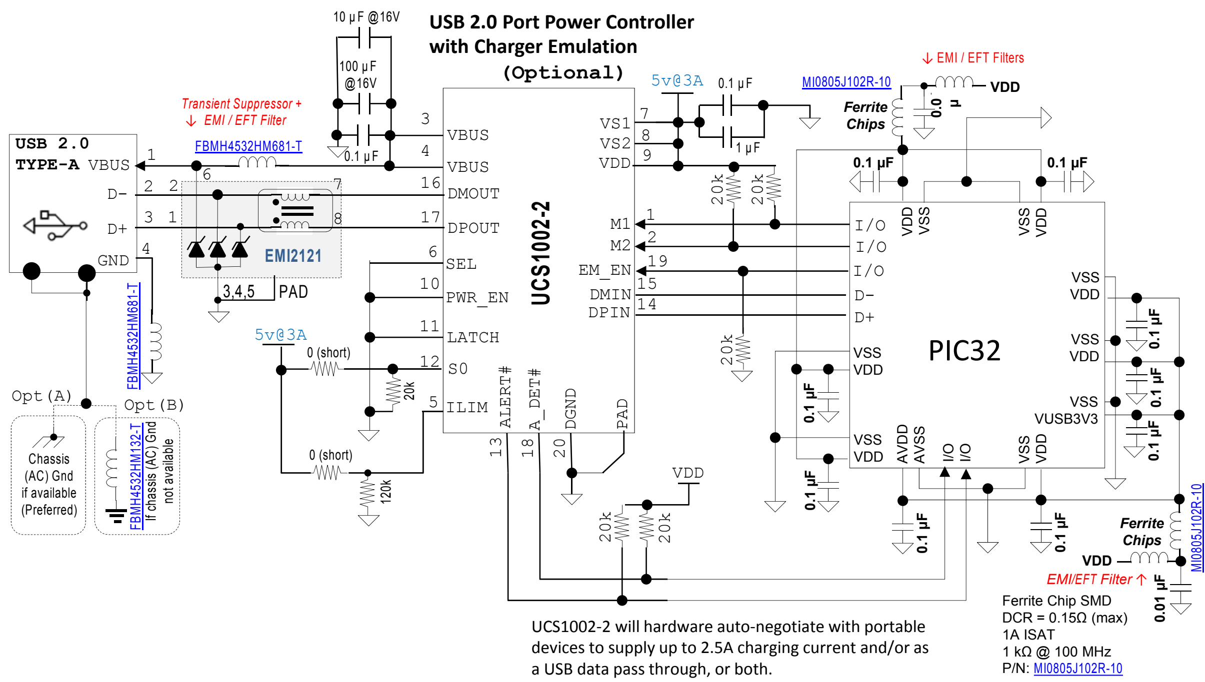


Note:

1. The TVS ground MUST be tied directly to the ground plane and not to a ground trace to minimize inductance. In addition, TVS should be located as close to the external DB9 connector as possible.
2. All CPU AVSS/VSS and filter bypass capacitor ground connections should be directly connected to the ground plane and not through a trace to ground, and on the same side of the board as the CPU.

12.3 USB 2.0 Schematic Protection

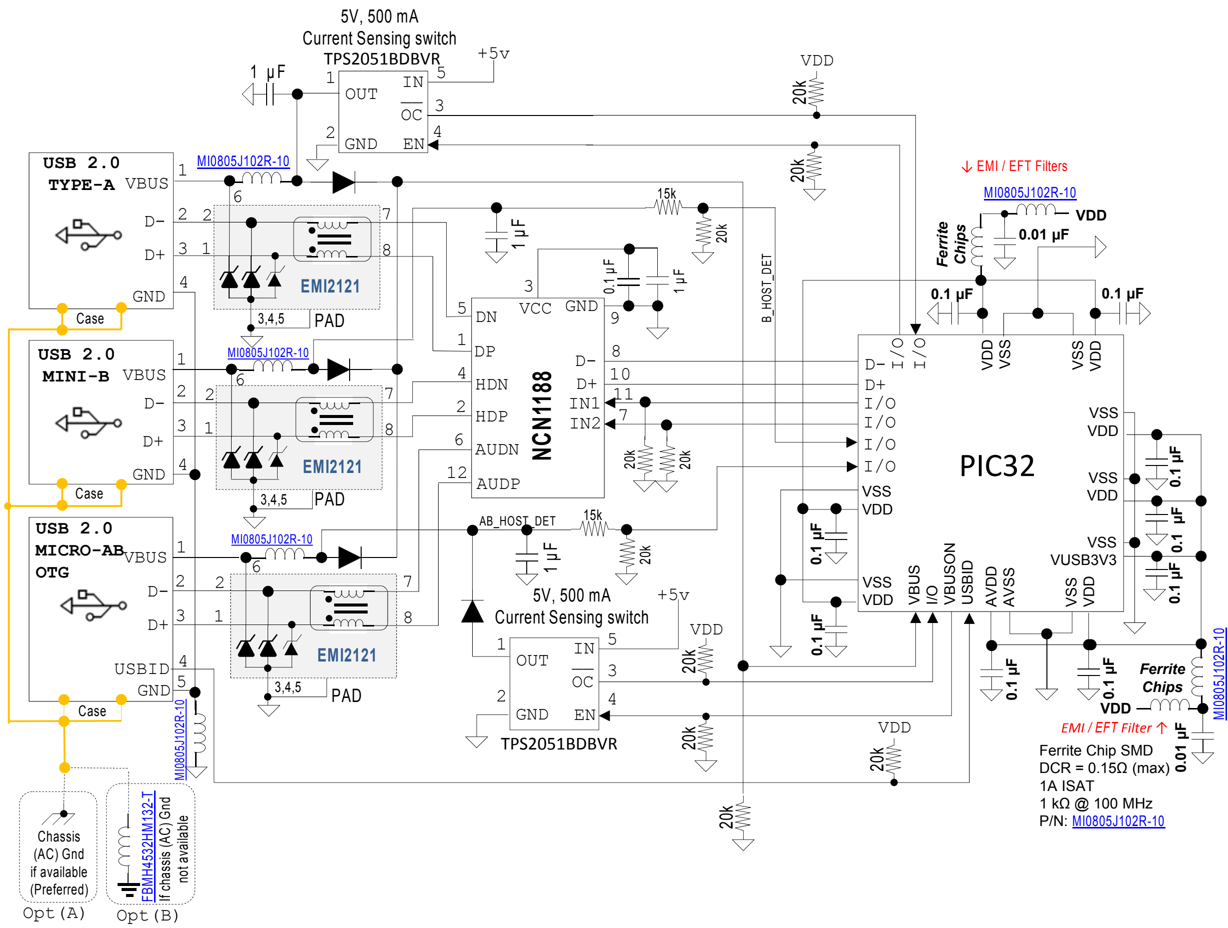
Figure 12-4. USB 2.0 Schematic Protection Example



Note:

1. Ground connection on all TVS must be directly connected to the ground plane and not through a trace to ground to minimize inductance. In addition, they should be located as close to the external USB Connector as possible.
2. The 5V supply required amperage rating depends on the UCS1002-2 ILIM resistor settings that determine the maximum available USB charging current up to 2.5A.
3. USB D+ and D- differential controlled layout rules apply. PCB layout should maintain 90 ohm controlled impedance. USB signals should not transition PCB layers, (i.e. no feed through holes.), and no broken ground, (i.e., ground voids), beneath D+ and D-.
4. All CPU AVSS/VSS and filter bypass capacitor ground connections should be directly connected to the ground plane and not through a trace to ground, and on the same side of the board as the CPU.

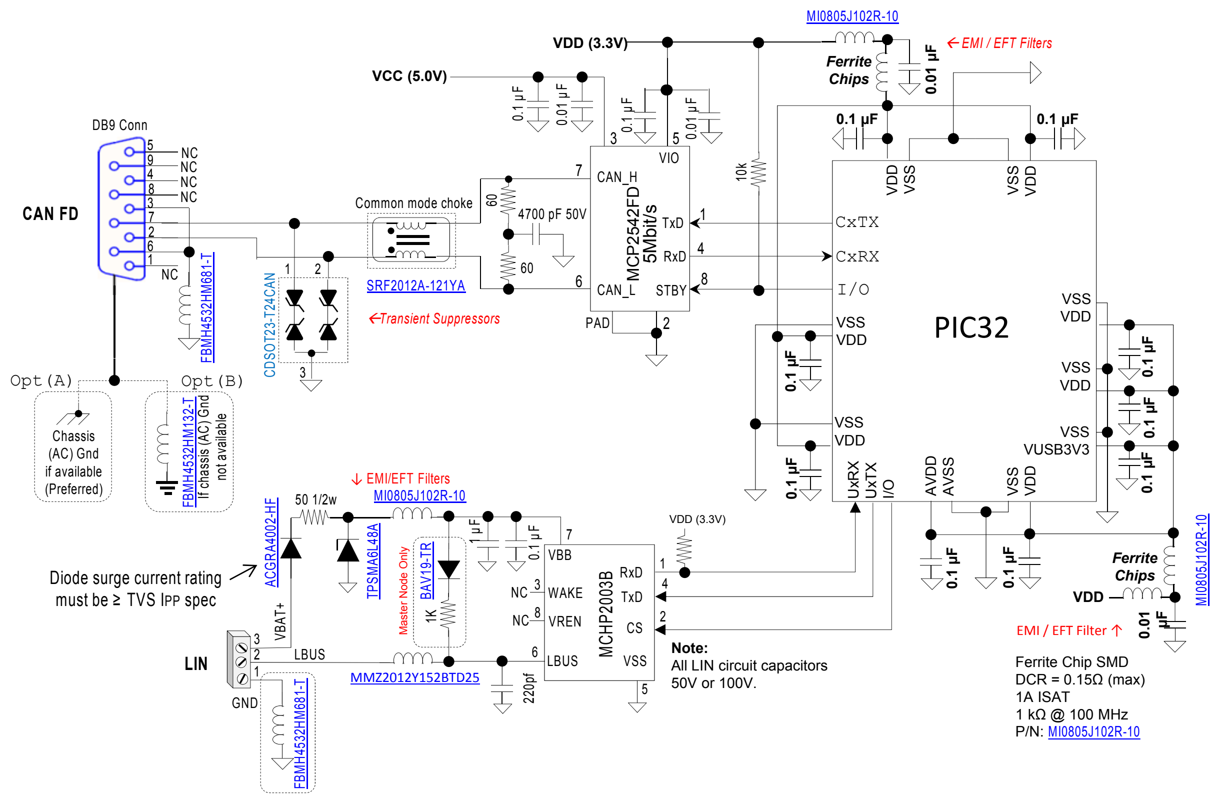
Figure 12-5. Multi-USB 2.0 Port Protection Example



Note: USB D+ and D- differential controlled layout rules apply. PCB layout should maintain 90Ω controlled impedance. USB signals should not transition PCB layers, (i.e., no feed through holes.), and no broken ground, (i.e., ground voids), beneath D+ and D-.

12.4 Controller Area Network Flexible Data-Rate (CAN FD) and LIN Bus Schematic Protection

Figure 12-6. CAN FD/LIN Bus Schematic Protection Example

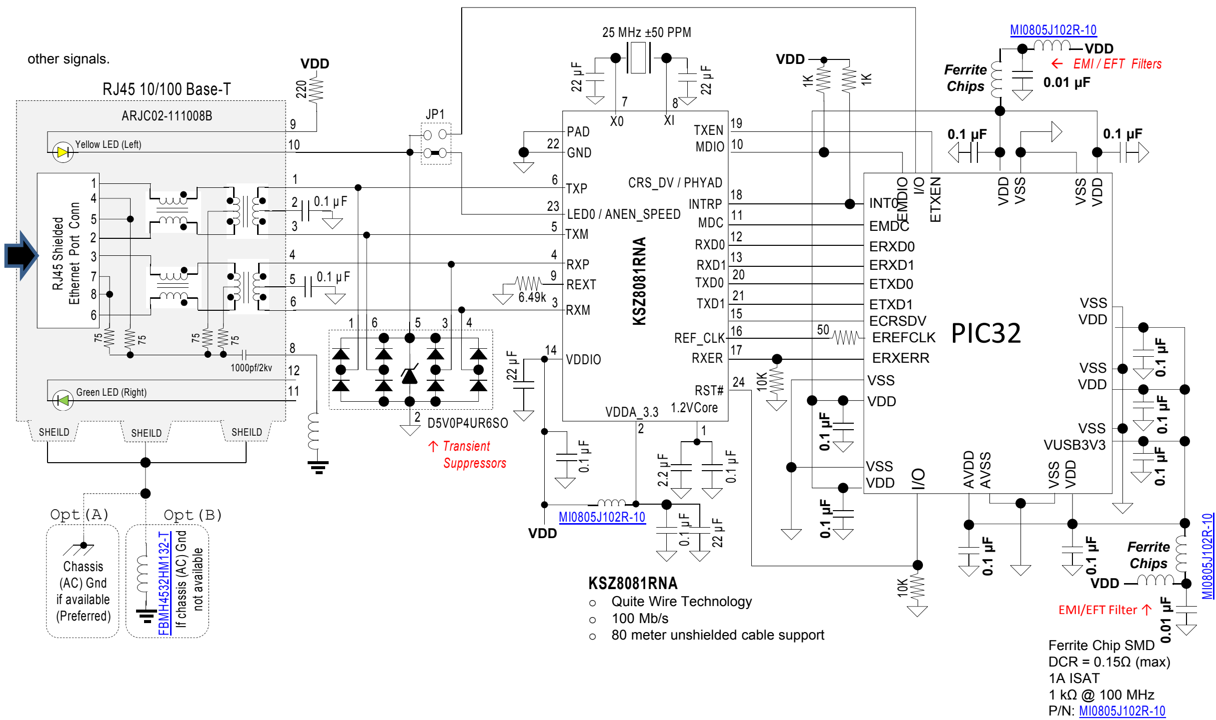


Note:

1. Ground connection on all TVS MUST be directly connected to the ground plane and not through a trace to ground to minimize inductance. In addition, they should be located as close to the external DB9 and LIN Connector as possible.
2. All CPU AVSS/VSS and filter bypass capacitor ground connections should be directly connected to ground plane and not through a trace to ground and on the same side of board as CPU.

12.5 Ethernet Schematic Protection

Figure 12-7. Ethernet Schematic Protection Example

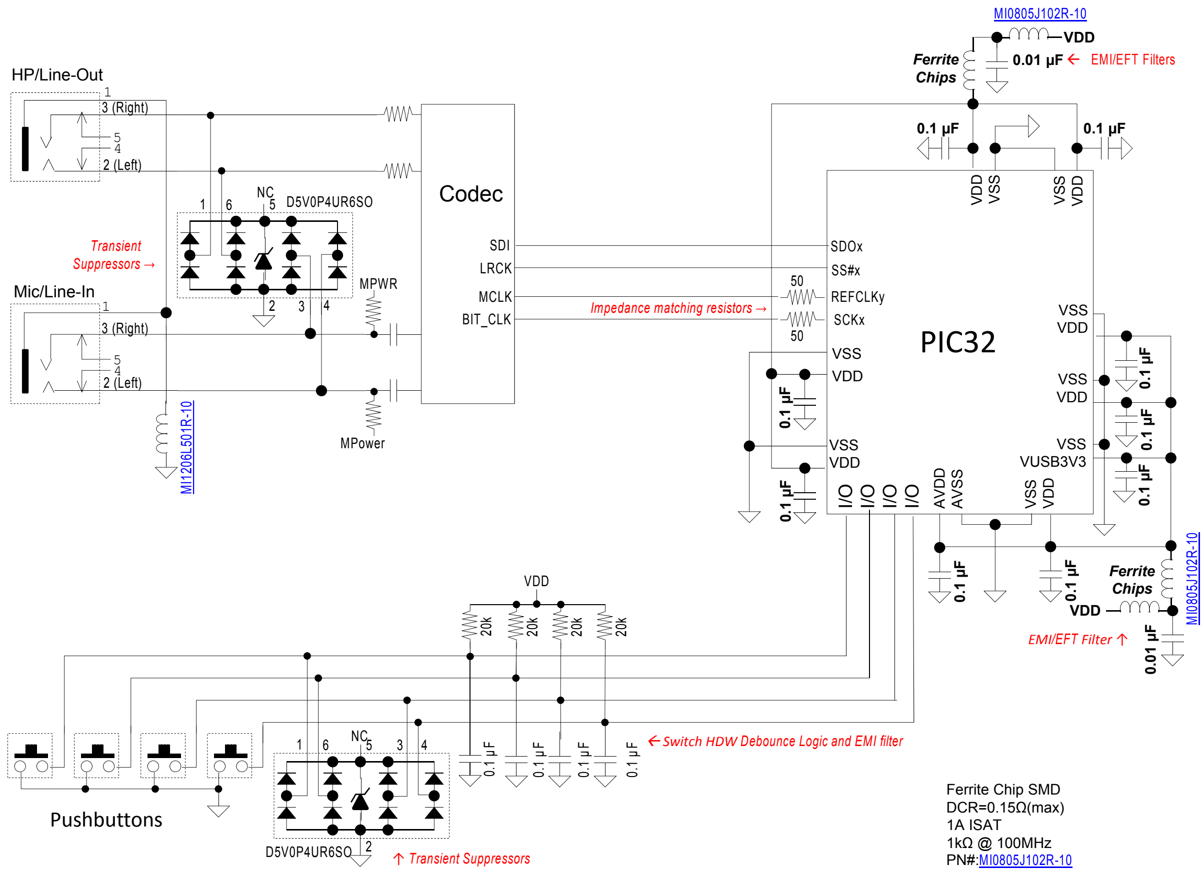


Note:

1. Route both traces of each differential pair as identical to each other as possible at 6 mil width/6 mil parallel spacing, and at least 18 mils away from all other signals.
2. Ground connection on all TVS MUST be directly connected to the ground plane and not through a trace to ground to minimize inductance. In addition, they should be located as close to the external RJ-45 connector as possible.
3. All CPU AVSS/VSS and filter bypass capacitor ground connections should be directly connected to the ground plane and not through a trace to ground and on the same side of the board as the CPU and as close as possible to the pins.
4. The user software must insure KSZ8081RN VDD minimum rise time ≥ 300 µs. The KSZ8081RN RST# signal must be asserted low for ≥ 500 µs. After RST# deassertion, user software must wait > 100 µs before attempting to configure the KSZ8081RN.

12.6 Audio Headphone and Microphone Schematic Protection

Figure 12-8. Audio Headphone and Microphone Schematic Protection Examples

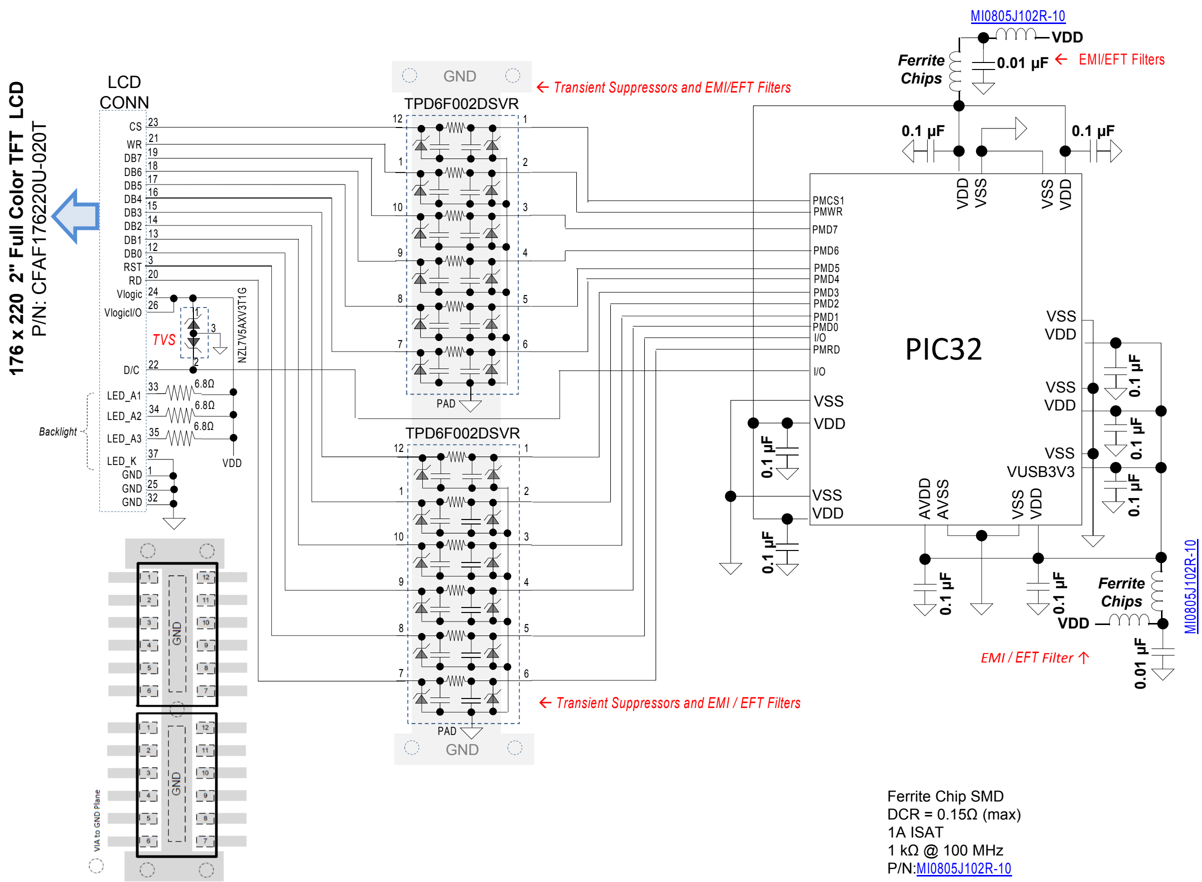


Note:

1. The TVS ground MUST be tied directly to the ground plane and not to a ground trace to minimize inductance.
2. The Ground connection on all TVS MUST be directly connected to the ground plane and not through a trace to ground to minimize inductance. In addition, they should be located as close to the external audio jacks connectors and switches as possible.
3. All CPU AVSS/VSS and filter bypass capacitor ground connections should be directly connected to the ground plane and not through a trace to ground and on the same side of the board as the CPU.

12.7 Typical LCD Interface Schematic Protection

Figure 12-9. Typical LCD Interface Schematic Protection

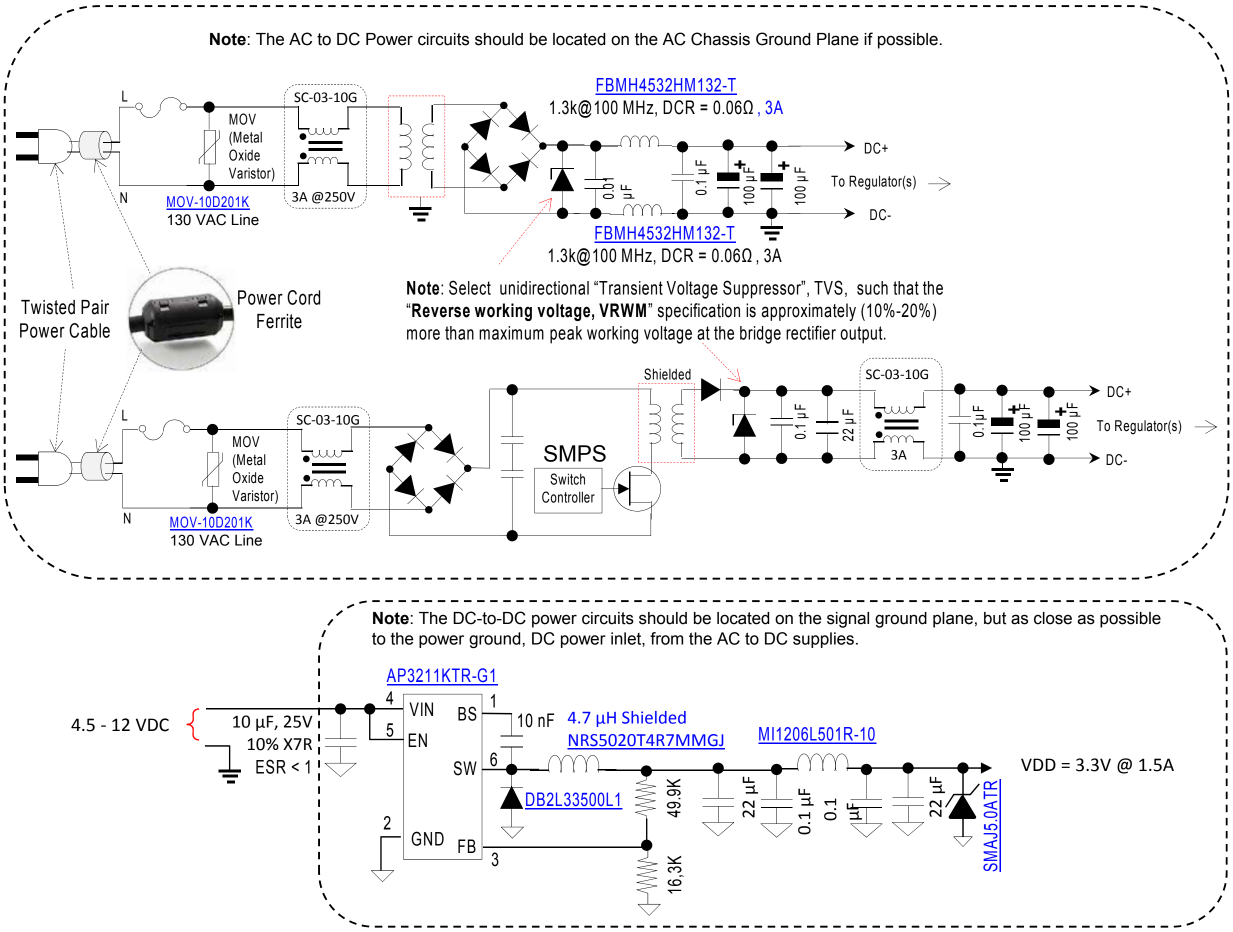


Note:

1. Ground connection on all TVS MUST be directly connected to the ground plane and not through a trace to ground to minimize inductance. In addition, they should be located as close to the external LCD connector as possible.
2. All CPU AVSS/VSS and filter bypass capacitor ground connections should be directly connected to the ground plane and not through a trace to ground, and on the same side of the board as the CPU.

12.8 ESD, EMI, and EFT Power Supply Sub-system Schematic Protection

Figure 12-10. EMI/EFT/ESD Power Supply Sub-system Schematic Protection Example

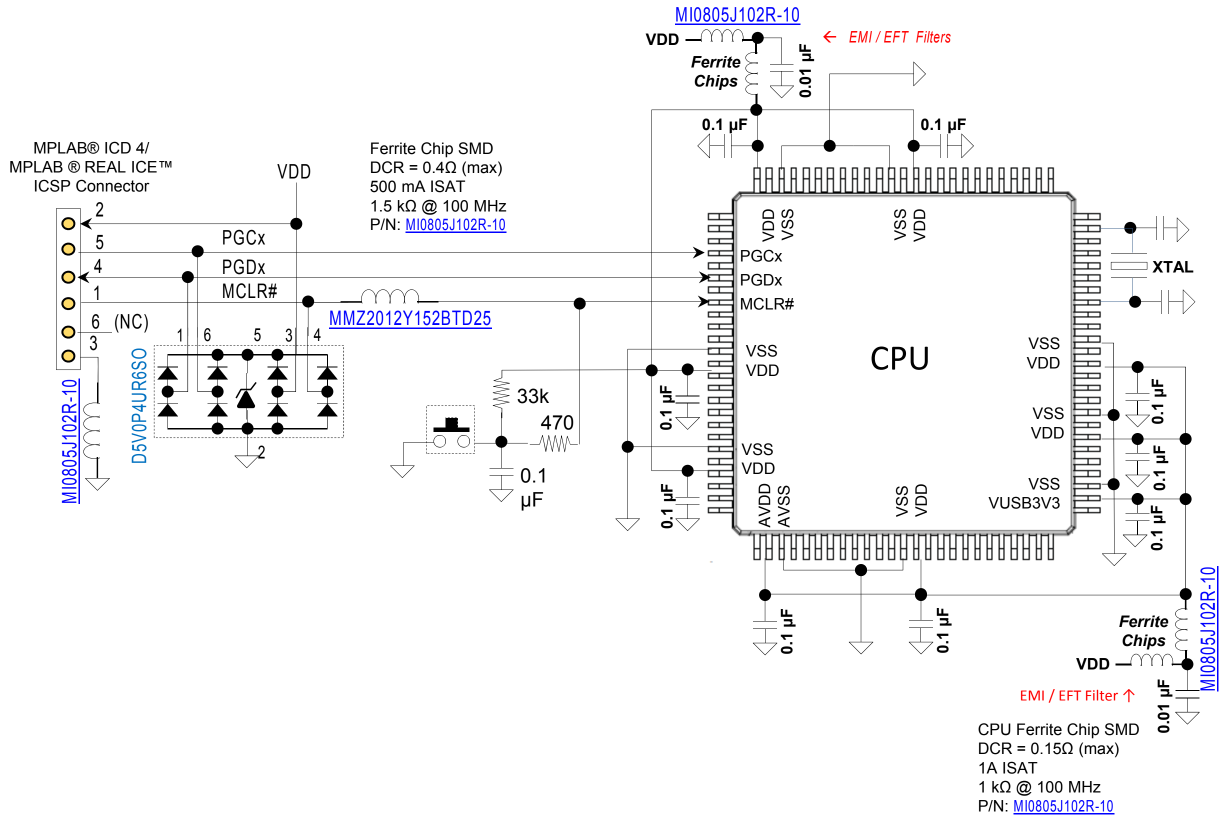


Note:

1. If possible, the AC to DC Power circuits should be located on the AC Chassis Ground Plane.
2. The DC to DC power circuits should be located on the signal ground plane, but as close as possible to the power ground DC power inlet from the AC to DC supplies.

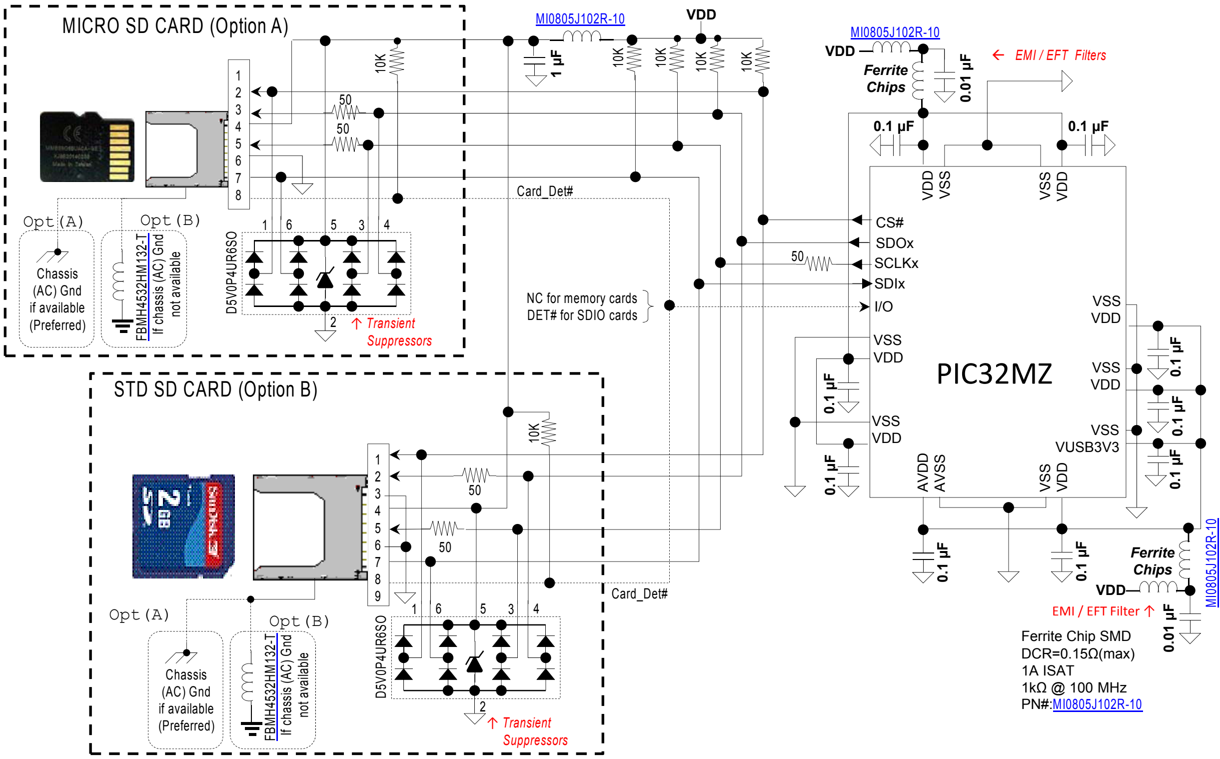
12.9 Reset and Programming Interface Schematic Protection

Figure 12-11. Reset/Programming Interface Schematic Protection Example



12.10 Secure Digital (SD) Memory Card Interface Schematic Protection

Figure 12-12. SPI SD Card Protection Example

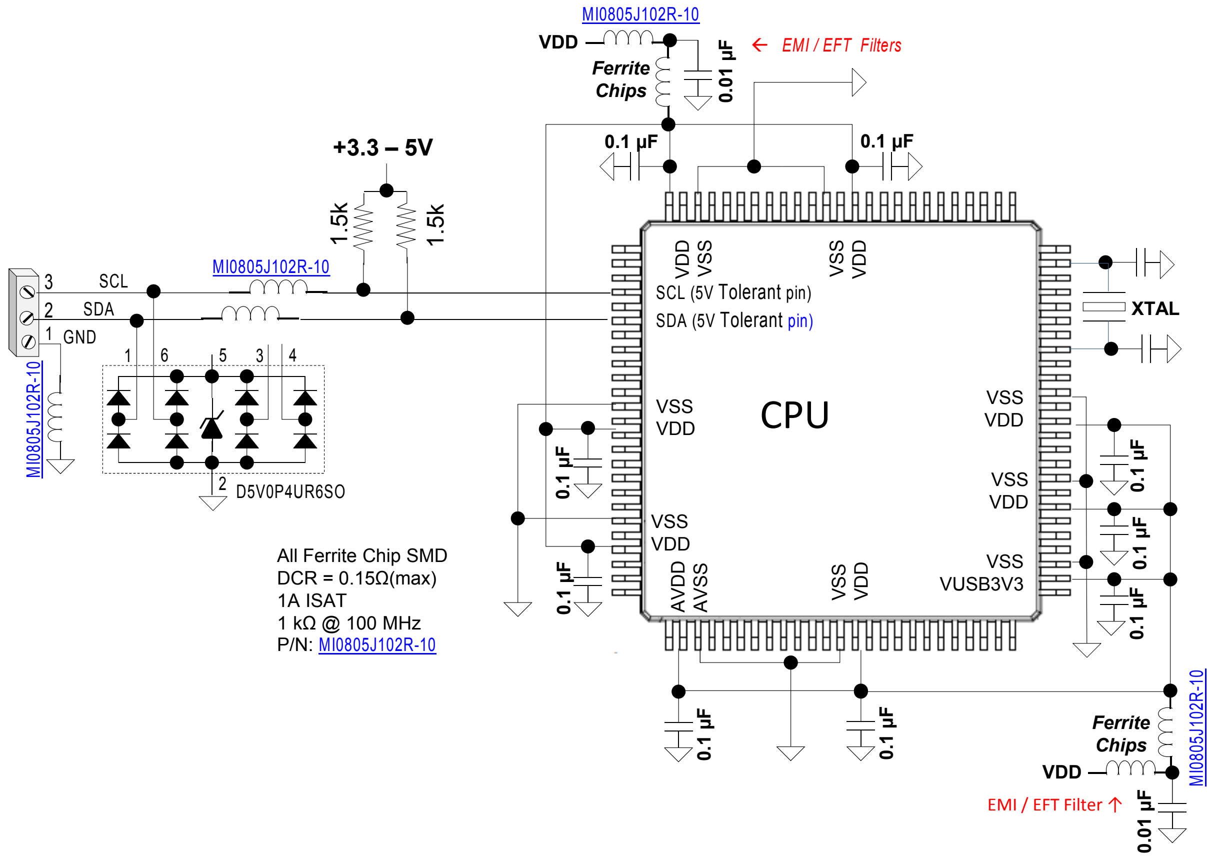


Note:

1. All CPU AVSS/VSS and filter bypass capacitor ground connections should be directly connected to the ground plane and not through a trace to ground, and on the same side of the board as the CPU.
2. Ground connection on all TVS must be directly connected to the ground plane and not through a trace to ground to minimize inductance. In addition, they should be located as close as possible to the external SD card connector.

12.11 I2C Interface Schematic Protection

Figure 12-13. I2C Protection Example



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