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Microchip's Clock Devices' Compliance with PCIe 4.0

Author: *Maurizio Gavardoni*
Microchip Technology Inc.

INTRODUCTION

PCI Express (PCIe) is a point-to-point serial communication standard that operates in consumer, computing, server, and storage applications. In virtually all modern computers, from consumer laptops and desktops to enterprise data servers, the PCIe bus serves as the primary motherboard-level interconnect, connecting the host system-processor with both integrated-peripherals and add-on peripherals (expansion cards). Currently, there are four generations of PCIe that each support different data rates. The latest generation, PCIe 4.0, supports the highest data rate of 16 Gbps.

This application note describes the requirements for the reference clock in the fourth and latest generation of PCIe and provides some ready-to-use Microchip clock solutions that are compliant with PCIe 4.0.

PCI EXPRESS SYSTEM OVERVIEW

Figure 1 below shows the block diagram of a generic PCIe system with the assumption of using a common clock architecture that feeds both the PCIe transmitting device as well as the PCIe receiving device. Each device has its own PLL that exhibits a 2nd order low-pass filter characteristic.

The receiver also uses a Clock Data Recovery (CDR) circuit that exhibits a high-pass filter characteristic (1st order).

The PCIe reference clock's jitter specification is given at the receiver latch. The transfer function of such a reference clock is defined by the difference function between the transmitter and receiver PLL, multiplied by the receiver CDR high-pass characteristic. The transfer function is also affected by the transport delay of the two paths from the reference clock to the receiver latch: one path goes through the TX PLL while the second path goes through the RX PLL and CDR. The transport delay is applied separately to the TX PLL and the RX PLL transfer functions and the worst case jitter from the two scenarios is considered.

EQUATION 1:

$$H(s) = (H_1(s) \times e^{-sT} - H_2(s)) \times H_3(s) = (H_2(s) \times e^{-sT} - H_1(s)) \times H_3(s)$$

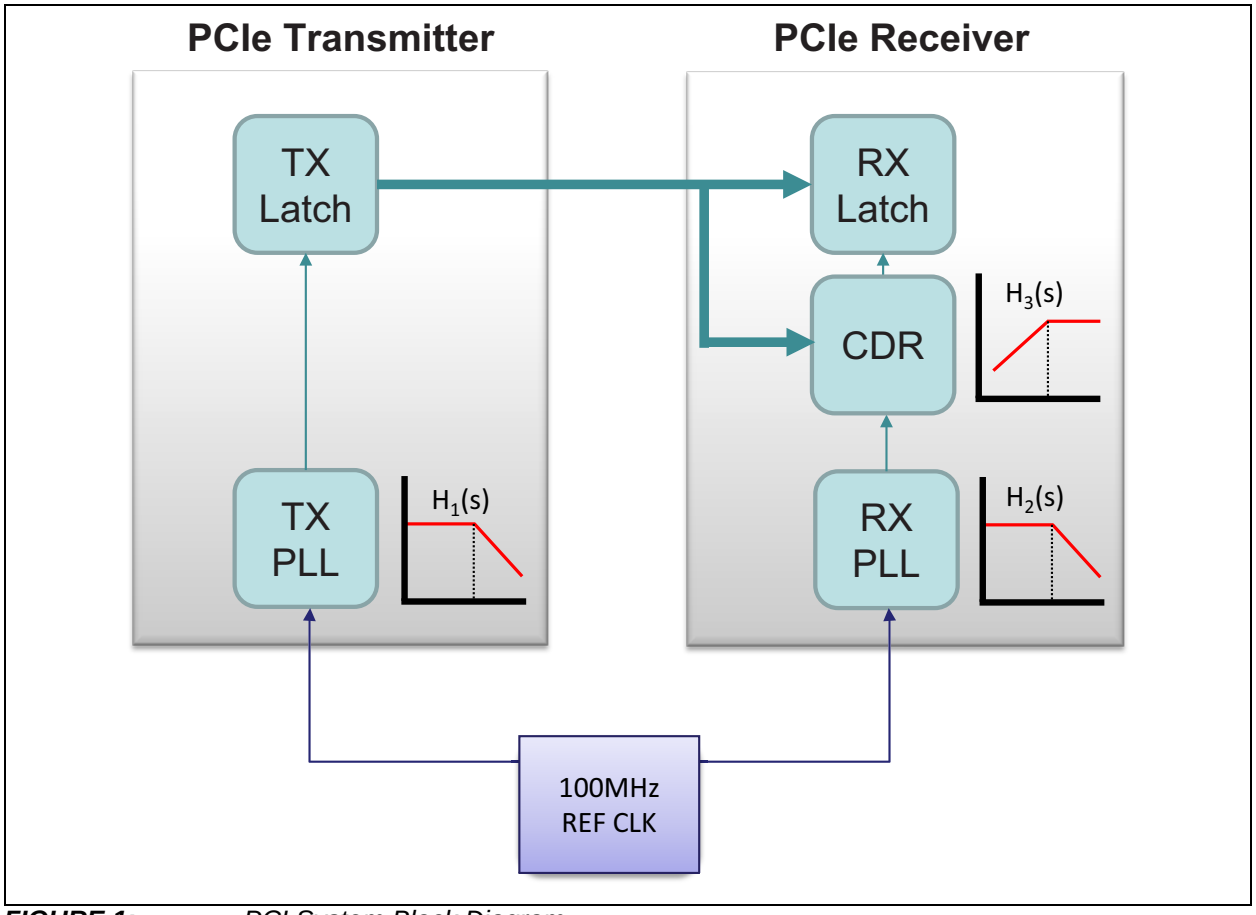

FIGURE 1: *PCI System Block Diagram.*

PCI EXPRESS PHASE NOISE BANDWIDTH AND JITTER REQUIREMENTS

PCIe specifications have historically specified multiple types of filtering. For PCIe 4.0, sixteen combinations of filters are provided, as shown in Table 1. Such combinations result into a phase-noise bandwidth that goes anywhere between 2 MHz – 5 MHz to 10 MHz (see Figure 2). The PCIe phase noise bandwidth is therefore considerably narrower than the traditional benchmark bandwidth from 12 kHz to 20 MHz.

The PCIe 4.0 jitter requirement (given at the receiver latch) is ≤500 fs_{RMS}. Jitter requirements across all PCIe generations are summarized in Table 2 below.

TABLE 1: SUMMARY OF PCIE 4.0 FILTERS

Number	Data Rate	PLL1 BW	PLL1 Peak	PLL2 BW	PLL2 Peak	CDR BW	CDR Peak
1	16 Gbps	2 MHz	0.01 dB	2 MHz	0.01 dB	10 MHz	0 dB
2	16 Gbps	2 MHz	0.01 dB	2 MHz	1 dB	10 MHz	0 dB
3	16 Gbps	2 MHz	2 dB	2 MHz	0.01 dB	10 MHz	0 dB
4	16 Gbps	2 MHz	2 dB	2 MHz	1 dB	10 MHz	0 dB
5	16 Gbps	2 MHz	0.01 dB	5 MHz	0.01 dB	10 MHz	0 dB
6	16 Gbps	2 MHz	0.01 dB	5 MHz	1 dB	10 MHz	0 dB
7	16 Gbps	2 MHz	2 dB	5 MHz	0.01 dB	10 MHz	0 dB
8	16 Gbps	2 MHz	2 dB	5 MHz	1 dB	10 MHz	0 dB
9	16 Gbps	4 MHz	0.01 dB	2 MHz	0.01 dB	10 MHz	0 dB
10	16 Gbps	4 MHz	0.01 dB	2 MHz	1 dB	10 MHz	0 dB
11	16 Gbps	4 MHz	2 dB	2 MHz	0.01 dB	10 MHz	0 dB

TABLE 1: SUMMARY OF PCIE 4.0 FILTERS (CONTINUED)

Number	Data Rate	PLL1 BW	PLL1 Peak	PLL2 BW	PLL2 Peak	CDR BW	CDR Peak
12	16 Gbps	4 MHz	2 dB	2 MHz	1 dB	10 MHz	0 dB
13	16 Gbps	4 MHz	0.01 dB	5 MHz	0.01 dB	10 MHz	0 dB
14	16 Gbps	4 MHz	0.01 dB	5 MHz	1 dB	10 MHz	0 dB
15	16 Gbps	4 MHz	2 dB	5 MHz	0.01 dB	10 MHz	0 dB
16	16 Gbps	4 MHz	2 dB	5 MHz	1 dB	10 MHz	0 dB

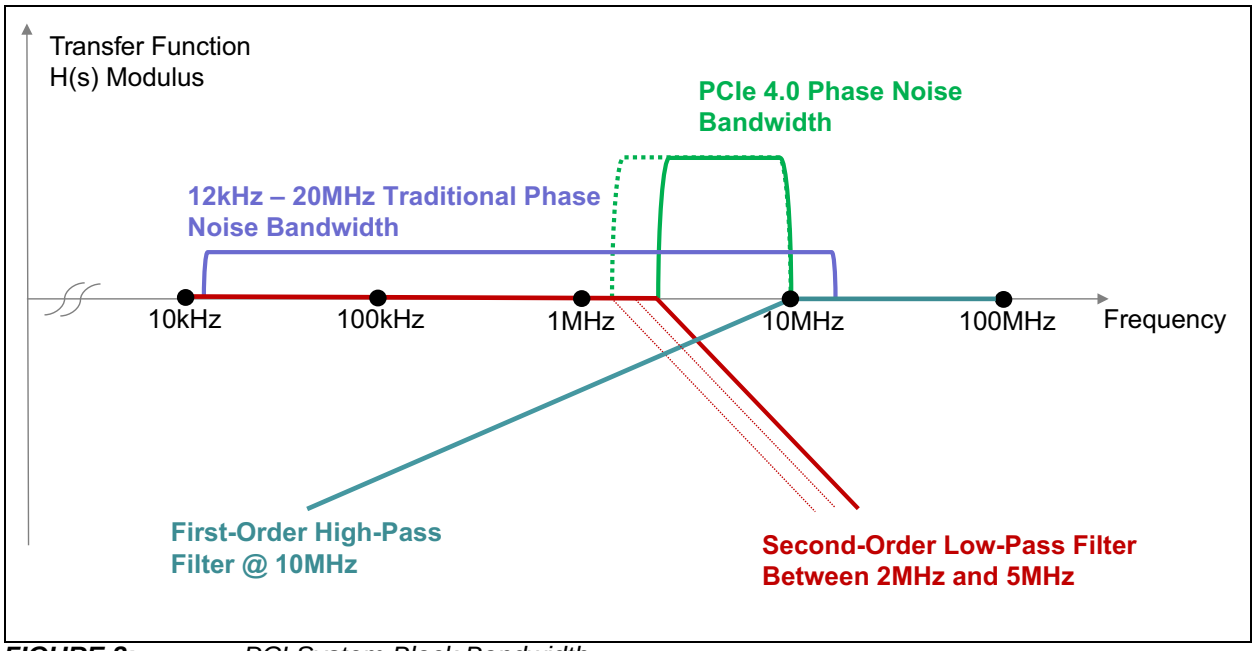

FIGURE 2: *PCI System Block Bandwidth.*

TABLE 2: PCIE DATA-RATE AND JITTER REQUIREMENTS ACROSS GENERATIONS

PCIe Generation	Data Rate	Common Clock Jitter Limit at Receiver Latch
1.0	2.5 Gbps	108 ps Peak-to-Peak
2.0	5 Gbps	3.1 ps_{RMS}
3.0	8 Gbps	1 ps_{RMS}
4.0	16 Gbps	500 fs_{RMS}

MICROCHIP CLOCK DEVICES' COMPLIANCE WITH PCI EXPRESS 4.0

Some Microchip clock generators and buffers have been tested for PCIe 4.0 compliance. All are compliant with the latest generation, PCIe 4.0. Because the jitter requirements of generation four are the most stringent, the same family of devices is also compliant with all the previous PCIe generations.

TABLE 3: PCI EXPRESS 4.0-COMPLIANT MICROCHIP PARTS

Part Number	Device Family	Device Family URL	PCIe 4.0 Compliance
DSC557, DSC400, DSC1104	MEMS Technology	http://www.microchip.com/wwwproducts/en/DSC557-03	PASS
SM802xxx	High performance clock generator with external crystal/ reference	http://www.microchip.com/wwwproducts/en/SM802XXX	PASS
MX85xxxx	High performance clock generator with integrated crystal	http://ww1.microchip.com/downloads/en/device-doc/mx85xxxx.pdf	PASS
PL602-21	Clock generator with crystal input (–130 dBc at 10 kHz offset)	http://www.microchip.com/wwwproducts/en/PL602-21	PASS
SY75576L/8L	HCSL multi-output buffers	http://www.microchip.com/wwwproducts/en/SY75576L	PASS

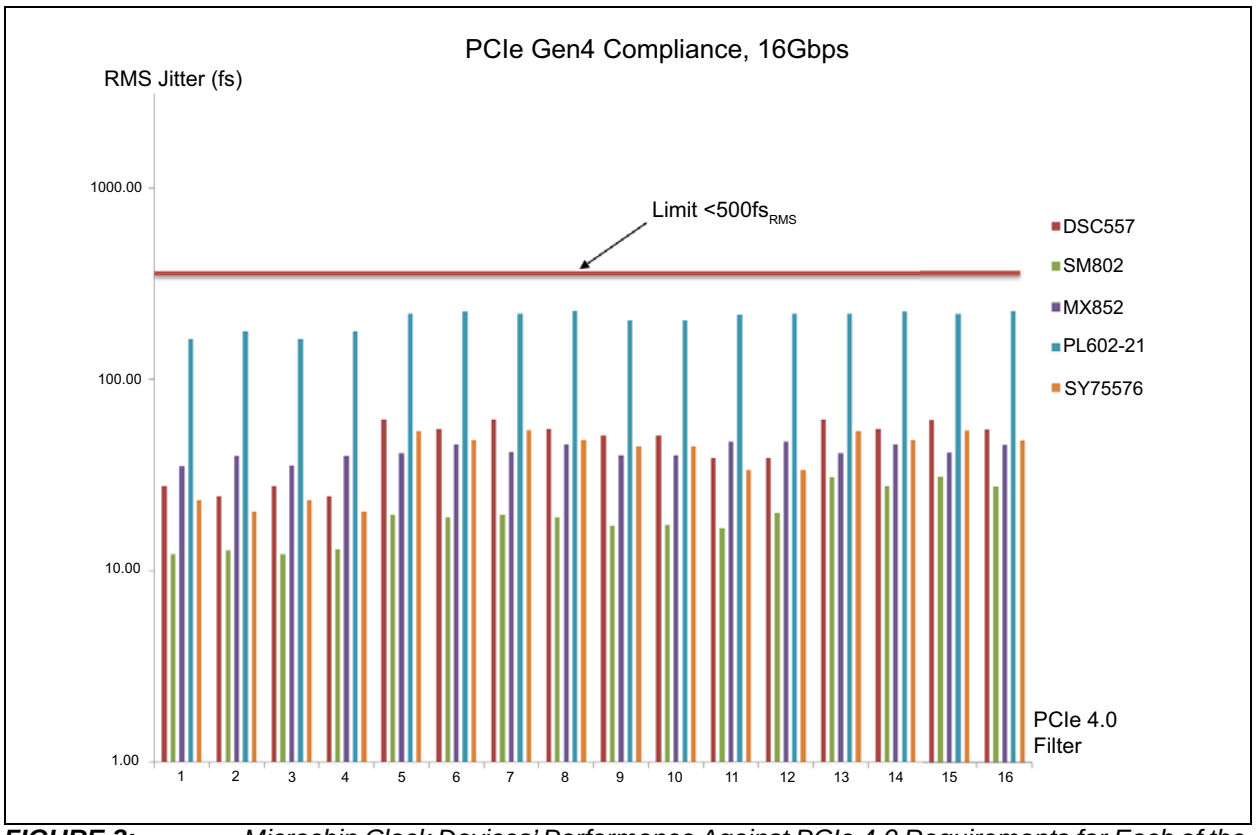

FIGURE 3: *Microchip Clock Devices' Performance Against PCIe 4.0 Requirements for Each of the 16 Filters.*

TABLE 4: SUMMARY OF PCIE 4.0 FILTERS AND MICROCHIP CLOCK DEVICES TEST RESULTS

Number	DSC557	Test Result	SM802xxx	Test Result	MX85xxxx	Test Result	PL602-21	Test Result	SY75576L	Test Result
1	27.53	PASS	12.18	PASS	35.20	PASS	161.54	PASS	23.46	PASS
2	24.44	PASS	12.81	PASS	39.56	PASS	177.09	PASS	20.36	PASS
3	27.61	PASS	12.22	PASS	35.31	PASS	162.05	PASS	23.53	PASS
4	24.46	PASS	12.82	PASS	39.59	PASS	177.25	PASS	20.38	PASS
5	61.63	PASS	19.52	PASS	41.26	PASS	218.61	PASS	53.91	PASS
6	54.75	PASS	19.02	PASS	45.41	PASS	226.67	PASS	47.91	PASS
7	61.68	PASS	19.54	PASS	41.30	PASS	218.81	PASS	53.96	PASS
8	54.8	PASS	19.04	PASS	45.45	PASS	226.88	PASS	47.95	PASS
9	50.86	PASS	17.18	PASS	39.81	PASS	201.39	PASS	44.44	PASS
10	50.98	PASS	17.22	PASS	39.90	PASS	201.85	PASS	44.55	PASS
11	38.73	PASS	16.64	PASS	47.06	PASS	218.14	PASS	33.46	PASS
12	38.82	PASS	20.01	PASS	47.17	PASS	218.64	PASS	33.54	PASS
13	61.63	PASS	30.77	PASS	41.26	PASS	218.61	PASS	53.91	PASS
14	54.75	PASS	27.59	PASS	45.41	PASS	226.67	PASS	47.91	PASS
15	61.68	PASS	30.79	PASS	41.30	PASS	218.81	PASS	53.96	PASS
16	54.8	PASS	27.62	PASS	45.45	PASS	226.88	PASS	47.95	PASS

Note 1: Jitter specification for PCIe 4.0 is <500 fs_{RMS}. All values in the table are fs_{RMS}.

CONCLUSION

Microchip offers several families of clock generators, oscillators, and buffers that are compliant with the latest generation of PCIe. That latest generation, PCIe 4.0, supports the highest data rate of 16 Gbps and is used as the primary motherboard-level interconnect in computers for the consumer, server, and storage markets.

NOTES:

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