JESD204B Clock Generator with 14 LVDS/HSTL Outputs

Data Sheet

AD9528

FEATURES

- 14 outputs configurable for HSTL or LVDS
- Maximum output frequency
  - 6 outputs up to 1.25 GHz
  - 8 outputs up to 1 GHz
- Dependent on the voltage controlled crystal oscillator (VCXO) frequency accuracy (start-up frequency accuracy: <±100 ppm)
- Dedicated 8-bit dividers on each output
  - Coarse delay: 63 steps at 1/2 the period of the RF VCO divider output frequency with no jitter impact
  - Fine delay: 15 steps of 31 ps resolution
- Typical output to output skew: 20 ps
- Duty cycle correction for odd divider settings
- Output 12 and Output 13, VCXO output at power-up
- Absolute output jitter: <160 fs at 122.88 MHz, 12 kHz to 20 MHz integration range
- Digital frequency lock detect
- SPI- and I²C-compatible serial control port
- Dual PLL architecture
  - PLL1
    - Provides reference input clock cleanup with external VCXO
    - Phase detector rate up to 110 MHz
    - Redundant reference inputs
    - Automatic and manual reference switchover modes
      - Revertive and nonrevertive switching
    - Loss of reference detection with holdover mode
    - Low noise LVDS/HSTL outputs from VCXO used for radio frequency/intermediate frequency (RF/IF) synthesizers
  - PLL2
    - Phase detector rate of up to 275 MHz
    - Integrated low noise VCO

APPLICATIONS

- High performance wireless transceivers
- LTE and multicarrier GSM base stations
- Wireless and broadband infrastructure
- Medical instrumentation
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs; supports JESD204B
- Low jitter, low phase noise clock distribution
- ATE and high performance instrumentation

FUNCTIONAL BLOCK DIAGRAM

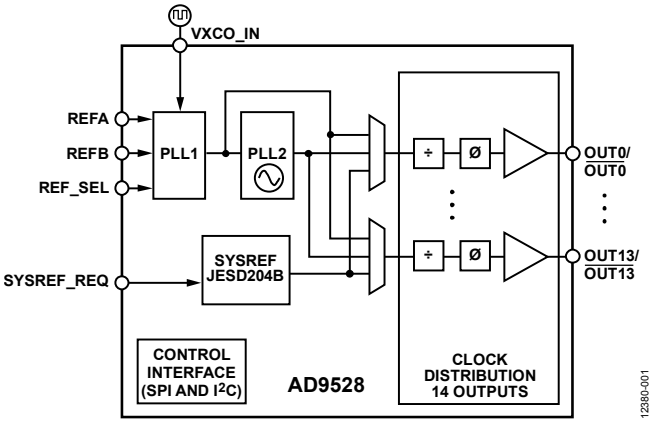


Figure 1.

GENERAL DESCRIPTION

The AD9528 is a two-stage PLL with an integrated JESD204B SYSREF generator for multiple device synchronization. The first stage phase-locked loop (PLL) (PLL1) provides input reference conditioning by reducing the jitter present on a system clock. The second stage PLL (PLL2) provides high frequency clocks that achieve low integrated jitter as well as low broadband noise from the clock output drivers. The external VCXO provides the low noise reference required by PLL2 to achieve the restrictive phase noise and jitter requirements necessary to achieve acceptable performance. The on-chip VCO tunes from 3.450 GHz to 4.025 GHz. The integrated SYSREF generator outputs single shot, N-shot, or continuous signals synchronous to the PLL1 and PLL2 outputs to time align multiple devices.

The AD9528 generates six outputs (Output 0 to Output 3, Output 12, and Output 13) with a maximum frequency of 1.25 GHz, and eight outputs with a maximum frequency of up to 1 GHz. Each output can be configured to output directly from PLL1, PLL2, or the internal SYSREF generator. Each of the 14 output channels contains a divider with coarse digital phase adjustment and an analog fine phase delay block that allows complete flexibility in timing alignment across all 14 outputs. The AD9528 can also be used as a dual input flexible buffer to distribute 14 device clock and/or SYSREF signals. At power-up, the AD9528 sends the VCXO signal directly to Output 12 and Output 13 to serve as the power-up ready clocks.

Note that, throughout this data sheet, the dual function pin names are referenced by the relevant function where applicable.

Rev. D

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

1/2018—Rev. C to Rev. D

Changes to Features Section and General Description Section 1
Added Input Noise Sensitivity Parameter, Table 4 6
Changes to HSTL Mode, Output Frequency Parameter, Test Conditions/Comments Column, Table 8 and LVDS Mode, 3.5 mA, Output Frequency Parameter, Test Conditions/Comments Column, Table 8 7
Changes to $\overline{CS}$ (Input) Parameter, Table 17 13
Changes to Figure 2 and Table 21 16
Changes to Overview Section 25
Added VCXO Input Section 27
Changes to PLL1 Reference Switchover Section 27
Changes to SPI/I²C Port Selection Section and Table 24 35
Change to Figure 53 43
Changes to Table 49 56
Changes to Table 57 59

7/2015—Rev. B to Rev. C

Changes to Differential Input Voltage, Sensitivity Frequency < 250 MHz Parameter and Differential Input Voltage, Sensitivity Frequency > 250 MHz Parameter, Table 4 6
Changes to Figure 12 Caption, Figure 13 Caption, and Figure 14 Caption 20
Changes to Figure 15 Caption, Figure 16 Caption, Figure 17 Caption, and Figure 18 Caption 21
Changes to Figure 27 25
Changes to Implementation Specific Details Section 35
Changes to I²C Serial Port Operation Section 38

4/2015—Rev. A to Rev. B

Changes to Serial Control Port Section and Table 24 35

3/2015—Rev. 0 to Rev. A

Moved Revision History 3
Changes to Table 8 7
Changes to Voltage Parameter, Table 15 12
Changes to Figure 2 16
Added Figure 13, Renumbered Sequentially 20
Deleted Figure 17 21
Added Figure 15 21
Changes to Figure 16 Caption 21
Changes to Figure 27 25
Changes to SYSREF Generator Section 34
Changes to Serial Control Port Section and Implementation Specific Details Section 35
Changes to Table 36 48
Changes to Table 37 52

10/2014—Revision 0: Initial Version

SPECIFICATIONS

The AD9528 is configured for dual loop mode. The REFA differential input is enabled at 122.88 MHz, f_{VCXO} = 122.88 MHz and single-ended, f_{VCO} = 3686.4 MHz, VCO divider = 3. Doubler and analog delay are off, SYSREF generation is on, unless otherwise noted. Typical is given for VDDx = 3.3 V ± 5%, and T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over the full VDDx and T_A (−40°C to +85°C) variation, as listed in Table 1.

CONDITIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
VDDx[1]	3.135	3.3	3.465	V	3.3 V ± 5%
TEMPERATURE					
Ambient Temperature Range, T_A	−40	+25	+85	°C	
Junction Temperature, T_J			+115	°C	Refer to the Power Dissipation and Thermal Considerations section to calculate the junction temperature

[1] VDDx includes the VDD pins (Pin 1, Pin 10, Pin 16, Pin 20, and Pin 72) and the VDD13 pin through the VDD0 pin, unless otherwise noted. See the Pin Configuration and Function Descriptions for details.

SUPPLY CURRENT

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT					Excludes clock distribution section; clock distribution outputs running as follows: 7 HSTL device clocks at 122.88 MHz, 7 LVDS SYSREF clocks (3.5 mA) at 960 kHz
Dual Loop Mode					PLL1 and PLL2 enabled
VDD (Pin 1, Pin 72)		19	21	mA	
VDD (Pin 10)		29	32	mA	
VDD (Pin 16)		34	37	mA	
VDD (Pin 20)		64	71	mA	
Single Loop Mode					PLL1 off and REFA and REFB inputs off
VDD (Pin 1, Pin 72)		7	9	mA	122.88 MHz reference source applied to the VCXO inputs (input to PLL2)
VDD (Pin 10)		29	32	mA	
VDD (Pin 16)		34	37	mA	
VDD (Pin 20)		64	71	mA	
Buffer Mode					PLL1 and PLL2 off, REFA and REFB inputs disabled; 122.88 MHz reference source applied to VCXO differential inputs to drive 7 of 14 outputs, internal SYSREF generator off, 960 kHz input source applied to SYSREF differential inputs to drive the other 7 outputs, dividers in clock distribution path bypassed in clock distribution channel
VDD (Pin 1, Pin 72)		17	19	mA	
VDD (Pin 10)		23	25	mA	
VDD (Pin 16)		2	3	mA	
VDD (Pin 20)		15	19	mA	
Chip Power-Down Mode					
VDD (Pin 1, Pin 10, Pin 16, Pin 20, and Pin 72)		15		mA	Chip power-down bit enabled (Register 0x0500, Bit 0 = 1)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT FOR EACH CLOCK DISTRIBUTION CHANNEL					Each clock output channel has a dedicated VDD pin. The current draw for each VDD pin includes the divider, fine delay, and output driver, fine delay is off; see the Pin Configuration and Function Descriptions section for pin assignment
LVDS Mode, 3.5 mA					
		21	23	mA	Output = 122.88 MHz, channel divider = 10
		24	26	mA	Output = 409.6 MHz, channel divider = 3
		28	30	mA	Output = 737.28 MHz, channel divider = 1, VCO divider = 5, LVDS boost mode of 4.5 mA recommended
LVDS Boost Mode, 4.5 mA					
		22	24	mA	Output = 122.88 MHz, channel divider =10
		25	27	mA	Output = 409.6 MHz, channel divider = 3
		29	31	mA	Output = 737.28 MHz, channel divider = 1, VCO divider = 5
HSTL Mode, 9 mA					
		25	27	mA	Output = 122.88 MHz, channel divider =10
		26	28	mA	Output = 409.6 MHz, channel divider = 3
		29	31	mA	Output = 983.04 MHz, channel divider = 1, VCO divider = 5, VCO = 3932.16 MHz
		37	41	mA	Output = 1228.8 MHz, channel divider = 1, only output channels OUT1 and OUT2 support output frequencies greater than ~1 GHz
Chip Power-Down Mode		2.5	4	mA	For each channel VDD pin, chip power-down bit enabled (Register 0x0500, Bit 0 = 1)

POWER DISSIPATION

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TOTAL POWER DISSIPATION					Does not include power dissipated in termination resistors
Typical Dual Loop Mode Configuration		1675	1780	mW	Differential REFA input at 122.88 MHz; f_{VCXO} = 122.88 MHz, f_{VCO} = 3686.4 MHz, VCO divider at 3 clock distribution outputs running as follows: 7 HSTL at 122.88 MHz, 7 LVDS (3.5 mA) at 960 kHz
Typical Single Loop Mode Configuration		1635	1810	mW	PLL1 off, differential VCXO input at 122.88 MHz, clock distribution outputs running as follows: 7 HSTL at 122.88 MHz, 7 LVDS (3.5 mA) at 960 kHz
Typical Buffer Mode		1030	1200	mW	PLL1 and PLL2 off, differential VCXO input at 122.88 MHz. SYSREF generator off, differential SYSREF input at 960 kHz; clock distribution outputs running as follows: 7 HSTL at 122.88 MHz, 7 LVDS (3.5 mA) at 960 kHz
Chip Power-Down Mode		65		mW	Chip power-down bit enabled (Register 0x0500, Bit 0 = 1)
$\overline{\text{RESET}}$ Enabled		1015	1200	mW	$\overline{\text{RESET}}$ pin low
INCREMENTAL POWER DISSIPATION					Does not include power dissipated in termination resistors
Low Power Base Configuration		590		mW	Dual loop mode, SYSREF generation and fine delay off; total power with 1 LVDS output running at 122.88 MHz, single-ended REFA at 122.88 MHz; REFB off, VCXO = 122.88 MHz, VCO = 3686.4 MHz
PLL1 OFF		0		mW	Define settings to power off PLL1
Output Distribution					Incremental power increase for each additional enable output
LVDS Mode, 3.5 mA		70		mW	Single 3.5 mA LVDS output at 122.88 MHz, channel divider = 10
		78		mW	Single 3.5 mA LVDS output at 409.6 MHz, channel divider = 3
		92		mW	Single 3.5 mA LVDS output at 737.28 MHz, VCO divider = 5, channel divider = 1
LVDS Mode, 4.5 mA		73		mW	Single 4.5 mA LVDS output at 122.88 MHz, channel divider = 10
		81		mW	Single 4.5 mA LVDS output at 409.6 MHz, channel divider = 3
		95		mW	Single 4.5 mA LVDS output at 737.28 MHz, VCO divider = 5

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL Mode, 9 mA		80		mW	Single 9 mA HSTL output at 122.88 MHz, channel divider = 10
		85		mW	Single 9 mA HSTL output at 409.6 MHz, channel divider = 3
		95		mW	Single 9 mA HSTL output at 983.04 MHz, VCO divider = 5, channel divider = 1
		125		mW	Single 9 mA HSTL output at 1228.8 MHz, channel divider = 1
REFA					
Differential On		72		mW	REFA and REFB running at 122.88 MHz, REF_SEL = REFB
Single-Ended		72		mW	REFA and REFB running at 122.88 MHz, REF_SEL = REFB
SYSREF Generator Enabled		5		mW	Single 3.5 mA LVDS output at 960 kHz
Fine Delay On		1		mW	Maximum delay setting

INPUT CHARACTERISTICS—REFA, $\overline{\text{REFA}}$, REFB, $\overline{\text{REFB}}$, VCXO_IN, $\overline{\text{VCXO\_IN}}$, SYSREF_IN, AND $\overline{\text{SYSREF\_IN}}$

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL MODE					
Input Frequency Range			400	MHz	
Input Frequency Range (VCXO_IN)			1250	MHz	For buffer mode
Input Slew Rate (VCXO_IN)	500			V/µs	Minimum limit imposed for jitter performance
Common-Mode Internally Generated Input Voltage	0.6	0.7	0.8	V	
Input Common-Mode Range	0.4		1.4	V	DC-coupled LVDS mode and HSTL mode supported
Differential Input Voltage, Sensitivity Frequency < 250 MHz	200			mV p-p	Can accommodate single-ended inputs via ac grounding of unused inputs; instantaneous voltage on either pin must not exceed 1.8 V dc
Differential Input Voltage, Sensitivity Frequency > 250 MHz	250			mV p-p	Can accommodate single-ended inputs via ac grounding of unused inputs; instantaneous voltage on either pin must not exceed 1.8 V dc
Input Noise Sensitivity		5		mV	
Differential Input Resistance		4.8		kΩ	
Differential Input Capacitance		4		pF	
Duty Cycle					Duty cycle limits are set by pulse width high and pulse width low
Pulse Width Low	1			ns	
Pulse Width High	1			ns	
CMOS MODE, SINGLE-ENDED INPUT					
Input Frequency Range			250	MHz	
Input High Voltage	1.4			V	
Input Low Voltage			0.65	V	
Input Capacitance		2		pF	
Duty Cycle					Duty cycle limits are set by pulse width high and pulse width low
Pulse Width Low	1.6			ns	
Pulse Width High	1.6			ns	

PLL1 CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PFD FREQUENCY			110	MHz	
Charge Pump Current LSB Size		0.5		µA	7-bit resolution
Reference Frequency Detector Threshold	950			kHz	Do not use automatic holdover if the reference frequency is less than the minimum value

VCXO_VT OUTPUT CHARACTERISTICS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE					
High	VDD – 0.15			V	R_{LOAD} > 20 kΩ
Low			150	mV	

PLL2 CHARACTERISTICS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCO (ON CHIP)					
Frequency Range	3450		4025	MHz	
Gain		48		MHz/V	
PLL2 FIGURE OF MERIT (FOM)		–226		dBc/Hz	
MAXIMUM PFD FREQUENCY			275	MHz	

CLOCK DISTRIBUTION OUTPUT CHARACTERISTICS

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL MODE					
Output Frequency			1000	MHz	All outputs
			1250	MHz	OUT0 to OUT3, OUT12, OUT13 outputs only
Rise Time/Fall Time (20% to 80%)		60	160	ps	100 Ω termination across output pair
Duty Cycle					
f < 500 MHz	48	50	53	%	
f = 500 MHz to 800 MHz	46	51	54	%	
f = 800 MHz to 1.25 GHz	44	50	62	%	
f = 800 MHz to 1.25 GHz	50		57	%	If using PLL2
Differential Output Voltage Swing	900	1000	1100	mV	$V_{OH} – V_{OL}$ for each leg of a differential pair for default amplitude setting with the driver not toggling; the peak-to-peak amplitude measured using a differential probe across the differential pair with the driver toggling is roughly 2× these values (see Figure 5 for variation over frequency)
Common-Mode Output Voltage	0.88	0.9	0.94	V	
LVDS MODE, 3.5 mA					3.5 mA
Output Frequency			1000	MHz	All outputs
			1250	GHz	OUT0 to OUT3, OUT12, OUT13 outputs only
Rise Time/Fall Time (20% to 80%)		50	216	ps	100 Ω termination across output pair
Duty Cycle					
f < 500 MHz	47	50	53	%	
f = 500 MHz to 800 MHz	46	51	54	%	
f = 800 MHz to 1.25 GHz	48	54	58	%	
Balanced, Differential Output Swing (VOD)	345		390	mV	Voltage swing between output pins; output driver static (see Figure 6 for variation over frequency)
Unbalanced, ΔVOD			3	mV	Absolute difference between voltage swing of normal pin and inverted pin; output driver static
Common-Mode Output Voltage	1.15		1.35	V	
Common-Mode Difference			1.2	mV	Voltage difference between output pins; output driver static
Short-Circuit Output Current		15	19	mA	Output driver static

OUTPUT TIMING ALIGNMENT CHARACTERISTICS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT TIMING SKEW					Delay off on all outputs, maximum deviation between rising edges of outputs; all outputs are on and in HSTL mode, unless otherwise noted
PLL1 Outputs					
PLL1 to PLL1		17	100	ps	PLL1 clock to PLL1 clock
PLL1 to SYSREF		17	100	ps	SYSREF retimed by PLL1 clock
PLL1 to SYSREF		361	510	ps	SYSREF not retimed by any clock
PLL1 to SYSREF		253	1150	ps	SYSREF retimed by PLL2 clock
PLL1 to PLL2		257	1000	ps	PLL1 clock to PLL2 clock
PLL2 Outputs					
PLL2 to PLL2		20	165	ps	PLL2 clock to PLL2 clock
PLL2 to SYSREF		20	165	ps	SYSREF retimed by PLL2 clock
PLL2 to SYSREF		620	750	ps	SYSREF not retimed by any clock
PLL2 to SYSREF		253	1150	ps	SYSREF retimed by PLL1 clock
PLL2 to PLL1		257	1000	ps	PLL2 clock to PLL1 clock
OUTPUT DELAY ADJUST					Enables digital and analog delay capability
Coarse Adjustable Delay		32		Steps	Resolution step is the period of VCO RF divider (M1) output/2
Fine Adjustable Delay		15		Steps	Resolution step
Resolution Step		31		ps	
Insertion Delay		425		ps	Analog delay enabled and delay setting equal to zero

SYSREF_IN, $\overline{\text{SYSREF\_IN}}$, VCXO_IN, AND $\overline{\text{VCXO\_IN}}$ TIMING CHARACTERISTICS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PROPAGATION LATENCY OF VCXO PATH	1.92	2.3	2.7	ns	VCXO input to device clock output, not retimed
PROPAGATION LATENCY OF SYSREF PATH	1.83	2.2	2.6	ns	SYSREF input to SYSREF output, not retimed
RETIMED WITH DEVICE CLOCK					
Setup Time of External SYSREF Relative to Device Clock Output	−1.13			ns	Given a SYSREF input clock rate equal to 122.88 MHz
Hold Time of External SYSREF Relative to Device Clock Output	0.7			ns	
RETIMED WITH VCXO					
Setup Time of External SYSREF Relative to VCXO Input	−0.21			ns	
Hold Time of External SYSREF Relative to VCXO	0.09			ns	

CLOCK OUTPUT ABSOLUTE PHASE NOISE—DUAL LOOP MODE

Application examples are based on a typical setups (see Table 2) using an external 122.88 MHz VCXO (Crystek CVHD-950); reference = 122.88 MHz; channel divider = 10 or 1; PLL2 loop bandwidth (LBW) = 450 kHz.

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL OUTPUT					
f_{OUT} = 122.88 MHz					
10 Hz Offset		−87		dBc/Hz	
100 Hz Offset		−106		dBc/Hz	
1 kHz Offset		−126		dBc/Hz	
10 kHz Offset		−135		dBc/Hz	
100 kHz Offset		−139		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
800 kHz Offset		−147		dBc/Hz	
1 MHz Offset		−149		dBc/Hz	
10 MHz Offset		−161		dBc/Hz	
40 MHz Offset		−162		dBc/Hz	
f_{OUT} = 1228.8 MHz					OUT1 and OUT2 only, channel divider = 1
10 Hz Offset		−62		dBc/Hz	
100 Hz Offset		−85		dBc/Hz	
1 kHz Offset		−106		dBc/Hz	
10 kHz Offset		−115		dBc/Hz	
100 kHz Offset		−119		dBc/Hz	
800 kHz Offset		−127		dBc/Hz	
1 MHz Offset		−129		dBc/Hz	
10 MHz Offset		−147		dBc/Hz	
100 MHz Offset		−153		dBc/Hz	
LVDS OUTPUT					
f_{OUT} = 122.88 MHz					
10 Hz Offset		−86		dBc/Hz	
100 Hz Offset		−106		dBc/Hz	
1 kHz Offset		−126		dBc/Hz	
10 kHz Offset		−135		dBc/Hz	
100 kHz Offset		−139		dBc/Hz	
800 kHz Offset		−147		dBc/Hz	
1 MHz Offset		−148		dBc/Hz	
10 MHz Offset		−157		dBc/Hz	
40 MHz Offset		−158		dBc/Hz	
f_{OUT} = 1228.8 MHz					OUT1 and OUT2 only, channel divider = 1
10 Hz Offset		−66		dBc/Hz	
100 Hz Offset		−86		dBc/Hz	
1 kHz Offset		−106		dBc/Hz	
10 kHz Offset		−115		dBc/Hz	
100 kHz Offset		−119		dBc/Hz	
800 kHz Offset		−127		dBc/Hz	
1 MHz Offset		−129		dBc/Hz	
10 MHz Offset		−147		dBc/Hz	
100 MHz Offset		−152		dBc/Hz	

CLOCK OUTPUT ABSOLUTE PHASE NOISE—SINGLE LOOP MODE

Single loop mode is based on the typical setup (see Table 2) using an external 122.88 MHz reference (SMA100A generator); reference = 122.88 MHz; channel divider = 10; PLL2 LBW = 450 kHz.

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL OUTPUT					
f_{OUT} = 122.88 MHz					
10 Hz Offset		−104		dBc/Hz	
100 Hz Offset		−113		dBc/Hz	
1 kHz Offset		−123		dBc/Hz	
10 kHz Offset		−135		dBc/Hz	
100 kHz Offset		−140		dBc/Hz	
800 kHz Offset		−147		dBc/Hz	
1 MHz Offset		−149		dBc/Hz	
10 MHz Offset		−161		dBc/Hz	
40 MHz Offset		−162		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
f_{OUT} = 1228.8 MHz					OUT1 and OUT2 only, channel divider = 1
10 Hz Offset		−85		dBc/Hz	
100 Hz Offset		−95		dBc/Hz	
1 kHz Offset		−103		dBc/Hz	
10 kHz Offset		−114		dBc/Hz	
100 kHz Offset		−120		dBc/Hz	
800 kHz Offset		−126		dBc/Hz	
1 MHz Offset		−128		dBc/Hz	
10 MHz Offset		−147		dBc/Hz	
100 MHz Offset		−153		dBc/Hz	
LVDS OUTPUT					
f_{OUT} = 122.88 MHz					
10 Hz Offset		−111		dBc/Hz	
100 Hz Offset		−113		dBc/Hz	
1 kHz Offset		−123		dBc/Hz	
10 kHz Offset		−135		dBc/Hz	
100 kHz Offset		−140		dBc/Hz	
800 kHz Offset		−147		dBc/Hz	
1 MHz Offset		−148		dBc/Hz	
10 MHz Offset		−157		dBc/Hz	
40 MHz Offset		−157		dBc/Hz	
f_{OUT} = 1228.8 MHz					OUT1 and OUT2 only, channel divider = 1
10 Hz Offset		−85		dBc/Hz	
100 Hz Offset		−95		dBc/Hz	
1 kHz Offset		−103		dBc/Hz	
10 kHz Offset		−114		dBc/Hz	
100 kHz Offset		−120		dBc/Hz	
800 kHz Offset		−126		dBc/Hz	
1 MHz Offset		−128		dBc/Hz	
10 MHz Offset		−146		dBc/Hz	
100 MHz Offset		−152		dBc/Hz	

CLOCK OUTPUT ABSOLUTE TIME JITTER

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT ABSOLUTE RMS TIME JITTER					Application examples are based on typical setups (see Table 2) using an external 122.88 MHz VCXO (Crystek CVHD-950); reference = 122.88 MHz; channel divider = 10 or 1; PLL2 LBW = 450 kHz
Dual Loop Mode					
HSTL Output		117		fs	Integrated BW = 200 kHz to 5 MHz
f_{OUT} = 122.88 MHz		123		fs	Integrated BW = 200 kHz to 10 MHz
		159		fs	Integrated BW = 12 kHz to 20 MHz
		172		fs	Integrated BW = 10 kHz to 40 MHz
		177		fs	Integrated BW = 1 kHz to 40 MHz
		109		fs	Integrated BW = 1 MHz to 40 MHz
f_{OUT} = 1228.8 MHz, Channel Divider = 1		114		fs	Integrated BW = 200 kHz to 5 MHz
		116		fs	Integrated BW = 200 kHz to 10 MHz
		147		fs	Integrated BW = 12 kHz to 20 MHz
		154		fs	Integrated BW = 10 kHz to 100 MHz
		160		fs	Integrated BW = 1 kHz to 100 MHz
		74		fs	Integrated BW = 1 MHz to 100 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVDS Output		124		fs	Integrated BW = 200 kHz to 5 MHz
f_{OUT} = 122.88 MHz		136		fs	Integrated BW = 200 kHz to 10 MHz
		179		fs	Integrated BW = 12 kHz to 20 MHz
		209		fs	Integrated BW = 10 kHz to 40 MHz
		213		fs	Integrated BW = 1 kHz to 40 MHz
		160		fs	Integrated BW = 1 MHz to 40 MHz
f_{OUT} = 1228.8 MHz, Channel Divider = 1		116		fs	Integrated BW = 200 kHz to 5 MHz
		118		fs	Integrated BW = 200 kHz to 10 MHz
		150		fs	Integrated BW = 12 kHz to 20 MHz
		157		fs	Integrated BW = 10 kHz to 100 MHz
		163		fs	Integrated BW = 1 kHz to 100 MHz
		76		fs	Integrated BW = 1 MHz to 100 MHz
Single Loop Mode					
HSTL Output		115		fs	Integrated BW = 200 kHz to 5 MHz
f_{OUT} = 122.88 MHz		122		fs	Integrated BW = 200 kHz to 10 MHz
		156		fs	Integrated BW = 12 kHz to 20 MHz
		171		fs	Integrated BW = 10 kHz to 40 MHz
		179		fs	Integrated BW = 1 kHz to 40 MHz
		110		fs	Integrated BW = 1 MHz to 40 MHz
f_{OUT} = 1228.8 MHz, Channel Divider = 1		116		fs	Integrated BW = 200 kHz to 5 MHz
		118		fs	Integrated BW = 200 kHz to 10 MHz
		146		fs	Integrated BW = 12 kHz to 20 MHz
		153		fs	Integrated BW = 10 kHz to 100 MHz
		163		fs	Integrated BW = 1 kHz to 100 MHz
		81		fs	Integrated BW = 1 MHz to 100 MHz
LVDS Output		123		fs	Integrated BW = 200 kHz to 5 MHz
f_{OUT} = 122.88 MHz		135		fs	Integrated BW = 200 kHz to 10 MHz
		177		fs	Integrated BW = 12 kHz to 20 MHz
		207		fs	Integrated BW = 10 kHz to 40 MHz
		214		fs	Integrated BW = 1 kHz to 40 MHz
		160		fs	Integrated BW = 1 MHz to 40 MHz
f_{OUT} = 1228.8 MHz, Channel Divider = 1		117		fs	Integrated BW = 200 kHz to 5 MHz
		119		fs	Integrated BW = 200 kHz to 10 MHz
		147		fs	Integrated BW = 12 kHz to 20 MHz
		155		fs	Integrated BW = 10 kHz to 100 MHz
		164		fs	Integrated BW = 1 kHz to 100 MHz
		83		fs	Integrated BW = 1 MHz to 100 MHz

CLOCK OUTPUT ADDITIVE TIME JITTER (BUFFER MODE)

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT ADDITIVE RMS TIME JITTER					Application examples are based on typical performance (see Table 2) using an external 122.88 MHz source driving VCXO inputs (distribution section only, does not include PLL and VCO)
Buffer Mode					
HSTL Output		66		fs	Integrated BW = 200 kHz to 5 MHz
f_{OUT} = 122.88 MHz		81		fs	Integrated BW = 200 kHz to 10 MHz
		112		fs	Integrated BW = 12 kHz to 20 MHz
		145		fs	Integrated BW = 10 kHz to 40 MHz
		146		fs	Integrated BW = 1 kHz to 40 MHz
		132		fs	Integrated BW = 1 MHz to 40 MHz
LVDS Output		79		fs	Integrated BW = 200 kHz to 5 MHz
f_{OUT} = 122.88 MHz		101		fs	Integrated BW = 200 kHz to 10 MHz
		140		fs	Integrated BW = 12 kHz to 20 MHz
		187		fs	Integrated BW = 10 kHz to 40 MHz
		189		fs	Integrated BW = 1 kHz to 40 MHz
		176		fs	Integrated BW = 1 MHz to 40 MHz

LOGIC INPUT PINS—$\overline{\text{RESET}}$, REF_SEL, AND SYSREF_REQ

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE					
Input High	1.3			V	
Input Low			0.6	V	
INPUT LOW CURRENT		13	14	µA	
CAPACITANCE		4		pF	
$\overline{\text{RESET}}$ TIMING					
Pulse Width Low	1.0			ns	
Inactive to Start of Register Programming	2.5			ns	

STATUS OUTPUT PINS—STATUS0 AND STATUS1

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE					
High	3			V	
Low			0.02	V	

SERIAL CONTROL PORT—SERIAL PORT INTERFACE (SPI) MODE

Table 17.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$ (INPUT)						$\overline{CS}$ has an internal 35 kΩ pull-up resistor
Voltage						
Input Logic 1			1.37		V	
Input Logic 0			1.33		V	
Current						
Input Logic 1			−52		µA	
Input Logic 0			−82		µA	
Input Capacitance			2		pF	
SCLK (INPUT) IN SPI MODE						SCLK has an internal 40 kΩ pull-down resistor in SPI mode but not in I^2C mode
Voltage						
Input Logic 1			1.76		V	
Input Logic 0			1.22		V	
Current						
Input Logic 1			0.0037		µA	
Input Logic 0			0.0012		µA	
Input Capacitance			2		pF	
SDIO						Input is in bidirectional mode
Voltage						
Input Logic 1			1.76		V	
Input Logic 0			1.22		V	
Current						
Input Logic 1			0.0037		µA	
Input Logic 0			0.0012		µA	
Input Capacitance			3.5		pF	
SDIO, SDO (OUTPUTS)						
Voltage						
Output Logic 1		3.11			V	
Output Logic 0				0.0018	V	
TIMING						
Clock Rate (SCLK, $1/t_{SCLK}$)				50	MHz	
Pulse Width High	t_{HIGH}	4			ns	
Pulse Width Low	t_{LOW}	2			ns	
SDIO to SCLK Setup	t_{DS}	2.2			ns	
SCLK to SDIO Hold	t_{DH}	−0.9			ns	
SCLK to Valid SDIO and SDO	t_{DV}			6	ns	
$\overline{CS}$ to SCLK Setup	t_S	1.25			ns	
$\overline{CS}$ to SCLK Hold	t_C	0			ns	
$\overline{CS}$ Minimum Pulse Width High	t_{PWH}	0.9			ns	

SERIAL CONTROL PORT—I²C MODE

Table 18.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL VOLTAGE						When inputting data
Input Logic 1		0.7 × VDD			V	
Input Logic 0				0.3 × VDD	V	
Input Current		−10		+10	µA	Input voltage between 0.1 × VDD and 0.9 × VDD
Hysteresis of Schmitt Trigger Inputs		0.015 × VDD			V	
SDA						When outputting data
Output Logic 0 Voltage at 3 mA Sink Current				0.2	V	
Output Fall Time from VIH_{MIN} to VIL_{MAX}		20 + 0.1 C_B[1]		250	ns	Bus capacitance from 10 pF to 400 pF
TIMING						All I²C timing values are referred to VIH_{MIN} (0.3 × VDD) and VIL_{MAX} levels (0.7 × VDD)
Clock Rate (SCL, f_{I2C})				400	kHz	
Bus Free Time Between a Stop and Start Condition	t_{IDLE}	1.3			µs	
Setup Time for a Repeated Start Condition	$t_{SET;\ STR}$	0.6			µs	
Hold Time (Repeated) Start Condition	$t_{HLD;\ STR}$	0.6			µs	After this period, the first clock pulse is generated
Setup Time for a Stop Condition	$t_{SET;\ STP}$	0.6			µs	
Low Period of the SCL Clock	t_{LOW}	1.3			µs	
High Period of the SCL Clock	t_{HIGH}	0.6			µs	
SCL, SDA Rise Time	t_{RISE}	20 + 0.1 C_B[1]		300	ns	
SCL, SDA Fall Time	t_{FALL}	20 + 0.1 C_B[1]		300	ns	
Data Setup Time	$t_{SET;\ DAT}$	100			ns	
Data Hold Time	$t_{HLD;\ DAT}$	0			ns	
Capacitive Load for Each Bus Line	C_B[1]			400	pF	

[1] C_B is the capacitance of one bus line in picofarads (pF).

ABSOLUTE MAXIMUM RATINGS

Table 19.

Parameter	Rating
VDD	−0.3 V to +3.6 V
REFA, $\overline{\text{REFA}}$, REFB, $\overline{\text{REFB}}$, VCXO_IN, $\overline{\text{VCXO\_IN}}$, SYSREF_IN, $\overline{\text{SYSREF\_IN}}$, SYSREF_REQ to GND	−0.3 V to +3.6 V
SCLK/SCL, SDIO/SDA, SDO, $\overline{\text{CS}}$ to GND	−0.3 V to +3.6 V
$\overline{\text{RESET}}$, REF_SEL, SYSREF_REQ to GND	−0.3 V to +3.6 V
STATUS0/SP0, STATUS1/SP1 to GND	−0.3 V to +3.6 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Table 20. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1, 2]	θ_{JC}[1, 3]	θ_{JB}[1, 4]	Ψ_{JT}[1, 2]	Unit
72-Lead LFCSP, 10 mm × 10 mm	0	21.3	1.7	12.6	0.1	°C/W
	1.0	20.1			0.2	°C/W
	2.5	18.1			0.3	°C/W

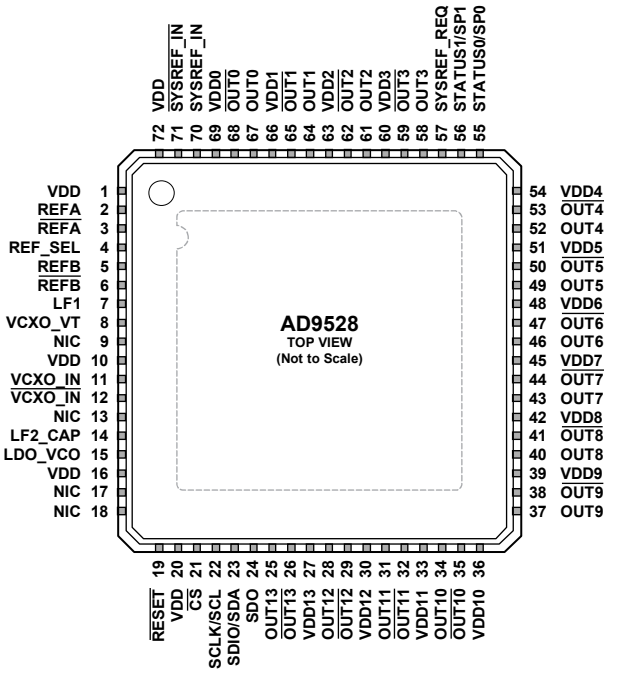
[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Additional power dissipation information can be found in the Power Dissipation and Thermal Considerations section.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED. THIS PIN CAN BE LEFT FLOATING.
2. THE EXPOSED PAD IS THE GROUND CONNECTION ON THE CHIP. IT MUST BE SOLDERED TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY AND HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

Figure 2. Pin Configuration

Table 21. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	VDD	P	3.3 V Supply for the PLL1 Input Section.
2	REFA	I	Reference Clock Input A. Along with $\overline{\text{REFA}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
3	$\overline{\text{REFA}}$	I	Complementary Reference Clock Input A. Along with REFA, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
4	REF_SEL	I	Reference Input Select. The reference input selection function defaults to software control via internal Register 0x010A, Bits[2:0]. When the REF_SEL pin is active, a logic low selects REFA and logic high selects REFB.
5	REFB	I	Reference Clock Input B. Along with $\overline{\text{REFB}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
6	$\overline{\text{REFB}}$	I	Complementary Reference Clock Input B. Along with REFB, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
7	LF1	O	PLL1 External Loop Filter.
8	VCXO_VT	O	VCXO Control Voltage. Connect this pin to the voltage control pin of the external VCXO.
9	NIC	NIC	Not Internally Connected. The pin can be left floating.
10	VDD	P	3.3 V Supply for the PLL2 Section.
11	VCXO_IN	I	PLL1 Oscillator Input. Along with $\overline{\text{VCXO\_IN}}$, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
12	$\overline{\text{VCXO\_IN}}$	I	Complementary PLL1 Oscillator Input. Along with VCXO_IN, this pin is the differential input for the PLL reference. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
13	NIC	NIC	Not Internally Connected. The pin can be left floating.
14	LF2_CAP	O	PLL2 External Loop Filter Capacitor Connection. Connect capacitor between this pin and the LDO_VCO pin.

Pin No.	Mnemonic	Type[1]	Description
15	LDO_VCO	P/O	2.5 V LDO Internal Regulator Decoupling for the VCO. Connect a 0.47 µF decoupling capacitor from this pin to ground. Note that, for best performance, the LDO bypass capacitor must be placed in close proximity to the device.
16	VDD	P	3.3 V Supply for the PLL2 Internal Regulator.
17	NIC	NIC	Not Internally Connected. The pin can be left floating.
18	NIC	NIC	Not Internally Connected. The pin can be left floating.
19	$\overline{\text{RESET}}$	I	Digital Input, Active Low. Resets internal logic to default states.
20	VDD	P	3.3 V Supply for the PLL2 Internal Regulator.
21	$\overline{\text{CS}}$		Serial Control Port Chip Select, Active Low. This pin has an internal 35 kΩ pull-up resistor.
22	SCLK/SCL	I	Serial Control Port Clock Signal for SPI Mode (SCLK) or I²C Mode (SCL). Data clock for serial programming.
23	SDIO/SDA	I/O	Serial Control Port Bidirectional Serial Data In/Data Out for SPI Mode (SDIO) or I²C Mode (SDA).
24	SDO	O	Serial Data Output. Use this pin to read data in 4-wire mode (high impedance in 3-wire mode). There is no internal pull-up or pull-down resistor on this pin.
25	OUT13	O	Square Wave Clocking Output 13.
26	$\overline{\text{OUT13}}$	O	Complementary Square Wave Clocking Output 13. High speed output up to 1.25 GHz.
27	VDD13	P	3.3 V Supply for the Output 13 Clock Driver. High speed output up to 1.25 GHz.
28	OUT12	O	Square Wave Clocking Output 12. High speed output up to 1.25 GHz.
29	$\overline{\text{OUT12}}$	O	Complementary Square Wave Clocking Output 12. High speed output up to 1.25 GHz.
30	VDD12	P	3.3 V Supply for the Output 12 Clock Divider.
31	OUT11	O	Square Wave Clocking Output 11.
32	$\overline{\text{OUT11}}$	O	Complementary Square Wave Clocking Output 11.
33	VDD11	P	3.3 V Supply for the Output 11 Clock Driver.
34	OUT10	O	Square Wave Clocking Output 10.
35	$\overline{\text{OUT10}}$	O	Complementary Square Wave Clocking Output 10.
36	VDD10	P	3.3 V Supply for the Output 10 Clock Divider.
37	OUT9	O	Square Wave Clocking Output 9.
38	$\overline{\text{OUT9}}$	O	Complementary Square Wave Clocking Output 9.
39	VDD9	P	3.3 V Supply for the Output 9 Clock Driver.
40	OUT8	O	Square Wave Clocking Output 8.
41	$\overline{\text{OUT8}}$	O	Complementary Square Wave Clocking Output 8.
42	VDD8	P	3.3 V Supply for the Output 8 Clock Divider.
43	OUT7	O	Square Wave Clocking Output 7.
44	$\overline{\text{OUT7}}$	O	Complementary Square Wave Clocking Output 7.
45	VDD7	P	3.3 V Supply for the Output 7 Clock Driver.
46	OUT6	O	Square Wave Clocking Output 6.
47	$\overline{\text{OUT6}}$	O	Complementary Square Wave Clocking Output 6.
48	VDD6	P	3.3 V Supply for the Output 6 Clock Divider.
49	OUT5	O	Square Wave Clocking Output 5.
50	$\overline{\text{OUT5}}$	O	Complementary Square Wave Clocking Output 5.
51	VDD5	P	3.3 V Supply for the Output 5 Clock Driver.
52	OUT4	O	Square Wave Clocking Output 4.
53	$\overline{\text{OUT4}}$	O	Complementary Square Wave Clocking Output 4.
54	VDD4	P	3.3 V Supply for the Output 4 Clock Divider.
55	STATUS0/SP0	I/O	Lock Detect and Other Status Signals/I²C Address. This pin has an internal 30 kΩ pull-down resistor.
56	STATUS1/SP1	I/O	Lock Detect and Other Status Signals/I²C Address. This pin has an internal 30 kΩ pull-down resistor.
57	SYSREF_REQ	I	SYSREF Request Input Logic Control.
58	OUT3	O	Square Wave Clocking Output 3.
59	$\overline{\text{OUT3}}$	O	Complementary Square Wave Clocking Output 3. High speed output up to 1.25 GHz.
60	VDD3	P	3.3 V Supply for the Output 3 Clock Driver. High speed output up to 1.25 GHz.
61	OUT2	O	Square Wave Clocking Output 2. High speed output up to 1.25 GHz.
62	$\overline{\text{OUT2}}$	O	Complementary Square Wave Clocking Output 2. High speed output up to 1.25 GHz.
63	VDD2	P	3.3 V Supply for the Output 2 Clock Divider.

Pin No.	Mnemonic	Type[1]	Description
64	OUT1	O	Square Wave Clocking Output 1. High speed output up to 1.25 GHz.
65	$\overline{\text{OUT1}}$	O	Complementary Square Wave Clocking Output 1. High speed output up to 1.25 GHz.
66	VDD1	P	3.3 V Supply for the Output 1 Clock Driver.
67	OUT0	O	Square Wave Clocking Output 0. High speed output up to 1.25 GHz.
68	$\overline{\text{OUT0}}$	O	Complementary Square Wave Clocking Output 0. High speed output up to 1.25 GHz.
69	VDD0	P	3.3 V Supply for the Output 0 Clock Divider.
70	SYSREF_IN	I	External SYSREF Input Clock. Along with $\overline{\text{SYSREF\_IN}}$, this pin is the differential input for an external SYSREF signal. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
71	$\overline{\text{SYSREF\_IN}}$	I	Complementary External SYSREF Input Clock. Along with SYSREF_IN, this pin is the differential input for an external SYSREF signal. Alternatively, this pin can be programmed as a single-ended 3.3 V CMOS input.
72	VDD	P	3.3 V Supply for the PLL1 Input Section.
EP	EP, GND	GND	Exposed Pad. The exposed pad is the ground connection on the chip. It must be soldered to the analog ground of the printed circuit board (PCB) to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.

[1] P means power, I means input, O means output, I/O means input/output, P/O means power/output, and GND means ground.

TYPICAL PERFORMANCE CHARACTERISTICS

f_{VCXO} = 122.88 MHz, REFA differential at 122.88 MHz, f_{VCO} = 3686.4 MHz, and doubler is off, unless otherwise noted. External PLL1 loop filter component values are as follows: R_{ZERO} = 10 kΩ, C_{ZERO} = 1 µF, C_{POLE} = 200 pF. External PLL2 external capacitor C_{ZERO} = 1 nF. PLL1 charge pump = 5 µA and PLL2 charge pump = 805 µA.

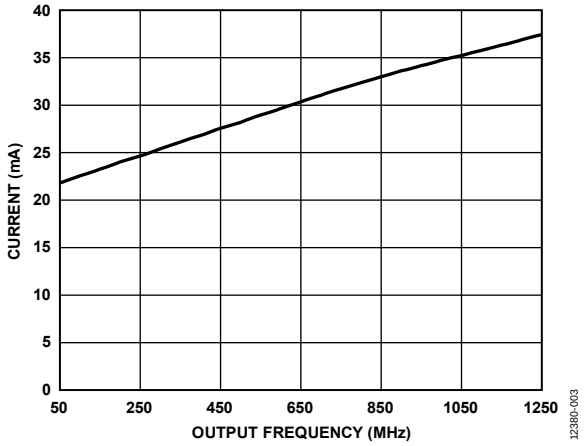


Figure 3. VDDx Current (Typical) vs. Output Frequency, HSTL Mode

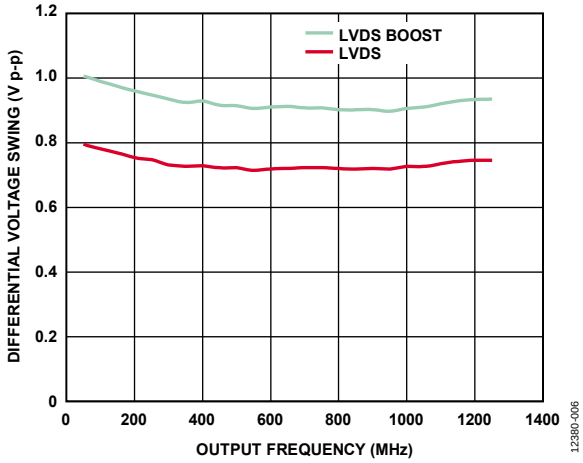


Figure 6. Differential Voltage Swing vs. Output Frequency, LVDS Mode and LVDS Boost Mode

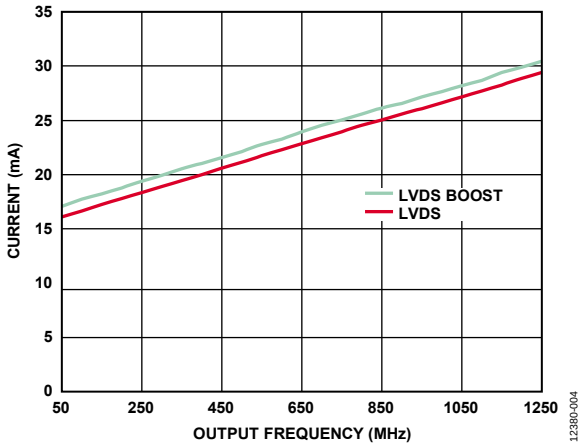


Figure 4. VDDx Current (Typical) vs. Output Frequency, LVDS Mode and LVDS Boost Mode

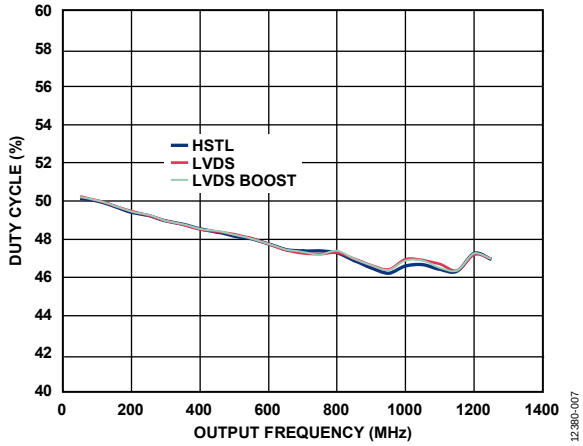


Figure 7. Positive Duty Cycle vs. Output Frequency, HSTL, LVDS, and LVDS Boost Modes

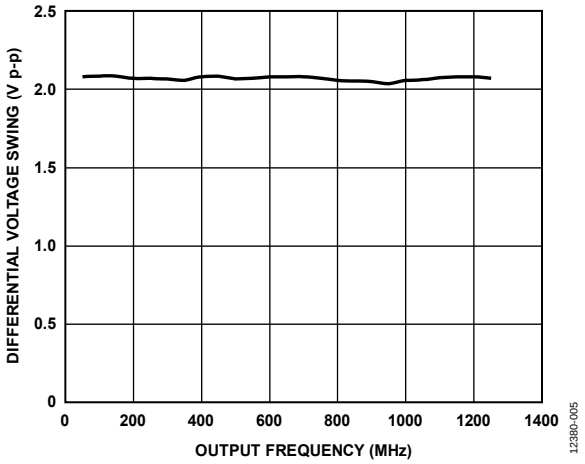


Figure 5. Differential Voltage Swing vs. Output Frequency, HSTL Mode

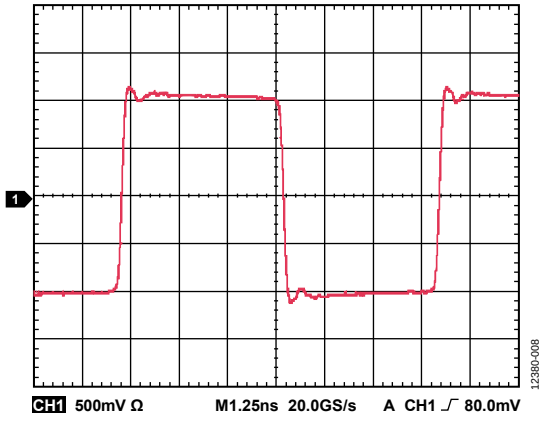


Figure 8. Output Waveform (Differential), HSTL at 122.88 MHz

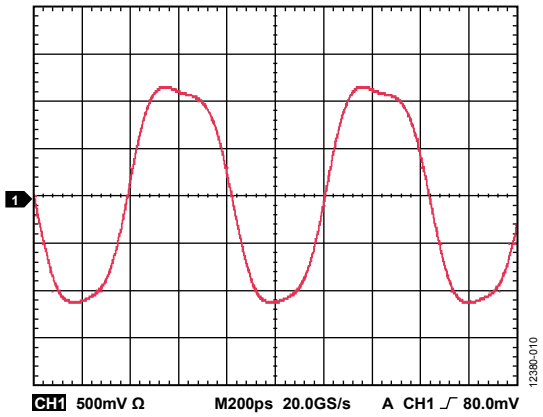


Figure 9. Output Waveform (Differential), HSTL at 1228.8 MHz

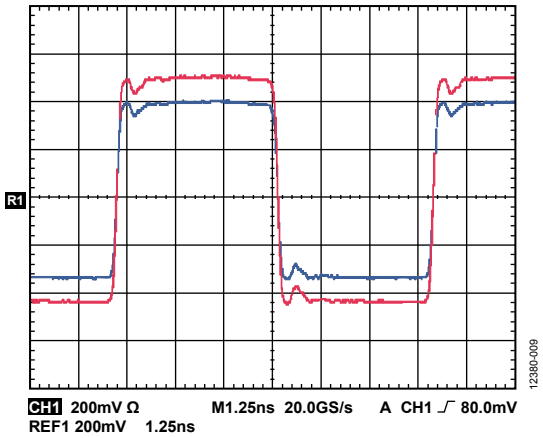


Figure 10. Output Waveform (Differential), LVDS and LVDS Boost Mode at 122.88 MHz

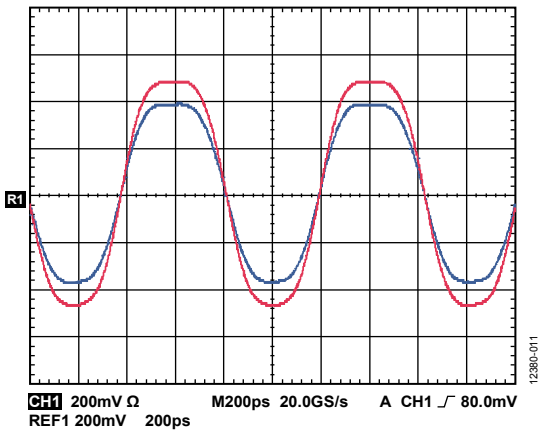


Figure 11. Output Waveform (Differential), LVDS and LVDS Boost Mode at 1228.8 MHz

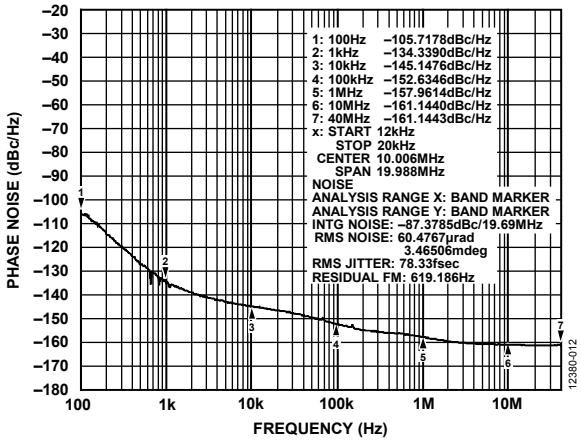


Figure 12. Phase Noise, Output = 122.88 MHz, HSTL Mode, PLL1 Output Sent Directly to Clock Distribution, PLL2 Off (VCXO = 122.88 MHz, Crystek VCXO CVHD-950)

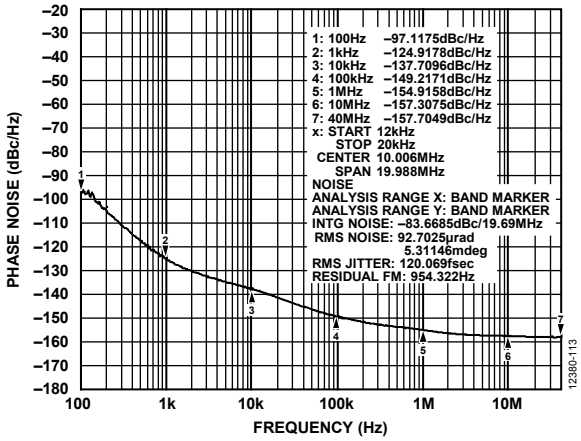


Figure 13. Phase Noise, Output = 122.88 MHz, HSTL Mode, PLL1 Output Sent Directly to Clock Distribution, PLL2 Off (VCXO = 122.88 MHz, TAITEN VCXO (A0145-0-011-3)

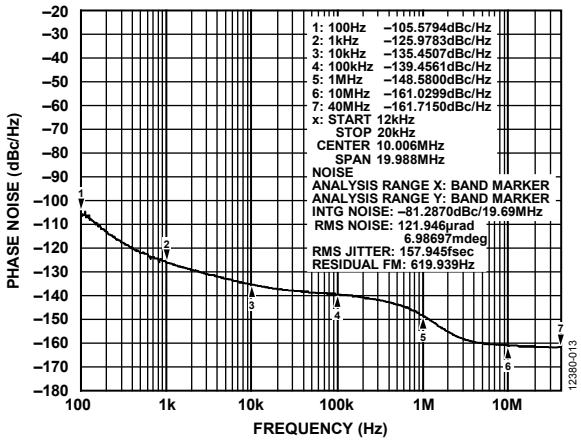


Figure 14. Phase Noise, Output = 122.88 MHz, HSTL Mode, Dual Loop Mode (VCXO = 122.88 MHz, Crystek VCXO CVHD-950, VCO = 3686.4 MHz)

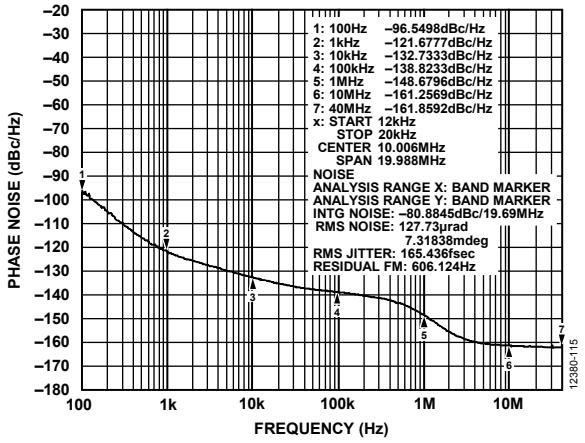


Figure 15. Phase Noise, Output = 122.88 MHz, HSTL Mode, Dual Loop Mode (VCXO = 122.88 MHz, TAITEN VCXO (A0145-0-011-3), VCO = 3686.4 MHz)

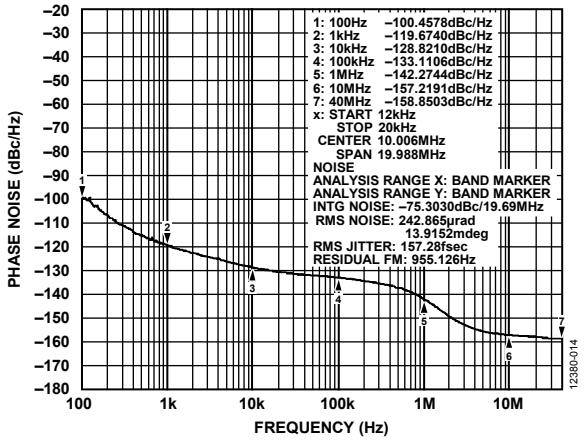


Figure 16. Phase Noise, Output = 245.76 MHz, HSTL Mode, Dual Loop Mode (VCXO = 122.88 MHz, Crystek VCXO CVHD-950, VCO = 3686.4 MHz)

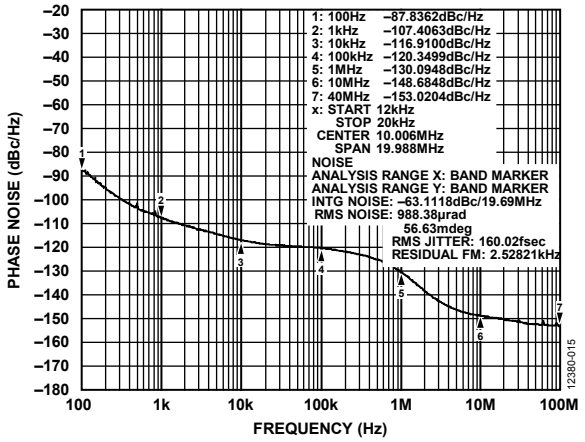


Figure 17. Phase Noise, Output = 983.04 MHz, HSTL Mode, Dual Loop Mode (VCXO = 122.88 MHz, Crystek VCXO CVHD-950, VCO = 3932.16 MHz)

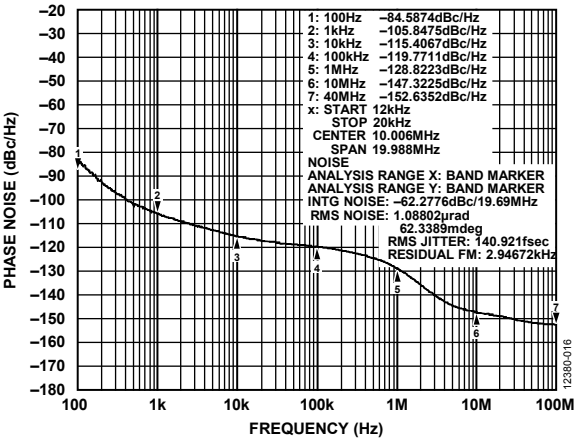


Figure 18. Phase Noise, Output = 1228.8 MHz, HSTL Mode, Dual Loop Mode (VCXO = 122.88 MHz, Crystek VCXO CVHD-950, VCO = 3686.4 MHz)

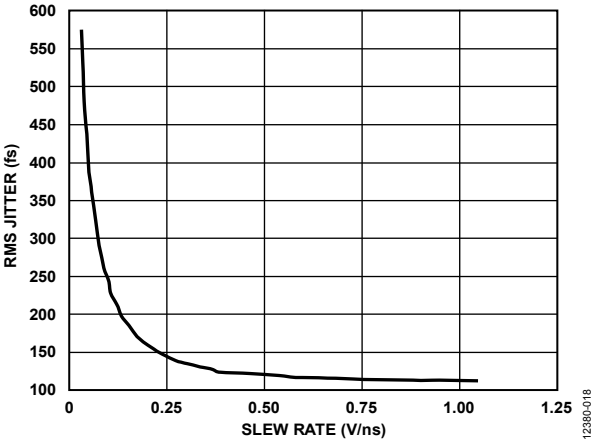


Figure 19. RMS Jitter in Buffer Mode with Both PLL1 and PLL2 Off vs. Slew Rate; Input Applied to the VCXO Input and Output Taken from Clock Distribution, Phase Noise Integration Range from 12 kHz to 20 MHz to Derive Jitter Number

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

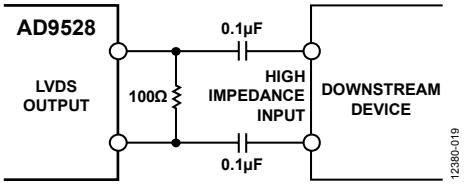


Figure 20. AC-Coupled LVDS Output Driver

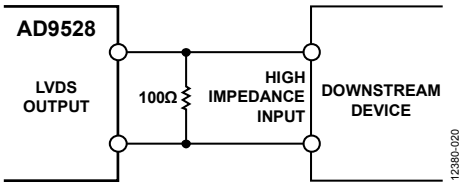


Figure 21. DC-Coupled LVDS Output Driver

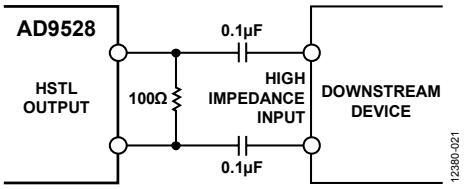


Figure 22. AC-Coupled HSTL Output Driver

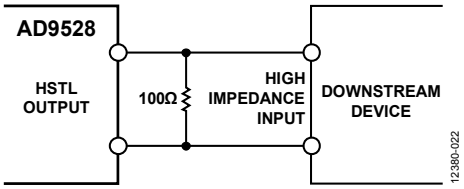


Figure 23. DC-Coupled HSTL Output Driver

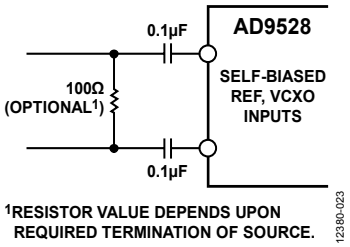


Figure 24. REFx, VCXO Input Differential Mode Receiver

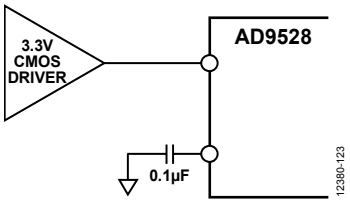


Figure 25. REFx, VCXO Input, Single-Ended Mode Receiver

TYPICAL APPLICATION CIRCUIT

The AD9528 is capable of synchronizing multiple devices designed to the JESD204B JEDEC standard. Figure 26 illustrates the AD9528 synchronizing to the system reference clock. The AD9528 first jitter cleans the system reference clock and multiples up to a higher frequency in dual loop mode. The clock distribution of the AD9528 is used to clock and synchronize all the surrounding JESD204B devices together in the system.

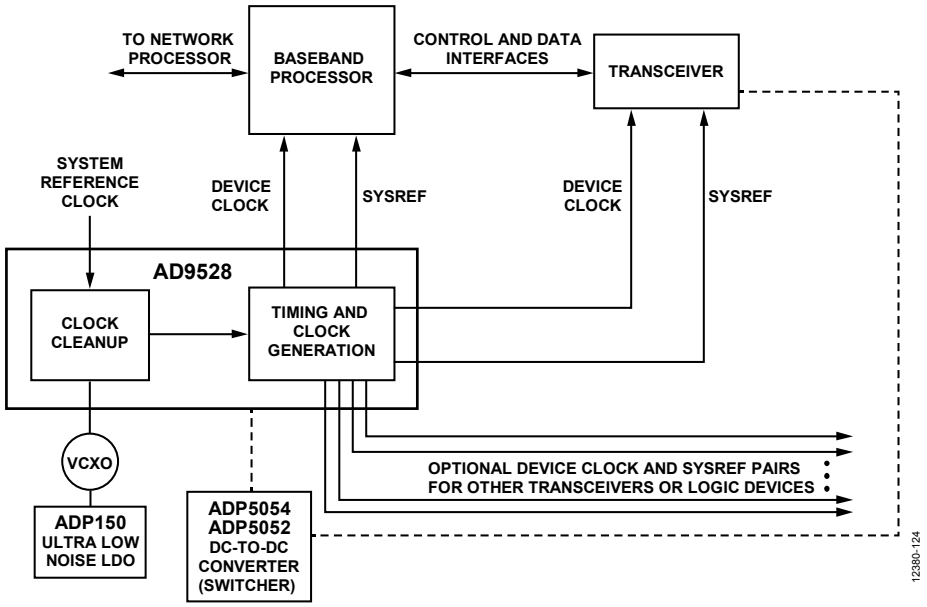


Figure 26. Synchronizing Multiple JESD204B Devices

TERMINOLOGY

Phase Jitter
An ideal sine wave has a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

Phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values with the units dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

In some applications, it is meaningful to integrate only the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase Noise
Phase noise has a detrimental effect on the performance of analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and radio frequency (RF) mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter
Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the SNR and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise
Additive phase noise is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter
Additive time jitter is the amount of time jitter that is attributable to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

THEORY OF OPERATION

DETAILED BLOCK DIAGRAM

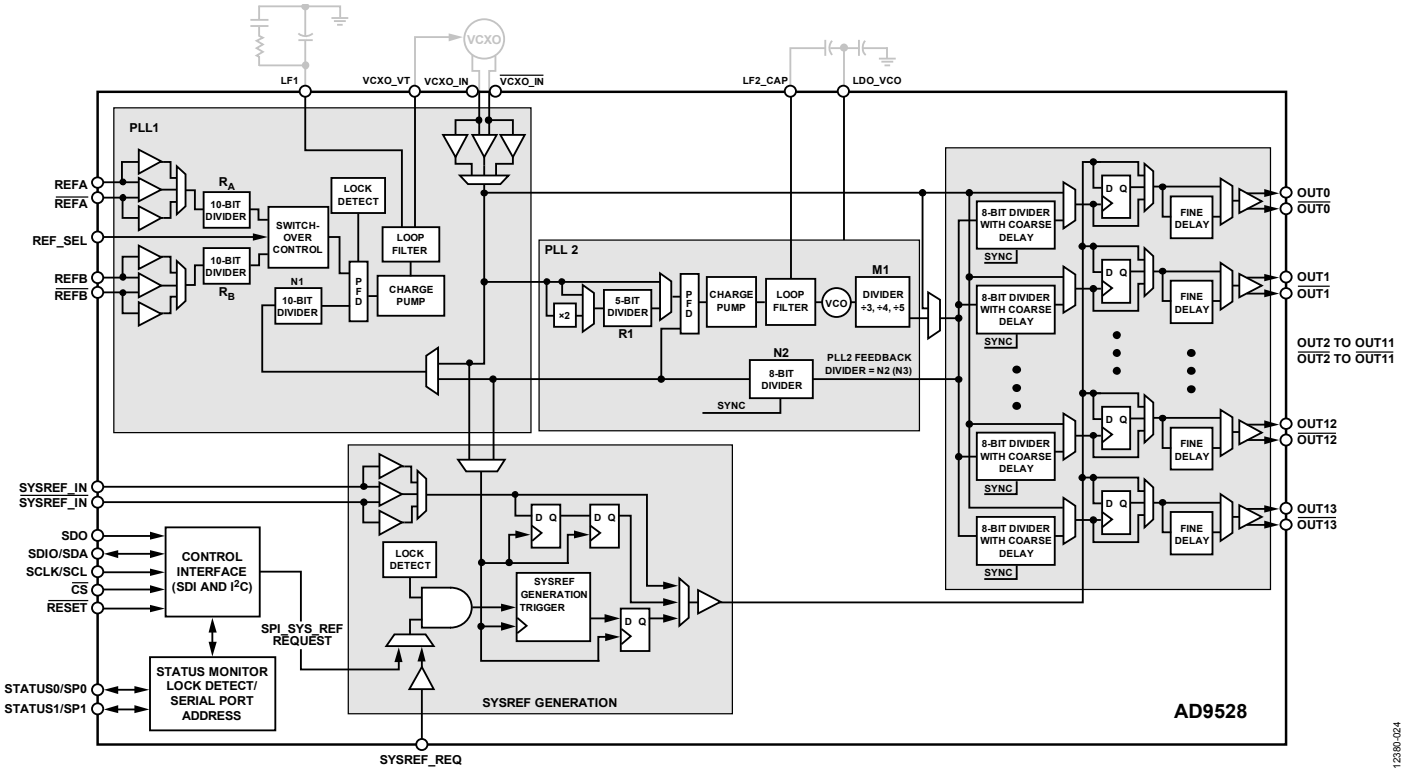


Figure 27. Top Level Diagram

OVERVIEW

The AD9528 is a clock generator that employs integer-N based phase-locked loops (PLL). The device architecture consists of two cascaded PLL stages. PLL1 consists of an integer division PLL that uses an external voltage controlled crystal oscillator (VCXO). PLL1 has a narrow loop bandwidth that provides initial jitter cleanup of the input reference signal for the input stage of PLL2. Conversely, the output of PLL1 is also routable to any clock distribution output, if desired.

PLL2 is a frequency multiplying PLL that translates the first PLL stage output frequency to a range of 3.450 GHz to 4.025 GHz. PLL2 incorporates an integer based feedback divider that enables integer frequency multiplication. An RF VCO divider (3, 4, or 5) divides the VCO output of PLL2 before being routed to the input of the clock distribution section. Programmable integer dividers (1 to 256) in the clock distribution follow the RF VCO divider, establishing a final output frequency up to 1 GHz or less for the 8 available outputs. The OUT0 to OUT3, OUT12, and OUT13 outputs can run up to 1.25 GHz.

All of the divider settings in the clock distribution section are configurable via the serial programming port, enabling a wide range of input/output frequency ratios under program control. The dividers also include a programmable coarse delay to adjust timing of the output signals, if required. In addition, a fine delay adjust is available in the clock distribution path.

The outputs are compatible with LVDS and HSTL logic levels. The AD9528 can produce a JESD204B SYSREF signal. This signal can be routed to any of the 14 outputs. The AD9528 can also receive an externally generated SYSREF signal and buffer to the outputs, with or without retiming. The AD9528 operates over the extended industrial temperature range of −40°C to +85°C.

The AD9528 includes reference monitoring and automatic/manual switchover and holdover. A reference select pin is available to manually select which input reference is active. The accuracy of the holdover is dependent on the external VCXO frequency stability.

All power supply pins on the AD9528 operate on a 3.3 V ±5% supply domain. However, each power supply pin has a dedicated internal LDO regulator that provides approximately 1.8 V for standard operation of the device. These independent regulators provide extra supply rejection and help with output to output coupling, since none of the output drivers or dividers share a supply.

COMPONENT BLOCKS—PLL1

PLL1 General Description

PLL1 consists of a phase/frequency detector (PFD), a charge pump, an external VCXO, and a partially external loop filter operating in a closed loop.

PLL1 has the flexibility to operate with a narrow loop bandwidth. This relatively narrow loop bandwidth gives the AD9528 the ability to suppress jitter that appears on the input references (REFA and REFB). The low phase noise output of PLL1 acts as the reference to PLL2 and can be routed to the clock distribution section.

PLL1 Reference Clock Inputs

The AD9528 features two separate reference clock inputs, REFA and REFB. These inputs can be configured to accept differential or single-ended signals. REFA and REFB are self biased in differential mode and high impedance in single ended CMOS mode. If REFA or REFB is driven single-ended, decouple the unused side ($\overline{\text{REFA}}$, $\overline{\text{REFB}}$) via a suitable capacitor to a quiet ground. These inputs may be dc-coupled, but set the dc operation point as specified in the Specifications section.

The differential reference input receiver is powered down when the differential reference input is not selected, or when the PLL1 is powered down. The single-ended buffers power down when the PLL1 is powered down, when their respective individual power-down registers are set, or when the differential receiver is selected.

PLL1 Loop Filter

The PLL1 loop filter is mostly external from LF1 (Pin 7) to ground. The value of the external components depend on the external VCXO and the configuration parameters, such as input clock rate and desired PLL1 loop bandwidth.

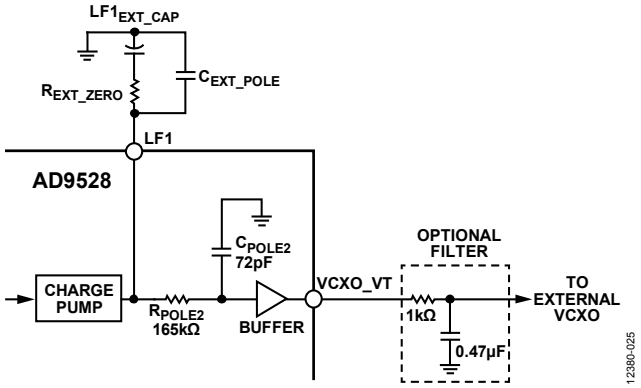


Figure 28. PLL1 Loop Filter

An external RC low-pass filter is recommended at the VCXO_VT output for the best noise performance at 1 kHz offset. The pole of this filter must be sufficiently high enough in frequency to avoid stability problems with the PLL loop bandwidth.

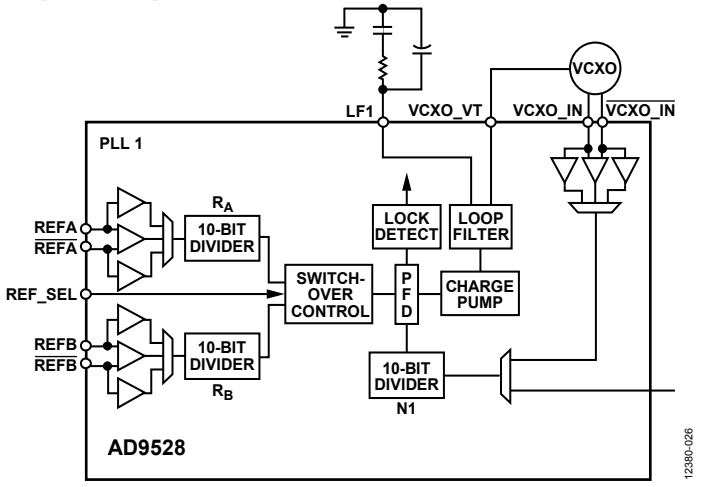


Figure 29. Input PLL (PLL1) Block Diagram

PLL1 Input Dividers

Each reference input has a dedicated reference divider block. The input dividers provide division of the reference frequency in integer steps from 1 to 1023.

VCXO Input

The VCXO receiver provides the low phase noise oscillator input for PLL1. This signal is also the reference input for PLL2. In addition, the VCXO input is used when either PLL1 is bypassed, or PLL1 and PL2 are bypassed to use the AD9528 as a buffer.

PLL1 Reference Switchover

The reference monitor verifies the presence or absence of the REFA and REFB signals. The status of the reference monitor guides the activity of the switchover control logic. The AD9528 supports automatic and manual PLL reference clock switching between REFA (the REFA and $\overline{\text{REFA}}$ pins) and REFB (the REFB and $\overline{\text{REFB}}$ pins).

There are several configurable modes of reference switchover. The manual switchover is achieved either via programming a register setting or by using the REF_SEL pin. If manually selecting REFB, REFB must be present prior to when the switchover to REFB occurs. The automatic switchover occurs when REFA disappears and a reference is on REFB. PLL1 operates with REFA as the primary reference input; this is relevant to the switchover operation of the device.

The reference switchover circuitry recognizes that REFA is the master reference. For the reference monitoring circuitry to work properly, REFA must be present during initial locking, regardless of whether REFB is present or not. When both references are used, REFA and REFB must be present. When a single reference is used, the reference must be REFA.

The reference automatic switchover can be set to work as follows:

- Nonrevertive. Stay on REFB. Switch from REFA to REFB when REFA disappears, but do not switch back to REFA if it reappears. If REFB disappears, then go back to REFA.
- Revert to REFA. Switch from REFA to REFB when REFA disappears. Return to REFA from REFB when REFA returns.

If a switchover event occurs in nonrevertive mode and the missing input to REFA is reestablished, the return of the missing reference does not reset the nonrevertive switchover logic. The result of this setup is that, if REFB is selected during nonrevertive switchover mode and nonrevertive switchover is disabled and reenabled, REFB is still the active reference, regardless if REFA is present. The switchover logic can be reset by issuing a device reset.

PLL1 Holdover

In the absence of both input references, the device enters holdover mode. When the device switches to holdover mode, the charge pump tristates, allowing VCXO_VT to maintain its existing value for a period of time. Optionally, the charge pump can be programmed to force VCXO_VT to VDD/2. The device continues operating in this mode until a reference signal becomes available. Then the device exits holdover mode, and PLL1 resynchronizes with the active reference. Automatic holdover mode can be disabled with a register bit. PLL2 remains locked to the VCXO signal even when PLL1 is in holdover.

PLL1 Lock Time

The typical PLL1 lock time occurs within 5× the period of the loop bandwidth, assuming a third-order loop filter with a phase margin of 55°. It may take up to 10× the period of the loop bandwidth for the PLL1 lock detector circuit to show locked status.

Calculate PLL1_TO in Figure 52 as

$$PLL1\_TO = 10/LBW_{PLL1}$$

where:
PLL1_TO is the PLL1 timeout.
LBW_{PLL1} is the loop bandwidth of PLL1.

COMPONENT BLOCKS—PLL2

PLL2 General Description

PLL2 consists of an optional input reference 2× multiplier, reference divider, a PFD, a mostly integrated analog loop filter, an integrated voltage controlled oscillator (VCO), and a feedback divider. The VCO produces a nominal 3.8 GHz signal with an output divider that is capable of division ratios of 3, 4, and 5.

PLL2 has a VCO with multiple bands spanning a range of 3.450 GHz to 4.025 GHz. The device automatically selects the appropriate band as part of its calibration process.

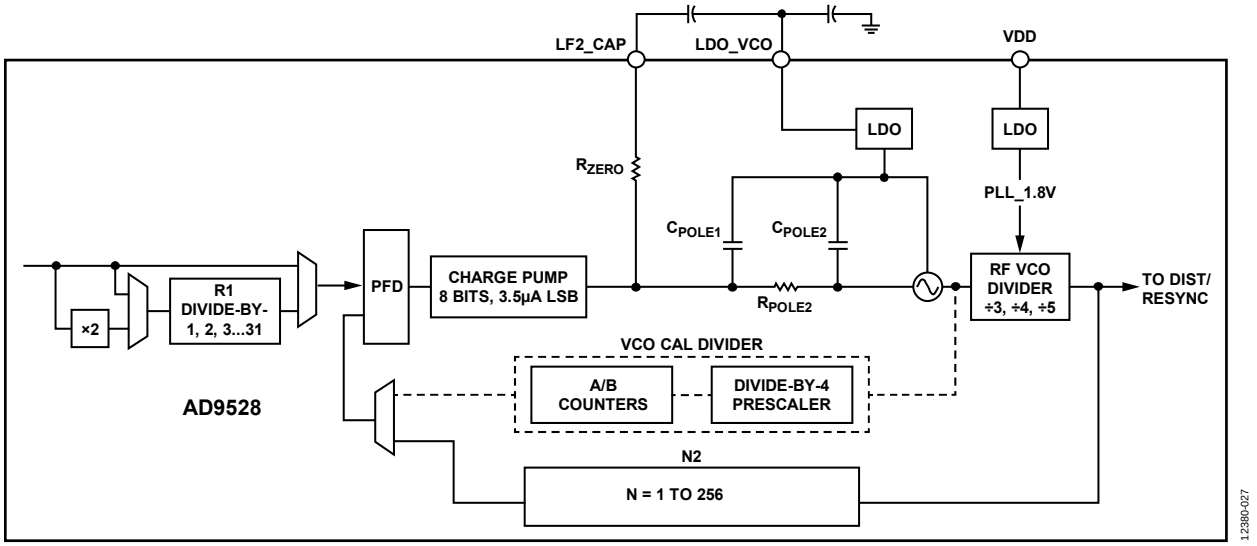


Figure 30. PLL2 Block Diagram

PLL2 Input 2× Frequency Multiplier

The 2× frequency multiplier provides the option to double the frequency at the PLL2 reference input. A higher frequency at the input to the PLL2 (PFD) allows reduced in-band phase noise and greater separation between the frequency generated by the PLL and the modulation spur associated with the PFD. Note that, as the input duty cycle deviates from 50%, harmonic distortion may increase. As such, beneficial use of the frequency multiplier is application specific. Typically, a VCXO with proper interfacing has a duty cycle that is approximately 50% at the VCXO_IN inputs. Note that the maximum output frequency of the 2× frequency multipliers must not exceed the maximum PFD rate specified in Table 7.

If the 2× frequency multiplier is used, a fixed phase offset can occur from power-up to power-up between the input to the 2× frequency multiplier and the PLL2 PFD reference input. This presents the possibility for a fixed phase offset between the VCXO_IN frequency and PLL2 output of ½ the period of the signal applied to the VCXO_IN and $\overline{\text{VCXO\_IN}}$ pins. If the internal SYSREF generator is used, choose the PLL2 feedback path as the input signal of the SYSREF generator to ensure fixed phase alignment of the SYSREF generator from power-up to power-up.

PLL2 Input Reference Divider

The input reference divider (R1) provides division in integer steps from 1 to 31 with a maximum input frequency of 275 MHz. The divider provides an option to prescale the PFD rate of PLL2 for output frequency planning and to accommodate more flexibility for setting the desired loop bandwidth for PLL2.

If the R1 divider is used along with the SYSREF generator, choose the PLL2 feedback path as the input signal of the SYSREF generator to ensure fixed phase alignment of the SYSREF generator from power-up to power-up.

PLL2 Feedback Dividers

PLL2 has two feedback paths as shown in Figure 30. In normal PLL2 operation mode, the PLL2 feedback path consists of N2 (an 8-bit divider) and M1 (a VCO RF divider). The product of N2 and M1 establishes the total PLL multiplication value for PLL2.

The second feedback path for PLL2 uses the VCO CAL divider (see Figure 30). The VCO CAL divider is exclusively used to calibrate the internal VCO of PLL2. Register 0x0201, Register 0x0204, Register 0x0207, and Register 0x0208 program the PLL multiplication values for both PLL2 feedback paths.

The total PLL multiplication in both feedback paths must equal one another for proper VCO calibration. After each VCO calibration, the VCO CAL divider feedback path automatically disables and reverts back to the feedback path with N2 and M1 dividers for normal operation. The VCO CAL divider is not available outside of VCO calibration.

The VCO CAL divider consists of a prescaler (P) divider and two counters, A and B. The total divider value is

$$VCO\ CAL\ divider = (P \times B) + A$$

where $P = 4$.

The VCO CAL feedback divider has a dual modulus prescaler architecture with a nonprogrammable P that is equal to 4. The value of the B counter can be from 3 to 63, and the value of the A counter can be from 0 to 3. 16 is the minimum supported divide value.

The VCO RF divider (M1) provides frequency division between the internal VCO and the clock distribution. The VCO RF divider can be set to divide by 3, 4, or 5. The VCO RF divider is part of the total PLL2 feedback path value for normal operation.

PLL2 Loop Filter

The PLL2 loop filter requires the connection of an external capacitor from LF2_CAP (Pin 14) to LDO_VCO (Pin 15). The value of the external capacitor depends on the operating mode and the desired phase noise performance. For example, a loop bandwidth of approximately 500 kHz produces the lowest integrated jitter. A lower bandwidth produces lower phase noise at 1 MHz but increases the total integrated jitter

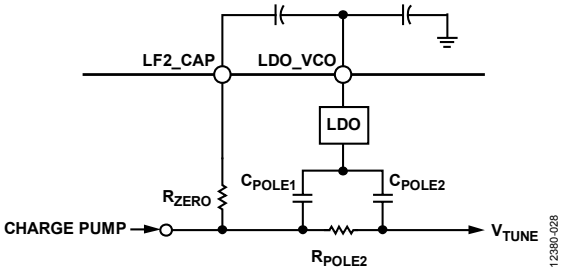


Figure 31. PLL2 Loop Filter

Table 22. PLL2 Loop Filter Programmable Values (Register 0x0205)

R_{ZERO} (Ω)	C_{POLE1} (pF)	R_{POLE2} (Ω)	C_{POLE2} (pF)	LF2_CAP[2] (pF)
3250	48	900	Fixed at 16	Typical at 1000
3000	40	450	N/A[1]	N/A[1]
2750	32	300	N/A[1]	N/A[1]
2500	24	225	N/A[1]	N/A[1]
2250	16	N/A[1]	N/A[1]	N/A[1]
2100	8	N/A[1]	N/A[1]	N/A[1]
2000	0	N/A[1]	N/A[1]	N/A[1]
1850		N/A[1]	N/A[1]	N/A[1]

[1] N/A means not applicable.
[2] External loop filter capacitor.

VCO

The VCO is tunable from 3.450 GHz to 4.025 GHz. The VCO operates off the VCO LDO supply. This LDO requires an external compensation cap of 0.47 µF to ground. The VCO requires calibration prior to use.

VCO Calibration

The AD9528 on-chip VCO must be manually calibrated to ensure proper PLL2 operation over process, supply, and temperature. VCO calibration requires a valid VCXO input clock and applicable preprogrammed PLL1 and PLL2 register values prior to issuing the VCO calibration to ensure a PLL2 phase lock condition.

In addition, the value of the VCO CAL feedback divider (see Figure 30) must equal the combined divider values of both the 8-bit N2 divider and RF VCO divider (M1). For example, if the N2 divide value is 10 and the M1 divide value is 3, the total PLL2 multiplication value is 30 in normal operation, so the VCO CAL divider value must be set to 30 prior to initiating a VCO calibration. See the PLL2 Feedback Dividers section for more details. When total PLL2 feedback divider value is 15, see Figure 53 for the detailed procedure.

VCO calibration is initiated by transitioning the calibrate VCO bit (Bit 0 of Register 0x0203) from 0 to 1 (this bit is not self clearing). The setting can be performed as part of the initial setup before executing the IO_UPDATE bit (Register 0x000F, Bit 0 = 1). A readback bit, VCO calibration in progress (Register 0x0509, Bit 0), indicates when a VCO calibration is in progress by returning a logic true (that is, Bit 0 = 1), however this bit is automatically cleared after the calibration is finished, so it tells if the calibration started but did not finish. After calibration, initiate a sync (see the Clock Distribution Synchronization section). A sync occurs automatically after calibration. See Figure 53 for the detailed procedure.

During power-up or reset, channels driven by the RF VCO driver are automatically held in sync until the first VCO calibration is finished. Therefore, none of those channel outputs can occur until VCO calibration is complete.

Initiate a VCO calibration under the following conditions:

- After changing the PLL2 N2 or M1 divider settings or after a change in the PLL2 reference clock frequency. This means that a VCO calibration must be initiated any time that a PLL2 register or reference clock changes such that a different VCO frequency is the result.
- Whenever system calibration is desired. The VCO is designed to operate properly over temperature extremes, even when it is first calibrated at the opposite extreme. However, a VCO calibration can be initiated at any time.

To calibrate using the 2× multiplier, the total feedback divide must be >16. If the application requires the use of a feedback divide value <16, see the following example:

For f_{VCXO} = 122.88 MHz, f_{VCO} = 3686.4 MHz, M1 = 3, N2 = 5, and with the 2× multiplier enabled, the total feedback divider value of 15 is less than the supported minimum for the calibration divider. To calibrate, the 2× multiplier must be disabled, and the calibration divider must be set to 30. After the calibration is complete, the 2× multiplier is enabled and the PLL acquires lock.

PLL2 Lock Time/VCO Calibration Time

The typical PLL2 lock time occurs within 5× the period of the loop bandwidth, assuming a phase margin of 55°. It can take up to 10× the period of the loop bandwidth for the PLL2 lock detector circuit to show locked status. The typical PLL2 VCO calibration time is 400,000 periods of the PLL2 PFD rate.

Calculate PLL2_TO in Figure 52 as

$$PLL2\_TO = 10/LBW_{PLL2} + 400{,}000/f_{PFD\_PLL2}$$

where f_{PFD_PLL2} is the frequency of the PLL2 phase detector.

CLOCK DISTRIBUTION

The clock distribution consists of 14 individual channels (OUT0 to OUT13). The input frequency source for each channel output is selectable as either the PLL1 output, PLL2 output, or SYSREF. Each of the output channels also includes a

dedicated 8-bit divider, two dedicated phase delay elements and an output driver, as shown in Figure 32.

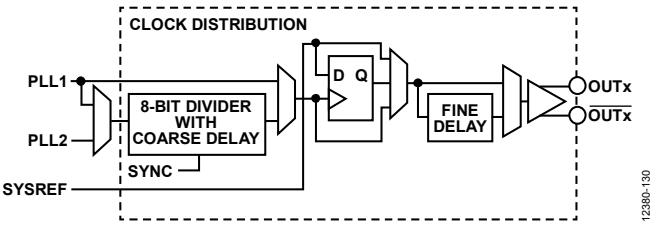


Figure 32. Clock Distribution Paths for PLL1, PLL2, and SYSREF Frequency Sources

The following are various channel limitations, depending on the channel configuration:

- Analog fine delay is supported for all channels, regardless of the input frequency source selected.
- Digital coarse delay is only supported when the channel divider is used. When SYSREF is used as the frequency source, the signal must be retimed by the output of the channel divider to use the digital coarse delay.
- Output channel synchronization is performed by synchronously resetting the 8-bit channel divider via the sync outputs bit in Register 0x032A, Bit 0. Therefore, the 8-bit divider path must be used to support synchronization. If SYSREF is the frequency source to an output, the SYSREF signal must be resampled by the output of the channel divider for a SYNC to occur.

Clock Dividers

The output clock distribution dividers are referred to as D0 to D13, corresponding to output channels OUT0 through OUT13, respectively. Each divider is programmable with 8 bits of precision equal to any number from 1 through 256. Dividers have duty cycle correction set to provide nominal 50% duty cycle, even for odd divides. Note that a sync output command must be issued after changing the divide value to ensure the intended divide ratio occurs at the channel output(s).

Digital Coarse Delay

The AD9528 supports programmable phase offsets from 0 to 63 steps (6 bits) in half period increments of the RF VCO divider output frequency. Note that a sync output command must be issued after the new phase offset(s) are programmed to ensure the intended phase offset occurs at the channel output(s). This is accomplished by programming the new phase offset and then issuing a sync command via Register 0x032A, Bit 0. All outputs are disabled temporarily while the sync is active, unless the channel is programmed to ignore the sync command. The ignore sync command for each channel is controlled via Register 0x032B and Register 0x032C.

Analog Fine Delay

Each channel includes a 4-bit fine analog delay block intended to provide substantially smaller delay steps compared to the half cycle of the RF VCO divider output. The fine analog delay enable bit in each channel activates the fine delay path; when the enable bit is asserted with the four delay bits = 0000, the minimum insertion delay is nominally 425 ps. Full-scale delay = 1111 adds another 496 ps of additional delay. The average fine delay resolution step is approximately 31 ps.

Output Channel Power-Down

Each output channel has independent power-down control via Register 0x0501 and Register 0x0502. The total device power is reduced with each channel powered down, keeping the output static until the user is ready to disable the channel power-down control. In addition, Register 0x0503 and Register 0x0504 offer additional power savings via LDO power-down control for each channel output.

Output Drivers

Each channel and corresponding output driver has a dedicated internal LDO to power both the channel and output driver. The equivalent output driver circuits are shown in Figure 33 and Figure 34. The output driver design supports a common external 100 Ω differential resistor for both HSTL and LVDS driver modes. In LVDS mode, a current of 3.5 mA causes a 350 mV peak voltage across the 100 Ω load resistor. In LVDS boost mode, a current of 4.5 mA causes a 450 mV peak voltage across the 100 Ω load resistor. Similarly, in HSTL mode, a current of 9 mA causes a 900 mV peak voltage across the 100 Ω load resistor.

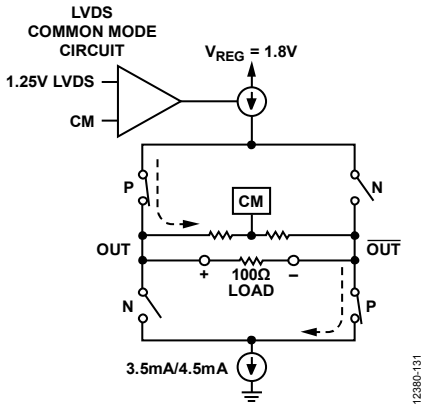


Figure 33. LVDS Output Driver

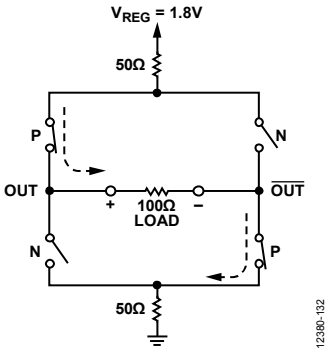


Figure 34. HSTL Output Driver

Clock Distribution Synchronization

A block diagram of the clock distribution synchronization functionality is shown in Figure 35. The synchronization feature edge aligns all outputs together or to forces a desired phase offset between output edges. An automatic synchronization of the channel dividers is initiated the first time the PLL2 locks after a power-up or reset event. Subsequent lock and unlock events do not initiate a resynchronization unless preceded by a power-down or reset of the device.

All outputs are disabled temporarily while the sync output bit in Register 0x032A, Bit 0 is active, unless the channel is programmed to ignore the sync output command. The ignore sync command for each channel is controlled via Register 0x032B and Register 0x032C.

When using the sync output bit to synchronize outputs, first set and then clear the bit. The synchronization event is the clearing operation (that is, the Logic 1 to Logic 0 transition of the bit). The channel dividers are automatically synchronized to each other when PLL2 is ready.

In normal operation, the phase offsets are already programmed through the SPI/I²C port before the AD9528 starts to provide outputs. Although the digital coarse phase offsets cannot be adjusted while the dividers are operating, it is possible to adjust the phase of all outputs relative to each other without powering down PLL1 and PLL2. This is accomplished by programming the new phase offset using Bits[5:0] in the clock distribution registers, and then issuing an output sync by using the sync outputs bit (Register 0x032A, Bit 0).

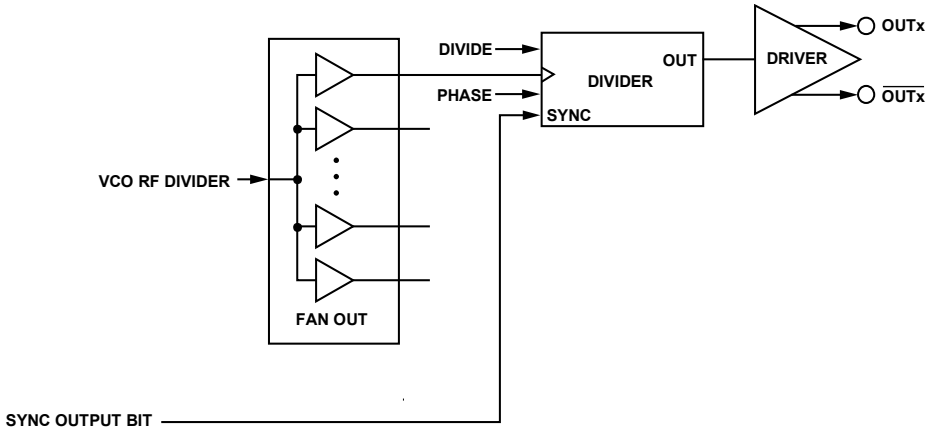


Figure 35. Clock Distribution Synchronization Block Diagram

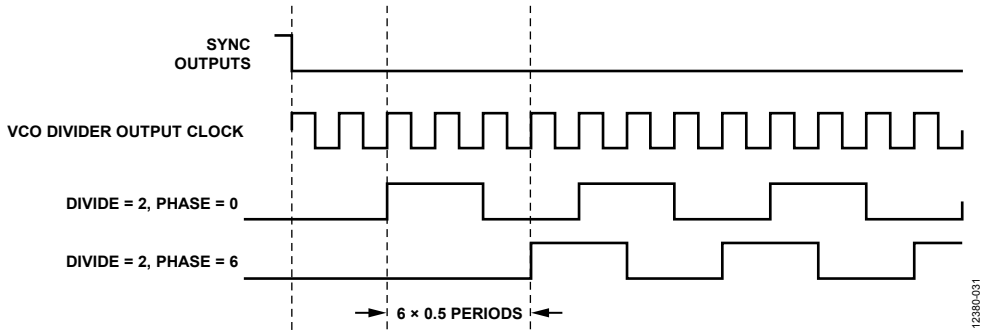


Figure 36. Clock Output Synchronization Timing Diagram

SYSREF OPERATION

The AD9528 supports the JESD204B standard for synchronizing high speed converters and logic devices such as FPGAs by providing paired device clock and SYSREF clock signals. The SYSREF clock or device clock can be distributed to any one or more of the 14 outputs via the clock distribution section within the AD9528. After the SYSREF clock reaches the clock distribution section, programmable digital coarse delay and/or analog fine delay is available to adjust timing between the SYSREF clock with respect to the device clock. The delay establishes proper setup and hold timing downstream between device clock and SYSREF clock at the inputs of the converter(s) or logic device(s).

SYSREF SIGNAL PATH

The AD9528 provides two sources for the purpose of generating a SYSREF signal. The first source is a user provided external SYSREF clock signal applied to SYSREF_IN and $\overline{\text{SYSREF\_IN}}$ (Pin 70 and Pin 71, respectively). The second source is an internal SYSREF generation circuit that enables the user to specify an internally generated pulse pattern. There are three modes of operation associated with the two sources as defined by Register 0x0403, Bits[7:6].

- 00 = Mode 1 (external SYSREF)
- 01 = Mode 2 (external SYSREF resampled by the VCXO or PLL2 feedback divider)
- 1x = Mode 3 (internally generated SYSREF).

SYSREF Mode 1: External

Figure 37 shows the SYSREF clock path with Mode 1 selected. Apply an external SYSREF clock signal to the SYSREF_IN and/or $\overline{\text{SYSREF\_IN}}$ pin(s). A single-ended signal may be applied to either pin separately or a differential signal may be applied across both pins. Note that the SYSREF_REQ pin and Bit 0 of Register 0x0403 (SPI SYSREF Request) are unused in Mode 1.

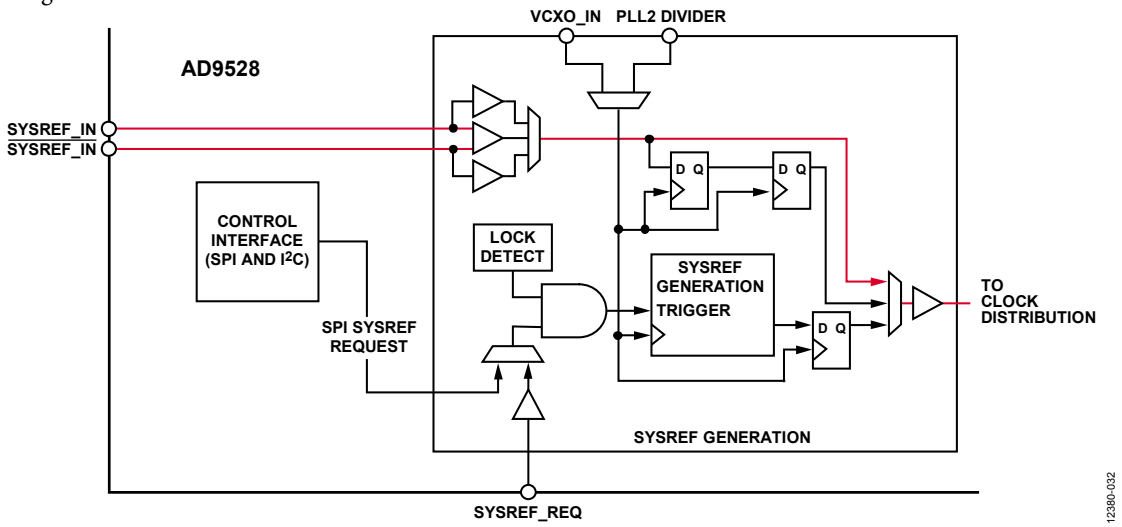


Figure 37. Mode 1, Routes the External SYSREF Directly to the Clock Distribution Output(s)

SYSREF Mode 2: External with Retiming

Figure 38 shows the SYSREF clock path with Mode 2 selected. Apply a differential or single-ended SYSREF clock signal to the SYSREF_IN and $\overline{\text{SYSREF\_IN}}$ pins (see Mode 1).

Unlike Mode 1, Mode 2 retimes the external SYSREF signal either with the signal originating at the VCXO_IN and $\overline{\text{VCXO\_IN}}$ pins (Pin 11 and Pin 12, respectively), or with the signal at the feedback node of PLL2. Register 0x0402, Bit 4 selects the source that retimes the external SYSREF signal. Note that the SYSREF_REQ pin and Bit 0 of Register 0x0403 (SPI SYSREF Request) are unused in Mode 2.

SYSREF Mode 3: Internal

Figure 39 shows the SYSREF clock path with Mode 3 selected. Mode 3 uses the internal SYSREF pattern generator and the SYSREF request feature to produce a user defined SYSREF signal. A SYSREF request can be made via hardware (the SYSREF_REQ pin) or software (Register 0x0403, Bit 0, the SPI SYSREF request bit). In internal SYSREF mode, the PLLs must be locked before the SYSREF request signal is used.

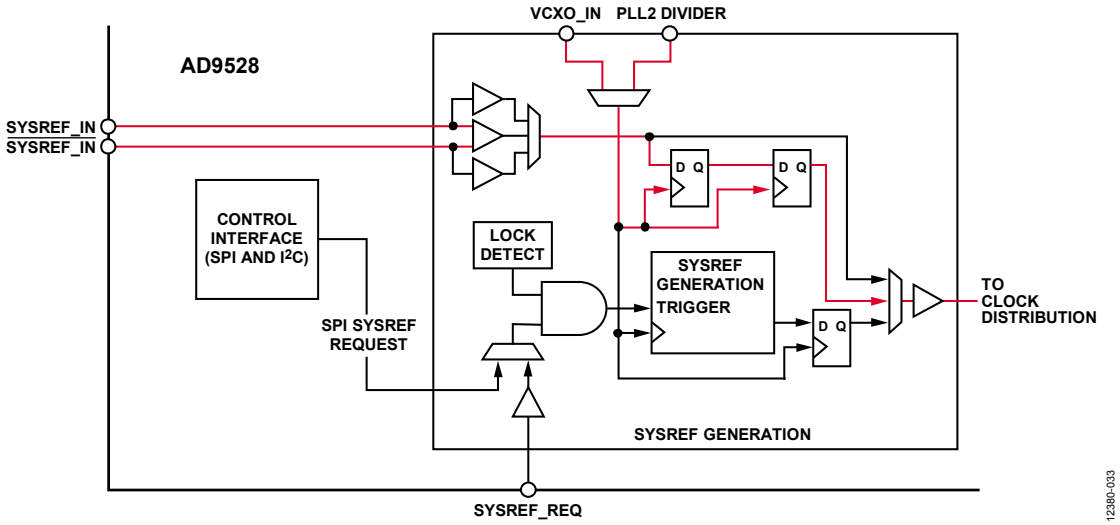


Figure 38. Mode 2, Retimes the External SYSREF to the Internal VCXO or PLL2 Input Divider Output and then Routes to the Clock Distribution Output(s)

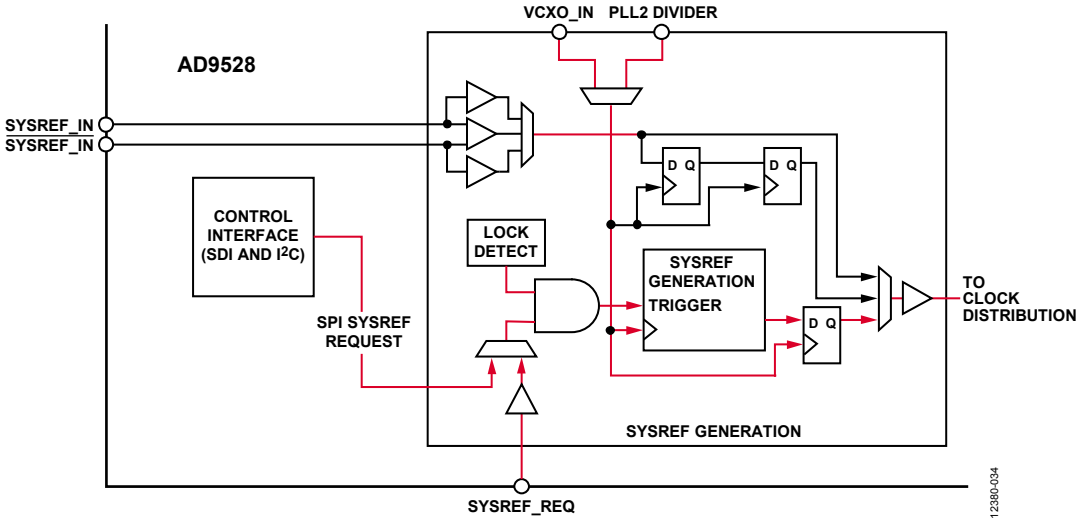


Figure 39. Mode 3, SYSREF Generated Internally and Routed to the Clock Distribution

SYSREF GENERATOR

The SYSREF pattern generator produces a user defined SYSREF signal (see Table 23). The input clock to the pattern generator is provided by the signal originating at the VCXO_IN and $\overline{\text{VCXO\_IN}}$ pins, or with the signal at the feedback node of PLL2. The pattern generator contains a fixed divide by 2 followed by a programmable 16-bit K divider (set by Register 0x0401 and Register 0x0400) to program the pulse width of the SYSREF. The value of K ranges from 0 to 65535. For example, if the pattern generator input clock is 122.88 MHz, the maximum SYSREF period is 131,070/122,880,000 seconds (1066 µs). The pattern generator acts as a timer that only issues pulses synchronous to all other outputs, regardless of when an asynchronous SYSREF request is issued.

SYSREF Request

The SYSREF request signal starts or stops the internal SYSREF pattern generator. The signal is controlled by software or via pin control. The SYSREF request method is controlled by Register 0x0402, Bit 7.

Software Control

In software control mode, the SYSREF pattern generator is always level trigger sensitive to the SYSREF pattern generator trigger control bits (Register 0x402, Bits[6:5]). With Bit 6 = 0 for level trigger mode, Bit 5 is used as the trigger. If N-shot mode is enabled, set Bit 5 = 1 from 0 to start the SYSREF pattern sequence. After the sequence is complete and N pulses are output, the SYSREF pattern generator automatically clears Bit 5 and waits for the next SYSREF request.

In continuous mode, the pattern sequence continues if Bit 5 = 1. Clear Bit 5 to stop the sequence and wait for the next SYSREF request.

Pin Control—Level Trigger Mode

In level trigger mode (Register 0x0402, Bit 6 = 0), the SYSREF pattern generator is controlled by the SYSREF_REQ pin. If N-shot mode is enabled, force the SYSREF_REQ pin to 1 from 0 to start the SYSREF pattern sequence. After the sequence is complete and N pulses are output, force the SYSREF_REQ pin to 0. The pattern generator then waits for the next SYSREF request.

In continuous mode, force the SYSREF_REQ pin to 1 from 0 to start the SYSREF pattern sequence. Force the SYSREF_REQ pin to 0 to stop the sequence. The pattern generator then waits for next SYSREF request.

Pin Control—Edge Trigger Mode

In edge trigger mode, the SYSREF pattern generator is controlled by the rising edge or falling edge on the SYSREF_REQ pin. The rising or falling active edge is determined by Register 0x0402, Bits[6:5]. With Bit 6 = 1, Bit 5 controls the active trigger edge. If N-shot mode is enabled, the SYSREF_REQ pin active edge starts the SYSREF pattern sequence. After the sequence is complete and N pulses are output, the pattern generator waits for the next SYSREF request. If SYSREF_REQ is set to 0 before N pulse(s) are done, the current pattern sequence is not affected. Therefore, if the new SYSREF_REQ active edge arrives before the pattern sequence is complete, the new request is missed.

In continuous mode, the SYSREF_REQ active edge starts the SYSREF pattern sequence. After the sequence, the pattern generator waits for the next SYSREF request.

Table 23. On-Chip SYSREF Generation Modes

SYSREF Pattern Generator Mode (Register 0x0403, Bits[5:4])	Generation Output Mode	Description
00	N-shot mode (Register 0x0403, Bits[3:1]) N-shot mode[2:0] = 001 = 1 pulse out N-shot mode[2:0] = 010 = 2 pulses out N-shot mode[2:0] = 011 = 4 pulses out N-shot mode[2:0] = 100 = 6 pulses out N-shot mode[2:0] = 101 = 8 pulses out N-shot mode[2:0] = 110 or greater = 1 pulse out	The SYSREF outputs N pulses after the SYSREF request is initiated and then the SYSREF output goes logic low until the next SYSREF request. N can be programmed as 1, 2, 4, 6, or 8.
01	Continuous mode	The SYSREF output continuously outputs a 101010…pulse train and behaves like a clock with a frequency of $f_{IN}/(2 \times K)$ after the SYSREF request is initiated.
10	PRBS	Not applicable.
11	Stop	In stop mode, the SYSREF output is static low.

SERIAL CONTROL PORT

The AD9528 serial control port is a flexible, synchronous serial communications port that provides a convenient interface to many industry-standard microcontrollers and microprocessors. The AD9528 serial control port is compatible with most synchronous transfer formats, including I²C, Motorola SPI, and Intel SSR protocols. The serial control port allows read/write access to the AD9528 register map.

The AD9528 uses the Analog Devices unified SPI protocol. The unified SPI protocol guarantees that all new Analog Devices products using the unified protocol have consistent serial port characteristics. The SPI port configuration is programmable via Register 0x0000. This register is a part of the SPI control logic rather than in the register map and is distinct from the I²C Register 0x0000.

Unified SPI differs from the SPI port found on older products like the AD9523 and AD9524 in the following ways:

- Unified SPI does not have byte counts. A transfer is terminated when the $\overline{CS}$ pin goes high. The W1 and W0 bits in the traditional SPI become the A12 and A13 bits of the register address. This is similar to streaming mode in the traditional SPI.
- The address ascension bit (Register 0x0000, Bit 2 and Bit 5) controls whether register addresses are automatically incremented or decremented regardless of the LSB/MSB first setting. In traditional SPI, LSB first dictated auto-increments and MSB first dictated autodecrements of the register address.
- Devices that adhere to the unified serial port have a consistent structure of the first 16 register addresses.

Although the AD9528 supports both the SPI and I²C serial port protocols, only one is active following power-up (as determined by the STATUS0/SP0 and STATUS1/SP1 multifunction pins during the start-up sequence). The only way to change the serial port protocol is to reset (or power cycle) the device.

SPI/I²C PORT SELECTION

The AD9528 has two serial interfaces, SPI and I²C. Users can select either the SPI or I²C depending on the states (logic high, logic low) of the two logic level input pins (STATUS0/SP0 and STATUS1/SP1), when initial power is applied or after a $\overline{RESET}$. When both STATUS/SP1 and STATUS0/SP0 are low, the SPI interface is active. Otherwise, I²C is active with two different I²C slave address settings (seven bits wide), as shown in Table 24. The five most significant bits (MSBs) of the slave address are hardware coded as 10101, and the two LSBs are determined by the logic levels of the STATUS1/SP1and STATUS0/SP0 pins.

Table 24. Serial Port Mode Selection

STATUS1/SP1	STATUS0/SP0	Address
Low	Low	SPI
Low	High	I²C = 1010100
High	Low	Undefined
High	High	I²C = 1010101

SPI SERIAL PORT OPERATION

Pin Descriptions

The SCLK (serial clock) pin serves as the serial shift clock. This pin is an input. SCLK synchronizes serial control port read and write operations. The rising edge SCLK registers write data bits, and the falling edge registers read data bits. The SCLK pin supports a maximum clock rate of 50 MHz.

The SPI port supports both 3-wire (bidirectional) and 4-wire (unidirectional) hardware configurations and both MSB-first and LSB-first data formats. Both the hardware configuration and data format features are programmable. The 3-wire mode uses the SDIO (serial data input/output) pin for transferring data in both directions. The 4-wire mode uses the SDIO pin for transferring data to the AD9528, and the SDO pin for transferring data from the AD9528.

The $\overline{CS}$ (chip select) pin is an active low control that gates read and write operations. Assertion (active low) of the $\overline{CS}$ pin initiates a write or read operation to the AD9528 SPI port. Any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented based on the setting of the address ascension bits (Register 0x0000, Bit 2 and Bit 5). $\overline{CS}$ must be deasserted at the end of the last byte transferred, thereby ending the stream mode. This pin is internally connected to a 35 kΩ pull-up resistor. When $\overline{CS}$ is high, the SDIO and SDO pins go into a high impedance state.

Implementation Specific Details

The following product specific items are defined in the unified SPI protocol:

- Analog Devices unified SPI protocol Revision: 1.0
- Chip type: 0x5
- Clock serial ID: 0x00F
- Physical layer: 3-and 4-wire supported
- Optional single-byte instruction mode: not supported
- Data link not used
- Control not used

Communication Cycle—Instruction Plus Data

The unified SPI protocol consists of a two-part communication cycle. The first part is a 16-bit instruction word that is coincident with the first 16 SCLK rising edges and a payload. The instruction word provides the AD9528 serial control port with information regarding the payload. The instruction word includes the R/$\overline{W}$ bit that indicates the direction of the payload transfer (that is, a read or write operation). The instruction word also indicates the starting register address of the first payload byte.

Write

If the instruction word indicates a write operation, the payload is written into the serial control port buffer of the AD9528. Data bits are registered on the rising edge of SCLK. Generally, it does not matter what data is written to blank registers; however, it is customary to use 0s. Note that there may be reserved registers with default values not equal to 0x00; however, every effort was made to avoid this.

Most of the serial port registers are buffered and data written into these buffered registers does not take effect immediately. An additional operation is needed to transfer buffered serial control port contents to the registers that actually control the device. This transfer is accomplished with an IO_UPDATE operation, which is performed in one of two ways. One method is to write a Logic 1 to Register 0x000F, Bit 0 (this bit is an autoclearing bit). The user can change as many register bits as desired before executing an IO_UPDATE. The IO_UPDATE operation transfers the buffer register contents to their active register counterparts.

Read

If the instruction word indicates a read operation, the next N × 8 SCLK cycles clock out the data starting from the address specified in the instruction word. N is the number of data bytes read. The readback data is driven to the pin on the falling edge and must be latched on the rising edge of SCLK. Blank registers are not skipped over during readback.

A readback operation takes data from either the serial control port buffer registers or the active registers, as determined by Register 0x0001, Bit 5.

SPI Instruction Word (16 Bits)

The MSB of the 16-bit instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next 15 bits are the register address (A14 to A0), which indicates the starting register address of the read/write operation (see Table 26). Note that A14 and A13 are ignored and treated as zeros in the AD9528 because there are no registers that require more than 13 address bits.

SPI MSB-/LSB-First Transfers

The AD9528 instruction word and payload can be MSB first or LSB first. The default for the AD9528 is MSB first. The LSB first mode can be set by writing a 1 to Register 0x0000, Bit 1 and Bit 6. Immediately after the LSB first bit is set, subsequent serial control port operations are LSB first.

Address Ascension

If the address ascension bits (Register 0x0000, Bit 2 and Bit 5) are zero, the serial control port register address decrements from the specified starting address toward Address 0x0000.

If the address ascension bits (Register 0x0000, Bit 2 and Bit 5) are one, the serial control port register address increments from the starting address toward Address 0x1FFF. Reserved addresses are not skipped during multibyte input/output operations; therefore, write the default value to a reserved register and 0s to unmapped registers. Note that it is more efficient to issue a new write command than to write the default value to more than two consecutive reserved (or unmapped) registers.

Table 25. Streaming Mode (No Addresses Skipped)

Address Ascension	Stop Sequence
Increment	0x0000…0x1FFF
Decrement	0x1FFF…0x0000

Table 26. Serial Control Port, 16-Bit Instruction Word

MSB															LSB
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

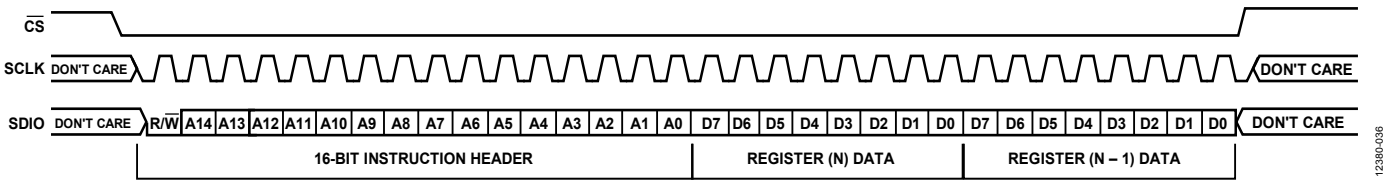


Figure 40. Serial Control Port Write—MSB First, Address Decrement, Two Bytes of Data

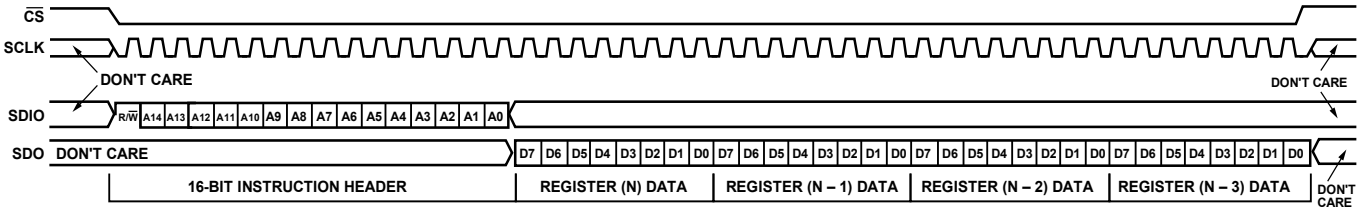


Figure 41. Serial Control Port Read—MSB First, Address Decrement, Four Bytes of Data

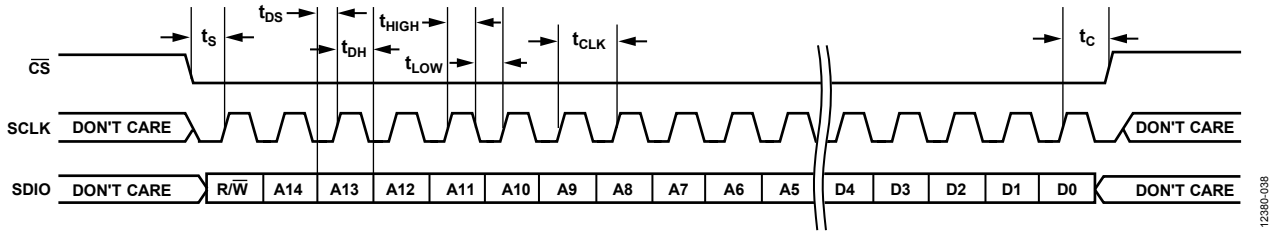


Figure 42. Timing Diagram for Serial Control Port Write—MSB First

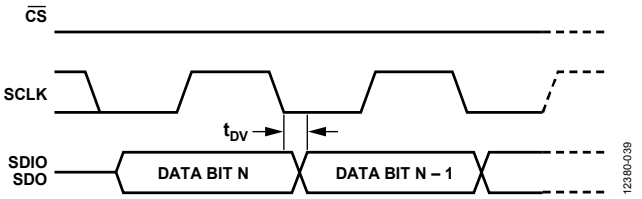


Figure 43. Timing Diagram for Serial Control Port Register Read—MSB First

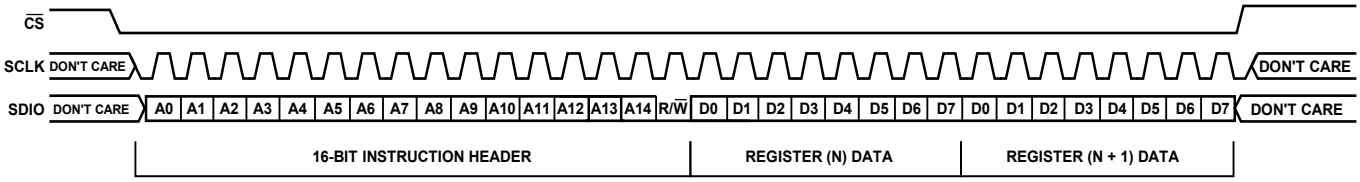


Figure 44. Serial Control Port Write—LSB First, Address Increment, Two Bytes of Data

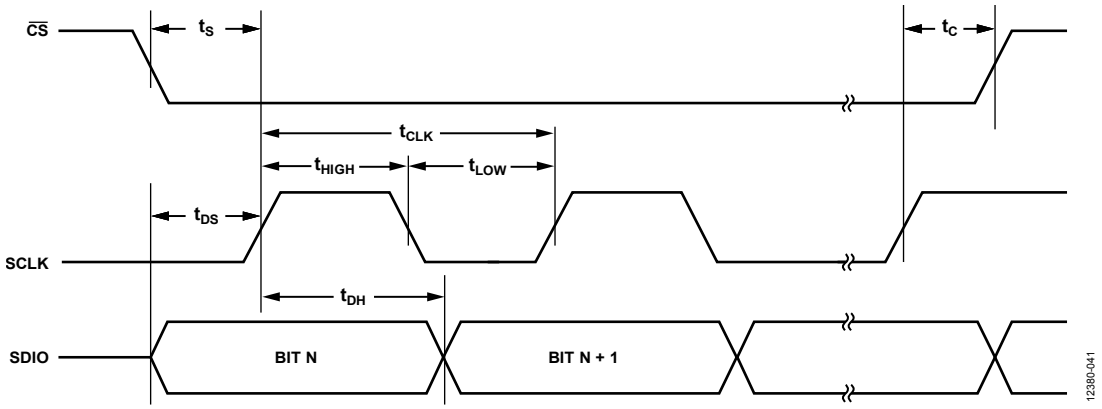


Figure 45. Serial Control Port Timing—Write

Table 27. Serial Control Port Timing

Parameter	Description
t_{DS}	Setup time between data and the rising edge of SCLK
t_{DH}	Hold time between data and the rising edge of SCLK
t_{CLK}	Period of the clock
t_S	Setup time between the $\overline{CS}$ falling edge and the SCLK rising edge (start of the communication cycle)
t_C	Setup time between the SCLK rising edge and $\overline{CS}$ rising edge (end of the communication cycle)
t_{HIGH}	Minimum period that SCLK is in a logic high state
t_{LOW}	Minimum period that SCLK is in a logic low state
t_{DV}	SCLK to valid SDIO (see Figure 43)

I²C SERIAL PORT OPERATION

The I²C interface is popular because it requires only two pins and easily supports multiple devices on the same bus. Its main disadvantage is programming speed, which is 400 kbps (maximum). The AD9528 I²C port design uses the I²C fast mode; however, it supports both the 100 kHz standard mode and 400 kHz fast mode.

The AD9528 does not strictly adhere to every requirement in the original I²C specification. In particular, specifications such as slew rate limiting and glitch filtering are not implemented. Therefore, the AD9528 is I²C compatible, but may not be fully I²C compliant.

The AD9528 I²C port consists of a serial data line (SDA) and a serial clock line (SCL). In an I²C bus system, the AD9528 is connected to the serial bus (data bus SDA and clock bus SCL) as a slave device; that is, no clock is generated by the AD9528. The AD9528 uses direct 16-bit memory addressing instead of more common 8-bit memory addressing.

The AD9528 allows up to two unique slave devices to occupy the I²C bus. These are accessed via a 7-bit slave address transmitted as part of an I²C packet. Only the device with a matching slave address responds to subsequent I²C commands. Table 24 lists the supported device slave addresses.

I²C Bus Characteristics

A summary of the various I²C abbreviations appears in Table 28.

Table 28. I²C Bus Abbreviation Definitions

Abbreviation	Definition
S	Start
Sr	Repeated start
P	Stop
A	Acknowledge
$\overline{A}$	No acknowledge
$\overline{W}$	Write
R	Read

The transfer of data is shown in Figure 46. One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can change only when the clock signal on the SCL line is low.

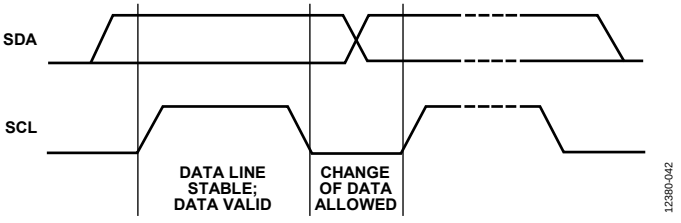


Figure 46. Valid Bit Transfer

Start/stop functionality is shown in Figure 47. The start condition is characterized by a high to low transition on the SDA line while SCL is high. The master always generates the start condition to initialize a data transfer. The stop condition is characterized by a low to high transition on the SDA line while SCL is high. The master always generates the stop condition to terminate a data transfer. Every byte on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit; bytes are sent MSB first.

The acknowledge bit (A) is the ninth bit attached to any 8-bit data byte. An acknowledge bit is always generated by the receiving device (receiver) to inform the transmitter that the byte has been received by pulling the SDA line low during the ninth clock pulse after each 8-bit data byte.

The no acknowledge bit ($\overline{A}$) is the ninth bit attached to any 8-bit data byte. A no acknowledge bit is always generated by the receiving device (receiver) to inform the transmitter that the byte has not been received by leaving the SDA line high during the ninth clock pulse after each 8-bit data byte. After issuing a no acknowledge bit, the AD9528 I²C state machine goes into an idle state.

Data Transfer Process

The master initiates data transfer by asserting a start condition, which indicates that a data stream follows. All I²C slave devices connected to the serial bus respond to the start condition.

The master then sends an 8-bit address byte over the SDA line, consisting of a 7-bit slave address (MSB first) plus an R/$\overline{W}$ bit. This bit determines the direction of the data transfer, that is, whether data is written to or read from the slave device (0 = write and 1 = read).

The peripheral whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is 0, the master (transmitter) writes to the slave device (receiver). If the R/$\overline{W}$ bit is 1, the master (receiver) reads from the slave device (transmitter).

The format for these commands is described in the Data Transfer Format section.

Data is then sent over the serial bus in the format of nine clock pulses, one data byte (eight bits) from either master (write mode) or slave (read mode) followed by an acknowledge bit from the receiving device. The number of bytes that can be transmitted per transfer is unrestricted. In write mode, the first two data bytes immediately after the slave address byte are the internal memory (control registers) address bytes, with the high address byte first. This addressing scheme gives a memory address of up to $2^{16} - 1 = 65,535$. The data bytes after these two memory address bytes are register data written to the control registers. In read mode, the data bytes after the slave address byte are register data written to or read from the control registers.

When all the data bytes are read or written, stop conditions are established. In write mode, the master (transmitter) asserts a stop condition to end data transfer during the clock pulse following the acknowledge bit for the last data byte from the slave device (receiver). In read mode, the master device (receiver) receives the last data byte from the slave device (transmitter) but does not pull SDA low during the ninth clock pulse. This is known as a no acknowledge bit. By receiving the no acknowledge bit, the slave device knows that the data transfer is finished and enters idle mode. The master then pulls the data line low during the low period before the 10th clock pulse, and high during the 10th clock pulse to assert a stop condition.

A start condition can be used in place of a stop condition. Furthermore, a start or stop condition can occur at any time, and partially transferred bytes are discarded.

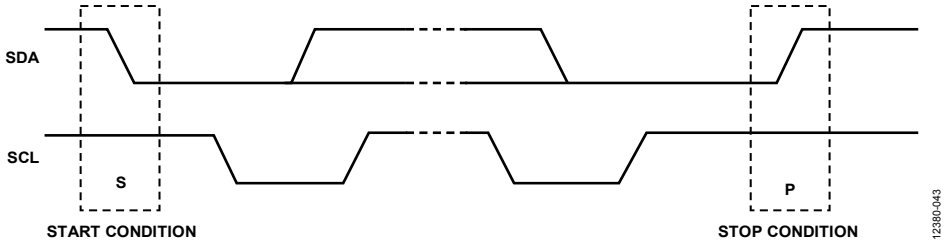


Figure 47. Start and Stop Conditions

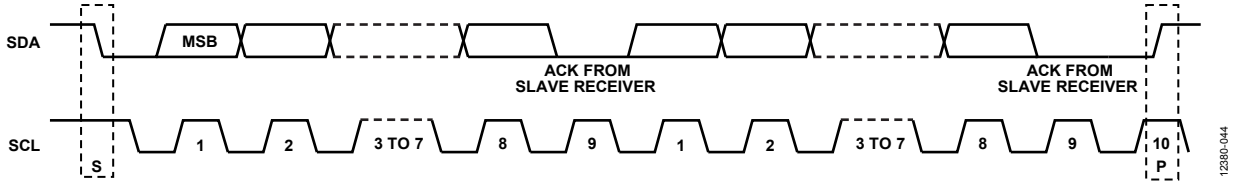


Figure 48. Acknowledge Bit

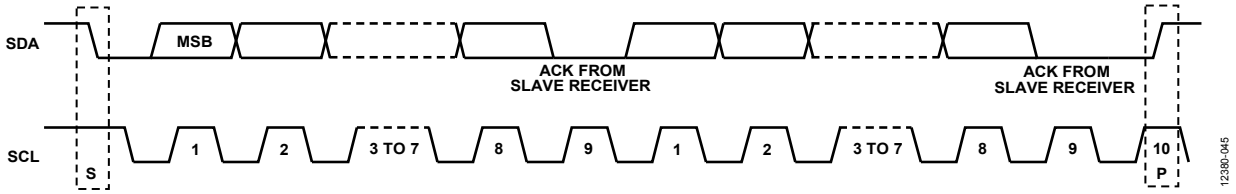


Figure 49. Data Transfer Process (Master Write Mode, 2-Byte Transfer)

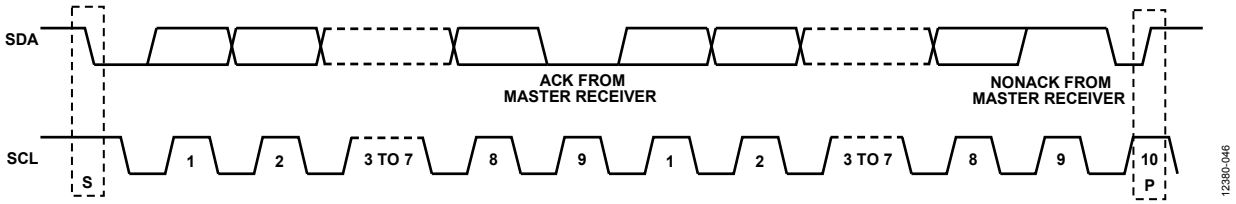


Figure 50. Data Transfer Process (Master Read Mode, 2-Byte Transfer), First ACK From Slave

Data Transfer Format

The write byte format is used to write a register address to the RAM starting from the specified RAM address (see Table 29).

Table 29. Data Transfer Format, Write Byte Format

S	Slave address	$\overline{W}$	A	RAM address high byte	A	RAM address low byte	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	A	P

The send byte format is used to set up the register address for subsequent reads (see Table 30).

Table 30. Data Transfer Format, Send Byte Format

S	Slave address	$\overline{W}$	A	RAM address high byte	A	RAM address low byte	A	P

The receive byte format is used to read the data byte(s) from RAM starting from the current address (see Table 31).

Table 31. Data Transfer Format, Receive Byte Format

S	Slave address	R	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	$\overline{A}$	P

The read byte format is the combined format of the send byte and the receive byte (see Table 32).

Table 32. Data Transfer Format, Read Byte Format

S	Slave address	$\overline{W}$	A	RAM address high byte	A	RAM address low byte	A	Sr	Slave address	R	A	RAM Data 0	A	RAM Data 1	A	RAM Data 2	$\overline{A}$	P

I²C Serial Port Timing

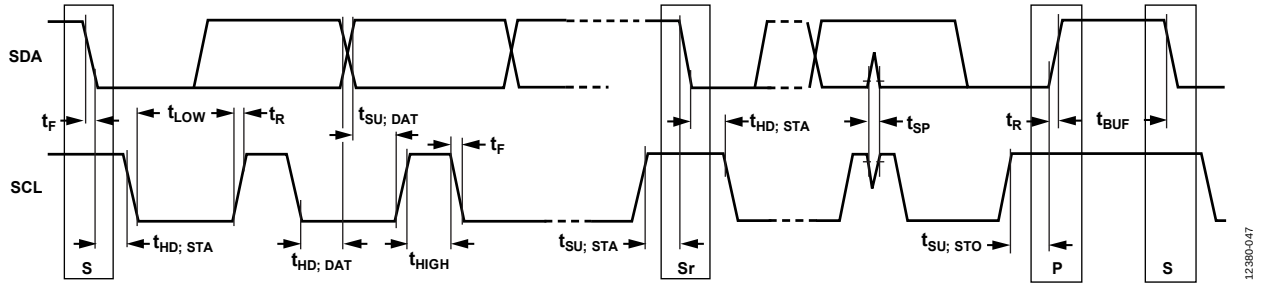


Figure 51. I²C Serial Port Timing

Table 33. I²C Timing Definitions

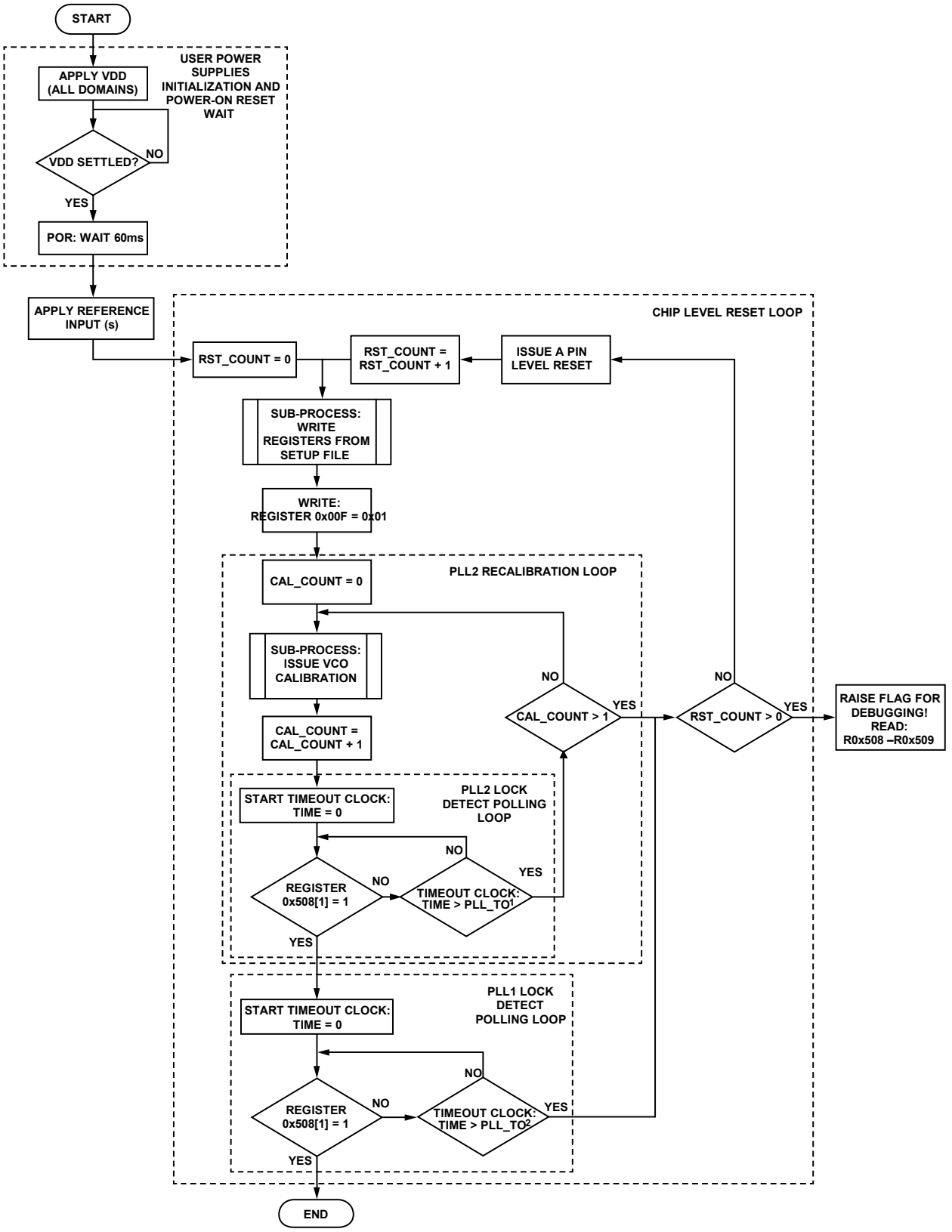
Parameter	Description
f_{SCL}	Serial clock
t_{BUF}	Bus free time between stop and start conditions
$t_{HD;\ STA}$	Repeated hold time start condition
$t_{SU;\ STA}$	Repeated start condition setup time
$t_{SU;\ STO}$	Stop condition setup time
$t_{HD;\ DAT}$	Data hold time
$t_{SU;\ DAT}$	Data setup time
t_{LOW}	SCL clock low period
t_{HIGH}	SCL clock high period
t_R	Minimum/maximum receive SCL and SDA rise time
t_F	Minimum/maximum receive SCL and SDA fall time
t_{SP}	Pulse width of voltage spikes that must be suppressed by the input filter

DEVICE INITIALIZATION AND CALIBRATION FLOWCHARTS

The flowcharts in this section show a typical AD9528 initialization routine using an evaluation software generated setup file (.stp), and calibration routines designed for robust system startup.

Figure 52, Figure 53, Figure 54, and Figure 55 assume the following: dual loop configuration, VCXO with a ±100 ppm pull range, and a valid frequency translation from a .stp file. These flowcharts are provided as recommendations.

The count variable for the chip level reset loop (RST_COUNT) and the count variable for the PLL2 recalibration loop (CAL_COUNT) are count variables used to establish a count limit to a loop, such that it is not an infinite loop. These variables only apply to initialization.



[1]PLL1_TO IS A CALCULATED VALUE TIME OUT VALUE. PLEASE SEE THEORY OF OPERATION–COMPONENT BLOCKS–PLL1 FOR ITS FORMULA.
[2]PLL2_TO IS A CALCULATED VALUE TIME OUT VALUE. PLEASE SEE THEORY OF OPERATION–COMPONENT BLOCKS–PLL2 FOR ITS FORMULA.

Figure 52. Main Process, Initialization

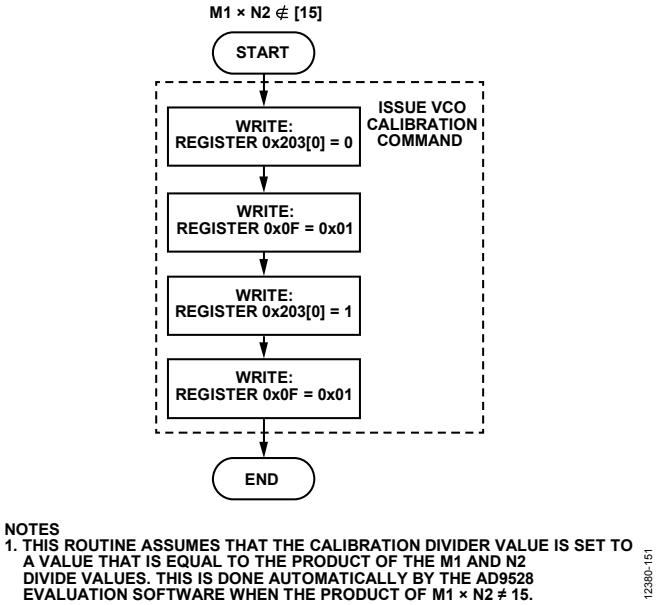
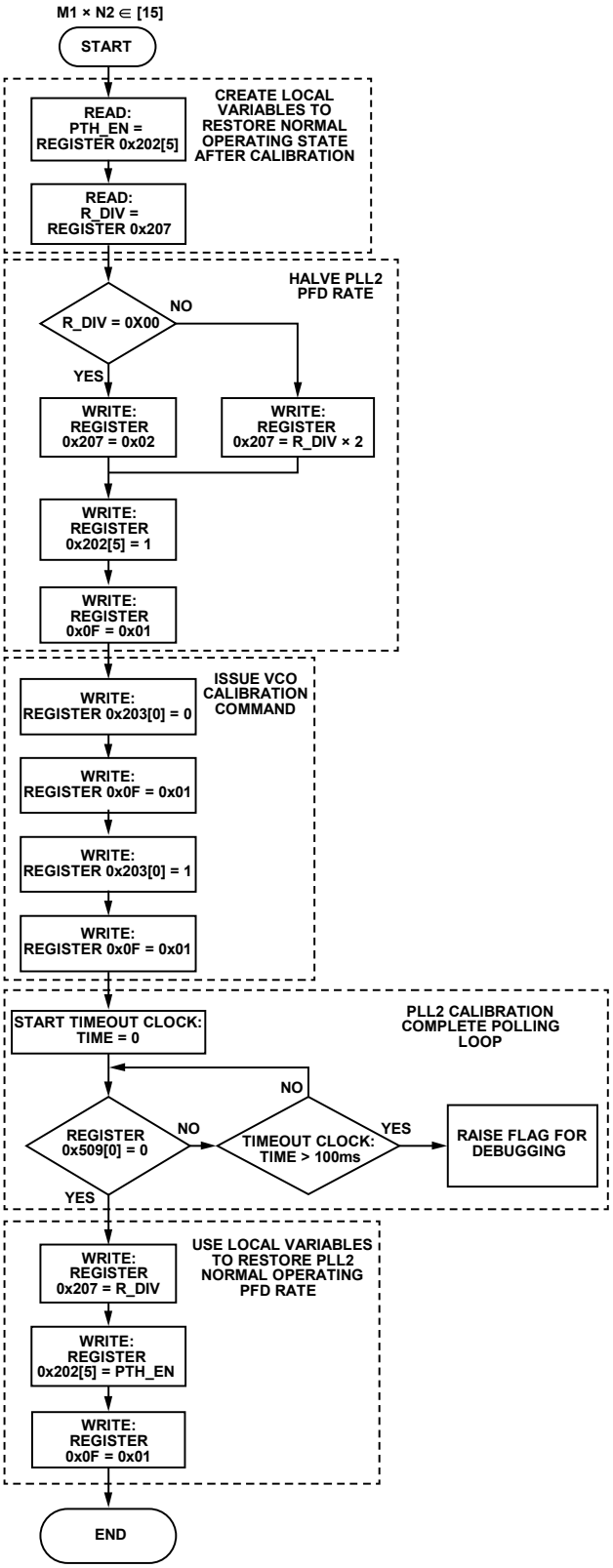


Figure 53. Subprocess, Issue VCO Calibration (M1 × N2 ≠ 15)



NOTES
1. THIS ROUTINE ASSUMES THAT THE CALIBRATION DIVIDER VALUE IS SET TO A VALUE THAT IS EQUAL TO TWICE THE PRODUCT OF THE M1 AND N2 DIVIDE VALUES. THIS IS DONE AUTOMATICALLY BY THE AD9528 EVALUATION SOFTWARE WHEN THE PRODUCT OF M1 × N2 = 15.

12380-251

Figure 54. Subprocess, Issue VCO Calibration (M1 × N2 = 15)

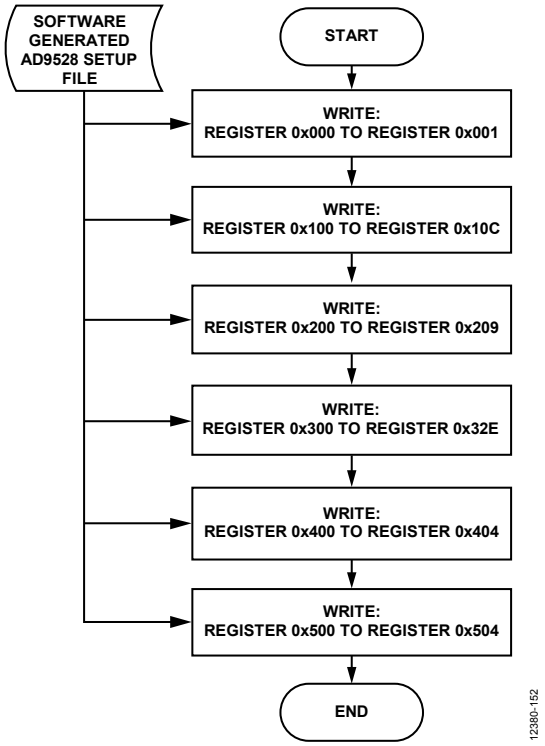


Figure 55. Subprocess, Write Registers from the Setup File

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The AD9528 is a multifunctional, high speed device that targets a wide variety of clock applications. The numerous innovative features contained in the device each consume incremental power. If all outputs are enabled in the maximum frequency and mode that have the highest power, the safe thermal operating conditions of the device may be exceeded. Careful analysis and consideration of power dissipation and thermal management are critical elements in the successful application of the AD9528.

The AD9528 is specified to operate within the industrial temperature range of –40°C to +85°C. This specification is conditional, such that the absolute maximum junction temperature is not exceeded (as specified in Table 19). At high operating temperatures, extreme care must be taken when operating the device to avoid exceeding the junction temperature and potentially damaging the device.

Many variables contribute to the operating junction temperature within the device, including

- Selected driver mode of operation
- Output clock speed
- Supply voltage
- Ambient temperature

The combination of these variables determines the junction temperature within the AD9528 for a given set of operating conditions.

The AD9528 is specified for an ambient temperature (T_A). To ensure that T_A is not exceeded, use an airflow source.

Use the following equation to determine the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured at the top center of the package.
Ψ_{JT} is the value from Table 20.
PD is the power dissipation of the AD9528.

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of Ψ_{JB} are provided for package comparison and PCB design considerations.

CLOCK SPEED AND DRIVER MODE

Clock speed directly and linearly influences the total power dissipation of the device and, therefore, the junction temperature. Two operating frequencies are listed under the incremental power dissipation parameter in Table 3. Using linear interpretation is a sufficient approximation for frequency not listed in the table. When calculating power dissipation for thermal consideration, remove the amount of power dissipated in the 100 Ω resistor. If using the data in Table 3, this power is already removed. If using the current vs. frequency graphs provided in the Typical Performance Characteristics section, the power into the load must be subtracted, using the following equation:

$$P_{LOAD} = Differential\ Output\ Voltage\ Swing^2/100\ \Omega$$

EVALUATION OF OPERATING CONDITIONS

The first step in evaluating the operating conditions is to determine the maximum power consumption (PD) internal to the AD9528. The maximum PD excludes power dissipated in the load resistors of the drivers because such power is external to the device. Use the power dissipation specifications listed in Table 3 to calculate the total power dissipated for the desired configuration.

Table 34 and Table 35 summarize the incremental power dissipation from the base power configuration for two different examples.

Table 34. Temperature Gradient Examples, Example 1

Description	Mode	Frequency (MHz)	Maximum Power (mW)
Base Typical Configuration	N/A[1]	N/A[1]	590
Output Driver	6 × HSTL	122.88	480
Output Driver	3 × LVDS	122.88	210
Output Driver	1 × LVDS	409.6	78
Total Power			1358

[1] N/A means not applicable.

Table 35. Temperature Gradient Examples, Example 2

Description	Mode	Frequency (MHz)	Maximum Power (mW)
Base Typical Configuration	N/A[1]	N/A[1]	590
Output Driver	13 × HSTL	122.88	1040
Total Power			1630

[1] N/A means not applicable.

The second step in evaluating the operating conditions is to multiply the power dissipated by the thermal impedance to determine the maximum power gradient. For this example, a thermal impedance of θ_{JA} = 21.1°C/W was used.

Example 1

(1358 mW × 21.1°C/W) = 29°C

With an ambient temperature of 85°C, the junction temperature is

T_J = 85°C + 29°C = 114°C

This junction temperature is below the maximum allowable.

Example 2

(1630 mW × 21.1°C/W) = 34°C

With an ambient temperature of 85°C, the junction temperature is

T_J = 85°C + 34°C = 119°C

This junction temperature is greater than the maximum allowable. The ambient temperature must be lowered by 4°C to operate in the condition of Example 2.

THERMALLY ENHANCED PACKAGE MOUNTING GUIDELINES

See the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, for more information about mounting devices with an exposed paddle.

CONTROL REGISTER MAP

Table 36. Register Summary

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
Serial Port Configuration										
0x0000	SPI Configuration A	Soft reset[1]	LSB first (SPI only)[2]	Address ascension (SPI only)[3]	SDO active (SPI only)[4]	SDO active (SPI only)[4]	Address ascension (SPI only)[3]	LSB first (SPI only)[2]	Soft reset[1]	0x00
0x0001	SPI Configuration B	Reserved		Read buffer register	Reserved		Reset sans regmap	Reserved		0x00
0x0002	Reserved	Reserved								0x00
Clock Part Family ID										
0x0003	Chip type	Reserved				Chip type, Bits[3:0]				0x05
0x0004	Product ID	Clock part serial ID, Bits[3:0]				Reserved				0xFF
0x0005		Clock part serial ID, Bits[11:4]								0x00
0x0006	Revision	Part versions, Bits[7:0]								0x03
0x0007	Reserved	Reserved								0x00
0x0008	Reserved	Reserved								0x00
0x0009	Reserved	Reserved								0x00
0x000A	Reserved	Reserved								0x00
0x000B	SPI version	SPI version, Bits[7:0]								0x00
0x000C	Vendor ID	Vendor ID, Bits[7:0]								0x56
0x000D		Vendor ID, Bits[15:8]								0x04
0x000E	Reserved	Reserved								0x00
0x000F	IO_UPDATE	Reserved							IO_UPDATE	0x00
PLL1 Control										
0x0100	PLL1 REFA (R_A) divider	10-bit REFA (R_A) divider, Bits[7:0]								0x00
0x0101		Reserved						10-bit REFA (R_A) divider, Bits[9:8]		0x00
0x0102	PLL1 REFB (R_B) divider	10-bit REFB (R_B) divider, Bits[7:0]								0x00
0x0103		Reserved						10-bit REFB (R_B) divider, Bits[9:8]		0x00
0x0104	PLL1 feedback divider (N1)	10-bit N1 divider [7:0]								0x00
0x0105		Reserved						10 bit N1 divider, Bits[9:8]		0x00
0x0106	PLL1 charge pump control	Force holdover	PLL1 charge pump current (µA), Bits[6:0]							0x0C
0x0107		Reserved		Disable holdover	Reserved			Charge pump mode, Bits[1:0]		0x00
0x0108	PLL1 input receiver control	Frequency detector power-down enable	$\overline{\text{REFB}}$ differential receiver enable	$\overline{\text{REFA}}$ differential receiver enable	REFB input receiver enable	REFA input receiver enable	VCXO receiver power-down enable	VCXO single-ended negative pin enable CMOS mode	VCXO differential receiver enable	0x00
0x0109		Reserved		N1 feedback divider reset	REFB divider (R_B) reset	REFA divider (R_A) reset	PLL1 feedback divider source	REFB single-ended negative pin enable (CMOS mode)	REFA single-ended negative pin enable (CMOS mode)	0x00
0x010A		Reserved				Holdover mode	Reference selection mode, Bits[2:0]			0x00
0x010B	PLL1 fast lock	Fast lock enable	Fast lock charge pump current (µA), Bits[6:0]							0x00

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
PLL2 Control										
0x0200	PLL2 charge pump control	PLL2 CP current (μA), Bits[7:0]								0x00
0x0201	PLL2 VCO CAL feedback dividers	A divider, Bits[1:0]		B divider, Bits[5:0]						0x04
0x0202	PLL2 control	Lock detect power-down enable	Reserved	Frequency doubler enable	Reserved			PLL2 charge pump mode, Bits[1:0]		0x03
0x0203	PLL2 VCO control	Reserved			Doubler and R1 divider path enable	Reset VCO calibration dividers	Treat reference as valid	Force VCO to midpoint frequency	Manual VCO calibrate (not autoclearing)	0x00
0x0204	PLL2 RF VCO divider (M1)	Reserved		PFD reference edge select	PFD feedback edge select	RF VCO divider (M1) power-down	RF VCO divider (M1), Bits[2:0]			0x00
0x0205	PLL2 loop filter control	R_{POLE2} (Ω), Bits[1:0]		R_{ZERO} (Ω), Bits[1:0]			C_{POLE1} (pF), Bits[1:0]			0x00
0x0206		Reserved							Bypass internal R_{ZERO} resistor	0x00
0x0207	PLL2 input divider (R1)	Reserved			5-bit R1 divider, Bits[4:0]					0x00
0x0208	PLL2 feedback divider (N2)	8-bit N2 divider, Bits[7:0]								0x00
0x0209		Reserved	N2 divider power-down	N2 phase, Bits[5:0]						0x00
Clock Distribution Control										
0x0300	Channel Output 0	Channel control, Bits[2:0]			Fine analog delay enable	Fine analog delay, Bits[3:0]				0x00
0x0301		Output format, Bits[1:0]		Coarse digital delay, Bits[5:0]						0x00
0x0302		Divide ratio, Bits[7:0]								0x04
0x0303	Channel Output 1	Channel control, Bits[2:0]			Fine analog delay enable	Fine analog delay, Bits[3:0]				0x40
0x0304		Output format, Bits[1:0]		Coarse digital delay, Bits[5:0]						0x00
0x0305		Divide ratio, Bits[7:0]								0x00
0x0306	Channel Output 2	Channel Control, Bits[2:0]			Fine analog delay enable	Fine analog delay, Bits[3:0]				0x00
0x0307		Output format, Bits[1:0]		Coarse digital delay [5:0]						0x00
0x0308		Divide ratio [7:0]								0x04
0x0309	Channel Output 3	Channel control, Bits[2:0]			Fine analog delay enable	Fine analog delay, Bits[3:0]				0x40
0x030A		Output format, Bits[1:0]		Coarse digital delay, Bits[5:0]						0x00
0x030B		Divide ratio [7:0]								0x00
0x030C	Channel Output 4	Channel control, Bits[2:0]			Fine analog delay enable	Fine analog delay, Bits[3:0]				0x00
0x030D		Output format, Bits[1:0]		Coarse digital delay, Bits[5:0]						0x00
0x030E		Divide ratio, Bits[7:0]								0x04
0x030F	Channel Output 5	Channel control, Bits[2:0]			Fine analog delay enable	Fine analog delay, Bits[3:0]				0x40
0x0310		Output format, Bits[1:0]		Coarse digital delay, Bits[5:0]						0x00
0x0311		Divide ratio, Bits[7:0]								0x00
0x0312	Channel Output 6	Channel control, Bits[2:0]			Fine analog delay enable	Fine analog delay, Bits[3:0]				0x00
0x0313		Output format, Bits[1:0]		Coarse digital delay, Bits[5:0]						0x00
0x0314		Divide ratio, Bits[7:0]								0x04

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
0x0315	Channel Output 7	Channel control, Bits[2:0]			Fine analog delay enable	Fine analog delay, Bits[3:0]				0x40
0x0316		Output format, Bits[1:0]		Coarse digital delay, Bits[5:0]						0x00
0x0317		Divide ratio, Bits[7:0]								0x00
0x0318	Channel Output 8	Channel control, Bits[2:0]			Fine analog delay enable	Fine analog delay, Bits[3:0]				0x00
0x0319		Output format, Bits[1:0]		Coarse digital delay, Bits[5:0]						0x00
0x031A		Divide ratio, Bits[7:0]								0x04
0x031B	Channel Output 9	Channel control, Bits[2:0]			Fine analog delay enable	Fine analog delay, Bits[3:0]				0x40
0x031C		Output format, Bits[1:0]		Coarse digital delay, Bits[5:0]						0x00
0x031D		Divide ratio, Bits[7:0]								0x00
0x031E	Channel Output 10	Channel control, Bits[2:0]			Fine analog delay enable	Fine analog delay, Bits[3:0]				0x00
0x031F		Output format, Bits[1:0]		Coarse digital delay, Bits[5:0]						0x00
0x0320		Divide ratio, Bits[7:0]								0x04
0x0321	Channel Output 11	Channel control, Bits[2:0]			Fine analog delay enable	Fine analog delay, Bits[3:0]				0x40
0x0322		Output format, Bits[1:0]		Coarse digital delay, Bits[5:0]						0x00
0x0323		Divide ratio [7:0]								0x00
0x0324	Channel Output 12	Channel control, Bits[2:0]			Fine analog delay enable	Fine analog delay, Bits[3:0]				0x20
0x0325		Output format, Bits[1:0]		Coarse digital delay, Bits[5:0]						0x00
0x0326		Divide ratio, Bits[7:0]								0x00
0x0327	Channel Output 13	Channel control, Bits[2:0]			Fine analog delay enable	Fine analog delay, Bits[3:0]				0x20
0x0328		Output format, Bits[1:0]		Coarse digital delay, Bits[5:0]						0x00
0x0329		Divide ratio, Bits[7:0]								0x00
Sync Control										
0x032A	Distribution sync	Reserved							Sync outputs	0x00
0x032B	Ignore sync enable	Channel 7 ignore sync	Channel 6 ignore sync	Channel 5 ignore sync	Channel 4 ignore sync	Channel 3 ignore sync	Channel 2 ignore sync	Channel 1 ignore sync	Channel 0 ignore sync	0x00
0x032C		Reserved	PLL2 feedback N2 divider ignore sync	Channel 13 ignore sync	Channel 12 ignore sync	Channel 11 ignore sync	Channel 10 ignore sync	Channel 9 ignore sync	Channel 8 ignore sync	0x00
0x032D	SYSREF Bypass resample control	Channel 6 bypass SYSREF resample	Channel 5 bypass SYSREF resample	Channel 4 bypass SYSREF resample	Channel 3 bypass SYSREF resample	Channel 2 bypass SYSREF resample	Channel 1 bypass SYSREF resample	Channel 0 bypass SYSREF resample	Enable VCXO receiver path to distribution	0x00
0x032E		Reserved	Channel 13 bypass SYSREF resample	Channel 12 bypass SYSREF resample	Channel 11 bypass SYSREF resample	Channel 10 bypass SYSREF resample	Channel 9 bypass SYSREF resample	Channel 8 bypass SYSREF resample	Channel 7 bypass SYSREF resample	0x00
SYSREF Control										
0x0400	SYSREF pattern generator K divider	K divider, Bits[7:0]								0x00
0x0401		K divider, Bits[15:8]								0x00
0x0402	SYSREF control	SYSREF request method	SYSREF pattern generator trigger control, Bits[1:0]		SYSREF pattern generator clock source	Resample clock source for external SYSREF	SYSREF test mode, Bits[1:0]		SYSREF reset	0x00
0x0403		SYSREF source, Bits[1:0]		SYSREF pattern generator mode, Bits[1:0]		N-shot mode, Bits[2:0]			SPI SYSREF request	0x00
0x0404	SYSREF_IN receiver control	Reserved					SYSREF IN receiver power-down	Single-ended source negative input (CMOS mode)	SYSREF differential receiver enable	0x04

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
Power-Down Control										
0x0500	Power-down control enable	Reserved			Bias generation power-down disable or power-down	PLL2 power-down enable	PLL1 power-down enable	Clock distribution power-down enable	Chip power-down enable	0x10
0x0501	Output channel power down enable	Channel 7 power-down	Channel 6 power-down	Channel 5 power-down	Channel 4 power-down	Channel 3 power-down	Channel 2 power-down	Channel 1 power-down	Channel 0 power-down	0x00
0x0502		Reserved		Channel 13 power-down	Channel 12 power-down	Channel 11 power-down	Channel 10 power-down	Channel 9 power-down	Channel 8 power-down	0x00
0x0503	LDO regulator enable	Channel 7 LDO enable	Channel 6 LDO enable	Channel 5 LDO enable	Channel 4 LDO enable	Channel 3 LDO enable	Channel 2 LDO enable	Channel 1 LDO enable	Channel 0 LDO enable	0xFF
0x0504		PLL2 LDO enable	PLL1 LDO enable	Channel 13 LDO enable	Channel 12 LDO enable	Channel 11 LDO enable	Channel 10 LDO enable	Channel 9 LDO enable	Channel 8 LDO enable	0xFF
Status and Status Readback[5]										
0x0505	Status control signals	Status Monitor 0 Control, Bits[7:0]								0x00
0x0506		Status Monitor 1 Control, Bits[7:0]								0x00
0x0507	Status pin enable and status divider enable	Reserved				STATUS1 pin output enable	STATUS0 pin output enable	STATUS0 divider enable	STATUS1 divider enable	0x00
0x0508	Status Readback 0	PLL2 feedback status	PLL1 feedback status	VCXO status	Both REFA/REFB missing	REFB status	REFA status	PLL2 locked status	PLL1 locked status	0x00
0x0509	Status Readback 1	Reserved				Holdover active status	Selected reference	Fast lock in progress	VCO calibration busy status	0x00

[1] The soft reset bits (Bit 0 and Bit 7) are logically AND gated internally; therefore, set or clear both bits together.
[2] The LSB first bits (Bit 1 and Bit 6) are logically AND gated internally; therefore, set or clear both bits together.
[3] The address ascension bits (Bit 2 and Bit 5) are logically AND gated internally; therefore, set or clear both bits together.
[4] The SDO active bits (Bit 3 and Bit 4) are logically AND gated internally; therefore, set or clear both bits together.
[5] Register 0x0505, Register 0x0506, and Register 0x0507 are control status pins as notated by bit names 0x0505 (Status 0) and 0x0506 (Status 1). Register 0x0508 and Register 0x0509 are for readback via SPI/I^{2}C.

CONTROL REGISTER MAP BIT DESCRIPTIONS

SERIAL CONTROL PORT CONFIGURATION (REGISTER 0x0000 TO REGISTER 0x0001)

Table 37. SPI Configuration A (Register 0x0000)

Bits	Bit Name	Description
7	Soft reset (SPI only)	Device reset.
6	LSB first (SPI only)	Bit order for SPI port. This bit has no effect in I^2C mode. 1 = least significant bit first. 0 (default) = most significant bit first.
5	Address ascension (SPI only)	This bit controls whether the register address is automatically incremented during a multibyte transfer. This bit has no effect in I^2C mode. 1 = register addresses are automatically incremented in multibyte transfers. 0 (default) = register addresses are automatically decremented in multibyte transfers.
4	SDO active (SPI only)	Enables SPI port SDO pin. This bit has no effect in I^2C mode. 1 = 4-wire mode (SDO pin enabled). 0 (default) = 3-wire mode.
[3:0]		These bits are mirrors of Bits[7:4] of this register. However, each pair of the following corresponding bits are logically AND gated internally; therefore, set the bits to Logic 1 or Logic 0 together. Bit 3 corresponds to Bit 4. Bit 2 corresponds to Bit 5. Bit 1 corresponds to Bit 6. Bit 0 corresponds to Bit 7.

Table 38. SPI Configuration B (Register 0x0001)

Bits	Bit Name	Description
[7:6]	Reserved	Reserved.
5	Read buffer register	For buffered registers, this bit controls whether the value read from the serial port is from the actual (active) registers or the buffered copy. 1 = reads buffered values that take effect on the next assertion of IO_UPDATE. 0 (default) = reads values currently applied to the internal logic of the device.
[4:3]	Reserved	Reserved.
2	Reset sans regmap	This bit resets the device while maintaining the current register settings. 1 = resets the device. 0 (default) = no action.
[1:0]	Reserved	Reserved.

CLOCK PART FAMILY ID (REGISTER 0x0003 TO REGISTER 0x0006)

Table 39. Clock Part Family ID

Address	Bits	Bit Name	Description
0x0003	[7:4]	Reserved	Reserved.
	[3:0]	Chip type, Bits[3:0]	The Analog Devices unified SPI protocol reserves this read only register location for identifying the type of device. The default value of 0x05 identifies the AD9528 as a clock IC.
0x0004	[7:4]	Clock part serial ID, Bits[3:0]	The Analog Devices unified SPI protocol reserves this read only register location as the lower four bits of the clock part serial ID that, along with Register 0x0005, uniquely identifies the AD9528 within the Analog Devices clock chip family. No other Analog Devices chip that adheres to the Analog Devices unified SPI has these values for Register 0x0003, Register 0x0004, and Register 0x0005. The clock part serial ID is 0x00F; for these four bits it is 0xF.
	[3:0]	Reserved	Default = 0xF.
0x0005	[7:0]	Clock part serial ID, Bits[11:4]	The Analog Devices unified SPI protocol reserves this read only register location as the upper eight bits of the clock part serial ID that, along with Register 0x0004, uniquely identifies the AD9528 within the Analog Devices clock chip family. No other Analog Devices chip that adheres to the Analog Devices unified SPI has these values for Register 0x0003, Register 0x0004, and Register 0x0005. Default: 0x00.
0x0006	[7:0]	Part versions, Bits[7:0]	The Analog Devices unified SPI protocol reserves this read only register location for identifying the die revision. Default = 0x03.

SPI VERSION (REGISTER 0x000B)

Table 40. SPI Version

Bits	Bit Name	Description
[7:0]	SPI version, Bits[7:0]	The Analog Devices unified SPI protocol reserves this read only register location for identifying the version of the unified SPI protocol. Default = 0x00.

VENDOR ID (REGISTER 0x000C TO REGISTER 0x000D)

Table 41. Vendor ID

Address	Bits	Bit Name	Description
0x000C	[7:0]	Vendor ID, Bits[7:0]	The Analog Devices unified SPI protocol reserves this read only register location for identifying Analog Devices as the chip vendor of this device. All Analog Devices devices adhering to the unified serial port specification have the same value in this register. Default = 0x56.
0x000D	[7:0]	Vendor ID, Bits[15:8]	The Analog Devices unified SPI protocol reserves this read only register location for identifying Analog Devices as the chip vendor of this device. All Analog Devices devices adhering to the unified serial port specification have the same value in this register. Default = 0x04.

IO_UPDATE (REGISTER 0x000F)

Table 42. IO_UPDATE

Bits	Bit Name	Description
[7:1]	Reserved	Reserved. Default = 0000000b.
0	IO_UPDATE	Writing a 1 to this bit transfers the data in the serial input/output buffer registers to the internal control registers of the device. This is an autoclearing bit.

PLL1 CONTROL (REGISTER 0x0100 TO REGISTER 0x010B)

Table 43. PLL1 REFA Divider (R_A) and REFB Divider (R_B) Control

Address	Bits	Bit Name	Description
0x0100	[7:0]	10-bit REFA (R_A) divider	10-bit REFA divider, Bits[7:0] (LSB). Divide by 1 to divide by 1023. 0000000000, 0000000001 = divide by 1.
0x0101	[1:0]		10-bit REFA divider, Bits[9:8] (MSB).
0x0102	[7:0]	10-bit REFB (R_B) divider	10-bit REFB divider, Bits[7:0] (LSB). Divide by 1 to divide by 1023. 0000000000, 0000000001 = divide by 1.
0x0103	[1:0]		10-bit REFB divider, Bits[9:8] (MSB).

Table 44. PLL1 Feedback Divider (N1)

Address	Bits	Bit Name	Description
0x0104	[7:0]	10-bit N1 divider	10-bit feedback divider, Bits[7:0] (LSB). Divide by 1 to divide by 1023. 0000000000, 0000000001 = divide by 1.
0x0105	[1:0]		10-bit feedback divider, Bits[9:8] (MSB).

Table 45. PLL1 Charge Pump Control

Address	Bits	Bit Name	Description
0x0106	7	Force holdover	Tristates the PLL1 charge pump. 0 = normal operation. 1 = forces holdover.
	[6:0]	PLL1 charge pump current (µA), Bits[6:0]	These bits set the magnitude of the PLL1 charge pump current. Granularity is ~0.5 µA with a full-scale magnitude of ~63.5 µA.
0x0107	[7:6]	Reserved	Reserved.
	5	Disable holdover	Disable automatic holdover. 0 = automatic holdover enabled. 1 = automatic holdover disabled.
	[4:2]	Reserved	Reserved.
	[1:0]	Charge pump mode, Bits[1:0]	Controls the mode of the PLL1 charge pump. 00 = tristate (default). 01 = pump down. 10 = pump up. 11 = normal.

Table 46. PLL1 Input Receiver Control

Address	Bits	Bit Name	Description
0x0108	7	Frequency detector power-down enable	1 = enabled. 0 = disabled (default).
	6	REFB differential receiver enable	1 = differential receiver mode. 0 = single-ended receiver mode (also depends on Register 0x0109, Bit 1) (default).
	5	REFA differential receiver enable	1 = differential receiver mode. 0 = single-ended receiver mode (also depends on Register 0x0109, Bit 0) (default).
	4	REFB input receiver enable	REFB receiver power-down control mode. 1 = enable REFB receiver. 0 = power-down (default).
	3	REFA input receiver enable	REFA receiver power-down control mode. 1 = enable REFA receiver. 0 = power-down (default).
	2	VCXO receiver power-down enable	Enables control over power-down of the VCXO receivers. 1 = power-down control enabled. 0 = both receivers enabled (default).
	1	VCXO single-ended receiver mode enable CMOS mode	Selects which single-ended input pin is enabled when in the single-ended receiver mode (Register 0x0108, Bit 0 = 0). 1 = negative receiver from VCXO input ($\overline{\text{VCXO\_IN}}$ pin) selected. 0 = positive receiver from VCXO input (VCXO_IN pin) selected (default).
	0	VCXO differential receiver enable	1 = differential receiver mode. 0 = single-ended receiver mode (default).
0x0109	[7:6]	Reserved	Reserved.
	5	N1 feedback divider reset	Puts divider in reset. 1 = Divider held in reset. 0 = divider normal operation.
	4	REFB divider (R_B) reset	Puts divider in reset. 1 = Divider held in reset. 0 = divider normal operation.
	3	REFA divider (R_A) reset	Puts divider in reset. 1 = Divider held in reset. 0 = divider normal operation.
	2	PLL1 Feedback Divider Source	Selects the input source to the PLL1 feedback divider. 1 = selects VCXO as the input to the PLL1 feedback divider. 0 = selects the PLL2 feedback divider output as the input to the PLL1 feedback divider.
	1	$\overline{\text{REFB}}$ single-ended negative pin enable (CMOS mode)	Selects which single-ended input pin is enabled when in single-ended receiver mode (also depends on Register 0x0108, Bit 6 = 0). 1 = $\overline{\text{REFB}}$ pin enabled. 0 = REFB pin enabled.
	0	$\overline{\text{REFA}}$ single-ended negative pin mode enable (CMOS mode)	Selects which single-ended input pin is enabled when in single-ended receiver mode (also depends on Register 0x0108, Bit 5 = 0). 1 = $\overline{\text{REFA}}$ pin enabled. 0 = REFA pin enabled.

Address	Bits	Bit Name	Description
0x010A	[7:4]	Reserved	Reserved.
	3	Holdover mode	High permits the VCXO_CTRL control voltage to be forced to midsupply when the feedback or input clocks fail. Low tristates the charge pump output. 1 = VCXO_CTRL control voltage goes to VCC/2. 0 = VCXO_CTRL control voltage tracks the tristated (high impedance) charge pump (through the buffer).
	[2:0]	Reference selection mode, Bits[2:0]	Programs the REFA, REFB mode selection (default = 000).

REF_SEL Pin	Bit 2	Bit 1	Bit 0	Description
X[1]	0	0	0	Nonrevertive: stay on REFB.
X[1]	0	0	1	Revert to REFA.
X[1]	0	1	0	Select REFA.
X[1]	0	1	1	Select REFB.
0	1	X[1]	X[1]	REF_SEL pin = 0 (low): REFA.
1	1	X[1]	X[1]	REF_SEL pin = 1 (high): REFB.

[1] X means don't care.

Table 47. PLL Fast Lock (Register 0x010B)

Bits	Bit Name	Description
7	PLL1 fast lock enable	Enables PLL1 fast lock operation.
[6:0]	Fast lock charge pump current (µA), Bits[6:0]	These bits set the magnitude of the PLL1 charge pump current. Granularity is ~0.5 µA with a full-scale magnitude of ~63.5 µA.

PLL2 (REGISTER 0x0200 TO REGISTER 0x0209)

Table 48. PLL2 Charge Pump Control (Register 0x0200)

Bits	Bit Name	Description
[7:0]	PLL2 CP current (µA), Bits[7:0]	These bits set the magnitude of the PLL2 charge pump current. Granularity is ~3.5 µA with a full-scale magnitude of ~900 µA.

Table 49. PLL2 Feedback VCO CAL Divider Control (Register 0x0201)

Bits	Bit Name	Description
[7:6]	A divider, Bits[1:0]	A divider word
[5:0]	B divider, Bits[5:0]	B divider word

Feedback Divider Constraints		
A Divider (Bits[7:6])	**B Divider (Bits[5:0])**	**Allowed N Division (4 × B + A)**
A = 0 or A = 1	B = 4	N = 16 to 255
A = 0 to A = 2	B = 5	
A = 0 to A = 2	B = 6	
A = 0 to A = 3	B ≥ 7	

Table 50. PLL2 Control (Register 0x0202)

Bits	Bit Name	Description
7	Lock detect power-down enable	Controls power-down of the PLL2 lock detector. 1 = lock detector powered down. 0 = lock detector active.
6	Reserved	Default = 0; value must remain 0.
5	Frequency doubler enable	Enables doubling of the PLL2 reference input frequency. 1 = enabled. 0 = disabled.

Bits	Bit Name	Description
[4:2]	Reserved	Reserved
[1:0]	PLL2 charge pump mode	Controls the mode of the PLL2 charge pump. 00 = tristate. 01 = pump down. 10 = pump up. 11 (default) = normal.

Table 51. PLL2 VCO Control (Register 0x0203)

Bits	Bit Name	Description
[7:5]	Reserved	Reserved.
4	Doubler and R1 divider path enable	0 (default) = bypasses doubler and R1 divider path to PLL2 frequency detector. 1 = enables doubler and R1 divider path.
3	Reset VCO calibration dividers	0 (default) = normal operation. 1 = resets A and B dividers.
2	Treat reference as valid	0 (default) = uses the PLL1 VCXO indicator to determine when the reference clock to the PLL2 is valid. 1 = treats the reference clock as valid even if PLL1 does not consider it to be valid.
1	Force VCO to midpoint frequency	Selects VCO control voltage functionality. 0 (default) = normal VCO operation. 1 = forces VCO control voltage to midscale.
0	Manual VCO calibrate (not autoclearing)	1 = initiates VCO calibration (this is not an autoclearing bit). 0 = resets the VCO calibration.

Table 52. PLL2 RF VCO Divider (M1) (Register 0x0204)

Bits	Bit Name	Description			
[7:6]	Reserved	Reserved.			
5	PFD reference edge select	1 = falling edge. 0 = rising edge.			
4	PFD feedback edge select	1 = falling edge. 0 = rising edge.			
3	RF VCO divider (M1) power-down	1 = powers down the M1 divider. 0 = normal operation.			
[2:0]	RF VCO divider (M1), Bits[2:0]	**Bit 2**	**Bit 1**	**Bit 0**	**Divider Value**
		0	1	1	Divide by 3.
		1	0	0	Divide by 4.
		1	0	1	Divide by 5.

Table 53. PLL2 Loop Filter Control

Address	Bits	Bit Name	Description			
0x0205	[7:6]	R_{POLE2} (Ω), Bits[1:0]	**Bit 7**	**Bit 6**	**R_{POLE2} (Ω)**	
			0	0	900	
			0	1	450	
			1	0	300	
			1	1	225	
	[5:3]	R_{ZERO} (Ω), Bits[1:0]	**Bit 5**	**Bit 4**	**Bit 3**	**R_{ZERO} (Ω)**
			0	0	0	3250
			0	0	1	2750
			0	1	0	2250
			0	1	1	2100
			1	0	0	3000
			1	0	1	2500
			1	1	0	2000
			1	1	1	1850
	[2:0]	C_{POLE1} (pF), Bits[1:0]	**Bit 2**	**Bit 1**	**Bit 0**	**C_{POLE1} (pF)**
			0	0	0	0
			0	0	1	8
			0	1	0	16
			0	1	1	24
			1	0	0	24
			1	0	1	32
			1	1	0	40
			1	1	1	48
0x0206	[7:1]	Reserved	Reserved.			
	0	Bypass internal R_{ZERO} resistor	Bypasses the internal R_{ZERO} resistor (R_{ZERO} = 0 Ω). Requires the use of a series external zero resistor. This bit is the MSB of the loop filter control register (Register 0x0205 and Register 0x0206). 1 = internal R_{ZERO} bypassed. 0 = internal R_{ZERO} used.			

Table 54. PLL2 Input Divider (R1) (Register 0x0207)

Bits	Bit Name	Description
[7:5]	Reserved	Reserved.
[4:0]	5-bit R1 divider	Divide by 1 to divide by 31. 00000, 00001 = divide by 1.

Table 55. PLL2 Feedback Divider (N2) (Register 0x0208)

Bits	Bit Name	Description
[7:0]	8-bit N2 divider	Division = Channel Divider Bits[7:0] + 1. For example, [7:0] = 0 is divided by 1, [7:0] = 1 is divided by 2…[7:0] = 255 is divided by 256.

Table 56. PLL2 R1 Reference Divider (Register 0x0208 and Register 0x0209)

Address	Bits	Bit Name	Description
0x0209	7	Reserved	Reserved.
	6	N2 divider power-down	0: (default) normal operation. 1: N2 divider powered down
	[5:0]	N2 phase, Bits[5:0]	Divider initial phase after a sync is asserted relative to the divider input clock (from the VCO divider output). LSB = ½ of a period of the divider input clock. Phase 0 = no phase offset. Phase 1 = ½ period offset. … Phase 63 = 31.5 period offset.

CLOCK DISTRIBUTION (REGISTER 0x300 TO REGISTER 0x0329)

Table 57. Channel 0 to Channel 13 Control (This Same Map Applies to All 14 Channels)

Address	Bits	Bit Name	Description			
0x0300, 0x0303, 0x0306, 0x0309, 0x030C, 0x030F, 0x0312, 0x0315, 0x0318, 0x031B, 0x031E, 0x0321, 0x0324, 0x0327	[7:5]	Channel control, Bits[2:0]	Controls which signal source is selected by the output driver.			
			Bit 7	**Bit 6**	**Bit 5**	**Output Signal Source**
			0	0	0	PLL2/divider output.
			0	0	1	PLL1/VCXO output.
			0	1	0	SYSREF (retimed by PLL2 output).
			0	1	1	SYSREF (retimed by PLL1 output).
			1	0	0	PLL2/divider output.
			1	0	1	Inverted PLL1/VCXO output.
			1	1	0	SYSREF (retimed by PLL2 output).
			1	1	1	SYSREF (retimed by inverted PLL1 output).
	4	Fine analog delay enable	1 = enables fine delay for the corresponding channel. 600 ps insertion delay. 0 (default) = disables fine analog delay for the corresponding channel.			
	[3:0]	Fine analog delay, Bits[3:0]	15 fine delay steps. Step size = 31 ps.			
0x0301, 0x0304, 0x0307, 0x030A, 0x030D, 0x0310, 0x0313, 0x0316, 0x0319, 0x031C, 0x031F, 0x0322, 0x0325, 0x0328	[7:6]	Output format, Bits[1:0]	Determines the output logic to be applied.			
			Bit 7	**Bit 6**	**Output Logic Type**	
			0	0	LVDS.	
			0	1	LVDS (boost mode).	
			1	X	HSTL.	
	[5:0]	Coarse digital delay, Bits[5:0]	Divider initial phase after a sync is asserted relative to the divider input clock (from the VCO divider output). LSB = ½ of a period of the divider input clock. Phase = 0: no phase offset. Phase = 1: ½ period offset … Phase = 63: 31.5 period offset.			
0x0302, 0x0305, 0x0308, 0x030B, 0x030E, 0x031A, 0x0314, 0x0317, 0x031A, 0x031D, 0x0320, 0x0323, 0x0326, 0x0329	[7:0]	Divide ratio, Bits[7:0] (LSB)	Division = Channel divider Bits[7:0] + 1. For example, [7:0] = 0 is divided by 1, [7:0] = 1 is divided by 2…[7:0] = 255 is divided by 256. 8-bit channel divider.			

Table 58. Distribution Sync

Address	Bits	Bit Name	Description
0x032A	[7:1]	Reserved	Reserved.
	0	SYNC outputs	Issues SYNC on transition of bit 0 from 1 to 0.

Table 59. Ignore SYNC Enable

Address	Bits	Bit Name	Description
0x032B	7	Channel 7 ignore sync	0 = Channel 7 synchronizes to sync command. 1 = Channel 7 ignores sync command.
	6	Channel 6 ignore sync	0 = Channel 6 synchronizes to sync command. 1 = Channel 6 ignores sync command.
	5	Channel 5 ignore sync	0 = Channel 5 synchronizes to sync command. 1 = Channel 5 ignores sync command.
	4	Channel 4 ignore sync	0 = Channel 4 synchronizes to sync command. 1 = Channel 4 ignores sync command.
	3	Channel 3 ignore sync	0 = Channel 3 synchronizes to sync command. 1 = Channel 3 ignores sync command.
	2	Channel 2 ignore sync	0 = Channel 2 synchronizes to sync command. 1 = Channel 2 ignores sync command.
	1	Channel 1 ignore sync	0 = Channel 1 synchronizes to sync command. 1 = Channel 1 ignores sync command.
	0	Channel 0 ignore sync	0 = Channel 0 synchronizes to sync command. 1 = Channel 0 ignores sync command.
0x032C	7	Reserved	Reserved.
	6	PLL2 feedback N2 divider ignore sync	0 = PLL2 N2 divider synchronizes to sync command 1 = PLL2 N2 divider ignores sync command
	5	Channel 13 ignore sync	0 = Channel 13 synchronizes to sync command 1 = Channel 13 ignores sync command
	4	Channel 12 ignore sync	0 = Channel 12 synchronizes to sync command 1 = Channel 12 ignores sync command
	3	Channel 11 ignore sync	0 = Channel 11 synchronizes to sync command 1 = Channel 11 ignores sync command
	2	Channel 10 ignore sync	0 = Channel 10 synchronizes to sync command 1 = Channel 10 ignores sync command
	1	Channel 9 ignore sync	0 = Channel 9 synchronizes to sync command 1 = Channel 9 ignores sync command
	0	Channel 8 ignore sync	0 = Channel 8 synchronizes to sync command 1 = Channel 8 ignores sync command

Table 60. SYSREF Bypass Resample Control

Address	Bits	Bit Name	Description
0x032D	7	Channel 6 bypass SYSREF resample	0 = not bypassed. 1 = Channel 6 bypass SYSREF resample.
	6	Channel 5 bypass SYSREF resample	0 = not bypassed. 1 = Channel 5 bypass SYSREF resample.
	5	Channel 4 bypass SYSREF resample	0 = not bypassed. 1 = Channel 4 bypass SYSREF resample.
	4	Channel 3 bypass SYSREF resample	0 = not bypassed. 1 = Channel 3 bypass SYSREF resample.
	3	Channel 2 bypass SYSREF resample	0 = not bypassed. 1 = Channel 2 bypass SYSREF resample.
	2	Channel 1 bypass SYSREF resample	0 = not bypassed. 1 = Channel 1 bypass SYSREF resample.
	1	Channel 0 bypass SYSREF resample	0 = not bypassed. 1 = Channel 0 bypass SYSREF resample.
	0	Enable VCXO receiver path to distribution	0 = path disabled. 1 = enables path.
0x032E	7	Reserved	Reserved.
	6	Channel 13 bypass SYSREF resample	0 = not bypassed. 1 = Channel 13 bypass SYSREF resample.
	5	Channel 12 bypass SYSREF resample	0 = not bypassed. 1 = Channel 12 bypass SYSREF resample.
	4	Channel 11 bypass SYSREF resample	0 = not bypassed. 1 = Channel 11 bypass SYSREF resample.
	3	Channel 10 bypass SYSREF resample	0 = not bypassed. 1 = Channel 10 bypass SYSREF resample.
	2	Channel 9 bypass SYSREF resample	0 = not bypassed. 1 = Channel 9 bypass SYSREF resample.
	1	Channel 8 bypass SYSREF resample	0 = not bypassed. 1 = Channel 8 bypass SYSREF resample.
	0	Channel 7 bypass SYSREF resample	0 = not bypassed. 1 = Channel 7 bypass SYSREF resample.

Table 61. SYSREF Pattern Generator K Divider

Address	Bits	Bit Name	Description
0x0400, 0x0401	[7:0], [15:8]	K divider	The 16-bit K divider divides the input clock to the SYSREF pattern generator to program the SYSREF pulse width. Bits[7:0] are the LSB byte, and Bits[15:8] are the MSB byte.

Table 62. SYSREF Control

Address	Bits	Bit Name	Description
0x0402	7	SYSREF request method	SYSREF request method 0 = SPI controlled 1 = Pin controlled
	[6:5]	SYSREF pattern generator trigger control, Bits[1:0]	SYSREF pattern generator trigger control 0x: level sensitive, active high 10: edge sensitive, rising edge 11: edge sensitive, falling edge
	4	SYSREF pattern generator clock source	0 = PLL2 feedback divider 1 = PLL1 out
	3	Resample clock source for external SYSREF	0 = device clock 1 = PLL1 out
	[2:1]	SYSREF test mode, Bits[1:0]	SYSREF test mode 00 = GND 01 = VDD 1x = counter output clock
	0	SYSREF reset	SYSREF reset
0x0403	[7:6]	SYSREF source, Bits[1:0]	SYSREF source 00 = external 01 = external resampled 10 = internal
	[5:4]	SYSREF pattern generator mode, Bits[1:0]	Pattern mode 00 = N-shot 01 = continuous 10 = PRBS 11 = stop
	[3:1]	N-shot mode, Bits[1:0]	N-shot mode 001 = 1 pulse 010 = 2 pulses 011 = 4 pulses 100 = 6 pulses 101 = 8 pulses Others = 1 pulse
	0	SPI SYSREF request	SPI SYSREF request In N-shot mode, the SYSREF pattern starts at the transition of this bit from 0 to 1 and bit automatically clears after the pattern completes In continuous or PRBS mode, SYSREF pattern starts at the transition of this bit from 0 to 1 and the bit stays set to 1 until user clears the bit; when the user clears the bit, the SYSREF pattern stops

Table 63. SYSREF_IN Receiver Control

Address	Bits	Bit Name	Description
0x0404	[7:3]	Reserved	Reserved.
	2	SYSREF IN receiver power-down	Enables control over power-down of the SYSREF input receivers. 1 = power-down control enabled (default). 0 = both receivers enabled.
	1	Single-ended source negative input (CMOS mode)	Selects which single-ended input pin is enabled when in the SYSREF single-ended receiver mode (Register 0x0404, Bit 0 = 0). 1 = negative receiver from SYSREF input ($\overline{\text{SYSREF\_IN}}$ pin) selected. 0 = positive receiver from SYSREF input ($\overline{\text{SYSREF\_IN}}$ pin) selected (default).
	0	SYSREF differential receiver enable	1 = differential receiver mode, single-ended receivers disabled. 0 = single-ended receiver mode (default).

POWER-DOWN CONTROL (REGISTER 0x0500 TO REGISTER 0x0504)

Table 64. Power-Down Control Enable

Address	Bits	Bit Name	Description
0x0500	[7:5]	Reserved	Reserved
	4	Bias generation power-down disable or power-down	0 = power-down 1 = normal operation
	3	PLL2 power-down enable	0 = normal operation 1 = power-down
	2	PLL1 power-down enable	0 = normal operation 1 = power-down
	1	Clock distribution power-down enable	0 = normal operation 1 = power-down
	0	Chip power-down enable	0 = normal operation 1 = power-down

Table 65. Output Channel Power-Down Control

Address	Bits	Bit Name	Description
0x0501	7	Channel 7 power-down	0 = normal operation 1 = Channel 7 power-down
	6	Channel 6 power-down	0 = normal operation 1 = Channel 6 power-down
	5	Channel 5 power-down	0 = normal operation 1 = Channel 5 power-down
	4	Channel 4 power-down	0 = normal operation 1 = Channel 4 power-down
	3	Channel 3 power-down	0 = normal operation 1 = Channel 3 power-down
	2	Channel 2 power-down	0 = normal operation 1 = Channel 2 power-down
	1	Channel 1 power-down	0 = normal operation 1 = Channel 1 power-down
	0	Channel 0 power-down	0 = normal operation 1 = Channel 0 power-down
0x0502	[7:6]	Reserved	Reserved
	5	Channel 13 power-down	0 = normal operation 1 = Channel 13 power-down
	4	Channel 12 power-down	0 = normal operation 1 = Channel 12 power-down
	3	Channel 11 power-down	0 = normal operation 1 = Channel 11 power-down
	2	Channel 10 power-down	0 = normal operation 1 = Channel 10 power-down
	1	Channel 9 power-down	0 = normal operation 1 = Channel 9 power-down
	0	Channel 8 power-down	0 = normal operation 1 = Channel 8 power-down

Table 66. LDO Regulator Enable

Address	Bits	Bit Name	Description
0x0503	7	Channel 7 LDO enable	0: Channel 7 LDO power down 1: normal operation
	6	Channel 6 LDO enable	0: Channel 6 LDO power down 1: normal operation
	5	Channel 5 LDO enable	0: Channel 5 LDO power down 1: normal operation
	4	Channel 4 LDO enable	0: Channel 4 LDO power down 1: normal operation
	3	Channel 3 LDO enable	0: Channel 3 LDO power down 1: normal operation
	2	Channel 2 LDO enable	0: Channel 2 LDO power down 1: normal operation
	1	Channel 1 LDO enable	0: Channel 1 LDO power down 1: normal operation
	0	Channel 0 LDO enable	0: Channel 0 LDO power down 1: normal operation
0x0504	7	PLL2 LDO enable	0: PLL2 LDO power down 1: normal operation
	6	PLL1 LDO enable	0: PLL1 LDO power down 1: normal operation
	5	Channel 13 LDO enable	0: Channel 13 LDO power down 1: normal operation
	4	Channel 12 LDO enable	0: Channel 12 LDO power down 1: normal operation
	3	Channel 11 LDO enable	0: Channel 11 LDO power down 1: normal operation
	2	Channel 10 LDO enable	0: Channel 10 LDO power down 1: normal operation
	1	Channel 9 LDO enable	0: Channel 9 LDO power down 1: normal operation
	0	Channel 8 LDO enable	0: Channel 8 LDO power down 1: normal operation

STATUS CONTROL (REGISTER 0x0505 TO REGISTER 0x0509)

Table 67. Status Control Signals

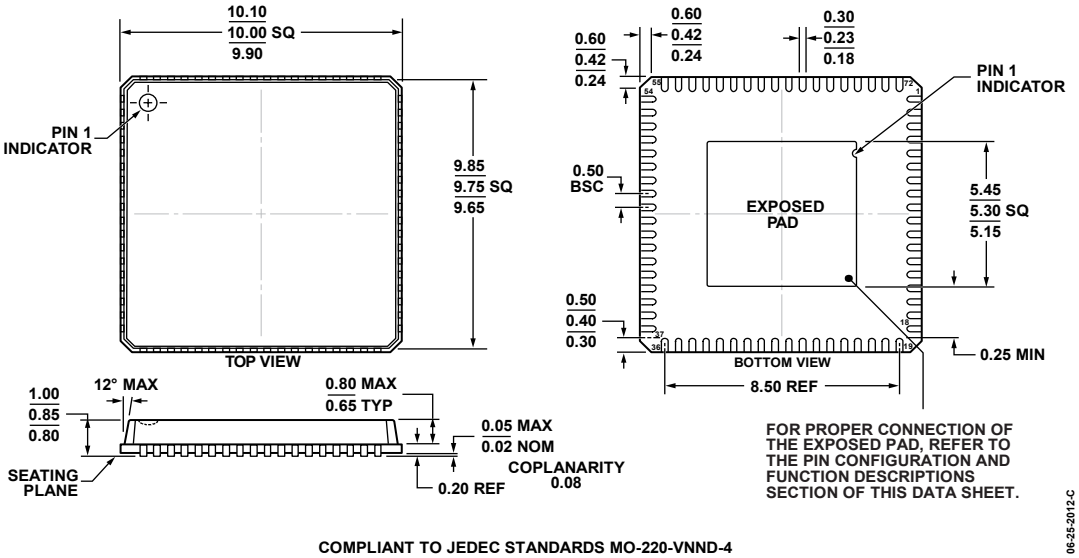
Address	Bits	Bit Name	Description						
0x0505	[7:0]	Status Monitor 0 control	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Mux Out**
			0	0	0	0	0	0	GND
			0	0	0	0	0	1	PLL1 and PLL2 locked
			0	0	0	0	1	0	PLL1 locked
			0	0	0	0	1	1	PLL2 locked
			0	0	0	1	0	0	Both references are missing (REFA and REFB)
			0	0	0	1	0	1	Both references are missing and PLL2 is locked
			0	0	0	1	1	0	REFB selected (applies only to auto select mode)
			0	0	0	1	1	1	REFA is correct
			0	0	1	0	0	0	REFB is correct
			0	0	1	0	0	1	PLL1 in Holdover
			0	0	1	0	1	0	VCXO is correct
			0	0	1	0	1	1	PLL1 feedback is correct
			0	0	1	1	0	0	PLL2 feedback clock is correct
			0	0	1	1	0	1	Fast lock in progress
			0	0	1	1	1	0	REFA and REFB are correct
			0	0	1	1	1	1	All clocks are correct
			0	1	0	0	0	0	PLL1 feedback divide by 2
			0	1	0	0	0	1	PLL1 PFD down divide by 2
			0	1	0	0	1	0	PLL1 REF divide by 2
			0	1	0	0	1	1	PLL1 PFD up divide by 2
			0	1	0	1	0	0	GND
			0	1	0	1	0	1	GND
			0	1	0	1	1	0	GND
			0	1	0	1	1	1	GND
			Note that all bit combinations after 010111 are reserved						
0x0506	[7:0]	Status Monitor 1 control	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Mux Out**
			0	0	0	0	0	0	GND
			0	0	0	0	0	1	PLL1 and PLL2 locked
			0	0	0	0	1	0	PLL1 locked
			0	0	0	0	1	1	PLL2 locked
			0	0	0	1	0	0	Both references are missing (REFA and REFB)
			0	0	0	1	0	1	Both references are missing and PLL2 is locked
			0	0	0	1	1	0	REFB selected (applies only to auto select mode)
			0	0	0	1	1	1	REFA is correct
			0	0	1	0	0	0	REFB is correct
			0	0	1	0	0	1	PLL1 in Holdover
			0	0	1	0	1	0	VCXO is correct
			0	0	1	0	1	1	PLL1 feedback is correct
			0	0	1	1	0	0	PLL2 feedback clock is correct
			0	0	1	1	0	1	Fast Lock in Progress
			0	0	1	1	1	0	REFA and REFB are correct
			0	0	1	1	1	1	All clocks are correct
			0	1	0	0	0	0	GND
			0	1	0	0	0	1	GND
			0	1	0	0	1	0	GND
			0	1	0	0	1	1	GND
			0	1	0	1	0	0	PLL2 feedback divide by 2
			0	1	0	1	0	1	PLL2 PFD down divide by 2

Address	Bits	Bit Name	Description
			0 1 0 1 1 0 PLL2 REF divide by 2 0 1 0 1 1 1 PLL2 PFD up divide by 2 Note that all bit combinations after 010111 are reserved.
0x0507	[7:4]	Reserved	Reserved.
	3	STATUS1 pin Output enable	Enables the status on the STATUS1 pin. 1: enable status output. 0: disable status output.
	2	STATUS0 pin Output enable	Enables the status on the STATUS0 pin. 1: enable status output. 0: disable status output.
	1	STATUS0 pin divider enable	Enables a divide by 4 on the STATUS0 pin, allowing dynamic signals to be viewed at a lower frequency (such as the PFD input clocks). Not to be used with dc states on the status pins, which occur when the settings of Register 0x0505, Bits[5:0] are in the range of 000000 to 001111. 1: enabled. 0: disabled.
	0	STATUS1 pin divider enable	Enables a divide by 4 on the STATUS1 pin, allowing dynamic signals to be viewed at a lower frequency (such as the PFD input clocks). Not to be used with dc states on the status pins, which occur when the settings of Register 0x0506, Bits[5:0] are in the range of 000000 to 001111. 1: enable. 0: disable.

Table 68. Readback Registers (Readback 0 and Readback 1)

Address	Bits	Bit Name	Description
0x0508	7	PLL2 feedback status	1 = correct. 0 = off/clocks are missing.
	6	PLL1 feedback status	1 = correct. 0 = off/clocks are missing.
	5	VCXO status	1 = correct. 0 = off/clocks are missing.
	4	Both REFA/REFB missing	1 = off/clocks are missing. 0 = correct.
	3	REFB status	1 = correct. 0 = off/clocks are missing.
	2	REFA status	1 = correct. 0 = off/clocks are missing.
	1	PLL2 locked status	1 = locked. 0 = unlocked.
	0	PLL1 locked status	1 = locked. 0 = unlocked.
0x0509	[7:4]	Reserved	Reserved.
	3	Holdover active status	1 = holdover is active (both references are missing). 0 = normal operation.
	2	Selected reference	Selected reference (applies only when the device automatically selects the reference; for example, not in manual control mode). 1 = REFB. 0 = REFA.
	1	Fast Lock in progress	1 = fast lock in progress. 0 = fast lock not in progress.
	0	VCO calibration busy status	1 = VCO calibration in progress. 0 = VCO calibration not in progress.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VNND-4

Figure 56. 72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
10 mm × 10 mm Body, Very Thin Quad
(CP-72-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9528BCPZ	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-6
AD9528BCPZ-REEL7	−40°C to +85°C	72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-72-6
AD9528/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

AD9528BCPZ AD9528BCPZ-REEL7