



## Dual or Quad Selectable Programmable Crystal Oscillator

### Output: LV-PECL



Product Number  
**SG-8503CA : X1G005011xxx00**  
**SG-8504CA : X1G005021xxx00**

# SG-8503CA / SG-8504CA

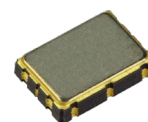
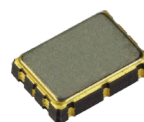
- Dual frequency Selectable: SG-8503CA, 7.0 × 5.0 × 1.5 mm (6 pins)
- Quad frequency Selectable: SG-8504CA, 7.0 × 5.0 × 1.5 mm (8 pins)
- Frequency range: 50 MHz to 800 MHz
- Supply voltage: 2.5 V to 3.3 V

#### Features

- User-specified two (FSEL) or four (FSEL0, FSEL1) startup frequencies
- High frequency fundamental tone crystal, Low jitter PLL technology
- Available field oscillator programmer "SG-Writer II"

#### Application

- OTN, BTS, Test Instrument



## Specifications (characteristics)

Item	Symbol	Specifications	Conditions / Remarks
Output frequency range	f <sub>o</sub>	50 MHz to 800 MHz	-
Supply voltage	V <sub>CC</sub>	2.5 V - 0.125 V to 3.3 V + 0.33 V	-
Storage temperature range	T <sub>stg</sub>	-55 °C to +125 °C	Store as bare product after packing
Operating temperature range	T <sub>use</sub>	-40 °C to +85 °C	-
Frequency tolerance *1	f <sub>tol</sub>	K : ±31.5 × 10 <sup>-6</sup> L : ±50 × 10 <sup>-6</sup>	Customized Product (Option)
Current consumption	I <sub>CC</sub>	90 mA Max.	OE Active, L <sub>ECL</sub> = 50 Ω
Disable current	I <sub>dis</sub>	40 mA Max. 70 mA Max.	OE Inactive, Output Standby: Hi-Z mode OE Inactive, Output Standby: Fix mode
Symmetry	SYM	45 % to 55 %	At outputs crossing point
Output voltage	V <sub>OH</sub> V <sub>OL</sub>	V <sub>CC</sub> - 1.025 V Min. V <sub>CC</sub> - 1.62 V Max.	DC characteristics
Output load condition	L <sub>ECL</sub>	50 Ω	Termination to V <sub>CC</sub> - 2.0 V
Input voltage	V <sub>IH</sub> V <sub>IL</sub>	70% V <sub>CC</sub> Min. 30% V <sub>CC</sub> Max.	SG-8503CA : OE, FSEL SG-8504CA : OE, FSEL0, FSEL1
Rise time / Fall time	t <sub>r</sub> / t <sub>f</sub>	400 ps Max.	Between 20% and 80% of (V <sub>OH</sub> - V <sub>OL</sub> )
Start-up time	t <sub>str</sub>	10 ms Max.	Time at minimum supply voltage to be 0 s
Setting time for frequency change	t <sub>SET1</sub>	1.5 ms Max.	SG-8503CA : From setting FSEL pin to output new frequency SG-8504CA : From setting FSEL0 / FSEL1 pin to output new frequency

\*1 Frequency tolerance includes initial frequency tolerance, temperature variation, supply voltage change, reflow drift and 10 years aging at +25 °C.

Product Name SG-8503 CA 156MHz 625MHz A P R L Z  
 (Standard form) ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨

① Model, ② Package type,

③ Frequency-0 (50 ~ 800 MHz), ④ Frequency-1 (50 ~ 800 MHz), ⑤ Internal crystal frequency, ⑥ Output enable pin Polarity,

⑦ Supply voltage/Output format, ⑧ Frequency tolerance/Operating temperature, ⑨ Output standby type

Product Name SG-8504 CA 156.2MHz nnnn A P R L Z  
 (Standard form) ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨

① Model, ② Package type,

③ Frequency-0 (50 ~ 800 MHz), ④ Parameter identifier, ⑤ Internal crystal frequency, ⑥ Output enable pin Polarity,

⑦ Supply voltage/Output format, ⑧ Frequency tolerance/Operating temperature, ⑨ Output standby type

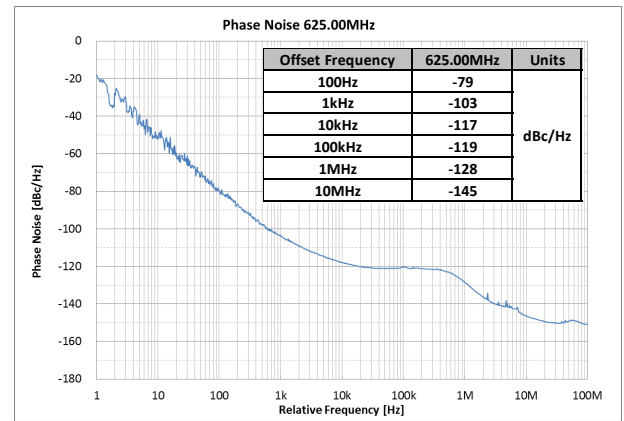
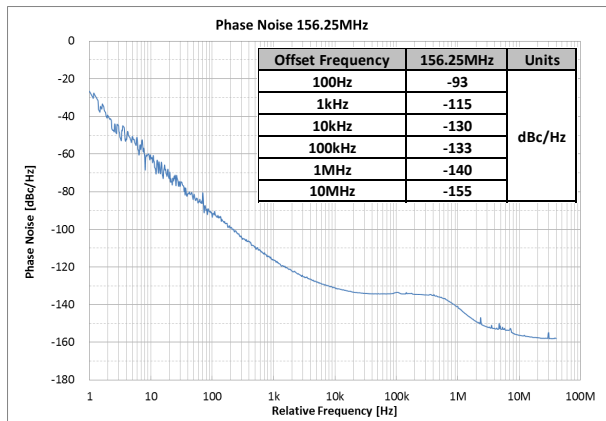
⑤ Internal crystal frequency	⑥ Output enable pin Polarity	⑦ Supply voltage/ Output format	⑧ Frequency tolerance/ Operating temperature	⑨ Output standby type
A 114.1444 MHz	P Active High Q Active Low	R 2.5 V ~ 3.3 V/LVPECL	K ±31.5 × 10 <sup>-6</sup> /-40 to +85 °C L ±50 × 10 <sup>-6</sup> /-40 to +85 °C	F Fix (OUT="L", OUTN="H") Z High-Z

## Phase Jitter

	Offset Frequency	100.00 MHz	125.00 MHz	156.25 MHz	250.00 MHz	312.50 MHz	500.00 MHz	625.00 MHz
Phase jitter *2 Typ.	12 kHz to 20 MHz	0.31 ps	0.30 ps	0.26 ps	0.26 ps	0.29 ps	0.28 ps	0.29 ps

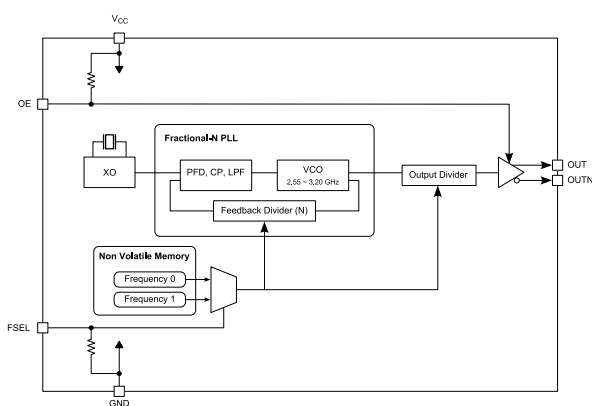
\*2 In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1 μF + 10 μF) between V<sub>CC</sub> and GND pin should be placed as close to the V<sub>CC</sub> pin as possible.

## Phase Noise

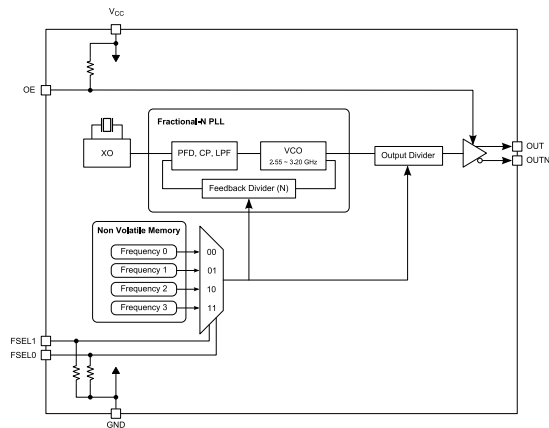


## Block diagram

SG-8503CA



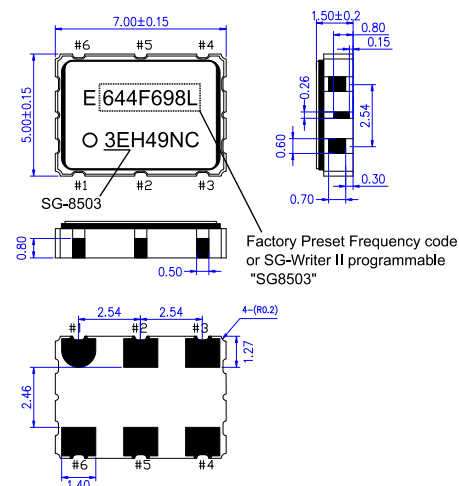
SG-8504CA



## External dimensions

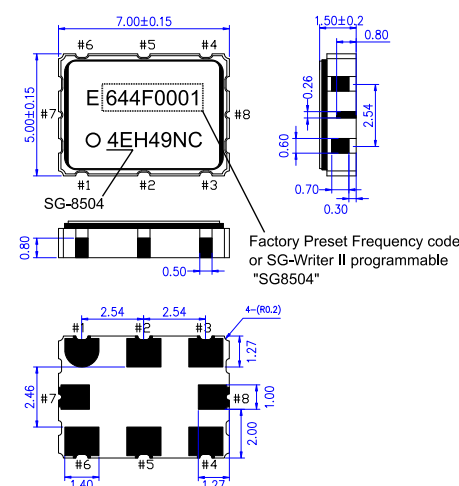
(Unit: mm)

SG-8503CA



Pin	Connection
1	OE
2	FSEL (L = Frequency-0, H = Frequency-1)
3	GND
4	OUT
5	OUTN
6	Vcc

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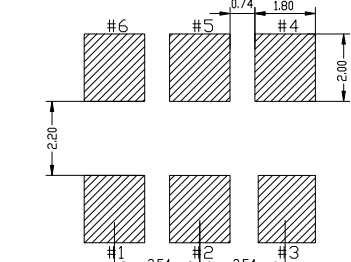


Pin	Connection	Pin	Connection
1	NC	5	OUTN
2	OE	6	Vcc
3	GND	7	FSEL0
4	OUT	8	FSEL1

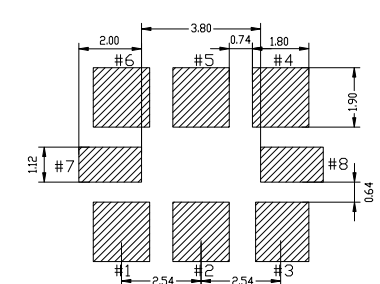
FSEL1, FSEL0	Output Frequency
LL	Frequency-0
LH	Frequency-1
HL	Frequency-2
HH	Frequency-3

## Footprint (Recommended)(Unit: mm)

SG-8503CA







SG-8504CA



In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1  $\mu$ F + 10  $\mu$ F) between Vcc and GND pin should be placed as close to the Vcc pin as possible.

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	► Complies with EU RoHS directive. *About the products without the Pb-free mark. Contains Pb in products exempted by EU RoHS directive. (Contains Pb in sealing glass, high melting temperature type solder or other.)
	► Designed for automotive general equipment.
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