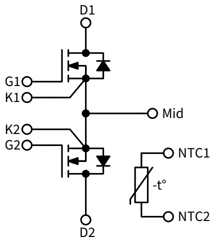
CLB650M17HM3, CLB650M17HM3T

1700 V, 650 A, Silicon Carbide, Common-Source Module

V_{DS}	1700 V
I_{DS}	650 A

Technical Features

- Low Inductance, Low Profile 62 mm Footprint
- High Junction Temperature (175 °C) Operation
- Implements Third Generation SiC MOSFET Technology
- Light Weight AlSiC Baseplate
- High Reliability Silicon Nitride Insulator



Typical Applications

- Solid State Circuit Breakers
- EV Battery Disconnect
- T-type Inverters
- Four-Quadrant Power Converters
- UPS and SMPS

System Benefits

- Lightweight, Compact Form Factor with 62 mm Compatible Baseplate Enables System Retrofit
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- High Reliability Material Selection

Maximum Parameters (Verified by Design)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source Voltage	V_{DS}			1700	V		
Gate-Source Voltage, Maximum Value	$V_{GS(max)}$	-8		+19	V	Transient	Note 1 Fig. 19
Gate-Source Voltage, Recommended	$V_{GS(op)}$		-4/+15		V	Static	Note 1 Fig. 19
DC Continuous Drain Current	I_D		916		A	V_{GS} = 15 V, T_C = 25 °C, T_{VJ} ≤ 175 °C	Notes 2, 3 Fig. 13
			694		A	V_{GS} = 15 V, T_C = 90 °C, T_{VJ} ≤ 175 °C	Notes 2, 3 Fig. 13
DC Source-Drain Current (Body Diode)	$I_{SD(BD)}$		593		A	V_{GS} = -4 V, T_C = 25 °C, T_{VJ} ≤ 175 °C	Notes 2, 3 Fig. 13
Pulsed Drain-Source Current	I_{DM}		2776		A	t_{Pmax} limited by T_{VJmax} V_{GS} = 15 V, T_C = 25 °C	Notes 2, 3 Fig. 13
Power Dissipation	P_D		2780		W	T_C = 25 °C, T_{VJ} ≤ 175 °C	Note 4 Fig. 14
Virtual Junction Temperature	$T_{VJ(op)}$	-40		175	°C		

Note (1): Recommended turn-on gate voltage is 15 V with ±5 % regulation tolerance
Note (2): Current limit calculated by $I_{D(max)} = \sqrt{(P_D/R_{DS(typ)}(T_{VJ(max)}, I_{D(max)}))}$
Note (3): Verified by design
Note (4): $P_D = (T_{VJ} - T_C)/R_{TH(JC,typ)}$

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MOSFET Characteristics (Per Position) (T_{VJ} = 25 °C Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1700			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6	V	V_{DS} = V_{GS}, I_D = 305 mA	
			2.0			V_{DS} = V_{GS}, I_D = 305 mA, T_{VJ} = 175 °C	
Zero Gate Voltage Drain Current	I_{DSS}		12	500	μA	V_{GS} = 0 V, V_{DS} = 1700 V	
Gate-Source Leakage Current	I_{GSS}		0.12	3.0	μA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		1.42	1.86	mΩ	V_{GS} = 15 V, I_D = 650 A	Fig. 2 Fig. 3
			3.04			V_{GS} = 15 V, I_D = 650 A, T_{VJ} = 175 °C	
Transconductance	g_{fs}		553		S	V_{DS} = 20 V, I_{DS} = 650 A	Fig. 4
			561			V_{DS} = 20 V, I_{DS} = 650 A, T_{VJ} = 175 °C	
Internal Gate Resistance	$R_{G(int)}$		0.62		Ω	f = 100 kHz	
Input Capacitance	C_{iss}		97.3		nF	V_{GS} = 0 V, V_{DS} = 1200 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
Output Capacitance	C_{oss}		2.3		nF		
Reverse Transfer Capacitance	C_{rss}		63		pF		
Gate to Source Charge	Q_{GS}		960		nC	V_{DS} = 1200 V, V_{GS} = -4 V/15 V I_D = 650 A Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		840		nC		
Total Gate Charge	Q_G		2988		nC		
FET Thermal Resistance, Junction to Case	$R_{th\ JC}$		0.054		°C/W		Fig. 11

Diode Characteristics (Per Position) (T_{VJ} = 25 °C Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Body Diode Forward Voltage	V_{SD}		5.4		V	V_{GS} = -4 V, I_{SD} = 650 A	Fig. 7
			4.7			V_{GS} = -4 V, I_{SD} = 650 A, T_{VJ} = 175 °C	

Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Package Resistance, M1	$R_{1\text{-}2}$		106.5		μΩ	T_C = 125 °C, Note 5
Package Resistance, M2	$R_{2\text{-}3}$		126.3		μΩ	T_C = 125 °C, Note 5
Stray Inductance	L_{Stray}		4.9		nH	Between Terminals 1 and 3
Case Temperature	T_C	-40		125	°C	
Weight	W		179		g	
Mounting Torque	M_S	3.0	4.5	5.0	N-m	CLB650M17HM3, Baseplate, M6 Bolts
		4.5		6.0		CLB650M17HM3T, Baseplate, M6 Bolts
		0.9	1.1	1.3		Power Terminals, M4 × 0.7 mm Bolts
Case Isolation Voltage	V_{isol}	4			kV	AC, 50 Hz, 1 min
Comparative Tracking Index	CTI	600				
Clearance Distance		9.43			mm	Terminal to Terminal
		12.70				Terminal to Baseplate
Creepage Distance		13.05				Terminal to Terminal
		15.30				Terminal to Baseplate

Note (5): Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance

Temperature Sensor (NTC) Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Resistance at 25 °C	R_{25}		4700		Ω	T_{NTC} = 25 °C
Tolerance of R_{25}			±1		%	
Beta Value for 25 °C to 85 °C	$B_{25/85}$		3435		K	
Beta Value for 0 °C to 100 °C	$B_{0/100}$		3399		K	
Tolerance of $B_{25/85}$			±1		%	
Maximum Power Dissipation	P_{25}		50		mW	

Steinhart & Hart Coefficients for NTC Resistance & NTC Temperature Computation (T in K)

$$\ln\left(\frac{R}{R_{25}}\right) = A + \frac{B}{T} + \frac{C}{T^2} + \frac{D}{T^3}$$

A	B	C	D
-1.289E+01	4.245E+03	-8.749E+04	-9.588E+06

$$\frac{1}{T} = A_1 + B_1 \ln\left(\frac{R}{R_{25}}\right) + C_1 \ln^2\left(\frac{R}{R_{25}}\right) + D_1 \ln^3\left(\frac{R}{R_{25}}\right)$$

A_1	B_1	C_1	D_1
3.354E-03	3.001E-04	5.085E-06	2.188E-07

Typical Performance

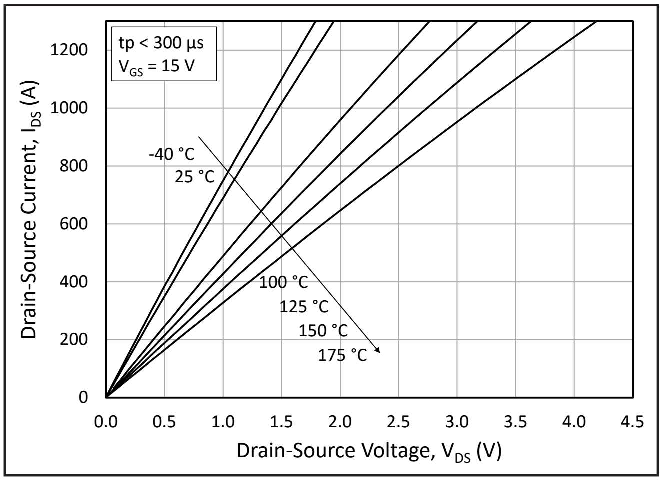


Figure 1. Output Characteristics for Various Junction Temperatures

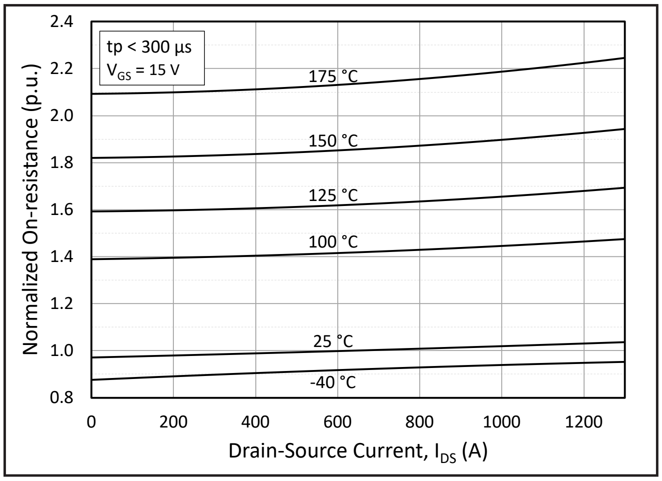


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

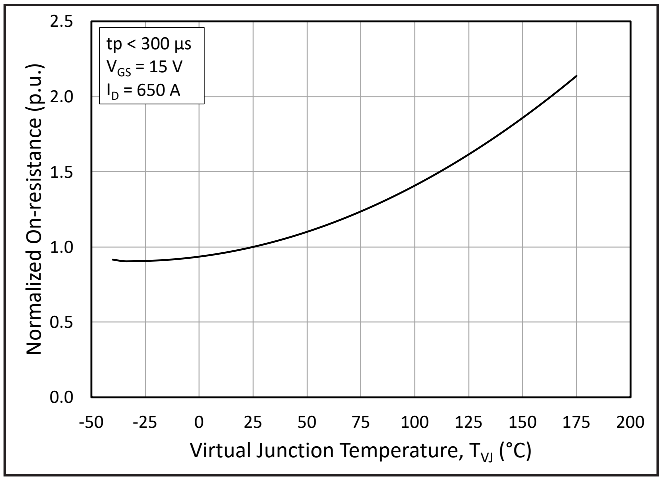


Figure 3. Normalized On-State Resistance vs. Junction Temperature

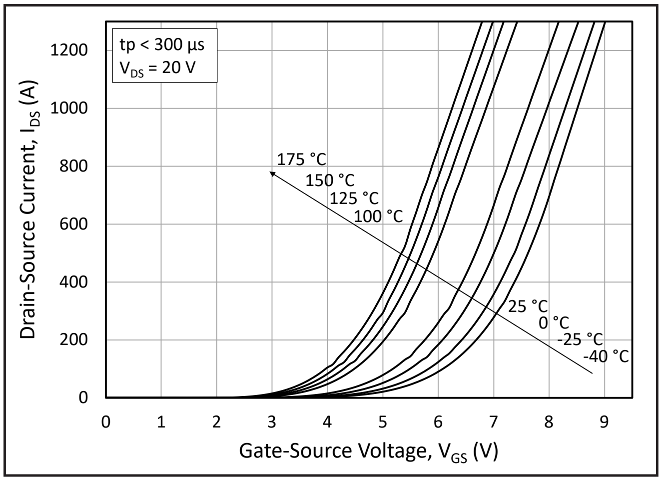


Figure 4. Transfer Characteristic for Various Junction Temperatures

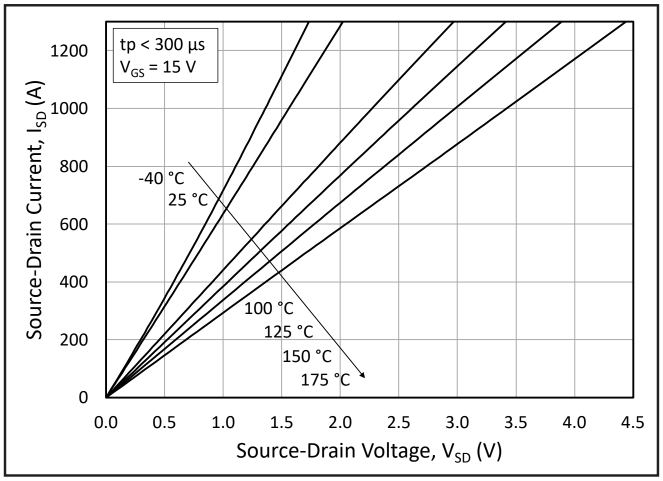


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

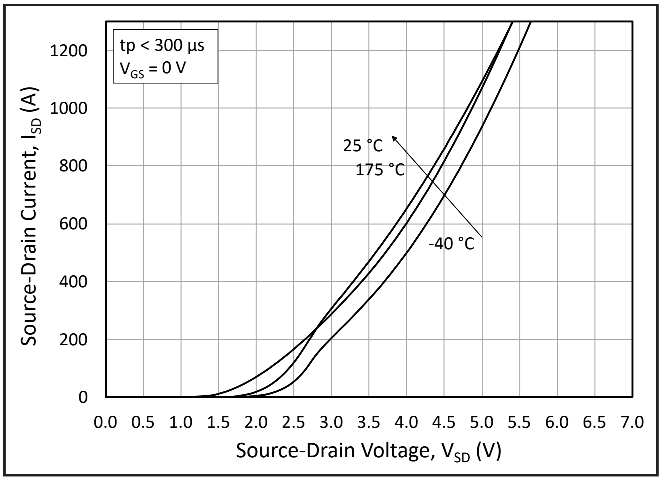


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V (Body Diode)

Typical Performance

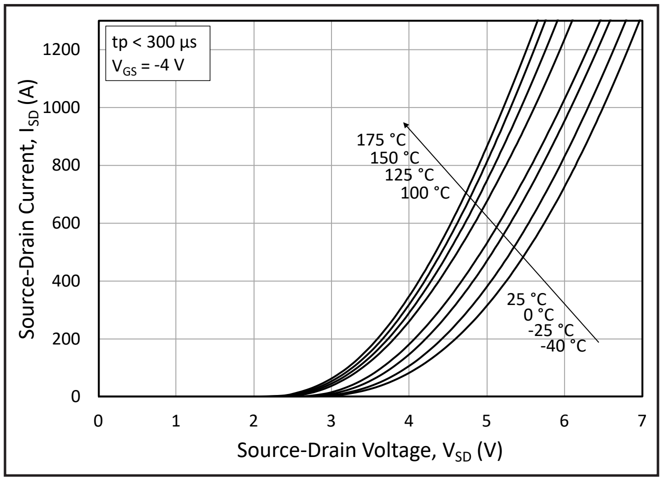


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = -4 V (Body Diode)

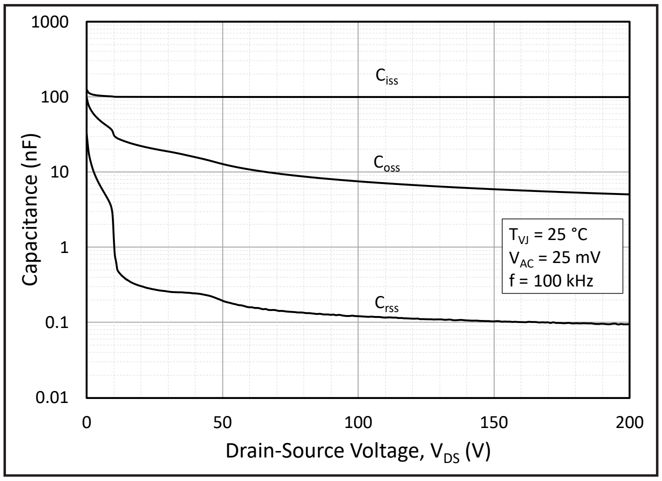


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200 V)

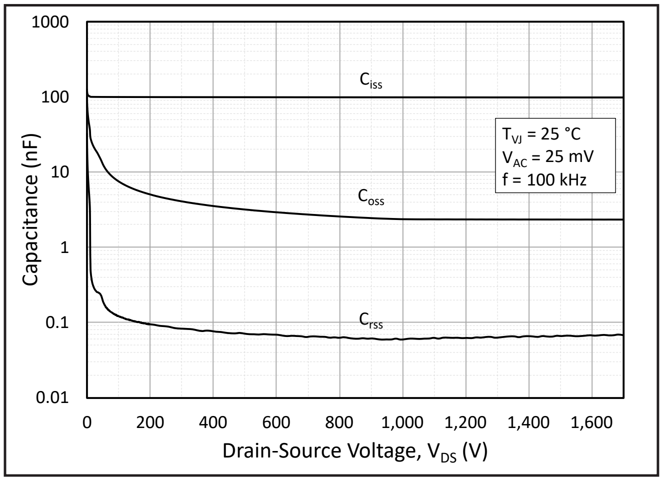


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1700V)

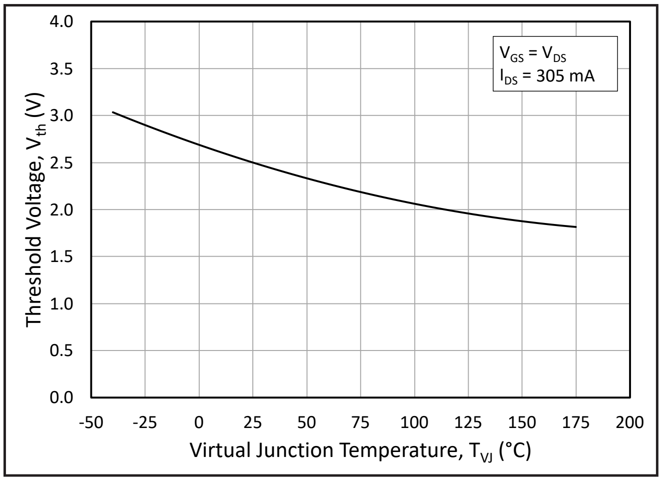


Figure 10. Threshold Voltage vs. Junction Temperature

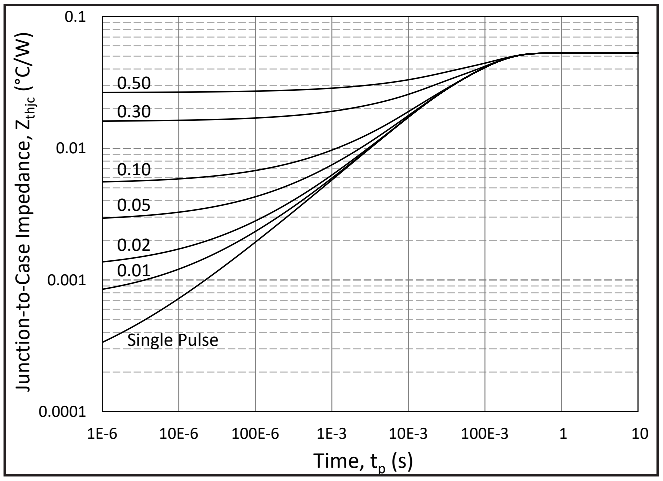


Figure 11. MOSFET Junction to Case Transient Thermal Impedance, $Z_{th\,JC}$ (°C/W)

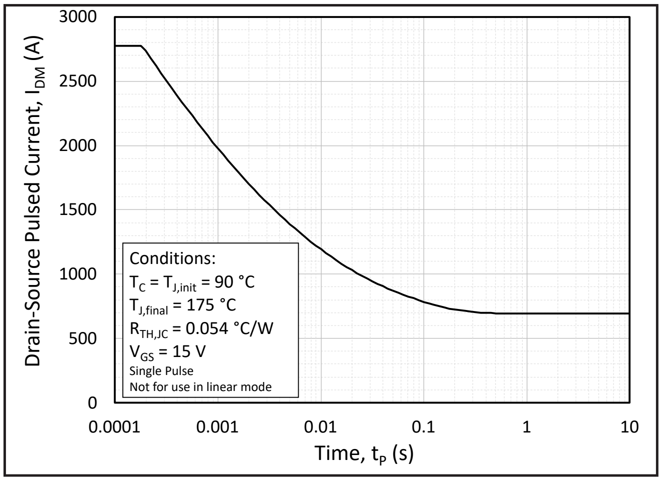


Figure 12. Pulsed Current SOA

Typical Performance

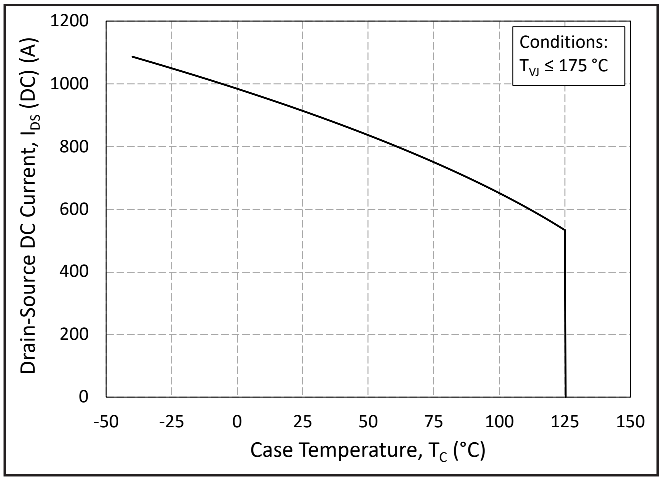


Figure 13. Continuous Drain Current Derating vs. Case Temperature

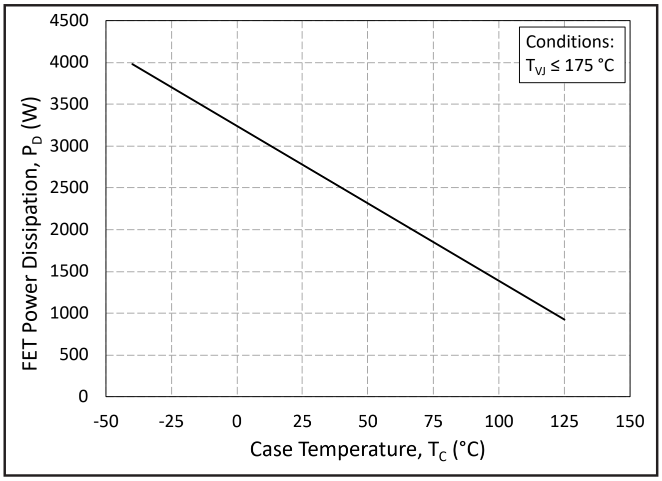


Figure 14. Maximum Power Dissipation Derating vs. Case Temperature

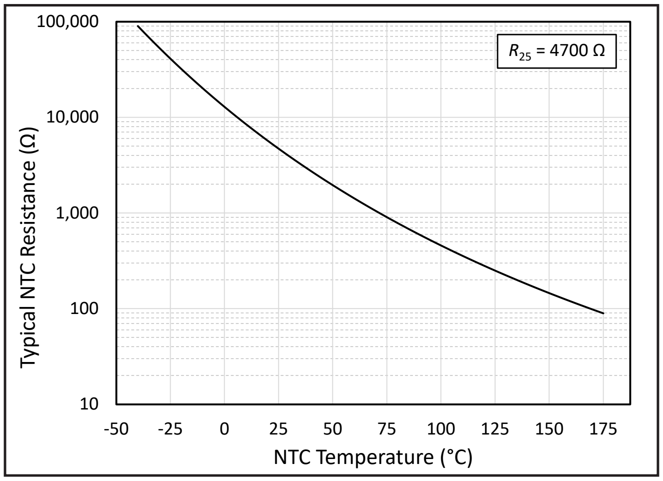


Figure 15. Typical NTC Resistance vs. Temperature

Definitions

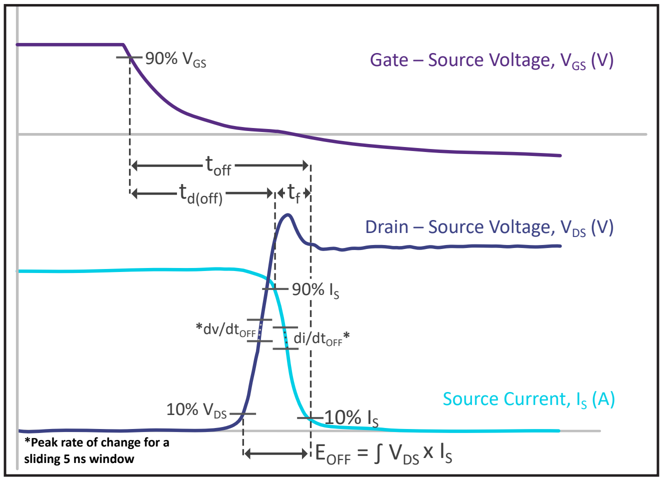


Figure 16. Turn-Off Transient Definitions

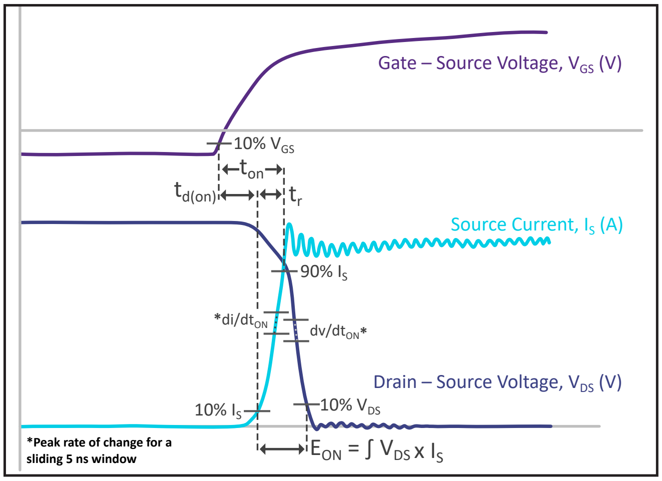


Figure 17. Turn-On Transient Definitions

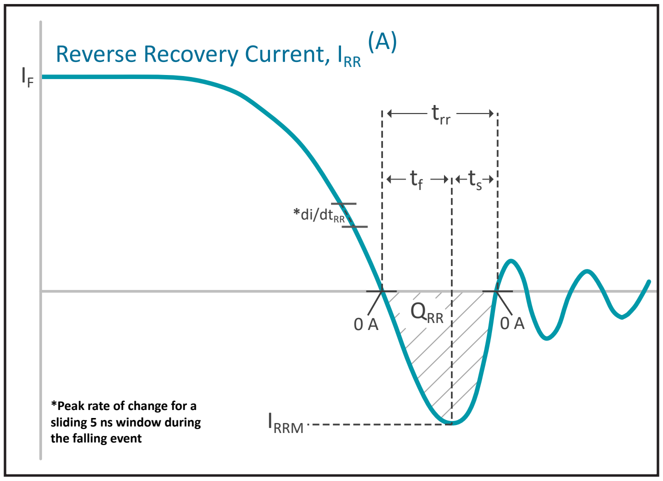


Figure 18. Reverse Recovery Definitions

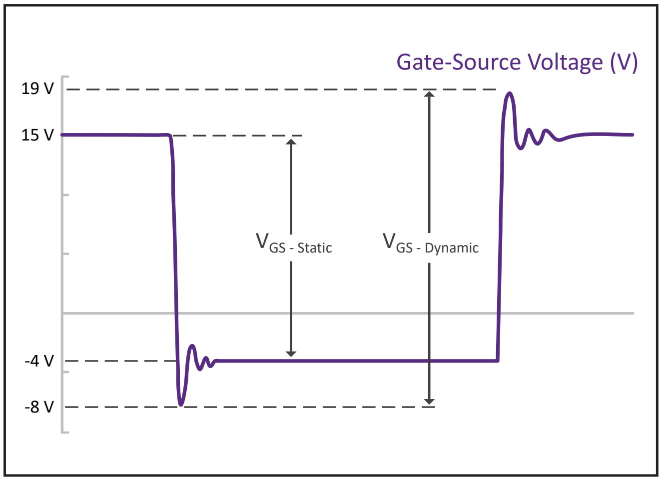
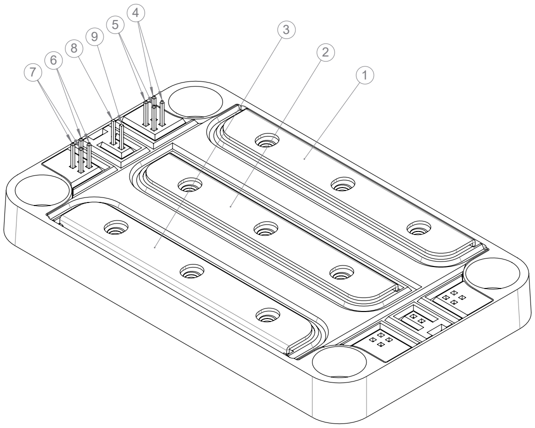
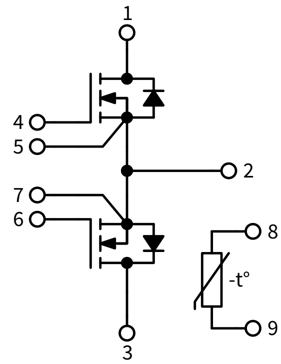


Figure 19. V_{GS} Transient Definitions

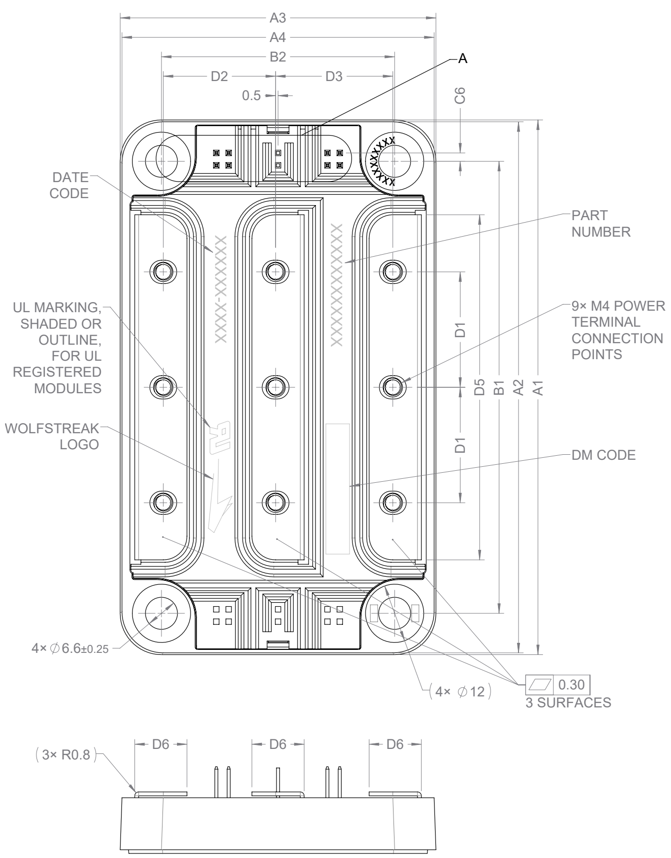
Schematic and Pin Out

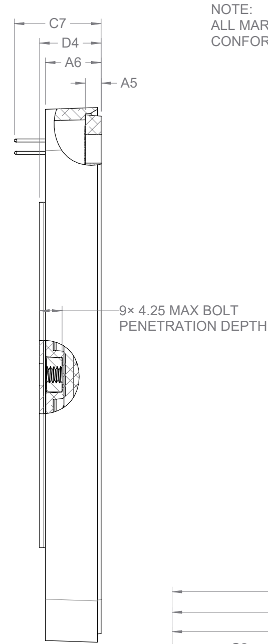


PIN OUT SCHEME	
PIN	LABEL
1	D1
2	Mid
3	D2
4	G1, Top row pins (2)
5	K1, Bottom row pins (2)
6	G2, Top row pins (2)
7	K2, Bottom row pins (2)
8	NTC1
9	NTC2



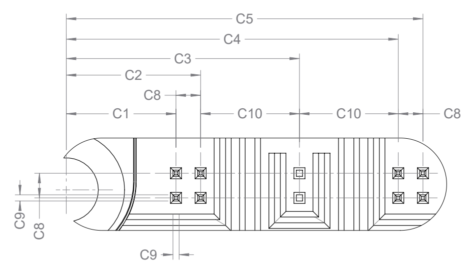
Package Dimensions (mm)





NOTE:
ALL MARKINGS SHALL CONFORM TO PRC-00786.

DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	110	±0.60
A2	109.25	±0.60
A3	65	±0.60
A4	64.25	±0.60
A5	3.25	±0.40
A6	11.45	±0.60
B1	93	±0.30
B2	48	±0.30
C1	11.29	±0.40
C2	13.83	±0.40
C3	24	±0.40
C4	34.17	±0.40
C5	36.71	±0.40
C6	1.71	±0.40
C7	17.84	±0.75
C8	2.54	±0.30
C9	0.64	±0.30
C10	10.17	±0.40
D1	23.75	±0.50
D2	23.13	±0.50
D3	24.13	±0.50
D4	12.65	±0.50
D5	71	±0.30
D6	10.75	±0.50



DETAIL A
SCALE: 4 : 1

Note (6): To improve product traceability, Wolfspeed products include Data Matrix Content barcodes in the form of ZZZZZZZZZZZ-DDDDDD-XXXX-NNNNNNNNNN, where -Z, -D, -X/-N represent product number, date code, and module serial number, respectively. For instance, CLB650M17HM3-FA2036-0042-6706546042 is a CLB650M17HM3 produced in 2020 week 36 with a unique serial number.

Note (7): CLB650M17HM3 has been certified by UL as an "Electrically Isolated Semiconductor Devices – Component" in accordance with UL 1557. Only power modules that bear the UL marking shown in the Package Dimension figure above should be considered as being covered under the UL Component Recognition Program.

Product Ordering Code

Part Number	Description
CLB650M17HM3	Without Pre-Applied Phase Change Thermal Interface Material
CLB650M17HM3T	With Pre-Applied Phase Change Thermal Interface Material

Supporting Links & Tools

Evaluation Tools & Support

- SpeedFit 2.0 Design Simulator™
- Technical Support Forum
- LTspice and PLECS Models

Dual-Channel Gate Driver Board

- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers
- CGD1700HB3P-HM3 Wolfspeed H Module Gate Driver Board
- EVAL-ADUM4146WHB1Z: Analog Devices® Gate Driver Board
- UCC21710QDWEVM-054: Texas Instruments® Gate Driver Board

Application Notes

- PRD-04814: Design Options for Wolfspeed® Silicon Carbide MOSFET Gate Bias Power Supplies
- PRD-06379: Environmental Considerations for Power Electronics Systems
- PRD-08333: Wolfspeed Module CIL Evaluation Kits User Guide
- PRD-07933: Wolfspeed Power Module Thermal Interface Material Application User Guide
- PRD-08376: Thermal Characterization Methods and Applications
- PRD-07845: Power Module Baseplate Capacitance and Electromagnetic Compatibility
- PRD-08710: Measuring Stray Inductance in Power Electronics Systems
- PRD-08911: Considerations for Current Balancing in Paralleled SiC Power Modules
- PRD-09035: Power Module RC Thermal Models User Guide
- PRD-07913: Wolfspeed Power Module SPICE Models User Guide
- PRD-09002: Wolfspeed H Module Mounting Guide

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REACh Compliance

REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

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