

C4MS065120K1

Silicon Carbide Power MOSFET
Switching Optimized 1200V 65mΩ Industrial
N-Channel Enhancement Mode

Features

- Industry compatible drive voltage 15V...18V/-5V...0V
- Soft body diode with low V_{DS} overshoot and ringing
- Low $R_{DS(on)}$ at high operating temperatures
- Improved device capacitances ratio (C_{iss}/C_{rss})
- High transient voltage robustness with improved lifetime
- Halogen free, RoHS compliant

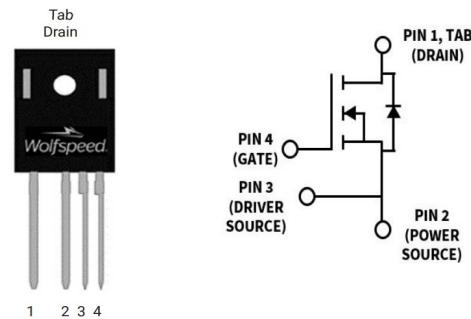
Benefits

- Higher efficiency with lower switching losses and EMI
- Faster switching operation enabling high power density
- Enables system level price performance optimization
- Reduction in system level cooling requirements

Typical Applications

- EV Chargers
- Solar/ESS
- Motor Control
- Industrial Power Supplies
- High Voltage DC/DC Converters

Package



Orderable Part number	Package type	Marking
C4MS065120K1	TO-247-4 LP	C4MS065120K1

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1200	V		
Transient Drain - Source Voltage				1300		<100hrs of lifetime	Note 1
Maximum Gate - Source Voltage	$V_{GS(max)}$	-10		+23			Note 2
DC Continuous Drain Current	I_D		39		A	$V_{GS} = 18\text{ V}, T_c = 25\text{ }^\circ\text{C}, T_j \leq 175\text{ }^\circ\text{C}$	Note 3
			28			$V_{GS} = 18\text{ V}, T_c = 100\text{ }^\circ\text{C}, T_j \leq 175\text{ }^\circ\text{C}$	
Pulsed Drain Current	I_{DM}			105		t_{Pmax} limited by T_{jmax} $V_{GS} = 18\text{ V}, T_c = 25\text{ }^\circ\text{C}$	
Power Dissipation	P_D		182		W	$T_c = 25\text{ }^\circ\text{C}, T_j = 175\text{ }^\circ\text{C}$	Note 4
Operating Junction and Storage Temperature	T_j, T_{stg}	-40		+175	$^\circ\text{C}$		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	

Note (1): 100 hours of total accumulated lifetime of the product.

Note (2): When applying IPC-9592B or OCP M-CRPS derating standards, a maximum Gate-Source voltage (V_{GS}) of +25V is permissible.

Note (3): Current limit calculated by $I_{D(max)} = \sqrt{(P_D / R_{DS(typ)}) (T_{j(max)} / I_{D(max)})}$

Note(4): $P_D = (T_j - T_c) / R_{th(jc,typ)}$


Electrical Characteristics (T_c = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V _{(BR)DSS}	Drain-Source Breakdown Voltage	1200			V	V _{GS} = 0 V, I _D = 100 µA	
V _{GS(th)}	Gate Threshold Voltage	2	2.6	3.9	V	V _{DS} = V _{GS} , I _D = 4.16 mA	Fig. 11
			2.0		V	V _{DS} = V _{GS} , I _D = 4.16 mA, T _J = 175°C	
I _{DSS}	Zero Gate Voltage Drain Current		1	50	µA	V _{DS} = 1200 V, V _{GS} = 0 V	
I _{GSS}	Gate-Source Leakage Current		10	250	nA	V _{GS} = 18 V, V _{DS} = 0 V	
V _{GS(op)}	Recommended Turn on Gate-Source Voltage	+15...+18			V		Refer to PRD-09634
	Recommended Turn off Gate-Source Voltage	-5...0					
R _{DS(on)}	Drain-Source On-State Resistance		65	85	mΩ	V _{GS} = 18 V, I _D = 15.1 A	Fig. 4, 5, 6
			116			V _{GS} = 18 V, I _D = 15.1 A, T _J = 175°C	
			71			V _{GS} = 15 V, I _D = 15.1 A	
g _{fs}	Transconductance		11		S	V _{DS} = 20 V, I _D = 15.1 A, T _J = 25°C	Fig. 7
			10			V _{DS} = 20 V, I _D = 15.1 A, T _J = 175°C	
R _{DS(on)Tempco}	On resistance temperature coefficient		1.88			V _{GS} = 18 V, I _D = 15.1 A	Note 5
C _{iss}	Input Capacitance		1225		pF	V _{GS} = 0 V, V _{DS} = 1000 V f = 100 kHz V _{AC} = 25 mV	Fig. 17, 18
C _{oss}	Output Capacitance		47				
C _{rss}	Reverse Transfer Capacitance		2.4				
C _{iss/C_{rss}}	Capacitance Ratio		630				
E _{oss}	C _{oss} Stored Energy		30		µ		Fig. 16
C _{o(er)}	Effective Output Capacitance (Energy Related)		68		pF	V _{GS} = 0 V, V _{DS} = 0...800 V	
C _{o(tr)}	Effective Output Capacitance (Time Related)		108				
E _{on}	Turn-On Switching Energy (Body Diode FWD)				µ	V _{DS} = 800 V, V _{GS} = -4 V/18 V, I _D = 15.1 A, R _{G(ext)} = 2Ω, L _σ = 25 nH	Fig. 26, 29, 31
	T _J =25C		164				
E _{off}	T _J =175C		193				
	Turn-Off Switching Energy (Body Diode FWD)						
E _{off}	T _J =25C		19		ns	V _{DD} = 800 V, V _{GS} = -4 V/18 V I _D = 15.1 A, R _{G(ext)} = 2Ω, Timing relative to V _{DS} Inductive load	Fig. 26, 29, 32
	T _J =175C		20				
t _{d(on)}	Turn-On Delay Time		9				
t _r	Rise Time		2				
t _{d(off)}	Turn-Off Delay Time		21		nC	V _{DS} = 800 V, V _{GS} = -4 V/18 V I _D = 15.1 A, T _J = 25°C Per IEC60747-8-4 pg 21	Fig. 27, 28
t _f	Fall Time		10				
R _{G(int)}	Internal Gate Resistance		3.1		Ω	f = 1 MHz	
Q _{gs}	Gate to Source Charge		14				
Q _{gd}	Gate to Drain Charge		12				Fig. 12
Q _g	Total Gate Charge		51				

Note (5): R_{DS(on)Tempco} refers to R_{DS(on)} at 175°C / R_{DS(on)} at 25°C, C4MS 1200V product family value

Note (6): Capacitance ratio is a FOM for Partial turn-on immunity PRD-09633, C4MS 1200V product family value

Co(er), a lumped capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 800V

Co(tr), a lumped capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 800V



Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.1		V	$V_{GS} = -4\text{ V}$, $I_{SD} = 7.6\text{ A}$, $T_j = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.5		V	$V_{GS} = -4\text{ V}$, $I_{SD} = 7.6\text{ A}$, $T_j = 175^\circ\text{C}$	
I_s	Continuous Diode Forward Current	26		A	$V_{GS} = -4\text{ V}$, $T_c = 25^\circ\text{C}$	
I_{SM}	Diode Pulse Current		105	A	$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{jmax}	
t_{rr}	Reverse Recovery Time	11		ns	$V_{GS} = -4\text{ V}$, $I_s = 15.1\text{ A}$, $V_{SD} = 800\text{V}$ $T_j = 175^\circ\text{C}$, $dI/dt = 12.1\text{ A/ns}$	
Q_{rr}	Reverse Recovery Charge	325		nC		
I_{RRM}	Peak Reverse Recovery current	57		A		
E_{RR}	Reverse recovery Energy $T_j = 25^\circ\text{C}$ $T_j = 175^\circ\text{C}$	45		μJ	$V_{DS} = 800\text{ V}$, $I_D = 15.1\text{ A}$, $V_{GS} = -4\text{ V}/18\text{ V}$, $R_{G(on)} = 2\Omega$, $L\sigma = 25\text{nH}$	
		87				

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.82	$^\circ\text{C}/\text{W}$		

Typical Performance

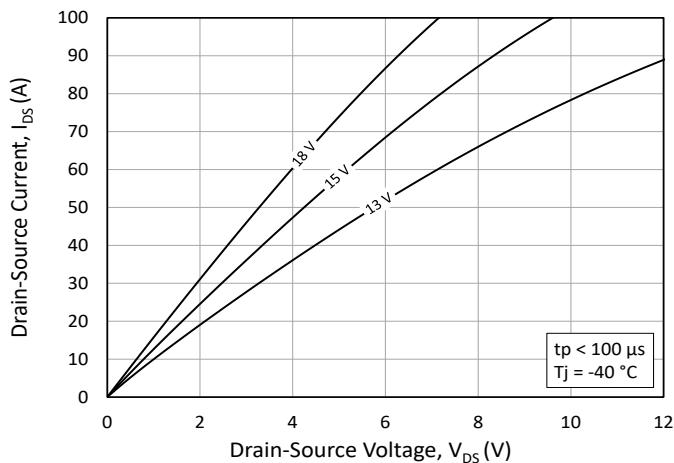
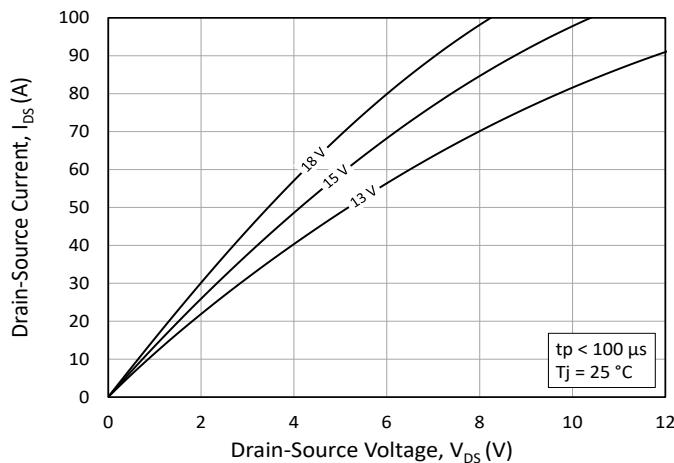
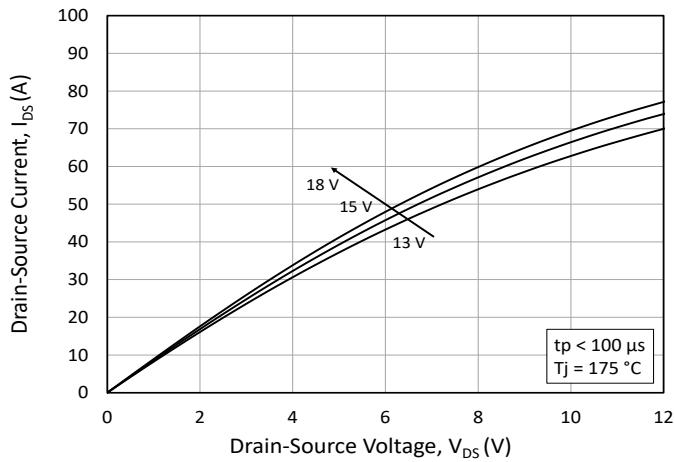
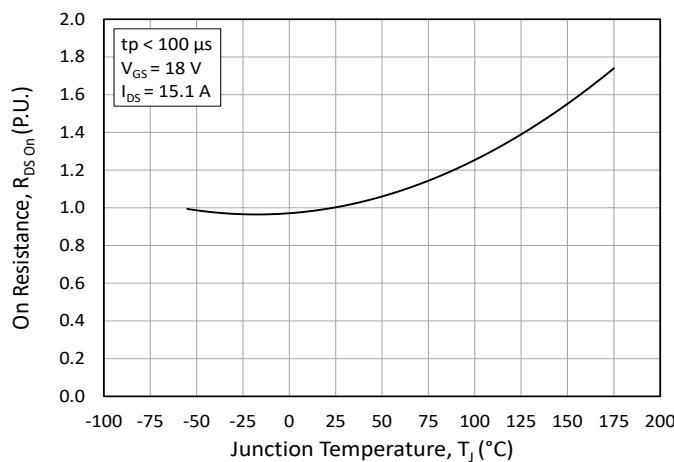
Figure 1. Output Characteristics $T_j = -40^\circ\text{C}$ Figure 2. Output Characteristics $T_j = 25^\circ\text{C}$ Figure 3. Output Characteristics $T_j = 175^\circ\text{C}$ 

Figure 4. Normalized On-Resistance vs. Temperature

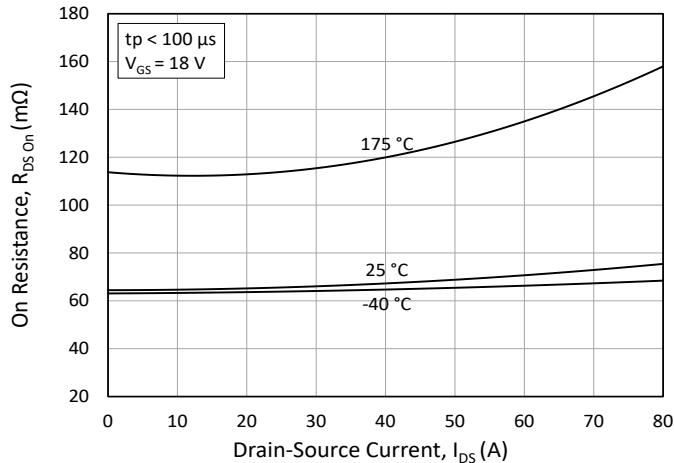


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

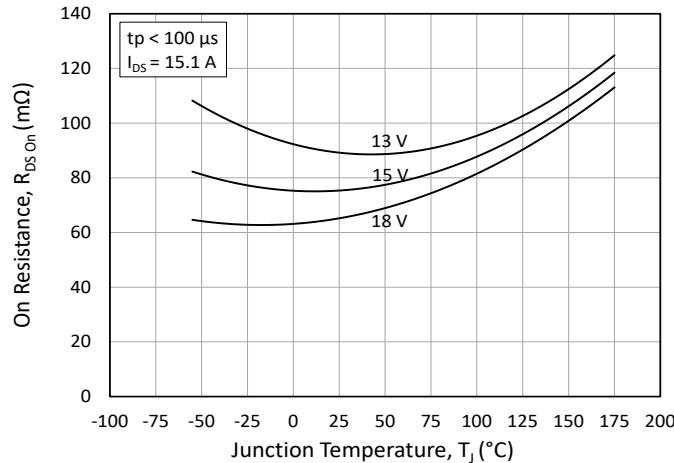
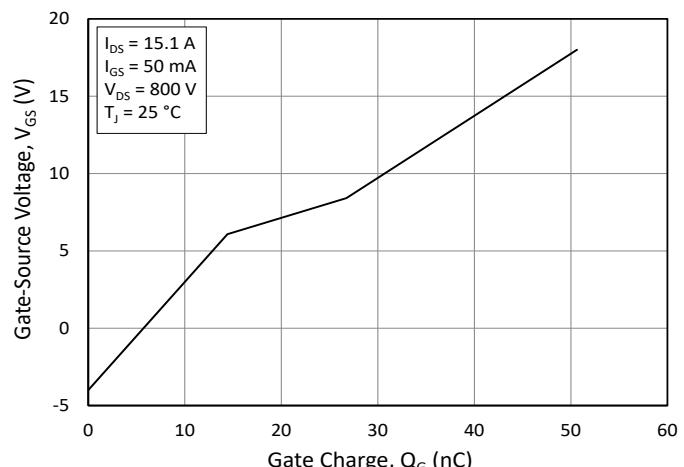
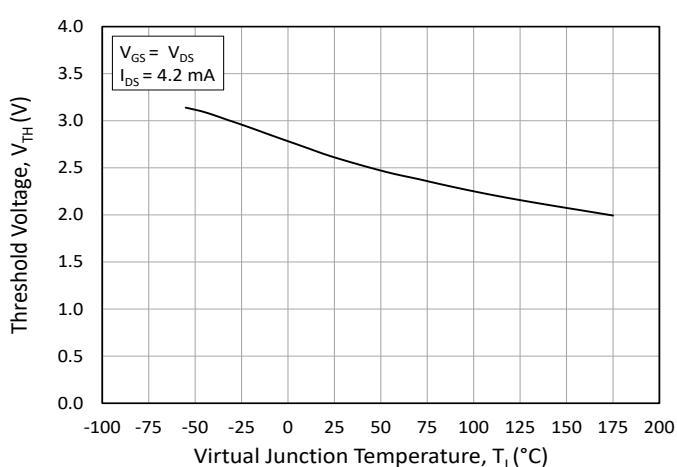
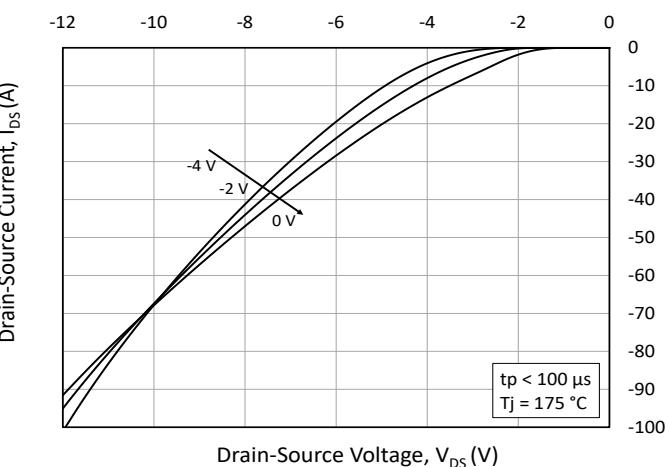
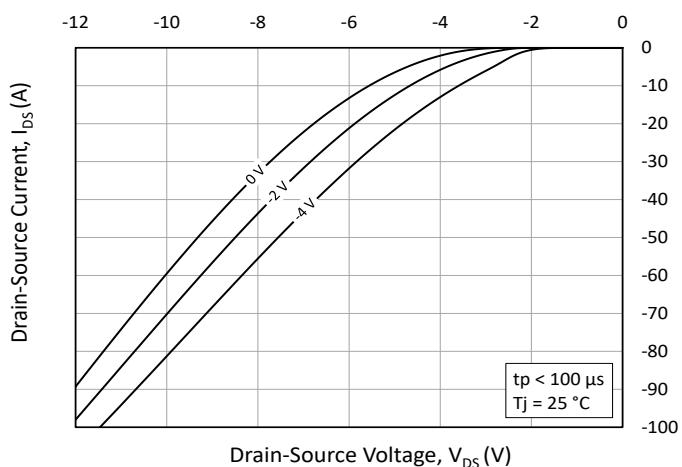
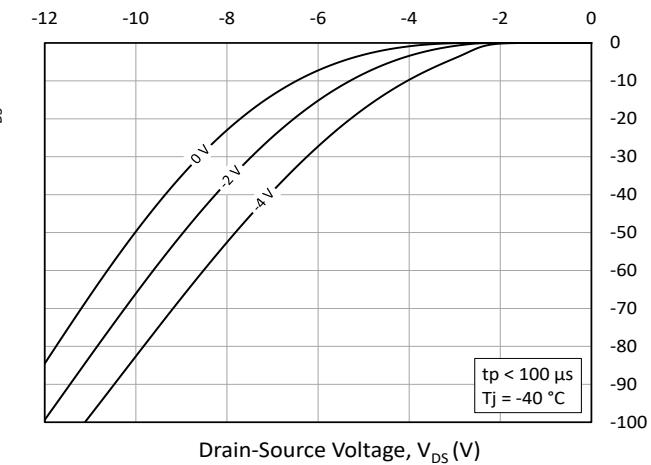
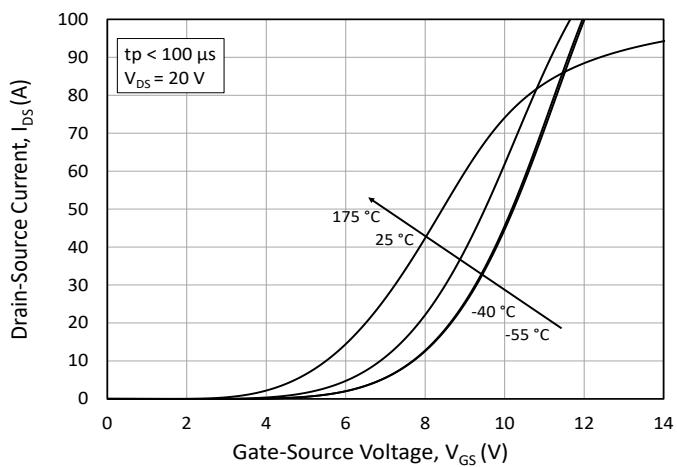


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

Typical Performance



Typical Performance

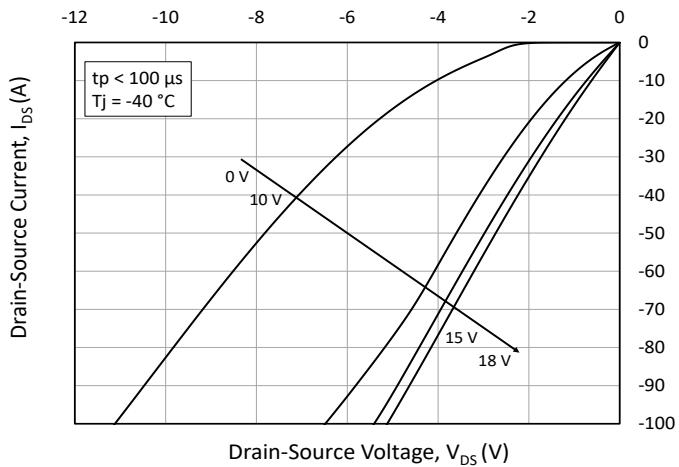
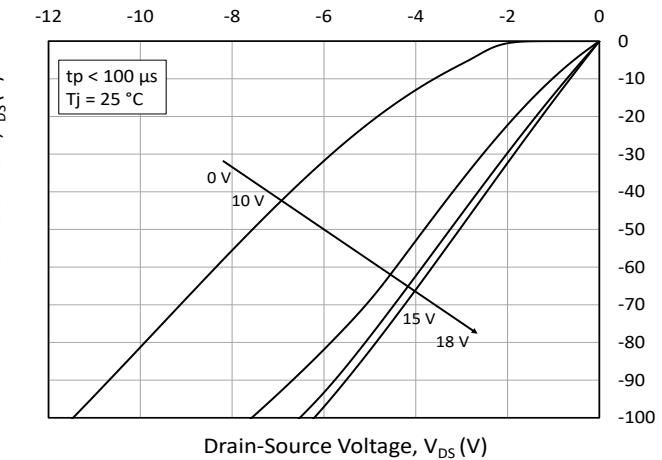
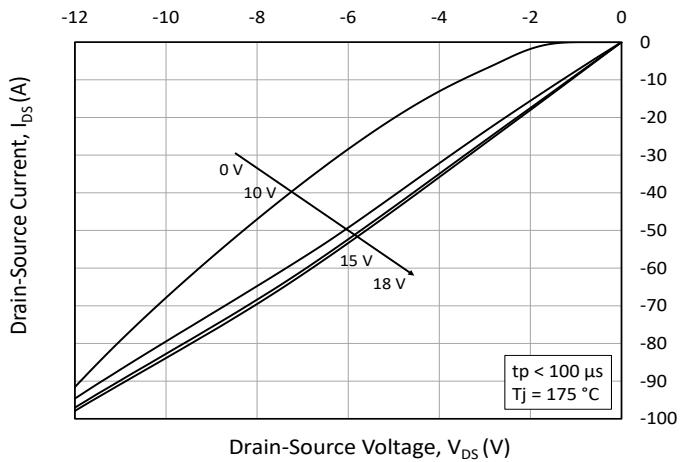
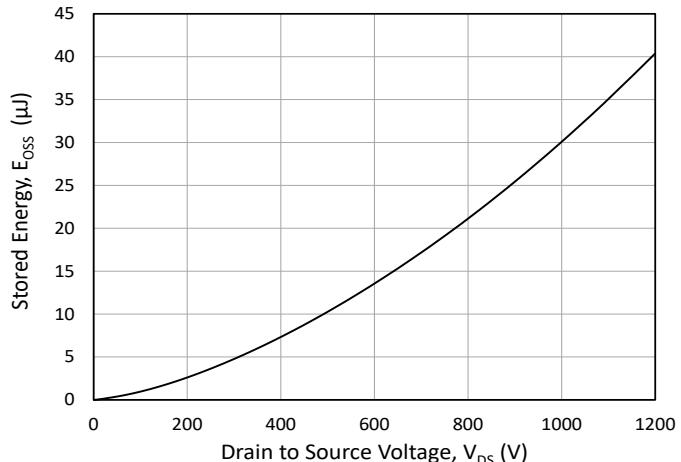
Figure 13. 3rd Quadrant Characteristic at -40°C Figure 14. 3rd Quadrant Characteristic at 25°C Figure 15. 3rd Quadrant Characteristic at 175°C 

Figure 16. Output Capacitor Stored Energy

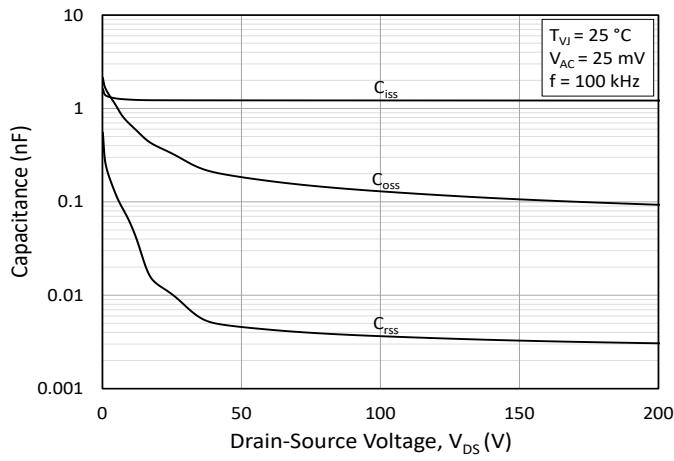


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

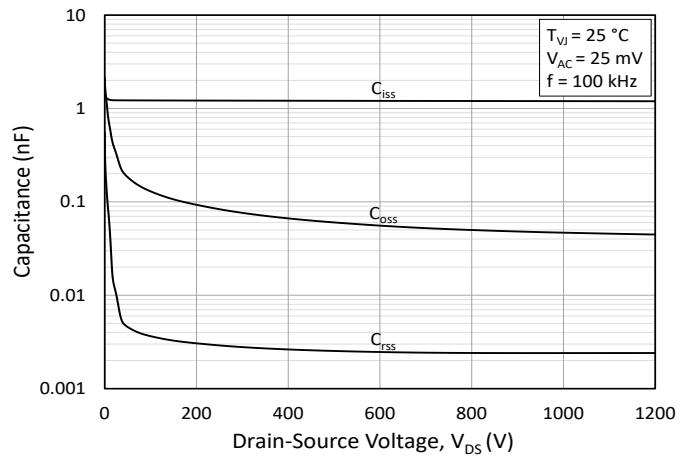


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200 V)

Typical Performance

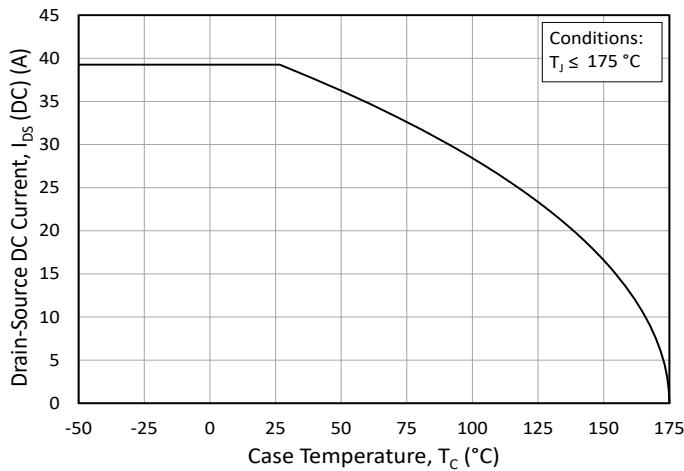


Figure 19. Continuous Drain Current Derating vs. Case Temperature

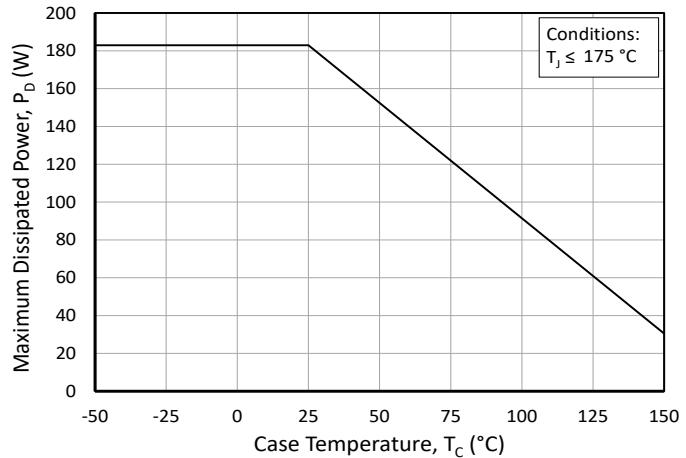


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

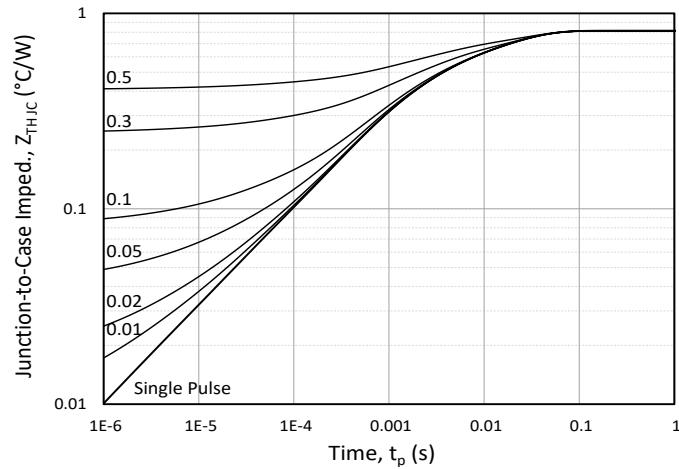


Figure 21. Transient Thermal Impedance (Junction - Case)

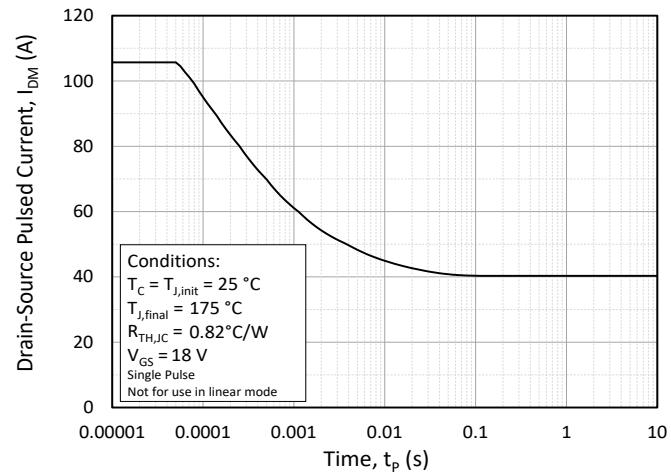


Figure 22. Safe Operating Area

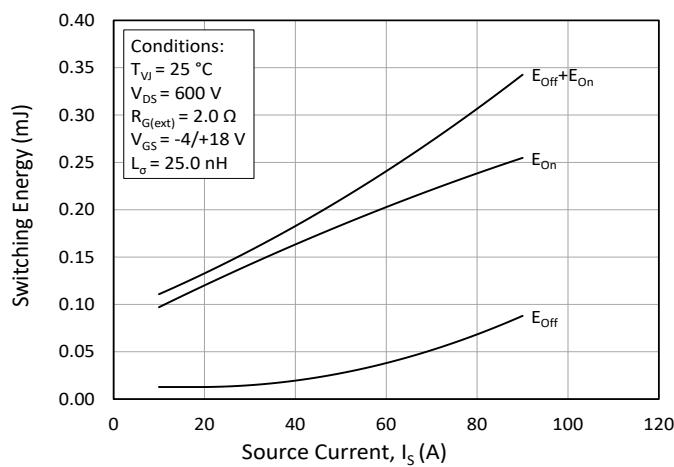


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 600$ V)

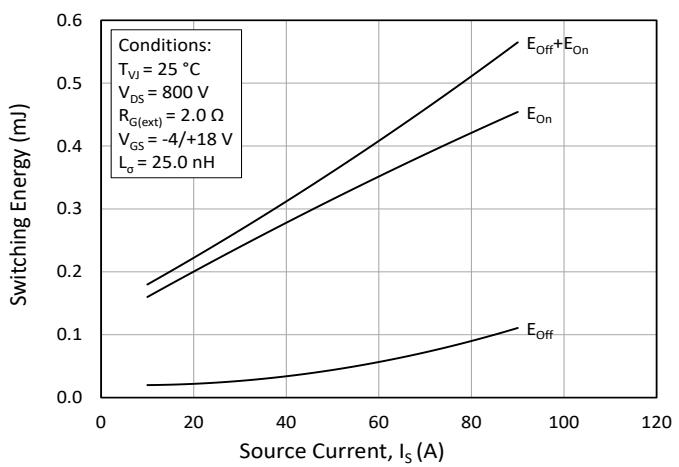


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 800$ V)

Typical Performance

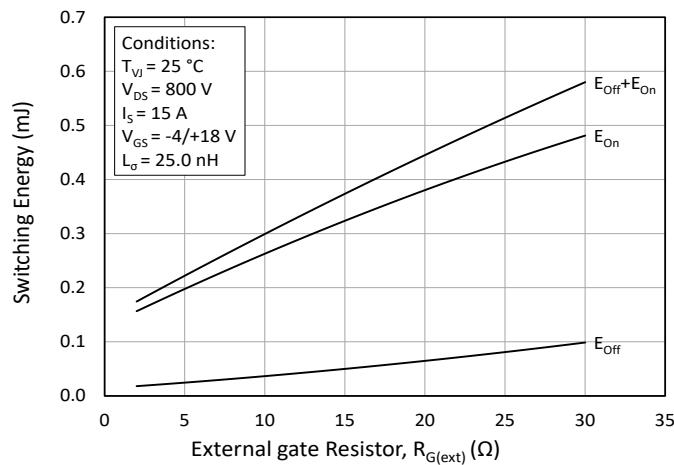
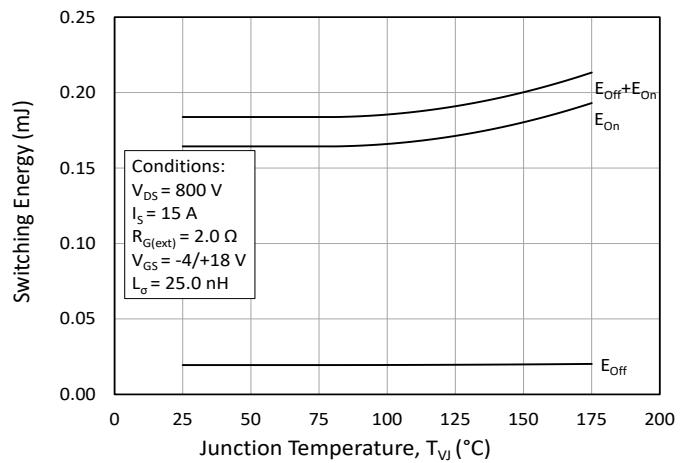
Figure 25. Clamped Inductive Switching Energy vs. $R_{G(\text{ext})}$ 

Figure 26. Clamped Inductive Switching Energy vs. Temperature

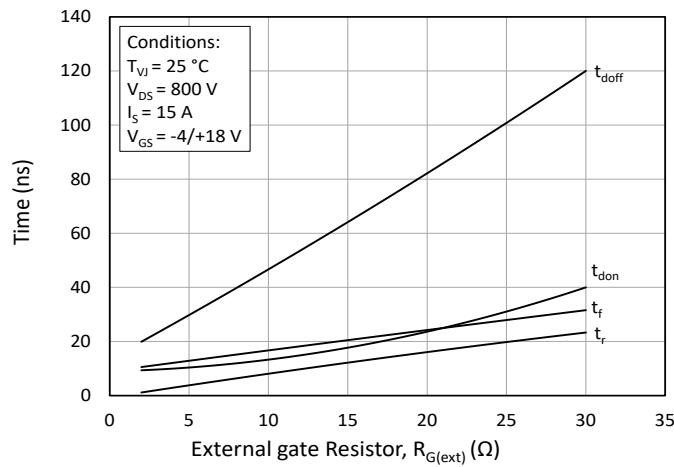
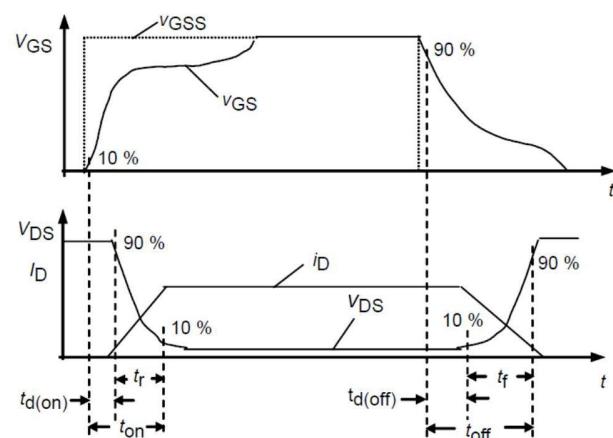
Figure 27. Switching Times vs. $R_{G(\text{ext})}$ 

Figure 28. Switching Times Definition

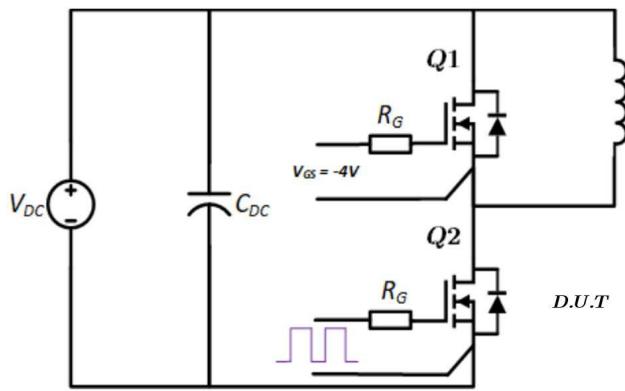


Figure 29. Clamped Inductive MOSFET Switching Waveform Test Circuit

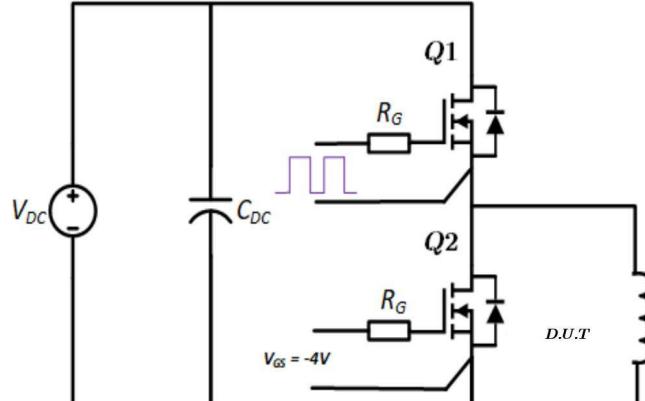
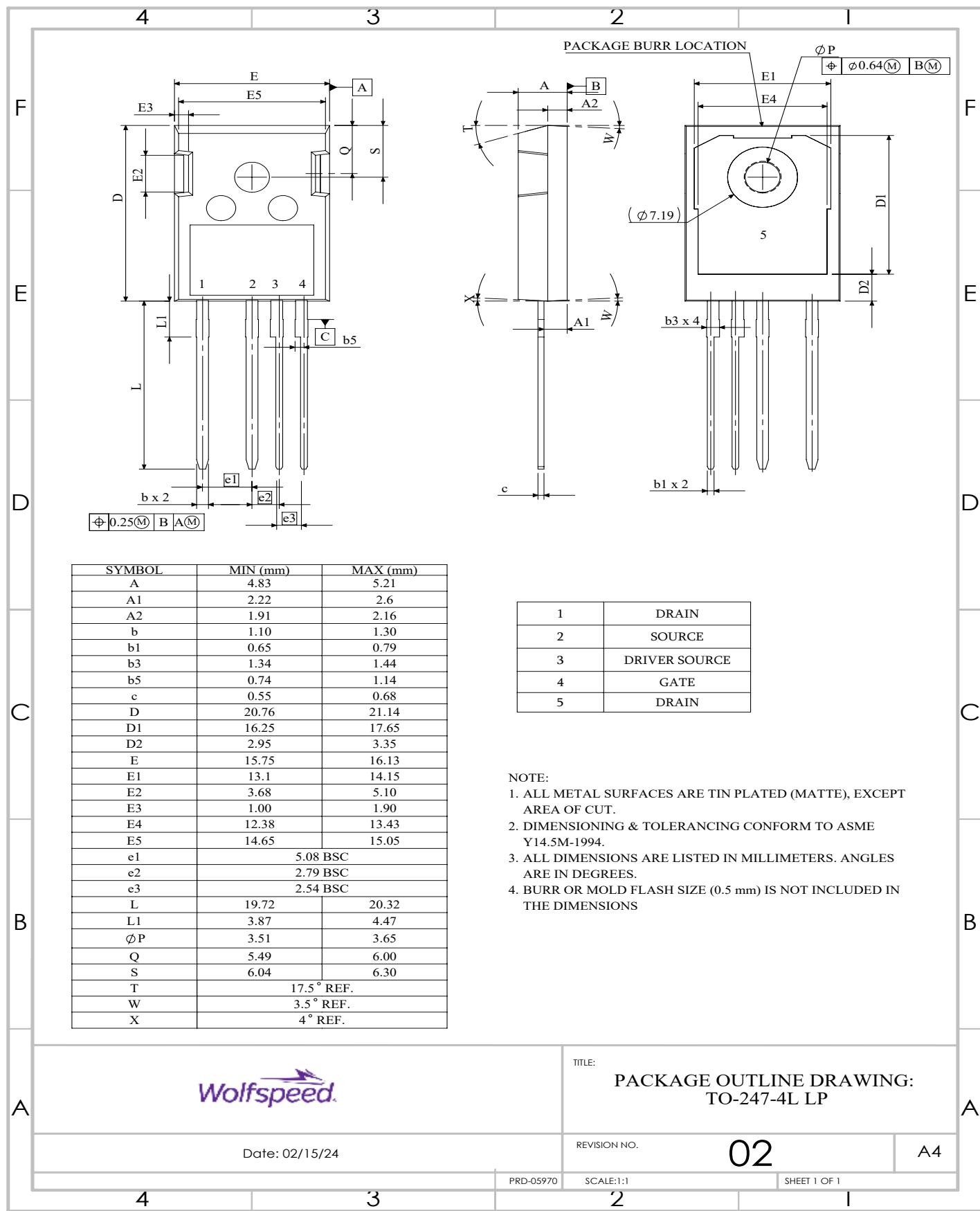


Figure 30. Clamped Inductive Body diode Switching Waveform Test Circuit

Package Dimensions



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TO-247-4L LP

Wolfspeed

Date: 02/15/24

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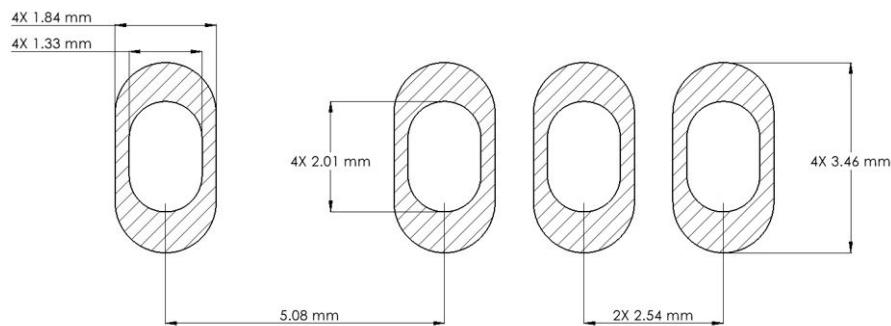
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SHEET 1 OF 1

Recommended Solder Pad Layout

All dimensions in mm



Revision history

Document Version	Date of release	Description of changes
1	November 2025	Initial release
2	December 2025	Updated Note 2



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