

# C4MS065120J2

Silicon Carbide Power MOSFET  
Switching Optimized 1200V 65mΩ Industrial  
N-Channel Enhancement Mode

## Features

- Industry compatible drive voltage 15V...18V/-5V...0V
- Soft body diode with low Vds overshoot and ringing
- Low Rds(on) at high operating temperatures
- Improved device capacitances ratio (Ciss/Crss)
- High transient voltage robustness with improved lifetime
- Halogen free, RoHS compliant

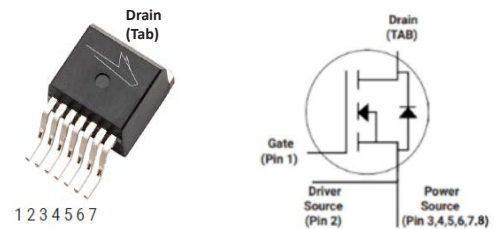
## Benefits

- Higher efficiency with lower switching losses and EMI
- Faster switching operation enabling high power density
- Enables system level price performance optimization
- Reduction in system level cooling requirements

## Typical Applications

- EV Chargers
- Solar/ESS
- Motor Control
- Industrial Power Supplies
- High Voltage DC/DC Converters

## Package



Orderable Part number	Package type	Marking
C4MS065120J2-TR	TO-263-7XL	C4MS065120J2

## Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	$V_{DS}$			1200	V		
Transient Drain - Source Voltage				1300		<100hrs of lifetime	Note 1
Maximum Gate - Source Voltage		-10		+23			Note 2
DC Continuous Drain Current	$I_D$		40		A	$V_{GS} = 18V, T_C = 25^\circ C, T_J \leq 175^\circ C$	Note 3
			30			$V_{GS} = 18V, T_C = 100^\circ C, T_J \leq 175^\circ C$	
Pulsed Drain Current	$I_{DM}$			105		$t_{Pmax}$ limited by $T_{Jmax}$ $V_{GS} = 18V, T_C = 25^\circ C$	
Power Dissipation	$P_D$		211		W	$T_C = 25^\circ C, T_J = 175^\circ C$	Note 4
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-40		+175	$^\circ C$		
Solder Temperature	$T_L$			260		According to JEDEC J-STD-020	

Note (1): 100 hours of total accumulated lifetime of the product.

Note (2): When applying IPC-9592B or OCP M-CRPS derating standards, a maximum Gate-Source voltage (Vgs) of +25V is permissible.

Note (3): Current limit calculated by  $I_{D(max)} = \sqrt{(P_D / R_{DS(typ)}) \cdot (T_{J(max)} - T_{D(max)})}$

Note(4):  $P_D = (T_J - T_C) / R_{th(JC, typ)}$


**Electrical Characteristics** ( $T_c = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	2	2.6	3.9	V	$V_{DS} = V_{GS}, I_D = 4.16\text{ mA}$	Fig. 11
			2.0		V	$V_{DS} = V_{GS}, I_D = 4.16\text{ mA}, T_J = 175^\circ\text{C}$	
$I_{DSS}$	Zero Gate Voltage Drain Current		1	50	$\mu\text{A}$	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$	
$I_{GSS}$	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 18\text{ V}, V_{DS} = 0\text{ V}$	
$V_{GS(op)}$	Recommended Turn on Gate-Source Voltage		+15...+18		V		Refer to PRD-09634
	Recommended Turn off Gate-Source Voltage		-5...0				
$R_{DS(on)}$	Drain-Source On-State Resistance		65	85	m $\Omega$	$V_{GS} = 18\text{ V}, I_D = 15.1\text{ A}$	Fig. 4, 5, 6
			116			$V_{GS} = 18\text{ V}, I_D = 15.1\text{ A}, T_J = 175^\circ\text{C}$	
			71			$V_{GS} = 15\text{ V}, I_D = 15.1\text{ A}$	
$g_{fs}$	Transconductance		11		S	$V_{DS} = 20\text{ V}, I_D = 15.1\text{ A}, T_J = 25^\circ\text{C}$	Fig. 7
			10			$V_{DS} = 20\text{ V}, I_D = 15.1\text{ A}, T_J = 175^\circ\text{C}$	
$R_{DS(on)Tempco}$	On resistance temperature coefficient		1.88			$V_{GS} = 18\text{ V}, I_D = 15.1\text{ A}$	Note 5
$C_{iss}$	Input Capacitance		1225		pF	$V_{GS} = 0\text{ V}, V_{DS} = 1000\text{ V}$ $f = 100\text{ kHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
$C_{oss}$	Output Capacitance		47				
$C_{rss}$	Reverse Transfer Capacitance		2.4				
$C_{iss}/C_{rss}$	Capacitance Ratio		630				Note 6
$E_{oss}$	$C_{oss}$ Stored Energy		30		$\mu\text{J}$		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		68		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0...800\text{ V}$	
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		108				
$E_{on}$	Turn-On Switching Energy (Body Diode FWD) $T_J = 25^\circ\text{C}$ $T_J = 175^\circ\text{C}$		164 193		$\mu\text{J}$	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/18\text{ V}, I_D = 15.1\text{ A},$ $R_{G(ext)} = 2\Omega, L_\sigma = 25\text{ nH}$	Fig. 26, 29, 31
	Turn-Off Switching Energy (Body Diode FWD) $T_J = 25^\circ\text{C}$ $T_J = 175^\circ\text{C}$		19 20				Fig. 26, 29, 32
$t_{d(on)}$	Turn-On Delay Time		9		ns	$V_{DD} = 800\text{ V}, V_{GS} = -4\text{ V}/18\text{ V}$ $I_D = 15.1\text{ A}, R_{G(ext)} = 2\Omega,$ Timing relative to $V_{DS}$ Inductive load	Fig. 27, 28
$t_r$	Rise Time		2				
$t_{d(off)}$	Turn-Off Delay Time		21				
$t_f$	Fall Time		10				
$R_{G(int)}$	Internal Gate Resistance		3.1		$\Omega$	$f = 1\text{ MHz}$	
$Q_{gs}$	Gate to Source Charge		14		nC	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/18\text{ V}$ $I_D = 15.1\text{ A}, T_J = 25^\circ\text{C}$ Per IEC60747-8-4 pg 21	Fig. 12
$Q_{gd}$	Gate to Drain Charge		12				
$Q_g$	Total Gate Charge		51				

Note (5):  $R_{DS(on)Tempco}$  refers to  $R_{DS(on)}$  at  $175^\circ\text{C}$  /  $R_{DS(on)}$  at  $25^\circ\text{C}$ , C4MS 1200V product family value

Note (6): Capacitance ratio is a FOM for Partial turn-on immunity PRD-06933, C4MS 1200V product family value

$C_{o(er)}$ , a lumped capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{ds}$  is rising from 0 to 800V

$C_{o(tr)}$ , a lumped capacitance that gives the same charging time as  $C_{oss}$  while  $V_{ds}$  is rising from 0 to 800V



Reverse Diode Characteristics (T<sub>c</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V <sub>SD</sub>	Diode Forward Voltage	5.1		V	V <sub>GS</sub> = -4 V, I <sub>SD</sub> = 7.6 A, T <sub>J</sub> = 25 °C	Fig. 8, 9, 10
		4.5		V	V <sub>GS</sub> = -4 V, I <sub>SD</sub> = 7.6 A, T <sub>J</sub> = 175 °C	
I <sub>S</sub>	Continuous Diode Forward Current	30		A	V <sub>GS</sub> = -4 V, T <sub>C</sub> = 25°C	
I <sub>SM</sub>	Diode Pulse Current		105	A	V <sub>GS</sub> = -4 V, pulse width t <sub>p</sub> limited by T <sub>Jmax</sub>	
t <sub>rr</sub>	Reverse Recovery Time	11		ns	V <sub>GS</sub> = -4 V, I <sub>S</sub> = 15.1 A, V <sub>SD</sub> = 800V T <sub>J</sub> = 175°C, diF/dt = 12.1 A/ns	
Q <sub>rr</sub>	Reverse Recovery Charge	325		nC		
I <sub>RRM</sub>	Peak Reverse Recovery current	57		A		
E <sub>RR</sub>	Reverse recovery Energy				V <sub>DS</sub> = 800 V, I <sub>D</sub> = 15.1 A,	
	T <sub>J</sub> = 25C	45		μJ	V <sub>GS</sub> = -4V/18V, R <sub>Gi(on)</sub> = 2 Ω, Lσ = 25nH	
	T <sub>J</sub> = 175C	87				

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
R <sub>θJC</sub>	Thermal Resistance from Junction to Case	0.71	°C/W		

## Typical Performance

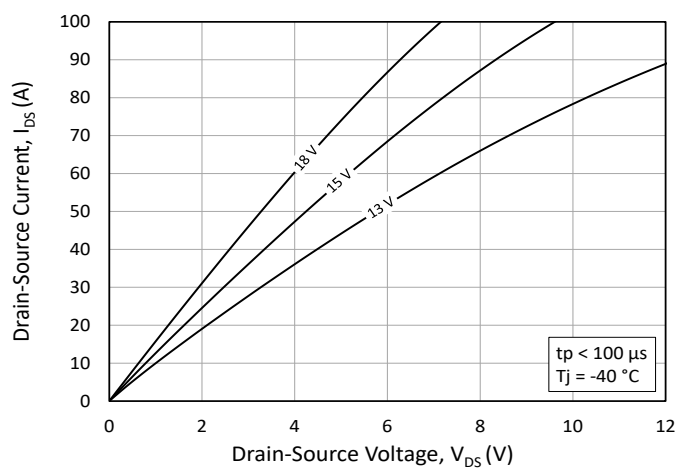
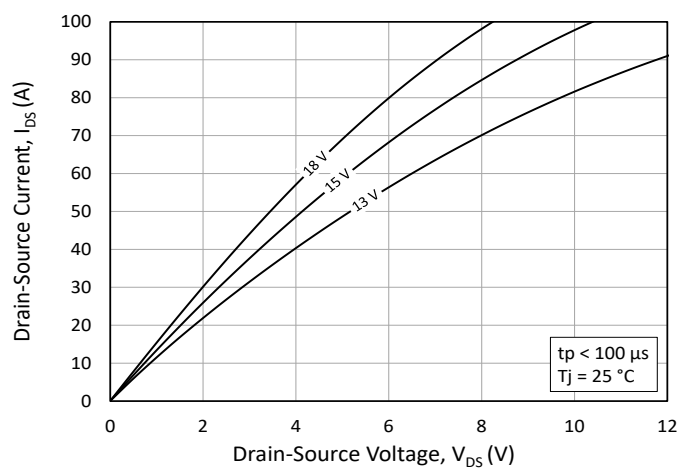
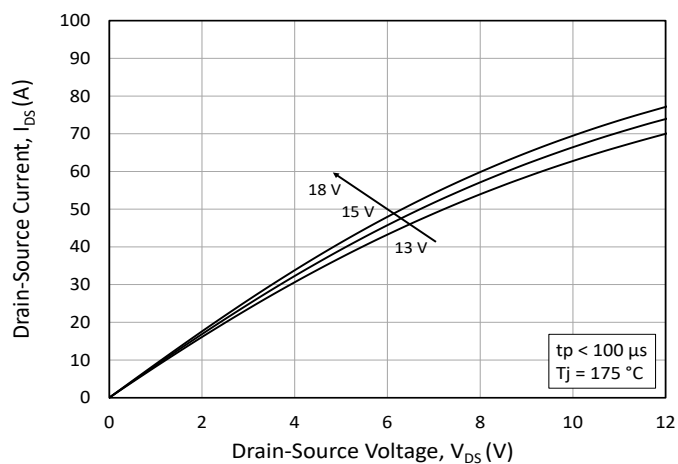
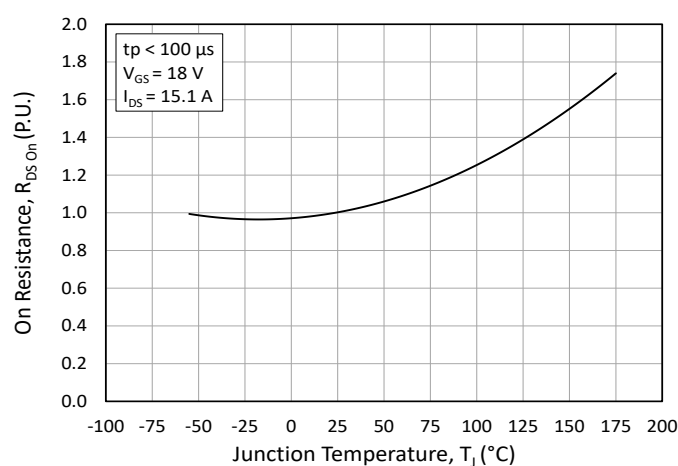
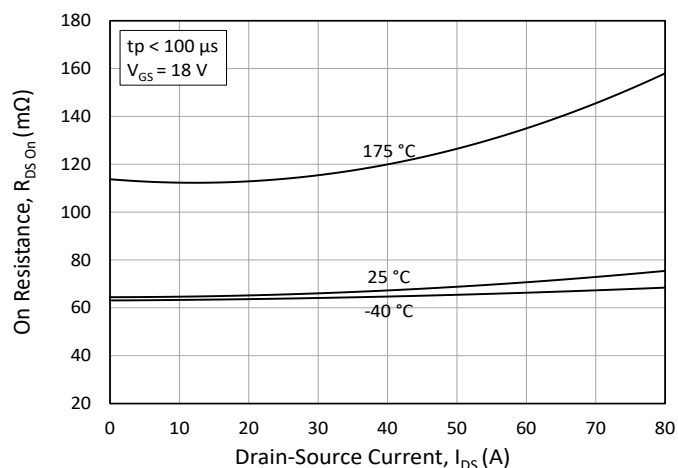
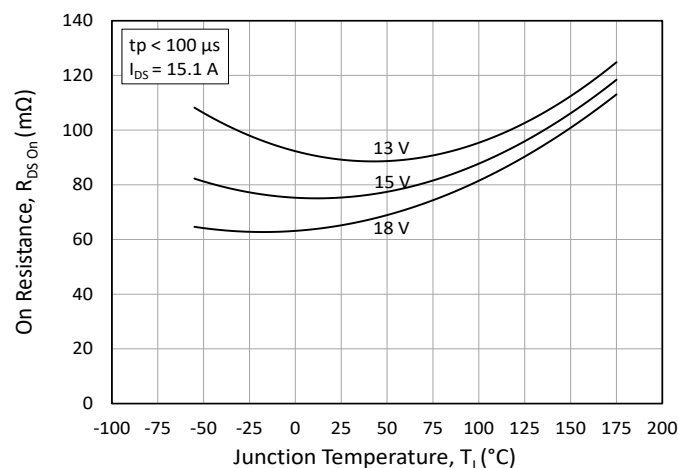
Figure 1. Output Characteristics  $T_j = -40^{\circ}\text{C}$ Figure 2. Output Characteristics  $T_j = 25^{\circ}\text{C}$ Figure 3. Output Characteristics  $T_j = 175^{\circ}\text{C}$ 

Figure 4. Normalized On-Resistance vs. Temperature

Figure 5. On-Resistance vs. Drain Current  
For Various TemperaturesFigure 6. On-Resistance vs. Temperature  
For Various Gate Voltage

## Typical Performance

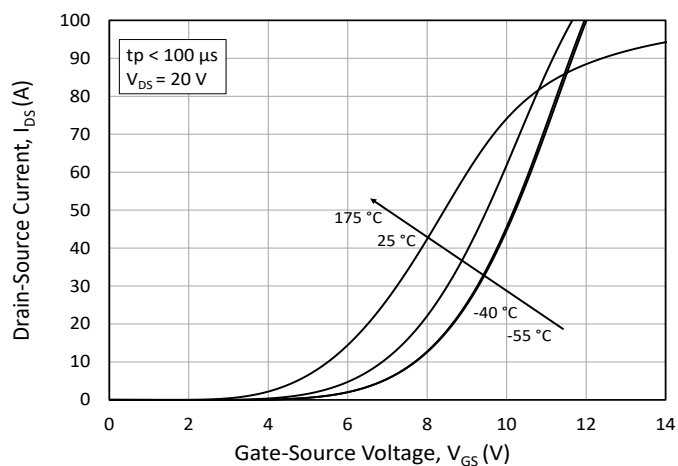


Figure 7. Transfer Characteristic for Various Junction Temperatures

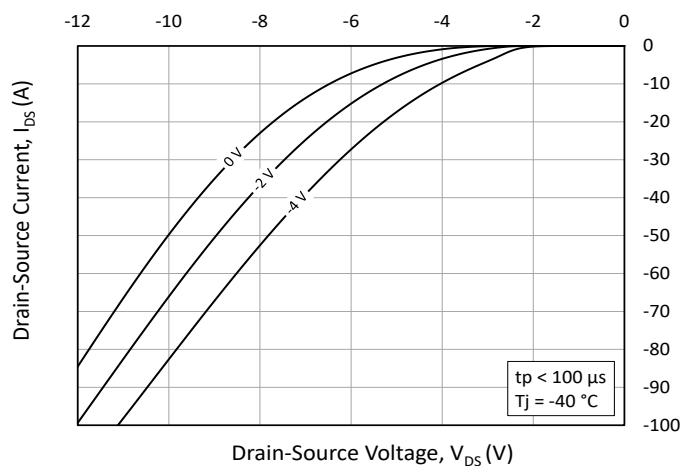


Figure 8. Body Diode Characteristic at -40 °C

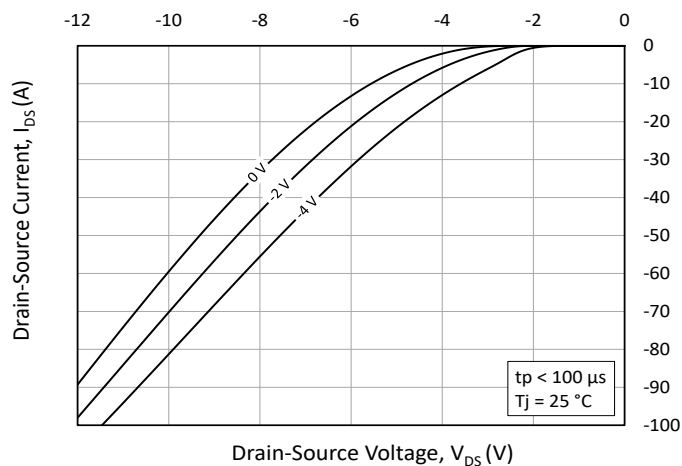


Figure 9. Body Diode Characteristic at 25 °C

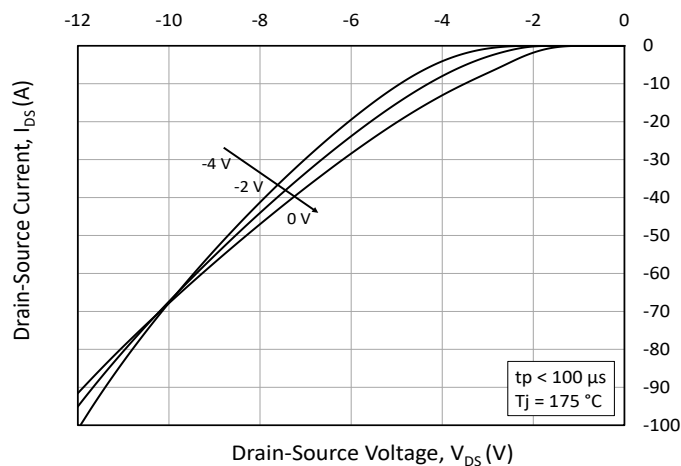


Figure 10. Body Diode Characteristic at 175 °C

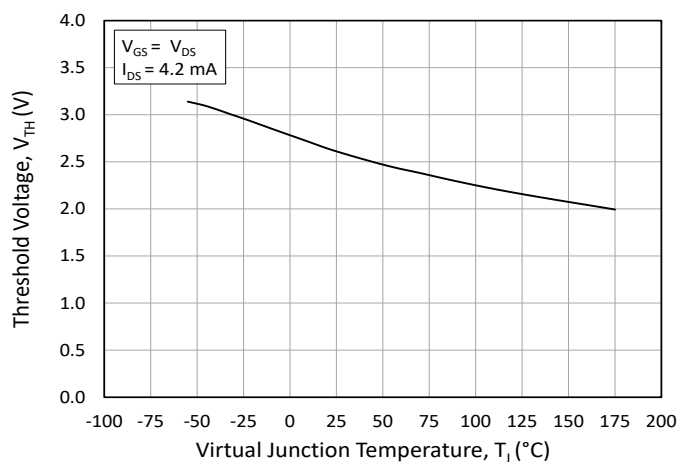


Figure 11. Threshold Voltage vs. Temperature

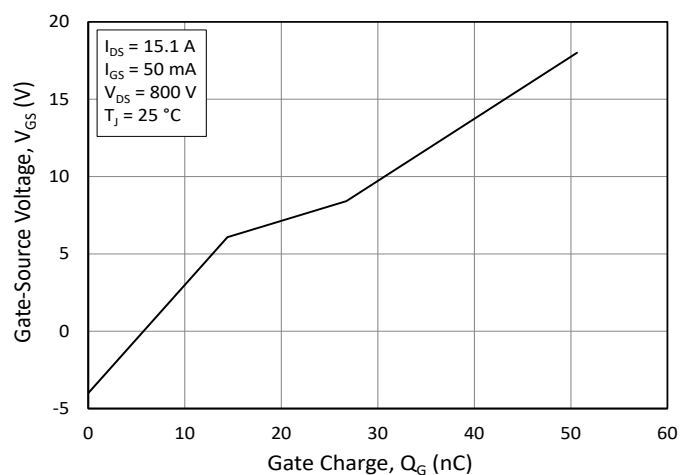


Figure 12. Gate Charge Characteristics

## Typical Performance

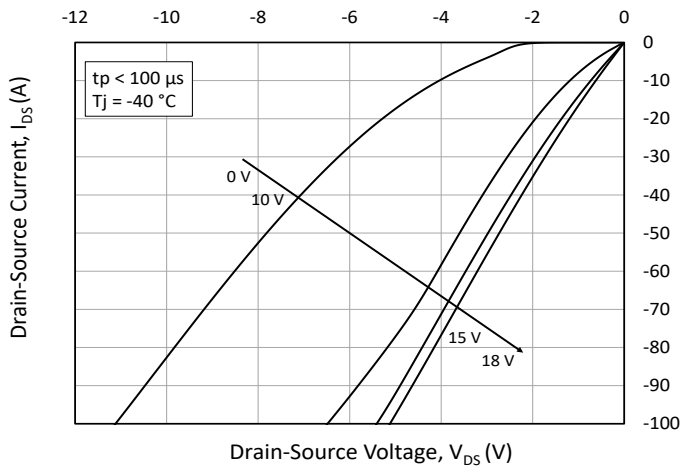


Figure 13. 3rd Quadrant Characteristic at -40°C

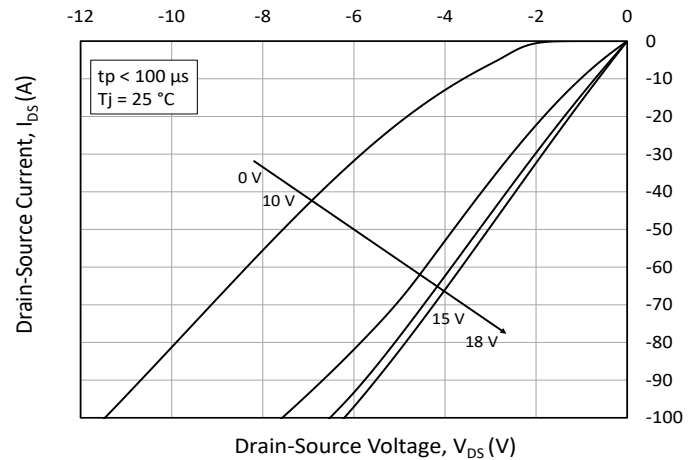


Figure 14. 3rd Quadrant Characteristic at 25°C

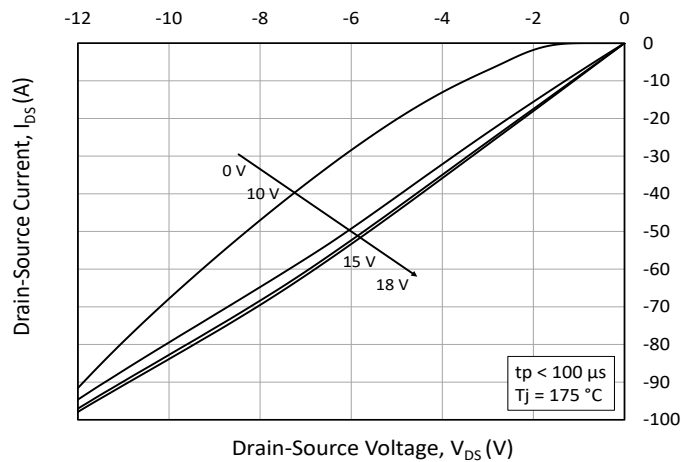


Figure 15. 3rd Quadrant Characteristic at 175°C

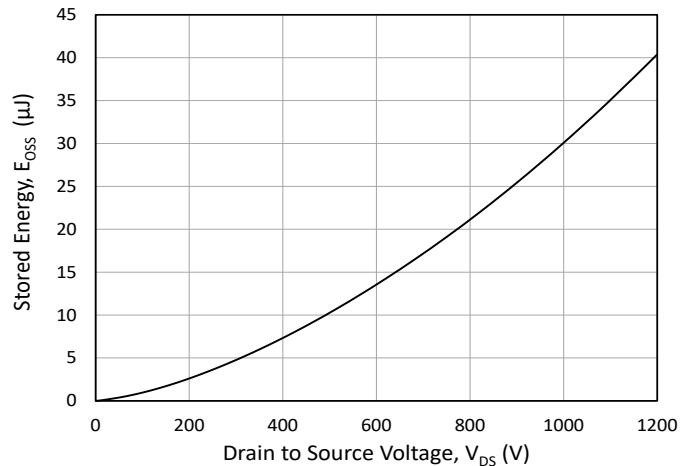


Figure 16. Output Capacitor Stored Energy

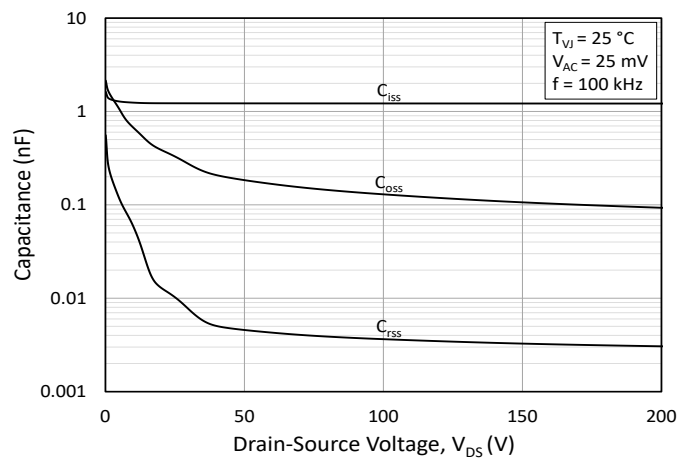


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

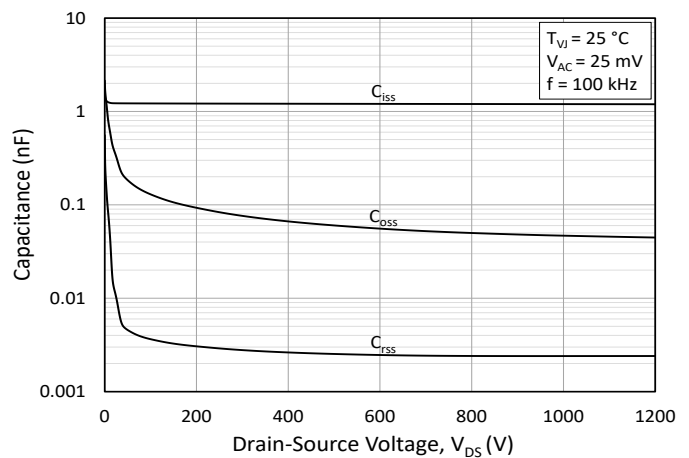


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200 V)

## Typical Performance

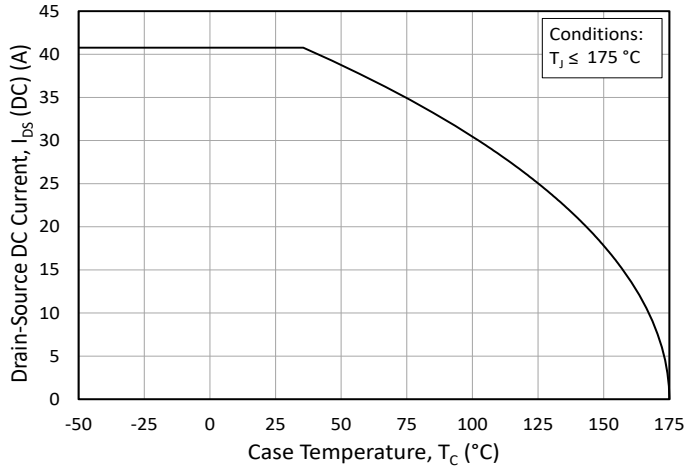


Figure 19. Continuous Drain Current Derating vs. Case Temperature

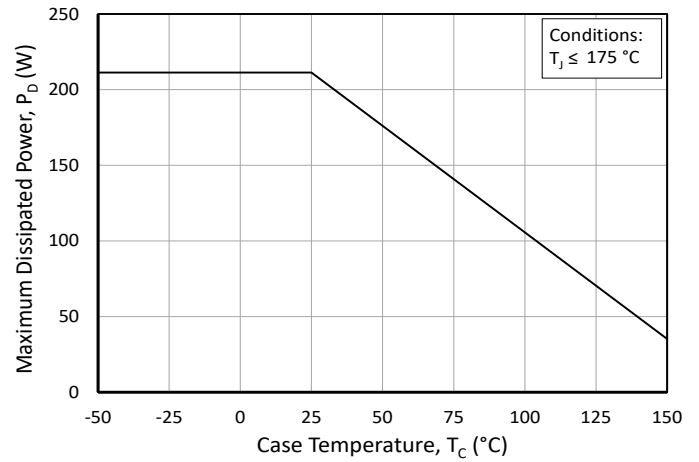


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

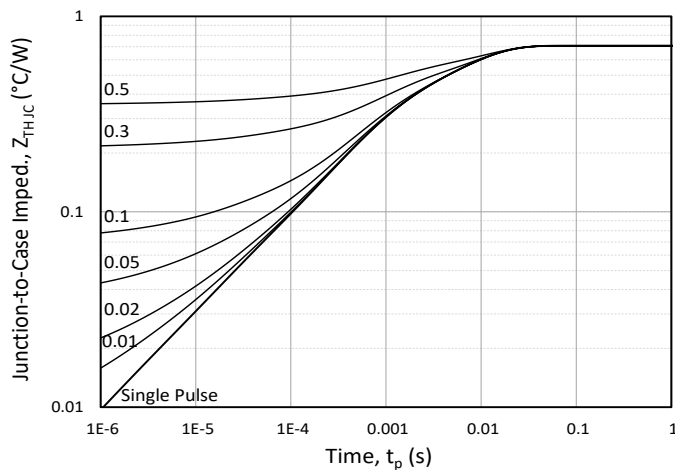


Figure 21. Transient Thermal Impedance (Junction - Case)

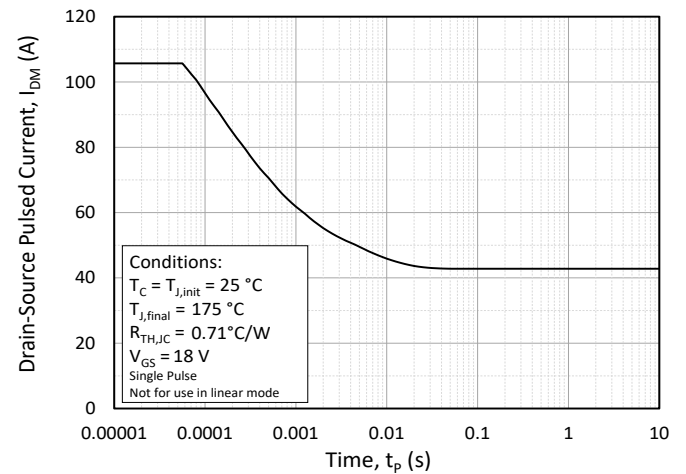
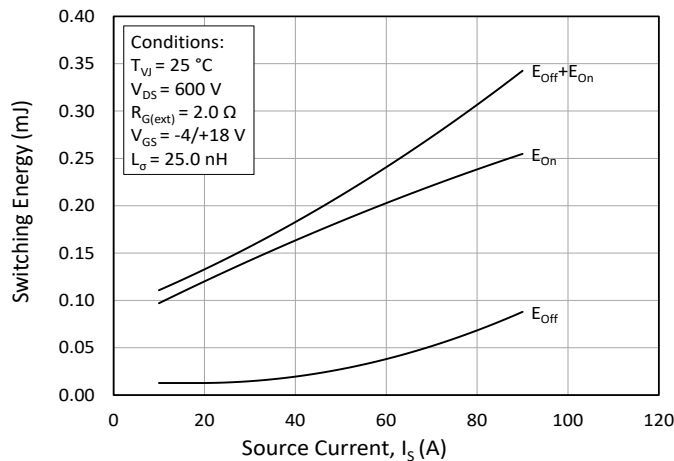
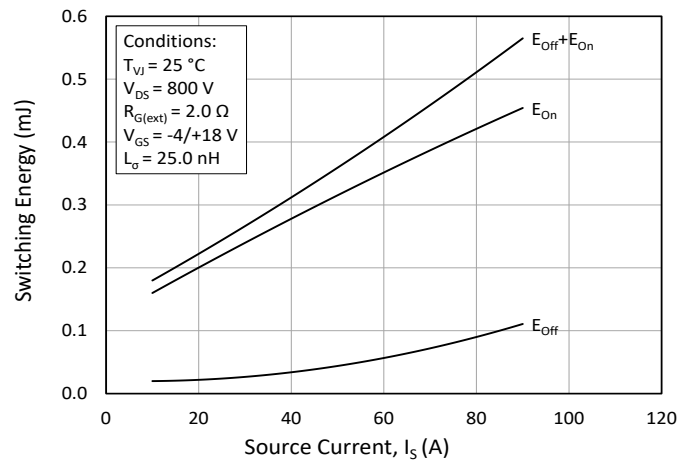


Figure 22. Safe Operating Area

Figure 23. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 600$  V)Figure 24. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 800$  V)

## Typical Performance

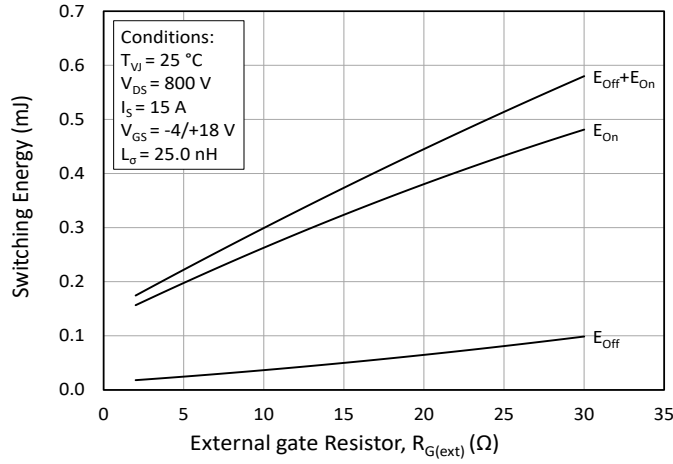
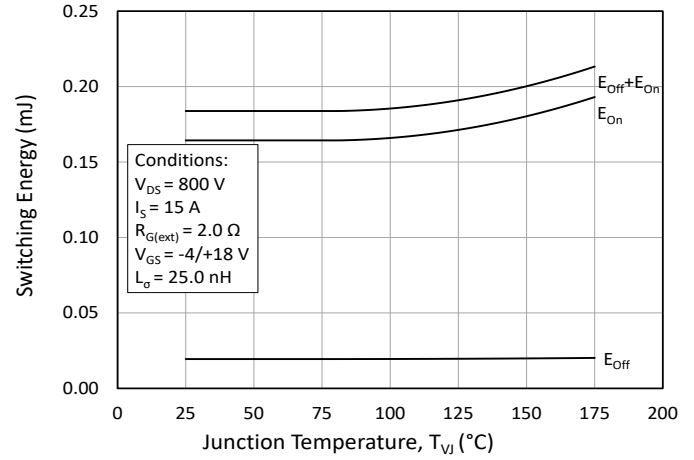
Figure 25. Clamped Inductive Switching Energy vs.  $R_{G(ext)}$ 

Figure 26. Clamped Inductive Switching Energy vs. Temperature

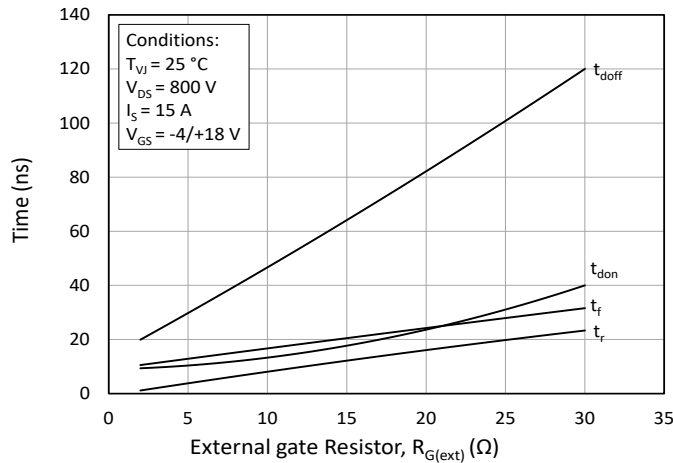
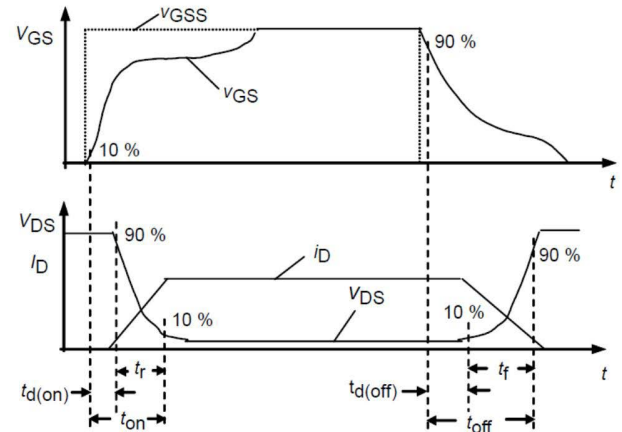
Figure 27. Switching Times vs.  $R_{G(ext)}$ 

Figure 28. Switching Times Definition

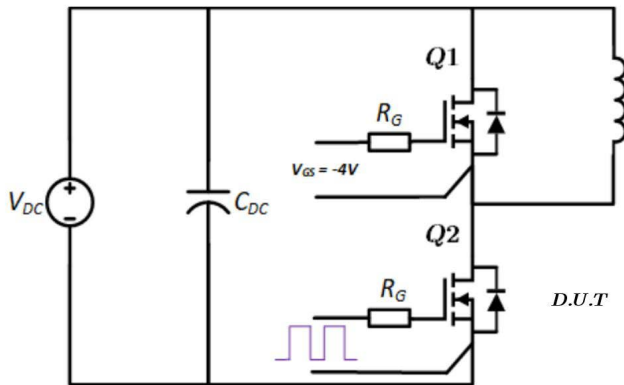


Figure 29. Clamped Inductive MOSFET Switching Waveform Test Circuit

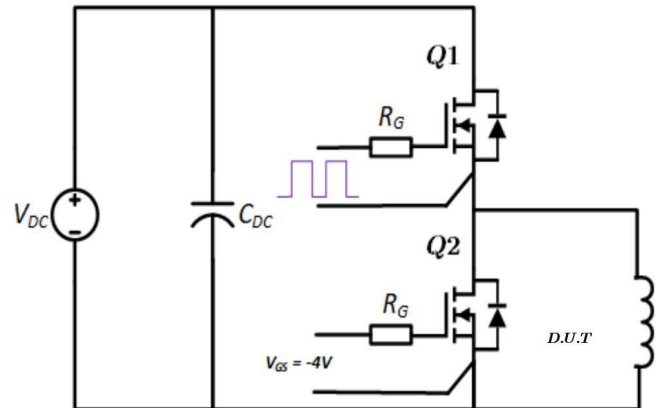
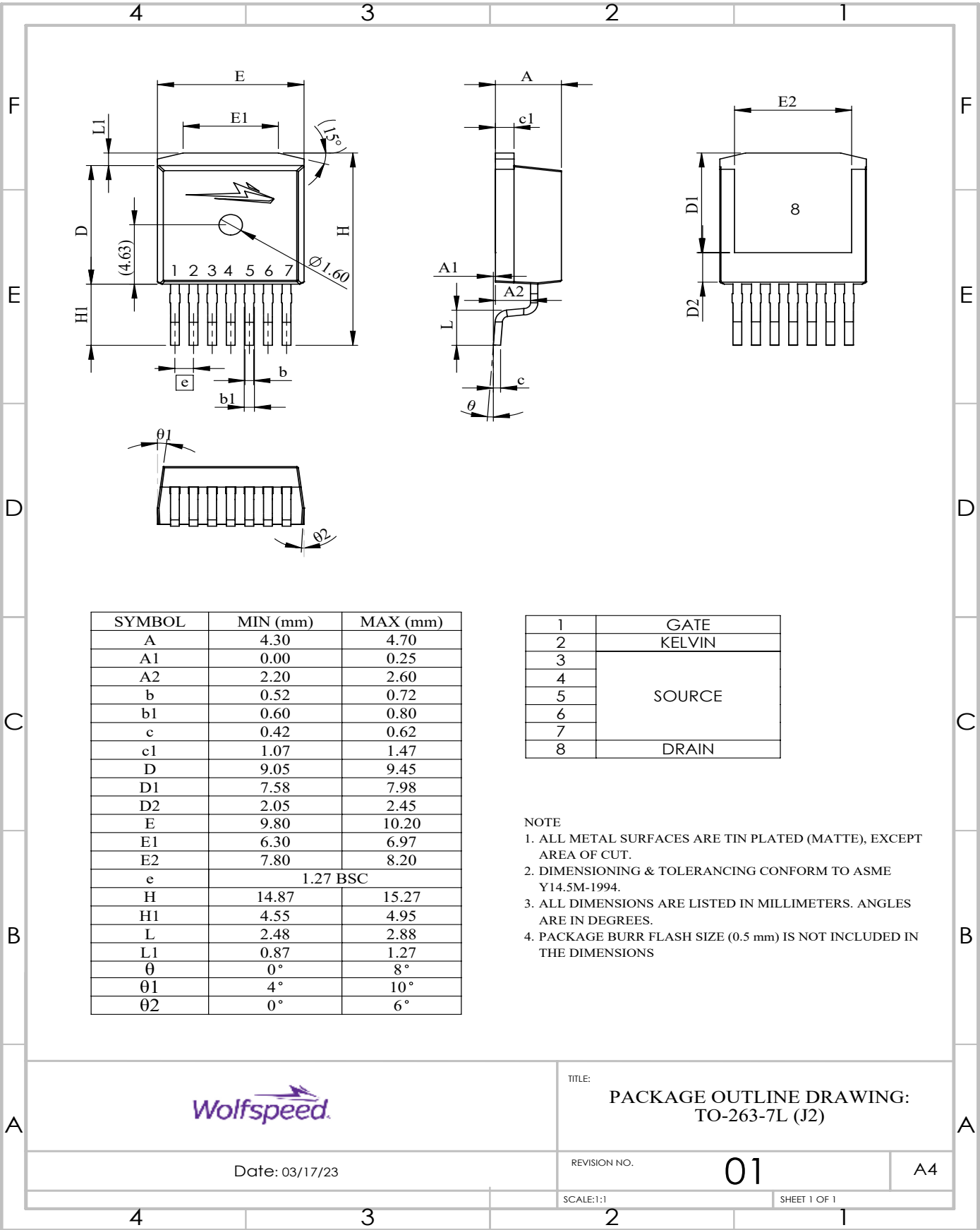


Figure 30. Clamped Inductive Body diode Switching Waveform Test Circuit

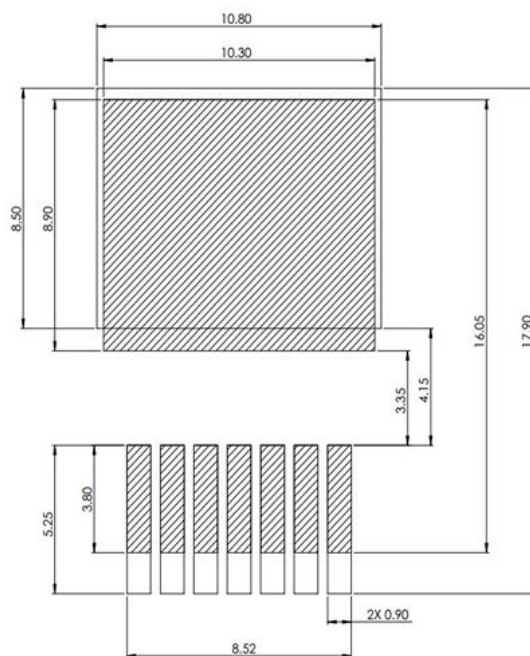


Package Dimensions



## Recommended Solder Pad Layout

All dimensions in mm



**Revision history**

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Document Version	Date of release	Description of changes
1	November 2025	Initial release
2	December 2025	Updated Note 2



## Notes & Disclaimer

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