

# C4MS065120J2

Silicon Carbide Power MOSFET  
Switching Optimized 1200V 65mΩ Industrial  
N-Channel Enhancement Mode

## Features

- Industry compatible drive voltage 15V...18V/-5V...0V
- Soft body diode with low  $V_{DS}$  overshoot and ringing
- Low  $R_{DS(on)}$  at high operating temperatures
- Improved device capacitances ratio ( $C_{iss}/C_{rss}$ )
- High transient voltage robustness with improved lifetime
- Halogen free, RoHS compliant

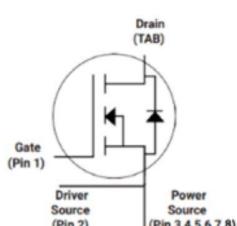
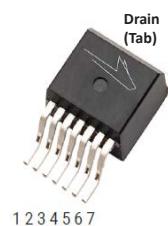
## Benefits

- Higher efficiency with lower switching losses and EMI
- Faster switching operation enabling high power density
- Enables system level price performance optimization
- Reduction in system level cooling requirements

## Typical Applications

- EV Chargers
- Solar/ESS
- Motor Control
- Industrial Power Supplies
- High Voltage DC/DC Converters

## Package



Orderable Part number	Package type	Marking
C4MS065120J2-TR	TO-263-7XL	C4MS065120J2

## Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	$V_{DS}$			1200	V		
Transient Drain - Source Voltage				1300		<100hrs of lifetime	Note 1
Maximum Gate - Source Voltage	$V_{GS(max)}$	-10		+23			Note 2
DC Continuous Drain Current	$I_D$		40		A	$V_{GS} = 18\text{ V}, T_c = 25\text{ °C}, T_j \leq 175\text{ °C}$	Note 3
			30			$V_{GS} = 18\text{ V}, T_c = 100\text{ °C}, T_j \leq 175\text{ °C}$	
Pulsed Drain Current	$I_{DM}$			105		$t_{Pmax}$ limited by $T_{jmax}$ $V_{GS} = 18\text{ V}, T_c = 25\text{ °C}$	
Power Dissipation	$P_D$		211		W	$T_c = 25\text{ °C}, T_j = 175\text{ °C}$	Note 4
Operating Junction and Storage Temperature	$T_j, T_{stg}$	-40		+175	°C		
Solder Temperature	$T_L$			260		According to JEDEC J-STD-020	

Note (1): 100 hours of total accumulated lifetime of the product.

Note (2): When applying IPC-9592B or OCP M-CRPS derating standards, a maximum Gate-Source voltage ( $V_{GS}$ ) of +25V is permissible.

Note (3): Current limit calculated by  $I_{D(max)} = \sqrt{(P_D / R_{DS(typ)})(T_{j(max)} / I_{D(max)})}$

Note(4):  $P_D = (T_j - T_c) / R_{th(jc,typ)}$


**Electrical Characteristics (T<sub>c</sub> = 25°C unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	1200			V	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 100 μA	
V <sub>GS(th)</sub>	Gate Threshold Voltage	2	2.6	3.9	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 4.16 mA	Fig. 11
			2.0		V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 4.16 mA, T <sub>J</sub> = 175°C	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current		1	50	μA	V <sub>DS</sub> = 1200 V, V <sub>GS</sub> = 0 V	
I <sub>GSS</sub>	Gate-Source Leakage Current		10	250	nA	V <sub>GS</sub> = 18 V, V <sub>DS</sub> = 0 V	
V <sub>GS(op)</sub>	Recommended Turn on Gate-Source Voltage	+15...+18			V		Refer to PRD-09634
	Recommended Turn off Gate-Source Voltage	-5...0					
R <sub>DS(on)</sub>	Drain-Source On-State Resistance		65	85	mΩ	V <sub>GS</sub> = 18 V, I <sub>D</sub> = 15.1 A	Fig. 4, 5, 6
			116			V <sub>GS</sub> = 18 V, I <sub>D</sub> = 15.1 A, T <sub>J</sub> = 175°C	
			71			V <sub>GS</sub> = 15 V, I <sub>D</sub> = 15.1 A	
g <sub>fs</sub>	Transconductance		11		S	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 15.1 A, T <sub>J</sub> = 25°C	Fig. 7
			10			V <sub>DS</sub> = 20 V, I <sub>D</sub> = 15.1 A, T <sub>J</sub> = 175°C	
R <sub>DS(on)Tempco</sub>	On resistance temperature coefficient		1.88			V <sub>GS</sub> = 18 V, I <sub>D</sub> = 15.1 A	Note 5
C <sub>iss</sub>	Input Capacitance		1225		pF	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 1000 V f = 100 kHz V <sub>AC</sub> = 25 mV	Fig. 17, 18
C <sub>oss</sub>	Output Capacitance		47				
C <sub>rss</sub>	Reverse Transfer Capacitance		2.4				
C <sub>iss/C<sub>rss</sub></sub>	Capacitance Ratio		630				
E <sub>oss</sub>	C <sub>oss</sub> Stored Energy		30		μ		Fig. 16
C <sub>o(er)</sub>	Effective Output Capacitance (Energy Related)		68		pF	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0...800 V	
C <sub>o(tr)</sub>	Effective Output Capacitance (Time Related)		108				
E <sub>on</sub>	Turn-On Switching Energy (Body Diode FWD)				μ	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = -4 V/18 V, I <sub>D</sub> = 15.1 A, R <sub>G(ext)</sub> = 2Ω, L <sub>σ</sub> = 25 nH	Fig. 26, 29, 31
	T <sub>J</sub> =25C		164				
E <sub>off</sub>	T <sub>J</sub> =175C		193				
	Turn-Off Switching Energy (Body Diode FWD)						
E <sub>off</sub>	T <sub>J</sub> =25C		19		ns	V <sub>DD</sub> = 800 V, V <sub>GS</sub> = -4 V/18 V I <sub>D</sub> = 15.1 A, R <sub>G(ext)</sub> = 2Ω, Timing relative to V <sub>DS</sub> Inductive load	Fig. 26, 29, 32
	T <sub>J</sub> =175C		20				
t <sub>d(on)</sub>	Turn-On Delay Time		9				
t <sub>r</sub>	Rise Time		2				
t <sub>d(off)</sub>	Turn-Off Delay Time		21		nC	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = -4 V/18 V I <sub>D</sub> = 15.1 A, T <sub>J</sub> = 25°C Per IEC60747-8-4 pg 21	Fig. 27, 28
t <sub>f</sub>	Fall Time		10				
R <sub>G(int)</sub>	Internal Gate Resistance		3.1		Ω	f = 1 MHz	
Q <sub>gs</sub>	Gate to Source Charge		14				
Q <sub>gd</sub>	Gate to Drain Charge		12				Fig. 12
Q <sub>g</sub>	Total Gate Charge		51				

Note (5): R<sub>DS(on)Tempco</sub> refers to R<sub>DS(on)</sub> at 175°C / R<sub>DS(on)</sub> at 25°C, C4MS 1200V product family value

Note (6): Capacitance ratio is a FOM for Partial turn-on immunity PRD-09633, C4MS 1200V product family value

Co(er), a lumped capacitance that gives the same stored energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 800V

Co(tr), a lumped capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 800V



### Reverse Diode Characteristics ( $T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$V_{SD}$	Diode Forward Voltage	5.1		V	$V_{GS} = -4\text{ V}$ , $I_{SD} = 7.6\text{ A}$ , $T_j = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.5		V	$V_{GS} = -4\text{ V}$ , $I_{SD} = 7.6\text{ A}$ , $T_j = 175^\circ\text{C}$	
$I_s$	Continuous Diode Forward Current	30		A	$V_{GS} = -4\text{ V}$ , $T_c = 25^\circ\text{C}$	
$I_{SM}$	Diode Pulse Current		105	A	$V_{GS} = -4\text{ V}$ , pulse width $t_p$ limited by $T_{jmax}$	
$t_{rr}$	Reverse Recovery Time	11		ns	$V_{GS} = -4\text{ V}$ , $I_s = 15.1\text{ A}$ , $V_{SD} = 800\text{V}$ $T_j = 175^\circ\text{C}$ , $dI/dt = 12.1\text{ A/ns}$	
$Q_{rr}$	Reverse Recovery Charge	325		nC		
$I_{RRM}$	Peak Reverse Recovery current	57		A		
$E_{RR}$	Reverse recovery Energy			$\mu\text{J}$	$V_{DS} = 800\text{ V}$ , $I_D = 15.1\text{ A}$ ,	
	Tj=25C	45			$V_{GS} = -4\text{V}/18\text{V}$ , $R_{G(on)} = 2\Omega$ , $L\sigma = 25\text{nH}$	
	Tj= 175C	87				

### Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.71	°C/W		

## Typical Performance

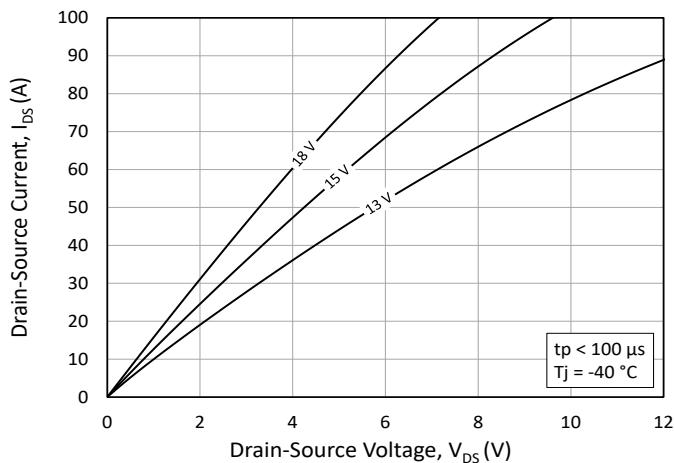
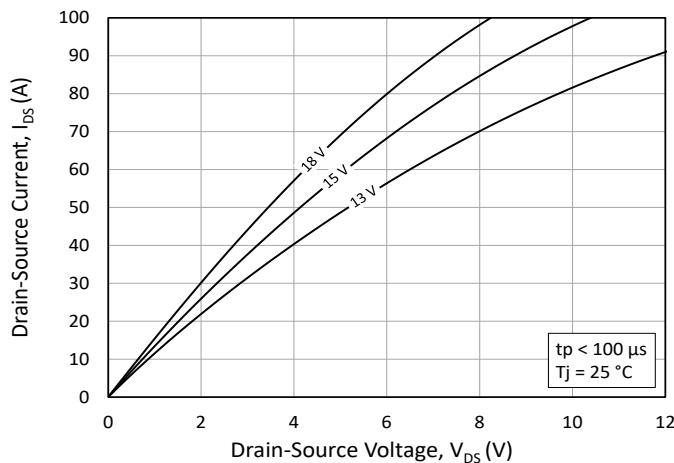
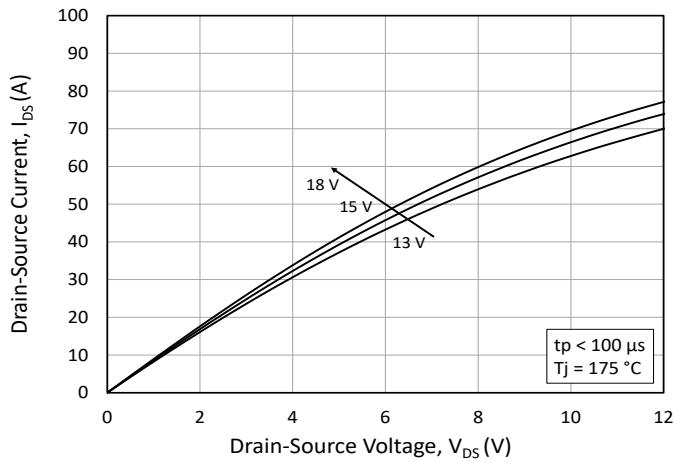
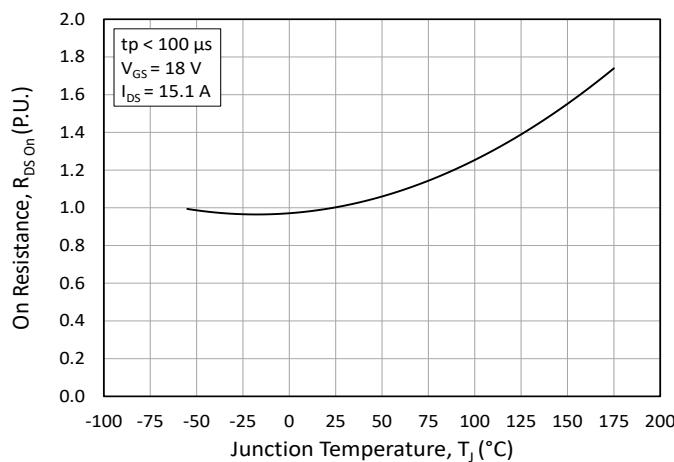
Figure 1. Output Characteristics  $T_j = -40^\circ\text{C}$ Figure 2. Output Characteristics  $T_j = 25^\circ\text{C}$ Figure 3. Output Characteristics  $T_j = 175^\circ\text{C}$ 

Figure 4. Normalized On-Resistance vs. Temperature

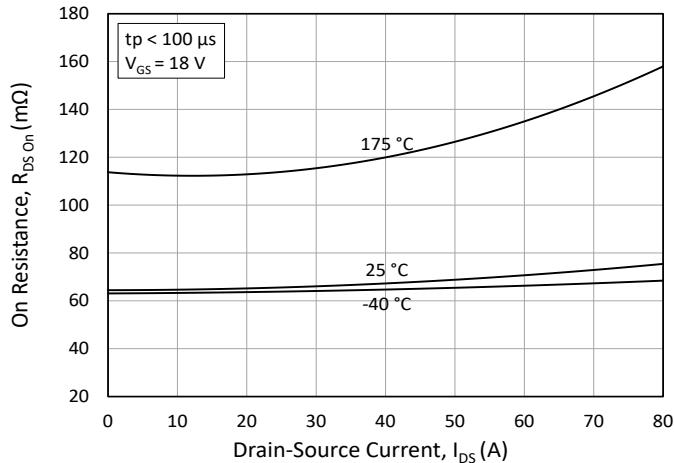


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

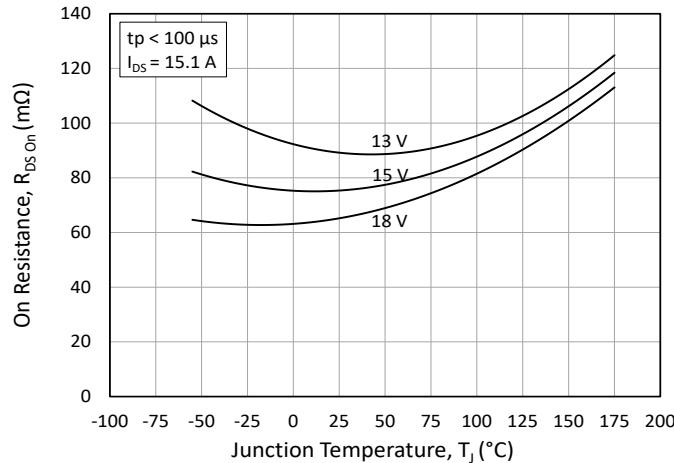
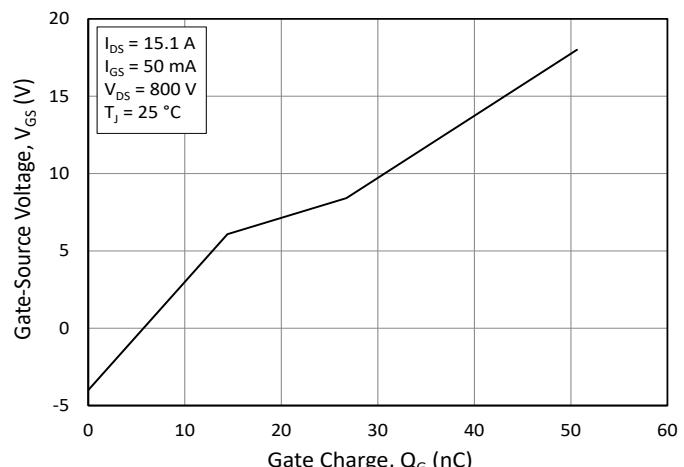
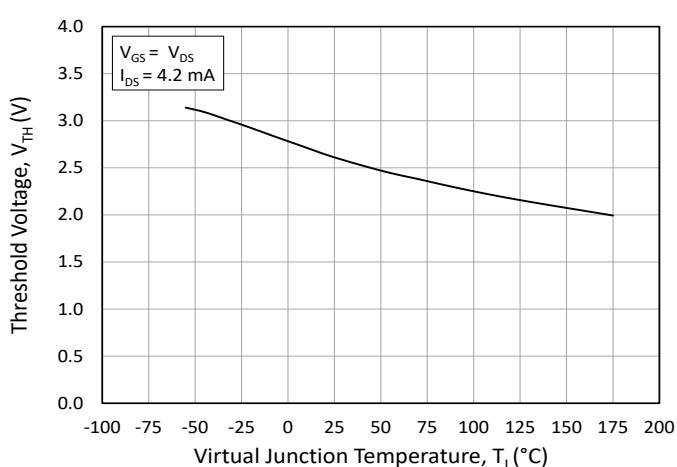
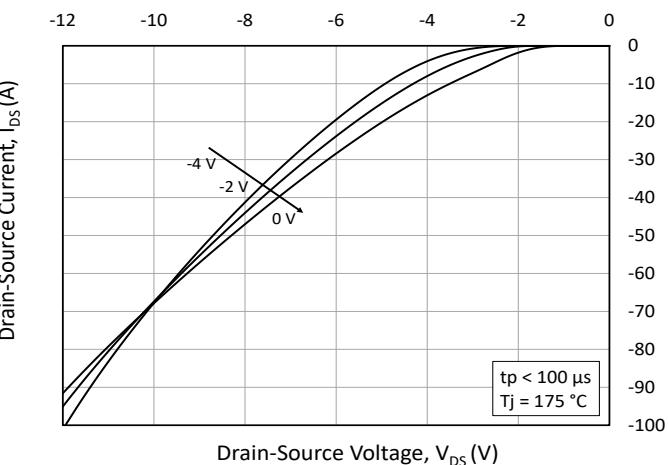
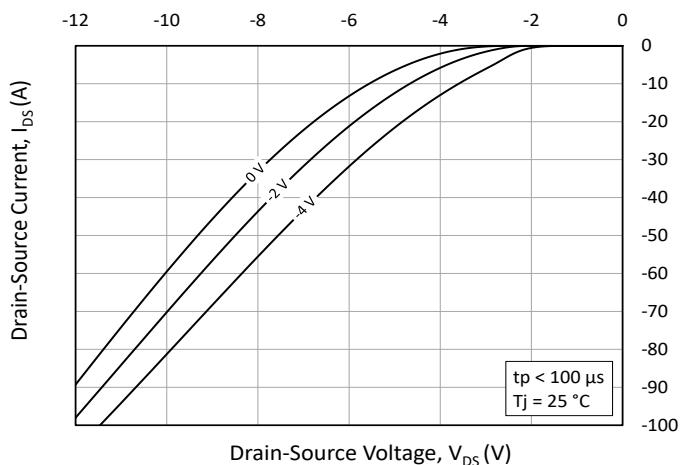
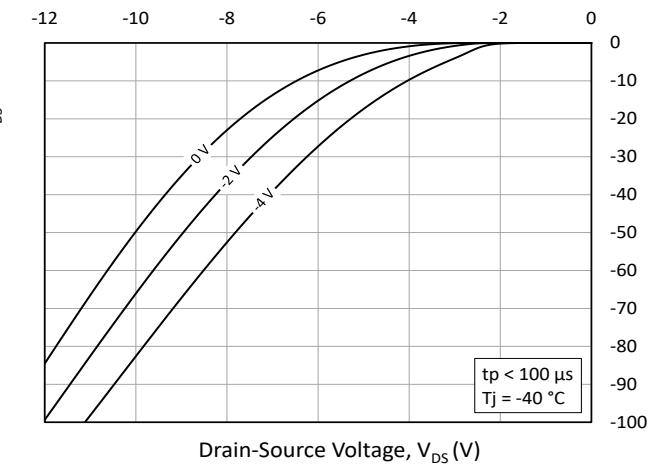
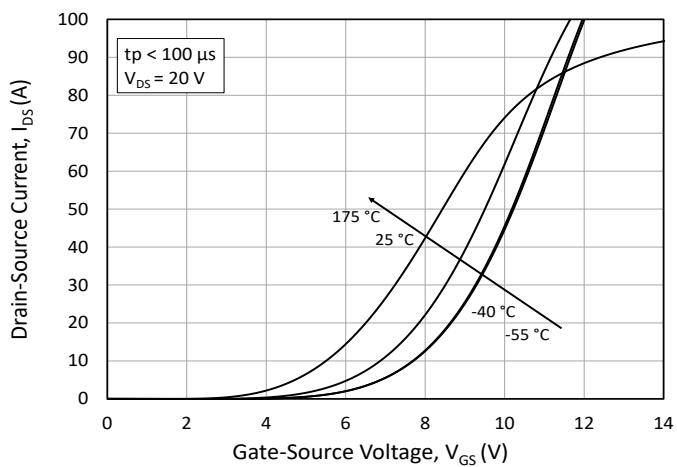


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

## Typical Performance



## Typical Performance

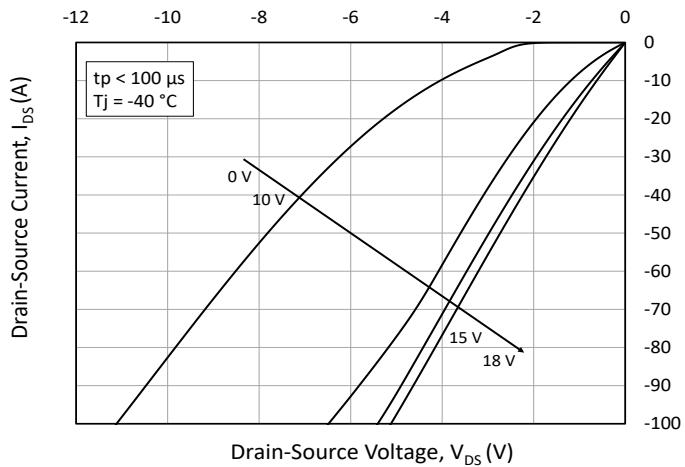
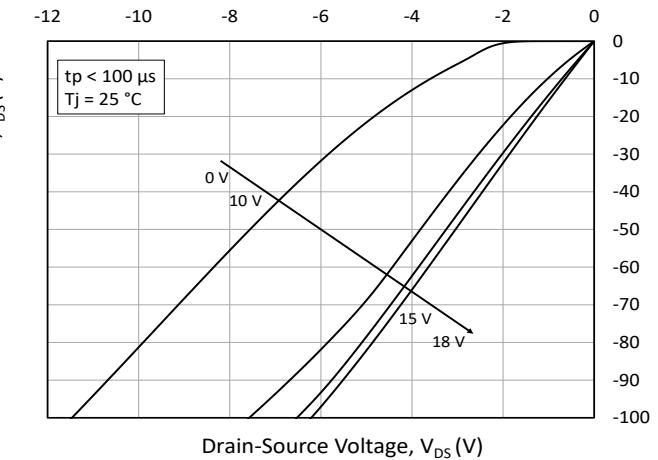
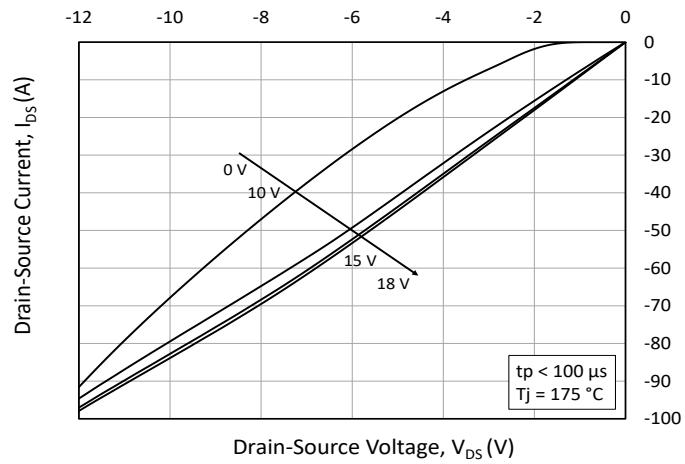
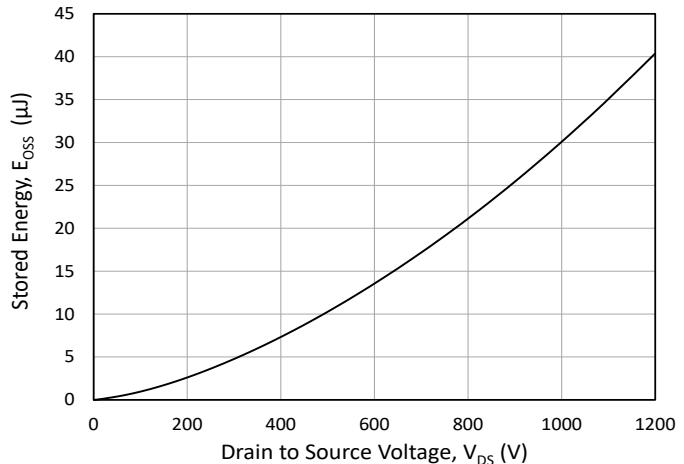
Figure 13. 3rd Quadrant Characteristic at  $-40^{\circ}\text{C}$ Figure 14. 3rd Quadrant Characteristic at  $25^{\circ}\text{C}$ Figure 15. 3rd Quadrant Characteristic at  $175^{\circ}\text{C}$ 

Figure 16. Output Capacitor Stored Energy

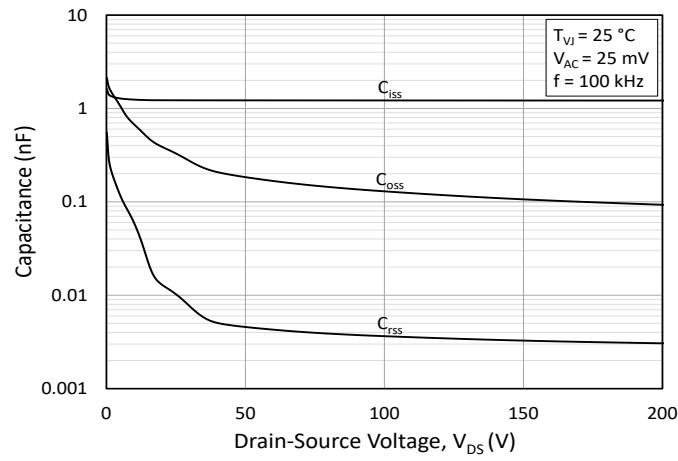


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

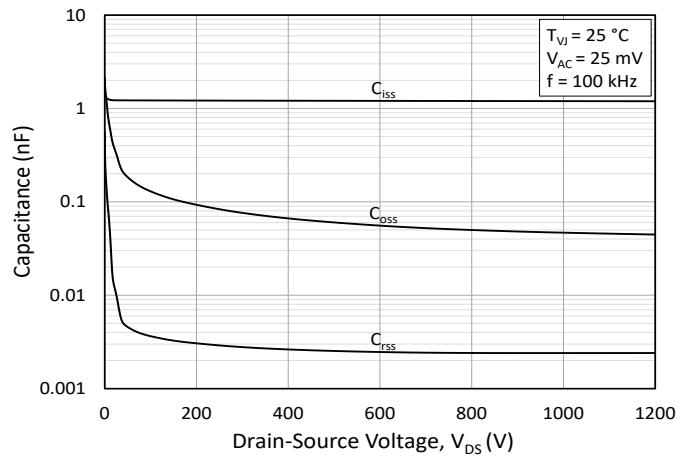


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200 V)

## Typical Performance

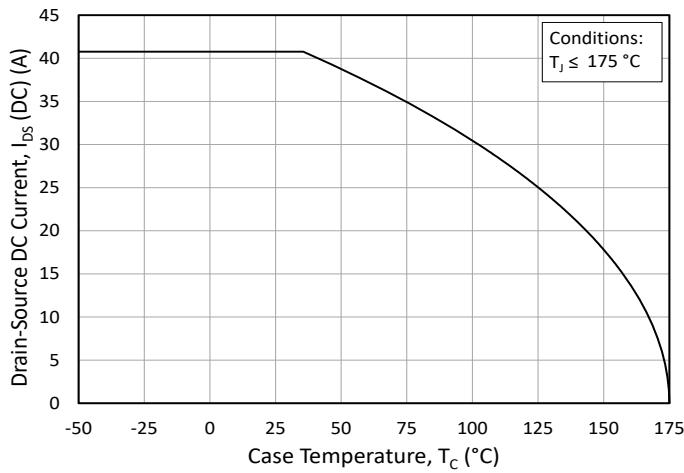


Figure 19. Continuous Drain Current Derating vs. Case Temperature

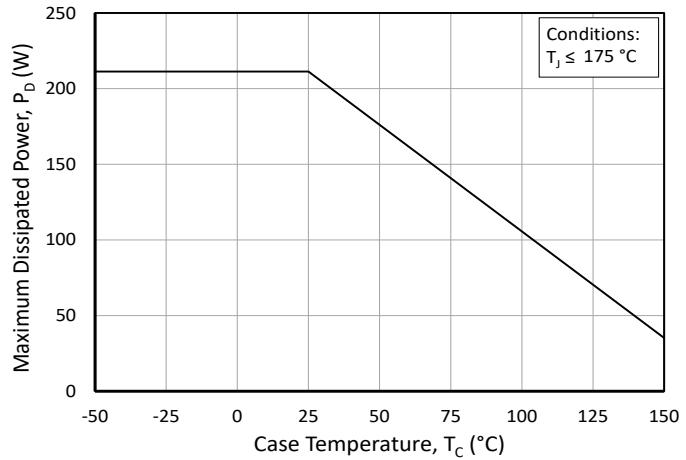


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

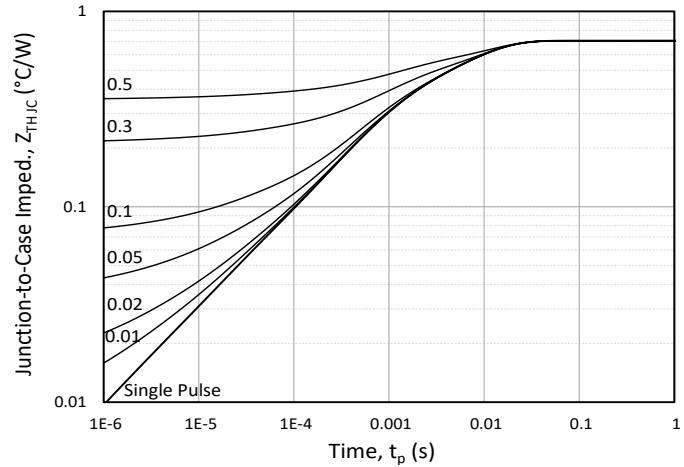


Figure 21. Transient Thermal Impedance (Junction - Case)

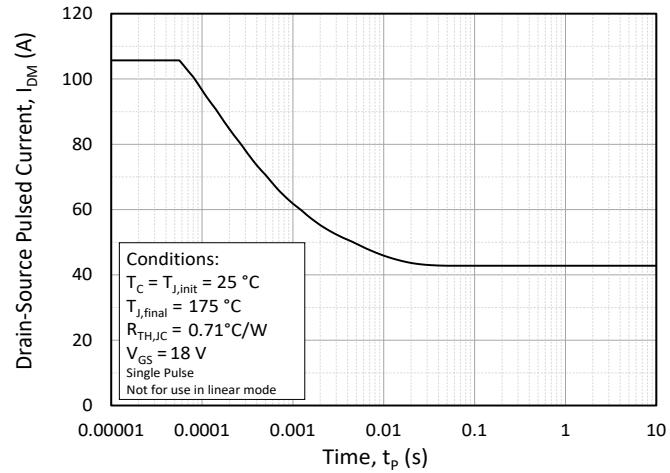


Figure 22. Safe Operating Area

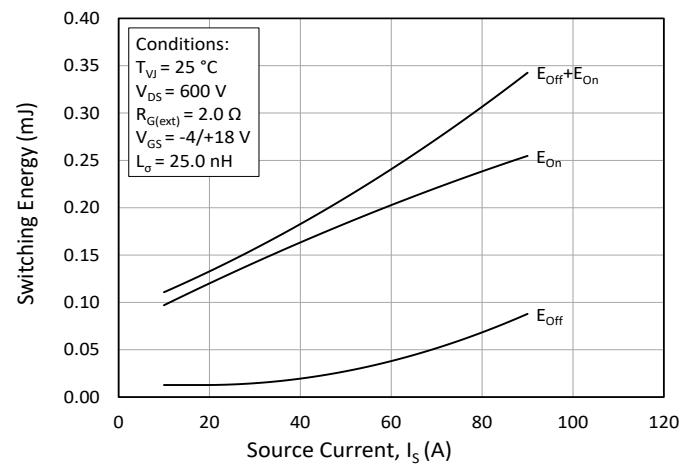


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 600$  V)

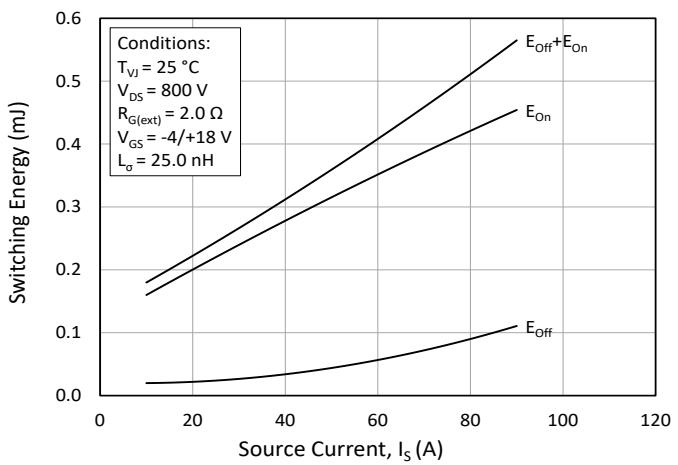


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 800$  V)

## Typical Performance

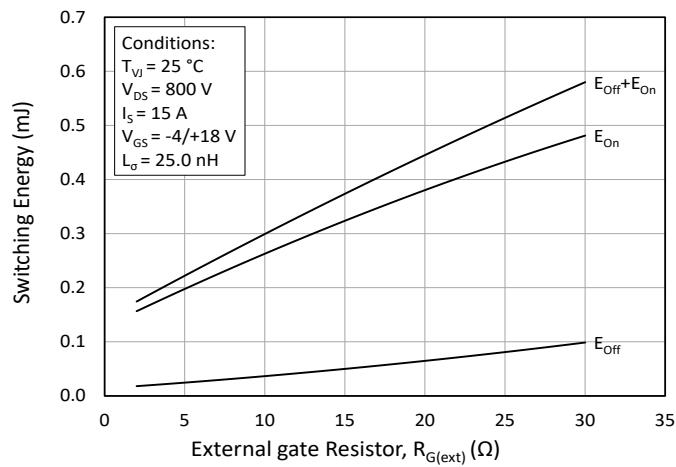
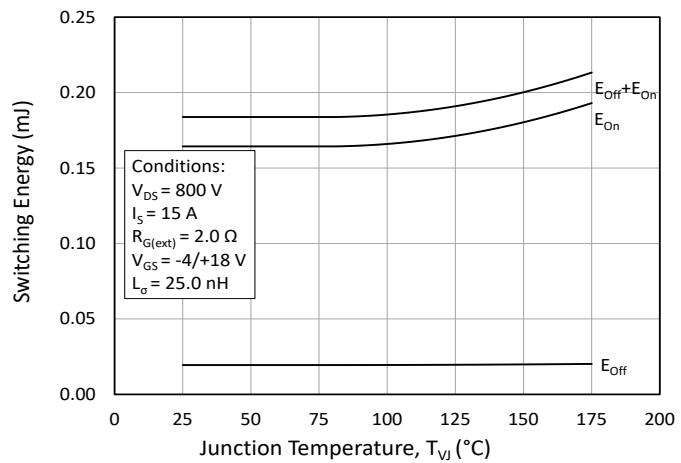
Figure 25. Clamped Inductive Switching Energy vs.  $R_{G(\text{ext})}$ 

Figure 26. Clamped Inductive Switching Energy vs. Temperature

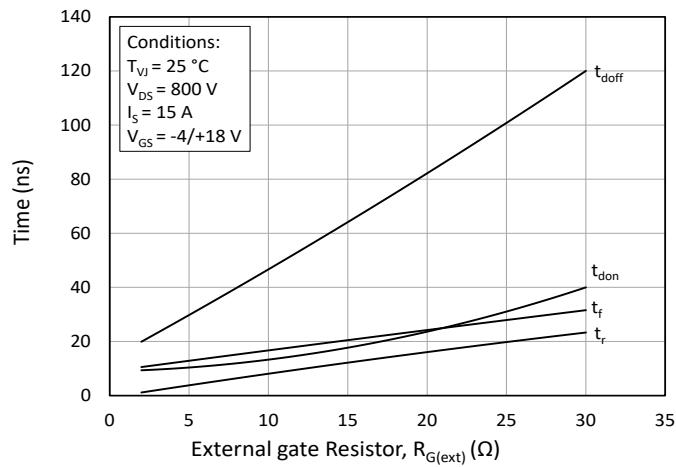
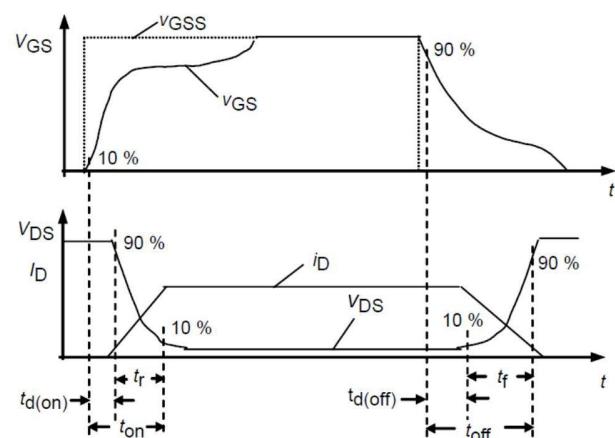
Figure 27. Switching Times vs.  $R_{G(\text{ext})}$ 

Figure 28. Switching Times Definition

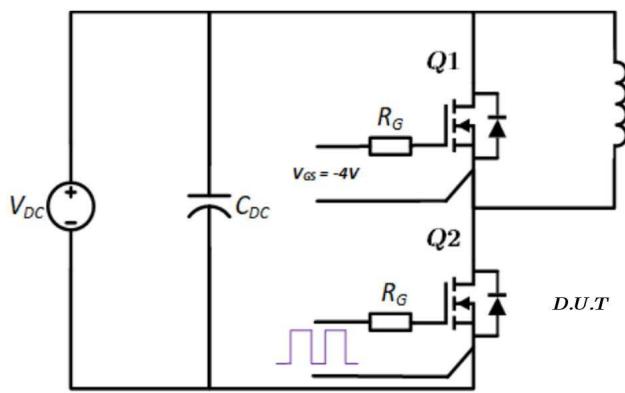


Figure 29. Clamped Inductive MOSFET Switching Waveform Test Circuit

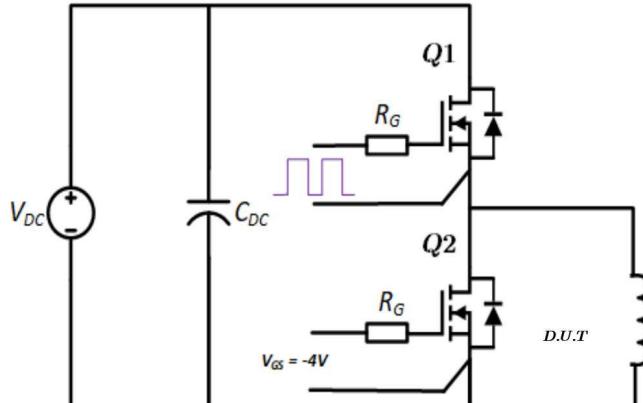
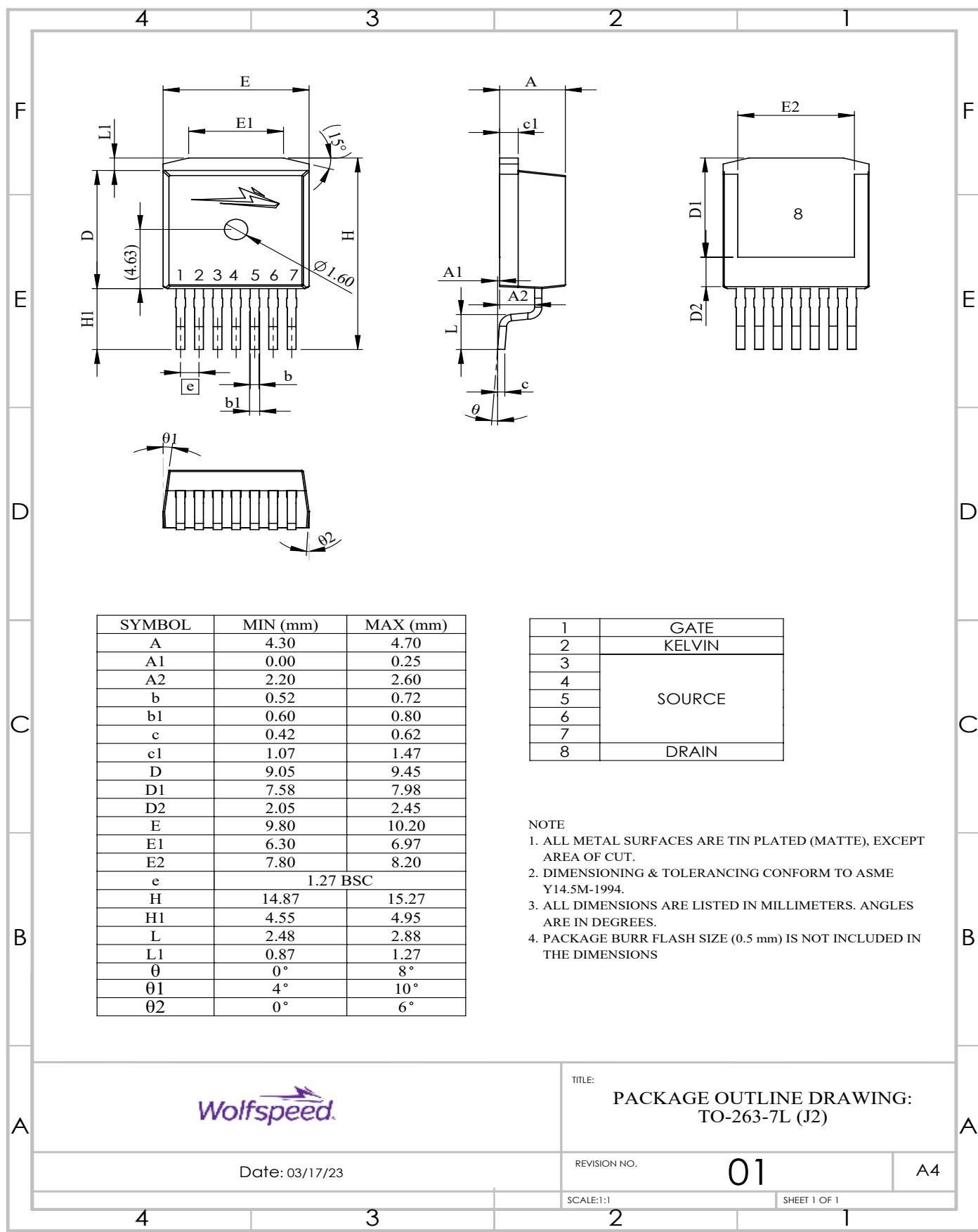


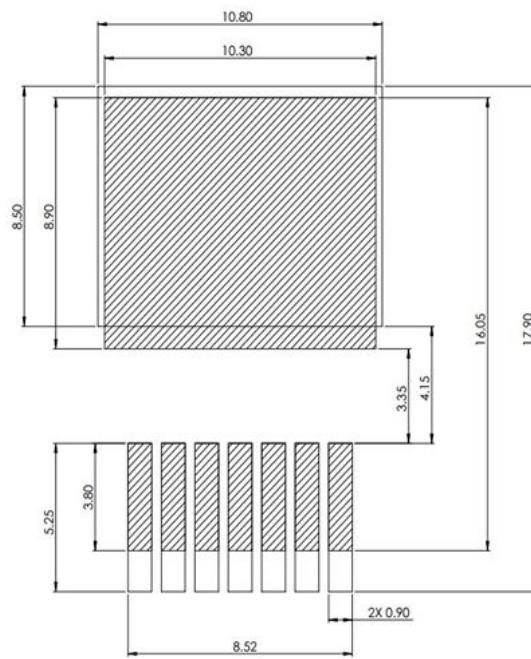
Figure 30. Clamped Inductive Body diode Switching Waveform Test Circuit

## Package Dimensions



**Recommended Solder Pad Layout**

All dimensions in mm



Revision history

Document Version	Date of release	Description of changes
1	November 2025	Initial release
2	December 2025	Updated Note 2



## Notes & Disclaimer

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