C4MS036120K

Silicon Carbide Power MOSFET
Switching Optimized 1200V 36mΩ Industrial
N-Channel Enhancement Mode

Features

- Industry compatible drive voltage 15V...18V/-5V...0V
- Soft body diode with low Vds overshoot and ringing
- Low Rds(on) at high operating temperatures
- Improved device capacitances ratio (Ciss/Crss)
- High transient voltage robustness with improved lifetime
- Halogen free, RoHS compliant

Benefits

- Higher efficiency with lower switching losses and EMI
- Faster switching operation enabling high power density
- Enables system level price performance optimization
- Reduction in system level cooling requirements

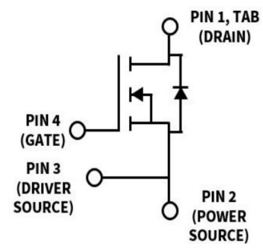
Typical Applications

- EV Chargers
- Solar/ESS
- Motor Control
- Industrial Power Supplies
- High Voltage DC/DC Converters

Package

Halogen-Free F Cl Br I

RoHS compliant



Orderable Part number	Package type	Marking
C4MS036120K	TO-247-4	C4MS036120K

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1200	V		
Transient Drain - Source Voltage				1300		<100hrs of lifetime	Note 1
Maximum Gate - Source Voltage	$V_{GS(max)}$	-10		+23			Note 2
DC Continuous Drain Current	I_D		60		A	V_{GS} = 18 V, T_C = 25 °C, T_J ≤175 °C	Note 3
			44			V_{GS} = 18 V, T_C = 100 °C, T_J ≤175 °C	
Pulsed Drain Current	I_{DM}			193		t_{Pmax} limited by T_{jmax} V_{GS} = 18V, T_C = 25 °C	
Power Dissipation	P_D		272		W	T_C = 25˚C, T_J = 175 °C	Note 4
Operating Junction and Storage Temperature	T_J, T_{stg}	-40		+175	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	

Note (1): 100 hours of total accumulated lifetime of the product.
Note (2): When applying IPC-9592B or OCP M-CRPS derating standards, a maximum Gate-Source voltage (Vgs) of +25V is permissible.
Note (3): Current limit calculated by $I_{D(max)}=\sqrt{(P_D/R_{DS(typ)}(T_{J(max)},I_{D(max)}))}$
Note(4): $P_D=(T_J-T_C)/R_{th(JC,typ)}$

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Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	2	2.6	3.9	V	V_{DS} = V_{GS}, I_D = 7.6 mA	Fig. 11
			2.0		V	V_{DS} = V_{GS}, I_D = 7.6 mA, T_J = 175°C	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 18 V, V_{DS} = 0 V	
$V_{GS(op)}$	Recommended Turn on Gate-Source Voltage		+15...+18		V		Refer to PRD-09634
	Recommended Turn off Gate-Source Voltage		-5...0				
$R_{DS(on)}$	Drain-Source On-State Resistance		36	47	mΩ	V_{GS} = 18 V, I_D = 27.6 A	Fig. 4, 5, 6
			66			V_{GS} = 18 V, I_D = 27.6 A, T_J = 175ºC	
			42			V_{GS} = 15 V, I_D = 27.6 A	
g_{fs}	Transconductance		20		S	V_{DS} = 20 V, I_D = 27.6 A, T_J = 25ºC	Fig. 7
			19			V_{DS} = 20 V, I_D = 27.6 A, T_J = 175ºC	
$R_{DS(on)Tempco}$	On resistance temperature coefficient		1.88			V_{GS} = 18 V, I_D = 27.6 A	Note 5
C_{iss}	Input Capacitance		2164		pF	V_{GS} = 0 V, V_{DS} = 1000 V f = 100 kHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		72				
C_{rss}	Reverse Transfer Capacitance		3.2				
C_{iss}/C_{rss}	Capacitance Ratio		630				Note 6
E_{oss}	C_{oss} Stored Energy		46		μJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		106		pF	V_{GS}= 0V, V_{DS}= 0...800V	
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		173				
E_{on}	Turn-On Switching Energy (Body Diode FWD) Tj=25C Tj=175C		 303 393		μJ	V_{DS} = 800 V, V_{GS} = -4 V/18 V, I_D = 27.6A, $R_{G(ext)}$ = 2Ω, Lσ =25nH	Fig. 26, 29, 31
E_{off}	Turn-Off Switching Energy (Body Diode FWD) Tj=25C Tj=175C		 18 26				Fig. 26, 29, 32
$t_{d(on)}$	Turn-On Delay Time		12		ns	V_{DD} = 800 V, V_{GS} = -4 V/18 V I_D = 27.6 A, $R_{G(ext)}$ = 2 Ω, Timing relative to V_{DS} Inductive load	Fig. 27, 28
t_r	Rise Time		3				
$t_{d(off)}$	Turn-Off Delay Time		29				
t_f	Fall Time		4				
$R_{G(int)}$	Internal Gate Resistance		2.4		Ω	f = 1 MHz	
Q_{gs}	Gate to Source Charge		24		nC	V_{DS} = 800 V, V_{GS} = -4 V/18 V I_D = 27.6 A, T_J = 25ºC Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		23				
Q_g	Total Gate Charge		88				

Note (5): $R_{DS(on)Tempco}$ refers to $R_{DS(on)}$ at 175 C/ $R_{DS(on)}$ at 25C, C4MS 1200V product family value
Note (6): Capacitance ratio is a FOM for Partial turn-on immunity PRD-06933, C4MS 1200V product family value

Co(er), a lumped capacitance that gives the same stored energy as Coss while Vds is rising from 0 to 800V
Co(tr), a lumped capacitance that gives the same charging time as Coss while Vds is rising from 0 to 800V

Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.2		V	V_{GS} = -4 V, I_{SD} = 13.8 A, T_J = 25 °C	Fig. 8, 9, 10
		4.6		V	V_{GS} = -4 V, I_{SD} = 13.8 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current	40		A	V_{GS} = -4 V, T_C = 25˚C	
I_{SM}	Diode Pulse Current		193	A	V_{GS} = -4 V, pulse width t_p limited by T_{jmax} max	
t_{rr}	Reverse Recovery Time	11		ns	V_{GS}=-4 V, I_S =27.6 A, V_{SD} =800V T_J =175ºC, diF/dt= 7.6 A/ns	
Q_{rr}	Reverse Recovery Charge	335		nC		
I_{RRM}	Peak Reverse Recovery current	49		A		
E_{RR}	Reverse recovery Energy Tj=25C Tj= 175C	 29 35		µJ	V_{DS}=800 V, I_D =27.6 A, V_{GS}=-4V/18V, $R_{G(on)}$ =2 Ω, Lσ =25nH	

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.55	°C/W		

Typical Performance

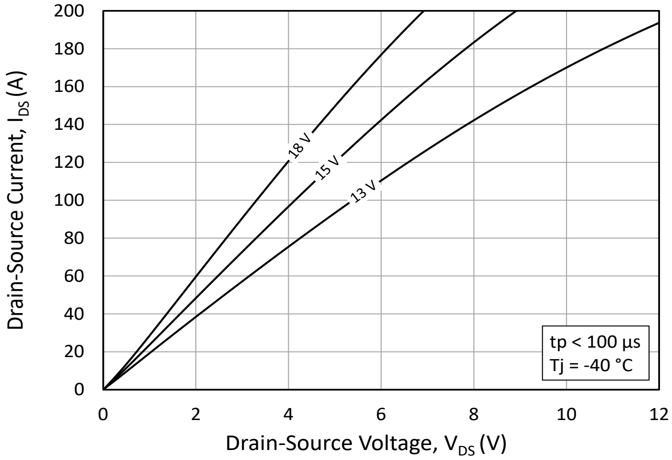


Figure 1. Output Characteristics T_J = -40°C

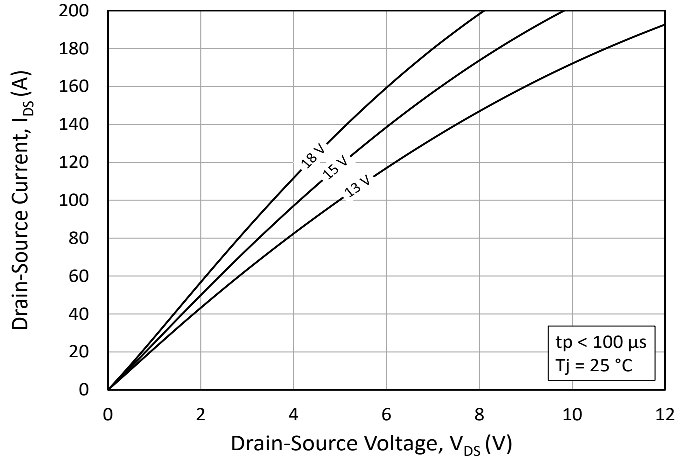


Figure 2. Output Characteristics T_J = 25°C

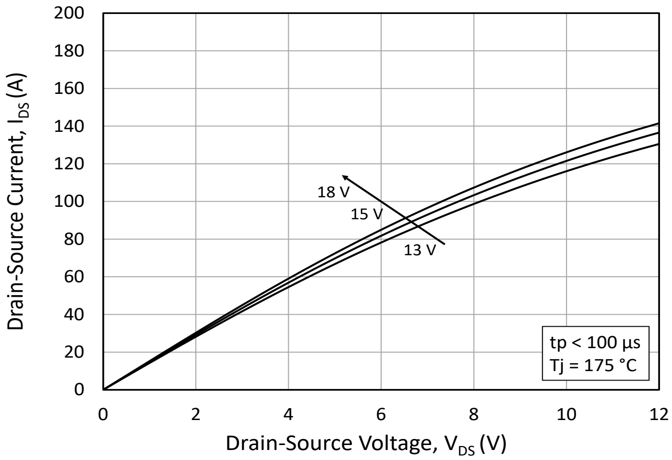


Figure 3. Output Characteristics T_J = 175°C

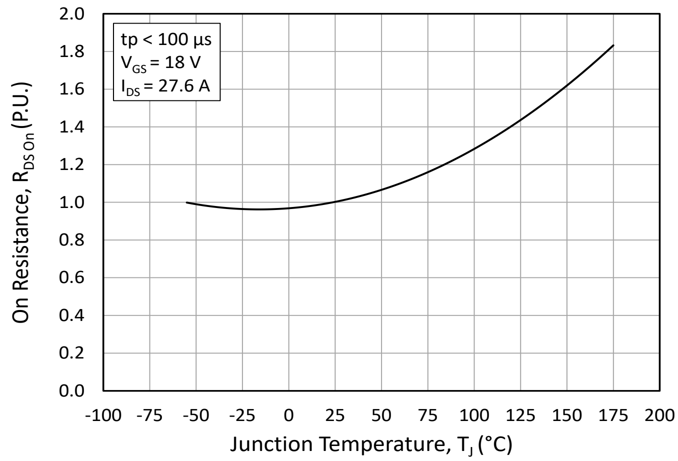


Figure 4. Normalized On-Resistance vs. Temperature

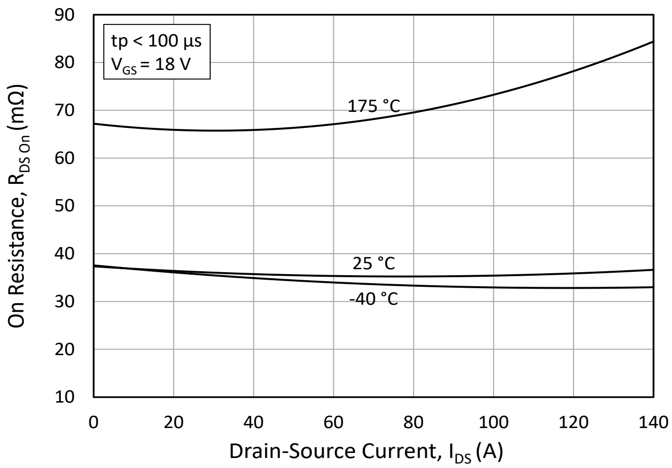


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

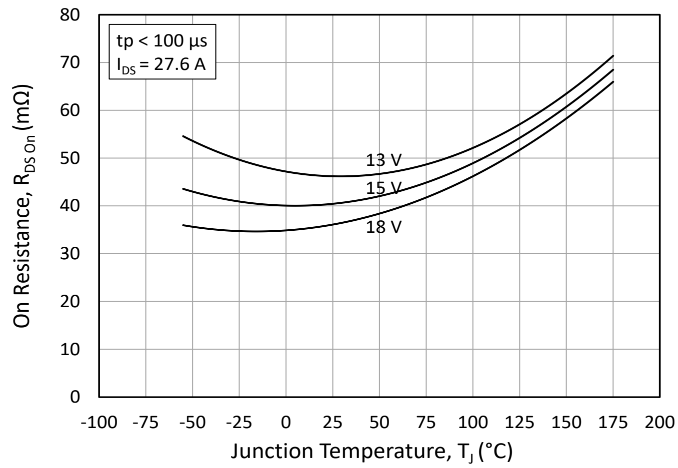


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

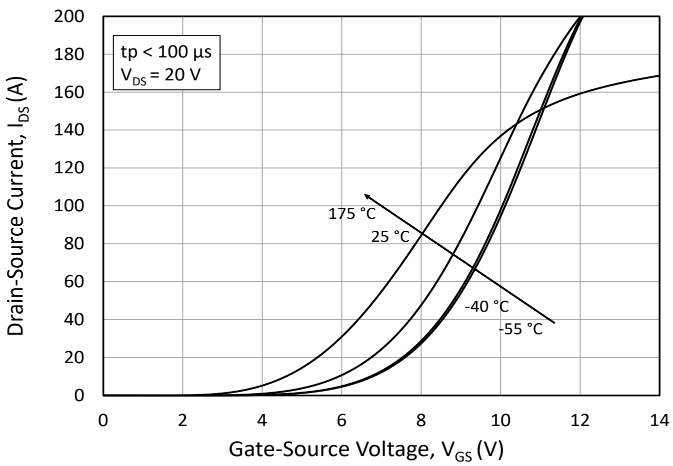


Figure 7. Transfer Characteristic for Various Junction Temperatures

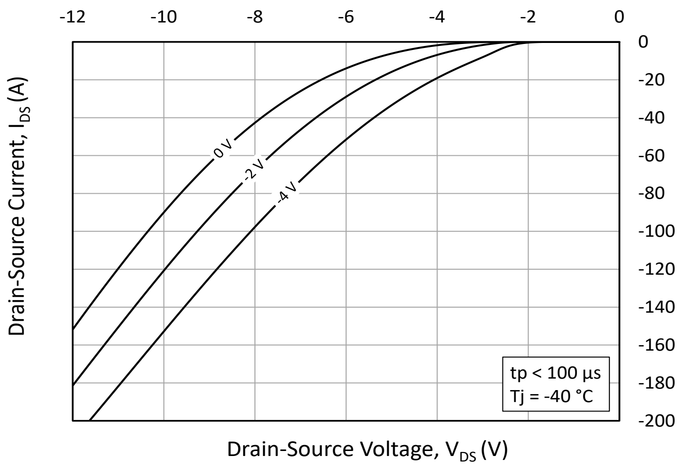


Figure 8. Body Diode Characteristic at -40ºC

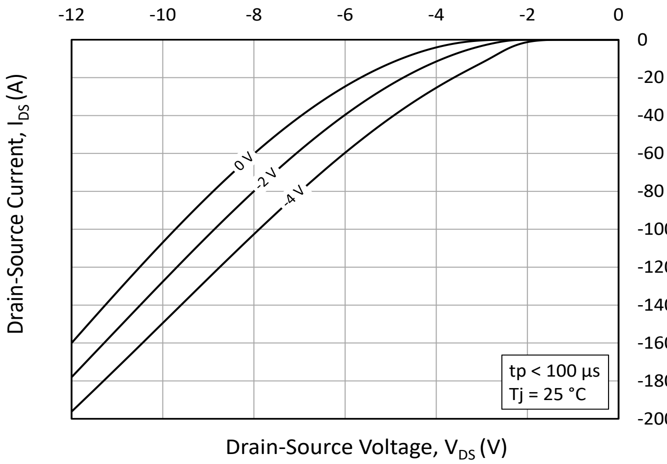


Figure 9. Body Diode Characteristic at 25ºC

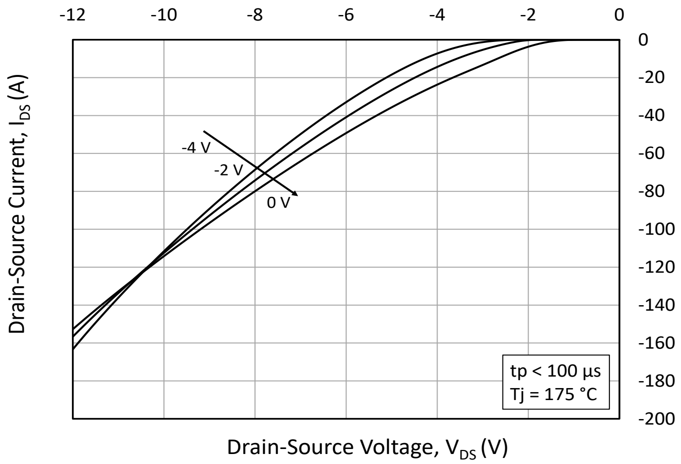


Figure 10. Body Diode Characteristic at 175ºC

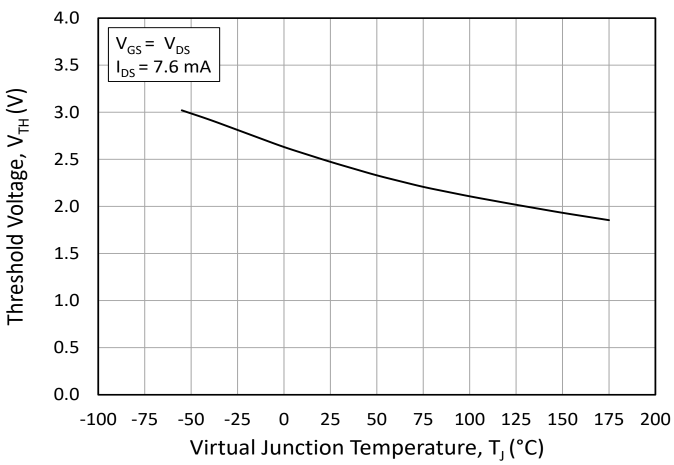


Figure 11. Threshold Voltage vs. Temperature

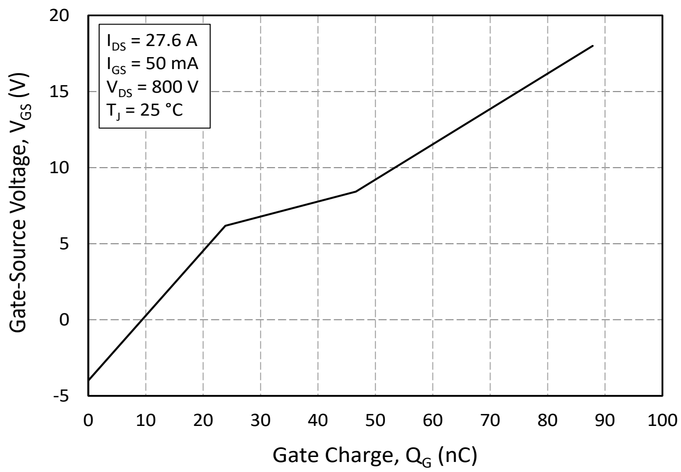


Figure 12. Gate Charge Characteristics

Typical Performance

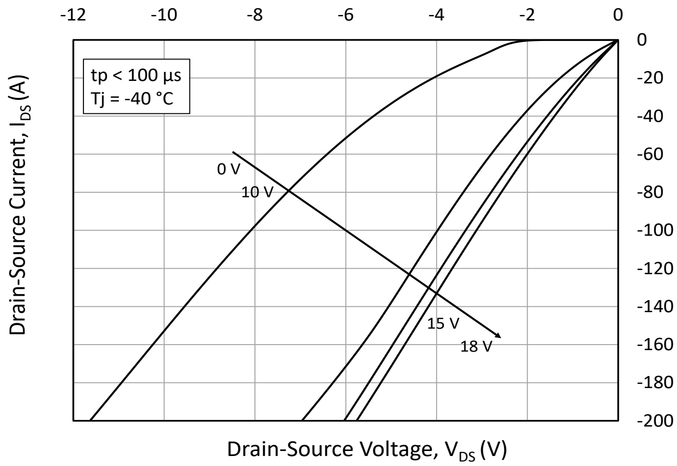


Figure 13. 3rd Quadrant Characteristic at -40°C

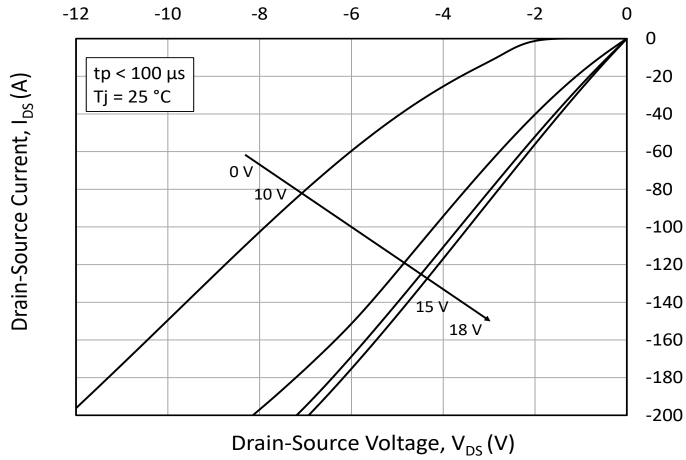


Figure 14. 3rd Quadrant Characteristic at 25°C

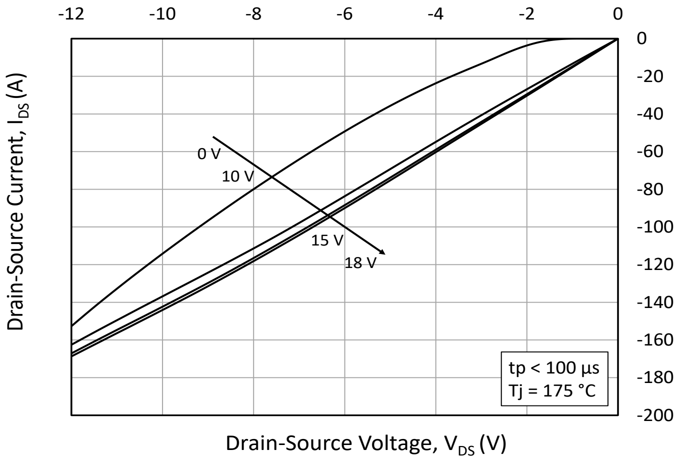


Figure 15. 3rd Quadrant Characteristic at 175°C

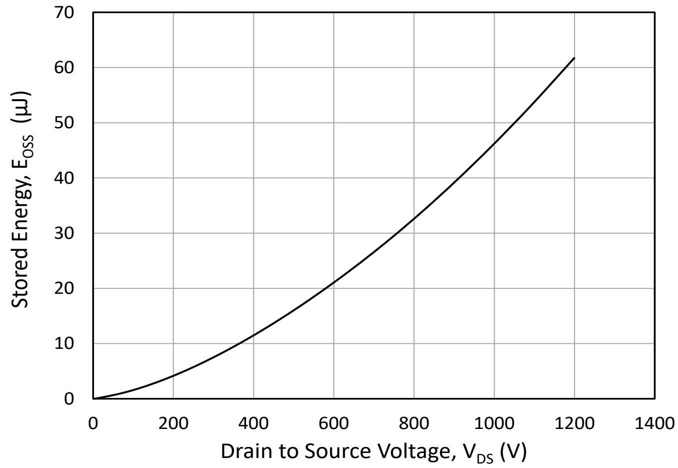


Figure 16. Output Capacitor Stored Energy

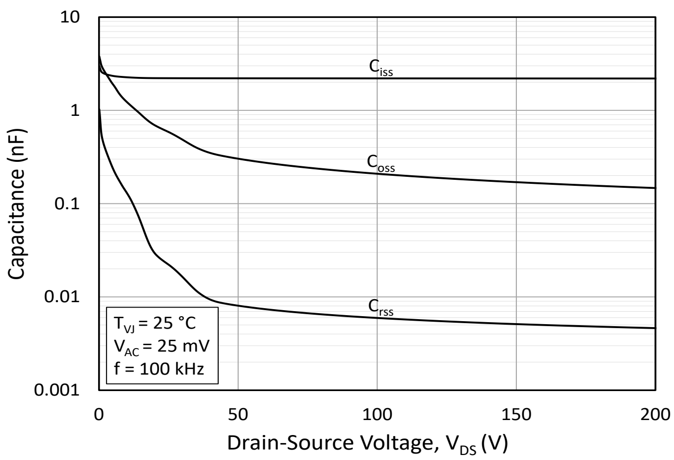


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

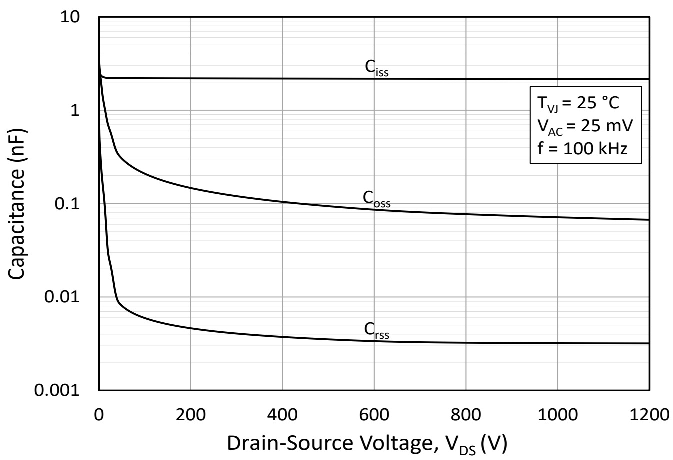


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200 V)

Typical Performance

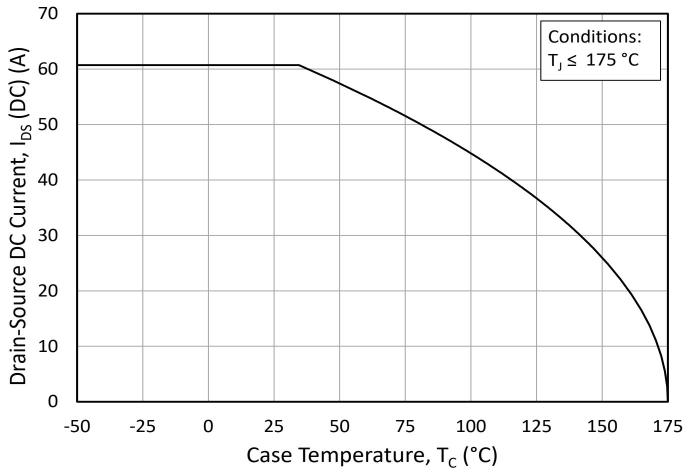


Figure 19. Continuous Drain Current Derating vs. Case Temperature

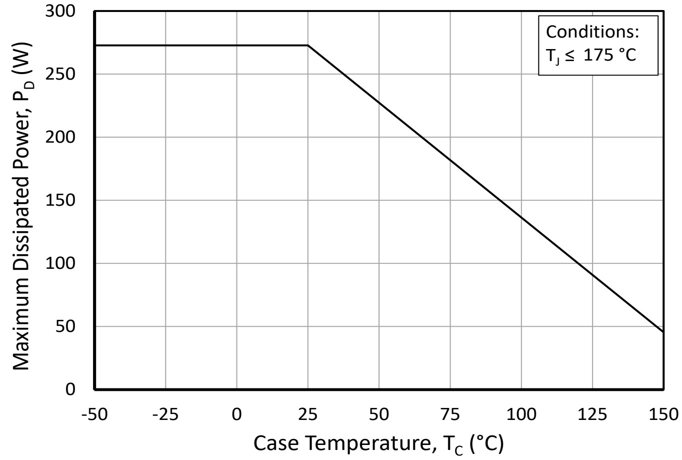


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

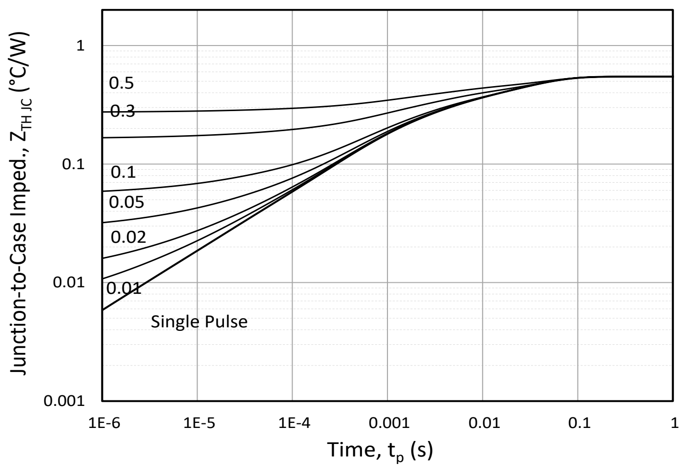


Figure 21. Transient Thermal Impedance (Junction - Case)

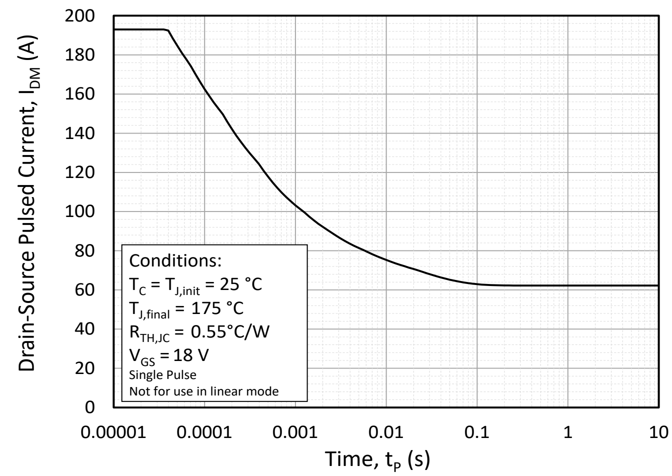


Figure 22. Safe Operating Area

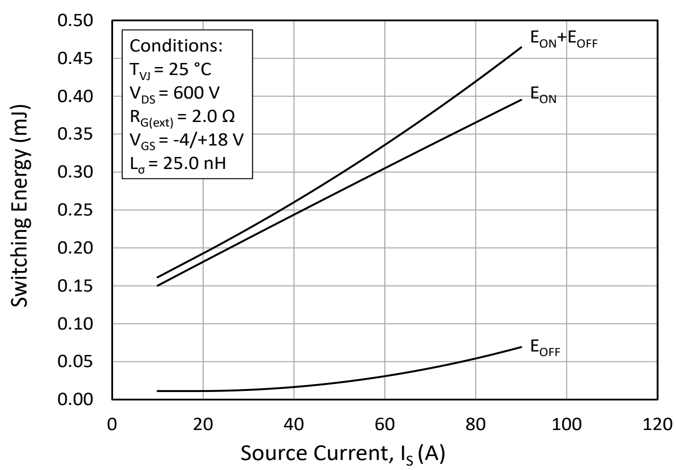


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 600 V)

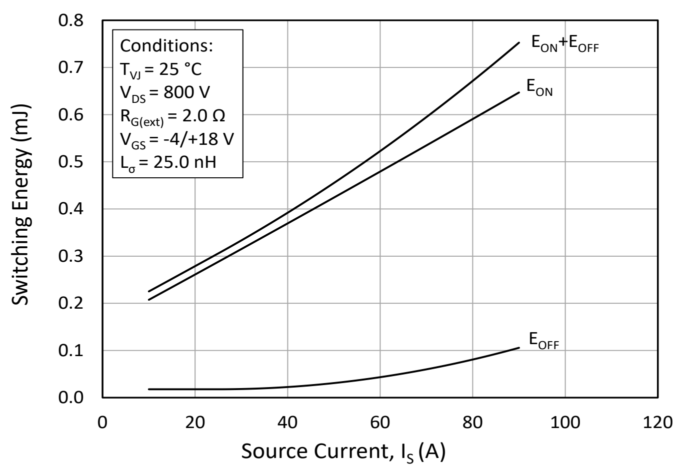


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 800 V)

Typical Performance

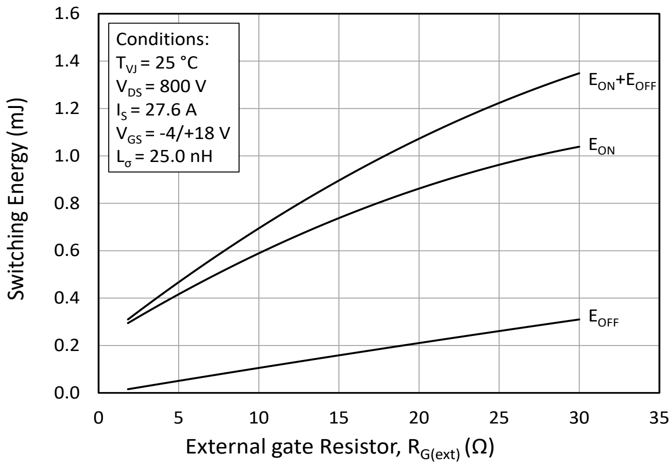


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

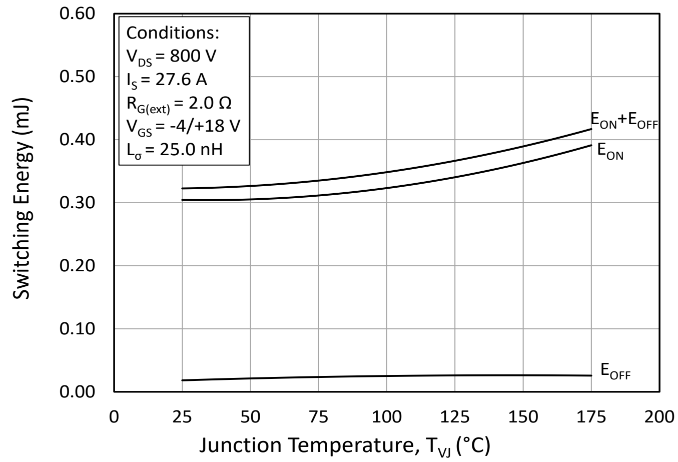


Figure 26. Clamped Inductive Switching Energy vs. Temperature

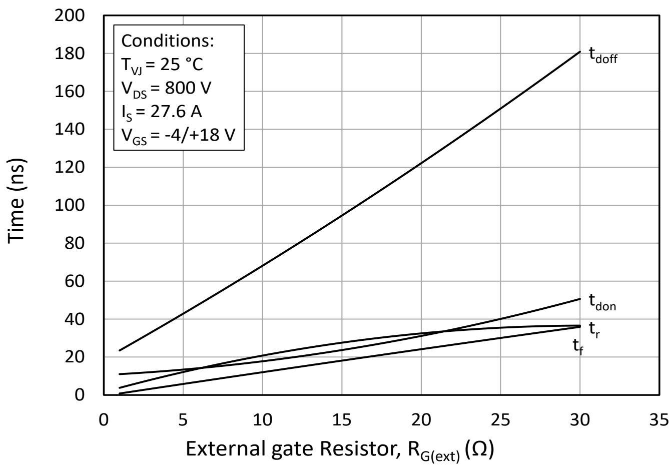


Figure 27. Switching Times vs. $R_{G(ext)}$

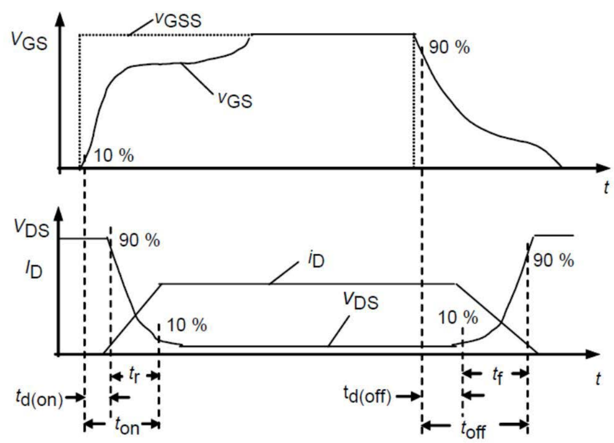


Figure 28. Switching Times Definition

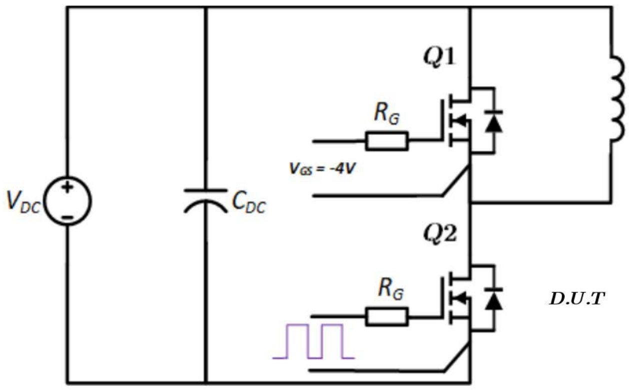


Figure 29. Clamped Inductive MOSFET Switching Waveform Test Circuit

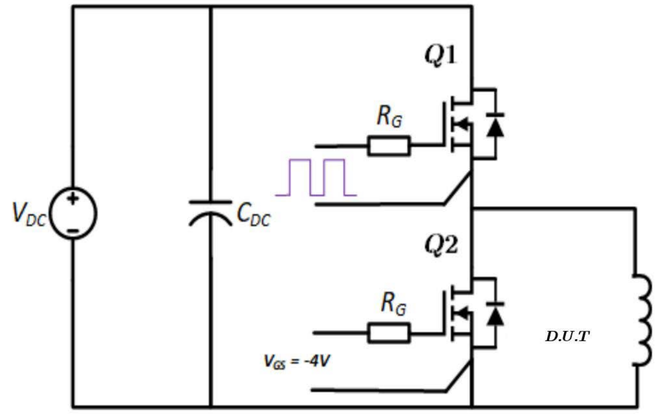
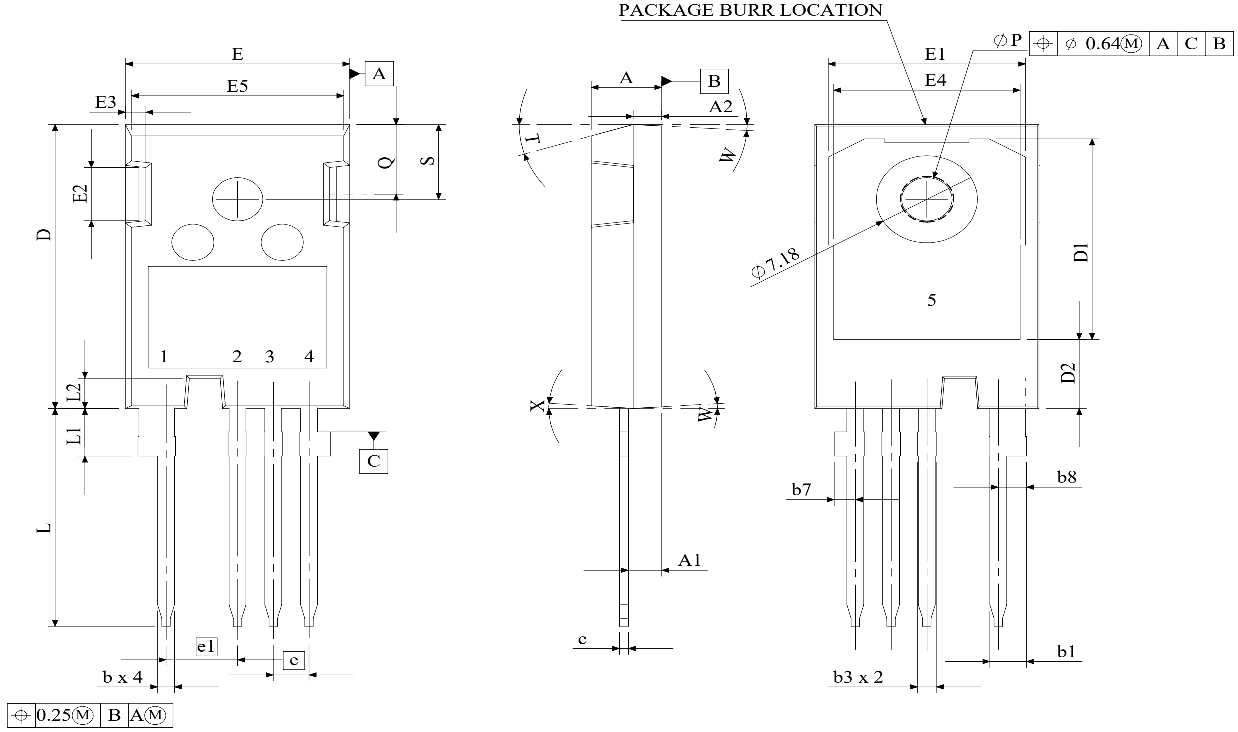


Figure 30. Clamped Inductive Body diode Switching Waveform Test Circuit

Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.23	2.54
A2	1.91	2.16
b	1.07	1.33
b1	2.39	2.94
b3	1.07	1.60
b7	1.30	1.70
b8	1.80	2.20
c	0.55	0.68
D	23.30	23.63
D1	16.25	17.65
D2	5.55	5.95
E	15.75	16.13
E1	13.1	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
E5	14.65	15.05
e1	5.08 BSC	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
∅P	3.51	3.65
Q	5.49	6.00
S	6.04	6.30
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	DRAIN
2	SOURCE
3	DRIVER SOURCE
4	GATE
5	DRAIN

NOTE:
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

TITLE: PACKAGE OUTLINE DRAWING: TO-247-4L

Date: 3/4/24

REVISION NO. 02

A4

PRD 05966 SCALE:1:1 SHEET 1 OF 1

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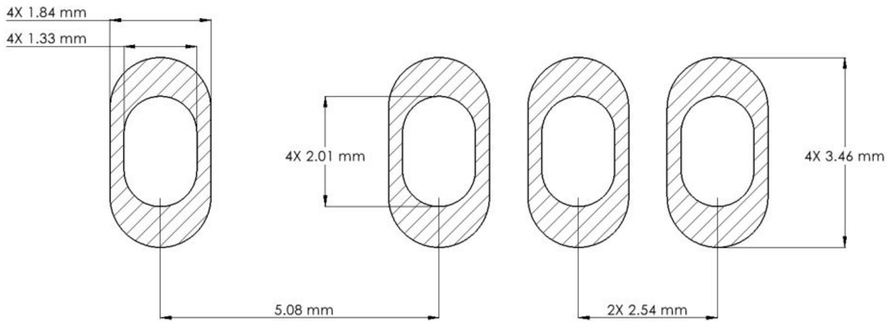
Recommended Solder Pad Layout

All dimensions in mm



Revision history

Document Version	Date of release	Description of changes
1	November 2025	Initial release
2	December 2025	Updated Note 2

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The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented February 2, 2013. RoHS Declarations for this product can be obtained from your Wolfspeed representative or from the Product Documentation sections of www.wolfspeed.com.

REACh Compliance

REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

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