

C4MS025120K1

Silicon Carbide Power MOSFET
Switching Optimized 1200V 25mΩ Industrial
N-Channel Enhancement Mode

Features

- Industry compatible drive voltage 15V...18V/-5V...0V
- Soft body diode with low V_{DS} overshoot and ringing
- Low $R_{DS(on)}$ at high operating temperatures
- Improved device capacitances ratio (C_{iss}/C_{rss})
- High transient voltage robustness with improved lifetime
- Halogen free, RoHS compliant

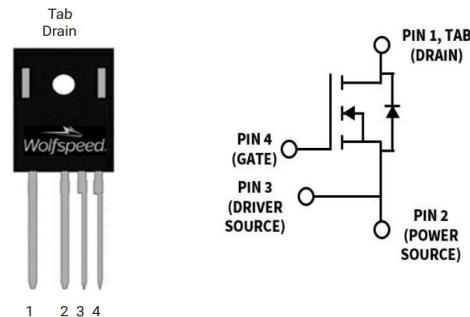
Benefits

- Higher efficiency with lower switching losses and EMI
- Faster switching operation enabling high power density
- Enables system level price performance optimization
- Reduction in system level cooling requirements

Typical Applications

- EV Chargers
- Solar/ESS
- Motor Control
- Industrial Power Supplies
- High Voltage DC/DC Converters

Package



Orderable Part number	Package type	Marking
C4MS025120K1	TO-247-4 LP	C4MS025120K1

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1200	V		
Transient Drain - Source Voltage				1300		<100hrs of lifetime	Note 1
Maximum Gate - Source Voltage	$V_{GS(max)}$	-10		+23			Note 2
DC Continuous Drain Current	I_D		86		A	$V_{GS} = 18\text{ V}, T_c = 25\text{ }^\circ\text{C}, T_j \leq 175\text{ }^\circ\text{C}$	Note 3
			62			$V_{GS} = 18\text{ V}, T_c = 100\text{ }^\circ\text{C}, T_j \leq 175\text{ }^\circ\text{C}$	
Pulsed Drain Current	I_{DM}			274		t_{Pmax} limited by T_{jmax} $V_{GS} = 18\text{ V}, T_c = 25\text{ }^\circ\text{C}$	
Power Dissipation	P_D		366		W	$T_c = 25\text{ }^\circ\text{C}, T_j = 175\text{ }^\circ\text{C}$	Note 4
Operating Junction and Storage Temperature	T_j, T_{stg}	-40		+175	$^\circ\text{C}$		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	

Note (1): 100 hours of total accumulated lifetime of the product.

Note (2): When applying IPC-9592B or OCP M-CRPS derating standards, a maximum Gate-Source voltage (V_{GS}) of +25V is permissible.

Note (3): Current limit calculated by $I_{D(max)} = \sqrt{(P_D / R_{DS(typ)})(T_{j(max)} / T_{j(max)})}$

Note(4): $P_D = (T_j - T_c) / R_{th(jC,typ)}$


Electrical Characteristics (T_c = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V _{(BR)DSS}	Drain-Source Breakdown Voltage	1200			V	V _{GS} = 0 V, I _D = 100 μA	
V _{GS(th)}	Gate Threshold Voltage	2	2.6	3.9	V	V _{DS} = V _{GS} , I _D = 10.8 mA	Fig. 11
			2.0		V	V _{DS} = V _{GS} , I _D = 10.8 mA, T _J = 175°C	
I _{DSS}	Zero Gate Voltage Drain Current		1	50	μA	V _{DS} = 1200 V, V _{GS} = 0 V	
I _{GSS}	Gate-Source Leakage Current		10	250	nA	V _{GS} = 18 V, V _{DS} = 0 V	
V _{GS(op)}	Recommended Turn on Gate-Source Voltage	+15...+18			V		Refer to PRD-09634
	Recommended Turn off Gate-Source Voltage	-5...0					
R _{DS(on)}	Drain-Source On-State Resistance		25	33	mΩ	V _{GS} = 18 V, I _D = 39.2 A	Fig. 4, 5, 6
			47			V _{GS} = 18 V, I _D = 39.2 A, T _J = 175°C	
			28			V _{GS} = 15 V, I _D = 39.2 A	
g _{fs}	Transconductance		28		S	V _{DS} = 20 V, I _D = 39.2 A, T _J = 25°C	Fig. 7
			27			V _{DS} = 20 V, I _D = 39.2 A, T _J = 175°C	
R _{DS(on)Tempco}	On resistance temperature coefficient		1.88			V _{GS} = 18 V, I _D = 39.2 A	Note 5
C _{iss}	Input Capacitance		3087		pF	V _{GS} = 0 V, V _{DS} = 1000 V f = 100 kHz V _{AC} = 25 mV	Fig. 17, 18
C _{oss}	Output Capacitance		103				
C _{rss}	Reverse Transfer Capacitance		4.7				
C _{iss/C_{rss}}	Capacitance Ratio		630				Note 6
E _{oss}	C _{oss} Stored Energy		63		μJ		Fig. 16
C _{o(er)}	Effective Output Capacitance (Energy Related)		145		pF	V _{GS} = 0 V, V _{DS} = 0...800 V	
C _{o(tr)}	Effective Output Capacitance (Time Related)		238				
E _{on}	Turn-On Switching Energy (Body Diode FWD) T _J =25C T _J =175C				μJ	V _{DS} = 800 V, V _{GS} = -4 V/18 V, I _D = 39.2 A, R _{G(ext)} = 1 Ω, L _σ = 25 nH	Fig. 26, 29, 31 Fig. 26, 29, 32
			394				
E _{off}	Turn-Off Switching Energy (Body Diode FWD) T _J =25C T _J =175C		470				
			57				
t _{d(on)}	Turn-On Delay Time		12		ns	V _{DD} = 800 V, V _{GS} = -4 V/18 V I _D = 39.2 A, R _{G(ext)} = 1 Ω, Timing relative to V _{DS} Inductive load	Fig. 27, 28
t _r	Rise Time		4				
t _{d(off)}	Turn-Off Delay Time		36				
t _f	Fall Time		11				
R _{G(int)}	Internal Gate Resistance		2.6		Ω	f = 1 MHz	
Q _{gs}	Gate to Source Charge		35		nC	V _{DS} = 800 V, V _{GS} = -4 V/18 V I _D = 39.2 A, T _J = 25°C Per IEC60747-8-4 pg 21	Fig. 12
Q _{gd}	Gate to Drain Charge		30				
Q _g	Total Gate Charge		125				

Note (5): R_{DS(on)Tempco} refers to R_{DS(on)} at 175°C / R_{DS(on)} at 25°C, C4MS 1200V product family value

Note (6): Capacitance ratio is a FOM for Partial turn-on immunity PRD-09633, C4MS 1200V product family value

Co(er), a lumped capacitance that gives the same stored energy as Coss while V_{DS} is rising from 0 to 800V

Co(tr), a lumped capacitance that gives the same charging time as Coss while V_{DS} is rising from 0 to 800V



Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.1		V	$V_{GS} = -4\text{ V}$, $I_{SD} = 19.6\text{ A}$, $T_j = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.6		V	$V_{GS} = -4\text{ V}$, $I_{SD} = 19.6\text{ A}$, $T_j = 175^\circ\text{C}$	
I_S	Continuous Diode Forward Current	59		A	$V_{GS} = -4\text{ V}$, $T_c = 25^\circ\text{C}$	
I_{SM}	Diode Pulse Current		274	A	$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{jmax}	
t_{rr}	Reverse Recovery Time	14		ns	$V_{GS} = -4\text{ V}$, $I_S = 39.2\text{ A}$, $V_{SD} = 800\text{V}$ $T_j = 175^\circ\text{C}$, $dI/dt = 15.8\text{ A/ns}$	
Q_{rr}	Reverse Recovery Charge	742		nC		
I_{RRM}	Peak Reverse Recovery current	94		A		
E_{RR}	Reverse recovery Energy			μJ	$V_{DS} = 800\text{ V}$, $I_D = 39.2\text{ A}$,	
	$T_j = 25^\circ\text{C}$	102			$V_{GS} = -4\text{ V}/18\text{V}$, $R_{G(on)} = 1\Omega$, $L_\sigma = 25\text{nH}$	
	$T_j = 175^\circ\text{C}$	256				

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.41	$^\circ\text{C/W}$		

Typical Performance

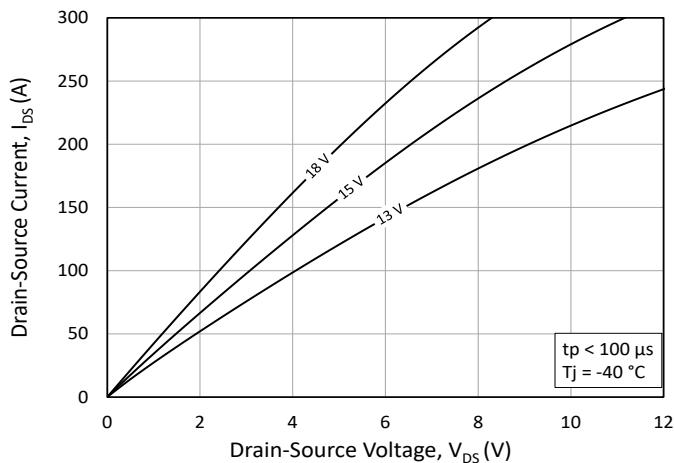
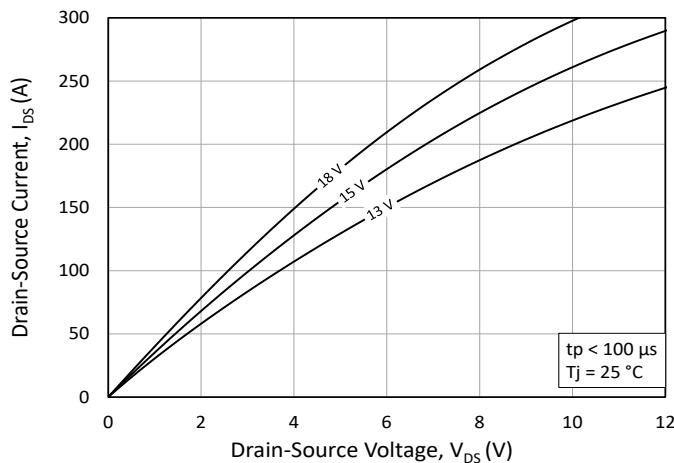
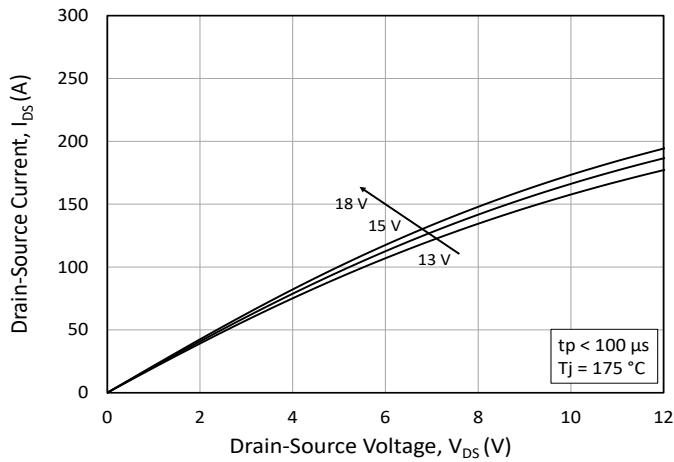
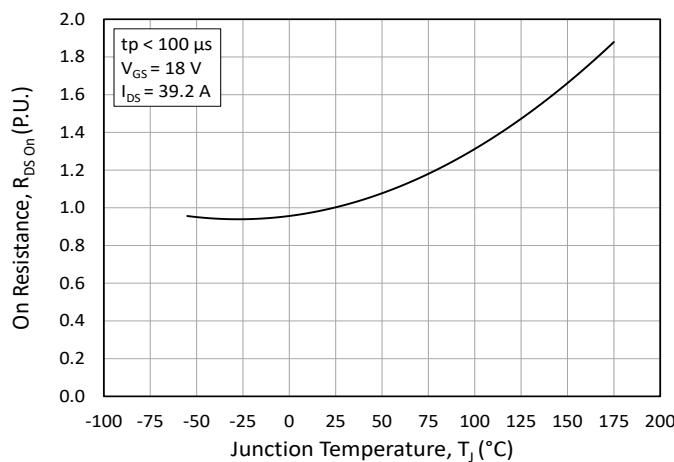
Figure 1. Output Characteristics $T_j = -40^\circ\text{C}$ Figure 2. Output Characteristics $T_j = 25^\circ\text{C}$ Figure 3. Output Characteristics $T_j = 175^\circ\text{C}$ 

Figure 4. Normalized On-Resistance vs. Temperature

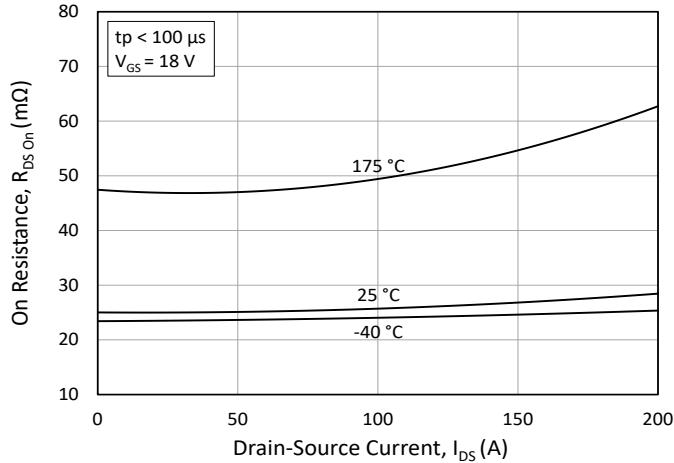


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

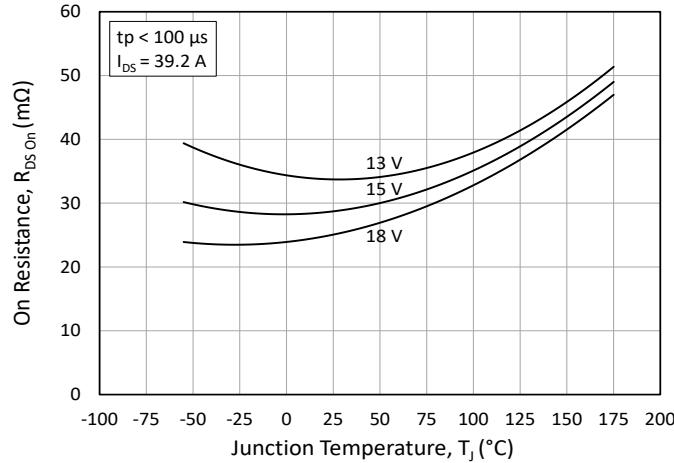


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

Typical Performance

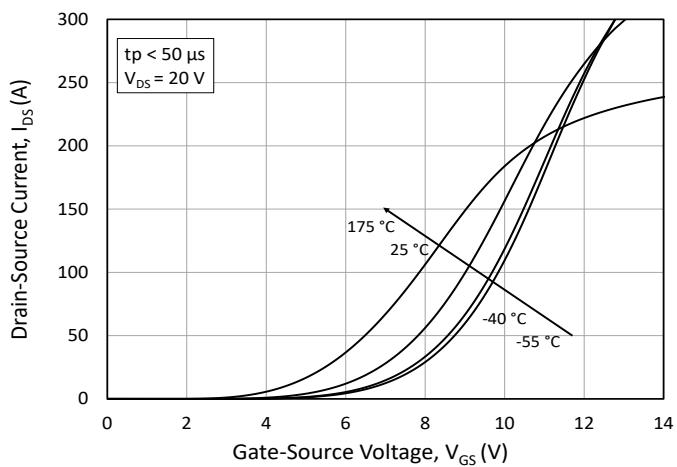


Figure 7. Transfer Characteristic for Various Junction Temperatures

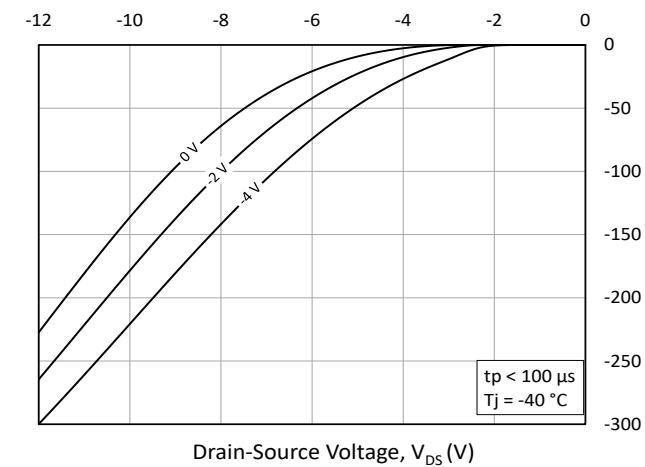


Figure 8. Body Diode Characteristic at -40°C

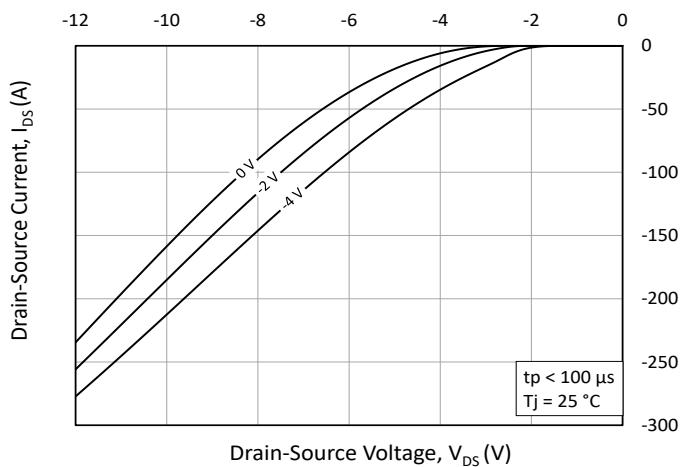


Figure 9. Body Diode Characteristic at 25°C

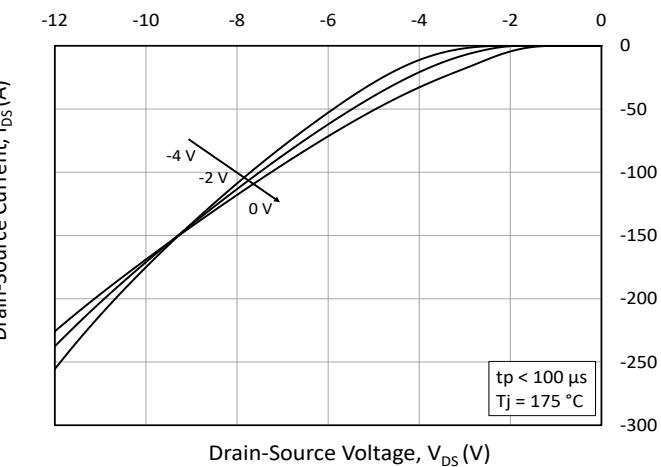


Figure 10. Body Diode Characteristic at 175°C

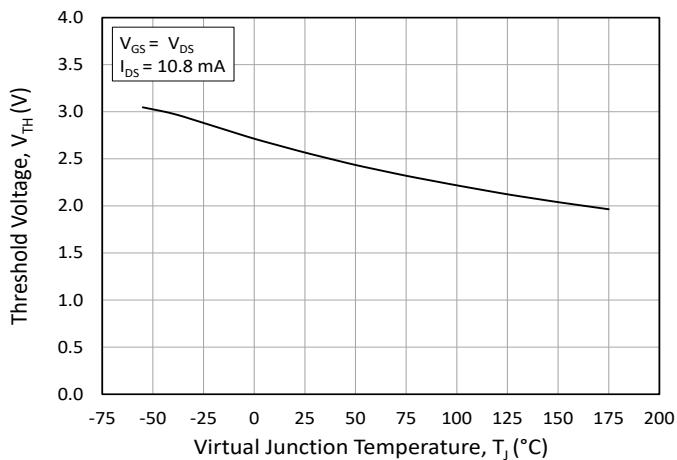


Figure 11. Threshold Voltage vs. Temperature

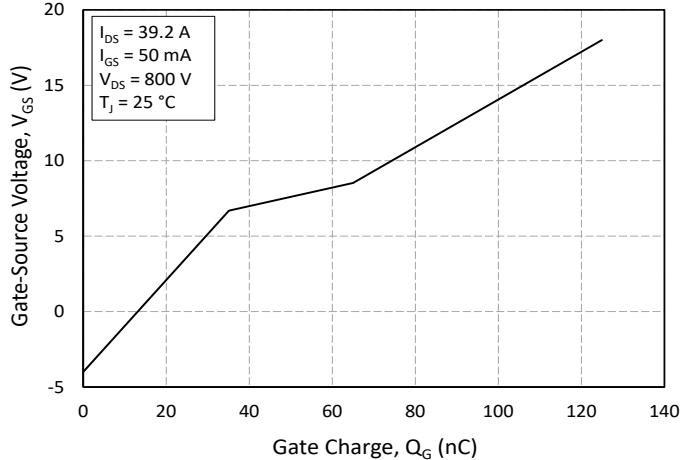


Figure 12. Gate Charge Characteristics

Typical Performance

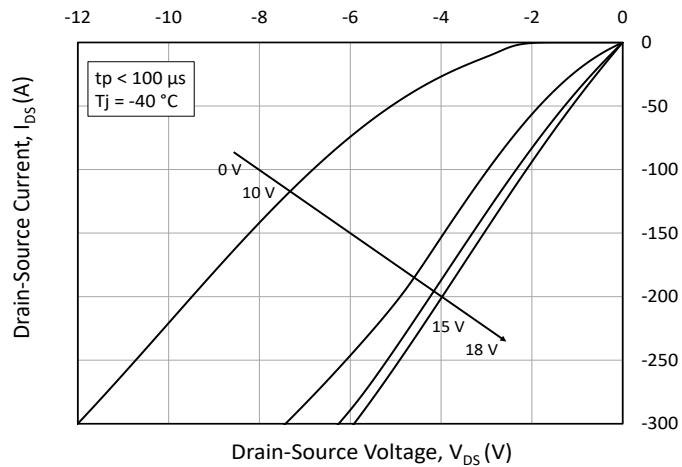
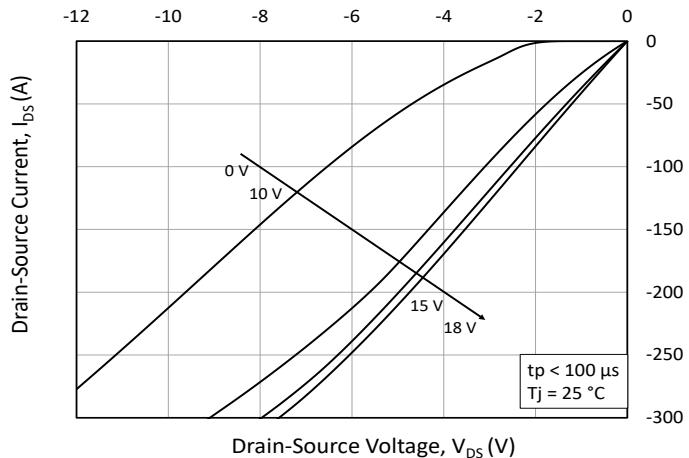
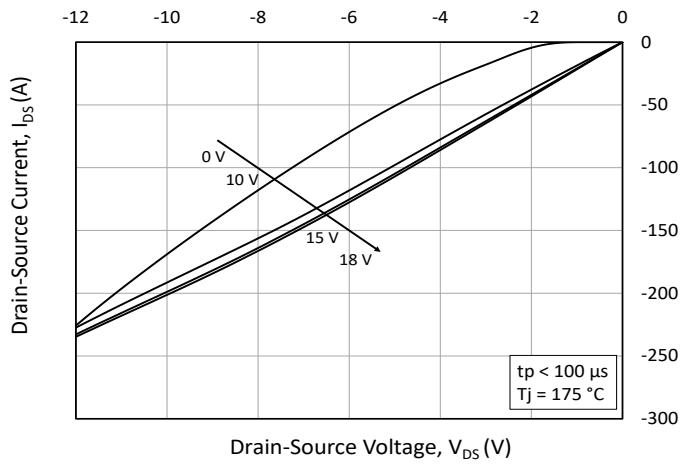
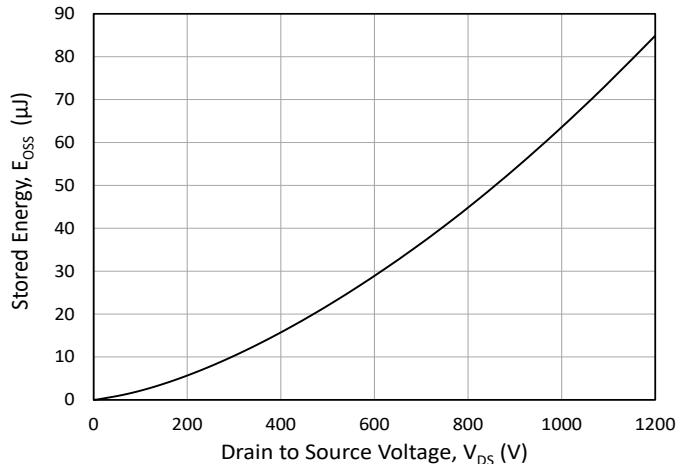
Figure 13. 3rd Quadrant Characteristic at -40°C Figure 14. 3rd Quadrant Characteristic at 25°C Figure 15. 3rd Quadrant Characteristic at 175°C 

Figure 16. Output Capacitor Stored Energy

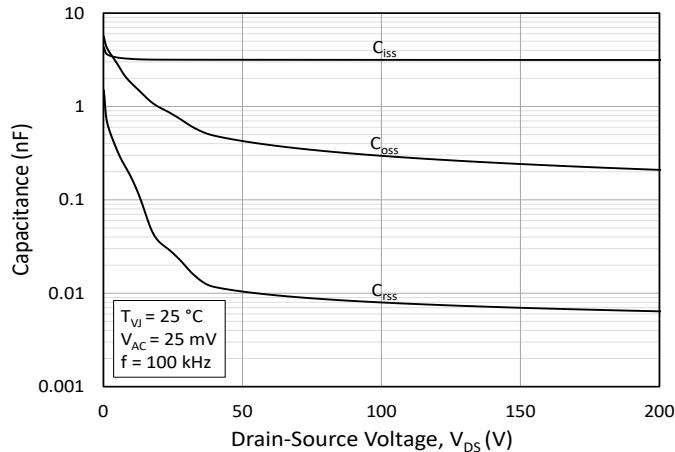


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

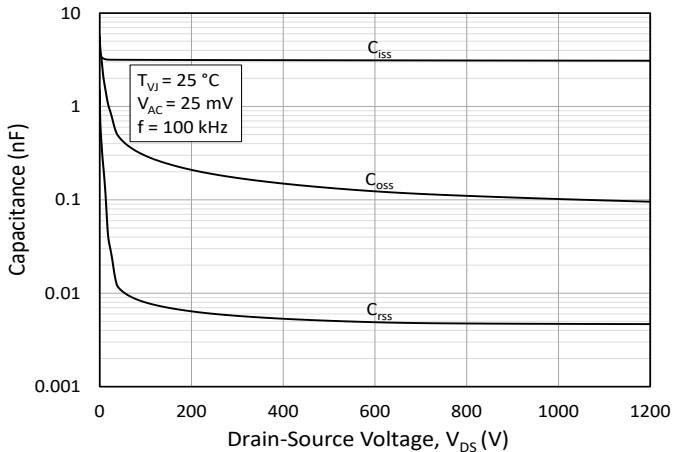


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200 V)

Typical Performance

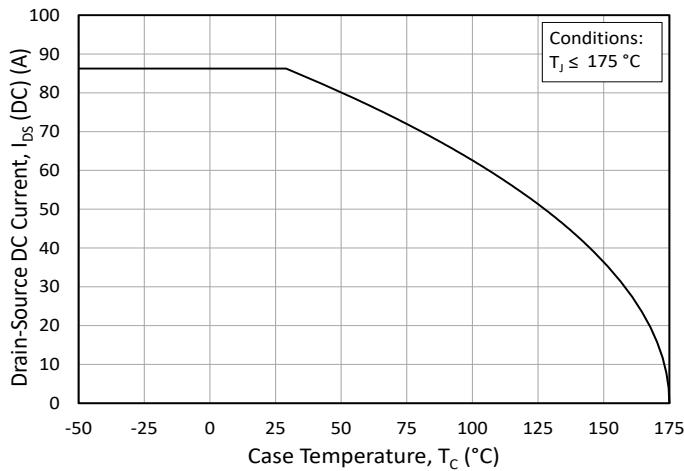


Figure 19. Continuous Drain Current Derating vs. Case Temperature

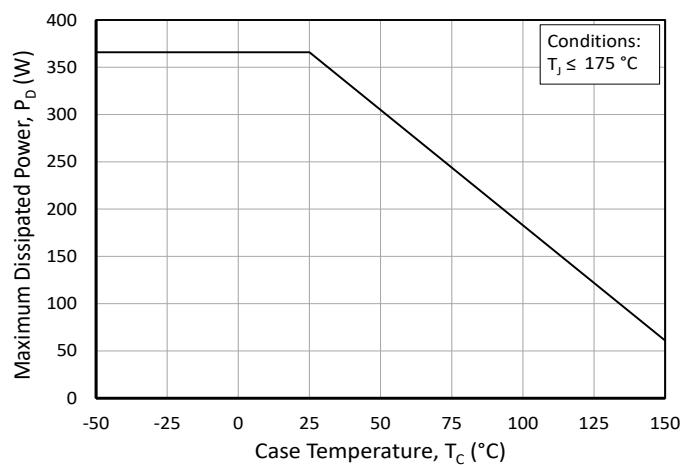


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

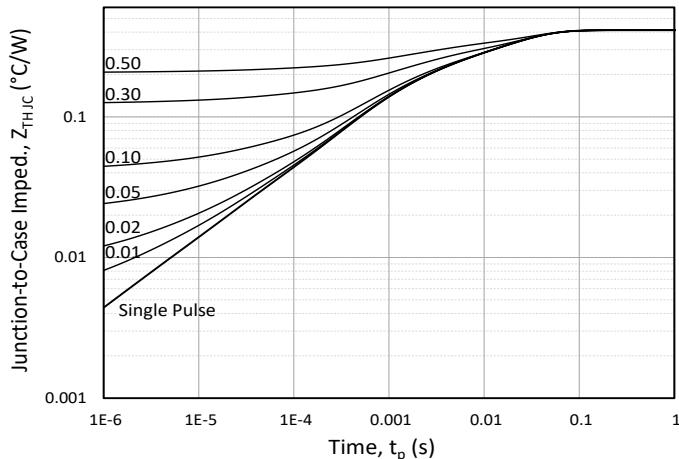


Figure 21. Transient Thermal Impedance (Junction - Case)

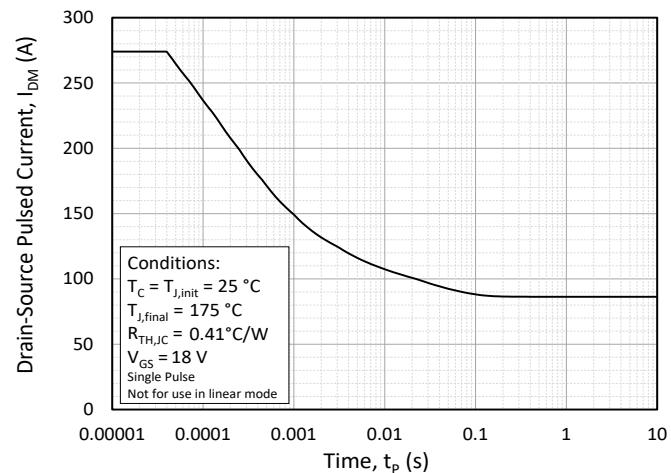


Figure 22. Safe Operating Area

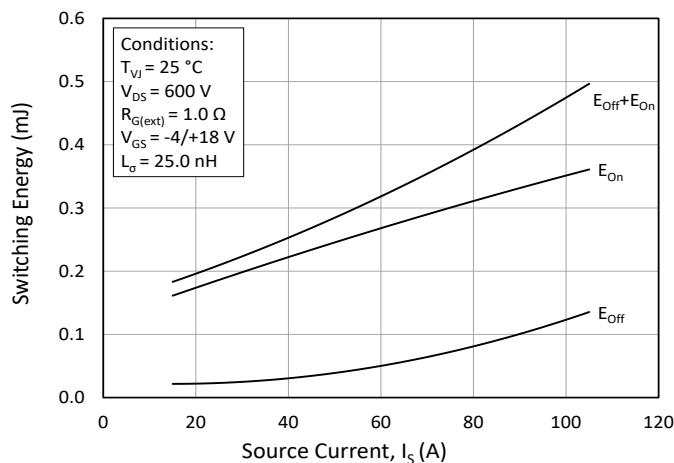


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 600$ V)

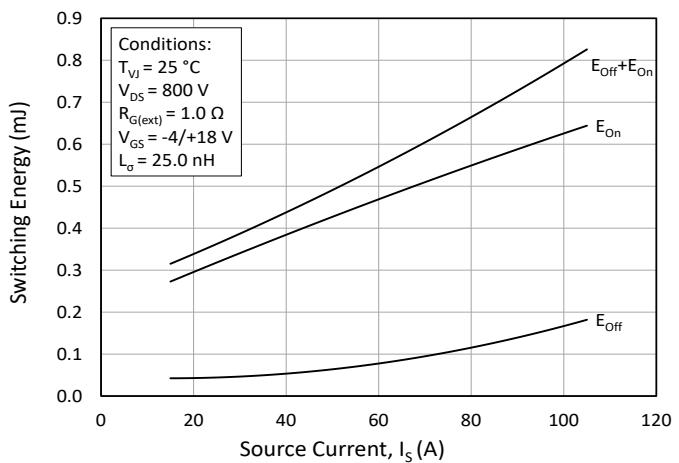


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 800$ V)

Typical Performance

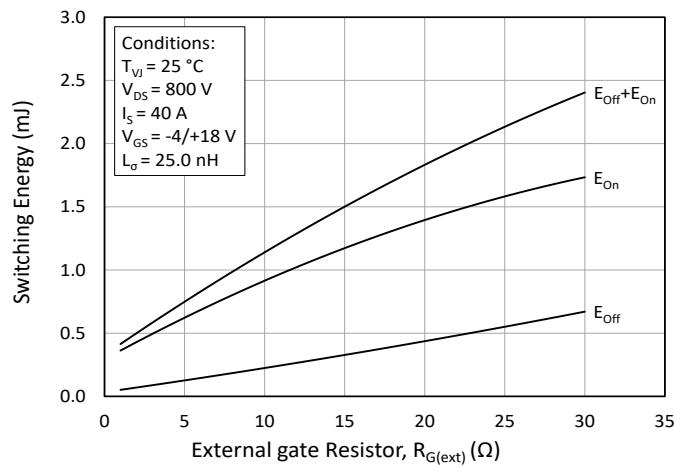
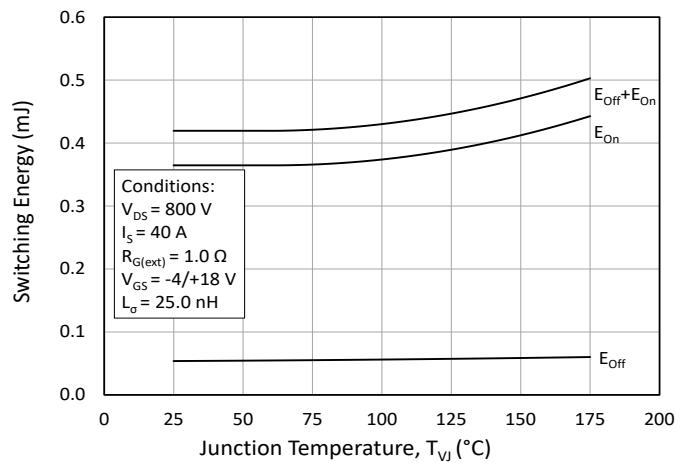
Figure 25. Clamped Inductive Switching Energy vs. $R_{G(\text{ext})}$ 

Figure 26. Clamped Inductive Switching Energy vs. Temperature

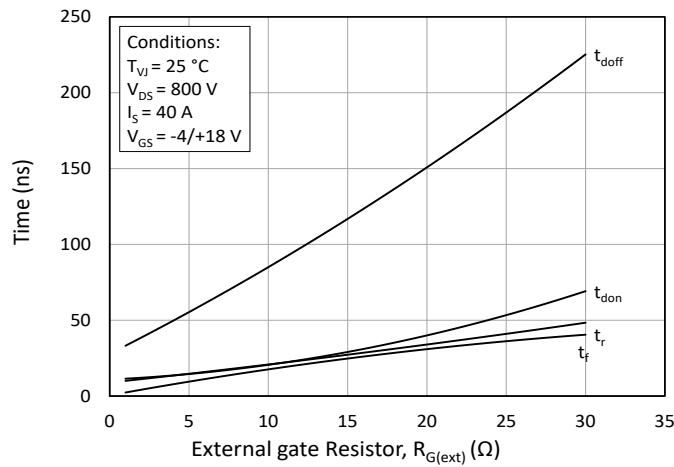
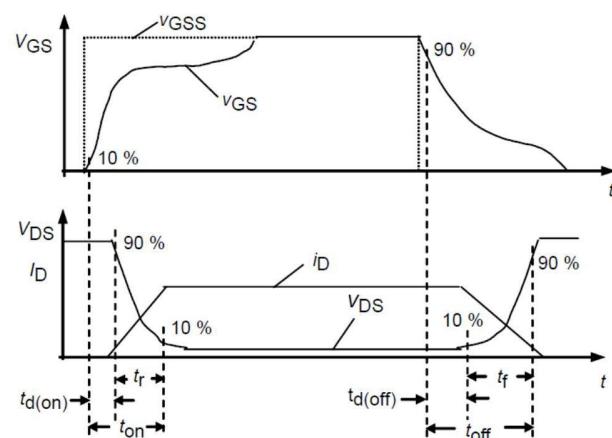
Figure 27. Switching Times vs. $R_{G(\text{ext})}$ 

Figure 28. Switching Times Definition

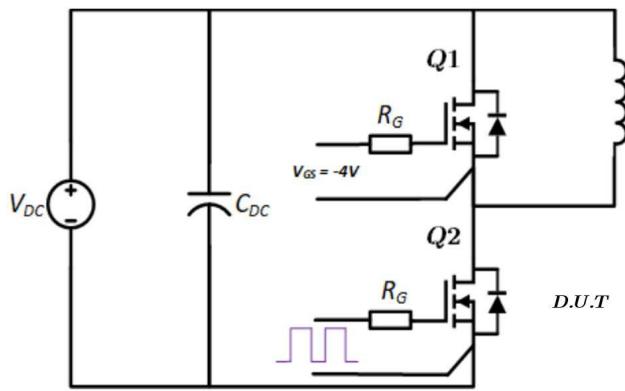


Figure 29. Clamped Inductive MOSFET Switching Waveform Test Circuit

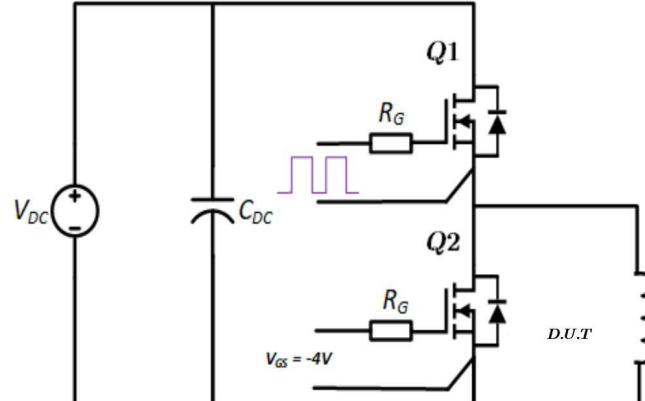
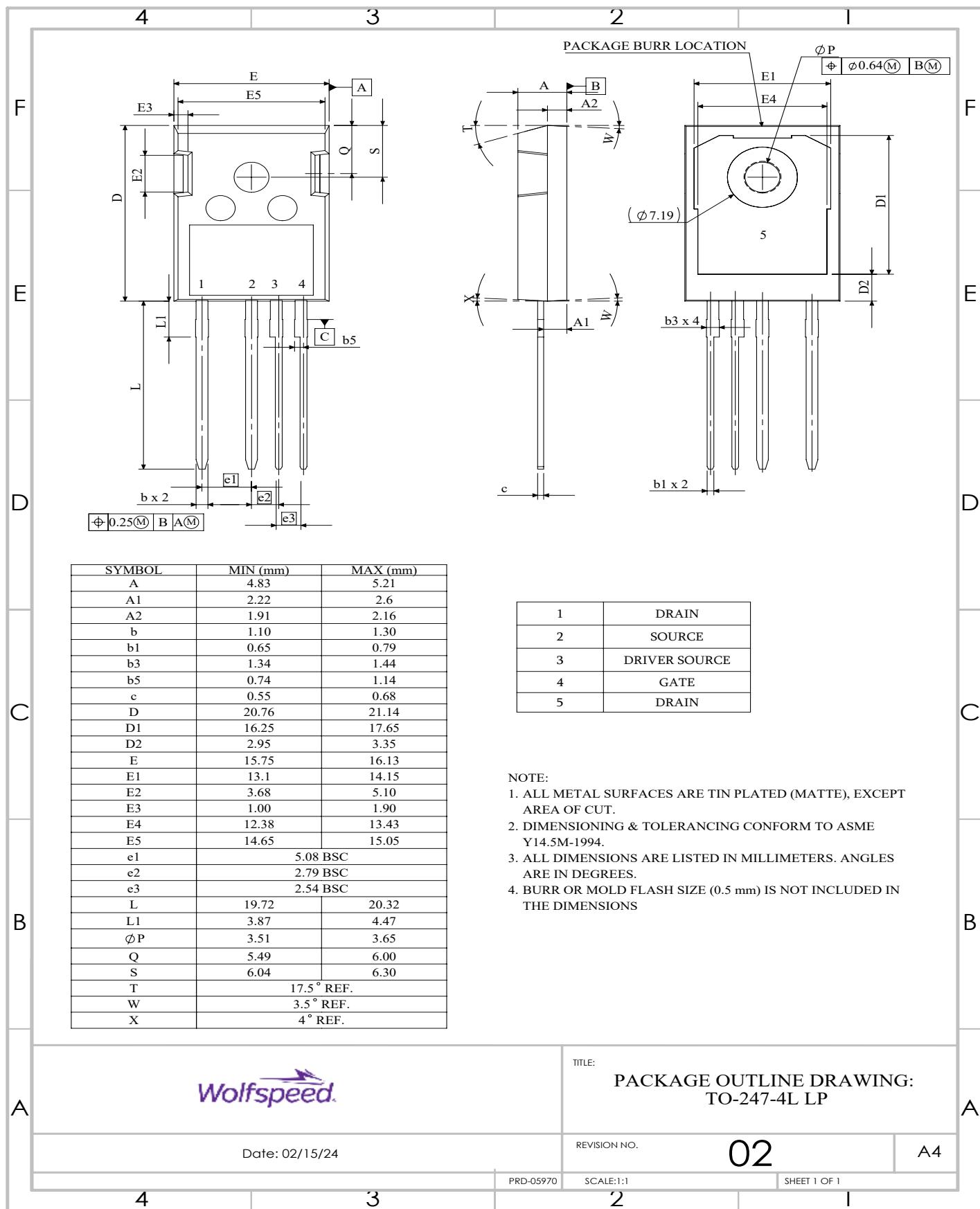


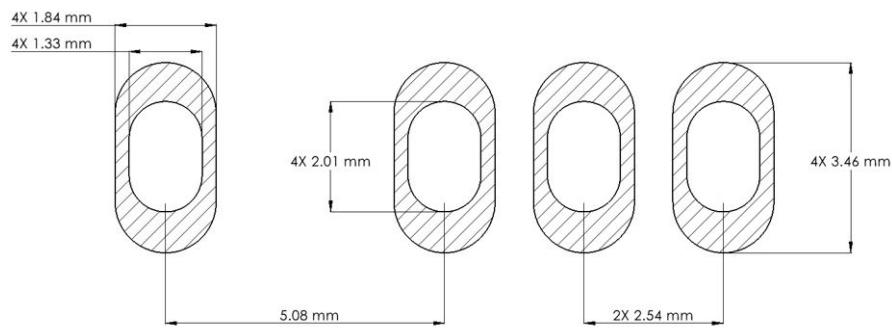
Figure 30. Clamped Inductive Body diode Switching Waveform Test Circuit

Package Dimensions



Recommended Solder Pad Layout

All dimensions in mm



Revision history

Document Version	Date of release	Description of changes
1	November 2025	Initial release
2	December 2025	Updated Note 2



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