RVSY018 Fast Turn-off Synchronous Rectification Controller

FEATURES

- Relative Maximum Voltage Detection Ensures Effective Turn-on Performance
- Programmable Intelligent Voltage-limited Conduction to Adapt to SR MOSFET
- Supports DCM and CCM Operations
- Ultra-fast Turn-off Delay: 10ns/Turn-on Delay: 30ns
- Programmable Turn-off Threshold
- Programmable Blanking Time
- Supports Maximum Operating Frequency of 700kHz
- High-power Self-powering. No Need for Auxiliary Winding
- Supports Both High-side and Low-side Synchronous Rectification
- The Detection Pin is Effectively Designed to Withstand Negative Voltage, Regardless of Negative Voltage Generated by the Body Diode
- Industrial-grade Operating Temperature Range -40~125°C
- SOT23-6 Package

APPLICATIONS

- DC-DC Power Converter
- AC-DC Power Supplies
- Battery Management System Power Supplies
- Various Module Power Supplies

DESCRIPTION

RVSY018 is a high-performance synchronous rectification (SR) controller designed to support both deep Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) operations. It operates at frequencies up to 700kHz, making it ideal for high-speed power conversion applications. Key functional parameters are programmable via external resistors, allowing flexible configuration and optimization according to the characteristics of the selected SR MOSFET for improved overall system performance.

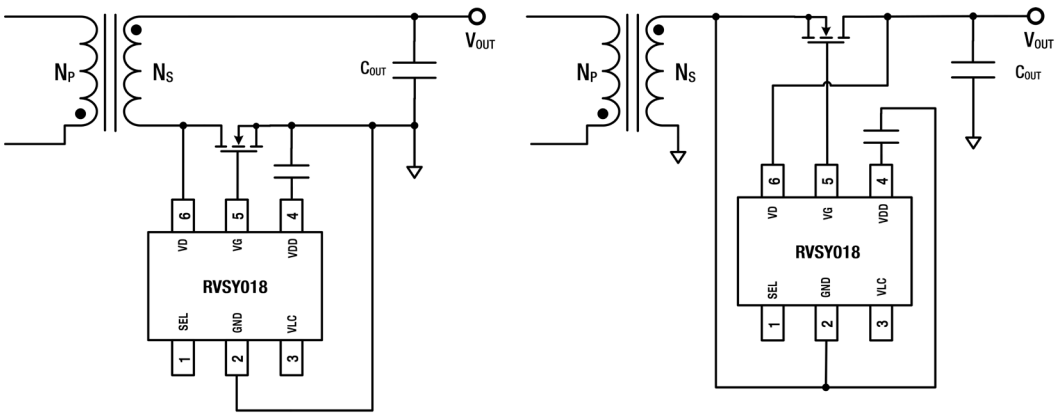
RVSY018 utilizes relative maximum voltage detection technology to enable accurate SR MOSFET turn-on, effectively preventing false triggering caused by resonant negative voltages in DCM. It is also compatible with soft-switching topologies such as Quasi-Resonant (QR) and Active Clamp Flyback (ACF). An intelligent voltage-limited conduction feature dynamically reduces the gate drive voltage when the V_{DS} drop is minimal. This increases the MOSFET's internal resistance, preventing premature turn-off and minimizing conduction losses, thereby enhancing overall efficiency.

The controller monitors the drain voltage of the SR MOSFET through the VD pin, which includes a built-in 100µA current source. The turn-off threshold is programmable via a resistor placed between the VD pin and the drain of the SR MOSFET. Additionally, the VD-to-VDD path acts as a linear regulator with robust power delivery capability, typically eliminating the need for an external auxiliary winding. The VD pin is specifically designed to tolerate negative voltage transients, ensuring stable internal circuit operation even in the presence of large negative V_{DS} swings.

Device Information

Part Number	Package	Size	SPQ
RVSY018	SOT23-6	3.0 mm x 2.8 mm	3000

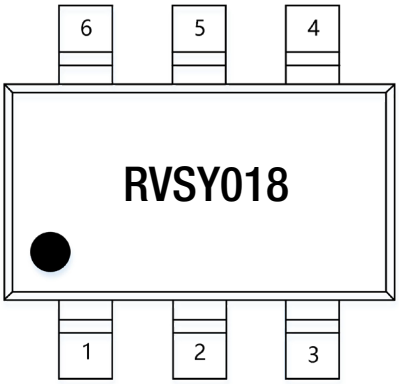
SIMPLIFIED SCHEMATIC



Low-Side

High-Side

PINOUT AND FUNCTIONS



NAME	PIN #	TYPE	DESCRIPTION
SEL	1	I	Blanking time selection pin (SEL): When SEL is left floating, the chip's internal circuit pulls the pin high, and the minimum on-time is set to 400ns. When SEL is connected to GND, the minimum on-time is set to 800ns.
GND	2	P	Ground.
VLC	3	I	Programmable intelligent voltage-limited conduction pin (VLC): Connecting a resistor of several hundred kΩ to GND increases the VG voltage when voltage-limited conduction is active. Connecting a resistor of several hundred kΩ to VG reduces the VG voltage when voltage-limited conduction is active. Connecting VLC to GND disables the voltage-limited conduction function.
VDD	4	P	IC power supply
VG	5	O	SR MOSFET gate driver.
VD	6	I	For SR MOSFET drain voltage sensing: When VD is directly connected to the drain of the SR MOSFET, the turn-off threshold is -1.5mV. Since the output current of this pin is 100µA, the turn-off threshold can be programmed by the resistor connected between VD and the drain of the SR MOSFET.

SPECIFICATIONS

Absolute Maximum Ratings

		MIN	MAX	UNIT
VDD, VG to GND	V_{DD}, V_G	-0.3	13	V
SEL, VLC to GND	V_{SEL}, V_{LC}	-0.3	6.6	
VD vs GND	V_D	-1	115	
VD to GND (transient less than 50ns)		-1.5		
Maximum Junction Temperature	T_{JMAX}		150	°C
Storage Temperature	T_{stg}	-55	150	

Stress exceeding the absolute maximum rated value may cause permanent damage to the device. These are only stress ratings and do not imply that the device operates beyond the recommended operating conditions under these or any other conditions. Long term exposure to absolute maximum rated conditions may affect the reliability of the device. All voltages are related to grounding. The current is positive input and negative output.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body mode HBM, per ESDA/JEDEC JS-001-2017, (Zap 1 pulse, Interval:>=0.1S)	±1500	V
		Charged Device Model CDM, per ESDA/JEDEC JS-002-2022	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM can be safely manufactured under standard ESD control processes.
(2) JEDEC document JEP157 states that 250-V CDM can be safely manufactured under standard ESD control processes.

Thermal Resistance

PACKAGING	θ_{JA}	Ψ_{JT}	UNIT
SOT23-6	143	17.37	°C/W

Note: Measured on a 1oz copper test board with dimensions of 7.62 cm × 11.43 cm.

Recommended Operatings Conditions

		MIN	TYP	MAX	UNIT
VD to GND Voltage	V_D			100	V
VDD to GND Voltage	V_{DD}	4.7		10	
SEL/VLC to GND Voltage	V_{SEL}, V_{LC}			6	
Ambient Temperature	T_A	-40		125	°C

Thermal Information

		MIN	TYP	MAX	UNIT
Junction-to-ambient Thermal Resistance	R_{eJA}		143.0		°C/W
Junction-to-top Characterization Parameter	Ψ_{JT}		17.4		

Note: Measured on a 1oz copper test board with dimensions of 7.62 cm × 11.43 cm.

Electrical Characteristics

V_{DD} = 9V and T = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD						
$V_{DD(ON)}$	VDD UVLO Rising Threshold	V_{DD} rising	4.3	4.7	5.0	V
$V_{DD(OFF)}$	VDD UVLO Falling	V_{DD} falling	4.0	4.3	4.6	V
$I_{VDD(ON)}$	VDD Startup Current	V_{DD} rising		320		uA
$I_{VDD(OP)}$	Operating Current	V_{DD}=5V, C_{LOAD}=2.2nF, f_{SW}=300kHz		4.1	5.0	mA
		V_{DD}=9V, C_{LOAD}=2.2nF, f_{SW}=300kHz		6.8	8.5	
$I_{VDD(Q)}$	Quiescent Current			630		µA
$I_{VDTOVDD}$	Maximum Charging Current	V_{DD}=4V, V_D=15V	100	140	180	mA
$V_{DD(REG)}$	Regulation Voltage	V_D=15V	8.0	9.0	10.0	V
VD						
$V_{th(on)}$	Turn-on Threshold (V_D - V_{GND})		-115	-95	-75	mV
$T_{D(on)}$	Turn-on Delay	C_{LOAD}=2.2nF		30	50	ns
$T_{B1(on)}$	Turn-on Blanking Time	SEL floating	300	400	550	ns
$T_{B2(on)}$		SEL connected to GND	600	800	1000	ns
$V_{th(off)}$	Turn-off Threshold (V_D -V_{GND})		-3.0	-1.5	1.5	mV
$T_{D(off)}$	Turn-off delay	C_{LOAD}=2.2nF		10		ns
$V_{th(OVP)}$	Overvoltage Threshold (V_D - V_{GND})		450	500	550	mV
$T_{D1(OVP)}$	Overvoltage Comparator Delay	SEL floating	120	150	180	ns
$T_{D2(OVP)}$		SEL connected to GND	200	250	300	ns
I_{VD}	Outflow Current	V_D=0V	80	100	120	µA
VLC						
V_{BTH}	VG Minimum Drive Voltage		1.4	1.6	1.8	V
A_V	Proportional Coefficient (d_{VG}/d_{VDS})		63	71	79	V/V
V_Z	Zener Clamping Voltage		5.0	5.7	6.2	V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SEL						
$V_{SEL(H)}$	High Logic Voltage	V_{DD}>5V	2.8	3.4	4.0	V
$V_{SEL(L)}$	Low Logic Voltage		1.1	1.4	1.7	V
$T_{B1(EN)}$	Blanking Time for Prohibiting Enable Signal Generation	SEL floating	200	250	300	ns
$T_{B2(EN)}$		SEL connected to GND	400	500	600	ns
VG						
$V_{G(low)}$	Output Voltage Drop at Low Level	I_{VG}=-100mA		0.04		V
$V_{G(high)}$	Output Voltage Drop at High Level	I_{VG}=100mA, V_{DD}=9V		0.2		V
$I_{VG(SRC)}$	Maximum Source Current			1		A
$I_{VG(SNK)}$	Maximum Sink Current			4		A
R_{SNK}	Pull Down Impedance	I_{VG}=100mA		0.4		Ω

Typical Characteristics

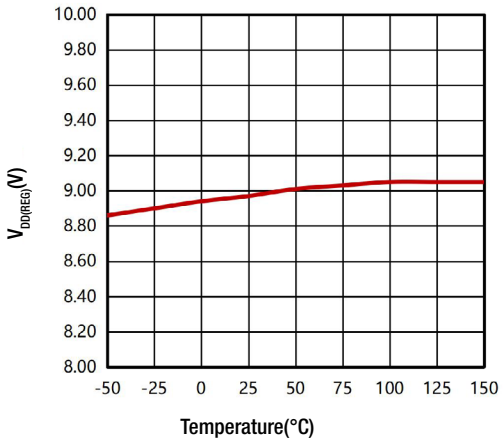


Fig. 1 $V_{DD(REG)}$ vs Temperature

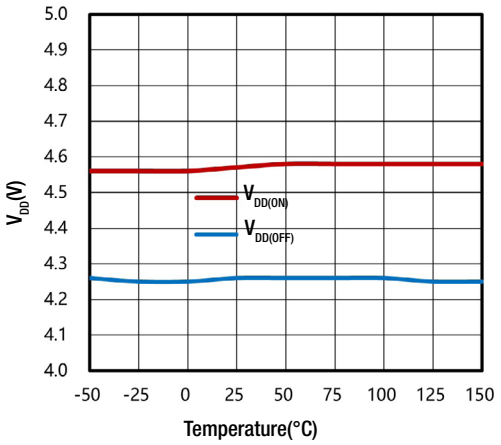


Fig. 2 $V_{DD(ON)}$ and $V_{DD(OFF)}$ vs Temperature

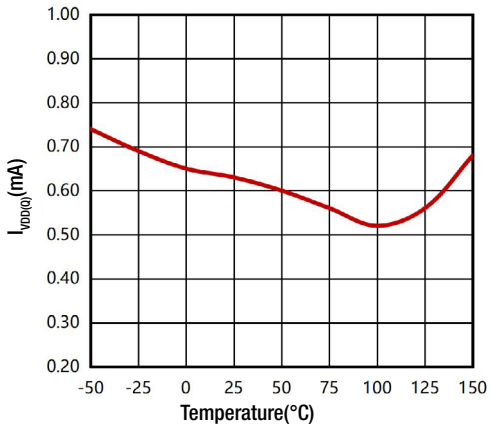


Fig. 3 $I_{VDD(Q)}$ vs Temperature

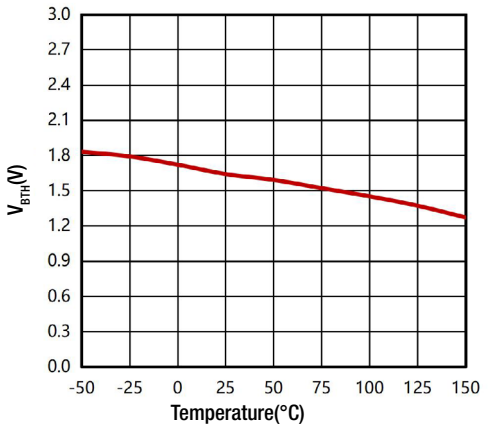


Fig. 4 V_{BTH} vs Temperature

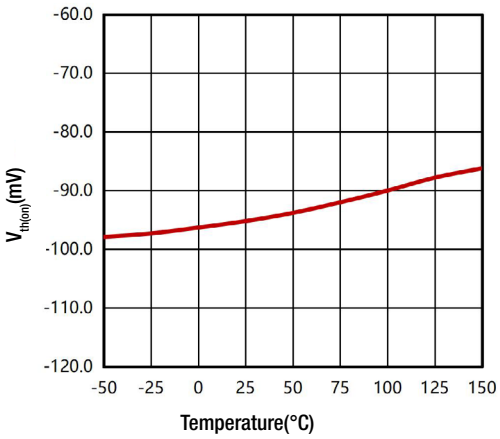


Fig. 5 $V_{th(on)}$ vs Temperaturew

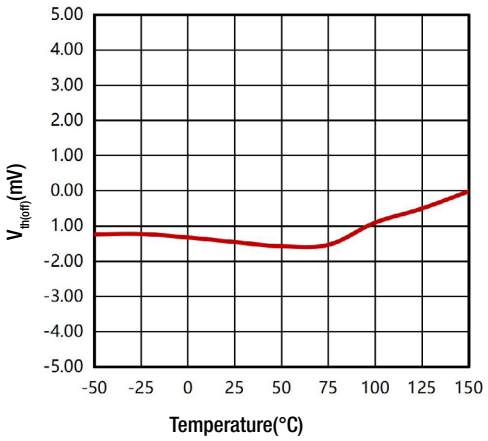


Fig. 6 $V_{th(off)}$ vs Temperature

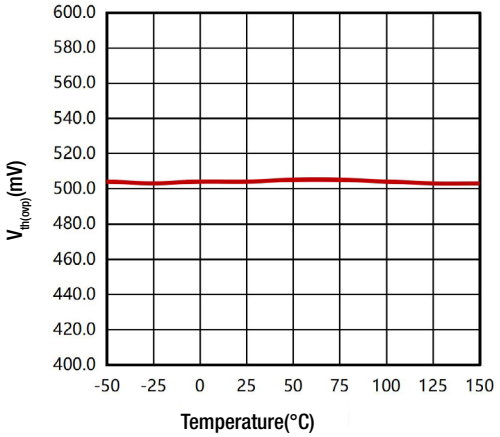


Fig. 7 $V_{th(OVP)}$ vs Temperature

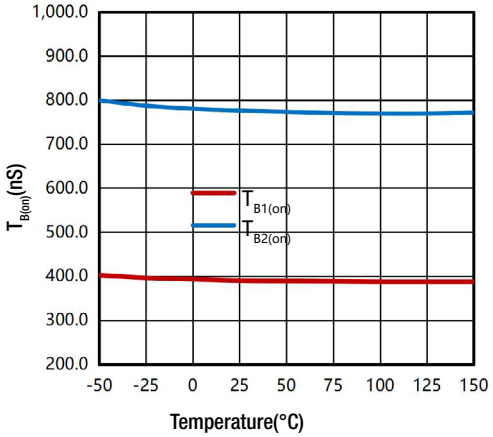


Fig. 8 $T_{B1(on)}$ and $T_{B2(on)}$ vs Temperature

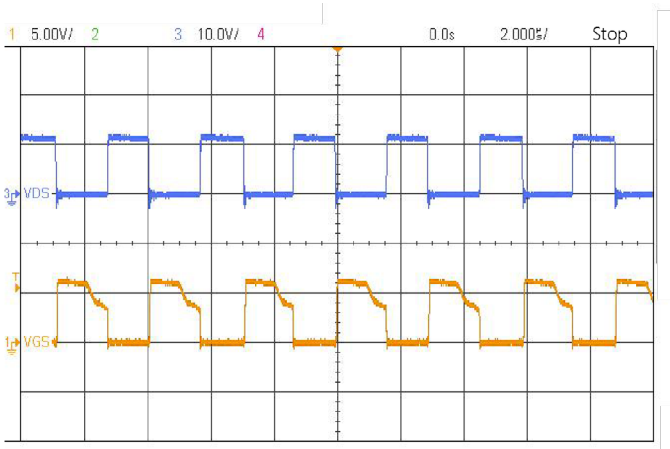


Fig. 9 V_{IN}=15V, V_O=5V, I_O=4A, F_{SW}=330kHz

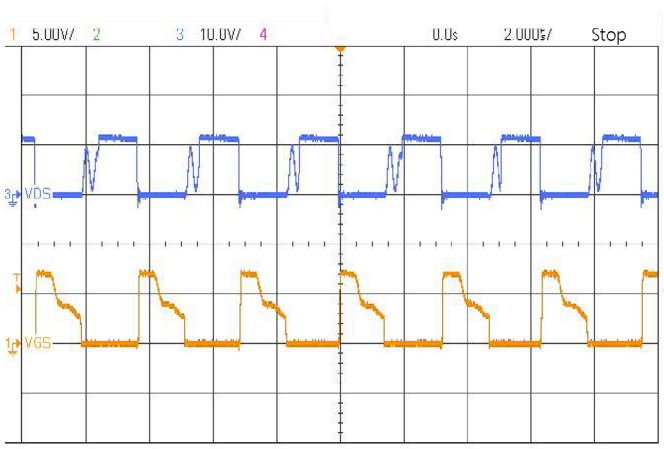


Fig. 10 V_{IN}=15V, V_O=5V, I_O=2A, F_{SW}=330kHz

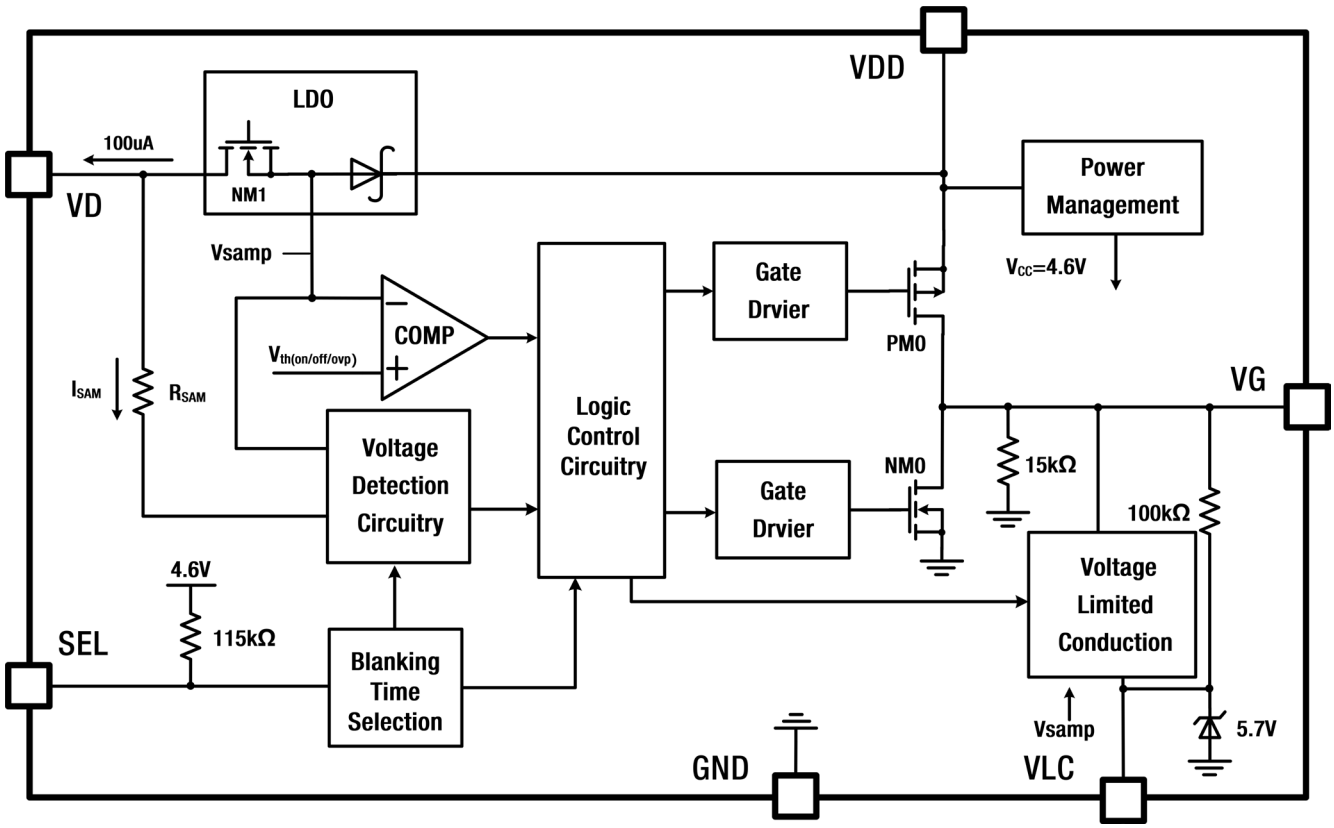
DETAILED DESCRIPTION

Overview

RVSY018 is a high-performance synchronous rectifier (SR) controller that supports operation in Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), Quasi-Resonant (QR) mode, and Active Clamp Flyback (ACF) topologies. The device supports operating frequencies up to 700kHz. Two selectable turn-off detection blanking times-400ns or 800ns-can be configured via the logic level applied to the SEL pin. The parameters for voltage-limited conduction can be adjusted through the VLC pin to match the characteristics of the selected SR MOSFET, enabling optimal adaptive performance.

The RVSY018 monitors the drain voltage of the SR MOSFET via the VD pin and includes a built-in 100µA current source. The turn-off threshold is programmable using a resistor between the VD pin and the MOSFET's drain. The path from VD to VDD also functions as a linear regulator with strong power supply capability, typically eliminating the need for an auxiliary winding. The VD pin is designed to withstand negative voltage transients, ensuring stable internal operation even under large negative V_{DS} conditions.

FUNCTIONAL BLOCK DIAGRAM



FEATURE DESCRIPTION

VDD Supplies

The VD-to-VDD path in the RVSY018 functions as a linear regulator, generating a steady-state voltage of approximately 9V at the VDD pin. However, if the duty cycle of the VD high-level pulse is low or the high-level voltage is insufficient, the resulting VDD voltage may fall below the expected steady-state level. To reduce voltage ripple at the VDD pin, it is recommended to connect a 0.68µF to 2µF filter capacitor between VDD and GND. Since the charging current from VD to VDD can exceed 100mA before VDD reaches the startup threshold, using a filter capacitor around 1µF typically does not cause significant startup delay.

Before VDD rises above the startup threshold $V_{DD(ON)}$, the VG pin remains at a low level. Once V_{DD} exceeds $V_{DD(ON)}$, all internal circuits become active, and VG is allowed to output a high-level signal. If V_{DD} subsequently drops below the lockout threshold $V_{DD(OFF)}$, the RVSY018 stops normal operation and the VG pin is pulled low again.

Turn-on Phase

The V_{DS} voltage of the SR MOSFET must fall below the turn-on threshold voltage $V_{TH(ON)}$ to enable turn-on. This threshold must be greater than the body diode voltage to ensure correct operation. For the RVSY018, $V_{TH(ON)}$ is set to -95mV. However, in Discontinuous Conduction Mode (DCM), the resonant interaction between the inductor and parasitic capacitance can cause V_{DS} to drop well below $V_{TH(ON)}$, which can lead to false turn-on events. To address this, the RVSY018 employs relative maximum voltage detection technology to accurately identify the excitation stage of the transformer or magnetic element and generate an enable signal T_{EN}. The SR MOSFET will only turn on after T_{EN} is generated and V_{DS} falls below $V_{TH(ON)}$, effectively preventing false triggering due to resonant ringing. As illustrated in Figure 11, a current-mode detection method is used in conjunction with a relative voltage comparison. The VD pin produces a sampling current I_{SAM} across an external sampling resistor R_{SAM}. A slowly decaying follower current I_C is maintained by the relative maximum voltage detection circuit. When I_{SAM} approaches I_C, the follower is refreshed so that I_{SAM}= I_C, forming peak-tracking currents I_{C1}, I_{C2}, etc. These currents correspond to relative maximum values and trigger corresponding enable signals T_{EN1}, T_{EN2}, and so on.

Typically, relative maximum value can only be detected during the excitation phase of the V_{DS} waveform, avoiding interference from parasitic ringing. However, in certain power supply designs, the first one or two cycles of ringing may closely resemble the excitation voltage. To mitigate this, the RVSY018 incorporates a blanking time $T_{B(EN)}$, during which relative maximum value detection is disabled and no enable signal is generated. If V_{DS} drops to a low level during $T_{B(EN)}$, the internal timer is restarted, automatically extending the blanking period until V_{DS} no longer falls below the threshold. This ensures that the SR MOSFET is not turned on by mistake. Once V_{DS} stabilizes, the blanking function is revoked and will resume detection in the next switching cycle.
Therefore, even under extremely light load conditions-when the excitation time is very short-the relative maximum value can still be accurately sampled without being affected by the blanking mechanism $T_{B(EN)}$.

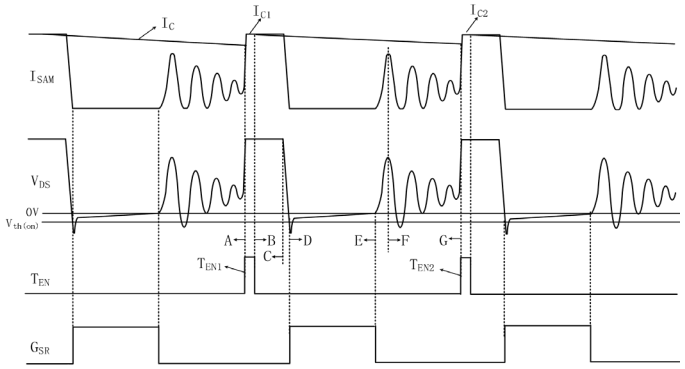


Fig. 11

Blanking Time Selection

The RVSY018 includes a blanking time selection pin (SEL) that allows users to configure internal blanking durations based on specific application needs. When the SEL pin is left floating, the IC internally pulls the pin voltage high. In this state, the turn-off comparator blanking time is set to $T_{B1(ON)}$=400ns, and the enable signal suppression time is set to $T_{B1(EN)}$=250ns. Conversely, if the SEL pin is connected to GND, the IC selects longer blanking times, with the turn-off comparator blanking time set to $T_{B2(ON)}$=800ns and the enable signal suppression time set to $T_{B2(EN)}$=500ns.

Intelligent Voltage Limited Conduction

The RVSY018 adopts programmable intelligent voltage-limited conduction technology, allowing it to adapt to the characteristics of the selected SR MOSFET and optimize efficiency across the entire load range. The behavior of this function is determined by the connection configuration of the VLC pin. There are three supported connection methods for the VLC pin, each corresponding to a different conduction mode:
① In general, the VLC pin can be left floating. At this time, the relationship between V_G and V_{DS} in the voltage-limited conduction stage is:

$$V_G = V_{BTH} + \frac{100k\Omega}{1.4k\Omega} \times |V_{DS}| = 1.6V + 71 \times |V_{DS}|$$

Among the control parameters, V_{BTH} represents the minimum voltage threshold for voltage-limited conduction. It is a fixed value with a negative temperature coefficient, and its variation with temperature is illustrated in Figure 4. At room temperature, V_{BTH} = 1.6V. The gate voltage V_G decreases as the forward voltage drop V_F of the SR MOSFET decreases. This behavior serves two primary purposes. First, it slightly increases the on-resistance $R_{DS(ON)}$ of the SR MOSFET, ensuring that the device is not turned off prematurely when V_F is very small but the MOSFET still needs to conduct. Second, the gate drive voltage is reduced just enough to lower V_F, thereby improving efficiency, without compromising proper conduction. Additionally, this mechanism helps reduce turn-off delay, as a large negative V_{DS} voltage forward-biases the MOSFET's body diode, which often exhibits slow reverse recovery characteristics. An excessive negative V_{DS} increases recovery time and leads to longer sampling delays. The relationship between V_{DS} and V_G during this process is illustrated in Figure 12. As the drain current through the SR MOSFET decreases, V_{DS} gradually approaches the turn-off threshold $V_{TH(OFF)}$.

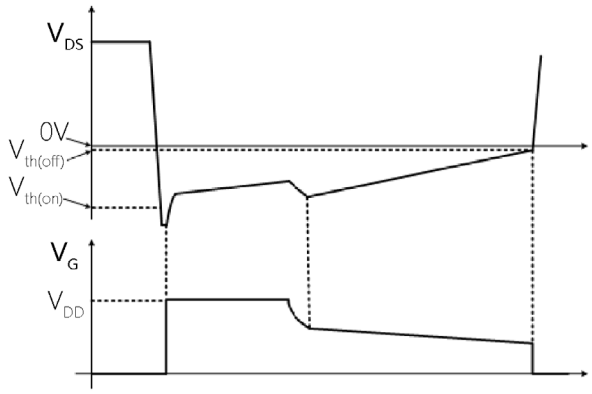


Fig. 12

②If the SR MOSFET has a low threshold voltage, particularly when $R_{DS(ON)}$ is very small, it may experience premature turn-off under light load conditions. To mitigate this, a resistor R_L can be connected between the VG pin and the VLC pin, as illustrated in Figure 13, to intentionally reduce the gate drive voltage. This adjustment helps maintain conduction without premature shutdown. Under these conditions, the relationship between V_G and V_{DS} during the voltage-limited conduction stage is defined as:

$$V_G = V_{BTH} + \frac{100k\Omega||R_L}{1.4k\Omega} \times |V_{DS}| = 1.6V + \frac{100k\Omega||R_L}{1.4k\Omega} \times |V_{DS}|$$

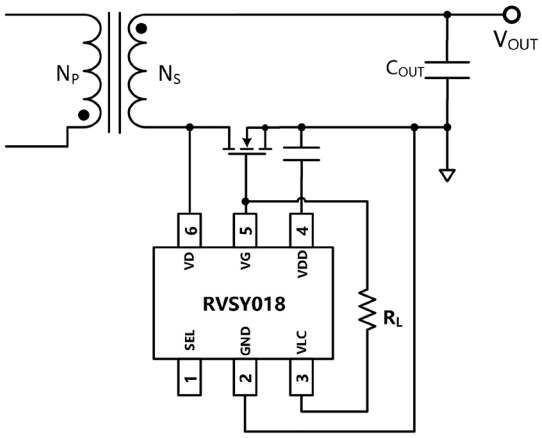


Fig. 13

③If the SR MOSFET has a high threshold voltage or a large $R_{DS(ON)}$, a resistor R_H can be connected between the VG pin and GND, as shown in Figure 14, to increase the gate drive voltage and thereby enhance conduction efficiency. In this configuration, the relationship between V_G and V_{DS} during the voltage-limited conduction stage is defined as:

$$V_G = \left(1 + \frac{100k\Omega}{R_H}\right) \times V_{BTH} + \frac{100k\Omega}{1.4k\Omega} \times |V_{DS}| = \left(1 + \frac{100k\Omega}{R_H}\right) \times 1.6V + 71 \times |V_{DS}|$$

If R_H=0, the maximum gate drive voltage equals the VDD voltage, and there is no voltage-limited driving.

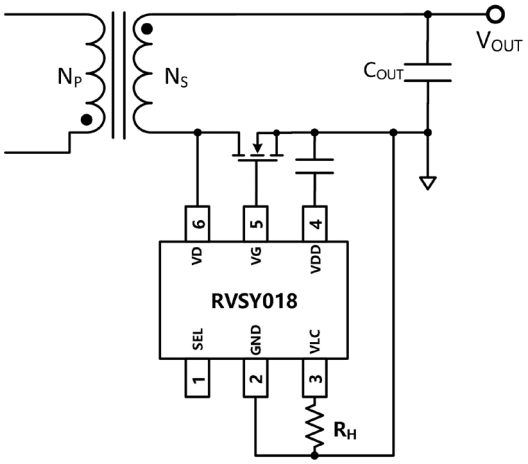


Fig. 14

Turn-off Phase

After the SR MOSFET is turned on, the overvoltage comparator remains active throughout the entire turn-on phase. Once the V_{DS} voltage exceeds Vth(ovp) and persists for longer than $T_{D1(ovp)}$ or $T_{D2(ovp)}$, VG is immediately pulled low to quickly turn off the SR MOSFET. After the SR MOSFET is turned on, the turn-off comparator is enabled following a blanking time delay of $T_{B1(ON)}$ or $T_{B2(ON)}$. Once the V_{DS} voltage exceeds $V_{th(off)}$, VG is immediately pulled low to quickly turn off the SR MOSFET. The VG pin of the RVSY018 has a 4A pull-down capability, with minimal turn-off delay. Additionally, a resistor R_{VD} is connected between the VD pin and the drain of the SR MOSFET to program the turn-off threshold voltage, as shown in Figure 15. In this case, $V_{th2(off)}$=$V_{th(off)}$-100μA×R_{VD}.

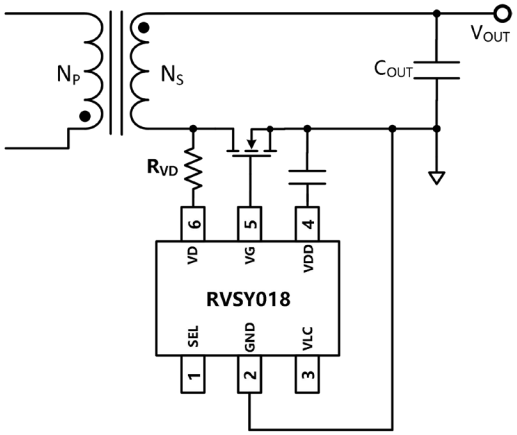
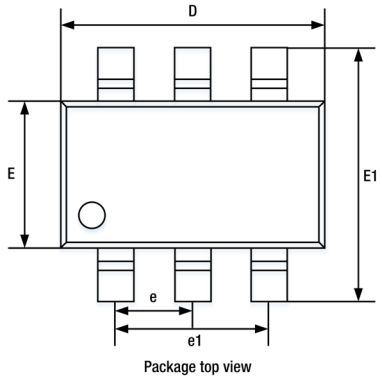


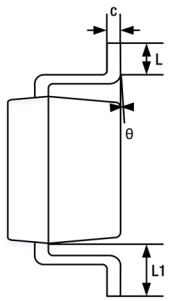
Fig. 15

PACKAGING INFORMATION

SOT23-6

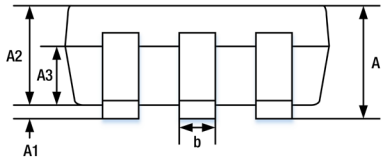


Package top view

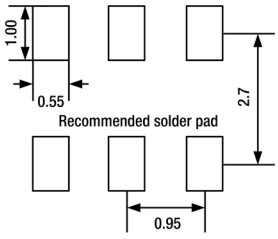


Package side view

DIMENBSION TABLE			
SYMBOL	MILLIMETER		
	MINMUN	NOMINAL	MAXMUN
A	-	-	1.25
A1	0.04	-	0.12
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33	-	0.50
c	0.14	-	0.20
D	2.82	2.92	3.02
E	1.50	1.60	1.70
E1	2.6	2.8	3.0
e	0.95 BSC		
e1	1.90 BSC		
L1	0.59 REF		
L	0.35	0.45	0.60
θ	0°	-	8°



Package front view



ORDER INFORMATION

Device	Package Type	PIN	Packaging Method	QTY	Marking Code*	MSL
RVSY018-SR-R	SOT23-6	6	Tape and Reel	3000	RVSY018	MSL-3
RVSY018-SR-CT	SOT23-6	6	Moisture Barrier Bag	10	RVSY018	MSL-3

*Marking Code:
RVSY018—— Product Code