RVPW012 Current Mode PWM Controller

4-80VIN/132V/0.2Ω POWER MOSFET

FEATURES

- 4V~80V Ultra-wide Range of Input Voltage
- PSR Feedback Minimum Sampling Time as low as 0.4μS
- Turn on in Boundary Conduction Mode (BCM) at the Heavy Load
- Integrated 132V/0.2Ω LDMOS
- Integrated Lossless Current Sampling
- Programmable Peak Current
- Programmable Power MOSFET Driving Speed
- Programmable Input Undervoltage and Overvoltage Protection
- Short Circuit Protection, and Over Temperature Protection
- Decrease the Operating Frequency to Improve Efficiency Under Light-load Conditions
- Programmable Power MOSFET Driving Speed
- Programmable Feedforward Compensation
- Programmable Soft Start
- Internal PSR Loop Compensation
- Output Diode Voltage Drop Temperature Compensation
- QFN5x5 Strong Heat Dissipation Packaging

APPLICATIONS

- Energy Storage Isolation Power Converters
- Industrial Power Conversion
- BMS Auxiliary Power Supplies
- POE Power Supplies
- Isolation Communication Power Supplies

DESCRIPTION

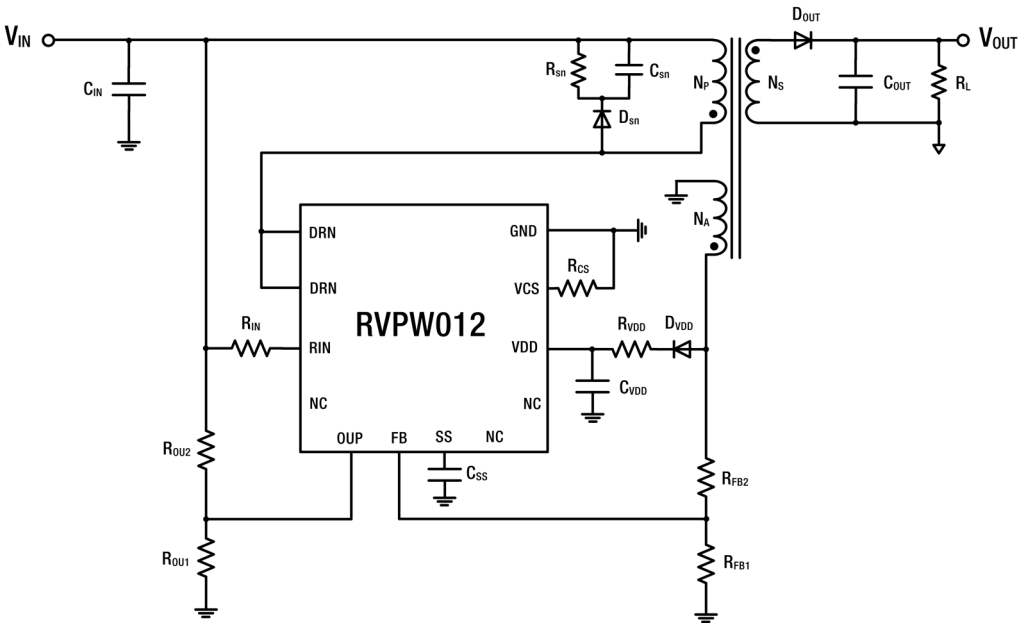
RVPW012 is a flyback converter that achieves voltage regulation by sampling the primary winding of the transformer, enabling Primary Side Regulation (PSR) feedback at operating frequencies of several hundred kHz. Its internal output voltage sampling circuit requires a sampling voltage time width as short as 400 nanoseconds. The built-in loop compensation circuit, featuring a fast dynamic response, ensures excellent stability and responsiveness of the switching power supply.

RVPW012 integrates multiple control functions and requires only simple peripheral components, which can be configured according to actual design needs. It supports three key functions-startup, feedforward compensation, and programming the shutdown speed of the internal power MOSFET-using external resistors. Additionally, the peak current of the power MOSFET can be programmed via a resistor for “lossless” current sensing. With two resistors, both input undervoltage and overvoltage protection thresholds can be set simultaneously. The device also includes comprehensive protection features such as overload protection(OLP), output short-circuit protection(SCP), output overvoltage protection(OVP), and overtemperature protection(OTP). It is capable of self-recovery once abnormal conditions are resolved, thereby maximizing the reliability of the switching power supply system.

Device information

Part Number	Package	Weight(mg)	Dimension	SPQ
RVPW012	QFN5x5	61.12	5.0 mm x 5.0 mm	4000

SIMPLIFIED SCHEMATIC



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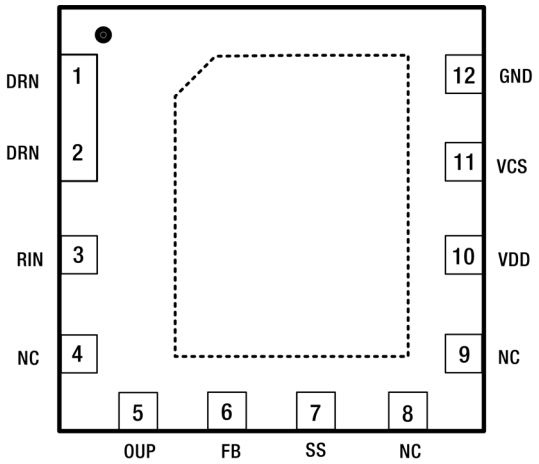
PIN CONFIGURATION AND FUNCTIONS



Name	No.	Type	Description
DRN	1,2	O	Pins 1 and 2 are connected together, they are the drain of the internal LDMOS.
RIN	3	I	Connecting an external resistor to VIN can achieve the functions of starting, power MOSFET shutdown speed adjustment, and feedforward compensation.
NC	4, 8, 9	---	No function pin, no electrical connection.
OUP	5	I	Input overvoltage\undervoltage protection multiplexed pin. The input undervoltage protection threshold and recovery threshold can be designed by the proportional coefficient of the peripheral voltage divider resistors, and the input overvoltage protection threshold can be designed by the resistance value of the voltage divider resistors.
FB	6	I	Output voltage feedback pin. This port can sample the output voltage of the switching power supply through auxiliary winding or directly using two voltage divider resistors.The sampled voltage is modulated by an error amplifier to adjust the duty cycle of the power MOSFET, in order to stabilize the output voltage of the switching power supply.
SS	7	I	Soft-start pin. The internal 28uA current source flows out of this pin to charge the external Soft-start capacitor, and the ramp voltage generated by charging controls the error amplifier output voltage VEA rising gradually , which controls the duty cycle of the converter unfolding gradually when the converter start-up.
VDD	10	P	The power supply port of the chip, VDD generates an internal power supply V_{CC} through low dropout voltage LDO to supply power to the control circuit, the LDO operates in the linear region with a V_{CC} voltage of 5.3V, and operates in the dropout voltage region, there is a dropout voltage approximately 0.3V between VDD and V_{CC}. VDD also has a voltage clamp function, the clamping voltage is about 10V, if the current absorbed by the clamp exceeds 6.3mA, the power MOSFET is prohibited from being turned on and enters a self-recovery protection state.
VCS	11	I	Peak current threshold setting pin. Connect a resistor of tens of KΩ to GND, and set the maximum and minimum peak current range for internal lossless current sampling.
GND	12	P	The reference ground of the chip. This port is the signal ground for internal control logic and also the source of the internal LDMOS.
EP	---	P	Die bonding pad. This pad is bonded to the bottom of die. and can be connected to GND. The pad must be fully connected to the PCB board to facilitate heat of die dissipation.

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SPECIFICATIONS

Absolute Maximum Ratings

		MIN	MAX	UNIT
RIN to GND	V_{RIN}	-0.3	35	V
VDD to GND	V_{DD}	-0.3	13	
DRN to GND	V_{DRN}	-1.3	132	
FB to GND	V_{FB}	-0.5	6	
The peak current of FB to GND	$I_{FB(PEAK)}$		-2.5	mA
Other pins to GND	V_{COM}, V_{CS}, V_{OUP}	-0.3	6	V
Maximum operating junction temperature	T_{JMAX}		150	°C

Stress exceeding the absolute maximum rated value may cause permanent damage to the device. These are only stress ratings and do not imply that the device operates beyond the recommended operating conditions under these or any other conditions. Long term exposure to absolute maximum rated conditions may affect the reliability of the device. All voltages are related to grounding. The current is positive input and negative output.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model HBM, per ESDA/JEDEC JS-001-2023; (Zap 1 pulse, Interval :>=0.1S)	±2000	V
		Charged device model CDM, per ESDA/JEDEC JS-002-2022	±1000	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Thermal Resistance

Packaging	θ_{JA}	Ψ_{JT}	UNIT
QFN5x5	62.5	3.11	°C/W

Note: The measurements were made on a test plate with a thickness of 1oz and an area of 7.62 x 11.43CM

Recommended Operatings Conditions

		MIN	NOM	MAX	UNIT
Power MOSFET drain voltage	V_{DRN}			125	V
VDD input voltage	V_{DD}	4		10	
VCS external resistor	R_{CS}	10			kΩ
RIN external resistor	R_{IN}			1	MΩ
FB Current	I_{FB}	-2			mA
Operating ambient temperature	T_A	-40		125	°C

Electrical Characteristics

Unless otherwise specified, the following parameters were measured under the condition of V_{DD}= 7V and temperature T=25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD						
$V_{DD(ON)}$	VDD turn on threshold	V_{DD} rising	3.1	3.3	3.5	V
$V_{DD(OFF)}$	VDD turn off threshold	V_{DD} falling	2.8	3.0	3.2	V
$I_{VDD(ON)}$	VDD turn on current	V_{DD} rising		61	100	μA
$I_{VDD(UVP)}$	Operating current under Input voltage	OUP= 0V		143	200	μA
$V_{DD(DMAX)}$	MOSFET for starting up supply voltage@D_{MAX}	F_{DRN}=330kHz, D_{MAX}=80%	2.8	3.4	4.6	V
$V_{BV(DIODE)}$	Break voltage of anti reflow diode		37			V
$V_{DD(OVP)}$	VDD overvoltage shutdown threshold	V_{DD} rising	9.5	10	10.8	V
$I_{VDD(OVP)}$	VDD absorbs current during overvoltage protection	V_{DD}= $V_{DD(OVP)}$	5.5	6.3	7.5	mA

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SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RIN						
V_{ZB}	MOSFET for starting up bias Voltage	$I_{RIN=}$1uA	6.0	6.9	8.0	V
$R_{IN(IN)}$	Input resistance			100		kΩ
VCS						
$V_{CS(MAX)}$	Maximum threshold voltage		1.85	2.00	2.15	V
$V_{CS(MIN)}$	Minimum threshold voltage		200	300	380	mV
K_{CS}	Proportional coefficient between peak current of power MOSFET and VCS current		27900	33000	38100	A/A
OUP						
$V_{OUP(ON)}$	Undervoltage protection turn-on voltage		1.9	2.0	2.1	V
$V_{OUP(OFF)}$	Undervoltage protection turn-off voltage		1.67	1.75	1.83	V
$V_{OUP(OC)}$	Input overcurrent protection clamp voltage	I_{OUP}=50uA injected into OUP pin	2.1	2.2	2.4	V
$I_{OUP(OFF)}$	Input overcurrent protection comparison current	I_{OUP} gradually increasing	92	100	108	uA
$I_{OUP(ON)}$	Input overcurrent protection recovery comparison current	I_{OUP} gradually decreasing	83	90	97	uA
FB						
$V_{REF(REG)}$	Reference voltage of EA		1.97	2.00	2.03	V
A_V	Low frequency gain of EA			1400		V/V
$T_{D(SAMP)}$	Delay time of sampling			252	400	nS
K_{VTC}	The temperature coefficient of temperature compensation voltage			3.5		mV/ °C
I_{FB}	Pin output current			-40		nA
SS						
$V_{SS(OPEN)}$	Open circuit voltage of soft start pin		5.0	5.3	5.6	V
$V_{SS(SCP)}$	Short-circuit protection selection comparator threshold			3.5	3.8	V
I_{SS}	External soft start current		23	28	34	uA
$R_{SS(DIS)}$	Bleeder resistor			173		Ω
DRN						
$R_{DS(ON)}$	MOSFET on-state resistance	I_{DS}= 4A, T=25°C		200		mΩ
		I_{DS}= 4A, T=125°C		300		mΩ
f_{ST}	Start-up frequency	FB=SS=0	60	67	74	kHz
f_{osc}	Maximum operating frequency		300	330	360	kHz
f_{MIN}	Minimum operating frequency		0.85	1.15	1.45	kHz
$t_{ON(MIN)}$	Minimum on time	VCS float, drain connected to a 120Ω pull-up resistor and pull-up voltage 24V		300		nS
Other Protection Functions						
T_{SHDN}	Over temperature protection threshold		148	163	178	°C
$T_{SHDN(HYS)}$	Over temperature protection hysteresis			18		°C
$t_{DLY(OLP)}$	OLP trigger time	From V_{COM}> $V_{COM(OLP)}$ to enter protection		100		mS
T_{REST}	Rest time after self recovery protection			1.4		S

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Typical Characteristics

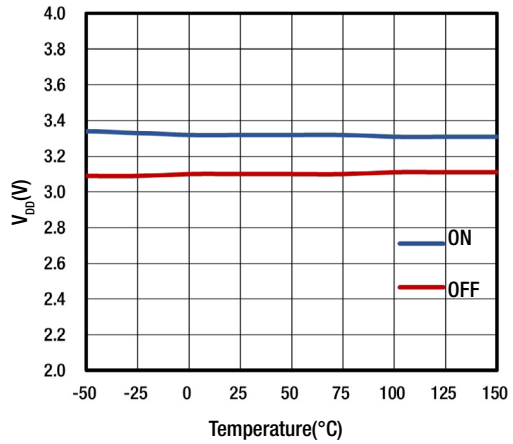

Fig. 1. $V_{DD(ON)}$ and $V_{DD(OFF)}$ vs Temperature

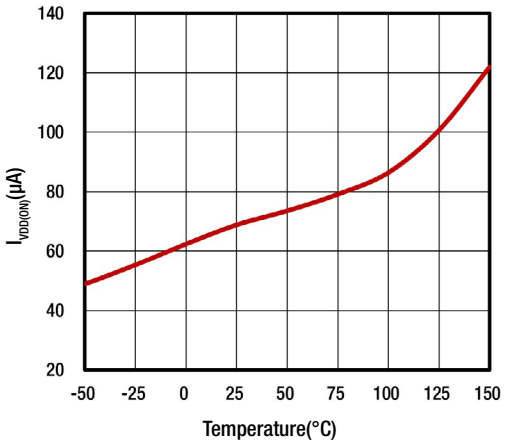

Fig. 2. $I_{VDD(ON)}$ vs Temperature

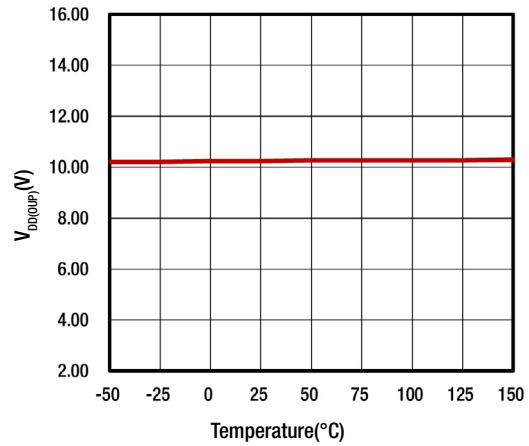

Fig. 3 $V_{DD(OVP)}$ vs Temperature

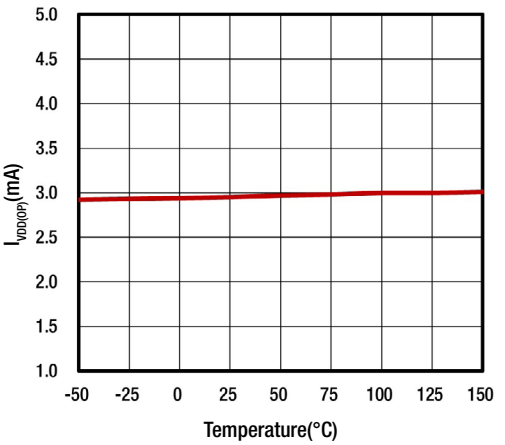

Fig. 4 $I_{VDD(OP)}$ vs Temperature

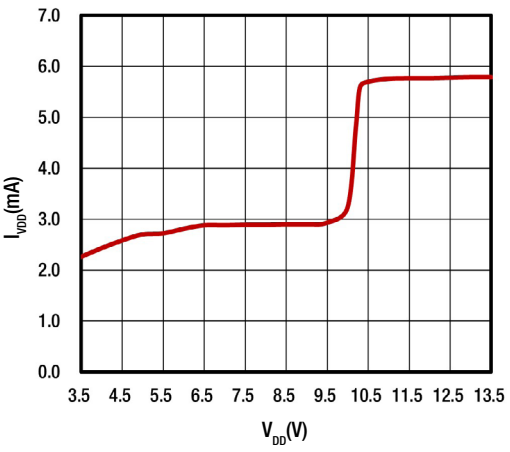

Fig. 5. V_{DD} vs I_{VDD}

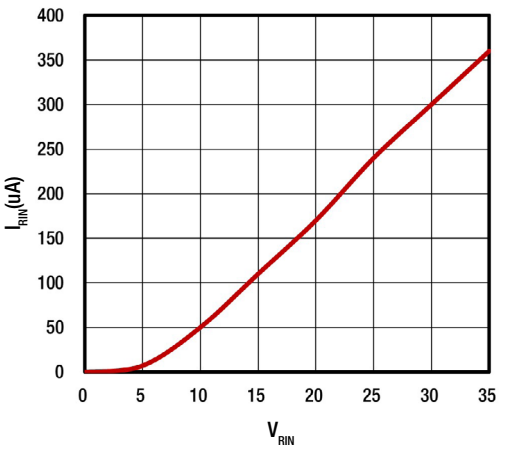

Fig. 6. V_{RIN} vs I_{RIN}

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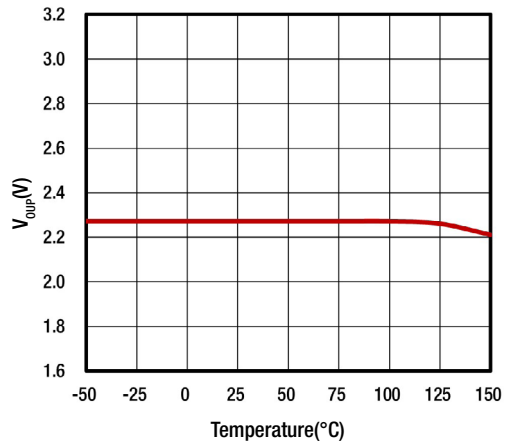

Fig. 7. $V_{OUP(OC)}$ vs Temperature

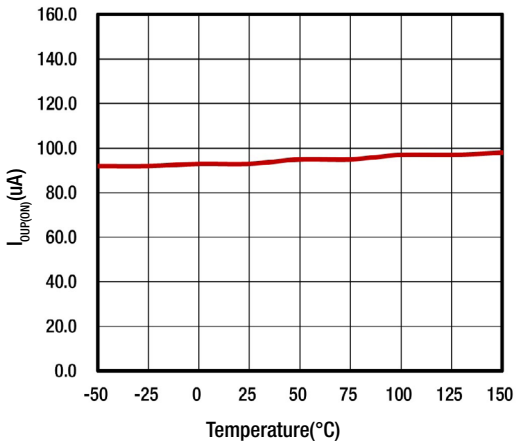

Fig. 8. $I_{OUP(ON)}$ vs Temperature

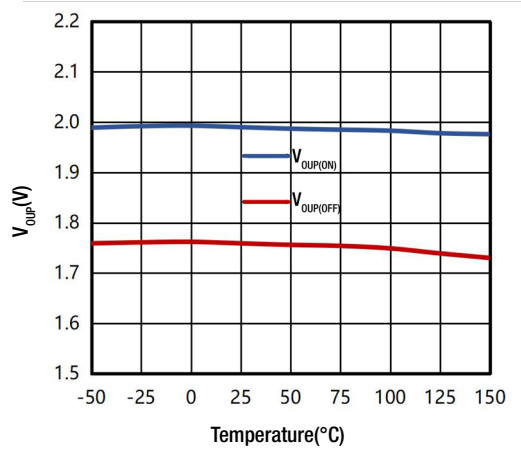

Fig. 9. $V_{OUP(ON)}$ & $V_{OUP(OFF)}$ vs Temperature

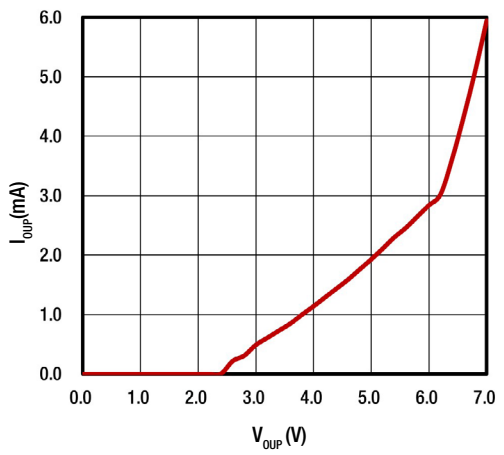

Fig. 10. I_{OUP} vs V_{OUP}

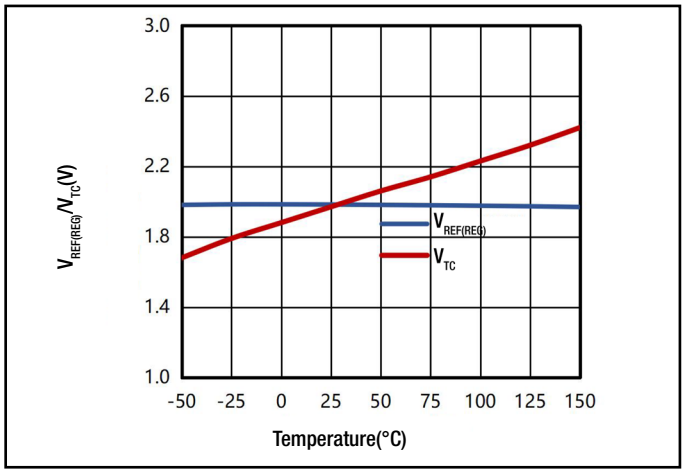

Fig. 11. $V_{REF(REG)}$ vs Temperature

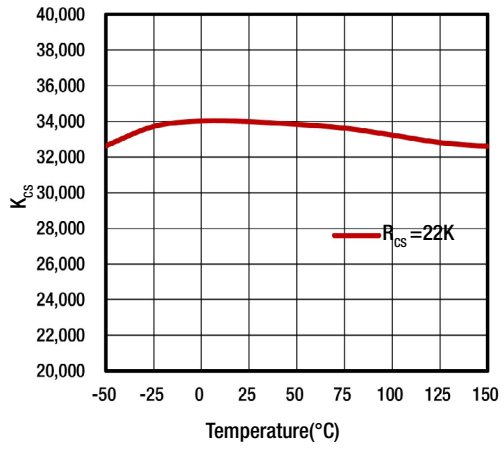

Fig. 12. K_{CS} vs Temperature

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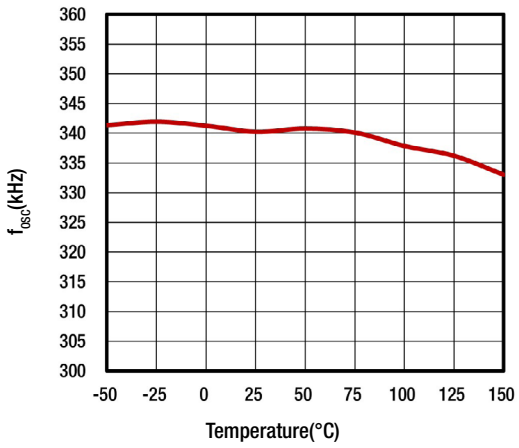

Fig. 13. f_{osc} vs Temperature

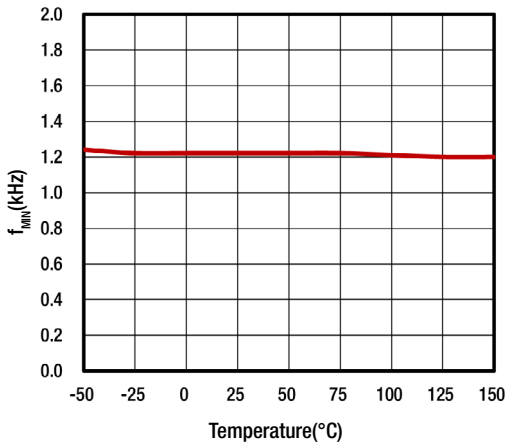

Fig. 14. f_{MIN} vs Temperature

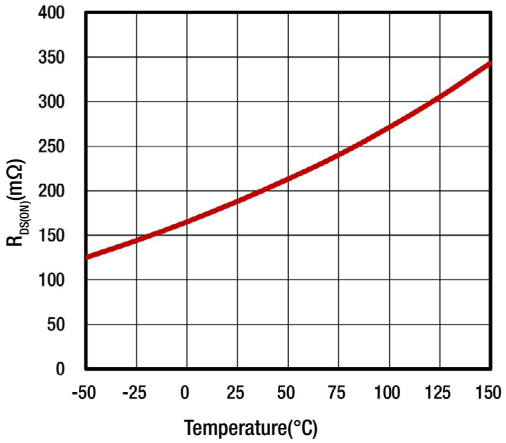

Fig. 15. $R_{DS(ON)}$ vs Temperature

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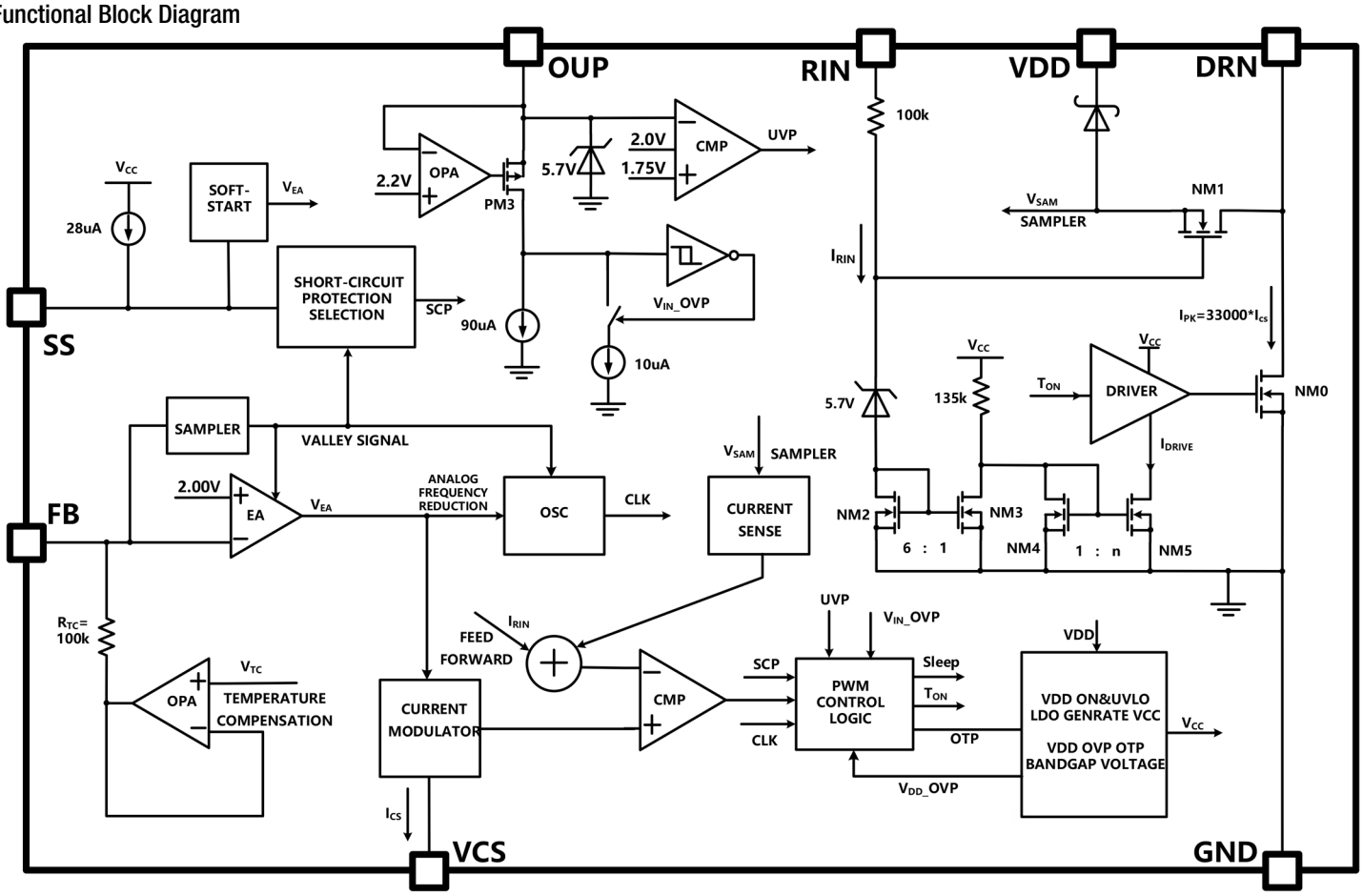
DETAILED DESCRIPTION

Overview

RVPW012 is a current-mode PWM converter that integrates control circuitry and a power MOSFET on a single die using advanced BCD technology. It is well-suited for flyback power converter applications. By sensing the output voltage through the transformer windings, the RVPW012 eliminates the need for isolation components such as optocouplers and feedback devices like the TL431. This simplifies the peripheral circuit and reduces overall system cost. Under heavy load conditions, the device switches at the first resonant valley following transformer degaussing, operating in boundary conduction mode (BCM). This mode of operation enables high conversion efficiency and superior EMI performance. RVPW012 integrates a power nLDMOS and supports programmable peak current limiting for the power switch, making it easy to maintain BCM operation across common load conditions. In addition to programmable peak current, various other parameters can be configured to suit specific application requirements. These include MOSFET turn-off speed, feedforward compensation, soft-start timing, output diode temperature compensation, and input undervoltage/overvoltage protection thresholds. RVPW012 supports the miniaturization of switching power supplies and is widely adopted in systems with broad input voltage ranges, including IGBT-based motor drives, industrial automation, medical instruments, and more.

Functional Block Diagram



Feature Description

Function and Resistance Value of External Resistor R_{IN}

Figure 16, a resistor RIN is connected between the R_{IN} pin of the RVPW012 and the converter's input voltage (V_{IN}). This resistor serves three primary functions: 1. it provides bias current for initiating the internal startup MOSFET (NM1); 2. it programs the shutdown speed of the internal power MOSFET (NM0); 3. it enables the feedforward compensation function.

Startup and Power Supply: R_{IN} resistor supplies bias current to a 5.7V Zener diode and NM2, which are connected between the gate and source of NM2. The sum of the Zener diode breakdown voltage and the gate-to-source voltage of NM2 is approximately 6.9V. This voltage provides the necessary bias for the startup MOSFET NM1. The startup current charges the VDD capacitor via the DRN pin (drain of NM0), through NM1 and a Schottky diode. After the converter's output voltage is properly established, it is recommended to use an auxiliary winding to supply power to the VDD pin. Due to the relatively high power consumption of the internal startup circuit, the VDD voltage should exceed 6V to ensure the startup circuit fully shuts down. Additionally, the VDD pin features a voltage clamp and overvoltage protection. The clamp voltage is 10V. If the current drawn by the clamp exceeds 6.3mA, overvoltage protection is activated and the IC enters a protection mode. In flyback converter applications, the proportional relationship between the auxiliary winding and the secondary output voltage allows VDD overvoltage protection to function as output overvoltage protection.

Switching Speed of Power MOSFET NM0: The input current I_{RIN} of the pin RIN is calculated to generate the driving current I_{DRIVE}, and their relationship is:

$$\frac{I_{DRIVE}}{n} = \frac{V_{CC} - V_{GS4}}{135k\Omega} - \frac{1}{6} \times \frac{V_{IN} - 5.7V - V_{GS2}}{R_{IN} + 100k\Omega}$$

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In the above equation, V_{CC}=5.3V and V_{GS2}=V_{GS4}≈1.2V. For example, if R_{IN}= 330kΩ and the equation yields zero, I_{DRIVE}=0 occurs when V_{IN}=85V. Under this condition, the internal gate driver turns NM0 on and off using only its intrinsic drive capability, resulting in the slowest shutdown speed. When I_{DRIVE}>0, the shutdown speed of NM0 increases accordingly. From this relationship, two key conclusions can be drawn: ① The shutdown speed of NM0 can be programmed by adjusting the value of R_{IN}. A larger resistance value results in faster shutdown. ② As the input voltage V_{IN} increases, I_{DRIVE} decreases, which slows down the shutdown speed of NM0. This behavior helps suppress voltage spikes caused by leakage inductance at high input voltages.

Feedforward Compensation Function: The current I_{RIN} flowing through NM2 is proportionally mirrored and used as a feedforward compensation current. This current is superimposed with the current sampled from the power MOSFET NM0 and the slope compensation current, and the total is fed to the PWM comparator. As the input voltage increases, the feedforward compensation current also increases, which helps reduce discrepancies in overcurrent detection thresholds between high and low input voltages. This compensates for delays in both PWM comparison and gate drive timing.

RIN Resistor Design Guidelines: RVPW012 includes an internal 100kΩ series resistor, which serves two purposes: First, it absorbs part of the applied voltage, allowing the use of compact, low-voltage-rated external resistors without compromising voltage withstand distance. Second, in low input voltage applications, the external R_{IN} resistor may be omitted altogether to simplify the circuit. There is no strict requirement for the R_{IN} value from a startup perspective. Its value should instead be selected based on a trade-off between the desired shutdown speed of NM0 and the effectiveness of feedforward compensation. Typically, R_{IN} values in the range of several hundred kΩ to 1MΩ are recommended.

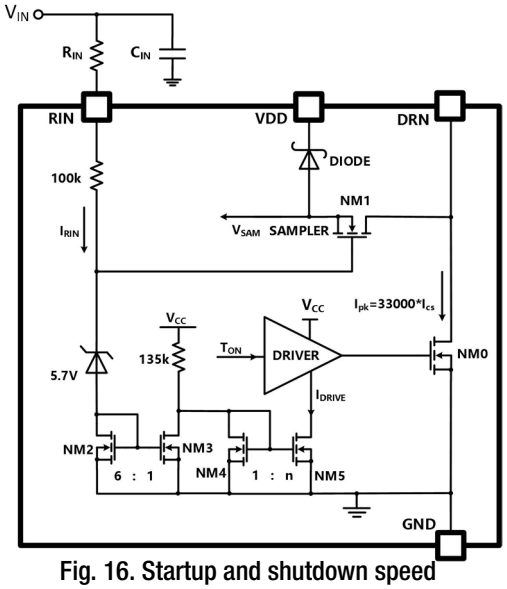

Fig. 16. Startup and shutdown speed

Input Over/Under Voltage Protection

Figure 17, the input overvoltage protection and undervoltage protection functions of the RVPW012 are implemented through a single pin, OUP. The threshold voltages for both protections can be programmed according to actual application requirements. The operating principle is as follows:

When the pin voltage is less than 2.2V, the pin does not draw current, the turn-on voltage and turn-off voltage of V_{IN} undervoltage protection can be easily calculated as follows:

$$V_{INON(UVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU1}} \times 2V$$

$$V_{INOFF(UVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU1}} \times 1.75V$$

When the voltage at the OUP pin exceeds 2.2V, the pin begins to draw current and stabilizes at this voltage until the current exceeds 100μA. At this point, the condition is recognized as an OUP input overcurrent event, and the chip disables switching of the power MOSFET NM0, entering a protection state. As the input voltage decreases and the drawn current falls below 90μA, the chip exits the protection state and resumes normal operation. The input overvoltage protection voltage and input overvoltage protection recovery voltage can be calculated as follows:

$$V_{INOFF(UVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU1}} \times 2.2V + 100\mu A \times R_{OU2}$$

$$V_{INON(UVP)} = \frac{R_{OU1} + R_{OU2}}{R_{OU1}} \times 2.2V + 90\mu A \times R_{OU2}$$

When designing the resistance values of R_{OU1} and R_{OU2} , a more practical formula can be obtained to quickly determine the resistance:

$$R_{OU2} = \frac{V_{INOFF(OVP)} - 1.1 \times V_{INON(UVP)}}{100\mu A}$$

As long as the operating range of the input voltage of the converter is determined, R_{OU2} can be calculated, and then combined with the undervoltage protection formula, R_{OU1} can be calculated.

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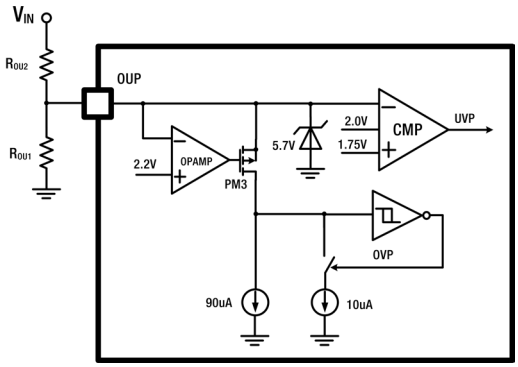

Fig. 17. Input over/under voltage protection

Short Circuit Protection

RVPW012 integrates a short-circuit protection function for the output of the switching converter. When a short circuit occurs at the output, the feedback FB voltage drops significantly, making it impossible to detect the resonant valley. In this condition, an internal timer is triggered. If the valley detection failure persists beyond a predetermined duration, $t_{DLY(OLP)}$, the device enters open-loop protection mode. In this mode, pulse output at the DRN pin is disabled. After a predefined rest period, t_{SLEEP}, the chip automatically resumes operation.

If short-circuit protection is not required in a particular application, this function can be selectively disabled. The short-circuit protection is suppressed when the SS voltage is approximately 1.2V lower than the internal low-voltage supply V_{CC}. To ensure that the protection function remains inactive, even under minimum V_{CC} variation, it is recommended to clamp the SS voltage below 3.8V. The bias current flowing out of the SS pin is 28μA. To achieve this clamping effect, a 120kΩ resistor should be connected between the SS pin and ground (GND).

PWM and PFM Control

Current Sampling: Current sampling is achieved by detecting the conduction voltage drop of the power MOSFET NM0 at the source of the startup MOSFET NM1. This voltage is replicated by an internal operational amplifier and applied to a sampling MOSFET, which is of the same type as NM0 but designed with a higher internal resistance. As a result, an induced current proportional to the peak current I_{PK} of NM0 is generated through the sampling MOSFET, enabling accurate current measurement.

Current Modulator: The pulse-width modulation voltage V_{EA} generates a modulation current across the external resistor connected to the VCS pin. As illustrated in Figure 18, the relationship between V_{EA}, V_{CS}, and the switching frequency f_{DRN} shows that V_{CS} follows the variation in V_{EA}. This behavior modulates the current across the external resistor, thereby controlling the peak current of NM0 and regulating the converter's output voltage. When V_{EA} exceeds 2.75V, V_{CS} reaches its maximum value, $V_{CS(MAX)}$, which in turn limits the maximum peak current of NM0. To ensure adequate demagnetization time for the FB pin to accurately sample the output voltage, the minimum value of V_{CS} is clamped to $V_{CS(MIN)}$=300mV. This sets the minimum energy transferred per switching cycle and requires the presence of sufficient dummy load under no-load conditions to prevent output voltage drift.

PWM Control: The modulation current generated from V_{EA} serves as the positive input to the PWM comparator. Meanwhile, the combined current-consisting of the sampled current from NM0, the slope compensation current, and the feedforward compensation current-is applied to the comparator's negative input. The comparator then outputs a pulse-width signal to drive NM0, maintaining the converter's output voltage at the desired regulated level. In the BCM operating state, the output power and frequency can be calculated by the formula:

$$P_{OUT} = 0.5 \times I_{PK} \times V_{IN} \times D \times \eta$$

Where I_{PK} is the peak current of the power MOSFET, V_{IN} is the input voltage, η is the conversion efficiency of the transformer, and D is the duty cycle, which is:

$$D = \frac{N_{PS} \times (V_{OUT} + V_F)}{N_{PS} \times (V_{OUT} + V_F) + V_{IN}}$$

where N_{PS} is the transformer primary and secondary winding turns ratio, V_F is the output diode voltage drop. The formula for the operating frequency is as follows:

$$f_{DRN} = \frac{V_{IN}}{L_P \times I_{PK}} \times \frac{N_{PS} \times (V_{OUT} + V_F)}{N_{PS} \times (V_{OUT} + V_F) + V_{IN}}$$

PFM Control: The operating frequency of the RVPW012 varies according to three distinct states. First, during the BCM operating state-such as in the C to D stage shown in Figure 18 as the load on the switching converter decreases, the modulation voltage V_{EA} gradually drops. Consequently, the peak current, excitation time, and demagnetization time all reduce, leading to a gradual increase in the operating frequency, as indicated by the f_{DRN} formula. Second, with a further decrease in load, the operating frequency may exceed the maximum limit of 330kHz. This situation is most likely to occur under light load conditions and high input voltages, as illustrated by the red solid line in stages B to C of the figure. At this point, the frequency becomes fixed at its maximum value, and the system stops switching at the first resonance valley. As a result, it exits BCM and transitions into DCM. Third, at even lighter loads, to improve efficiency and reduce no-load power consumption, the RVPW012 activates its analog frequency reduction function. As the converter load continues to decrease, the V_{EA} voltage declines further, leading to a corresponding reduction in operating frequency. Due to the primary-side regulation (PSR) control, the output voltage can only be sampled during the transformer's demagnetization stage, requiring the minimum operating frequency to be limited to f_{MIN}=1.15kHz.

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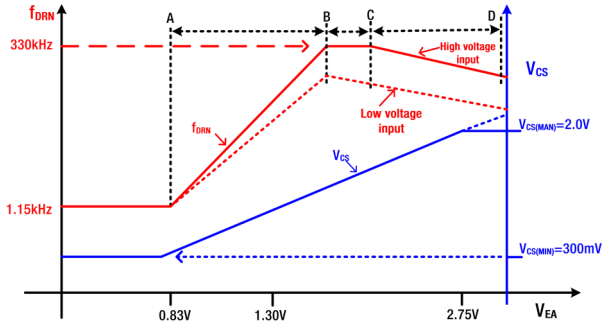

Fig. 18. Variation curves of switching frequency and peak current modulation with V_{EA}

Peak Current Setting of Power MOSFET

The peak current of the power MOSFET NM0 in the RVPW012 is regulated by a current modulator, which adjusts the current I_{CS} based on the voltage at the VCS[11] pin and the external resistor R_{CS}. The current through the power MOSFET is 33,000 times greater than I_{CS}. The value of R_{CS} can be calculated using the following formula:

$$R_{CS} = 33000 \times \frac{V_{CS(MAX)}}{I_{PK}}$$

Among them: $V_{CS(MAX)}$ is the maximum threshold voltage of VCS pin,with a typical value of 2V; I_{PK} is the maximum peak current of the primary winding of the flyback converter.

FB Pin PSR Feedback Voltage Sampling

RVPW012 senses the output voltage of the switching power supply through the transformer's auxiliary winding. A sampling resistor connected to the auxiliary winding feeds the signal to the FB pin. During the transformer's demagnetization stage, the sampled voltage serves as the negative input to the error amplifier EA, where it is differentially compared with the positive reference voltage $V_{REF(REG)}$=2V. This comparison generates the duty cycle modulation voltage V_{EA}, which in turn controls the converter's duty cycle, as illustrated in Figure 19. The corresponding auxiliary winding voltage waveform is shown in Figure 20. Once the feedback loop stabilizes, the sampled voltage at the FB pin equals the EA reference voltage of 2V. Based on this, the following calculation can be made:

$$V_{FB} = (V_{OUT} + V_F + I_S R_S) \times \frac{N_A}{N_S} \times \frac{R_{FB1}}{R_{FB1} + R_{FB2}} = 2V$$

$$V_{OUT} = \frac{N_S}{N_A} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \times 2V - (V_F + I_S R_S)$$

Voltage Sampling and Load Regulation: In the transformer, N_S and N_A represent the turns of the secondary output winding and the primary auxiliary winding, respectively. R_{FB1} and R_{FB2} are the sampling resistors connected to the auxiliary winding, V_F is the forward voltage drop of the output diode, I_S is the secondary output current, and R_S is the total resistance of the transformer's secondary output circuit. From the formula analysis, it can be seen that the term $I_S R_S$ influences the load regulation of the switching power supply's output and should be minimized wherever possible. To address this, the RVPW012 samples the voltage at the FB pin at the end of the transformer's demagnetization stage-when the secondary current I_S reaches its minimum. In Discontinuous Conduction Mode (DCM), when I_S=0, the output voltage is no longer affected by the $I_S R_S$ drop, enabling higher output voltage accuracy. Therefore, to achieve precise output regulation, it is recommended to design the converter to operate in DCM. In Continuous Conduction Mode CCM, however, the presence of $I_S R_S$ causes the output voltage to decrease as the load increases.

RVPW012 uses a 20% drop in FB voltage as the condition to detect the end of the transformer's demagnetization period. Upon detection, a signal is sent to latch the output voltage of the error amplifier (EA). Because the EA output is designed with a delay, it remains stable during the brief moment when the FB voltage drops abruptly. As a result, the latched voltage effectively represents the FB level just before the sudden drop. In the early phase of demagnetization-immediately after the power MOSFET turns off-resonance between the transformer's leakage inductance and parasitic capacitance may cause significant fluctuations in the FB voltage. To prevent incorrect sampling during this period, a sampling delay $T_{D(SAMP)}$ is introduced, during which the sampler remains inactive. Sampling only occurs during the designated sampling time T_{SAMP}, and within this window, the peak-to-peak amplitude of the resonance must be limited to within 20% approximately 400mV of the FB platform voltage. When evaluating the equivalent voltage at the auxiliary winding, the voltage divider ratio of the sampling resistors must be taken into account. To maintain waveform integrity, it is strongly recommended not to place filter capacitors in parallel between the FB pin and ground. Such capacitors can distort the FB voltage waveform and degrade the output voltage accuracy, especially in high-frequency applications operating in the hundreds of kilohertz range. Additionally, under light-load conditions-when demagnetization time is short-the parasitic capacitance of oscilloscope probes may distort the FB waveform and affect output voltage performance. To balance waveform quality and power consumption in the sampling network, it is recommended that R_{FB1} be selected within the range of 2.5kΩ to 10kΩ, with a typical value of 6kΩ. Care should also be taken to ensure that the negative current flowing into the FB pin during transformer excitation does not exceed 2mA.

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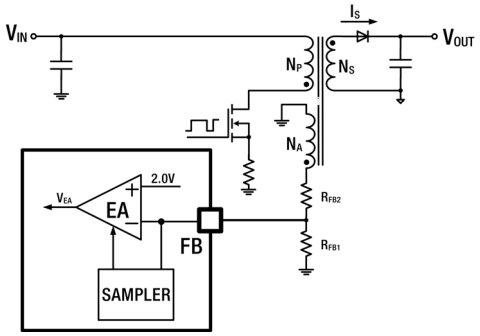

Fig. 19

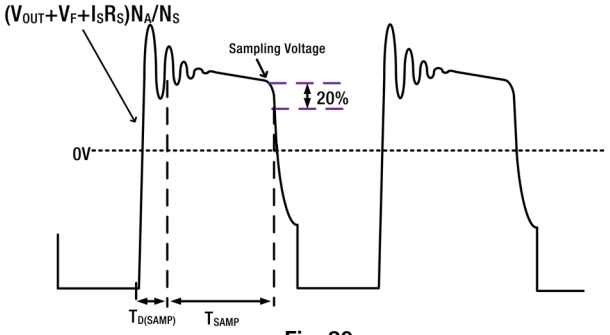

Fig. 20

Output Diode Temperature Compensation

Temperature Compensation Function: RVPW012 includes a selectable temperature compensation feature. As shown in Figure 21, the positive temperature coefficient voltage V_{TC} is buffered by a unity-gain amplifier to provide drive capability and is then connected to the FB pin through a resistor R_{TC}=100kΩ. V_{TC} has a temperature coefficient of +3.5 mV/°C and is equal to the reference voltage $V_{REF(REG)}$ at room temperature. This design enables the RVPW012 to provide temperature compensation in primary-side feedback flyback power supply applications. The magnitude of the compensation effect is determined by the value of the feedback voltage divider resistor R_{FB2}.

$$V_{OUT} = \frac{N_S}{N_A} \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \times V_{REF(REG)} - \{\frac{N_S}{N_A} \times \frac{R_{FB2}}{R_{TC}} \left[V_{TC} - V_{REF(REG)}\right] + V_D\}$$

In the above equation, N_S and N_A are respectively the turns of the secondary winding and auxiliary winding of the transformer, and V_D is the voltage drop across the output diode junction. To make the temperature coefficient of the output voltage small, taking the derivative of temperature to zero yields:

$$R_{FB2} = \frac{N_A}{N_S} \times \frac{\Delta V_D}{577.5mV} \times 100k\Omega$$

ΔV_D is the change in voltage drop of the output diode of the switching power supply from -40~125°C. Determine the size of R_{FB2} based on the temperature change value of the output diode junction voltage drop and the transformer turn ratio, and then determine the size of R_{FB1} based on the output voltage.

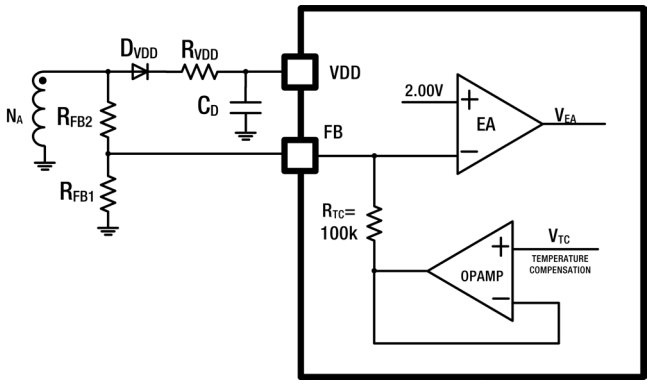

Fig. 21

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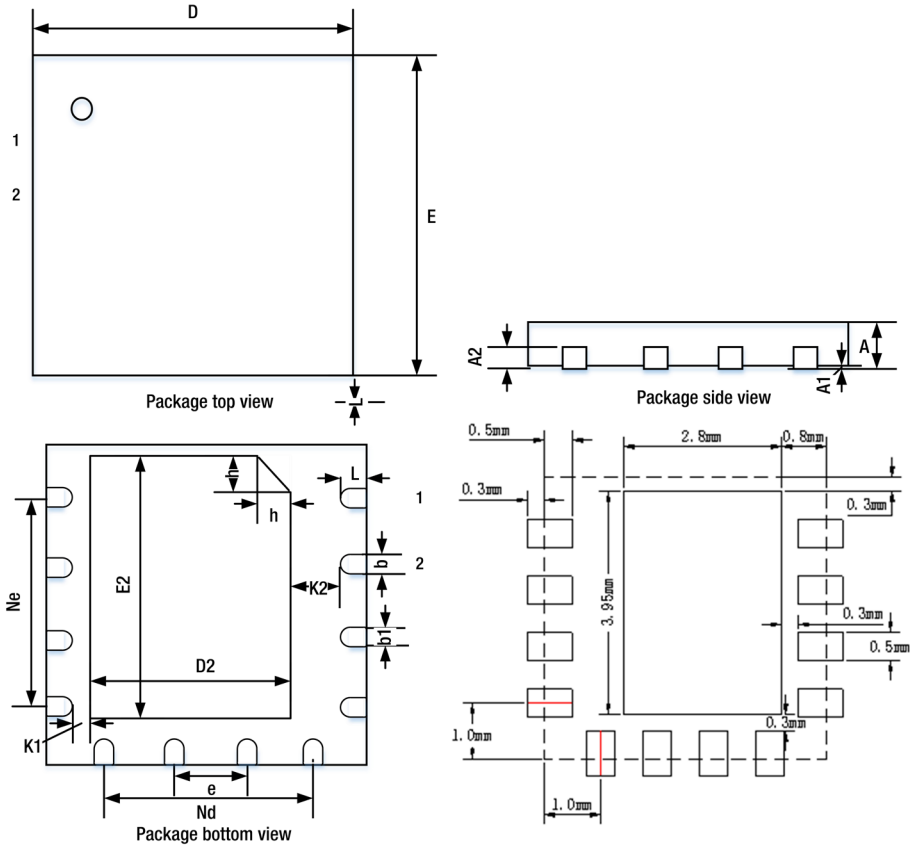
PACKAGING INFORMATION

QFN5x5-12L



DIMENSION TABLE			
SYMBOL	MILLIMETER		
	MINIMUM	NOMINAL	MAXIMUM
A	0.70	0.75	0.80
A1	-	0.02	0.05
A2		0.203 REF	
b	0.25	0.30	0.35
b1	0.17	0.22	0.27
D	4.90	5.00	5.10
D2	2.70	2.80	2.90
Ne		3.00 BSC	
e		1.00 BSC	
E	4.90	5.00	5.10
E2	3.85	3.95	4.05
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K1	0.35	0.40	0.45
K2	0.95	1.00	1.05

ORDER INFORMATION

Device	Package Type	PIN	Packaging Method	QTY	Marking Code*	MSL
RVPW012-FJ2-R	QFN5x5-12L	12	Tape and Reel	4000	RVPW012	MSL-3
RVPW012-FJ2-CT	QFN5x5-12L	12	Moisture Barrier Bag	10	RVPW012	MSL-3

*Marking Code :
RVPW012—— Product Code

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