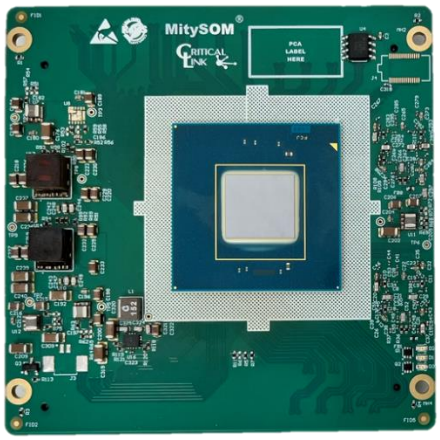
FEATURES

- **Agilex 5 E-Series FPGA / Processor from Altera**
  - Device Group A or B support
  - Up to Quad Hard Processor System
    - Dual core Cortex-A76@1.4/1.8GHz(1)
      - 64 KB L1 Instruction Cache
      - 64 KB L1 Data Cache
      - 256 KB L2 Unified Cache
    - Dual core Cortex-A55@1.2/1.5GHz(1)
      - 64 KB L1 Instruction Cache
      - 64 KB L1 Data Cache
      - 128 KB L2 Unified Cache
    - 2 MB L3 Cache (Shared)
  - 512 KB on-chip RAM
- **Memory**
  - Up to 8 GB HPS FPGA shared LPDDR4
    - 32 bits wide
    - 10.6/14.9 GB/sec burst rate(1)
  - Up to 8 GB FPGA LPDDR4(2)
    - 32 bits wide
    - 10.6/14.9 GB/sec burst rate(1)
  - Up to 128 MB QSPI Configuration FLASH
- **FPGA Fabric**
  - Up To 656K Logic Elements (LE)
  - Up to 1 GHz Clock Routing
  - Up To 31.4 Mb M20K Memory
  - Up to 6.8 Mb MLAB Memory
  - Up To 1692 Fixed Point Multipliers
  - Up to 22/26 TOPS w/AI Tensor Blocks(1)
  - 32 Global Clock Networks
- **FPGA IO**
  - 146 User FPGA HVIO Pins(2)
    - 1.8/2.5/3.3V CMOS
  - 216 User FPGA HSIO Pins(2)
    - 24 1.1V Single Ended
    - 2x 96 pin banks supporting 1.1V/1.2V/1.3V standards
    - Up to 108 LVDS pair supported
    - MIPI D-PHY to 2.5/3.5 Gbps(1)
  - 48 HPS IO Pins
  - Up to 24 Transceiver Pairs(2)
- **Serial Transceivers**
  - Up to 24 at 17.16/28.1 Gbps(1)
  - Up to six x4 PCIe 4.0(3)/PCIe 3.0 Hard IP Blocks, End Point or Root Port
  - 10/25 GbE MAC(1), PCS, FEC



- **Mechanical**
  - 82 mm (3.23”) x 82mm (3.23”) size
  - 2x 400 pin board to board connectors
  - 1x 30 pin top expansion connector(2)
- **Hard Processor System (HPS) IO**
  - Up to 3 10/100/1000/2500 Mbps Ethernet MACs with TSN Support
  - 1 USB 2.0 On-The-Go (OTG) Port
  - 1 USB 3.1 Gen 1 Superspeed Port
  - 2 UARTs
  - 1 MMC/SD/SDIO
  - 2 SPI Masters and 2 SPI Slaves
  - 5 I2C/2 I3C controllers
- Integrated Power Management
- Power, Reset and Clock Management
- Integrated Secure Device Manager with encryption acceleration.

APPLICATIONS

- Robotics
- Image Processing
- Embedded AI processing
- Embedded/Industrial Instrumentation
- Embedded/Industrial Automation and Control
- Medical Instrumentation

BENEFITS

- Rapid Development / Deployment
- Multiple Connectivity and I/O Options
- High System Integration
- Supports Altera FPGA AI Suite
- Supports HLS acceleration
- High Level OS Support
  - Embedded Linux

(1) Dual parameters above represent Agilex 5E Device Group B/Group A specified performance; Critical Link offers options for both device groups. CPU speeds are maximum speeds based on available speed grade options.
(2) See Table 2 for I/O Scaling based on Density
(3) PCIe 4.0 available on Speed Grade 4 and faster devices

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DESCRIPTION

The MitySOM-A5E is a highly configurable, small form-factor System-on-Module (SOM) featuring an Agilex 5 SoC FPGA E-Series from Altera. In addition to the processor, the module includes on-board power supplies, an LPDDR4 RAM memory subsystem, and SPI NOR Flash configuration memory. The MitySOM-A5E provides a complete and flexible CPU infrastructure for highly integrated embedded systems.

The MitySOM-A5E is available with up to a 656K Logic Element (KLE) Agilex 5E which provides a Quad Core Hard Processor Subsystem (HPS) including a dual-core Cortex-A76 and a dual-core Cortex-A55. Options for 85, 138, 282, 434, and 524 KLE devices are also possible. The HPS can run a rich set of real-time operating systems containing software applications programming interfaces (APIs) expected by modern system designers. The ARM architecture supports several operating systems, including Linux.

Figure 1 illustrates a block diagram of the MitySOM-A5E. As shown in the figure, the primary interface to the MitySOM-A5E is through two 400 Pin vertical board-to-board mezzanine connectors, J1 and J2. The MitySOM-A5E is intended to interface to a carrier card base module for applications development. Details of the board-to-board interfaces are included in the Interface Description section. The MitySOM-A5E J1 is pin compatible with the MitySOM-A5E Mini SOM J1 connector.

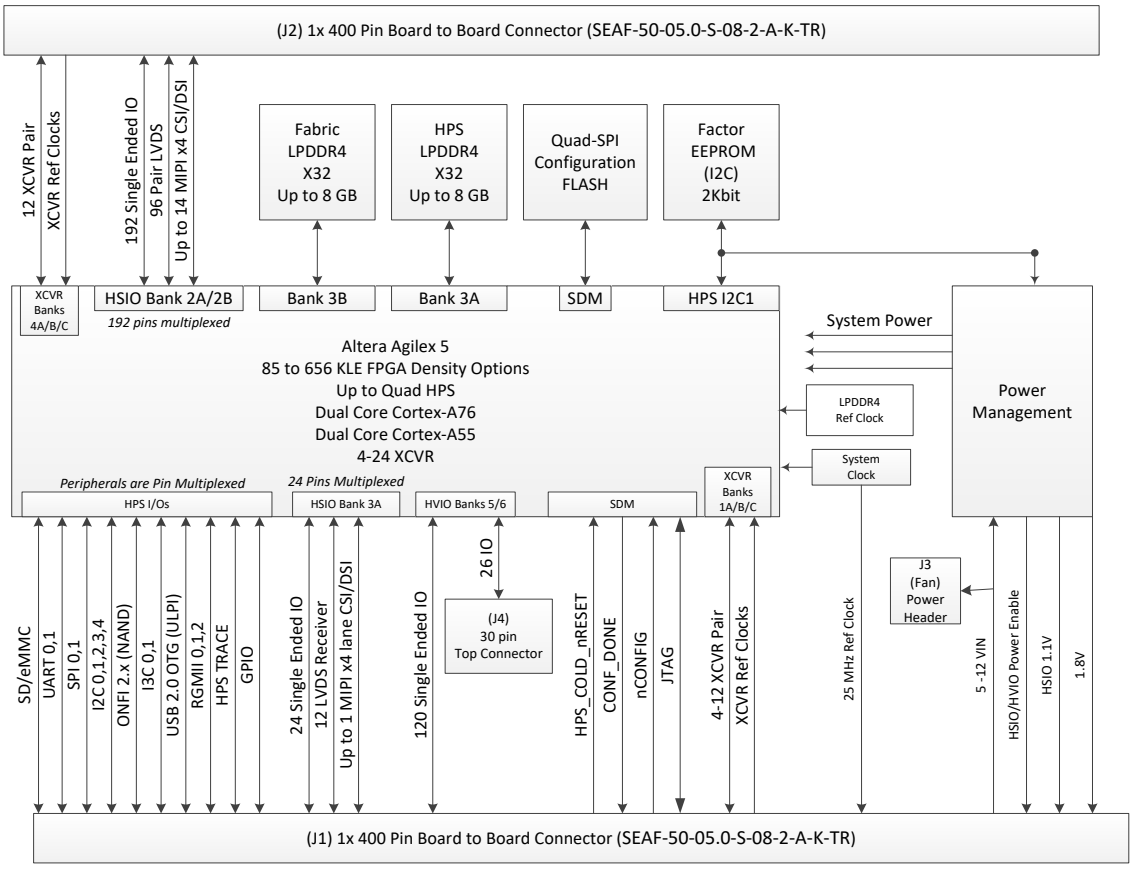

Figure 1 MitySOM-A5E Block Diagram

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LPDDR4 Memory – HPS Shared Memory

The MitySOM-A5E includes a dedicated HPS 32-bit LPDDR4 memory interface that can address a maximum of 8GB of RAM. This LPDDR4 memory is available for both the HPS as well as the FPGA fabric through an AXI high speed interface internal to the Agilex 5E.

The MitySOM-A5E family adheres to Altera's Agilex 5E maximum memory speeds as defined by device speed grade. The HPS memory is clocked up to 1333MHz by default for Group B devices and up to 1866MHz for Group A. Refer to Figure 3 for the maximum supported DDR data rate for each speed grade.

LPDDR4 Memory – FPGA Dedicated Memory

The MitySOM-A5E includes a dedicated FPGA fabric 32-bit LPDDR4 memory interface that can address a maximum of 8GB of RAM. This LPDDR4 memory is available for the FPGA fabric through an AXI high speed interface internal to the Agilex 5E. It is possible to bridge HPS access to this memory, but it will not be as efficient for the HPS as compared to the dedicated HPS memory bank.

The MitySOM-A5E family adheres to Altera's Agilex 5E maximum memory speeds as defined by device speed grade. The HPS memory is clocked up to 1333MHz by default for Group B devices and up to 1866MHz for Group A. Refer to Figure 3 for the maximum supported DDR data rate for each speed grade.

HPS-FPGA AXI

The high bandwidth HPS-FPGA AXI bridges provided by Altera in the Agilex 5E SoC allow masters in the FPGA fabric to communicate with slaves in the HPS logic and vice versa. These bridges can be configured for 32, 64, or 128 bit widths.

For example, designers can instantiate additional memories or peripherals in the FPGA fabric, and master interfaces belonging to components in the HPS logic can access them. Designers can also instantiate components such as a Nios® V processor in the FPGA fabric and their master interfaces can access memories or peripherals in the HPS logic, including

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LPDDR4 Memory – HPS Shared Memory.

Configuration EEPROM

MitySOM-A5E modules contain a 2048 x 8-bit EEPROM that is used to hold factory configuration data for the module. The EEPROM is connected to the Agilex 5E using the HPS I2C1 interface. This EEPROM contains information such as the module type, Serial Number, and MAC addresses for the Ethernet interface(s). This EEPROM is not available for customer use.

Dedicated HPS Interfaces

The following HPS interfaces have been dedicated as fixed function in order to support proper operation. The module was designed to allow as many HPS fixed and Shared IO pins to be user accessible as possible. See the J1 connector interface description for information on HPS and FPGA Shared IO pins that may be user defined.

Console Serial port

The console serial port (UART1) is supported on pins E40 (RX) and F37 (TX) of the 400 pin Samtec connector (J1) with 1.8V compatible asynchronous UART I/O. By default, the flow control signals are not enabled but can be added to the console serial interface if desired.

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I2C1 Interface

The I2C1 peripheral is consumed local to the module. It is used for the Configuration EEPROM, as well as power supply monitoring.

Table 1 I2C0 Peripherals

Address	Device	Feature
1010000	CAT24C256WI-GT3	256Kbit EEPROM for factory configuration parameters
0001110	FS1525	0.7-0.85V Core Power Supply
0001101	FS1525	0.7-0.85V Core Power Supply*
0001011	FS1406	1.1V Power Supply
0001010	FS1406	1.0V Power Supply
0001001	FS1406	1.2V Power Supply
0001000	FS1406	1.8V Power Supply

- This supply will not be installed on SOMs with FPGAs having less than 434 KLEs.

Debug JTAG

The JTAG interface signals for the Agilex 5E FPGA fabric processor are available through the 400-pin Samtec connector.

JTAG Signal	Samtec Connector Pin	FPGA Pin
TCK	D44	CA112
TMS	F40	CA109
TDO	D42	BW112
TDI	D45	BW109

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SOM Clocking

The MitySOM-A5E has multiple oscillators to drive both the HPS and FPGA. There is a dedicated 25Mhz oscillator to drive the HPS reference clock. The SOM clock network is shown in Figure 2.

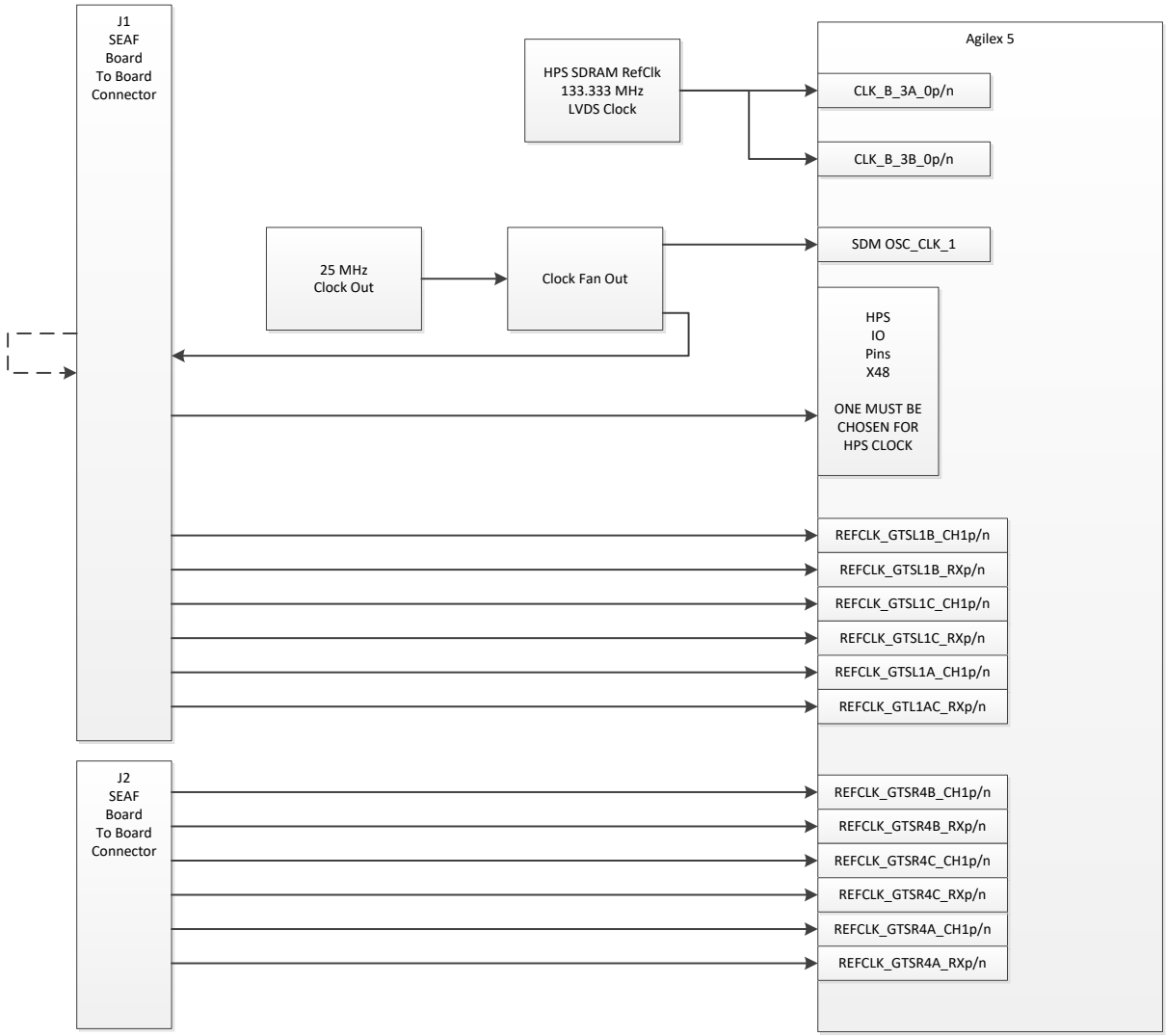

Figure 2 SOM Clocking

Note 1: The HPS clock *MUST* be looped back into an HPS IO pin, **otherwise the module will not boot**. The user may use any HPS IO pin for the HPS clock source. The SOM design requires looping the clock back on the baseboard to allow for maximum flexibility in multiplexed HPS IO selection so as not to remove a desired interface option.

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External Interfaces and I/O Scaling

The Agilex-5E supports functional pin multiplexing, providing a configurable set of external interfaces that can be adapted to a wide range of applications.

Within the Agilex-5 SoC architecture, the availability of HSIO and transceiver resources scales with FPGA density: higher-density devices expose a greater number of these high-speed interfaces, while lower-density devices provide a reduced set consistent with their intended use. In contrast, for smaller density devices (85KLE to 282KLE), additional HVIO resources are made accessible through a dedicated top-side connector (J4), providing expanded general-purpose I/O beyond the standard SOM pinout.

Table 2 MitySOM-A5 Standard SOM IO Availability summarizes these density-based characteristics and their impact on the SOM I/O count.

Table 2 MitySOM-A5 Standard SOM IO Availability

FPGA Density	HPS DDR	FPGA DDR	GXB Lanes (Banks)	HSIO (LVDS Pairs)	HVIO (SE IOs)
656 KLE	Y	Y	24 (6)	216 (108)	120
523 KLE	Y	Y	24 (6)	216 (108)	120
434 KLE	Y	Y	16 (4)	216 (108)	120
282 KLE	Y	N	12 (3)	120 (60)	146
138 KLE	Y	N	4 (1)	120 (60)	146
85 KLE	Y	N	4 (1)	120 (60)	146

HPS Interfaces

A list of the interfaces/functions that are available to the user from the HPS is provided below.

- 1 Universal Serial Bus (USB) 3.1 Gen 1 Super-Speed Controller
- 1 Universal Serial Bus (USB) 2.0 High-Speed On-The-Go Controller
- 2 Improved Inter-Integrated Circuit (I3C) Ports
- 5 Inter-Integrated Circuit (I2C) Ports
    - I2C1 is dedicated for use on J1 (pins A32/A33) with 4.7k ohm pull-up resistors at 1.8V and is available for user access.
    -
- Up to 2 Serial Peripheral (SPI) Ports
- 2 Universal Asynchronous Receive/Transmit (UART) Ports
- Up to 3 Ethernet MACs (10/100/1000/2500 Mbps) with TSN Support

Additionally, most of the pin multiplexed signals can be configured as general purpose I/O signals with interrupt capability.

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FPGA Interfaces

GPIO

The Agilex 5E offers up to 48 HPS GPIO signals and up to 340 general FPGA IO pins, all of which are available externally to the module.

The FPGA IO pins provided on J1(A to D) and are connected to Banks 3A, 5A, 5B, 6A, 6B, 6C, and 6D of the Agilex 5E FPGA. Banks 5A, 5B, 6A, 6B, 6C, and 6D have 120 pins supporting 1.8/2.5/3.3V CMOS logic, while Bank 3A supports 24 1.1V single ended logic signals. The FPGA IO pins on J2 (A to D) are connected to Banks 2A and 2B of the Agilex 5E FPGA. Banks 2A and 2B have a total of 196 pins supporting 1.1/1.2/1.3V singled ended IO as well as True Differential Signaling (TDS) standards including LVDS, D-PHY (used for MIPI protocols), and various HSTL standards. The FPGA IO pins on J4 are connected to Banks 6E and 6F of the Agilex 5E FPGA. Banks 6E and 6F support 1.8/2.5/3.3V CMOS logic. Bank 6E has 20 pins connected to J4, where Bank 6F has 6 pins connected to J4.

Several of the pins on banks 5 and 6 of the Agilex 5E also provide alternate functions for routing clock signals into the FPGA for use by the fabric and transceiver subsystems. Users are encouraged to refer to the Agilex 5E datasheet and technical reference manuals for more information.

LVDS / MIPI

There are up to 92 pairs on Banks 2A and 9B that may be used for LVDS or MIPI D-PHY signaling. Users should refer to the Agilex 5 FPGA IO guidelines and power the relevant bank voltage correctly for the desired standard (the VCCIO lines are available for 2A and 2B at the J2 connector interface).

In addition, up to 12 LVDS pairs may be configured as receivers utilizing the 24 pins available from Bank 3A. This pins support differential signaling and include support for MIPI DPHY transmitter or receiver configuration. Note: The differential IO pairs must honor the Agilex 5 Datasheet requirements for HSIO Bank pins. This requires adjusting the common mode of standard LVDS signals such that the maximum value of the pins do not exceed the Bank voltage levels.

Transceivers

A maximum of twenty-four (24) high speed transceiver pairs are available on the module for supporting high speed serial interfaces.

Maximum transceiver speed supported is 28Gbps for SOM modules configured with Agilex 5E device group A devices and 17Gbps for those configured with Agilex 5E device group B.

The number of transceiver pairs available is dependent upon device density. All 24 pairs are available in the 524KLE and 656KLE FPGA densities. 16 pairs are available in the 434KLE FPGA density. 12 pairs are available in the 282KLE FPGA density. And a total of four transceiver pairs is available in the 85KLE and 138KLE FPGA densities. 12 pairs are routed to J1 interface, and the additional 12 pairs are routed to the J2 interface. These pairs may be bonded to support protocols such as HDMI, DisplayPort, CoaXpress, PCIe, 10Gb Ethernet, Interlaken, CIPRI, JESD204B, etc.

PCIe 4.0 functionality is supported by all Group A devices, as well as on speed grade 4 Group B devices. Group B devices at speed grade 5 and slower are limited to PCIe 3.0 operation.

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Configuration and Boot Modes

The Agilex 5E MSEL pins (SDM_IO5, SDM_IO7, SDM_IO9) are used to configure the boot source for the SDM. On the MitySOM-A5E, the MSEL pins are strapped to fixed settings on the board as described below. The MitySOM-A5E provides a local 25 MHz clock source to the OSC_CLK_1 pin for SDM booting purposes.

Boot Media Configuration

The Agilex 5E is configured to boot from its Quad SPI flash using the MSEL pins set to [2:0] '011'b. The MSEL pins are pulled up to 1.8V or down to ground using 4.7k resistors on the SOM, selecting the boot mode "AS (Normal Mode)," as referenced in the Technical Reference Manual (TRM). These bootstrapping pins are not accessible to the user through the Samtec connector. The Agilex 5E may also be configured using the HPS or a JTAG interface.

HPS clocking

The MitySOM-A5E includes a 25 MHz clock output (HPS_CLKIN) on the J1 interface connector that is coherent with the local 25 MHZ clock used to drive the SDM OSC_CLK_1 pin. This clock should be routed back to one of the HPS IO pins to serve as the reference clock for the HPS PLL subsystem. Users may select which HPS IO pin to use based on their specific application need.

Debug LEDs

There are 3 debug LEDs on the MitySOM-A5E module.

Power Status LEDs

D3 illuminates, green, when the MitySOM-A5E on-module power supplies have been enabled in sequence and are operating correctly.

Configuration Debug

D2 is connected to the INIT_DONE pin on the Agilex 5E. When lit, green, it indicates the device has been initialized.

D1 is connected to the CONF_DONE pin on the Agilex 5E. When lit, green, it indicates the device configuration has been completed.

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Power Interfaces

Input Voltage

The MitySOM-A5E is powered using the VCC_IN input and ground pins on J1. The MitySOM-A5E accepts an input voltage from +5V DC up to +12V DC, and generates +2.5V, +1.8V, +1.2V, +1.1V, +1.0V, and +0.8V on the SOM. **Note**: for applications where the SOM FPGA is expected to consume greater than 15 Watts, Critical Link recommends operating the SOM above 6.5V.

Power utilization of the MitySOM-A5E is heavily dependent on end-user application. Major factors include: ARM CPU PLL configuration, CPU Utilization, and external LPDDR4 RAM utilization. Customers should use Altera's Early Power Estimator (EPE) for the Agilex 5E to better understand the power requirements of the system for power supply sizing for custom baseboards. This utility will assist in estimating the potential power usage of the processor for a given application.

In addition to the main power input rail, the MitySOM-A5E also requires combined input voltages for HVIO banks 6A and 6B, combined input voltages for HVIO banks 6C and 6D, input voltages for HSIO Bank 2A, and input voltages for HSIO Bank 2B. HVIO banks must be provided a voltage of 1.8V, 2.5V, or 3.3V depending on end user requirements. HSIO banks must be provided a voltage of 1.1V, 1.2V, or 1.3V depending on end user requirements. See the Agilex 5 FPGA fabric user's guide for more information. These pins must be powered on with the HVIO_ENABLE signal.

Power Sequencing

The state of the local power supplies is provided on J1 (G30) via the HVIO_ENABLE signal. Until this signal is asserted, the local FPGA power supplies should not be assumed to be on and stable. This signal should be used to sequence or enable any user IO to the module.

Software and FPGA Development Support

Users of the MitySOM-A5E are encouraged to develop applications using the GCC based MitySOM-A5E software development kit (SDK) provided by Critical Link LLC. The SDK is an expansion of the Altera platform support package for the Agilex 5E and includes an implementation of a Yocto Project-compatible board support package providing a Linux root filesystem/distribution and compatible gcc compiler tool-chain with debugger.

FPGA developers should use the Altera Quartus Prime Pro Edition Design Software when working with the MitySOM-A5E.

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Absolute Maximum Ratings

If Military/Aerospace specified cards are required, please contact Critical Link at info@criticallink.com for availability and specifications.

Table 3 Absolute Maximum Ratings

Maximum Supply Voltage (VCC_IN)	13.2 V
Storage Temperature Range	-55ºC to 150ºC

Operating Conditions

The following are the minimum temperature ratings for the components that are installed on a MitySOM-A5E. For specifications not contained in this table please contact Critical Link at info@criticallink.com.

Table 4 Module Component Temperature Ratings

Temperature Range	Component Ratings*
Commercial (-RC)	0ºC to 70ºC
Industrial (-RI)	-40ºC to 85ºC

**** Please see the Thermal Management section below for ambient/operating temperature recommendations.***

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Thermal Management

The MitySOM-A5E module requires careful consideration of thermal management. Depending on load, different thermal management will be required for operation at room temperatures and above. The primary thermal concern is with the Agilex 5E SoC device. Even when idle, case temperature on this device rises significantly. Additional processing activity will require more power consumption and more heat dissipation.

Thermal management is a system level issue that must be addressed in conjunction with the overall system design. Some systems may have available airflow with limited space for a heat sink; others may have room for a heat sink with or without the possibility for additional airflow. As a result, the approach taken for thermal management is a design consideration that must be addressed by the overall system designers when integrating the MitySOM-A5E.

Every end product is different and it is advisable to perform thorough testing to ensure that the product will meet desired performance and longevity specifications. Customers should use Altera's Early Power Estimator (EPE) for the Agilex 5E. This utility will assist in estimating the potential power usage of the processor for a given application. To achieve reliable operation at the maximum specified operating temperatures it has been determined that some form of thermal management (e.g., forced air, heat sink, etc.) will be required.

Critical Link has designed the SOM to work with the MAXIGRIP FANSINK 32.5 × 32.5 × 9.5 mm (MPN: ATS-61325D-C1-R0). A 2-pin connector (MPN: 0532610271, Designator J3) is provided on the SOM to supply 12 V power to an optional fan that can be mounted to the fansink. This reference solution has been included to help simplify the thermal management design process for customers by providing a known, compatible cooling option. However, every end product and deployment environment is different, and system designers are strongly encouraged to evaluate their own thermal requirements and determine whether this solution—or an alternative—is most appropriate to ensure reliable performance and product longevity.

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Connector Interfaces

The next sections outline the connector pin interfaces. The pin interfaces are grouped into the signal classes defined in the table below.

Table 5 Connector Interface Signal Class Groups

Class	Applicable IO Standard	Description
POWER/PWR	N/A	These are module power input pins and corresponding return pins.
POWER OUT	N/A	These are module power output pins.
XCVR_TX	High Speed Differential I/O	These pins are directly connected to the Gigabit Transceiver Transmit lanes of the Agilex 5.
XCVR_RX	High Speed Differential I/O	These pins are directly connected to the Gigabit Transceiver Receive lanes of the Agilex 5.
XCVR_REFCLK	High Speed Differential I/O	These pins are directly connected to the Gigabit Transceiver Reference input clocks.
HSIO	GPIO, PHYLITE, LVDS SERDES, MIPI	These pins are directly connected to FPGA HSIO pins. The Bank voltage is 1.1 V for Bank 3A pins. The Bank 3A pins are on the same bank as the on-board HPS LPDDR4. For Bank 2A and 2B, the bank voltage must be configured using the VCCIO_2A and VCCIO_2B input pins on J2 and must be in the range of 1.1V to 1.3V based on user IO requirements.
HVIO	1.8V CMOS, 2.5V CMOS, 3.3V CMOS	These pins provide single-ended IO buffers that support 1.8V, 2.5V, or 3.3V CMOS logic according to the power inputs bins associated with their FPGA bank location.
HPS I/O	1.8V CMOS	These pins provide I/O buffer and support to interface with the HPS. These pins may be configured to support interfaces such as JTAG, mass storage flash, etc. The bank voltage for these pins is 1.8V.
SDM I/O	1.8V CMOS	These pins are connected to the Secure Data Manager subsystem may be used as I/O pins, but can also be configured to support internal pull up and pull down resistors, open-drain output, Schmitt Trigger input buffers, and more. See the interface description for details.
MISC	N/A	These are miscellaneous pins, refer to relevant notes for more details.

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Bank IO Availability

The number of accessible I/O banks on the Agilex-5 SOM varies with FPGA density. Table 6 lists the available banks for each device density, providing a reference for planning pin assignments and system integration.

Table 6 I/O Bank Availability

FPGA	HSIO Bank Availability			HVIO Bank Availability		
Density	2A	2B	3A	5[A,B]	6[A,B,C,D]	6[E,F]
656 KLE	Yes	Yes	Yes	Yes	Yes	N/A
523 KLE	Yes	Yes	Yes	Yes	Yes	N/A
434 KLE	Yes	Yes	Yes	Yes	Yes	N/A
282 KLE	Yes	N/A	Yes	Yes	Yes	Yes
138 KLE	Yes	N/A	Yes	Yes	Yes	Yes
85 KLE	Yes	N/A	Yes	Yes	Yes	Yes

Transceiver Bank Availability

The number of accessible transceiver banks on the Agilex-5 Mini SOM varies by FPGA density. Table 7 lists the available transceiver signals on connector J1 and shows how these signals map to the Agilex-5 transceiver banks for each device density. This information provides a reference for planning pin assignments and system integration.

Note that the bank designator changes per density but this does not affect the connection, it is simply a naming convention used by Altera. For more information, please refer to Altera's *"GTS Transceiver PHY User Guide: Agilex 5 FPGAs and SoCs"* and *"Device Migration Guidelines Agilex™ 5 FPGAs and SoCs E-Series"* documents.

Table 7 Transceiver Bank Availability

	J1 Transceiver Signal Groups			J2 Transceiver Signal Groups		
Density	GTSL1A*	GTSL1B*	GTSL1C*	GTSL4A*	GTSL4B*	GTSL4C*
656 KLE	Yes (Bank 1A)	Yes (Bank 1B)	Yes (Bank 1C)	Yes (Bank 4A)	Yes (Bank 4B)	Yes (Bank 4C)
523 KLE	Yes (Bank 1A)	Yes (Bank 1B)	Yes (Bank 1C)	Yes (Bank 4A)	Yes (Bank 4B)	Yes (Bank 4C)
434 KLE	N/A	Yes (Bank 1B)	Yes (Bank 1C)	N/A	Yes (Bank 4B)	Yes (Bank 4C)
282 KLE	N/A	Yes (Bank 1A)	Yes (Bank 1B)	N/A	Yes (Bank 4A)	N/A
138 KLE	N/A	N/A	Yes (Bank 1A)	N/A	N/A	N/A
85 KLE	N/A	N/A	Yes (Bank 1A)	N/A	N/A	N/A

J1 Interface Description

The connector used for J1 is a 400 Pin Samtec SEARAY™ series connector, SEAF-50-05.0-L-08-2-A-K-TR, which mates with Samtec SEAM-50-02.0-L-08-2-A-K-TR , resulting in a board to board stack height of 7 mm. The mating height of the SEAM series carrier card connector, indicated by the 02.0 in the part number, may be taller if desired. Up to 16 mm of stack height may be supported with the associated SEAM

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connector selection. The connector is logically broken up into 8 groups (rows) of 50 pins as documented below.

Table 8 contains a summary of the MitySOM-A5E J1 Interface pin-mapping.

For more information about pin definitions and pin connection guidelines please refer to the Agilex 5 Device Family Pin Connection Guidelines.

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Table 8 MitySOM-A5E J1 Connector Pin-Out

Pin	Class	Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6
A01	POWER	GND								
A02	HSIO	DIFF_IO_3A_T16_N	3A_T	M95	DIFF_IO_3A_T16n	PLL_3A_T_CLKOUT1n				
A03	HSIO	DIFF_IO_3A_T16_P	3A_T	K95	DIFF_IO_3A_T16p	PLL_3A_T_CLKOUT1p	PLL_3A_T_CLKOUT1	PLL_3A_T_FB1		
A04	POWER	GND								
A05	HSIO	DIFF_IO_3A_T14_P	3A_T	K84	DIFF_IO_3A_T14p					
A06	HSIO	DIFF_IO_3A_T14_N	3A_T	M84	DIFF_IO_3A_T14n					
A07	POWER	GND								
A08	HSIO	DIFF_IO_3A_T17_P	3A_T	P95	DIFF_IO_3A_T17p	RZQ_T_3A				
A09	HSIO	DIFF_IO_3A_T17_N	3A_T	T95	DIFF_IO_3A_T17n					
A10	POWER	GND								
A11	HSIO	DIFF_IO_3A_T24_N	3A_T	AG104	DIFF_IO_3A_T24n					
A12	HSIO	DIFF_IO_3A_T24_P	3A_T	AG100	DIFF_IO_3A_T24p					
A13	POWER	GND								
A14	HSIO	DIFF_IO_3A_T22_P	3A_T	AG90	DIFF_IO_3A_T22p					
A15	HSIO	DIFF_IO_3A_T22_N	3A_T	AG93	DIFF_IO_3A_T22n					
A16	POWER	GND								
A17	HSIO	DIFF_IO_3A_T20_P	3A_T	Y98	DIFF_IO_3A_T20p					
A18	HSIO	DIFF_IO_3A_T20_N	3A_T	Y95	DIFF_IO_3A_T20n					
A19	POWER	VCCIO_6C6D								
A20	POWER	VCCIO_6C6D								
A21	HVIO	HVIO_5A_1	5A	CD134	HVIO_5A_1	TXCLK1	Data_Ctrl1			
A22	HVIO	HVIO_5A_3	5A	CG134	HVIO_5A_3	TXCLK3	Data_Ctrl3			
A23	HVIO	HVIO_5A_6	5A	CF132	HVIO_5A_6	PIN_PERST_N_CVP_L1B_0	TXCLK6	Data_Ctrl6		
A24	HVIO	HVIO_5A_5	5A	CH132	HVIO_5A_5	PIN_PERST_N_CVP_L1A_0	TXCLK5	Data_Ctrl5		
A25	HVIO	HVIO_5A_11	5A	CF121	HVIO_5A_11	SOURCE_SYNC_CLK1	TXCLK11	RXCLK3	Data_Ctrl11	
A26	HVIO	HVIO_5A_10	5A	CL125	HVIO_5A_10	PLLREFCLK2	TXCLK10	RXCLK2	Data_Ctrl10	
A27	HVIO	HVIO_5A_12	5A	CF118	HVIO_5A_12	SOURCE_SYNC_CLK2	TXCLK12	RXCLK4	Data_Ctrl12	
A28	HVIO	HVIO_5A_16	5A	BW118	HVIO_5A_16	TXCLK16	Data_Ctrl16			
A29	HVIO	HVIO_5A_2	5A	CD135	HVIO_5A_2	TXCLK2	Data_Ctrl2			
A30	HVIO	HVIO_5A_15	5A	CA118	HVIO_5A_15	TXCLK15	Data_Ctrl15			
A31	POWER	GND								
A32	HPS	I2C1_SDA	HPS	M127	GPIO1_IO12	I2C1_SDA	NAND_ALE	SDMMC_PU_PD_DATA2	EMAC2_TX_CLK	TRACE_D10
A33	HPS	I2C1_SCL	HPS	K127	GPIO1_IO13	I2C1_SCL	NAND_RB_N	SDMMC_PWR_ENA	EMAC2_TX_CTL	TRACE_D9
A34	POWER	GND								
A35	POWER	GND								
A36	XCVR_RX	GTSL1B_RX_CH1_N	1B	BB133	GTSL1B_RX_CH1n					
A37	XCVR_RX	GTSL1B_RX_CH1_P	1B	BB135	GTSL1B_RX_CH1p					
A38	POWER	GND								
A39	POWER	GND								
A40	XCVR_RX	GTSL1B_RX_CH3_N	1B	AV133	GTSL1B_RX_CH3n					
A41	XCVR_RX	GTSL1B_RX_CH3_P	1B	AV135	GTSL1B_RX_CH3p					
A42	POWER	GND								
A43	POWER	GND								
A44	XCVR_RX	GTSL1C_RX_CH1_N	1C	AP133	GTSL1C_RX_CH1n					
A45	XCVR_RX	GTSL1C_RX_CH1_P	1C	AP135	GTSL1C_RX_CH1p					
A46	POWER	GND								
A47	POWER	GND								
A48	XCVR_RX	GTSL1C_RX_CH3_N	1C	AK133	GTSL1C_RX_CH3n					
A49	XCVR_RX	GTSL1C_RX_CH3_P	1C	AK135	GTSL1C_RX_CH3p					
A50	POWER	GND								

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Pin	Class	Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5
B01	POWER OUT	+1.8V							
B02	POWER OUT	+1.8V							
B03	HSIO	DIFF_IO_3A_T13_P	3A_T	T84	DIFF_IO_3A_T13p				
B04	HSIO	DIFF_IO_3A_T13_N	3A_T	P84	DIFF_IO_3A_T13n				
B05	POWER	GND							
B06	HSIO	DIFF_IO_3A_T15_N	3A_T	T87	DIFF_IO_3A_T15n				
B07	HSIO	DIFF_IO_3A_T15_P	3A_T	V87	DIFF_IO_3A_T15p				
B08	POWER	GND							
B09	HSIO	DIFF_IO_3A_T18_P	3A_T	V98	DIFF_IO_3A_T18p	CLK_T_3A_1p			
B10	HSIO	DIFF_IO_3A_T18_N	3A_T	T98	DIFF_IO_3A_T18n	CLK_T_3A_1n			
B11	POWER	GND							
B12	HSIO	DIFF_IO_3A_T23_N	3A_T	AC96	DIFF_IO_3A_T23n				
B13	HSIO	DIFF_IO_3A_T23_P	3A_T	AC100	DIFF_IO_3A_T23p				
B14	POWER	GND							
B15	HSIO	DIFF_IO_3A_T21_P	3A_T	AC90	DIFF_IO_3A_T21p	PLL_3A_T_CLKOUT0p	PLL_3A_T_CLKOUT0	PLL_3A_T_FB0	
B16	HSIO	DIFF_IO_3A_T21_N	3A_T	AC86	DIFF_IO_3A_T21n	PLL_3A_T_CLKOUT0n			
B17	POWER	GND							
B18	HSIO	DIFF_IO_3A_T19_P	3A_T	Y87	DIFF_IO_3A_T19p	CLK_T_3A_0p			
B19	HSIO	DIFF_IO_3A_T19_N	3A_T	Y84	DIFF_IO_3A_T19n	CLK_T_3A_0n			
B20	POWER OUT	+1.1V							
B21	POWER OUT	+1.1V							
B22	HVIO	HVIO_5A_19	5A	CK125	HVIO_5A_19	TXCLK19	Data_Ctrl19		
B23	HVIO	HVIO_5A_20	5A	CK128	HVIO_5A_20	TXCLK20	Data_Ctrl20		
B24	HVIO	HVIO_5A_8	5A	CK134	HVIO_5A_8	TXCLK8	Data_Ctrl8		
B25	HVIO	HVIO_5A_7	5A	CF128	HVIO_5A_7	PIN_PERST_N_CVP_L1C_0	TXCLK7	Data_Ctrl7	
B26	HVIO	HVIO_5A_4	5A	CG135	HVIO_5A_4	TXCLK4	Data_Ctrl4		
B27	HVIO	HVIO_5A_18	5A	CL130	HVIO_5A_18	TXCLK18	Data_Ctrl18		
B28	HVIO	HVIO_5A_17	5A	CL128	HVIO_5A_17	TXCLK17	Data_Ctrl17		
B29	HVIO	HVIO_5A_9	5A	CH128	HVIO_5A_9	PLLREFCLK1	TXCLK9	RXCLK1	Data_Ctrl9
B30	HVIO	HVIO_5A_14	5A	BR118	HVIO_5A_14	TXCLK14	Data_Ctrl14		
B31	HVIO	HVIO_5A_13	5A	BU118	HVIO_5A_13	TXCLK13	Data_Ctrl13		
B32	POWER	GND							
B33	POWER	GND							
B34	XCVR_TX	GTSL1C_TX_CH1_N	1C	AR126	GTSL1C_TX_CH1n				
B35	XCVR_TX	GTSL1C_TX_CH1_P	1C	AR129	GTSL1C_TX_CH1p				
B36	POWER	GND							
B37	POWER	GND							
B38	XCVR_TX	GTSL1C_TX_CH2_N	1C	AN126	GTSL1C_TX_CH2n				
B39	XCVR_TX	GTSL1C_TX_CH2_P	1C	AN129	GTSL1C_TX_CH2p				
B40	POWER	GND							
B41	POWER	GND							
B42	XCVR_TX	GTSL1C_TX_CH3_N	1C	AL126	GTSL1C_TX_CH3n				
B43	XCVR_TX	GTSL1C_TX_CH3_P	1C	AL129	GTSL1C_TX_CH3p				
B44	POWER	GND							
B45	POWER	GND							
B46	XCVR_TX	GTSL1C_RX_CH2_N	1C	AM133	GTSL1C_RX_CH2n				
B47	XCVR_TX	GTSL1C_RX_CH2_P	1C	AM135	GTSL1C_RX_CH2p				
B48	POWER	GND							
B49	POWER	GND							
B50	SDM	INIT_DONE	SDM	CA99	PWRMGT_SCL	PWRMGT_ALERT			

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Pin	Class	Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
C01	POWER	VCC_IN												
C02	POWER	VCC_IN												
C03	POWER	GND												
C04	POWER	GND												
C05	HVIO	HVIO_6A_1	6A	BU28	HVIO_6A_1	SYSPLLREFCLK_R4A_0	TXCLK1	Data_Ctrl1						
C06	HVIO	HVIO_6B_17	6B	CK2	HVIO_6B_17	TXCLK17	Data_Ctrl17							
C07	HVIO	HVIO_6B_14	6B	BM19	HVIO_6B_14	TXCLK14	Data_Ctrl14							
C08	HVIO	HVIO_6B_9	6B	BF29	HVIO_6B_9	PLLREFCLK1	TXCLK9	RXCLK1	Data_Ctrl9					
C09	HVIO	HVIO_6B_10	6B	BF25	HVIO_6B_10	PLLREFCLK2	TXCLK10	RXCLK2	Data_Ctrl10					
C10	HVIO	HVIO_6B_3	6B	BE43	HVIO_6B_3	TXCLK3	Data_Ctrl3							
C11	HVIO	HVIO_6A_10	6A	BP22	HVIO_6A_10	PLLREFCLK2	TXCLK10	RXCLK2	Data_Ctrl10					
C12	HVIO	HVIO_6A_12	6A	BR22	HVIO_6A_12	SOURCE_SYNC_CLK2	TXCLK12	RXCLK4	Data_Ctrl12					
C13	HVIO	HVIO_6B_1	6B	BF21	HVIO_6B_1	TXCLK1	Data_Ctrl1							
C14	HVIO	HVIO_6A_9	6A	BK31	HVIO_6A_9	PLLREFCLK1	TXCLK9	RXCLK1	Data_Ctrl9					
C15	POWER	GND												
C16	POWER	GND												
C17	POWER	GND												
C18	HVIO	HVIO_5B_19	5B	BH118	HVIO_5B_19	SYSPLLREFCLK_L1C_0	TXCLK19	Data_Ctrl19						
C19	HVIO	HVIO_5B_20	5B	BF120	HVIO_5B_20	TXCLK20	Data_Ctrl20							
C20	HVIO	HVIO_5B_18	5B	BK112	HVIO_5B_18	TXCLK18	Data_Ctrl18							
C21	HVIO	HVIO_5B_16	5B	BP112	HVIO_5B_16	TXCLK16	Data_Ctrl16							
C22	HVIO	HVIO_5B_17	5B	BM112	HVIO_5B_17	TXCLK17	Data_Ctrl17							
C23	HVIO	HVIO_5B_8	5B	BR109	HVIO_5B_8	TXCLK8	Data_Ctrl8							
C24	HVIO	HVIO_5B_9	5B	BE107	HVIO_5B_9	PLLREFCLK1	TXCLK9	RXCLK1	Data_Ctrl9					
C25	HVIO	HVIO_5B_14	5B	BK118	HVIO_5B_14	TXCLK14	Data_Ctrl14							
C26	HVIO	HVIO_5B_13	5B	BR112	HVIO_5B_13	TXCLK13	Data_Ctrl13							
C27	HVIO	HVIO_5B_15	5B	BM118	HVIO_5B_15	TXCLK15	Data_Ctrl15							
C28	POWER	GND												
C29	SDM	HPS_COLD_nRESET	SDM	CH109	AVSTx8_DATA7									
C30	SDM	SDM_IO13	SDM	BW102	AVSTx8_DATA5									
C31	SDM	SDM_IO8	SDM	CC102	AVSTx8_READY	AS_nCSO3								
C32	HPS	GPIO0_IO5	HPS	AL120	GPIO0_IO5	SPIM0_MOSI	UART1_RTS_N	I2C0_SCL	NAND_ADQ2	SDMMC_DATA2	USB0_NXT	EMAC2_PPSTRIG2	TRACE_D5	
C33	HPS	GPIO0_IO15	HPS	AD135	GPIO0_IO15	NAND_DQS	SDMMC_DATA_STROBE	USB1_DATA0	EMAC0_RX_CTL	TRACE_D7				
C34	POWER	GND												
C35	POWER	GND												
C36	HPS	GPIO0_IO11	HPS	T132	GPIO0_IO11	SPIM1_SS0_N	SPIS1_MISO	MDIO0_MDC	I2C_EMAC0_SCL	NAND_ADQ7	SDMMC_DATA7	USB0_DATA7	I3C0_SCL	TRACE_D11
C37	HPS	GPIO0_IO1	HPS	U135	GPIO0_IO1	SPIM1_SS1_N	SPIS0_MOSI	UART0_RTS_N	NAND_ADQ1	SDMMC_DATA1	USB0_STP	EMAC0_PPSTRIG0	TRACE_D9	
C38	POWER	GND												
C39	POWER	GND												
C40	HPS	GPIO1_IO17	HPS	Y127	GPIO1_IO17	SPIM0_SS1_N	UART1_RTS_N	NAND_ADQ9	I3C0_SCL	EMAC2_TXD1	TRACE_D5			
C41	HPS	GPIO1_IO21	HPS	Y124	GPIO1_IO21	SPIM0_MOSI	SPIS1_MOSI	I2C_EMAC2_SCL	NAND_ADQ13	EMAC2_TXD3	TRACE_D1			
C42	POWER	GND												
C43	POWER	GND												
C44	XCVR_REFCLK	REFCLK_GTSL1B_RX_N	1B	AY115	REFCLK_GTSL1B_RX_N									
C45	XCVR_REFCLK	REFCLK_GTSL1B_RX_P	1B	AY120	REFCLK_GTSL1B_RX_P									
C46	POWER	GND												
C47	POWER	GND												
C48	XCVR_REFCLK	REFCLK_GTSL1C_CH1_P	1C	AP120	REFCLK_GTSL1C_CH1p									
C49	XCVR_REFCLK	REFCLK_GTSL1C_CH1_N	1C	AP115	REFCLK_GTSL1C_CH1n									
C50	POWER	GND												

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Pin	Class	Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
D01	PWR	VCC_IN												
D02	PWR	VCC_IN												
D03	PWR	GND												
D04	PWR	GND												
D05	HVIO	HVIO_6B_18	6B	CJ2	HVIO_6B_18	TXCLK18	Data_Ctrl18							
D06	HVIO	HVIO_6B_19	6B	CK4	HVIO_6B_19	TXCLK19	Data_Ctrl19							
D07	HVIO	HVIO_6B_15	6B	BU19	HVIO_6B_15	TXCLK15	Data_Ctrl15							
D08	HVIO	HVIO_6B_20	6B	CH4	HVIO_6B_20	TXCLK20	Data_Ctrl20							
D09	HVIO	HVIO_6B_7	6B	BF32	HVIO_6B_7	PIN_PERST_N_R4C_1	TXCLK7	Data_Ctrl7						
D10	HVIO	HVIO_6A_3	6A	BR28	HVIO_6A_3	SYSPLLREFCLK_R4B_0	TXCLK3	Data_Ctrl3						
D11	HVIO	HVIO_6B_4	6B	BF40	HVIO_6B_4	TXCLK4	Data_Ctrl4							
D12	HVIO	HVIO_6A_11	6A	BK28	HVIO_6A_11	SOURCE_SYNC_CLK1	TXCLK11	RXCLK3	Data_Ctrl11					
D13	HVIO	HVIO_6A_14	6A	BU22	HVIO_6A_14	TXCLK14	Data_Ctrl14							
D14	HVIO	HVIO_6A_2	6A	BP31	HVIO_6A_2	SYSPLLREFCLK_R4A_1	TXCLK2	Data_Ctrl2						
D15	PWR	VCCIO_6A6B												
D16	PWR	VCCIO_6A6B												
D17	PWR	GND												
D18	HVIO	HVIO_5B_3	5B	BE115	HVIO_5B_3	SYSPLLREFCLK_L1B_0	TXCLK3	Data_Ctrl3						
D19	HVIO	HVIO_5B_4	5B	BF115	HVIO_5B_4	SYSPLLREFCLK_L1B_1	TXCLK4	Data_Ctrl4						
D20	HVIO	HVIO_5B_1	5B	BF111	HVIO_5B_1	SYSPLLREFCLK_L1A_0	TXCLK1	Data_Ctrl1						
D21	HVIO	HVIO_5B_7	5B	BF104	HVIO_5B_7	PIN_PERST_N_CVP_L1C_1	TXCLK7	Data_Ctrl7						
D22	HVIO	HVIO_5B_2	5B	BH109	HVIO_5B_2	SYSPLLREFCLK_L1A_1	TXCLK2	Data_Ctrl2						
D23	HVIO	HVIO_5B_5	5B	BF107	HVIO_5B_5	PIN_PERST_N_CVP_L1A_1	TXCLK5	Data_Ctrl5						
D24	HVIO	HVIO_5B_6	5B	BU109	HVIO_5B_6	PIN_PERST_N_CVP_L1B_1	TXCLK6	Data_Ctrl6						
D25	HVIO	HVIO_5B_11	5B	BE111	HVIO_5B_11	SOURCE_SYNC_CLK1	TXCLK11	RXCLK3	Data_Ctrl11					
D26	HVIO	HVIO_5B_10	5B	BK109	HVIO_5B_10	PLLREFCLK2	TXCLK10	RXCLK2	Data_Ctrl10					
D27	HVIO	HVIO_5B_12	5B	BM109	HVIO_5B_12	SOURCE_SYNC_CLK2	TXCLK12	RXCLK4	Data_Ctrl12					
D28	PWR	GND												
D29	PWR	GND												
D30	GPIO	GPIO0_IO3	HPS	AK115	GPIO0_IO3	SPIS0_MISO	UART0_RX	I2C1_SCL	NAND_RE_N	USB0_DATA0	EMAC1_PPSTRIG1	TRACE_D7		
D31	GPIO	GPIO0_IO19	HPS	AG129	GPIO0_IO19	SPIM1_SS1_N	I3C0_SCL	NAND_ADQ11	USB1_DATA3	EMAC0_RXD1	TRACE_CLK			
D32	GPIO	GPIO0_IO17	HPS	AD134	GPIO0_IO17	I3C1_SCL	NAND_ADQ9	USB1_NXT	EMAC0_TXD1	TRACE_D5				
D33	GPIO	GPIO0_IO7	HPS	AG115	GPIO0_IO7	SPIM0_SS0_N	MDIO2_MDC	UART1_RX	I2C_EMAC2_SCL	NAND_CLE	SDMMC_CMD	USB0_DATA3	TRACE_D15	
D34	GPIO	GPIO0_IO9	HPS	AK120	GPIO0_IO9	SPIM1_MOSI	SPIS1_MOSI	MDIO1_MDC	I2C_EMAC1_SCL	NAND_ADQ5	SDMMC_DATA5	USB0_DATA5	I3C1_SCL	TRACE_D13
D35	GPIO	GPIO0_IO6	HPS	R134	GPIO0_IO6	SPIM0_MISO	MDIO2_MDIO	UART1_TX	I2C_EMAC2_SDA	NAND_ADQ3	SDMMC_DATA3	USB0_DATA2	TRACE_D4	
D36	GPIO	GPIO0_IO10	HPS	N134	GPIO0_IO10	SPIM1_MISO	SPIS1_SS0_N	MDIO0_MDIO	I2C_EMAC0_SDA	NAND_ADQ6	SDMMC_DATA6	USB0_DATA6	I3C0_SDA	TRACE_D12
D37	GPIO	GPIO0_IO0	HPS	W135	GPIO0_IO0	SPIM0_SS1_N	SPIS0_CLK	UART0_CTS_N	NAND_ADQ0	SDMMC_DATA0	USB0_CLK	EMAC0_PPS0	TRACE_D10	
D38	GPIO	GPIO0_IO16	HPS	M132	GPIO0_IO16	I3C1_SDA	NAND_ADQ8	USB1_DATA1	EMAC0_TXD0	TRACE_D6				
D39	GPIO	GPIO1_IO7	HPS	AB132	GPIO1_IO7	SPIS1_MISO	UART1_RX	I2C1_SCL	NAND_CLE	SDMMC_CMD	I3C0_SCL	EMAC1_RXD1	TRACE_D15	
D40	PWR	GND												
D41	GPIO	GPIO1_IO19	HPS	AB124	GPIO1_IO19	SPIM0_SS0_N	MDIO1_MDC	I2C_EMAC1_SCL	NAND_ADQ11	EMAC2_RXD1	TRACE_CLK			
D42	GPIO	GPIO1_IO10	HPS	T124	GPIO1_IO10	JTAG_TDO	SPIS0_SS0_N	MDIO0_MDIO	I2C_EMAC0_SDA	NAND_ADQ6	SDMMC_DATA6	EMAC1_RXD2	TRACE_D12	
D43	GPIO	GPIO1_IO0	HPS	E135	GPIO1_IO0	SPIM1_CLK	UART0_CTS_N	EMAC0_PPS0	NAND_ADQ0	SDMMC_DATA0	EMAC1_TX_CLK	TRACE_D10		
D44	GPIO	GPIO1_IO8	HPS	T127	GPIO1_IO8	JTAG_TCK	SPIS0_CLK	MDIO2_MDIO	I2C_EMAC2_SDA	NAND_ADQ4	SDMMC_DATA4	EMAC1_TXD2	TRACE_D14	
D45	GPIO	GPIO1_IO11	HPS	P124	GPIO1_IO11	JTAG_TDI	SPIS0_MISO	MDIO0_MDC	I2C_EMAC0_SCL	NAND_ADQ7	SDMMC_DATA7	EMAC1_RXD3	TRACE_D11	
D46	GPIO	GPIO1_IO16	HPS	K124	GPIO1_IO16	UART1_CTS_N	NAND_ADQ8	I3C0_SDA	EMAC2_TXD0	TRACE_D6				
D47	GPIO	GPIO1_IO23	HPS	D124	GPIO1_IO23	SPIM0_SS0_N	SPIS1_MISO	MDIO0_MDC	I2C_EMAC0_SCL	NAND_ADQ15	EMAC2_RXD3	TRACE_D3		
D48	GPIO	GPIO1_IO14	HPS	M124	GPIO1_IO14	UART1_TX	NAND_CE_N	I3C1_SDA	EMAC2_RX_CLK	TRACE_D8				
D49	PWR	GND												
D50	MISC	HPS_CLKIN												

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Pin	Class	Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
E01	POWER	VCC_IN												
E02	POWER	VCC_IN												
E03	POWER	GND												
E04	HVIO	HVIO_6B_16	6B	BR19	HVIO_6B_16	TXCLK16	Data_Ctrl16							
E05	HVIO	HVIO_6B_12	6B	BH19	HVIO_6B_12	SOURCE_SYNC_CLK2	TXCLK12	RXCLK4	Data_Ctrl12					
E06	POWER	GND												
E07	POWER	GND												
E08	HVIO	HVIO_6B_13	6B	BK22	HVIO_6B_13	TXCLK13	Data_Ctrl13							
E09	HVIO	HVIO_6B_11	6B	BF16	HVIO_6B_11	SOURCE_SYNC_CLK1	TXCLK11	RXCLK3	Data_Ctrl11					
E10	POWER	GND												
E11	POWER	GND												
E12	HVIO	HVIO_6B_8	6B	BF36	HVIO_6B_8	TXCLK8	Data_Ctrl8							
E13	HVIO	HVIO_6B_5	6B	BE29	HVIO_6B_5	PIN_PERST_N_R4A1	TXCLK5	Data_Ctrl5						
E14	HVIO	HVIO_6A_5	6A	BU31	HVIO_6A_5	PIN_PERST_N_R4A0	TXCLK5	Data_Ctrl5						
E15	HVIO	HVIO_6A_8	6A	BM31	HVIO_6A_8	TXCLK8	Data_Ctrl8							
E16	HVIO	HVIO_6A_18	6A	CF12	HVIO_6A_18	TXCLK18	Data_Ctrl18							
E17	HVIO	HVIO_6A_7	6A	BW28	HVIO_6A_7	PIN_PERST_N_R4C_0	TXCLK7	Data_Ctrl7						
E18	HVIO	HVIO_6A_17	6A	BM22	HVIO_6A_17	TXCLK17	Data_Ctrl17							
E19	HVIO	HVIO_6A_16	6A	BH28	HVIO_6A_16	TXCLK16	Data_Ctrl16							
E20	HVIO	HVIO_6A_19	6A	BK19	HVIO_6A_19	SYSPLLREFCLK_R4C_0	TXCLK19	Data_Ctrl19						
E21	POWER	GND												
E22	HVIO	HVIO_6C_13	6C	C2	HVIO_6C_13	TXCLK13	Data_Ctrl13							
E23	HVIO	HVIO_6C_18	6C	J2	HVIO_6C_18	TXCLK18	Data_Ctrl18							
E24	HVIO	HVIO_6C_10	6C	K8	HVIO_6C_10	PLLREFCLK2	TXCLK10	RXCLK2	Data_Ctrl10					
E25	HVIO	HVIO_6C_14	6C	D4	HVIO_6C_14	TXCLK14	Data_Ctrl14							
E26	HVIO	HVIO_6C_20	6C	G1	HVIO_6C_20	TXCLK20	Data_Ctrl20							
E27	HVIO	HVIO_6C_6	6C	D15	HVIO_6C_6	TXCLK6	Data_Ctrl6							
E28	HVIO	HVIO_6C_9	6C	D8	HVIO_6C_9	PLLREFCLK1	TXCLK9	RXCLK1	Data_Ctrl9					
E29	HVIO	HVIO_6C_7	6C	F18	HVIO_6C_7	TXCLK7	Data_Ctrl7							
E30	HVIO	HVIO_6C_3	6C	H27	HVIO_6C_3	TXCLK3	Data_Ctrl3							
E31	HVIO	HVIO_6C_5	6C	H18	HVIO_6C_5	TXCLK5	Data_Ctrl5							
E32	POWER	GND												
E33	HPS	GPIO0_IO18	HPS	K132	GPIO0_IO18	I3C0_SDA	NAND_ADQ10	USB1_DATA2	EMAC0_RXD0	TRACE_D4				
E34	HPS	GPIO0_IO12	HPS	P132	GPIO0_IO12	NAND_ALE	SDMMC_PU_PD_DATA2	USB1_CLK	EMAC0_TX_CLK	TRACE_D10				
E35	HPS	GPIO0_IO4	HPS	U134	GPIO0_IO4	SPIM0_CLK	UART1_CTS_N	I2C0_SDA	NAND_WP_N	SDMMC_WRITE_PROTECT	USB0_DATA1	EMAC2_PPS2	TRACE_D6	
E36	HPS	GPIO0_IO2	HPS	W134	GPIO0_IO2	SPIS0_SS0_N	UART0_TX	I2C1_SDA	NAND_WE_N	SDMMC_CLK	USB0_DIR	EMAC1_PPS1	TRACE_D8	
E37	HPS	GPIO0_IO13	HPS	L135	GPIO0_IO13	NAND_RB_N	SDMMC_PWR_ENA	USB1_STP	EMAC0_TX_CTL	TRACE_D9				
E38	HPS	GPIO0_IO20	HPS	J134	GPIO0_IO20	SPIM1_CLK	SPIS0_CLK	UART0_CTS_N	I2C1_SDA	NAND_ADQ12	USB1_DATA4	EMAC0_TXD2	TRACE_D0	
E39	HPS	GPIO0_IO23	HPS	G135	GPIO0_IO23	SPIM1_SS0_N	SPIS0_MISO	UART0_RX	I2C0_SCL	NAND_ADQ15	USB1_DATA7	EMAC0_RXD3	TRACE_D3	
E40	HPS	GPIO1_IO15	HPS	AB127	GPIO1_IO15	UART1_RX	NAND_DQS	SDMMC_DATA_STROBE	I3C1_SCL	EMAC2_RX_CTL	TRACE_D7			
E41	HPS	GPIO1_IO5	HPS	AA135	GPIO1_IO5	SPIS1_MOSI	UART1_RTS_N	EMAC2_PPSTRIG2	NAND_ADQ2	SDMMC_DATA2	I3C1_SCL	EMAC1_TXD1	TRACE_D5	
E42	HPS	GPIO1_IO6	HPS	V127	GPIO1_IO6	SPIS1_SS0_N	UART1_TX	I2C1_SDA	NAND_ADQ3	SDMMC_DATA3	I3C0_SDA	EMAC1_RXD0	TRACE_D4	
E43	POWER	GND												
E44	HPS	GPIO1_IO1	HPS	F132	GPIO1_IO1	SPIM1_MOSI	UART0_RTS_N	EMAC0_PPSTRIG0	NAND_ADQ1	SDMMC_DATA1	EMAC1_TX_CTL	TRACE_D9		
E45	HPS	GPIO1_IO20	HPS	F127	GPIO1_IO20	SPIM0_CLK	SPIS1_CLK	I2C_EMAC2_SDA	NAND_ADQ12	EMAC2_TXD2	TRACE_D0			
E46	HPS	GPIO1_IO4	HPS	B134	GPIO1_IO4	SPIM1_SS1_N	SPIS1_CLK	UART1_CTS_N	EMAC2_PPS2	NAND_WP_N	SDMMC_WRITE_PROTECT	I3C1_SDA	EMAC1_TXD0	TRACE_D6
E47	HPS	GPIO1_IO2	HPS	D132	GPIO1_IO2	SPIM1_MISO	UART0_TX	I2C0_SDA	NAND_WE_N	SDMMC_CLK	EMAC1_RX_CLK	TRACE_D8		
E48	HPS	GPIO1_IO18	HPS	H127	GPIO1_IO18	SPIM0_MISO	MDIO1_MDIO	I2C_EMAC1_SDA	NAND_ADQ10	EMAC2_RXD0	TRACE_D4			
E49	HPS	GPIO1_IO22	HPS	F124	GPIO1_IO22	SPIM0_MISO	SPIS1_SS0_N	MDIO0_MDIO	I2C_EMAC0_SDA	NAND_ADQ14	EMAC2_RXD2	TRACE_D2		
E50	POWER	GND												

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Pin	Class	Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
F01	POWER	VCC_IN												
F02	POWER	VCC_IN												
F03	POWER	GND												
F04	POWER	GND												
F05	POWER	GND												
F06	XCVR_RX	GTSL1A_RX_CH2_P	1A	BJ135	GTSL1A_RX_CH2p									
F07	XCVR_RX	GTSL1A_RX_CH2_N	1A	BJ133	GTSL1A_RX_CH2n									
F08	POWER	GND												
F09	POWER	GND												
F10	XCVR_RX	GTSL1A_RX_CH0_P	1A	BV135	GTSL1A_RX_CH0p									
F11	XCVR_RX	GTSL1A_RX_CH0_N	1A	BV133	GTSL1A_RX_CH0n									
F12	POWER	GND												
F13	HVIO	HVIO_6B_6	6B	BE25	HVIO_6B_6	PIN_PERST_N_R4B_1	TXCLK6	Data_Ctrl6						
F14	HVIO	HVIO_6B_2	6B	BE21	HVIO_6B_2	TXCLK2	Data_Ctrl2							
F15	HVIO	HVIO_6A_15	6A	BW19	HVIO_6A_15	TXCLK15	Data_Ctrl15							
F16	HVIO	HVIO_6A_4	6A	BR31	HVIO_6A_4	SYSPLLREFCLK_R4B_1	TXCLK4	Data_Ctrl4						
F17	HVIO	HVIO_6A_13	6A	CH12	HVIO_6A_13	TXCLK13	Data_Ctrl13							
F18	HVIO	HVIO_6A_6	6A	BM28	HVIO_6A_6	PIN_PERST_N_R4B_0	TXCLK6	Data_Ctrl6						
F19	HVIO	HVIO_6A_20	6A	CF9	HVIO_6A_20	TXCLK20	Data_Ctrl20							
F20	POWER	GND												
F21	HVIO	HVIO_6C_16	6C	K4	HVIO_6C_16	TXCLK16	Data_Ctrl16							
F22	HVIO	HVIO_6C_17	6C	G2	HVIO_6C_17	TXCLK17	Data_Ctrl17							
F23	HVIO	HVIO_6C_19	6C	J1	HVIO_6C_19	TXCLK19	Data_Ctrl19							
F24	HVIO	HVIO_6C_12	6C	H8	HVIO_6C_12	SOURCE_SYNC_CLK2	TXCLK12	RXCLK4	Data_Ctrl12					
F25	HVIO	HVIO_6C_15	6C	F4	HVIO_6C_15	TXCLK15	Data_Ctrl15							
F26	HVIO	HVIO_6C_8	6C	F15	HVIO_6C_8	TXCLK8	Data_Ctrl8							
F27	HVIO	HVIO_6C_11	6C	F8	HVIO_6C_11	SOURCE_SYNC_CLK1	TXCLK11	RXCLK3	Data_Ctrl11					
F28	HVIO	HVIO_6C_2	6C	F24	HVIO_6C_2	TXCLK2	Data_Ctrl2							
F29	HVIO	HVIO_6C_4	6C	D24	HVIO_6C_4	TXCLK4	Data_Ctrl4							
F30	HVIO	HVIO_6C_1	6C	F27	HVIO_6C_1	TXCLK1	Data_Ctrl1							
F31	POWER	GND												
F32	HPS	GPIO0_IO21	HPS	AG120	GPIO0_IO21	SPIM1_MOSI	SPIS0_MOSI	UART0_RTS_N	I2C1_SCL	NAND_ADQ13	USB1_DATA5	EMAC0_TXD3	TRACE_D1	
F33	HPS	GPIO0_IO22	HPS	G134	GPIO0_IO22	SPIM1_MISO	SPIS0_SS0_N	UART0_TX	I2C0_SDA	NAND_ADQ14	USB1_DATA6	EMAC0_RXD2	TRACE_D2	
F34	POWER	GND												
F35	POWER	GND												
F36	HPS	GPIO0_IO8	HPS	N135	GPIO0_IO8	SPIM1_CLK	SPIS1_CLK	MDIO1_MDIO	I2C_EMAC1_SDA	NAND_ADQ4	SDMMC_DATA4	USB0_DATA4	I3C1_SDA	TRACE_D14
F37	HPS	GPIO0_IO14	HPS	J135	GPIO0_IO14	NAND_CE_N	USB1_DIR	EMAC0_RX_CLK	TRACE_D8					
F38	POWER	GND												
F39	POWER	GND												
F40	HPS	GPIO1_IO9	HPS	Y132	GPIO1_IO9	JTAG_TMS	SPIS0_MOSI	MDIO2_MDC	I2C_EMAC2_SCL	NAND_ADQ5	SDMMC_DATA5	EMAC1_TXD3	TRACE_D13	
F41	HPS	GPIO1_IO3	HPS	AG123	GPIO1_IO3	SPIM1_SS0_N	UART0_RX	I2C0_SCL	NAND_RE_N	EMAC1_RX_CTL	TRACE_D7			
F42	POWER	GND												
F43	POWER	GND												
F44	XCVR_REFCLK	REFCLK_GTSL1B_CH1_P	1B	AV120	REFCLK_GTSL1B_CH1p									
F45	XCVR_REFCLK	REFCLK_GTSL1B_CH1_N	1B	AV115	REFCLK_GTSL1B_CH1n									
F46	POWER	GND												
F47	POWER	GND												
F48	XCVR_REFCLK	REFCLK_GTSL1C_RX_P	1C	AT120	REFCLK_GTSL1C_RX_P									
F49	XCVR_REFCLK	REFCLK_GTSL1C_RX_N	1C	AT115	REFCLK_GTSL1C_RX_N									
F50	POWER	GND												

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Pin	Class	Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5
G01	MISC	CORE_EN							
G02	POWER	GND							
G03	POWER	GND							
G04	XCVR_RX	GTSL1A_RX_CH3_P	1A	BF135	GTSL1A_RX_CH3p				
G05	XCVR_RX	GTSL1A_RX_CH3_N	1A	BF133	GTSL1A_RX_CH3n				
G06	POWER	GND							
G07	POWER	GND							
G08	XCVR_RX	GTSL1A_RX_CH1_P	1A	BN135	GTSL1A_RX_CH1p				
G09	XCVR_RX	GTSL1A_RX_CH1_N	1A	BN133	GTSL1A_RX_CH1n				
G10	POWER	GND							
G11	POWER	GND							
G12	XCVR_REFCLK	REFCLK_GTSL1A_CH1_P	1A	BB120	REFCLK_GTSL1A_CH1p				
G13	XCVR_REFCLK	REFCLK_GTSL1A_CH1_N	1A	BB115	REFCLK_GTSL1A_CH1n				
G14	POWER	GND							
G15	POWER	GND							
G16	XCVR_REFCLK	REFCLK_GTSL1A_RX_P	1A	BC111	REFCLK_GTSL1A_RX_P				
G17	XCVR_REFCLK	REFCLK_GTSL1A_RX_N	1A	BC107	REFCLK_GTSL1A_RX_N				
G18	POWER	GND							
G19	POWER	VCC_BAT							
G20	HVIO	HVIO_6D_1	6D	A8	HVIO_6D_1	TXCLK1	Data_Ctrl1		
G21	HVIO	HVIO_6D_3	6D	A11	HVIO_6D_3	TXCLK3	Data_Ctrl3		
G22	HVIO	HVIO_6D_4	6D	B11	HVIO_6D_4	TXCLK4	Data_Ctrl4		
G23	HVIO	HVIO_6D_5	6D	B14	HVIO_6D_5	TXCLK5	Data_Ctrl5		
G24	HVIO	HVIO_6D_7	6D	A20	HVIO_6D_7	TXCLK7	Data_Ctrl7		
G25	HVIO	HVIO_6D_9	6D	A23	HVIO_6D_9	PLLREFCLK1	TXCLK9	RXCLK1	Data_Ctrl9
G26	HVIO	HVIO_6D_11	6D	B23	HVIO_6D_11	SOURCE_SYNC_CLK1	TXCLK11	RXCLK3	Data_Ctrl11
G27	HVIO	HVIO_6D_18	6D	B35	HVIO_6D_18	TXCLK18	Data_Ctrl18		
G28	HVIO	HVIO_6D_17	6D	A39	HVIO_6D_17	TXCLK17	Data_Ctrl17		
G29	HVIO	HVIO_6D_19	6D	D34	HVIO_6D_19	TXCLK19	Data_Ctrl19		
G30	MISC	HVIO_ENABLE							
G31	POWER	VCCIO_5A5B							
G32	POWER	VCCIO_5A5B							
G33	POWER	GND							
G34	XCVR_TX	GTSL1C_TX_CH0_N	1C	AU126	GTSL1C_TX_CH0n				
G35	XCVR_TX	GTSL1C_TX_CH0_P	1C	AU129	GTSL1C_TX_CH0p				
G36	POWER	GND							
G37	POWER	GND							
G38	XCVR_RX	GTSL1B_RX_CH0_N	1B	BD133	GTSL1B_RX_CH0n				
G39	XCVR_RX	GTSL1B_RX_CH0_P	1B	BD135	GTSL1B_RX_CH0p				
G40	POWER	GND							
G41	POWER	GND							
G42	XCVR_RX	GTSL1B_RX_CH2_N	1B	AY133	GTSL1B_RX_CH2n				
G43	XCVR_RX	GTSL1B_RX_CH2_P	1B	AY135	GTSL1B_RX_CH2p				
G44	POWER	GND							
G45	POWER	GND							
G46	XCVR_RX	GTSL1C_RX_CH0_N	1C	AT133	GTSL1C_RX_CH0n				
G47	XCVR_RX	GTSL1C_RX_CH0_P	1C	AT135	GTSL1C_RX_CH0p				
G48	POWER	GND							
G49	POWER	GND							
G50	SDM	CONF_DONE	SDM	BP102	PWRMGT_SDA				

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Pin	Class	Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5
H01	POWER	GND							
H02	XCVR_TX	GTSL1A_TX_CH3_P	1A	BG129	GTSL1A_TX_CH3p				
H03	XCVR_TX	GTSL1A_TX_CH3_N	1A	BG126	GTSL1A_TX_CH3n				
H04	POWER	GND							
H05	POWER	GND							
H06	XCVR_TX	GTSL1A_TX_CH2_P	1A	BL129	GTSL1A_TX_CH2p				
H07	XCVR_TX	GTSL1A_TX_CH2_N	1A	BL126	GTSL1A_TX_CH2n				
H08	POWER	GND							
H09	POWER	GND							
H10	XCVR_TX	GTSL1A_TX_CH1_P	1A	BT129	GTSL1A_TX_CH1p				
H11	XCVR_TX	GTSL1A_TX_CH1_N	1A	BT126	GTSL1A_TX_CH1n				
H12	POWER	GND							
H13	POWER	GND							
H14	XCVR_TX	GTSL1A_TX_CH0_P	1A	BY129	GTSL1A_TX_CH0p				
H15	XCVR_TX	GTSL1A_TX_CH0_N	1A	BY126	GTSL1A_TX_CH0n				
H16	POWER	GND							
H17	POWER	GND							
H18	HVIO	HVIO_6D_2	6D	B4	HVIO_6D_2	TXCLK2	Data_Ctrl2		
H19	HVIO	HVIO_6D_6	6D	A14	HVIO_6D_6	TXCLK6	Data_Ctrl6		
H20	HVIO	HVIO_6D_8	6D	A17	HVIO_6D_8	TXCLK8	Data_Ctrl8		
H21	HVIO	HVIO_6D_10	6D	B20	HVIO_6D_10	PLLREFCLK2	TXCLK10	RXCLK2	Data_Ctrl10
H22	HVIO	HVIO_6D_12	6D	B26	HVIO_6D_12	SOURCE_SYNC_CLK2	TXCLK12	RXCLK4	Data_Ctrl12
H23	HVIO	HVIO_6D_13	6D	B30	HVIO_6D_13	TXCLK13	Data_Ctrl13		
H24	HVIO	HVIO_6D_16	6D	A33	HVIO_6D_16	TXCLK16	Data_Ctrl16		
H25	HVIO	HVIO_6D_14	6D	A30	HVIO_6D_14	TXCLK14	Data_Ctrl14		
H26	HVIO	HVIO_6D_15	6D	A35	HVIO_6D_15	TXCLK15	Data_Ctrl15		
H27	HVIO	HVIO_6D_20	6D	B39	HVIO_6D_20	TXCLK20	Data_Ctrl20		
H28	POWER	GND							
H29	SDM	TCK	SDM	CA109	TCK				
H30	SDM	TDO	SDM	BW109	TDO				
H31	SDM	TMS	SDM	CA112	TMS				
H32	SDM	TDI	SDM	BW112	TDI				
H33	SDM	nSTATUS	SDM	BW99	nSTATUS				
H34	SDM	nCONFIG	SDM	BU99	nCONFIG				
H35	POWER	GND							
H36	XCVR_TX	GTSL1B_TX_CH0_N	1B	BE126	GTSL1B_TX_CH0n				
H37	XCVR_TX	GTSL1B_TX_CH0_P	1B	BE129	GTSL1B_TX_CH0p				
H38	POWER	GND							
H39	POWER	GND							
H40	XCVR_TX	GTSL1B_TX_CH1_N	1B	BC126	GTSL1B_TX_CH1n				
H41	XCVR_TX	GTSL1B_TX_CH1_P	1B	BC129	GTSL1B_TX_CH1p				
H42	POWER	GND							
H43	POWER	GND							
H44	XCVR_TX	GTSL1B_TX_CH2_N	1B	BA126	GTSL1B_TX_CH2n				
H45	XCVR_TX	GTSL1B_TX_CH2_P	1B	BA129	GTSL1B_TX_CH2p				
H46	POWER	GND							
H47	POWER	GND							
H48	XCVR_TX	GTSL1B_TX_CH3_N	1B	AW126	GTSL1B_TX_CH3n				
H49	XCVR_TX	GTSL1B_TX_CH3_P	1B	AW129	GTSL1B_TX_CH3p				
H50	POWER	GND							

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J2 Interface Description

The connector used for J2 is the same 400 Pin Samtec SEARAY™ series connector, SEAF-50-05.0-L-08-2-A-K-TR, as used for J1.

Table 9 contains a summary of the MitySOM-A5E J2 Interface pin-mapping.

For more information about pin definitions and pin connection guidelines please refer to the Agilex 5 Device Family Pin Connection Guidelines.

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Table 9 MitySOM-A5E J2 Connector Pin-Out

Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4
A01	POWER	GND						
A02	XCVR_TX	GTSR4A_TX_CH0_P	4A	BY7	GTSR4A_TX_CH0p			
A03	XCVR_TX	GTSR4A_TX_CH0_N	4A	BY10	GTSR4A_TX_CH0n			
A04	POWER	GND						
A05	POWER	GND						
A06	XCVR_TX	GTSR4A_TX_CH1_P	4A	BT7	GTSR4A_TX_CH1p			
A07	XCVR_TX	GTSR4A_TX_CH1_N	4A	BT10	GTSR4A_TX_CH1n			
A08	POWER	GND						
A09	POWER	GND						
A10	XCVR_TX	GTSR4A_TX_CH2_P	4A	BL7	GTSR4A_TX_CH2p			
A11	XCVR_TX	GTSR4A_TX_CH2_N	4A	BL10	GTSR4A_TX_CH2n			
A12	POWER	GND						
A13	POWER	GND						
A14	XCVR_TX	GTSR4A_TX_CH3_P	4A	BG7	GTSR4A_TX_CH3p			
A15	XCVR_TX	GTSR4A_TX_CH3_N	4A	BG10	GTSR4A_TX_CH3n			
A16	POWER	GND						
A17	POWER	GND						
A18	XCVR_REFCLK	REFCLK_GTSR4A_CH1_P	4A	BB16	REFCLK_GTSR4A_CH1p			
A19	XCVR_REFCLK	REFCLK_GTSR4A_CH1_N	4A	BB21	REFCLK_GTSR4A_CH1n			
A20	POWER	GND						
A21	HSIO	DIFF_IO_2A_T2_P	2A_T	CF62	DIFF_IO_2A_T2p			
A22	HSIO	DIFF_IO_2A_T2_N	2A_T	CH62	DIFF_IO_2A_T2n			
A23	HSIO	DIFF_IO_2A_T9_N	2A_T	BR62	DIFF_IO_2A_T9n			
A24	HSIO	DIFF_IO_2A_T9_P	2A_T	BU62	DIFF_IO_2A_T9p			
A25	POWER	GND						
A26	HSIO	DIFF_IO_2A_T17_P	2A_T	BH69	DIFF_IO_2A_T17p	RZQ_T_2A		
A27	HSIO	DIFF_IO_2A_T17_N	2A_T	BH71	DIFF_IO_2A_T17n			
A28	POWER	GND						
A29	HSIO	DIFF_IO_2B_B22_N	2B_B	CL66	DIFF_IO_2B_B22n			
A30	HSIO	DIFF_IO_2B_B22_P	2B_B	CK63	DIFF_IO_2B_B22p			
A31	HSIO	DIFF_IO_2B_B4_P	2B_B	BW49	DIFF_IO_2B_B4p	PLL_2B_B_CLKOUT1p	PLL_2B_B_CLKOUT1	PLL_2B_B_FB1
A32	HSIO	DIFF_IO_2B_B4_N	2B_B	CA49	DIFF_IO_2B_B4n	PLL_2B_B_CLKOUT1n		
A33	HSIO	DIFF_IO_2B_B6_N	2B_B	BU49	DIFF_IO_2B_B6n	CLK_B_2B_1n		
A34	HSIO	DIFF_IO_2B_B6_P	2B_B	BR49	DIFF_IO_2B_B6p	CLK_B_2B_1p		
A35	POWER	GND						
A36	XCVR_TX	GTSR4C_TX_CH0_P	4C	AU7	GTSR4C_TX_CH0p			
A37	XCVR_TX	GTSR4C_TX_CH0_N	4C	AU10	GTSR4C_TX_CH0n			
A38	POWER	GND						
A39	POWER	GND						
A40	XCVR_TX	GTSR4C_TX_CH1_P	4C	AR7	GTSR4C_TX_CH1p			
A41	XCVR_TX	GTSR4C_TX_CH1_N	4C	AR10	GTSR4C_TX_CH1n			
A42	POWER	GND						
A43	POWER	GND						
A44	XCVR_TX	GTSR4C_TX_CH2_P	4C	AN7	GTSR4C_TX_CH2p			
A45	XCVR_TX	GTSR4C_TX_CH2_N	4C	AN10	GTSR4C_TX_CH2n			
A46	POWER	GND						
A47	POWER	GND						
A48	XCVR_TX	GTSR4C_TX_CH3_P	4C	AL7	GTSR4C_TX_CH3p			
A49	XCVR_TX	GTSR4C_TX_CH3_N	4C	AL10	GTSR4C_TX_CH3n			
A50	POWER	GND						

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Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4
B01	POWER	VCCIO_2A						
B02	POWER	VCCIO_2A						
B03	POWER	GND						
B04	XCVR_RX	GTSR4A_RX_CH0_P	4A	CB1	GTSR4A_RX_CH0p			
B05	XCVR_RX	GTSR4A_RX_CH0_N	4A	CB3	GTSR4A_RX_CH0n			
B06	POWER	GND						
B07	POWER	GND						
B08	XCVR_RX	GTSR4A_RX_CH1_P	4A	BV1	GTSR4A_RX_CH1p			
B09	XCVR_RX	GTSR4A_RX_CH1_N	4A	BV3	GTSR4A_RX_CH1n			
B10	POWER	GND						
B11	POWER	GND						
B12	XCVR_RX	GTSR4A_RX_CH2_P	4A	BN1	GTSR4A_RX_CH2p			
B13	XCVR_RX	GTSR4A_RX_CH2_N	4A	BN3	GTSR4A_RX_CH2n			
B14	POWER	GND						
B15	POWER	GND						
B16	XCVR_RX	GTSR4A_RX_CH3_P	4A	BJ1	GTSR4A_RX_CH3p			
B17	XCVR_RX	GTSR4A_RX_CH3_N	4A	BJ3	GTSR4A_RX_CH3n			
B18	POWER	GND						
B19	HSIO	DIFF_IO_2A_T14_N	2A_T	BH59	DIFF_IO_2A_T14n			
B20	HSIO	DIFF_IO_2A_T14_P	2A_T	BH62	DIFF_IO_2A_T14p			
B21	HSIO	DIFF_IO_2A_T15_P	2A_T	BM62	DIFF_IO_2A_T15p			
B22	HSIO	DIFF_IO_2A_T15_N	2A_T	BP62	DIFF_IO_2A_T15n			
B23	POWER	GND						
B24	HSIO	DIFF_IO_2A_T16_P	2A_T	BM69	DIFF_IO_2A_T16p	PLL_2A_T_CLKOUT1p	PLL_2A_T_CLKOUT1	PLL_2A_T_FB1
B25	HSIO	DIFF_IO_2A_T16_N	2A_T	BK69	DIFF_IO_2A_T16n	PLL_2A_T_CLKOUT1n		
B26	POWER	GND						
B27	HSIO	DIFF_IO_2A_T21_N	2A_T	BF83	DIFF_IO_2A_T21n	PLL_2A_T_CLKOUT0n		
B28	HSIO	DIFF_IO_2A_T21_P	2A_T	BE83	DIFF_IO_2A_T21p	PLL_2A_T_CLKOUT0p	PLL_2A_T_CLKOUT0	PLL_2A_T_FB0
B29	POWER	GND						
B30	HSIO	DIFF_IO_2B_B5_P	2B_B	BR52	DIFF_IO_2B_B5p	RZQ_B_2B		
B31	HSIO	DIFF_IO_2B_B5_N	2B_B	BU52	DIFF_IO_2B_B5n			
B32	POWER	GND						
B33	POWER	GND						
B34	XCVR_RX	GTSR4C_RX_CH0_P	4C	AV1	GTSR4C_RX_CH0p			
B35	XCVR_RX	GTSR4C_RX_CH0_N	4C	AV3	GTSR4C_RX_CH0n			
B36	POWER	GND						
B37	POWER	GND						
B38	XCVR_RX	GTSR4C_RX_CH1_P	4C	AT1	GTSR4C_RX_CH1p			
B39	XCVR_RX	GTSR4C_RX_CH1_N	4C	AT3	GTSR4C_RX_CH1n			
B40	POWER	GND						
B41	POWER	GND						
B42	XCVR_RX	GTSR4C_RX_CH2_P	4C	AP1	GTSR4C_RX_CH2p			
B43	XCVR_RX	GTSR4C_RX_CH2_N	4C	AP3	GTSR4C_RX_CH2n			
B44	POWER	GND						
B45	POWER	GND						
B46	XCVR_RX	GTSR4C_RX_CH3_P	4C	AM1	GTSR4C_RX_CH3p			
B47	XCVR_RX	GTSR4C_RX_CH3_N	4C	AM3	GTSR4C_RX_CH3n			
B48	POWER	GND						
B49	POWER	GND						
B50	POWER	GND						

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Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1
C01	POWER	GND			
C02	XCVR_REFCLK	REFCLK_GTSR4A_RX_P	4A	BC29	REFCLK_GTSR4A_RX_P
C03	XCVR_REFCLK	REFCLK_GTSR4A_RX_N	4A	BC25	REFCLK_GTSR4A_RX_N
C04	POWER	GND			
C05	POWER	GND			
C06	HSIO	DIFF_IO_2A_B12_N	2A_B	BU89	DIFF_IO_2A_B12n
C07	HSIO	DIFF_IO_2A_B12_P	2A_B	BR89	DIFF_IO_2A_B12p
C08	POWER	GND			
C09	HSIO	DIFF_IO_2A_B10_N	2A_B	CA89	DIFF_IO_2A_B10n
C10	HSIO	DIFF_IO_2A_B10_P	2A_B	BW89	DIFF_IO_2A_B10p
C11	POWER	GND			
C12	HSIO	DIFF_IO_2A_B15_P	2A_B	CF81	DIFF_IO_2A_B15p
C13	HSIO	DIFF_IO_2A_B15_N	2A_B	CH81	DIFF_IO_2A_B15n
C14	POWER	GND			
C15	HSIO	DIFF_IO_2A_T5_N	2A_T	CA71	DIFF_IO_2A_T5n
C16	HSIO	DIFF_IO_2A_T5_P	2A_T	CC71	DIFF_IO_2A_T5p
C17	POWER	GND			
C18	HSIO	DIFF_IO_2A_T10_N	2A_T	CA69	DIFF_IO_2A_T10n
C19	HSIO	DIFF_IO_2A_T10_P	2A_T	BW69	DIFF_IO_2A_T10p
C20	POWER	GND			
C21	HSIO	DIFF_IO_2A_T1_P	2A_T	CF59	DIFF_IO_2A_T1p
C22	HSIO	DIFF_IO_2A_T1_N	2A_T	CH59	DIFF_IO_2A_T1n
C23	POWER	GND			
C24	HSIO	DIFF_IO_2A_T7_N	2A_T	CA59	DIFF_IO_2A_T7n
C25	HSIO	DIFF_IO_2A_T7_P	2A_T	BW59	DIFF_IO_2A_T7p
C26	POWER	GND			
C27	HSIO	DIFF_IO_2B_B24_N	2B_B	CL70	DIFF_IO_2B_B24n
C28	HSIO	DIFF_IO_2B_B24_P	2B_B	CK66	DIFF_IO_2B_B24p
C29	POWER	GND			
C30	HSIO	DIFF_IO_2B_B21_N	2B_B	CL60	DIFF_IO_2B_B21n
C31	HSIO	DIFF_IO_2B_B21_P	2B_B	CL56	DIFF_IO_2B_B21p
C32	POWER	GND			
C33	HSIO	DIFF_IO_2B_B17_P	2B_B	CK48	DIFF_IO_2B_B17p
C34	HSIO	DIFF_IO_2B_B17_N	2B_B	CL45	DIFF_IO_2B_B17n
C35	POWER	GND			
C36	HSIO	DIFF_IO_2B_B16_P	2B_B	CK39	DIFF_IO_2B_B16p
C37	HSIO	DIFF_IO_2B_B16_N	2B_B	CL39	DIFF_IO_2B_B16n
C38	POWER	GND			
C39	HSIO	DIFF_IO_2B_T10_P	2B_T	CK17	DIFF_IO_2B_T10p
C40	HSIO	DIFF_IO_2B_T10_N	2B_T	CL17	DIFF_IO_2B_T10n
C41	HSIO	DIFF_IO_2B_T7_P	2B_T	CK8	DIFF_IO_2B_T7p
C42	HSIO	DIFF_IO_2B_T7_N	2B_T	CL6	DIFF_IO_2B_T7n
C43	POWER	GND			
C44	XCVR_REFCLK	REFCLK_GTSR4C_RX_P	4C	AT16	REFCLK_GTSR4C_RX_P
C45	XCVR_REFCLK	REFCLK_GTSR4C_RX_N	4C	AT21	REFCLK_GTSR4C_RX_N
C46	POWER				
C47	POWER	GND			
C48	XCVR_REFCLK	REFCLK_GTSR4C_CH1_P	4C	AP16	REFCLK_GTSR4C_CH1p
C49	XCVR_REFCLK	REFCLK_GTSR4C_CH1_N	4C	AP21	REFCLK_GTSR4C_CH1n
C50	POWER	GND			

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Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2
D01	POWER	VCCIO_2A				
D02	POWER	VCCIO_2A				
D03	POWER	GND				
D04	HSIO	DIFF_IO_2A_B11_P	2A_B	BR92	DIFF_IO_2A_B11p	
D05	HSIO	DIFF_IO_2A_B11_N	2A_B	BU92	DIFF_IO_2A_B11n	
D06	HSIO	DIFF_IO_2A_B16_N	2A_B	CF89	DIFF_IO_2A_B16n	
D07	HSIO	DIFF_IO_2A_B16_P	2A_B	CH89	DIFF_IO_2A_B16p	
D08	HSIO	DIFF_IO_2A_B3_P	2A_B	BM81	DIFF_IO_2A_B3p	
D09	HSIO	DIFF_IO_2A_B3_N	2A_B	BP81	DIFF_IO_2A_B3n	
D10	POWER	GND				
D11	HSIO	DIFF_IO_2A_B14_P	2A_B	CA81	DIFF_IO_2A_B14p	
D12	HSIO	DIFF_IO_2A_B14_N	2A_B	CC81	DIFF_IO_2A_B14n	
D13	POWER	GND				
D14	HSIO	DIFF_IO_2A_B7_N	2A_B	CA78	DIFF_IO_2A_B7n	CLK_B_2A_0n
D15	HSIO	DIFF_IO_2A_B7_P	2A_B	BW78	DIFF_IO_2A_B7p	CLK_B_2A_0p
D16	POWER	GND				
D17	HSIO	DIFF_IO_2A_T11_P	2A_T	BR71	DIFF_IO_2A_T11p	
D18	HSIO	DIFF_IO_2A_T11_N	2A_T	BU71	DIFF_IO_2A_T11n	
D19	POWER	GND				
D20	HSIO	DIFF_IO_2A_T20_N	2A_T	BE75	DIFF_IO_2A_T20n	
D21	HSIO	DIFF_IO_2A_T20_P	2A_T	BE79	DIFF_IO_2A_T20p	
D22	POWER	GND				
D23	HSIO	DIFF_IO_2A_T19_P	2A_T	BF75	DIFF_IO_2A_T19p	CLK_T_2A_0p
D24	HSIO	DIFF_IO_2A_T19_N	2A_T	BF72	DIFF_IO_2A_T19n	CLK_T_2A_0n
D25	POWER	GND				
D26	HSIO	DIFF_IO_2B_B11_N	2B_B	CA52	DIFF_IO_2B_B11n	
D27	HSIO	DIFF_IO_2B_B11_P	2B_B	CC52	DIFF_IO_2B_B11p	
D28	POWER	GND				
D29	HSIO	DIFF_IO_2B_B8_N	2B_B	CA41	DIFF_IO_2B_B8n	
D30	HSIO	DIFF_IO_2B_B8_P	2B_B	CC41	DIFF_IO_2B_B8p	
D31	POWER	GND				
D32	HSIO	DIFF_IO_2B_B7_N	2B_B	CF38	DIFF_IO_2B_B7n	CLK_B_2B_0n
D33	HSIO	DIFF_IO_2B_B7_P	2B_B	CH38	DIFF_IO_2B_B7p	CLK_B_2B_0p
D34	POWER	GND				
D35	HSIO	DIFF_IO_2B_B1_P	2B_B	CA38	DIFF_IO_2B_B1p	
D36	HSIO	DIFF_IO_2B_B1_N	2B_B	BW38	DIFF_IO_2B_B1n	
D37	POWER	GND				
D38	HSIO	DIFF_IO_2B_T17_P	2B_T	BE64	DIFF_IO_2B_T17p	RZQ_T_2B
D39	HSIO	DIFF_IO_2B_T17_N	2B_T	BF64	DIFF_IO_2B_T17n	
D40	HSIO	DIFF_IO_2B_T15_P	2B_T	BF57	DIFF_IO_2B_T15p	
D41	HSIO	DIFF_IO_2B_T15_N	2B_T	BF53	DIFF_IO_2B_T15n	
D42	HSIO	DIFF_IO_2B_T19_N	2B_T	BM38	DIFF_IO_2B_T19n	CLK_T_2B_0n
D43	HSIO	DIFF_IO_2B_T19_P	2B_T	BK38	DIFF_IO_2B_T19p	CLK_T_2B_0p
D44	HSIO	DIFF_IO_2B_T20_N	2B_T	BH41	DIFF_IO_2B_T20n	
D45	HSIO	DIFF_IO_2B_T20_P	2B_T	BH38	DIFF_IO_2B_T20p	
D46	HSIO	DIFF_IO_2B_T24_N	2B_T	BP52	DIFF_IO_2B_T24n	
D47	HSIO	DIFF_IO_2B_T24_P	2B_T	BM52	DIFF_IO_2B_T24p	
D48	POWER	GND				
D49	POWER	GND				
D50	POWER	GND				

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Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4
E01	POWER	VCCIO_2B						
E02	POWER	VCCIO_2B						
E03	POWER	GND						
E04	HSIO	DIFF_IO_2A_B5_N	2A_B	BH92	DIFF_IO_2A_B5n			
E05	HSIO	DIFF_IO_2A_B5_P	2A_B	BH89	DIFF_IO_2A_B5p	RZQ_B_2A		
E06	POWER	GND						
E07	HSIO	DIFF_IO_2A_B1_P	2A_B	BM78	DIFF_IO_2A_B1p			
E08	HSIO	DIFF_IO_2A_B1_N	2A_B	BK78	DIFF_IO_2A_B1n			
E09	POWER	GND						
E10	HSIO	DIFF_IO_2A_B13_N	2A_B	CF78	DIFF_IO_2A_B13n			
E11	HSIO	DIFF_IO_2A_B13_P	2A_B	CH78	DIFF_IO_2A_B13p			
E12	POWER	GND						
E13	HSIO	DIFF_IO_2A_B8_N	2A_B	BU78	DIFF_IO_2A_B8n			
E14	HSIO	DIFF_IO_2A_B8_P	2A_B	BR78	DIFF_IO_2A_B8p			
E15	POWER	GND						
E16	HSIO	DIFF_IO_2A_T13_N	2A_T	BK59	DIFF_IO_2A_T13n			
E17	HSIO	DIFF_IO_2A_T13_P	2A_T	BM59	DIFF_IO_2A_T13p			
E18	POWER	GND						
E19	HSIO	DIFF_IO_2A_T12_P	2A_T	BR69	DIFF_IO_2A_T12p			
E20	HSIO	DIFF_IO_2A_T12_N	2A_T	BU69	DIFF_IO_2A_T12n			
E21	HSIO	DIFF_IO_2A_T3_P	2A_T	CA62	DIFF_IO_2A_T3p			
E22	HSIO	DIFF_IO_2A_T3_N	2A_T	CC62	DIFF_IO_2A_T3n			
E23	HSIO	DIFF_IO_2A_T23_N	2A_T	BF90	DIFF_IO_2A_T23n			
E24	HSIO	DIFF_IO_2A_T23_P	2A_T	BF93	DIFF_IO_2A_T23p			
E25	HSIO	DIFF_IO_2A_T24_N	2A_T	BE93	DIFF_IO_2A_T24n			
E26	HSIO	DIFF_IO_2A_T24_P	2A_T	BE96	DIFF_IO_2A_T24p			
E27	HSIO	DIFF_IO_2B_B12_P	2B_B	CF52	DIFF_IO_2B_B12p			
E28	HSIO	DIFF_IO_2B_B12_N	2B_B	CH52	DIFF_IO_2B_B12n			
E29	HSIO	DIFF_IO_2B_B10_P	2B_B	CF49	DIFF_IO_2B_B10p			
E30	HSIO	DIFF_IO_2B_B10_N	2B_B	CH49	DIFF_IO_2B_B10n			
E31	POWER	GND						
E32	HSIO	DIFF_IO_2B_B9_N	2B_B	CF41	DIFF_IO_2B_B9n	PLL_2B_B_CLKOUT0n		
E33	HSIO	DIFF_IO_2B_B9_P	2B_B	CH41	DIFF_IO_2B_B9p	PLL_2B_B_CLKOUT0p	PLL_2B_B_CLKOUT0	PLL_2B_B_FB0
E34	HSIO	DIFF_IO_2B_B3_P	2B_B	BR41	DIFF_IO_2B_B3p			
E35	HSIO	DIFF_IO_2B_B3_N	2B_B	BU41	DIFF_IO_2B_B3n			
E36	POWER	GND						
E37	HSIO	DIFF_IO_2B_B2_P	2B_B	BR38	DIFF_IO_2B_B2p			
E38	HSIO	DIFF_IO_2B_B2_N	2B_B	BU38	DIFF_IO_2B_B2n			
E39	POWER	GND						
E40	HSIO	DIFF_IO_2B_T16_P	2B_T	BE61	DIFF_IO_2B_T16p	PLL_2B_T_CLKOUT1p	PLL_2B_T_CLKOUT1	PLL_2B_T_FB1
E41	HSIO	DIFF_IO_2B_T16_N	2B_T	BE57	DIFF_IO_2B_T16n	PLL_2B_T_CLKOUT1n		
E42	HSIO	DIFF_IO_2B_T22_N	2B_T	BM49	DIFF_IO_2B_T22n			
E43	HSIO	DIFF_IO_2B_T22_P	2B_T	BK49	DIFF_IO_2B_T22p			
E44	HSIO	DIFF_IO_2B_T13_N	2B_T	BF46	DIFF_IO_2B_T13n			
E45	HSIO	DIFF_IO_2B_T13_P	2B_T	BE46	DIFF_IO_2B_T13p			
E46	HSIO	DIFF_IO_2B_T4_P	2B_T	CF28	DIFF_IO_2B_T4p			
E47	HSIO	DIFF_IO_2B_T4_N	2B_T	CC28	DIFF_IO_2B_T4n			
E48	POWER	GND						
E49	POWER	GND						
E50	POWER	GND						

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Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4
F01	POWER	GND						
F02	HSIO	DIFF_IO_2A_B6_N	2A_B	BM92	DIFF_IO_2A_B6n	CLK_B_2A_1n		
F03	HSIO	DIFF_IO_2A_B6_P	2A_B	BP92	DIFF_IO_2A_B6p	CLK_B_2A_1p		
F04	HSIO	DIFF_IO_2A_B4_N	2A_B	BM89	DIFF_IO_2A_B4n	PLL_2A_B_CLKOUT1n		
F05	HSIO	DIFF_IO_2A_B4_P	2A_B	BK89	DIFF_IO_2A_B4p	PLL_2A_B_CLKOUT1p	PLL_2A_B_CLKOUT1	PLL_2A_B_FB1
F06	HSIO	DIFF_IO_2A_B2_P	2A_B	BH81	DIFF_IO_2A_B2p			
F07	HSIO	DIFF_IO_2A_B2_N	2A_B	BH78	DIFF_IO_2A_B2n			
F08	POWER	GND						
F09	HSIO	DIFF_IO_2A_B9_N	2A_B	BU81	DIFF_IO_2A_B9n	PLL_2A_B_CLKOUT0n		
F10	HSIO	DIFF_IO_2A_B9_P	2A_B	BR81	DIFF_IO_2A_B9p	PLL_2A_B_CLKOUT0p	PLL_2A_B_CLKOUT0	PLL_2A_B_FB0
F11	POWER	GND						
F12	HSIO	DIFF_IO_2A_B17_P	2A_B	CF92	DIFF_IO_2A_B17p			
F13	HSIO	DIFF_IO_2A_B17_N	2A_B	CH92	DIFF_IO_2A_B17n			
F14	POWER	GND						
F15	HSIO	DIFF_IO_2A_T6_P	2A_T	CF71	DIFF_IO_2A_T6p			
F16	HSIO	DIFF_IO_2A_T6_N	2A_T	CH71	DIFF_IO_2A_T6n			
F17	POWER	GND						
F18	POWER	GND						
F19	HSIO	DIFF_IO_2A_T4_N	2A_T	CF69	DIFF_IO_2A_T4n			
F20	HSIO	DIFF_IO_2A_T4_P	2A_T	CH69	DIFF_IO_2A_T4p			
F21	POWER	GND						
F22	POWER	GND						
F23	HSIO	DIFF_IO_2A_T8_N	2A_T	BR59	DIFF_IO_2A_T8n			
F24	HSIO	DIFF_IO_2A_T8_P	2A_T	BU59	DIFF_IO_2A_T8p			
F25	POWER	GND						
F26	POWER	GND						
F27	HSIO	DIFF_IO_2B_B23_P	2B_B	CK73	DIFF_IO_2B_B23p			
F28	HSIO	DIFF_IO_2B_B23_N	2B_B	CL73	DIFF_IO_2B_B23n			
F29	POWER	GND						
F30	POWER	GND						
F31	HSIO	DIFF_IO_2B_B20_P	2B_B	CK56	DIFF_IO_2B_B20p			
F32	HSIO	DIFF_IO_2B_B20_N	2B_B	CL54	DIFF_IO_2B_B20n			
F33	HSIO	DIFF_IO_2B_B18_N	2B_B	CK45	DIFF_IO_2B_B18n			
F34	HSIO	DIFF_IO_2B_B18_P	2B_B	CL42	DIFF_IO_2B_B18p			
F35	POWER	GND						
F36	HSIO	DIFF_IO_2B_B14_P	2B_B	CK33	DIFF_IO_2B_B14p			
F37	HSIO	DIFF_IO_2B_B14_N	2B_B	CL30	DIFF_IO_2B_B14n			
F38	POWER	GND						
F39	HSIO	DIFF_IO_2B_T21_P	2B_T	BP41	DIFF_IO_2B_T21p	PLL_2B_T_CLKOUT0p	PLL_2B_T_CLKOUT0	PLL_2B_T_FB0
F40	HSIO	DIFF_IO_2B_T21_N	2B_T	BM41	DIFF_IO_2B_T21n	PLL_2B_T_CLKOUT0n		
F41	POWER	GND						
F42	HSIO	DIFF_IO_2B_T9_N	2B_T	CL11	DIFF_IO_2B_T9n			
F43	HSIO	DIFF_IO_2B_T9_P	2B_T	CL14	DIFF_IO_2B_T9p			
F44	POWER	GND						
F45	HSIO	DIFF_IO_2B_T11_N	2B_T	CK20	DIFF_IO_2B_T11n			
F46	HSIO	DIFF_IO_2B_T11_P	2B_T	CL20	DIFF_IO_2B_T11p			
F47	POWER	GND						
F48	HSIO	DIFF_IO_2B_T5_P	2B_T	CA31	DIFF_IO_2B_T5p			
F49	HSIO	DIFF_IO_2B_T5_N	2B_T	CC31	DIFF_IO_2B_T5n			
F50	POWER	GND						

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Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2
G01	POWER	VCCIO_2B				
G02	POWER	VCCIO_2B				
G03	HSIO	DIFF_IO_2A_B23_N	2A_B	CL97	DIFF_IO_2A_B23n	
G04	HSIO	DIFF_IO_2A_B23_P	2A_B	CK97	DIFF_IO_2A_B23p	
G05	POWER	GND				
G06	HSIO	DIFF_IO_2A_B22_N	2A_B	CK88	DIFF_IO_2A_B22n	
G07	HSIO	DIFF_IO_2A_B22_P	2A_B	CL88	DIFF_IO_2A_B22p	
G08	POWER	GND				
G09	HSIO	DIFF_IO_2A_B18_N	2A_B	CA92	DIFF_IO_2A_B18n	
G10	HSIO	DIFF_IO_2A_B18_P	2A_B	CC92	DIFF_IO_2A_B18p	
G11	HSIO	DIFF_IO_2A_T18_P	2A_T	BM71	DIFF_IO_2A_T18p	CLK_T_2A_1p
G12	HSIO	DIFF_IO_2A_T18_N	2A_T	BP71	DIFF_IO_2A_T18n	CLK_T_2A_1n
G13	HSIO	DIFF_IO_2A_T22_N	2A_T	BE86	DIFF_IO_2A_T22n	
G14	HSIO	DIFF_IO_2A_T22_P	2A_T	BF86	DIFF_IO_2A_T22p	
G15	POWER	GND				
G16	POWER	GND				
G17	XCVR_RX	GTSR4B_RX_CH0_P	4B	BF1	GTSR4B_RX_CH0p	
G18	XCVR_RX	GTSR4B_RX_CH0_N	4B	BF3	GTSR4B_RX_CH0n	
G19	POWER	GND				
G20	POWER	GND				
G21	XCVR_RX	GTSR4B_RX_CH1_P	4B	BD1	GTSR4B_RX_CH1p	
G22	XCVR_RX	GTSR4B_RX_CH1_N	4B	BD3	GTSR4B_RX_CH1n	
G23	POWER	GND				
G24	POWER	GND				
G25	XCVR_RX	GTSR4B_RX_CH2_P	4B	BB1	GTSR4B_RX_CH2p	
G26	XCVR_RX	GTSR4B_RX_CH2_N	4B	BB3	GTSR4B_RX_CH2n	
G27	POWER	GND				
G28	POWER	GND				
G29	XCVR_RX	GTSR4B_RX_CH3_P	4B	AY1	GTSR4B_RX_CH3p	
G30	XCVR_RX	GTSR4B_RX_CH3_N	4B	AY3	GTSR4B_RX_CH3n	
G31	POWER	GND				
G32	HSIO	DIFF_IO_2B_B19_N	2B_B	CK54	DIFF_IO_2B_B19n	
G33	HSIO	DIFF_IO_2B_B19_P	2B_B	CL51	DIFF_IO_2B_B19p	
G34	HSIO	DIFF_IO_2B_B15_N	2B_B	CL35	DIFF_IO_2B_B15n	
G35	HSIO	DIFF_IO_2B_B15_P	2B_B	CK35	DIFF_IO_2B_B15p	
G36	POWER	GND				
G37	HSIO	DIFF_IO_2B_B13_P	2B_B	CK30	DIFF_IO_2B_B13p	
G38	HSIO	DIFF_IO_2B_B13_N	2B_B	CL26	DIFF_IO_2B_B13n	
G39	POWER	GND				
G40	HSIO	DIFF_IO_2B_T8_N	2B_T	CL8	DIFF_IO_2B_T8n	
G41	HSIO	DIFF_IO_2B_T8_P	2B_T	CK11	DIFF_IO_2B_T8p	
G42	POWER	GND				
G43	HSIO	DIFF_IO_2B_T12_P	2B_T	CL23	DIFF_IO_2B_T12p	
G44	HSIO	DIFF_IO_2B_T12_N	2B_T	CK26	DIFF_IO_2B_T12n	
G45	POWER	GND				
G46	HSIO	DIFF_IO_2B_T3_N	2B_T	CA22	DIFF_IO_2B_T3n	
G47	HSIO	DIFF_IO_2B_T3_P	2B_T	CC22	DIFF_IO_2B_T3p	
G48	POWER	GND				
G49	HSIO	DIFF_IO_2B_T1_P	2B_T	CF19	DIFF_IO_2B_T1p	
G50	HSIO	DIFF_IO_2B_T1_N	2B_T	CC19	DIFF_IO_2B_T1n	

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Pin	Class	Schematic Net Name	FPGA Bank	FPGA Pin	Signal Option 1	Signal Option 2
H01	POWER	GND				
H02	POWER	GND				
H03	HSIO	DIFF_IO_2A_B24_N	2A_B	CK94	DIFF_IO_2A_B24n	
H04	HSIO	DIFF_IO_2A_B24_P	2A_B	CL91	DIFF_IO_2A_B24p	
H05	POWER	GND				
H06	HSIO	DIFF_IO_2A_B21_N	2A_B	CL85	DIFF_IO_2A_B21n	
H07	HSIO	DIFF_IO_2A_B21_P	2A_B	CK85	DIFF_IO_2A_B21p	
H08	POWER	GND				
H09	HSIO	DIFF_IO_2A_B20_N	2A_B	CL82	DIFF_IO_2A_B20n	
H10	HSIO	DIFF_IO_2A_B20_P	2A_B	CK80	DIFF_IO_2A_B20p	
H11	POWER	GND				
H12	HSIO	DIFF_IO_2A_B19_P	2A_B	CK76	DIFF_IO_2A_B19p	
H13	HSIO	DIFF_IO_2A_B19_N	2A_B	CL76	DIFF_IO_2A_B19n	
H14	POWER	GND				
H15	XCVR_REFCLK	REFCLK_GTSR4B_RX_P	4B	AY16	REFCLK_GTSR4B_RX_P	
H16	XCVR_REFCLK	REFCLK_GTSR4B_RX_N	4B	AY21	REFCLK_GTSR4B_RX_N	
H17	POWER	GND				
H18	POWER	GND				
H19	XCVR_TX	GTSR4B_TX_CH0_P	4B	BE7	GTSR4B_TX_CH0p	
H20	XCVR_TX	GTSR4B_TX_CH0_N	4B	BE10	GTSR4B_TX_CH0n	
H21	POWER	GND				
H22	POWER	GND				
H23	XCVR_TX	GTSR4B_TX_CH1_P	4B	BC7	GTSR4B_TX_CH1p	
H24	XCVR_TX	GTSR4B_TX_CH1_N	4B	BC10	GTSR4B_TX_CH1n	
H25	POWER	GND				
H26	POWER	GND				
H27	XCVR_TX	GTSR4B_TX_CH2_P	4B	BA7	GTSR4B_TX_CH2p	
H28	XCVR_TX	GTSR4B_TX_CH2_N	4B	BA10	GTSR4B_TX_CH2n	
H29	POWER	GND				
H30	POWER	GND				
H31	XCVR_TX	GTSR4B_TX_CH3_P	4B	AW7	GTSR4B_TX_CH3p	
H32	XCVR_TX	GTSR4B_TX_CH3_N	4B	AW10	GTSR4B_TX_CH3n	
H33	POWER	GND				
H34	POWER	GND				
H35	XCVR_REFCLK	REFCLK_GTSR4B_CH1_P	4B	AV16	REFCLK_GTSR4B_CH1p	
H36	XCVR_REFCLK	REFCLK_GTSR4B_CH1_N	4B	AV21	REFCLK_GTSR4B_CH1n	
H37	POWER	GND				
H38	HSIO	DIFF_IO_2B_T18_N	2B_T	BE68	DIFF_IO_2B_T18n	CLK_T_2B_1n
H39	HSIO	DIFF_IO_2B_T18_P	2B_T	BF68	DIFF_IO_2B_T18p	CLK_T_2B_1p
H40	POWER	GND				
H41	HSIO	DIFF_IO_2B_T23_N	2B_T	BH52	DIFF_IO_2B_T23n	
H42	HSIO	DIFF_IO_2B_T23_P	2B_T	BH49	DIFF_IO_2B_T23p	
H43	POWER	GND				
H44	HSIO	DIFF_IO_2B_T14_P	2B_T	BF50	DIFF_IO_2B_T14p	
H45	HSIO	DIFF_IO_2B_T14_N	2B_T	BE50	DIFF_IO_2B_T14n	
H46	POWER	GND				
H47	HSIO	DIFF_IO_2B_T2_N	2B_T	CH22	DIFF_IO_2B_T2n	
H48	HSIO	DIFF_IO_2B_T2_P	2B_T	CF22	DIFF_IO_2B_T2p	
H49	HSIO	DIFF_IO_2B_T6_P	2B_T	CH31	DIFF_IO_2B_T6p	
H50	HSIO	DIFF_IO_2B_T6_N	2B_T	CF31	DIFF_IO_2B_T6n	

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J4 Connector Interface

In addition to J1 and J2, there is an additional top side connector, J4, that is available for SOMs with FPGA densities of 232 KLE or less. The connector utilizes a Samtec SS4-15-3.00-L-D-K-TR 30 position male header and provides access to the HVIO Bank 6E and Bank 6F pins as well as the 1.8V supply used to power the Bank 6E/6F HVIO pins. Table 10 lists the connections to J4.

Table 10 J4 Pin Connection Information

J4 Pin	Net	FPGA Pin	FPGA Bank	J4 Pin	Net	FPGA Pin	FPGA Bank
1	+1.8V	-		2	+1.8V	-	
3	SPARE14	K18	6E	4	SPARE1	AJ1	6F
5	SPARE15	K15	6E	6	SPARE2	AJ2	6F
7	SPARE16	M18	6E	8	SPARE3	AF2	6F
9	SPARE17	M15	6E	10	SPARE4	AD1	6F
11	SPARE18	P15	6E	12	SPARE5	AH4	6E
13	SPARE19	T18	6E	14	SPARE6	AA1	6F
15	SPARE20	T15	6E	16	SPARE7	AD2	6F
17	SPARE21	M8	6E	18	SPARE8	AH8	6E
19	SPARE22	V18	6E	20	SPARE9	AG13	6E
21	SPARE23	Y18	6E	22	SPARE10	AB8	6E
23	SPARE24	Y15	6E	24	SPARE11	Y8	6E
25	SPARE25	T8	6E	26	SPARE12	V8	6E
27	SPARE26	AB18	6E	28	SPARE13	AB15	6E
29	GND	-		30	GND	-	

ELECTRICAL CHARACTERISTICS

Table 11 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCC_IN	Voltage supply, +5V to +12V input		5	12.0	13.2	Volts
I_{core}	Maximum current available for VCC_{core} and related FPGA supplies.	FPGA densities less than 434 KLE			25.0	Amps
		FPGA densities 434 KLE or higher.			50.0	Amps
$I_{12.0}$	Quiescent Current draw	12.0 volt input, 1333 MHz LPDDR4, no FPGA fabric, Linux prompt		7200		mA
$I_{12.0\text{-}max}$	Max current draw	12.0 volt input		TBS	5	A
	1. Power utilization of the MitySOM-A5E is heavily dependent on end-user application. Major factors include: ARM CPU PLL configuration, CPU Utilization, and external DDR4 RAM utilization. See section Power Interfaces for more info.					

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ORDERING INFORMATION

Growth Options

The MitySOM-A5E has been designed to support several upgrade options. These options include a range of speed grades, FPGA density, HPS and FPGA DDR memory configurations, and operating temperature specifications including commercial and industrial temperature ranges. Standard options are listed in the section below. For availability and additional ordering information regarding these options, or to inquire about a configuration not listed below, please contact Critical Link at info@criticallink.com.

Orderable Part Numbers

The following table lists the standard module configurations. For availability, price, and minimum order quantity of these configurations, or to inquire about a development kit for these products, contact Critical Link via email at info@criticallink.com.

Table 11 Standard Model Numbers

Model / Part Number	FPGA KLE	SoC Speed Grade	No. XCVRs	HPS RAM (32-bit)	FPGA RAM (32-bit)	On-board Flash	Component Temperature Ratings
A5ED-B64-144-SRI	656	4	24	4GB	4GB	32MB	-40C to +85C
A5ED-B46-144-SRI	434	6	16	4GB	4GB	32MB	-40C to +85C
A5ED-B16-1X4-SRI	138	6	4	4GB	N/A	32MB	-40C to +85C

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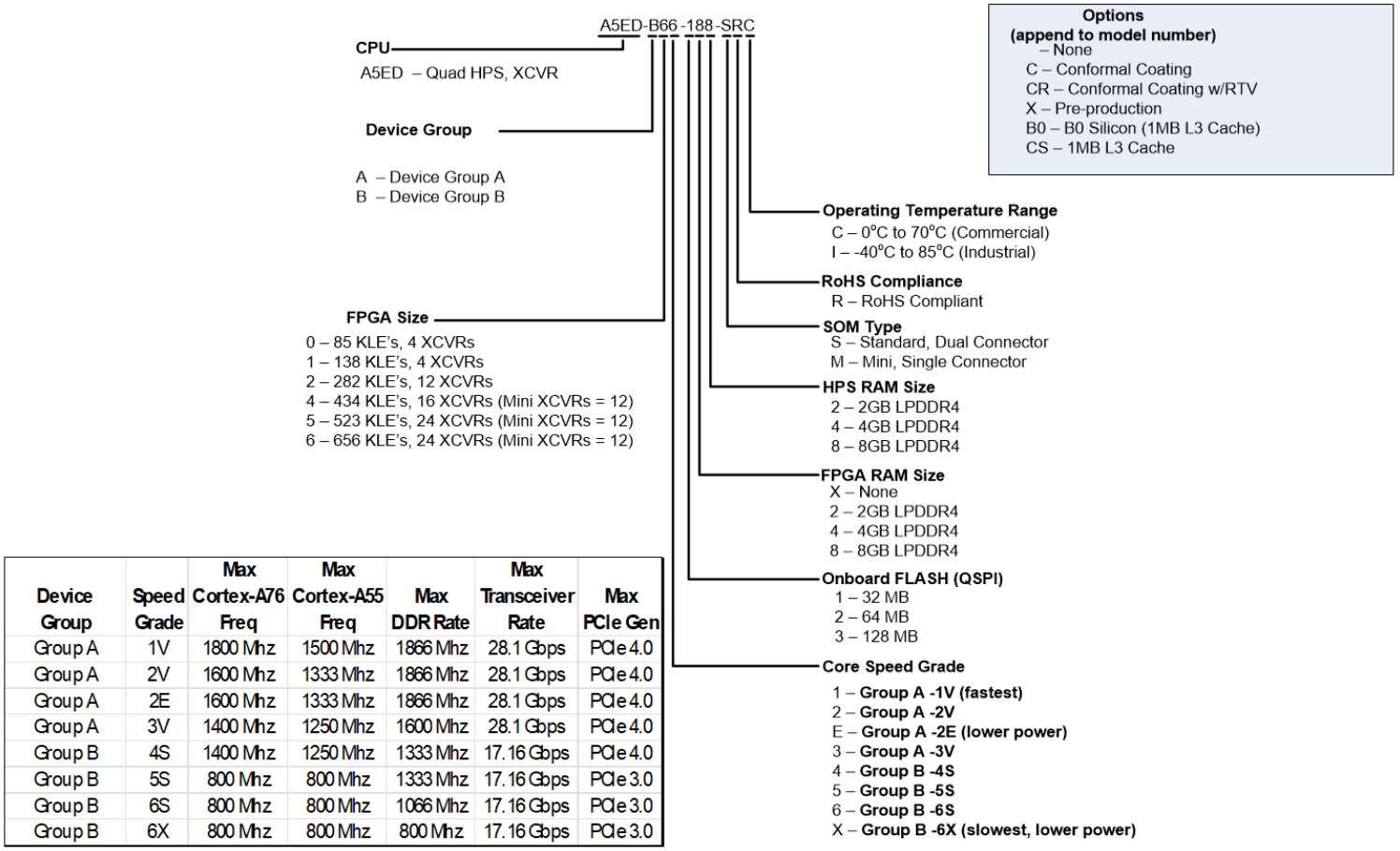
MitySOM-A5E Module Family Model Number Guide

If the standard variants listed above are not suitable for your requirements, customers may reference the following MitySOM-A5E model number decoder to configure a custom module. Please contact Critical Link at info@criticallink.com to determine pricing, lead-time and availability of a custom module. Note that some configurations may not be available.

Figure 3 MitySOM-A5E Family Model Number Scheme



Device Group	Speed Grade	Max Cortex-A76 Freq	Max Cortex-A55 Freq	Max DDR Rate	Max Transceiver Rate	Max PCIe Gen
Group A	1V	1800 Mhz	1500 Mhz	1866 Mhz	28.1 Gbps	PCIe 4.0
Group A	2V	1600 Mhz	1333 Mhz	1866 Mhz	28.1 Gbps	PCIe 4.0
Group A	2E	1600 Mhz	1333 Mhz	1866 Mhz	28.1 Gbps	PCIe 4.0
Group A	3V	1400 Mhz	1250 Mhz	1600 Mhz	28.1 Gbps	PCIe 4.0
Group B	4S	1400 Mhz	1250 Mhz	1333 Mhz	17.16 Gbps	PCIe 4.0
Group B	5S	800 Mhz	800 Mhz	1333 Mhz	17.16 Gbps	PCIe 3.0
Group B	6S	800 Mhz	800 Mhz	1066 Mhz	17.16 Gbps	PCIe 3.0
Group B	6X	800 Mhz	800 Mhz	800 Mhz	17.16 Gbps	PCIe 3.0

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MECHANICAL INTERFACE

A top and bottom view mechanical outline of the MitySOM-A5E is illustrated in Figure 4 and Figure 5. The alignment holes for the board-to-board interfaces are shown.

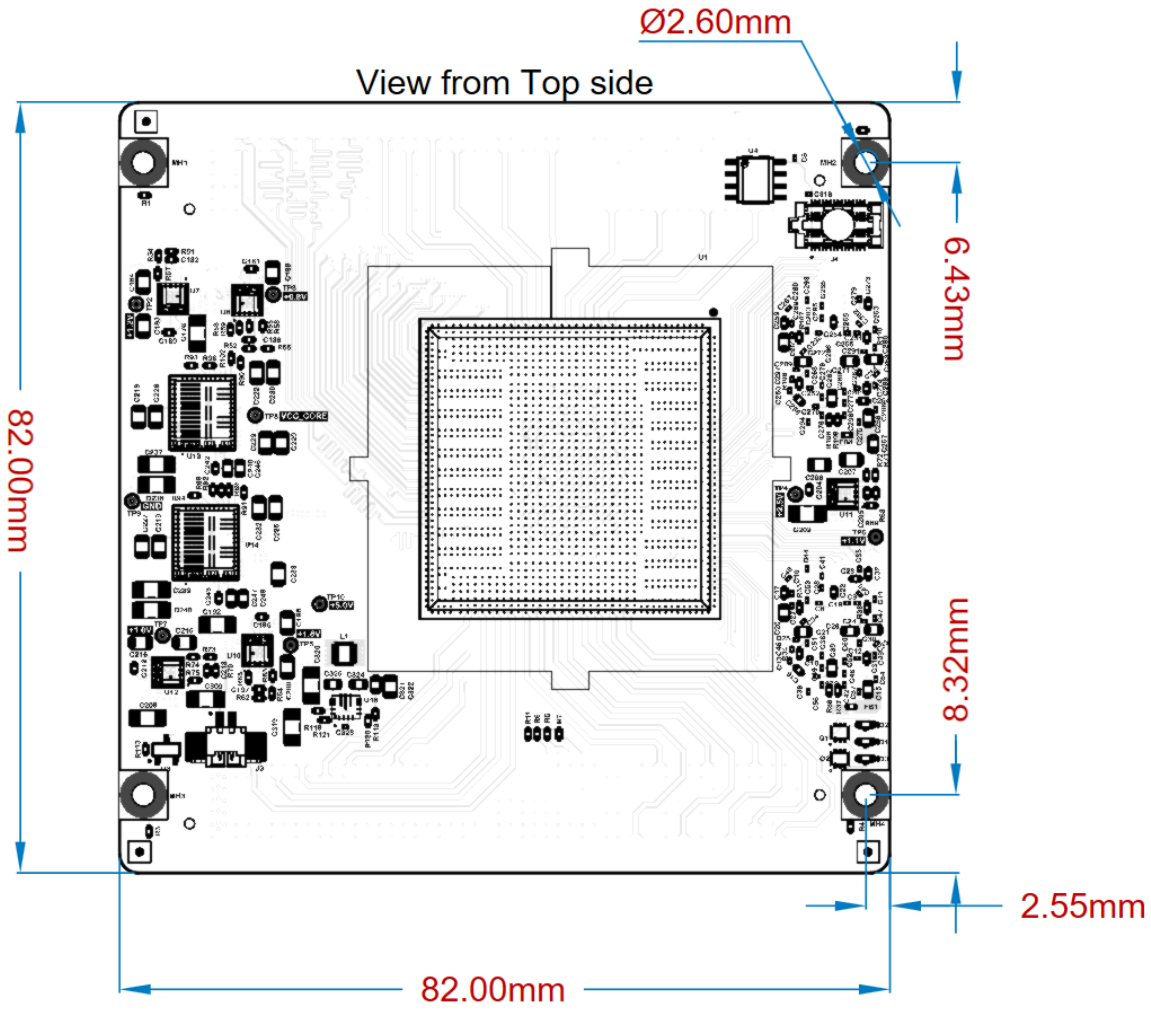

Figure 4 MitySOM-A5E Mechanical Outline, View from Top

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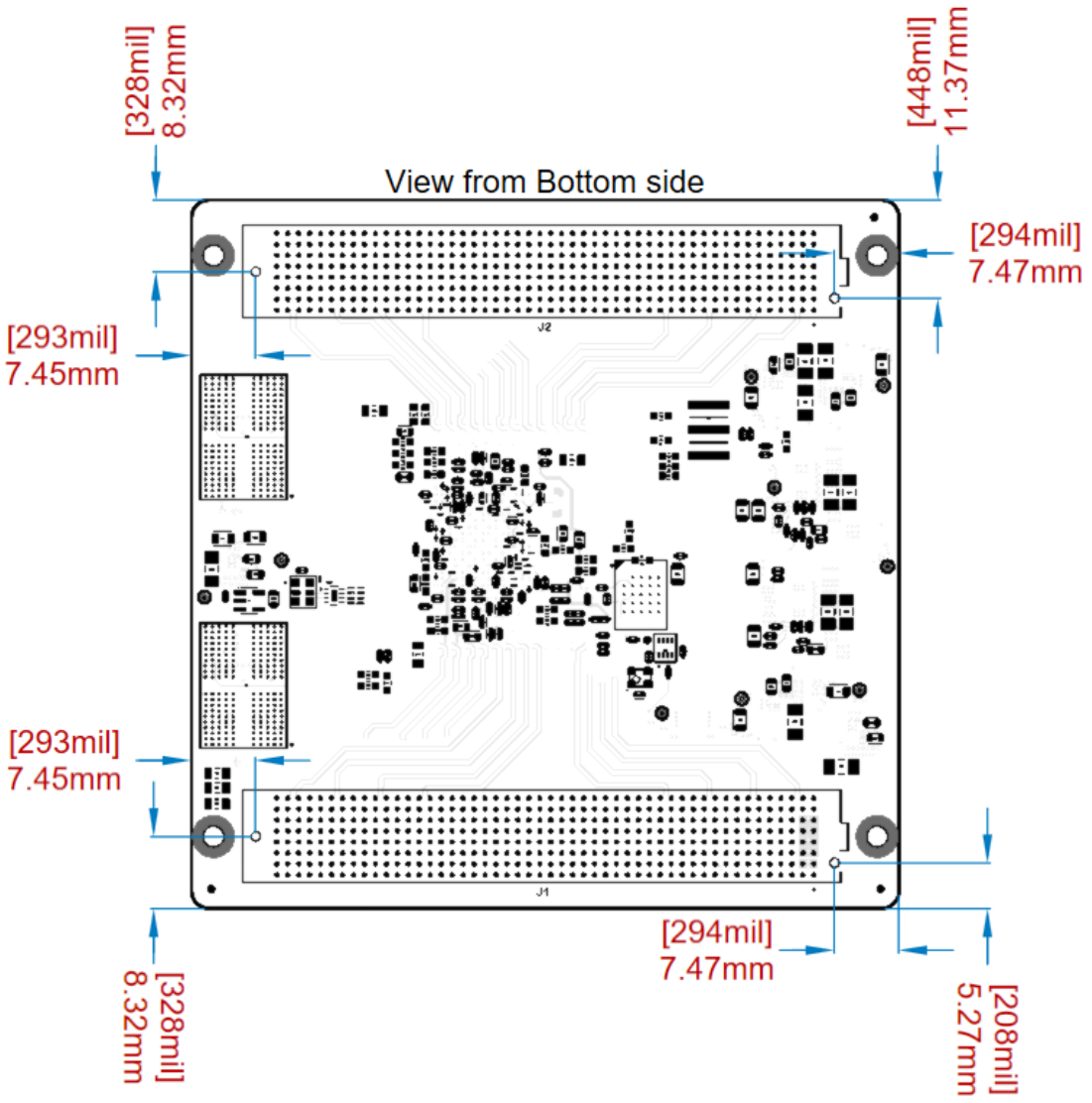

Figure 5 MitySOM-A5E Mechanical Outline, View from Bottom

REVISION HISTORY

Revision	Date	Change Description
A	November 19, 2024	Preliminary Release for early adopters
B	February 5, 2025	Updated J1 and J2 Connection Table, added J4 connection table. Updated Mechanical Drawings.
C	October 2, 2025	Clarification on IO availability per density and differences between speed grades
D	December 12, 2025	Updated DDR Rate for Speed grade 6 and 3 devices Clarification on transceiver block availability

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