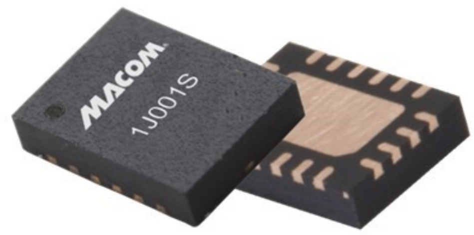
Features
- Saturated Power: 1 W
- Power Added Efficiency: 30 %
- Large Signal Gain: 23 dB
- Small Signal Gain: 27 dB
- Input Return Loss: -10 dB
- Output Return Loss: -8 dB
- CW Operation
- Small 4x3 mm footprint

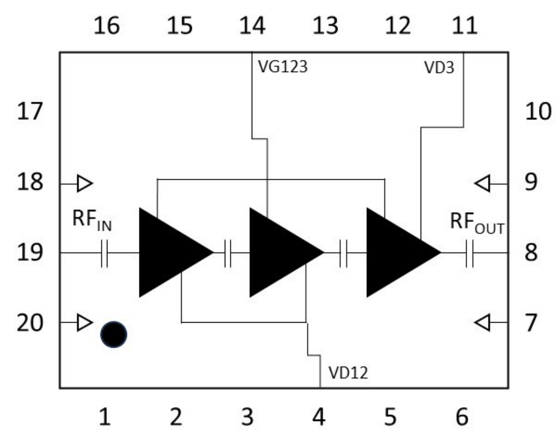


Applications
- Military, Commercial Radar, & Communications
- General Purposed Broadband Amplifier

Description
The CMPA1D1J001S is a 1 W packaged MMIC HPA utilizing a high performance, 0.15 µm GaN-on-SiC production process. The CMPA1D1J001S operates from 12.7 - 18.0 GHz and supports both radar and communication applications within both military and commercial markets. The CMPA1D1J001S achieves 1 W of saturated output power with 23 dB of large signal gain and typically 30% power-added efficiency under CW operation.

Packaged in a 4x3 mm plastic over-mold QFN, the CMPA1D1J001S provides superior broadband performance and environmental robustness in a small form factor allowing customers to improve SWaP-C benchmarks in their next-generation systems.

Functional Schematic



Pin Configuration[1, 2]

Pin #	Function
1-3, 5, 6, 10, 12, 13, 15-17	NC
7, 9, 18, 20	RF Ground
4	VD12
8	RF Output
11	VD3
14	VG123
19	RF Input

1. MACOM recommends connecting No Connection (N/C) pins to ground.
2. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

Ordering Information

Part Number	Package (MOQ/ Mult)
CMPA1D1J001S	Tray (100/100)
CMPA1D1J001S-AMP1	Sample Board (1/1)

RF Electrical Specifications: V_D = 22 V, I_{DQ} = 30 mA, CW, T_C = 25°C, Z_0 = 50 Ω

Parameter	Test Conditions	Frequency (GHz)	Units	Min.	Typ.	Max.
Output Power	P_{IN} = 8 dBm	12.7 14.25 18	dBm	30.0 30.0 30.0	30.5 31.0 30.5	—
Power Added Efficiency	P_{IN} = 8 dBm	12.7 14.25 18	%	27 28 30	28 32 34	—
Large Signal Gain	P_{IN} = 8 dBm	12.7 14.25 18	dB	22 22 22	22.5 23.0 22.5	—
Small Signal Gain	P_{IN} = -20 dBm	12.7 14.25 18	dB	—	27 27 24	—
Input Return Loss	P_{IN} = -20 dBm	12.7 - 18	dB	—	-10	—
Output Return Loss	P_{IN} = -20 dBm	12.7 - 18	dB	—	-8	—

DC Electrical Specifications:

Parameter	Units	Min.	Typ.	Max.
Drain Voltage	V	—	22	—
Gate Voltage	V	—	-2.0	—
Quiescent Drain Current	mA	—	30	—
Saturated Drain Current	mA	—	180	—

Recommended Operating Conditions

Parameter	Symbol	Unit	Min.	Typ.	Max.
Input Power	P_{IN}	dBm	—	8	—
Drain Voltage	V_D	V	—	22	—
Gate Voltage	V_G	V	—	-2.0	—
Quiescent Drain Current	I_{DQ}	mA	—	30	—
Operating Temperature	T_C	°C	-40	—	+85

Absolute Maximum Ratings[3,4]

Parameter	Symbol	Unit	Min.	Max.
Input Power	P_{IN}	dBm	—	10
Drain to Source Voltage	V_{DS}	V	—	84
Drain Voltage	V_D	V	—	28
Gate Voltage	V_G	V	-8	+2
Drain Current	I_D	A	—	0.8
Gate Current	I_G	mA	—	1.0
Dissipated Power @ +85°	P_{DISS}	W	—	4.4
VSWR	—	Ratio	—	5:1
Junction Temperature (MTTF > 1E6 Hrs)	T_J	°C	—	+225
Storage Temperature	T_{STG}	°C	-55	+150
Mounting Temperature (30 seconds)	T_M	°C	—	+260

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

Please observe the following precautions to avoid damage:

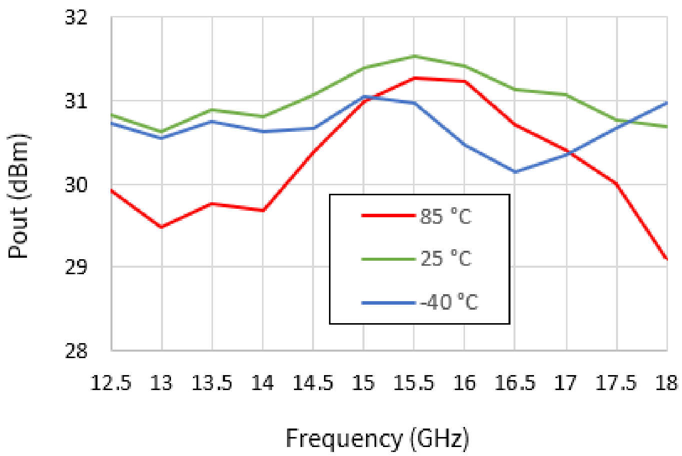
Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these HBM class 1A and CDM class C2a devices.

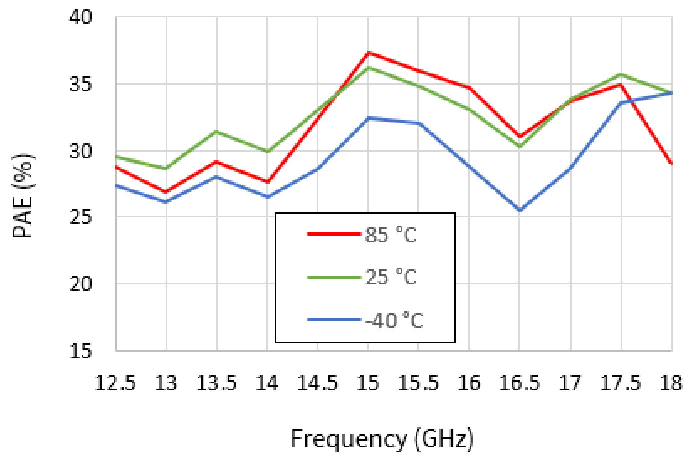
Typical Performance Curves - Large Signal over Temperature

V_D = 22 V, I_{DQ} = 30 mA, CW, P_{IN} = 8 dBm

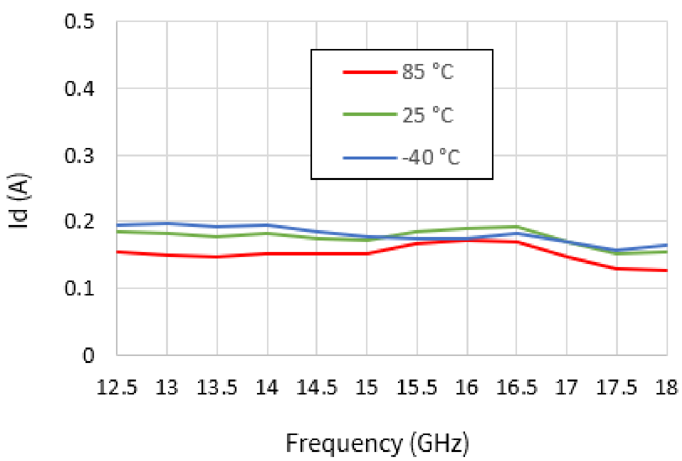
Output Power vs. Frequency



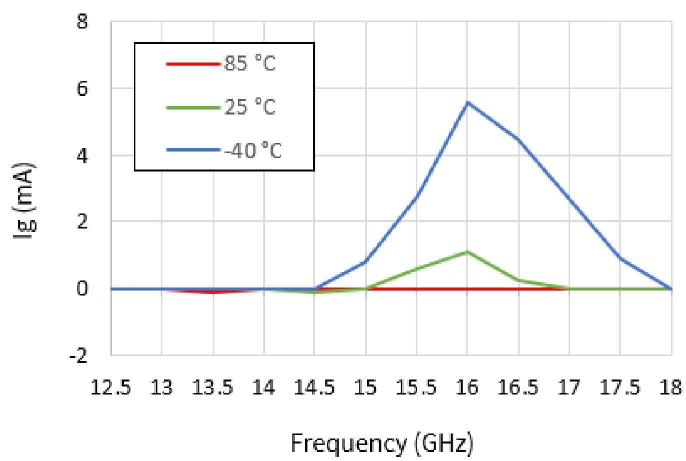
Power Added Efficiency vs. Frequency



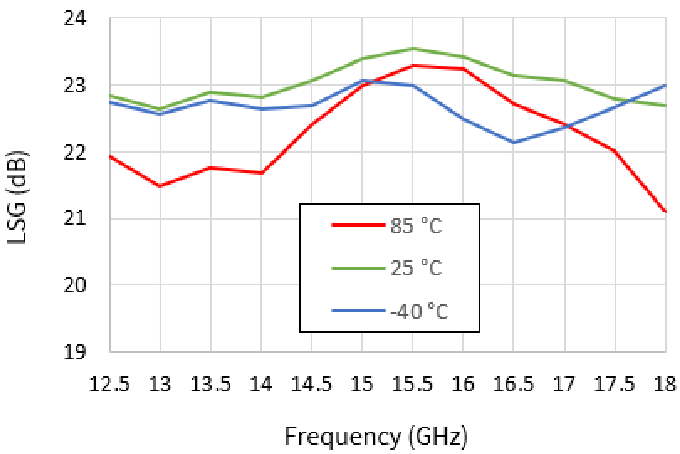
Drain Current vs. Frequency



Gate Current vs. Frequency



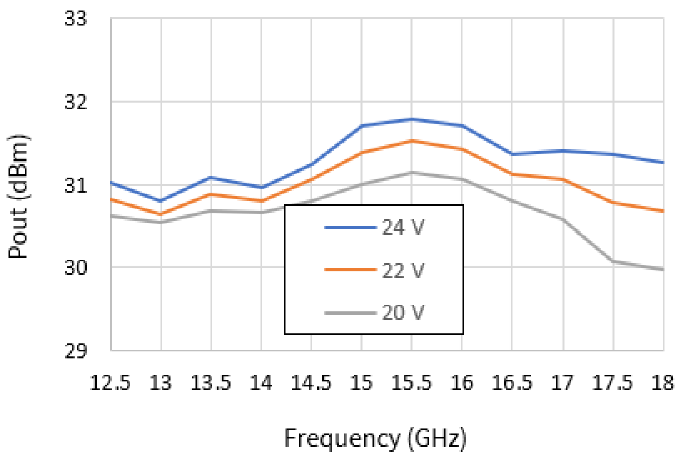
Large Signal Gain vs. Frequency



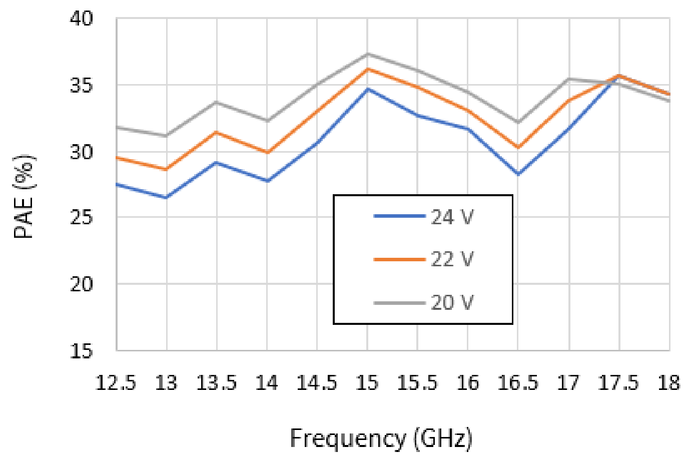
Typical Performance Curves - Large Signal over V_D

I_{DQ} = 30 mA, CW, P_{IN} = 8 dBm, T_C = 25°C

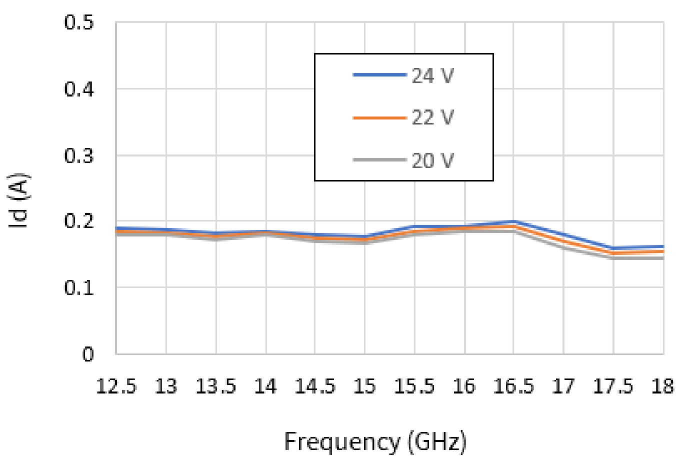
Output Power vs. Frequency



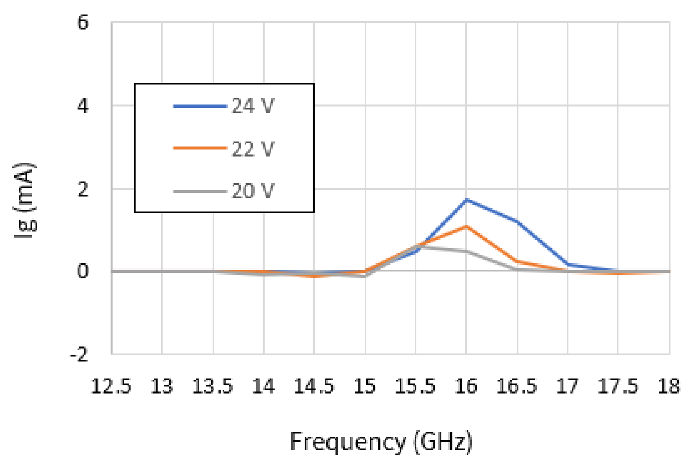
Power Added Efficiency vs. Frequency



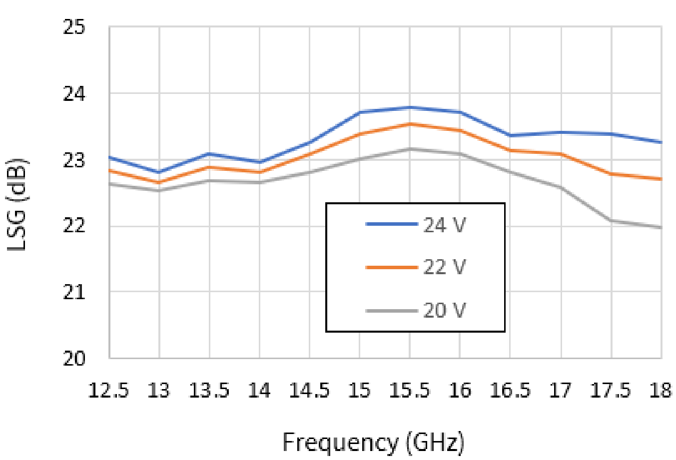
Drain Current vs. Frequency



Gate Current vs. Frequency



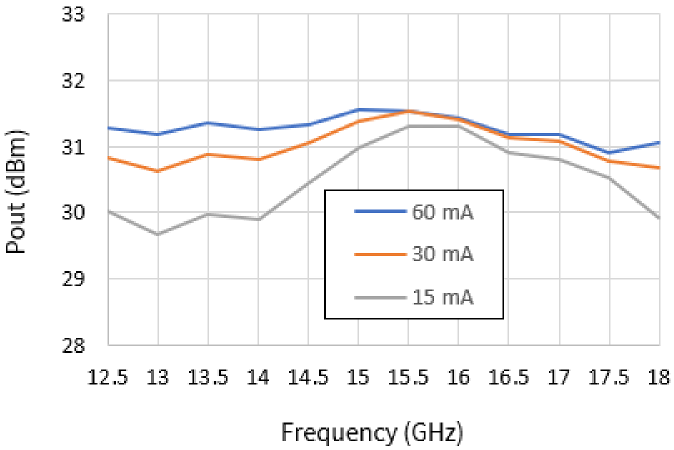
Large Signal Gain vs. Frequency



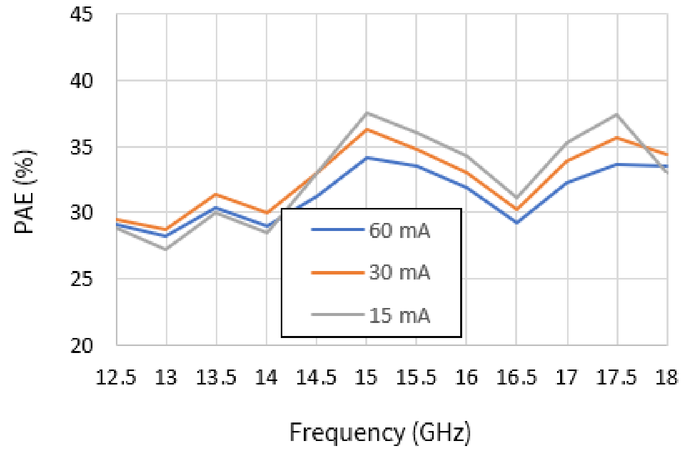
Typical Performance Curves - Large Signal over I_{DQ}

V_D = 22 V, CW, P_{IN} = 8 dBm, T_C = 25°C

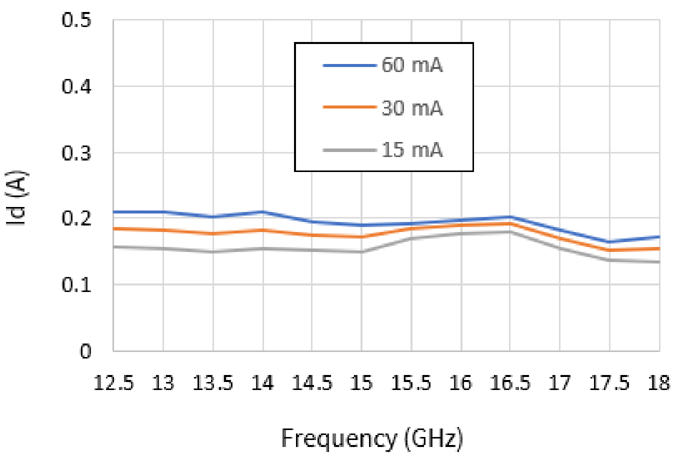
Output Power vs. Frequency



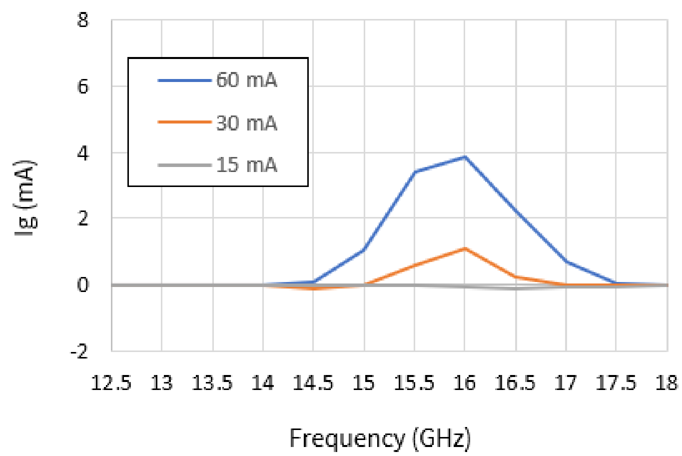
Power Added Efficiency vs. Frequency



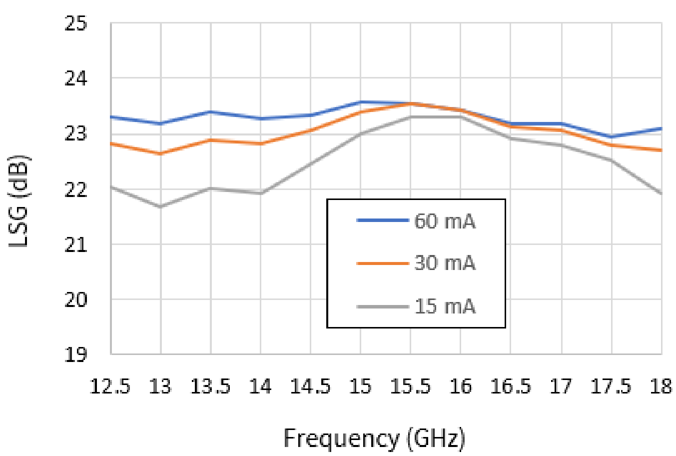
Drain Current vs. Frequency



Gate Current vs. Frequency



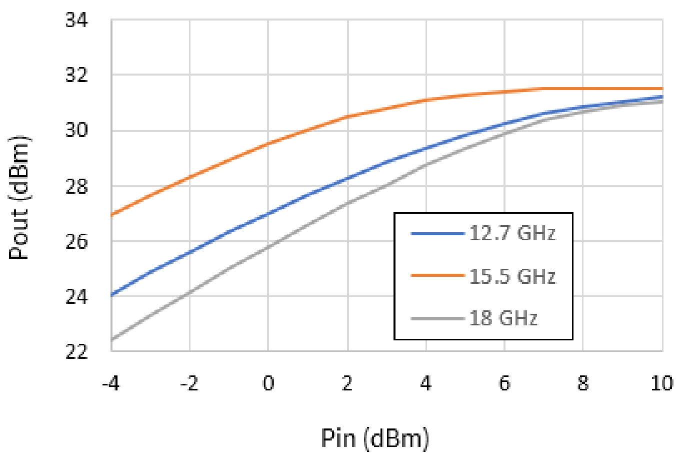
Large Signal Gain vs. Frequency



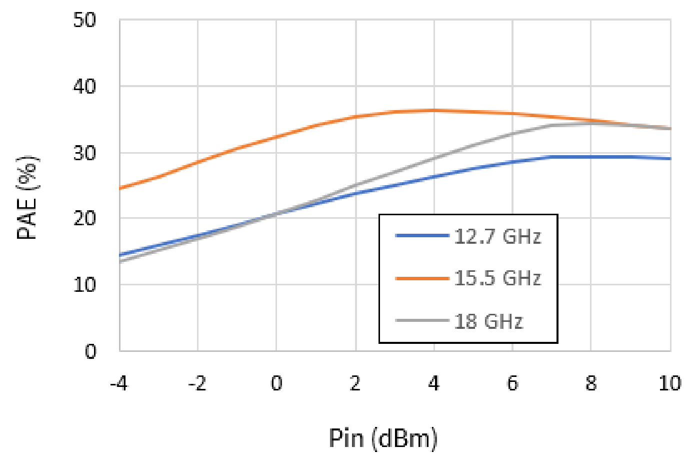
Typical Performance Curves - Drive-Up over Frequency

V_D = 22 V, I_{DQ} = 30 mA, CW, T_C = 25°C

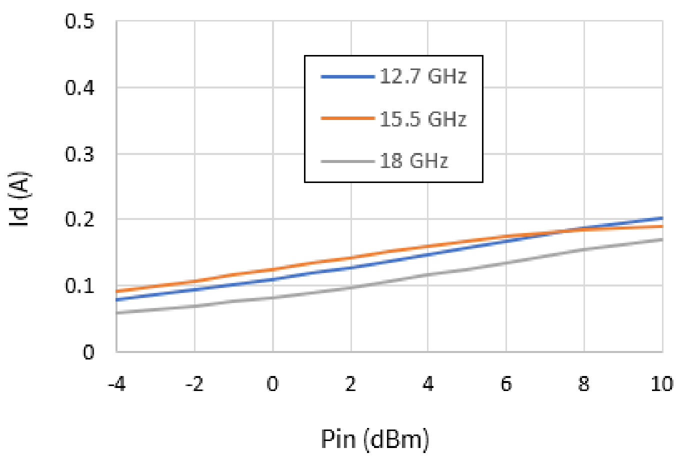
Output Power vs. Input Power



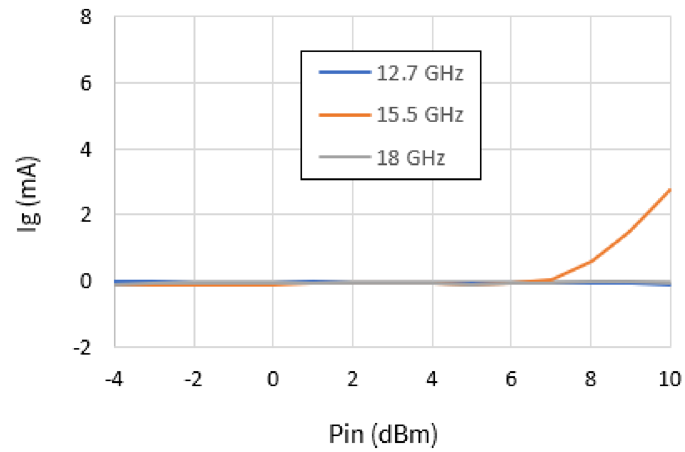
Power Added Efficiency vs. Input Power



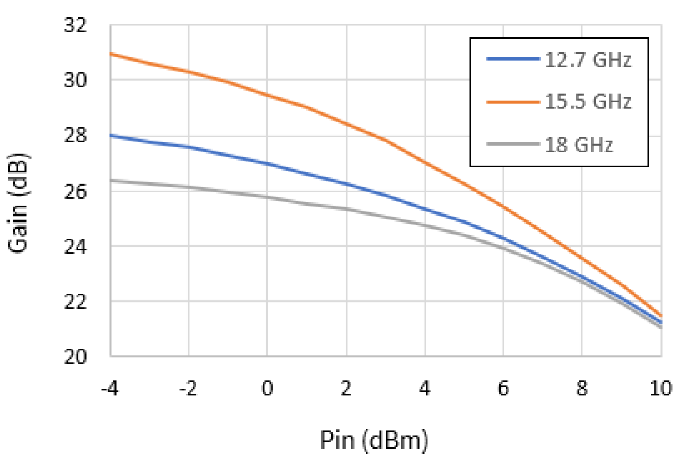
Drain Current vs. Input Power



Gate Current vs. Input Power



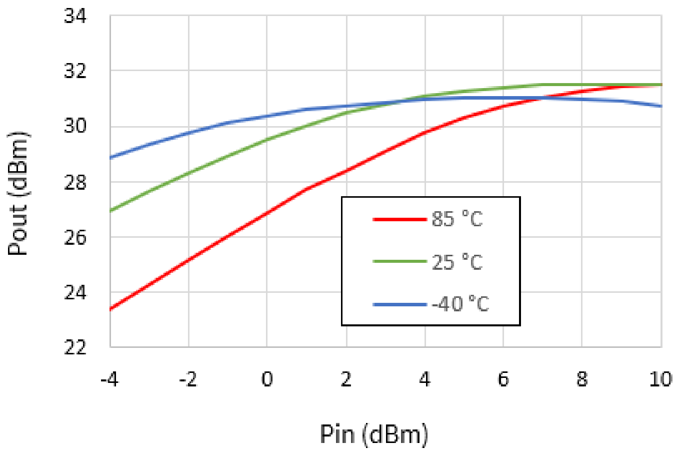
Gain vs. Input Power



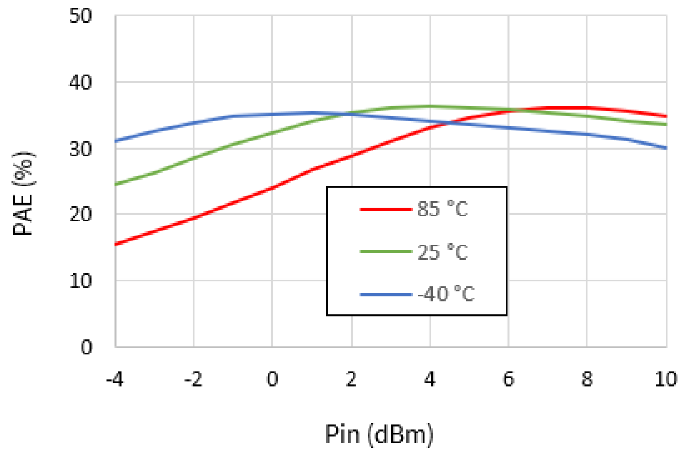
Typical Performance Curves - Drive-Up Over Temperature

V_D = 22 V, I_{DQ} = 30 mA, CW, Frequency = 15.5 GHz

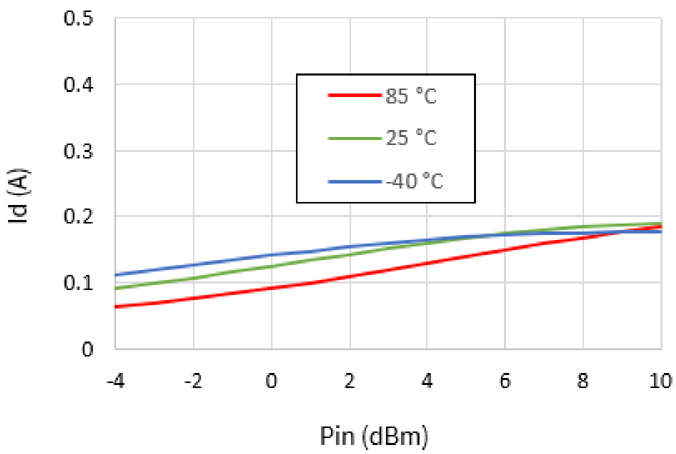
Output Power vs. Input Power



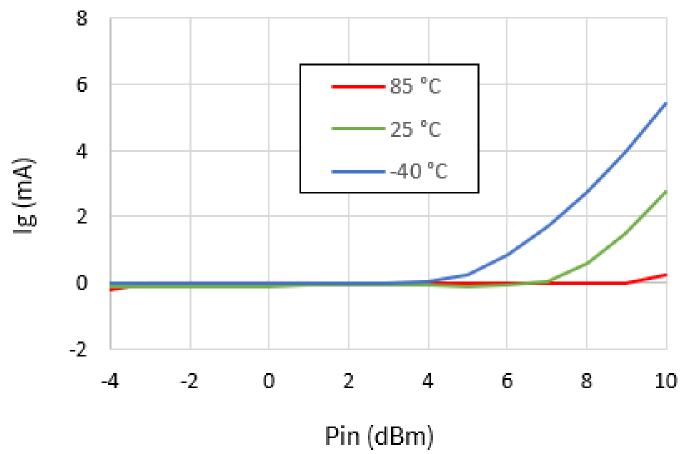
Power Added Efficiency vs. Input Power



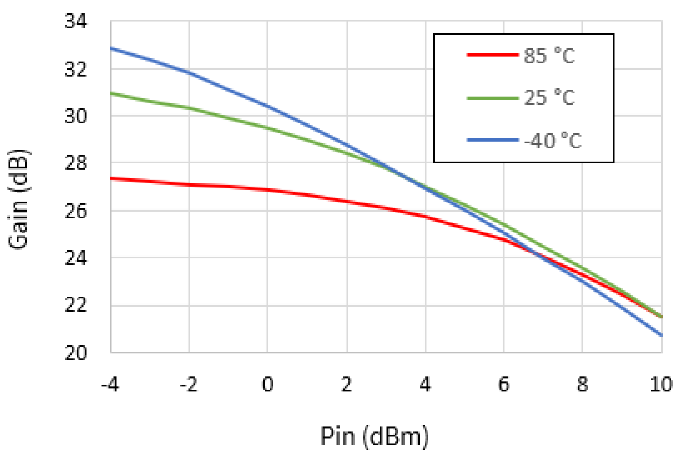
Drain Current vs. Input Power



Gate Current vs. Input Power



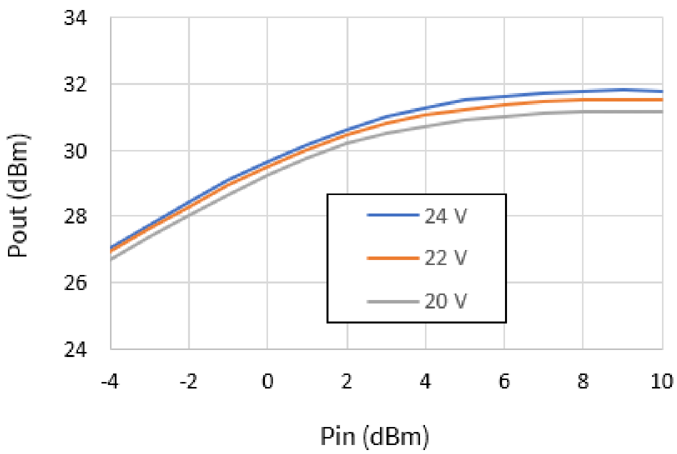
Gain vs. Input Power



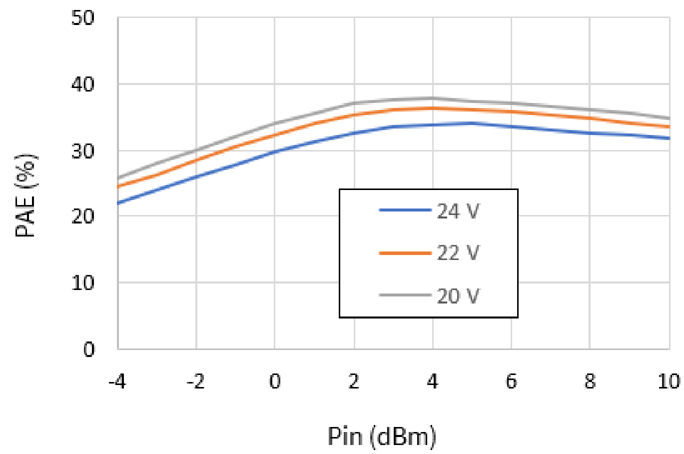
Typical Performance Curves - Drive-Up over V_D

I_{DQ} = 30 mA, CW, Frequency = 15.5 GHz, T_C = 25°C

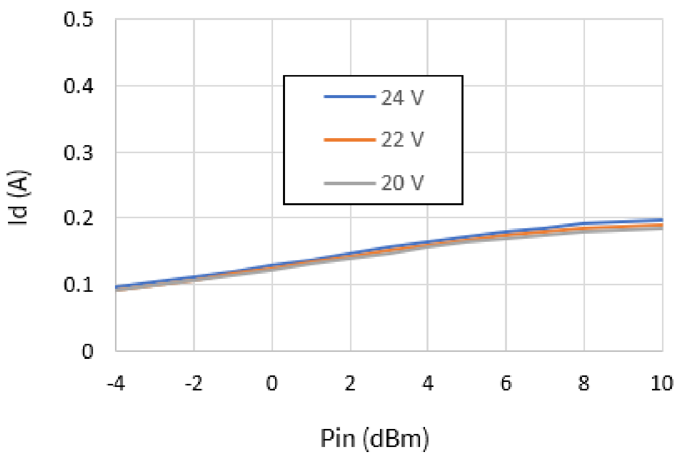
Output Power vs. Input Power



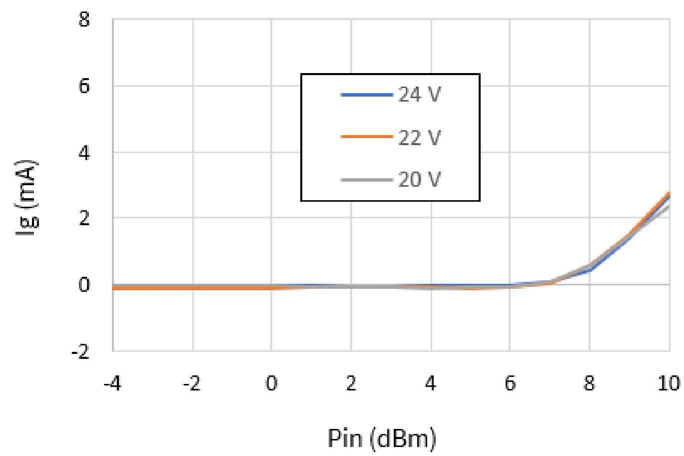
Power Added Efficiency vs. Input Power



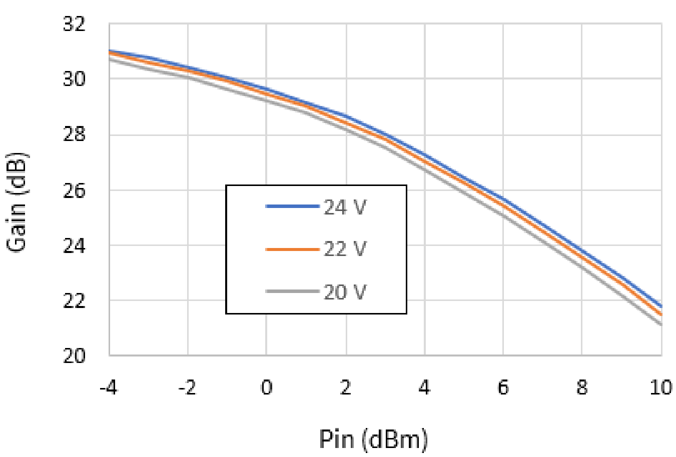
Drain Current vs. Input Power



Gate Current vs. Input Power



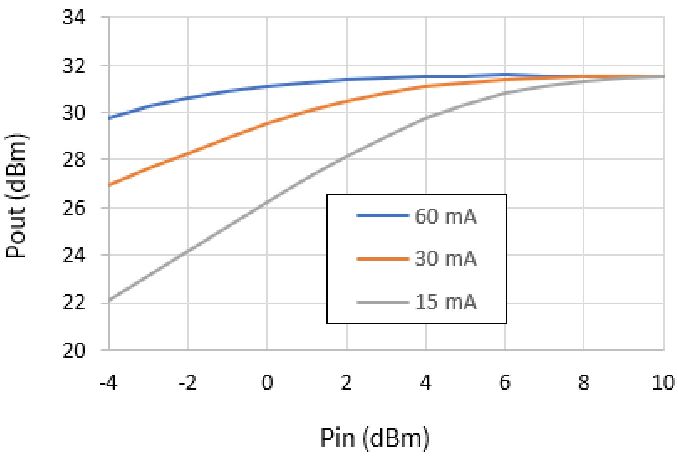
Gain vs. Input Power



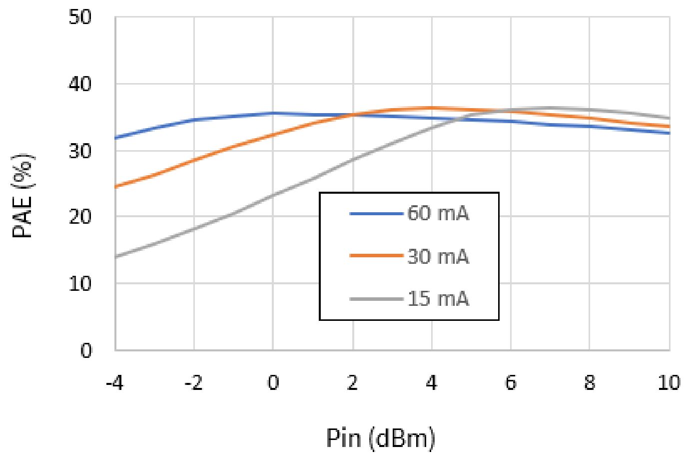
Typical Performance Curves - Drive-Up over I_{DQ}

V_D = 22 V, CW, Frequency = 15.5 GHz, T_C = 25°C

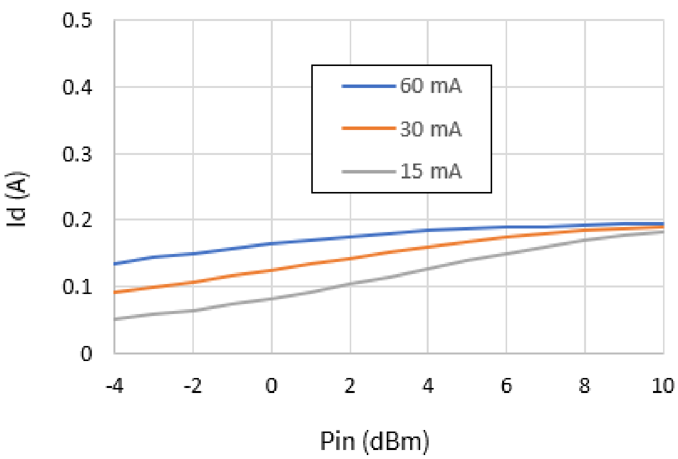
Output Power vs. Input Power



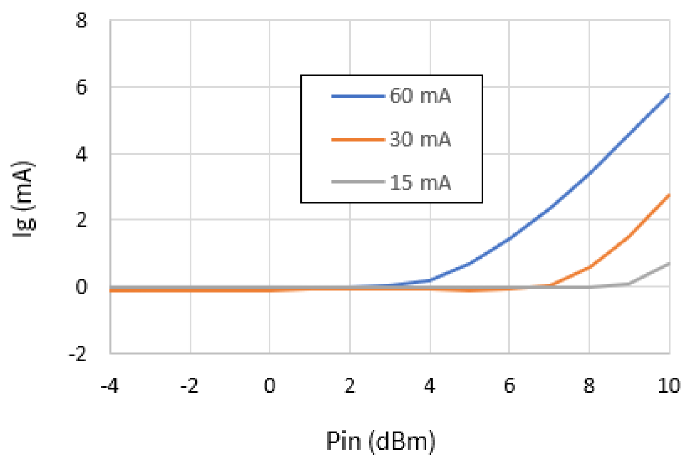
Power Added Efficiency vs. Input Power



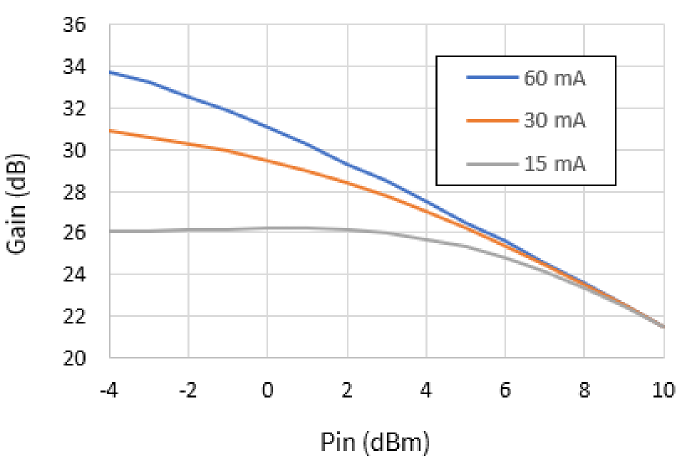
Drain Current vs. Input Power



Gate Current vs. Input Power



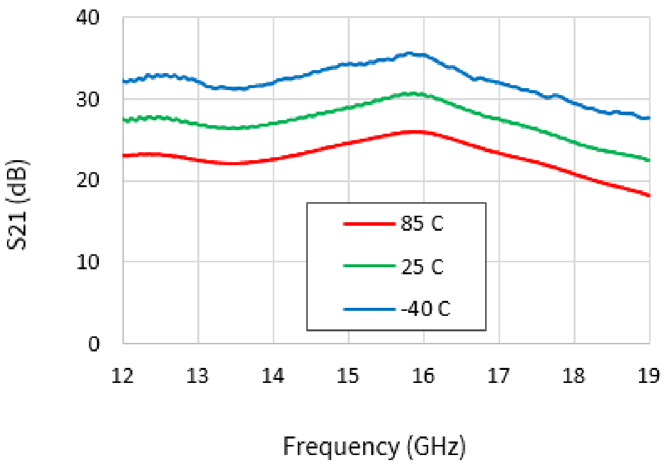
Large Signal Gain vs. Input Power



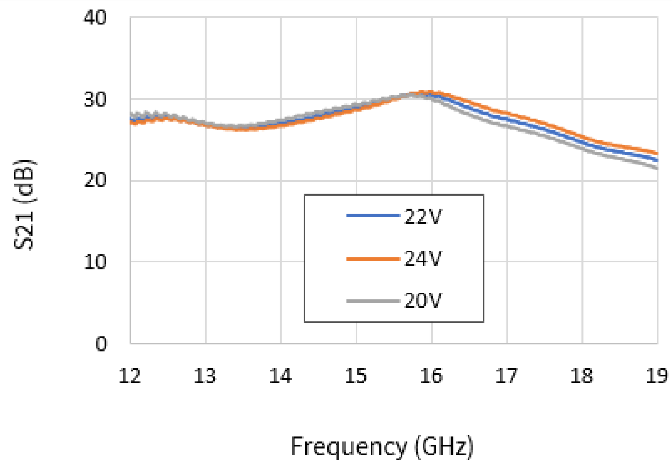
Typical Performance Curves - Small Signal over Temperature and V_D

I_{DQ} = 30 mA, CW, P_{IN} = -20 dBm

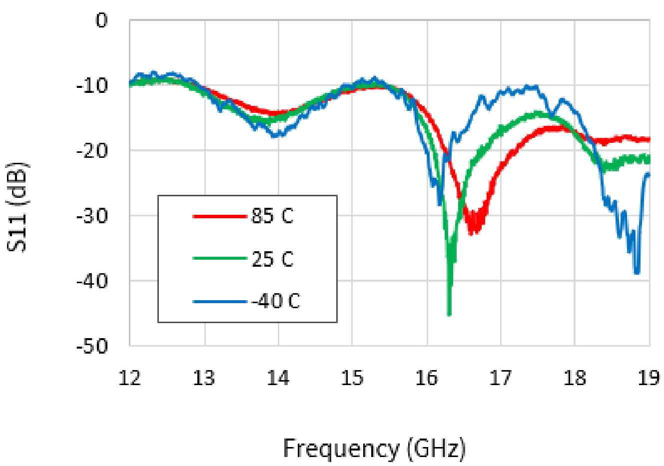
S21 vs. Frequency over Temperature @ V_D = 22 V



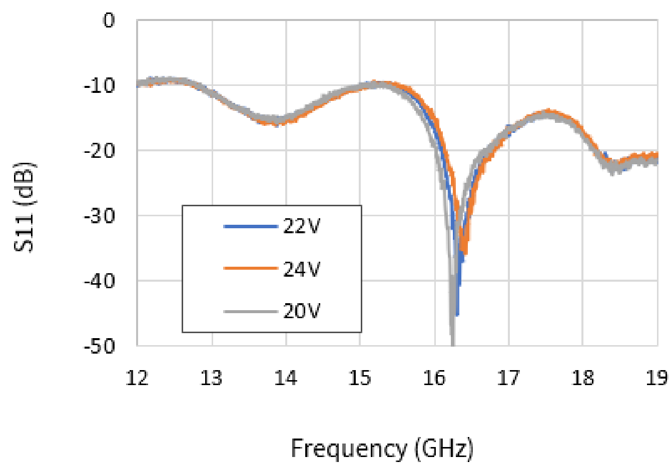
S21 vs. Frequency over V_D @ 25°C



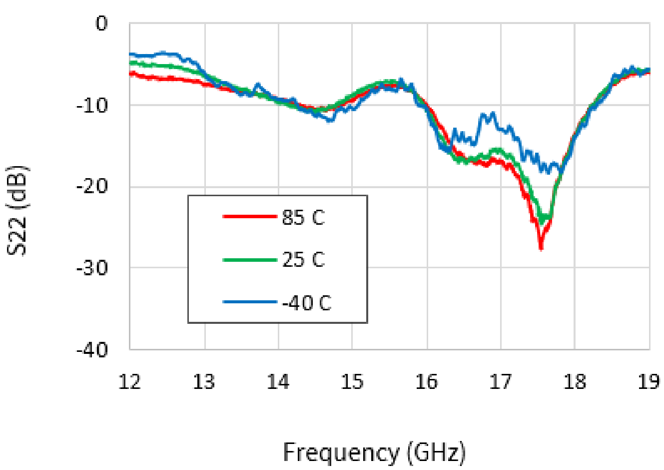
S11 vs. Frequency over Temperature @ V_D = 22 V



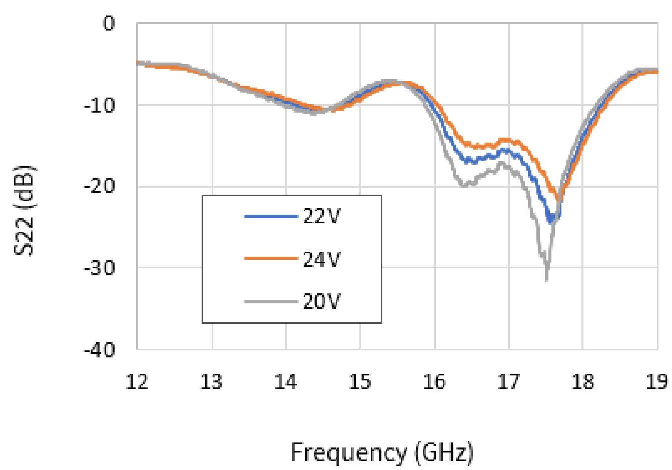
S11 vs. Frequency over V_D @ 25°C



S22 vs. Frequency over Temperature @ V_D = 22 V



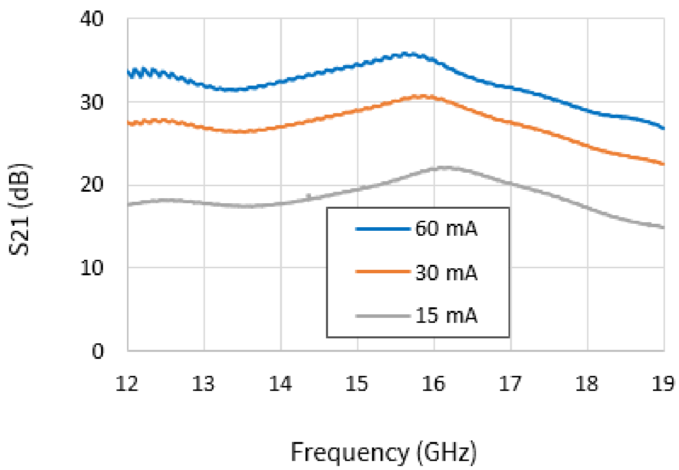
S22 vs. Frequency over V_D @ 25°C



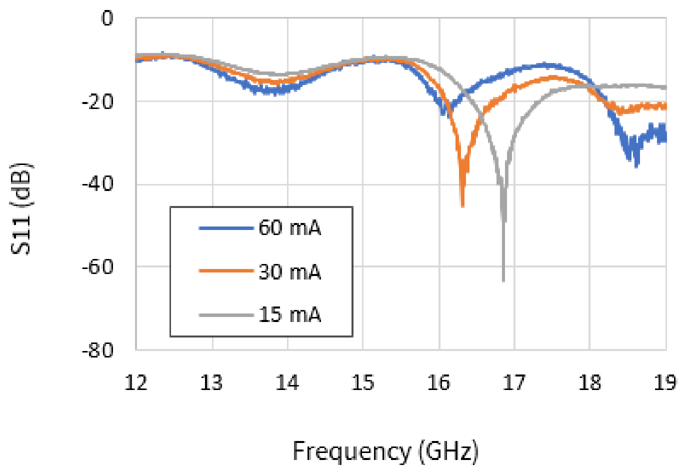
Typical Performance Curves - Small Signal over I_{DQ}

V_D = 22 V, CW, P_{IN} = -20 dBm, T_C = 25^{o}C

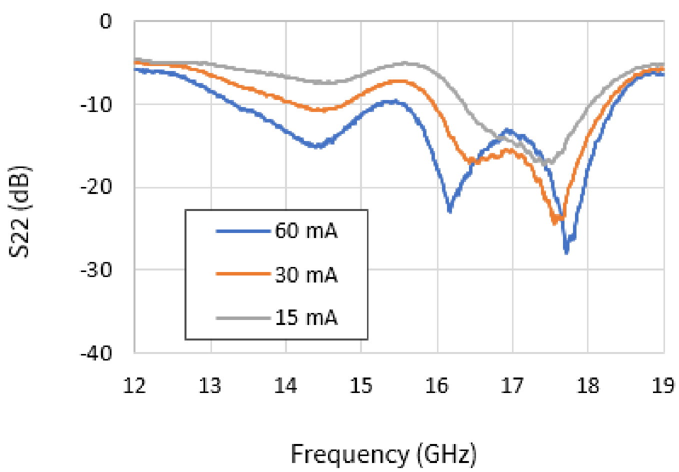
S21 vs. Frequency over I_{DQ}



S11 vs. Frequency over I_{DQ}



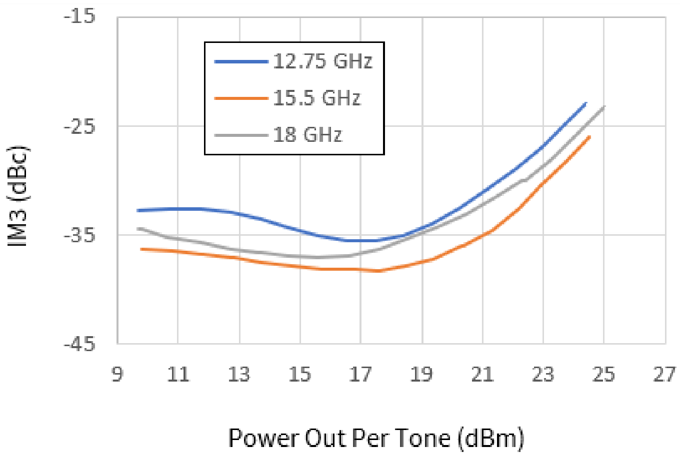
S22 vs. Frequency over I_{DQ}



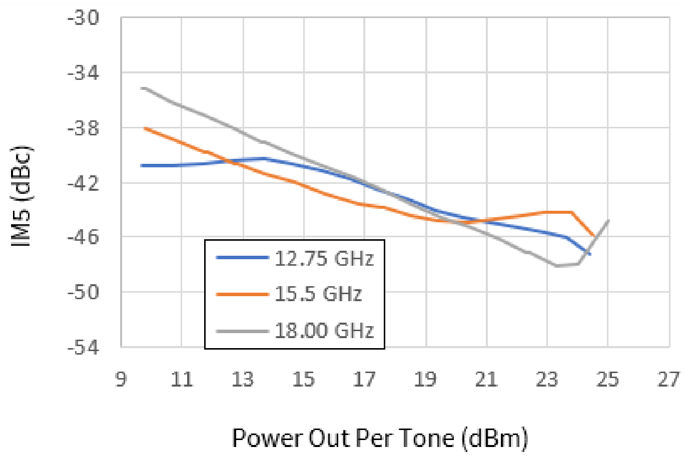
Typical Performance Curves - Linearity (IM3 and IM5)

V_D = 22 V, I_{DQ} = 30 mA, CW, Frequency = 15.5 GHz, Tone Spacing = 10 MHz, T_C = 25°C (unless otherwise stated)

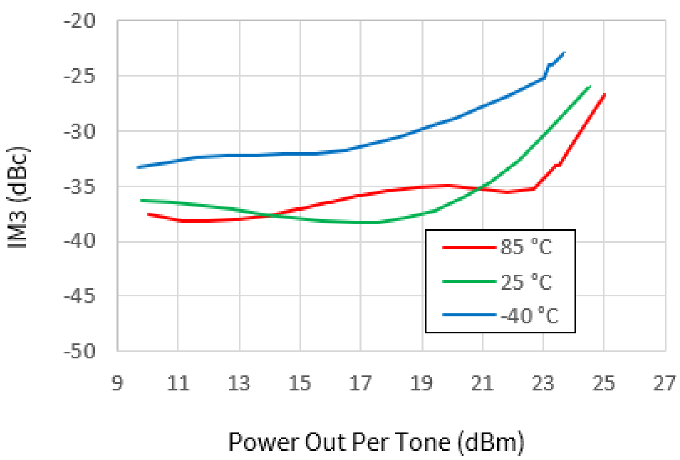
IM3 v. Output Power/Tone v. Frequency



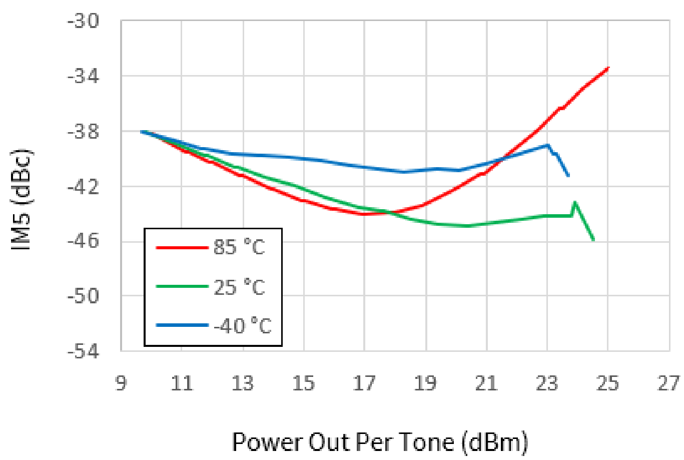
IM5 v. Output Power/Tone v. Frequency



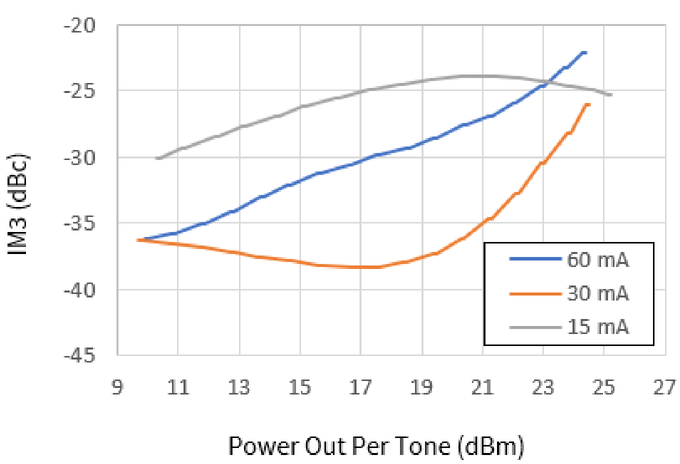
IM3 v. Output Power/Tone v. Temperature



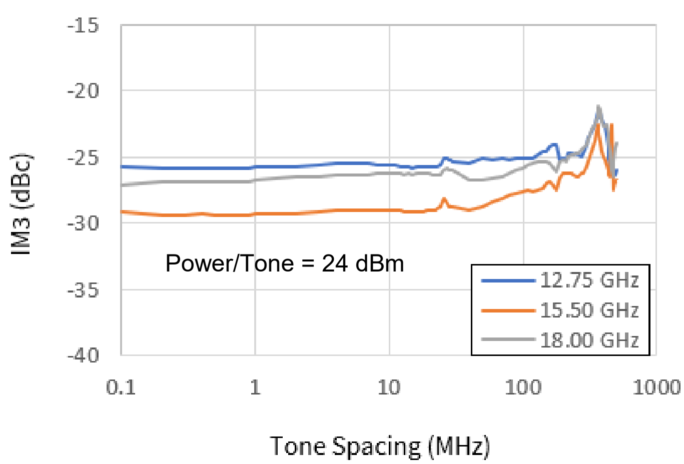
IM5 v. Output Power/Tone v. Temperature



IM3 v. Output Power/Tone v. I_{DQ}



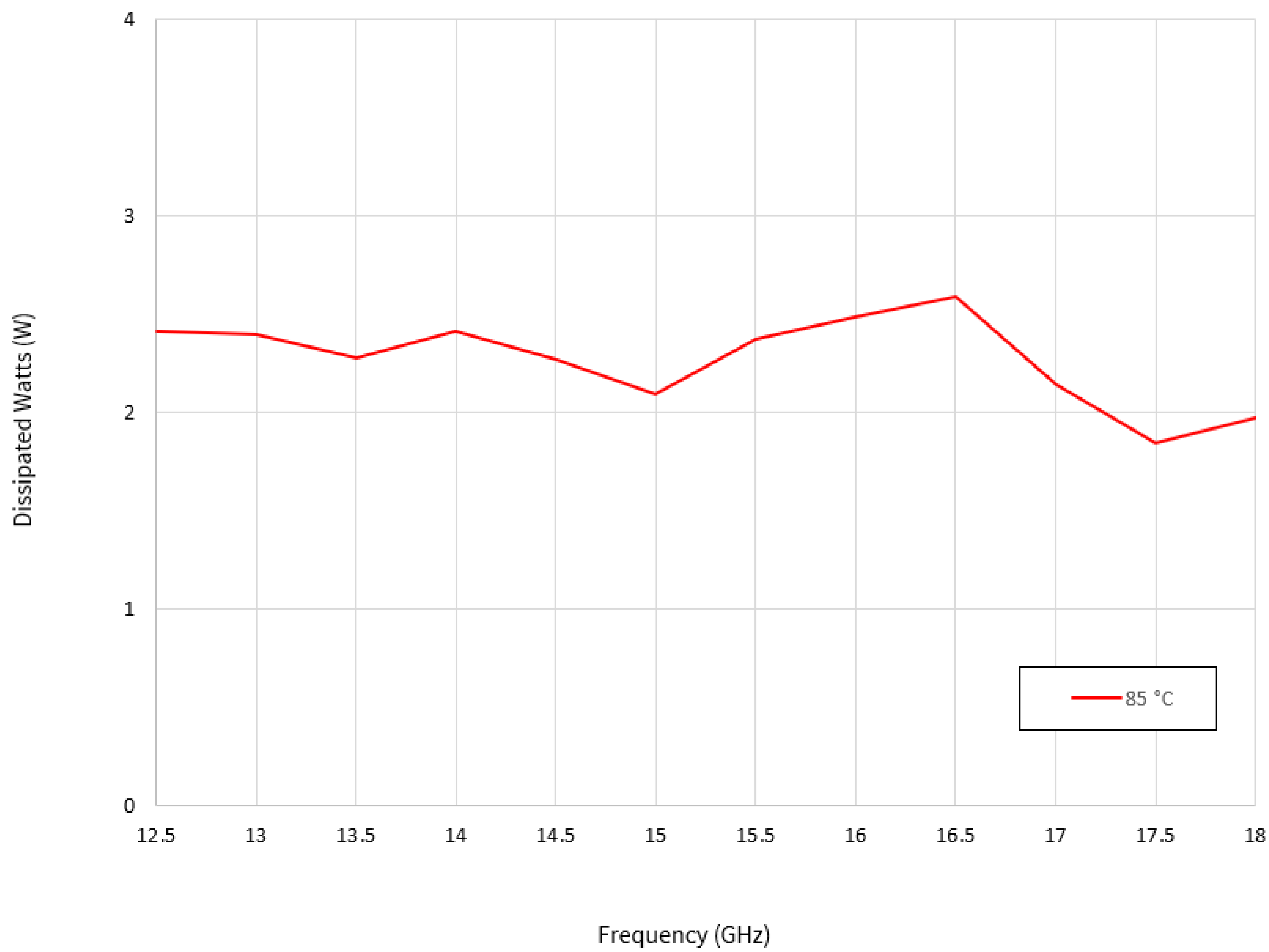
IM3 v. Tone Spacing v. Frequency



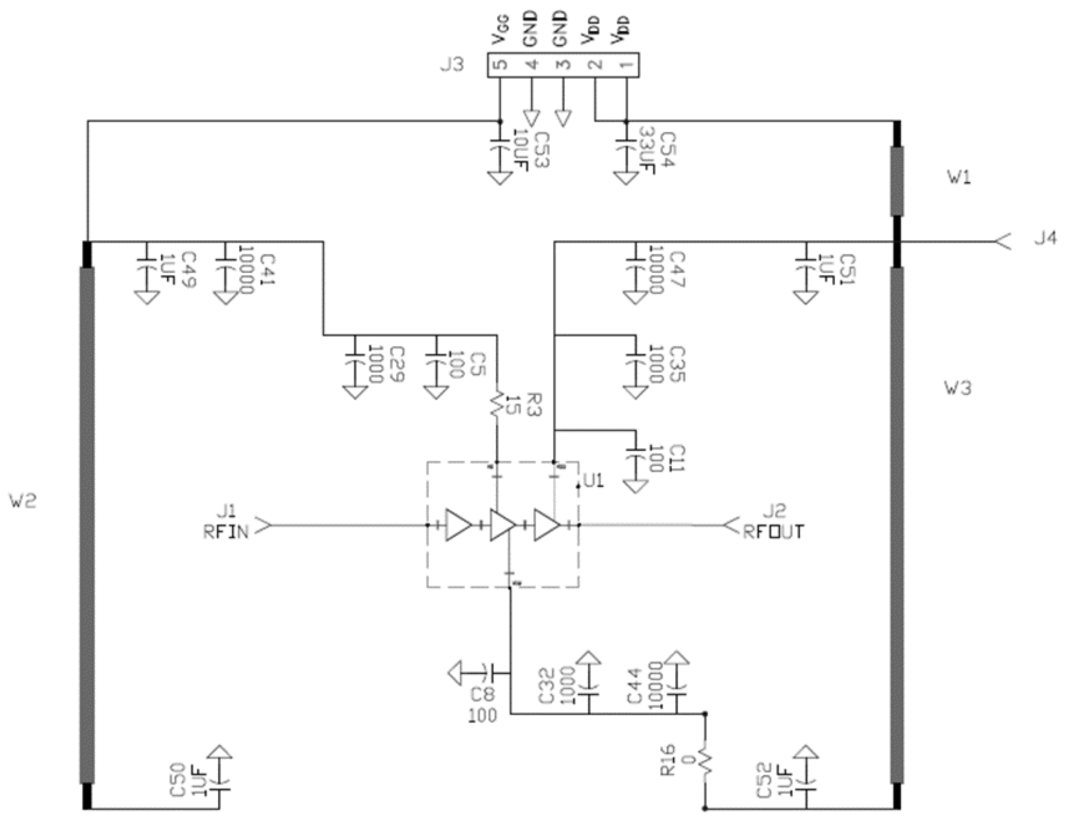
Thermal Characteristics

Parameter	Operating Conditions	Value
Operating Junction Temperature (T_J)	Freq = 15.5 GHz, V_D = 22 V, I_{DQ} = 30 mA, I_{DRIVE} = 190 mA , P_{IN} = 8 dBm, P_{OUT} = 31 dBm, P_{DISS} = 2.4 W, T_{CASE} = 85°C, CW	161.3ºC
Thermal Resistance, Junction to Case ($R_{\theta JC}$)		31.8ºC / W

Power Dissipation vs. Frequency (T_C = 85°C)



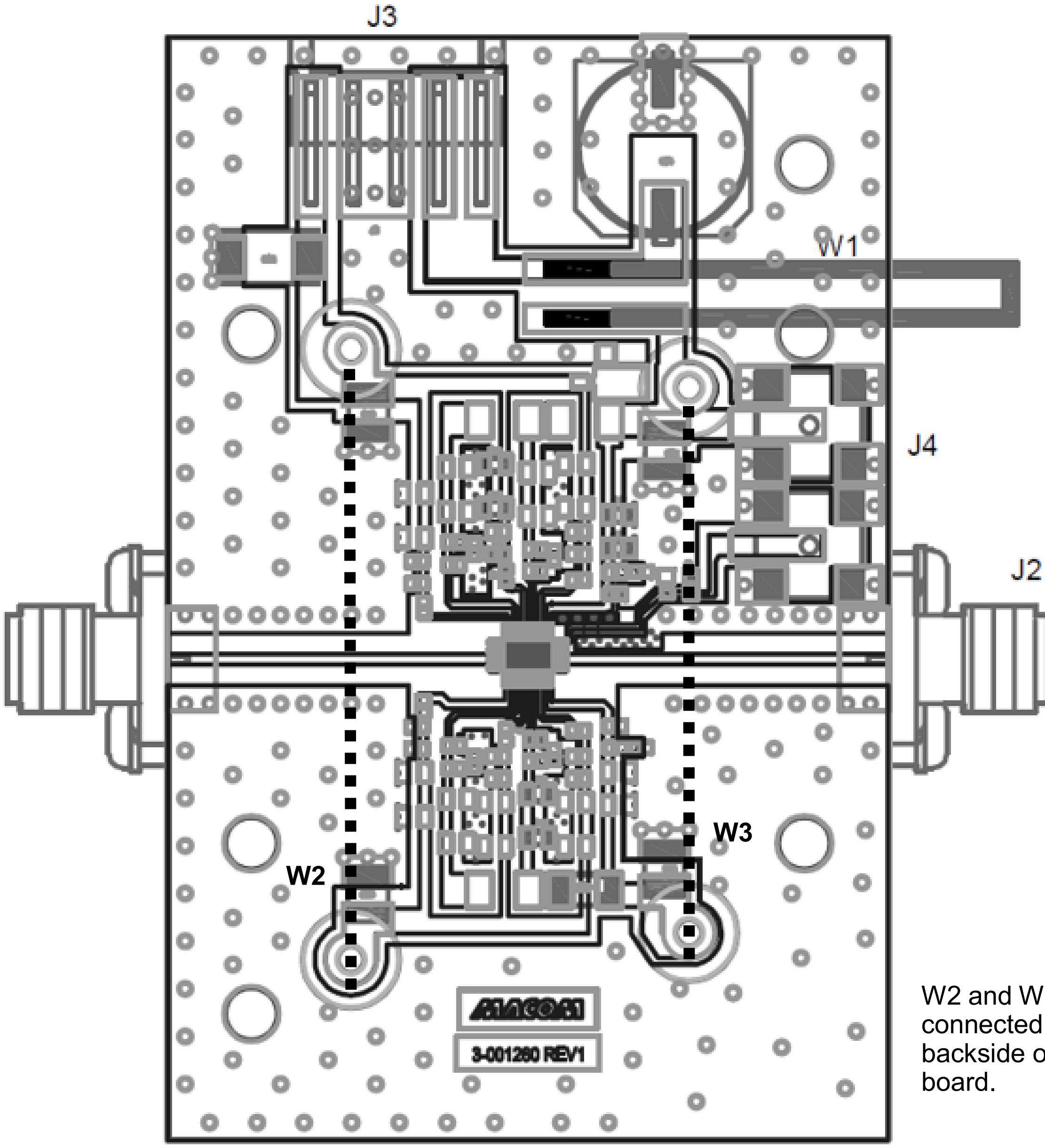
Evaluation Board Schematic (CMPA1D1J001S-AMP1)



Parts List

Part	Value	Qty.
C47, C41, C44	C0G, 10nF, +/-5%, 100V, 0603	3
C54	CAP, 33 UF, 20%, G CASE	1
C53	CAP, 10UF, 16V, TANTALUM	1
C11, C55, C5, C8	CAP, 100pF, +/-5%, 50V, 0402	4
R3	RES 15 OHM, +/-1%, 1/16W, 0402	1
C35, C29, C32	CAP, 1000PF, +/-5%, 100V, 0603	3
C49, C50, C51, C52	CAP, 1UF, 100V	4
R16	RES 0.0 OHM 1/16W 1206 SMD	1
-	PCB, RF-35, .010 THK, 3X4, 3-STAGE, QFN, CMPA1D1J001S	1
-	BASEPLATE 2.6”x1.7”x0.25” AL 3x4 QFN	1
-	2-56 SOC HD SCREW 3/16 SS	4
-	#2 SPLIT LOCKWASHER SS	4
J1, J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST, 20MIL	2
J4	CONN, SMB, STRAIGHT JACK RECEPTACLE, SMT, 50 OHM, Au PLATED	1
J3	HEADER RT>PLZ .1CEN LK 5POS	1
W2, W3	WIRE, BLACK, 20 AWG	1
W1	WIRE, BLACK, 22 AWG	3
U1	CMPA1D1J001S	1

Evaluation Board Assembly Drawing (CMPA1D1J001S-AMP1)



W2 and W3 are connected on the backside of the board.

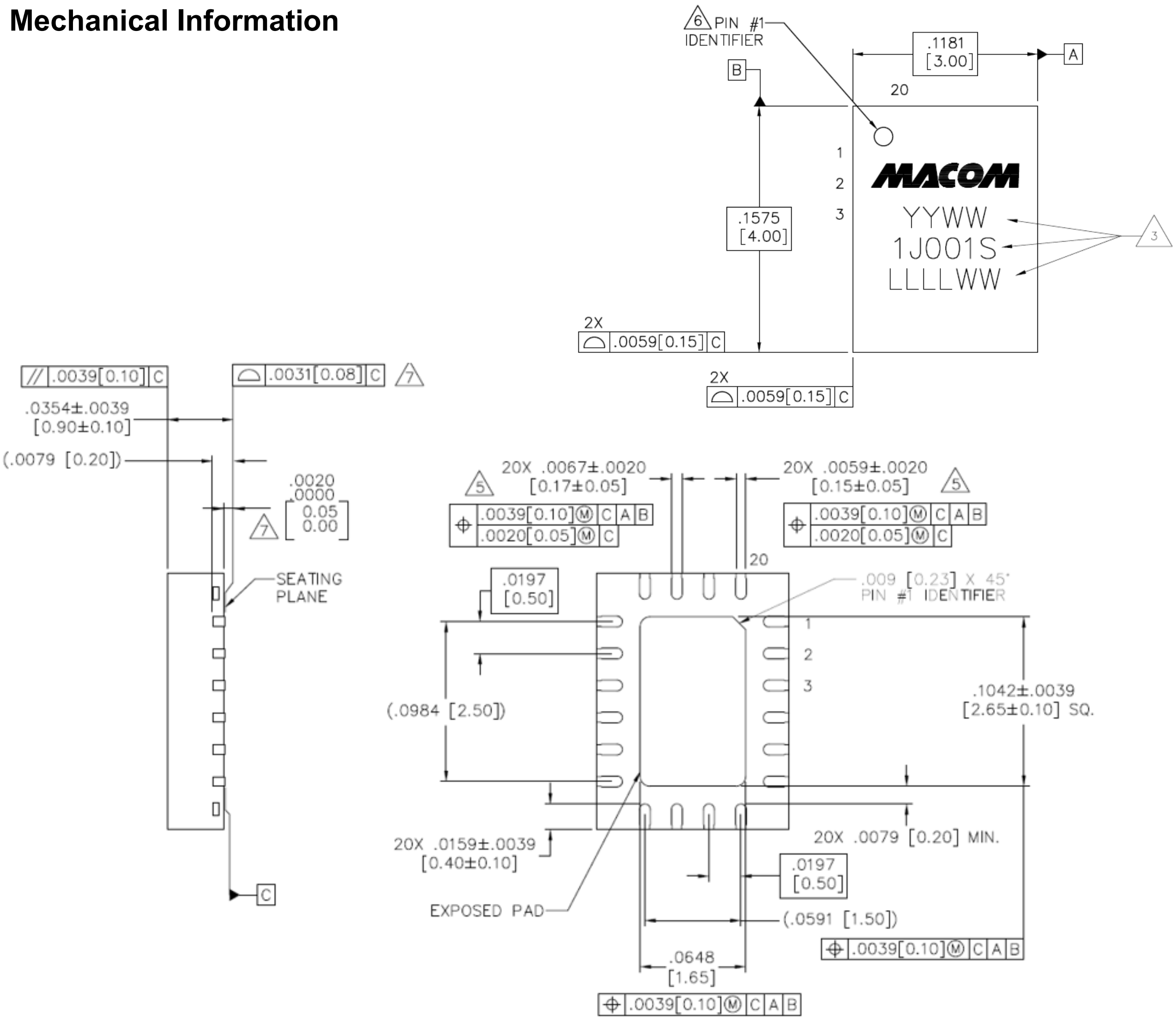
Bias On Sequence

1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (V_G)
3. Apply nominal drain voltage (V_D)
4. Adjust Vg to obtain desired quiescent drain current (I_{DQ})
5. Apply RF

Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate (V_G = -5 V)
3. Turn off drain voltage (V_D)
4. Turn off gate voltage (V_G)

Mechanical Information

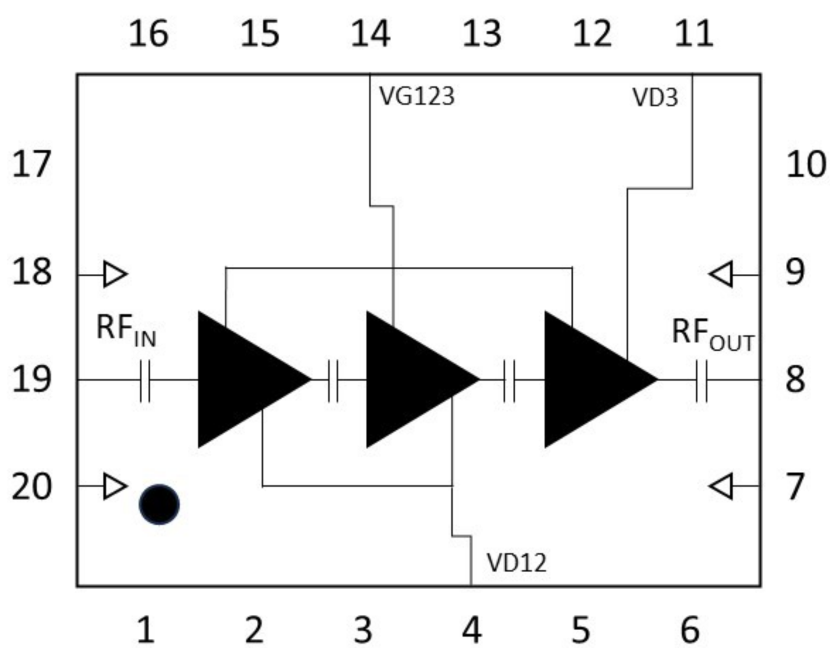


NOTES – UNLES OTHERWISE SPECIFIED:

1. ALL DIMENSIONS AND TOLERANCES ARE BASED ON JEDEC MO-220, VAR WITH SAW SINGULATION. ALL DIMENSIONS SHOWN AS in[mm]. CONTROLLING DIMENSIONS ARE IN mm AND CONVERTED in DIMENSIONS ARE NOT NECESSARILY EXACT.
2. LEAD FINISH: 100% MATTE TIN PLATE FOLLOWED BY A POST-PLATING ANNEALING OPERATION OF 1HR @150°C.
3. (△) MARKING: ALL MARKING SHALL BE PERMANENT AND LEGIBLE – AS SHOWN.
   LINE 1: DATE CODE SHALL CONSIST OF:
   A 2-DIGIT YEAR CODE FOLLOWED BY A 2-DIGIT WEEK CODE.
   LINE 2: PART NUMBER MARKING CODE (6 CHARACTERS MAX).
   LINE 3: LOT NUMBER SHALL CONSIST OF THE LAST 4 DIGITS OF THE U1 LOT NUMBER (LLLL) FOLLOWED BY 2-DIGITS WAFER NUMBER (WW).
4. ELECTROSTATIC DISCHARGE CONTROL PROGRAM FOR THE PROTECTION OF ELECTRICAL AND ELECTRONIC PARTS, ASSEMBLIES AND EQUIPMENT SHALL BE IN ACCORDANCE WITH ANSI/ESD 20.20.
5. (△) INDICATED DIMENSIONS/TOLERANCES APPLY TO THE PLATED LEAD AND IS MEASURED BETWEEN .0059[0.15] AND .0118[0.30] FROM THE LEAD END.
6. (△) EXACT SIZE AND SHAPE OF THIS FEATURE IS OPTIONAL.
7. (△) INDICATED DIMENSIONS/TOLERANCES APPLY TO LEADS AND EXPOSED PAD.
8. REFERENCE ASSEMBLY DRAWING DC-0034254 FOR ASSEMBLY INFORMATION.
9. ALL MATERIALS DESCRIBED IN THIS DOCUMENT/DRAWING SHALL BE IN COMPLIANCE WITH AND CONTAIN NO SUBSTANCES RESTRICTED OR REQUIRING SPECIAL RECLAMATION UNDER THE LATEST ROHS, WEEE OR ELV DIRECTIVES.

Pin Description

Pin #	Name	Description
1-3, 5, 6, 10, 12, 13, 15-17	NC	Recommended to connect NC pins to ground.
7, 9, 18, 20	GND	RF and DC ground
4	VD12	Drain bias for stages 1 and 2.
8	RF_{OUT}	RF Output. 50-ohm matched. Internally DC blocked.
11	VD3	Drain bias for stage 3.
14	VG123	Gate bias for stages 1, 2 and 3.
19	RF_{IN}	RF Input. 50-ohm matched. Internally DC blocked.
Paddle	GND	RF and DC ground



Revision History

Rev	Date	Change Description
V1	12/18/2024	Production release.