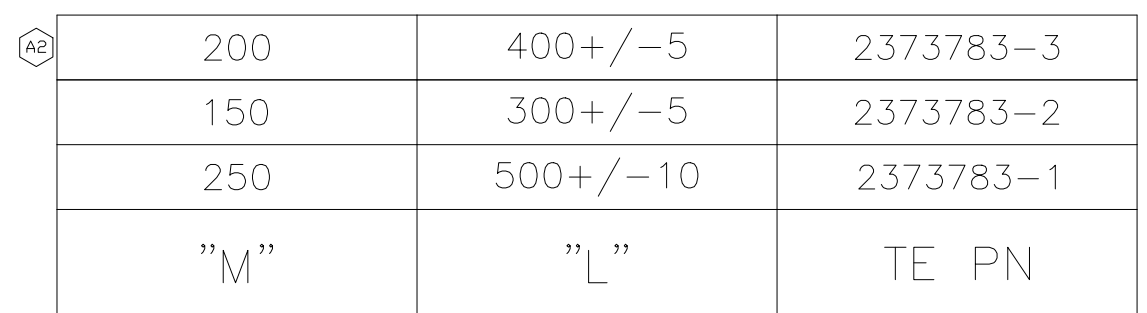




-  LABEL INFORMATION SHOWN BELOW:

8. SLIVER CABLE PLUG MATES WITH TERSEIVER P/N 2384218-X, OR 2369833-X.

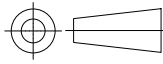
△ KEY CHARACTERISTIC PER STANDARD OPERATING PROCEDURE TEC-407-55.
APPLIES TO BOTH DIMENSION AND FEATURE CONTROL TOLERANCE.

THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN 15SEP2020 GARNETT WU CHK —		 TE Connectivity Ltd.	
DIMENSIONS: mm		TOLERANCES UNLESS OTHERWISE SPECIFIED: 0 PLC ± — 1 PLC ± — 2 PLC ± — 3 PLC ± — 4 PLC ± — ANGLES ± —		APVD 15SEP2020 DAVID ZHANG PRODUCT SPEC — APPLICATION SPEC —	
		WEIGHT —		NAME SLIVER 2.0 4C+ LEAD FRAME TO SLIVER 2.0 4C+ 30AWG 85OHM —	
MATERIAL —		FINISH —		SIZE CAGE CODE DRAWING NO RESTRICTED TO A2 00779 C=2373783 —	
CUSTOMER DRAWING				SCALE 1:1	SHEET 1 of 3
				REV A2	

P	LTR	DESCRIPTION	DATE	DWN	APVD
	—	SEE SHEET 1	—	—	—

P1		WIRE TYPE	P2	
PIN NUMBER	PIN DEFINE		PIN DEFINE	PIN NUMBER
OA1	RST_OCP_V3_1_A_2_N		RST_OCP_V3_1_A_2_N	OA1
OA2	RST_OCP_V3_1_A_3_N		RST_OCP_V3_1_A_3_N	OA2
OA3	OCP_V3_1_WAKE_N		OCP_V3_1_WAKE_N	OA3
OA4	OCP_V3_1_ISO_RBT_ARB_IN		OCP_V3_1_ISO_RBT_ARB_IN	OA4
OA5	OCP_V3_1_ISO_RBT_ARB_OUT		OCP_V3_1_ISO_RBT_ARB_OUT	OA5
OA6	OCP_V3_1_SLOT_ID1		OCP_V3_1_SLOT_ID1	OA6
OA7	NCSI_OCP_V3_1_ISO_TX_EN		NCSI_OCP_V3_1_ISO_TX_EN	OA7
OA8	NCSI_OCP_V3_1_ISO_TXD1		NCSI_OCP_V3_1_ISO_TXD1	OA8
OA9	NCSI_OCP_V3_1_ISO_TXD0		NCSI_OCP_V3_1_ISO_TXD0	OA9
OA10	GND		GND	OA10
OA11	CLK_100M_DB2001_OCP_V3_1_B_DN		CLK_100M_DB2001_OCP_V3_1_B_DN	OA11
OA12	CLK_100M_DB2001_OCP_V3_1_B_DP		CLK_100M_DB2001_OCP_V3_1_B_DP	OA12
OA13	GND		GND	OA13
OA14	CLK_50M_OCP_V3_1_ISO_RBT_REF		CLK_50M_OCP_V3_1_ISO_RBT_REF	OA14
	KEY		KEY	
A1	GND		GND	A1
A2	GND		GND	A2
A3	GND		GND	A3
A4	GND		GND	A4
A5	GND		GND	A5
A6	GND		GND	A6
A7	SMB_BMC_OCP_V3_1_A_SCL		SMB_BMC_OCP_V3_1_A_SCL	A7
A8	SMB_BMC_OCP_V3_1_A_SDA		SMB_BMC_OCP_V3_1_A_SDA	A8
A9	SMB_BMC_OCP_V3_1_A_RST_N		SMB_BMC_OCP_V3_1_A_RST_N	A9
A10	PRSN TA #		PRSN TA #	A10
A11	RST_OCP_V3_1_A_1_N		RST_OCP_V3_1_A_1_N	A11
A12	OCP_V3_1_PRSN T B2_N		OCP_V3_1_PRSN T B2_N	A12
A13	GND		GND	A13
A14	CLK_100M_DB2001_OCP_V3_1_D_DN		CLK_100M_DB2001_OCP_V3_1_D_DN	A14
A15	CLK_100M_DB2001_OCP_V3_1_D_DP		CLK_100M_DB2001_OCP_V3_1_D_DP	A15
A16	GND		GND	A16
A17	P3E_CPU0_PCIE3_RX_DP<0>		P3E_CPU0_PCIE3_RX_DP<0>	A17
A18	P3E_CPU0_PCIE3_RX_DN<0>		P3E_CPU0_PCIE3_RX_DN<0>	A18
A19	GND		GND	A19
A20	P3E_CPU0_PCIE3_RX_DP<1>		P3E_CPU0_PCIE3_RX_DP<1>	A20
A21	P3E_CPU0_PCIE3_RX_DN<1>		P3E_CPU0_PCIE3_RX_DN<1>	A21
A22	GND		GND	A22
A23	P3E_CPU0_PCIE3_RX_DP<2>		P3E_CPU0_PCIE3_RX_DP<2>	A23
A24	P3E_CPU0_PCIE3_RX_DN<2>		P3E_CPU0_PCIE3_RX_DN<2>	A24
A25	GND		GND	A25
A26	P3E_CPU0_PCIE3_RX_DP<3>		P3E_CPU0_PCIE3_RX_DP<3>	A26
A27	P3E_CPU0_PCIE3_RX_DN<3>		P3E_CPU0_PCIE3_RX_DN<3>	A27
A28	GND		GND	A28
	KEY		KEY	
A29	GND		GND	A29
A30	P3E_CPU0_PCIE3_RX_DP<4>		P3E_CPU0_PCIE3_RX_DP<4>	A30
A31	P3E_CPU0_PCIE3_RX_DN<4>		P3E_CPU0_PCIE3_RX_DN<4>	A31
A32	GND		GND	A32
A33	P3E_CPU0_PCIE3_RX_DP<5>		P3E_CPU0_PCIE3_RX_DP<5>	A33
A34	P3E_CPU0_PCIE3_RX_DN<5>		P3E_CPU0_PCIE3_RX_DN<5>	A34
A35	GND		GND	A35
A36	P3E_CPU0_PCIE3_RX_DP<6>		P3E_CPU0_PCIE3_RX_DP<6>	A36
A37	P3E_CPU0_PCIE3_RX_DN<6>		P3E_CPU0_PCIE3_RX_DN<6>	A37
A38	GND		GND	A38
A39	P3E_CPU0_PCIE3_RX_DP<7>		P3E_CPU0_PCIE3_RX_DP<7>	A39
A40	P3E_CPU0_PCIE3_RX_DN<7>		P3E_CPU0_PCIE3_RX_DN<7>	A40
A41	GND		GND	A41
A42	OCP_V3_1_PRSN T B1_N		OCP_V3_1_PRSN T B1_N	A42
	KEY		KEY	
A43	GND		GND	A43
A44	P3E_CPU0_PCIE3_RX_DP<8>		P3E_CPU0_PCIE3_RX_DP<8>	A44
A45	P3E_CPU0_PCIE3_RX_DN<8>		P3E_CPU0_PCIE3_RX_DN<8>	A45
A46	GND		GND	A46
A47	P3E_CPU0_PCIE3_RX_DP<9>		P3E_CPU0_PCIE3_RX_DP<9>	A47
A48	P3E_CPU0_PCIE3_RX_DN<9>		P3E_CPU0_PCIE3_RX_DN<9>	A48
A49	GND		GND	A49
A50	P3E_CPU0_PCIE3_RX_DP<10>		P3E_CPU0_PCIE3_RX_DP<10>	A50
A51	P3E_CPU0_PCIE3_RX_DN<10>		P3E_CPU0_PCIE3_RX_DN<10>	A51
A52	GND		GND	A52
A53	P3E_CPU0_PCIE3_RX_DP<11>		P3E_CPU0_PCIE3_RX_DP<11>	A53
A54	P3E_CPU0_PCIE3_RX_DN<11>		P3E_CPU0_PCIE3_RX_DN<11>	A54
A55	GND		GND	A55
A56	P3E_CPU0_PCIE3_RX_DP<12>		P3E_CPU0_PCIE3_RX_DP<12>	A56
A57	P3E_CPU0_PCIE3_RX_DN<12>		P3E_CPU0_PCIE3_RX_DN<12>	A57
A58	GND		GND	A58
A59	P3E_CPU0_PCIE3_RX_DP<13>		P3E_CPU0_PCIE3_RX_DP<13>	A59
A60	P3E_CPU0_PCIE3_RX_DN<13>		P3E_CPU0_PCIE3_RX_DN<13>	A60
A61	GND		GND	A61
A62	P3E_CPU0_PCIE3_RX_DP<14>		P3E_CPU0_PCIE3_RX_DP<14>	A62
A63	P3E_CPU0_PCIE3_RX_DN<14>		P3E_CPU0_PCIE3_RX_DN<14>	A63
A64	GND		GND	A64
A65	P3E_CPU0_PCIE3_RX_DP<15>		P3E_CPU0_PCIE3_RX_DP<15>	A65
A66	P3E_CPU0_PCIE3_RX_DN<15>		P3E_CPU0_PCIE3_RX_DN<15>	A66
A67	GND		GND	A67
A68	USB2_OCP_1_DN		USB2_OCP_1_DN	A68
A69	USB2_OCP_1_DP		USB2_OCP_1_DP	A69
A70	OCP_V3_1_PWRBRK_N		OCP_V3_1_PWRBRK_N	A70

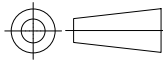
WIRE DIAGRAM

THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN GARNETT_WU	15SEP2020	 TE Connectivity Ltd.	
		CHK —	—		
DIMENSIONS: mm		APVD DAVID_ZHANG	15SEP2020	NAME SLIVER 2.0 4C+ LEAD FRAME TO SLIVER 2.0 4C+ 30AWG 850HM	
		PRODUCT SPEC —		APPLICATION SPEC —	
		TOLERANCES UNLESS OTHERWISE SPECIFIED: 0 PLC ± — 1 PLC ± — 2 PLC ± — 3 PLC ± — 4 PLC ± — ANGLES ± ± —		SIZE A2	
MATERIAL —		FINISH —		CAGE CODE 00779	DRAWING NO G=2373783
		WEIGHT —		RESTRICTED TO —	
		CUSTOMER DRAWING		SCALE 1:1	SHEET 2 of 3
				REV A2	

P	LTR	DESCRIPTION	DATE	DWN	APVD
	—	SEE SHEET 1	—	—	—

P1		WIRE TYPE	P2	
PIN NUMBER	PIN DEFINE		PIN DEFINE	PIN NUMBER
OB1	OCP_V3_1_NIC_PWR_GOOD		OCP_V3_1_NIC_PWR_GOOD	OB1
OB2	OCP_V3_1_MAIN_PWR_R_EN		OCP_V3_1_MAIN_PWR_R_EN	OB2
OB3	SGPIO_OCP_V3_1_LD_N		SGPIO_OCP_V3_1_LD_N	OB3
OB4	SGPIO_OCP_V3_1_DATA_IN		SGPIO_OCP_V3_1_DATA_IN	OB4
OB5	SGPIO_OCP_V3_1_DATA_OUT		SGPIO_OCP_V3_1_DATA_OUT	OB5
OB6	SGPIO_OCP_V3_1_CLK		SGPIO_OCP_V3_1_CLK	OB6
OB7	OCP_V3_1_SLOT_ID0		OCP_V3_1_SLOT_ID0	OB7
OB8	NCSI_OCP_V3_1_ISO_RXD1		NCSI_OCP_V3_1_ISO_RXD1	OB8
OB9	NCSI_OCP_V3_1_ISO_RXD0		NCSI_OCP_V3_1_ISO_RXD0	OB9
OB10	GND		GND	OB10
OB11	CLK_100M_DB2001_OCP_V3_1_A_DN		CLK_100M_DB2001_OCP_V3_1_A_DN	OB11
OB12	CLK_100M_DB2001_OCP_V3_1_A_DP		CLK_100M_DB2001_OCP_V3_1_A_DP	OB12
OB13	GND		GND	OB13
OB14	NCSI_OCP_V3_1_CR_S_R_DV		NCSI_OCP_V3_1_CR_S_R_DV	OB14
	KEY		KEY	
B1	P12V_OCP_V3_1		P12V_OCP_V3_1	B1
B2	P12V_OCP_V3_1		P12V_OCP_V3_1	B2
B3	P12V_OCP_V3_1		P12V_OCP_V3_1	B3
B4	P12V_OCP_V3_1		P12V_OCP_V3_1	B4
B5	P12V_OCP_V3_1		P12V_OCP_V3_1	B5
B6	P12V_OCP_V3_1		P12V_OCP_V3_1	B6
B7	OCP_V3_1_ISO_BIF0_N		OCP_V3_1_ISO_BIF0_N	B7
B8	OCP_V3_1_ISO_BIF1_N		OCP_V3_1_ISO_BIF1_N	B8
B9	OCP_V3_1_ISO_BIF2_N		OCP_V3_1_ISO_BIF2_N	B9
B10	RST_OCP_V3_1_A_0_N		RST_OCP_V3_1_A_0_N	B10
B11	P3V3_OCP_V3_1		P3V3_OCP_V3_1	B11
B12	OCP_V3_1_A_AUX_PWR_EN		OCP_V3_1_A_AUX_PWR_EN	B12
B13	GND		GND	B13
B14	CLK_100M_DB2001_OCP_V3_1_C_DN		CLK_100M_DB2001_OCP_V3_1_C_DN	B14
B15	CLK_100M_DB2001_OCP_V3_1_C_DP		CLK_100M_DB2001_OCP_V3_1_C_DP	B15
B16	GND		GND	B16
B17	P3E_CPU0_PCIE3_TX_C_DP<0>		P3E_CPU0_PCIE3_TX_C_DP<0>	B17
B18	P3E_CPU0_PCIE3_TX_C_DN<0>		P3E_CPU0_PCIE3_TX_C_DN<0>	B18
B19	GND		GND	B19
B20	P3E_CPU0_PCIE3_TX_C_DN<1>		P3E_CPU0_PCIE3_TX_C_DN<1>	B20
B21	P3E_CPU0_PCIE3_TX_C_DP<1>		P3E_CPU0_PCIE3_TX_C_DP<1>	B21
B22	GND		GND	B22
B23	P3E_CPU0_PCIE3_TX_C_DN<2>		P3E_CPU0_PCIE3_TX_C_DN<2>	B23
B24	P3E_CPU0_PCIE3_TX_C_DP<2>		P3E_CPU0_PCIE3_TX_C_DP<2>	B24
B25	GND		GND	B25
B26	P3E_CPU0_PCIE3_TX_C_DP<3>		P3E_CPU0_PCIE3_TX_C_DP<3>	B26
B27	P3E_CPU0_PCIE3_TX_C_DN<3>		P3E_CPU0_PCIE3_TX_C_DN<3>	B27
B28	GND		GND	B28
B29	GND		GND	B29
B30	P3E_CPU0_PCIE3_TX_C_DP<4>		P3E_CPU0_PCIE3_TX_C_DP<4>	B30
B31	P3E_CPU0_PCIE3_TX_C_DN<4>		P3E_CPU0_PCIE3_TX_C_DN<4>	B31
B32	GND		GND	B32
B33	P3E_CPU0_PCIE3_TX_C_DP<5>		P3E_CPU0_PCIE3_TX_C_DP<5>	B33
B34	P3E_CPU0_PCIE3_TX_C_DN<5>		P3E_CPU0_PCIE3_TX_C_DN<5>	B34
B35	GND		GND	B35
B36	P3E_CPU0_PCIE3_TX_C_DP<6>		P3E_CPU0_PCIE3_TX_C_DP<6>	B36
B37	P3E_CPU0_PCIE3_TX_C_DN<6>		P3E_CPU0_PCIE3_TX_C_DN<6>	B37
B38	GND		GND	B38
B39	P3E_CPU0_PCIE3_TX_C_DN<7>		P3E_CPU0_PCIE3_TX_C_DN<7>	B39
B40	P3E_CPU0_PCIE3_TX_C_DP<7>		P3E_CPU0_PCIE3_TX_C_DP<7>	B40
B41	GND		GND	B41
B42	OCP_V3_1_PR_SNTB0_N		OCP_V3_1_PR_SNTB0_N	B42
B43	GND		GND	B43
B44	P3E_CPU0_PCIE3_TX_C_DP<8>		P3E_CPU0_PCIE3_TX_C_DP<8>	B44
B45	P3E_CPU0_PCIE3_TX_C_DN<8>		P3E_CPU0_PCIE3_TX_C_DN<8>	B45
B46	GND		GND	B46
B47	P3E_CPU0_PCIE3_TX_C_DN<9>		P3E_CPU0_PCIE3_TX_C_DN<9>	B47
B48	P3E_CPU0_PCIE3_TX_C_DP<9>		P3E_CPU0_PCIE3_TX_C_DP<9>	B48
B49	GND		GND	B49
B50	P3E_CPU0_PCIE3_TX_C_DN<10>		P3E_CPU0_PCIE3_TX_C_DN<10>	B50
B51	P3E_CPU0_PCIE3_TX_C_DP<10>		P3E_CPU0_PCIE3_TX_C_DP<10>	B51
B52	GND		GND	B52
B53	P3E_CPU0_PCIE3_TX_C_DP<11>		P3E_CPU0_PCIE3_TX_C_DP<11>	B53
B54	P3E_CPU0_PCIE3_TX_C_DN<11>		P3E_CPU0_PCIE3_TX_C_DN<11>	B54
B55	GND		GND	B55
B56	P3E_CPU0_PCIE3_TX_C_DP<12>		P3E_CPU0_PCIE3_TX_C_DP<12>	B56
B57	P3E_CPU0_PCIE3_TX_C_DN<12>		P3E_CPU0_PCIE3_TX_C_DN<12>	B57
B58	GND		GND	B58
B59	P3E_CPU0_PCIE3_TX_C_DN<13>		P3E_CPU0_PCIE3_TX_C_DN<13>	B59
B60	P3E_CPU0_PCIE3_TX_C_DP<13>		P3E_CPU0_PCIE3_TX_C_DP<13>	B60
B61	GND		GND	B61
B62	P3E_CPU0_PCIE3_TX_C_DP<14>		P3E_CPU0_PCIE3_TX_C_DP<14>	B62
B63	P3E_CPU0_PCIE3_TX_C_DN<14>		P3E_CPU0_PCIE3_TX_C_DN<14>	B63
B64	GND		GND	B64
B65	P3E_CPU0_PCIE3_TX_C_DN<15>		P3E_CPU0_PCIE3_TX_C_DN<15>	B65
B66	P3E_CPU0_PCIE3_TX_C_DP<15>		P3E_CPU0_PCIE3_TX_C_DP<15>	B66
B67	GND		GND	B67
B68	TP_OCP_V3_1_RFU_1		TP_OCP_V3_1_RFU_1	B68
B69	TP_OCP_V3_1_RFU_2		TP_OCP_V3_1_RFU_2	B69
B70	OCP_V3_1_PR_SNTB3_N		OCP_V3_1_PR_SNTB3_N	B70

WIRE DIAGRAM

THIS DRAWING IS A CONTROLLED DOCUMENT.		DWN GARNETT WU 15SEP2020	 TE Connectivity Ltd.		
DIMENSIONS: mm		CHK —			
	TOLERANCES UNLESS OTHERWISE SPECIFIED: 0 PLC ± — 1 PLC ± — 2 PLC ± — 3 PLC ± — 4 PLC ± — ANGLES ± —	APVD DAVID ZHANG 15SEP2020	NAME SLIVER 2.0 4C+ LEAD FRAME TO SLIVER 2.0 4C+ 30AWG 850HM		
		PRODUCT SPEC —	APPLICATION SPEC —		
MATERIAL —	FINISH —	WEIGHT —	SIZE A2	CAGE CODE 00779	DRAWING NO G=2373783
CUSTOMER DRAWING			SCALE 1:1	SHEET 3 of 3	REV A2