PE64102

Document category: Product Specification

UltraCMOS® Digitally Tunable Capacitor (DTC), 100–3000 MHz

Features

- 3-wire (SPI-compatible) 8-bit serial interface with built-in bias voltage generation and standby mode for reduced power consumption
- DuNE™-enhanced UltraCMOS® device
- 5-bit 32-state digitally tunable capacitor
- C = 1.88–14.0 pF (7.4:1 tuning ratio) in discrete 391-fF steps
- RF power handing (up to 26 dBm, 6 V_{PK} RF) and high linearity
- High quality factor
- Wide power supply range (2.3–3.6V) and low current consumption (typ. I_{DD} = 30 µA @ 2.8V)
- Optimized for shunt configuration, but can also be used in series configuration
- Excellent 2 kV HBM ESD tolerance on all pins
- Packaging: 12-lead 2 × 2 × 0.55 mm QFN

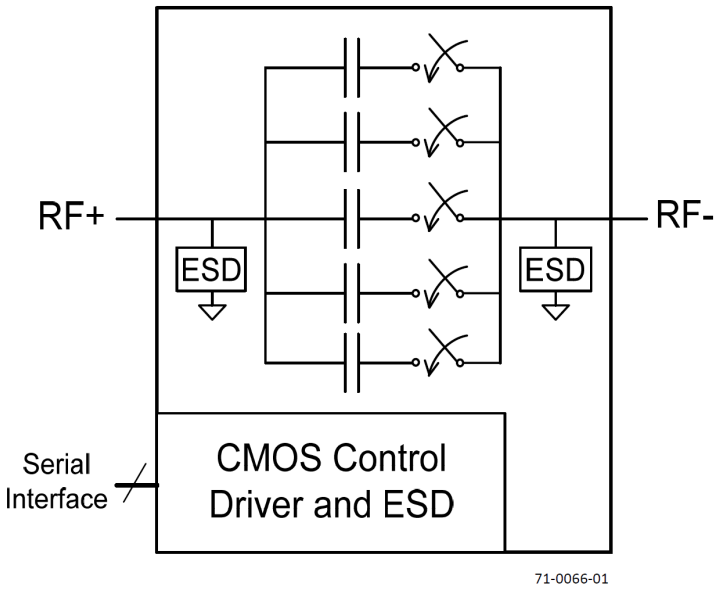


Figure 1. PE64102 functional diagram

Applications

- Antenna tuning
- Tunable filters
- Phase shifters
- Impedance matching

Product description

The PE64102 is a DuNE™-enhanced digitally tunable capacitor (DTC) based on pSemi's UltraCMOS® technology. DTC products provide a monolithically integrated impedance tuning solution for demanding RF applications. They also offer a linear capacitance change versus tuning state and excellent harmonic performance compared to varactor-based tunable solutions.

This highly versatile product can be mounted in series or shunt configurations and uses a 3-wire (SPI-compatible) serial interface. It has a high ESD rating of 2 kV HBM on all ports, making this the ultimate in integration and ruggedness. The DTC is offered in a standard 12-lead 2.0 × 2.0 × 0.55 mm QFN commercial package.

pSemi's DuNE™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS® process.

Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. PE64102 absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Power supply voltage	V_{DD}	-0.3	4.0	V
Voltage on any DC input	V_I	-0.3	4.0	V
ESD voltage HBM, all pins(1)	$V_{ESD,HBM}$	–	2000	V
ESD voltage MM, all pins(2)	$V_{ESD,MM}$	–	100	V
ESD voltage CDM, all pins(3)	$V_{ESD,CDM}$	–	250	V

1. Human body model (MIL–STD 883 Method 3015.7).
2. Machine model (JEDEC JESD22-A115-A).
3. Charged device model (JEDEC JESD22–C101).

Recommended operating conditions

Table 2 lists the PE64102 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. PE64102 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.3	2.8	3.6	V
Power supply current, normal mode(1)	I_{DD}	–	30	75	µA
Power supply current, standby mode(1)(2)	I_{DD}	–	20	45	µA
Control voltage high	V_{IH}	1.2	–	3.1	V
Control voltage low	V_{IL}	0	–	0.2	V
Peak operating RF voltage:(3) - V_P to V_M - V_P to RFGND - V_M to RFGND	–	–	–	 6 6 6	V_{PK}
RF input power (50Ω):(3)(4)(5) - Shunt - Series	–	–	–	 +26 +20	dBm
Input control current	I_{CTL}	–	1	10	µA
Operating temperature range	T_{OP}	-40	–	+85	°C
Storage temperature range	T_{ST}	-65	–	+150	°C

1. The I_{DD} current typical value is based on V_{DD} = 2.8V. The maximum I_{DD} is based on V_{DD} = 3.6V.
2. The DTC is active when STBY is low (set to 0), and in low-current standby mode when high (set to 1).
3. RF+ to RF- and RF+ or RF- to ground. Cannot exceed 6 V_{PK} or the maximum RF input power, whichever occurs first.
4. Maximum CW power available from a 50Ω source in shunt configuration.
5. Maximum CW power available from a 50Ω source in series configuration.

Electrical specifications

Table 3 lists the PE64102 key electrical specifications at +25 °C and V_{DD} = 2.8V, unless otherwise specified.

Table 3. PE64102 electrical specifications

Parameter	Config.	Condition	Min	Typ	Max	Unit
Operating frequency(1)	Both	–	100	–	3000	MHz
Minimum capacitance	Shunt(2)	State = 00000, 100 MHz (RF+ to grounded RF-)	-10%	1.88	+10%	pF
Maximum capacitance	Shunt(2)	State = 11111, 100 MHz (RF+ to grounded RF-)	-20%	14.0	+20%	pF
Tuning ratio	Shunt(2)	C_{max}/C_{min}, 100 MHz	–	7.4:1	–	–
Step size	Shunt(2)	5 bits (32 states), constant step size (100 MHz)	–	0.391	–	pF
Quality factor (C_{min})(3)	Shunt(2)	470–582 MHz with L_s removed 698–960 MHz with L_s removed 1710–2170 MHz with L_s removed	–	50 50 28	–	–
Quality factor (C_{max})(3)	Shunt(2)	470–582 MHz with L_s removed 698–960 MHz with L_s removed 1710–2170 MHz with L_s removed	–	25 20 5	–	–
Self-resonant frequency (SRF)	Shunt(1)	State 00000 State 11111	–	4.7 1.6	–	GHz
Second- and third-order harmonics (2_{fo} and 3_{fo})(4)	Shunt(2)	470–582 MHz, P_{IN} +26 dBm, 50Ω 698–915 MHz, P_{IN} +26 dBm, 50Ω 1710–1910 MHz, P_{IN} +26 dBm, 50Ω	–	–	-36 -36 -36	dBm
	Series(5)	470–582 MHz, P_{IN} +26 dBm, 50Ω 698–915 MHz, P_{IN} +26 dBm, 50Ω 1710–1910 MHz, P_{IN} +26 dBm, 50Ω	–	–	-36 -36 -36	dBm
Third-order intercept point	Shunt(2)	IIP3 = ($P_{blocker}$ + 2 × P_{tx} - [IMD3]) / 2, where IMD3 = -95 dBm, P_{tx} = +20 dBm, and $P_{blocker}$ = -15 dBm.	–	60	–	dBm
Switching time(6)(7)	Shunt(2)	State change to 10/90% delta capacitance between only two states.	–	2	10	µs
Startup time(6)	Shunt(2)	Time from V_{DD} within the specification to all performances within the specification.	–	5	20	µs
Wake-up time(6)(7)	Shunt(2)	State change from standby mode to RF state to all performances within the specification.	–	5	20	µs

Parameter	Config.	Condition	Min	Typ	Max	Unit

1. DTC operation above self-resonant frequency (SRF) is possible.
2. Connect RF- to ground.
3. Q for a shunt DTC is based on a series RLC equivalent circuit. $Q = X_C / R = (X - X_L) / R$, where $X = X_L + X_C$, $X_L = 2 \times \pi \times f \times L$, $X_C = -1 / (2 \times \pi \times C)$, which is equal to removing the effect of parasitic inductance L_S.
4. Between 50Ω ports in series or shunt configuration using a pulsed RF input with 4620 vs period, 50% duty cycle, measured per 3GPPTS45.005.
5. In series configuration, apply the greater RF power or a higher RF voltage to RF+.
6. To achieve the specified performance, provide a DC path to ground at RF+ and RF–.
7. State change activated on the falling edge of SEN following the data word.

Typical performance data

Figure 2–Figure 11 show the typical performance data at +25 °C and 2.8V, unless otherwise specified.

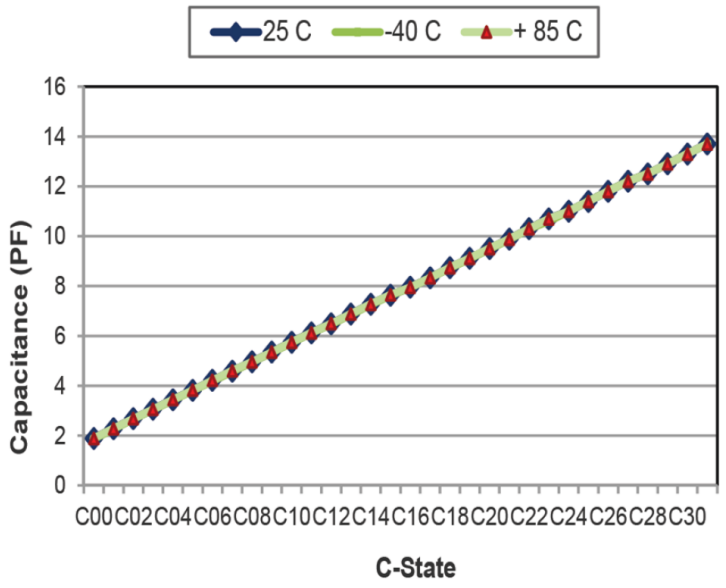


Figure 2. Measured shunt C (@100 MHz) vs state (temperature)

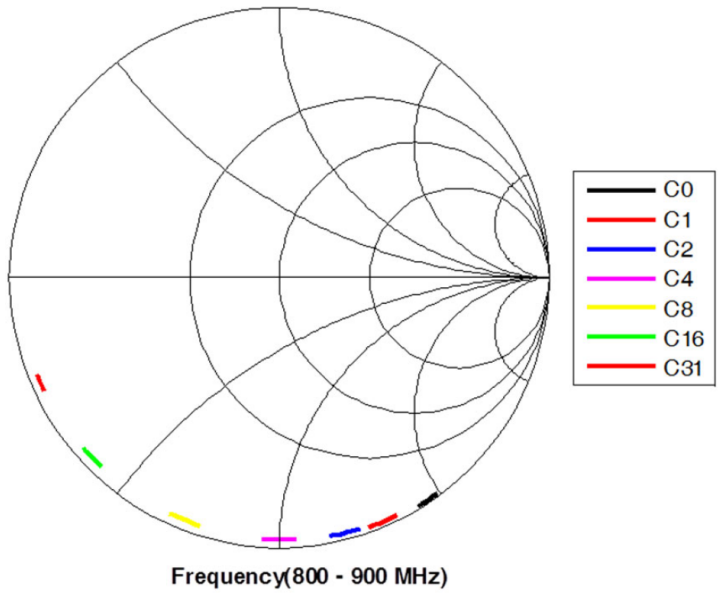


Figure 3. Measured shunt S_{11} (major states)

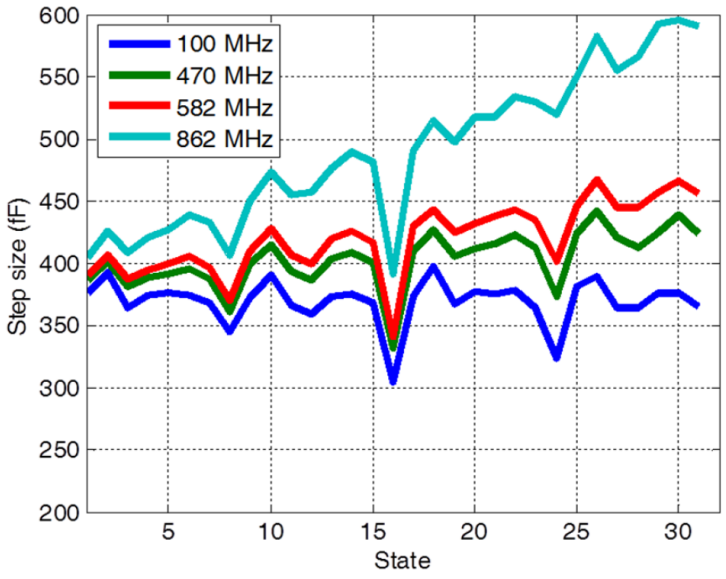


Figure 4. Measured step size vs. state (frequency)

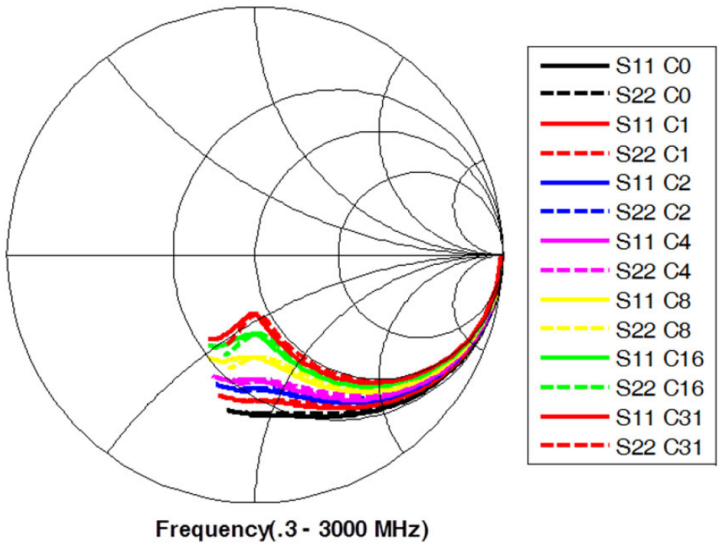


Figure 5. Measured series S_{11}/S_{22} (major states)

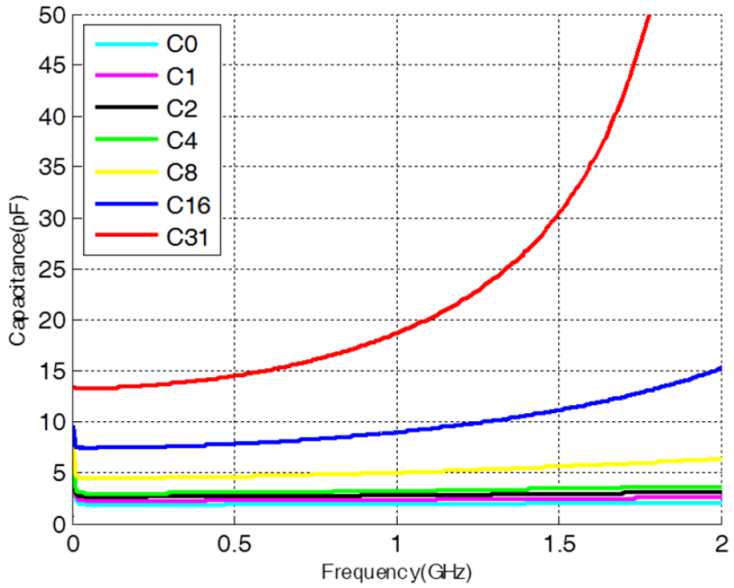


Figure 6. Measured shunt C vs. frequency (major states)

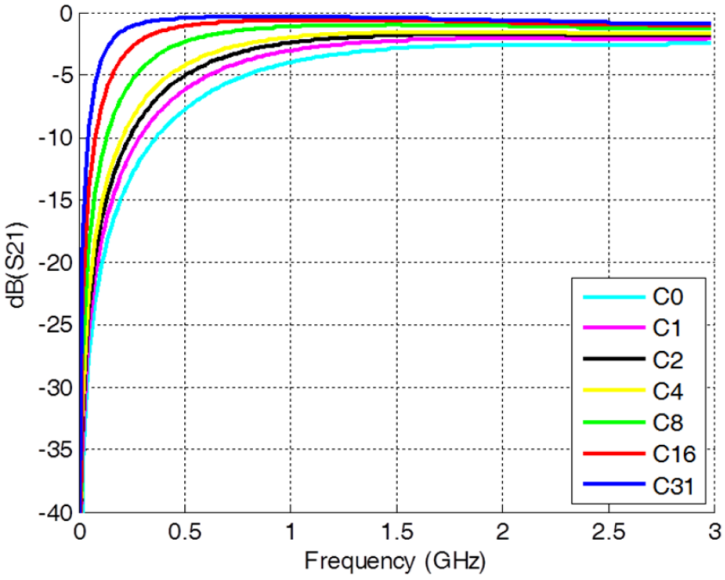


Figure 7. Measured series S_{21} vs. frequency (major states)

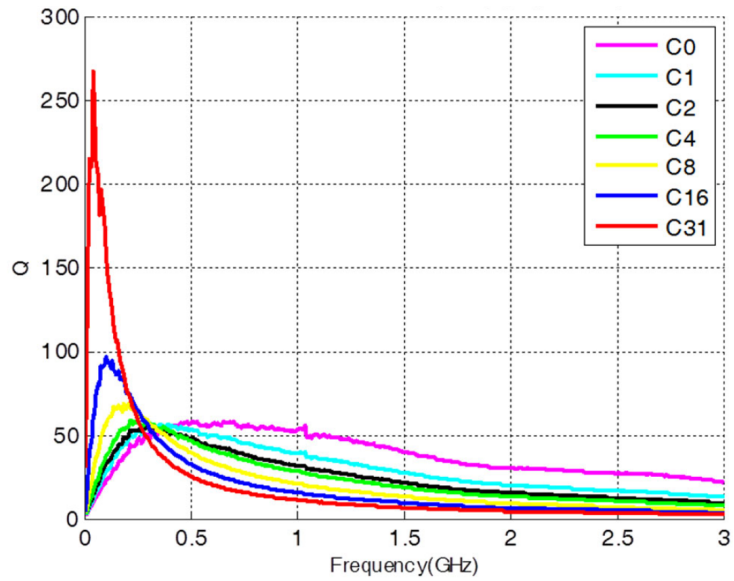


Figure 8. Measured shunt Q vs. frequency (major states)

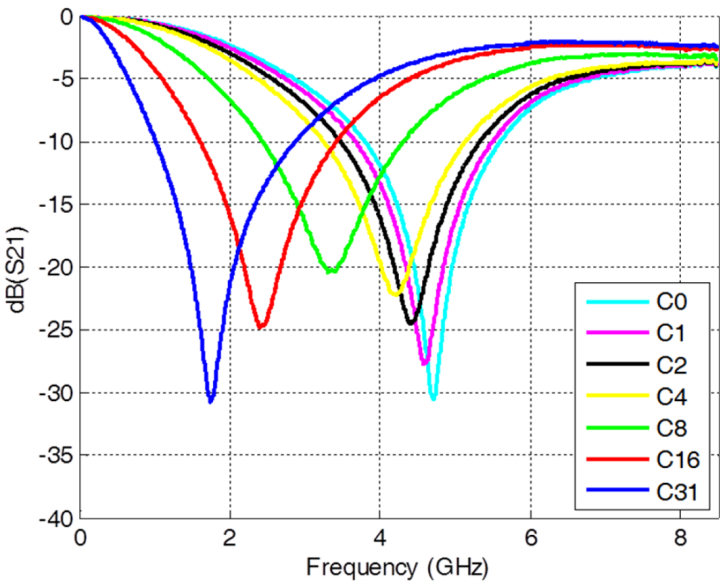


Figure 9. Measured 2-port shunt S_{21} vs. frequency (major states)

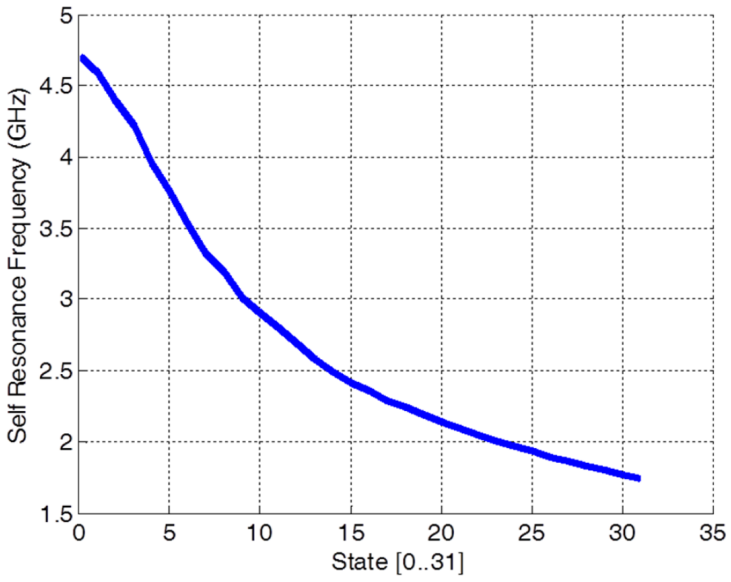


Figure 10. Measured self-resonance frequency (SRF) vs. state

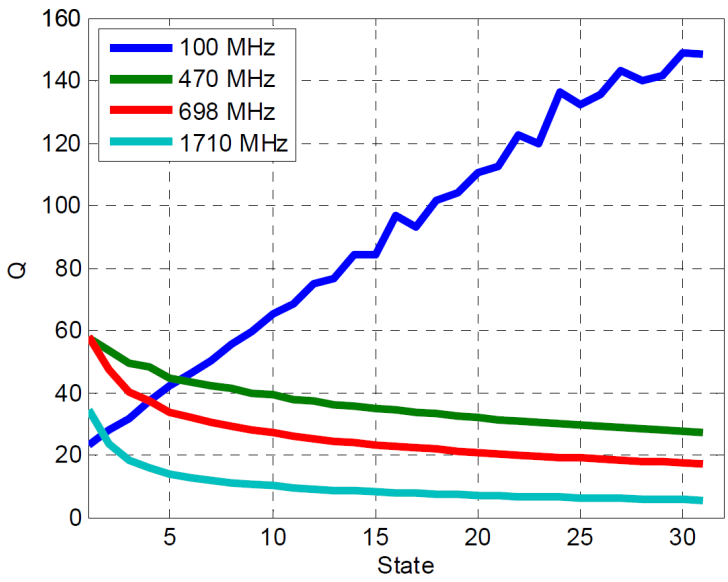


Figure 11. Measured shunt Q vs. state

Serial interface operation and sharing

The PE64102 is controlled by a 3-wire SPI-compatible interface. As shown in Figure 12, the serial master initiates the start of a telegram by driving the Serial Enable (SEN) line high. Each bit of the 8-bit telegram is clocked in on the rising edge of the Serial Clock (SCL) line. The Serial Data (SDA) bits are clocked by the most significant bit (MSB) first, as shown in Table 4 and Figure 12. Transactions on SDA are allowed on the falling edge of SCL. The DTC activates the data on the falling edge of SEN. The DTC does not count how many bits are clocked and only maintains the last eight bits it received.

You can control multiple DTCs with a single interface by using a dedicated enable (SEN) line for each DTC. The SDA, SCL, and V_{DD} lines can be shared, as shown in Figure 13. The dedicated SEN lines act as a chip select, so each DTC only responds to serial transactions intended for it. This makes each DTC change states sequentially as it is programmed.

Alternatively, you can use a dedicated SDA line with a common SEN. This allows all DTCs to change states simultaneously but requires all DTCs to be programmed even if the state is not changed.

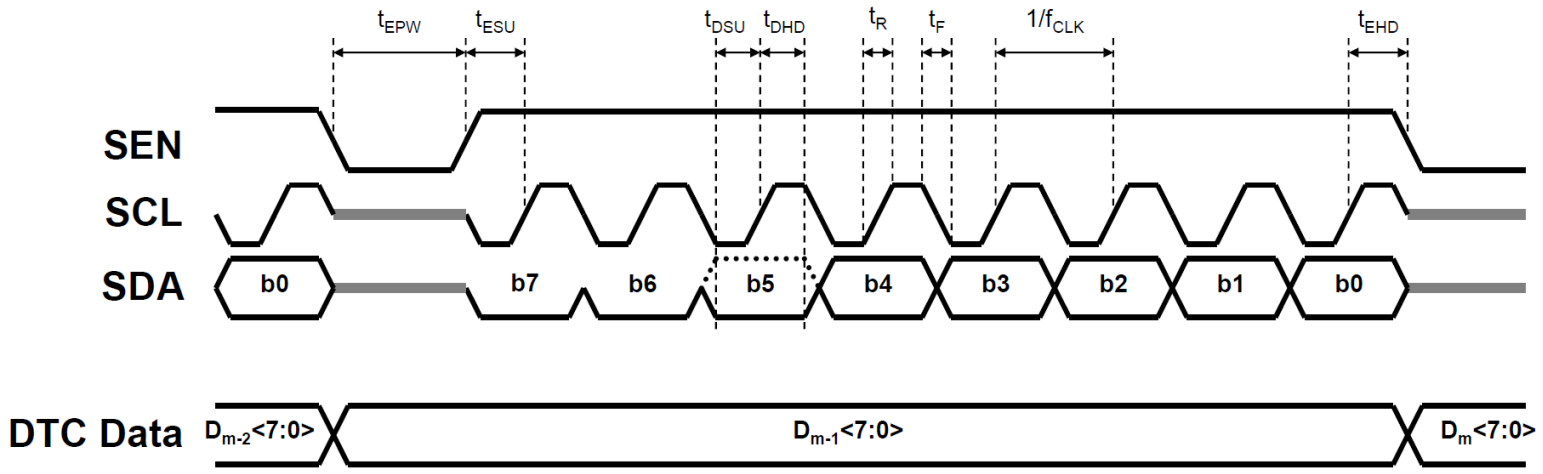


Figure 12. Serial interface timing diagram (oscilloscope view)

Table 4. 6-bit serial programming register map

b7	b6	b5	b4	b3	b2	b1	b0
0	0	STB(*)	d4	d3	d2	d1	d0
↑ MSB (first in)							LSB (last in) ↑

* The DTC is active when low (set to 0) and in low-current standby mode when high (set to 1).

In Table 5, 2.3V < V_{DD} < 3.6V and -40 °C < T_A < +85 °C, unless otherwise specified.

Table 5. Serial interface AC characteristics

Parameter	Symbol	Min	Max	Unit
Serial clock frequency	f_{CLK}	–	26	MHz
SCL, SDA, SEN rise time	t_R	–	6.5	ns
SCL, SDA, SEN falltime	t_F	–	6.5	
SEN rising edge to SCL rising edge	t_{ESU}	19.2	–	
SCL rising edge to SEN falling edge	t_{EHD}	19.2	–	
SDA valid to SCL rising edge	t_{DSU}	13.2	–	
SDA valid after SCL rising edge	t_{DHD}	13.2	–	
SEN falling edge to SEN rising edge	t_{EOW}	38.4	–	

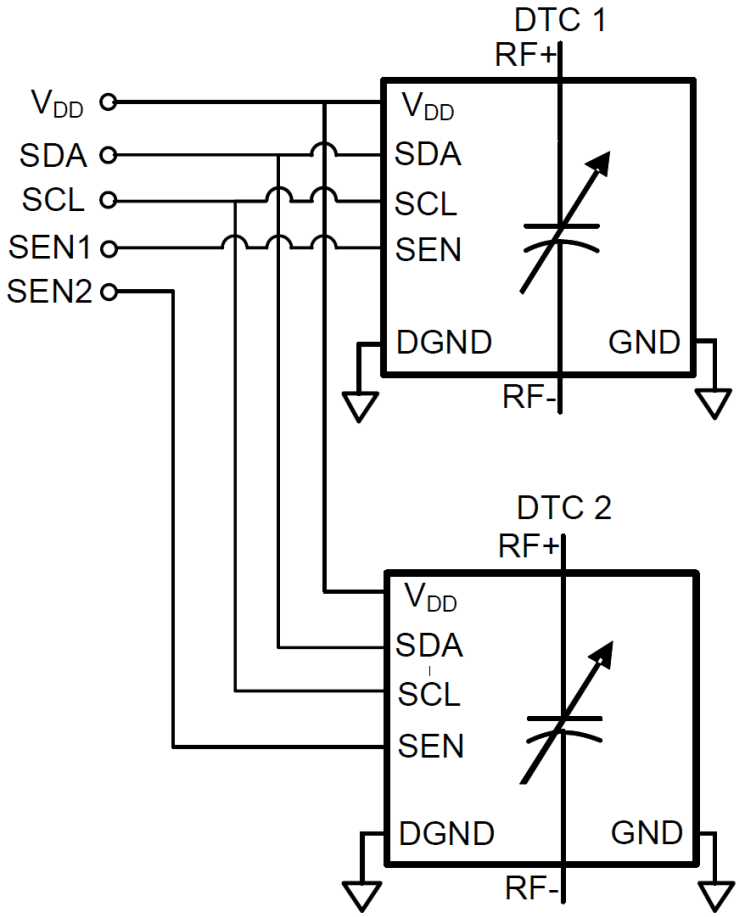


Figure 13. Recommended bus sharing

Equivalent circuit model description

The DTC equivalent circuit model includes all parasitic elements and is accurate in both series and shunt configurations, reflecting physical circuit behavior accurately and providing close correlation to measured data. It can easily be used in circuit simulation programs. Simple equations are provided for the state dependent parameters. The tuning core capacitance C_S represents the capacitance between the RF+ and RF- ports. It is linearly proportional to the state (0 to 31 in decimal) in a discrete fashion. The series tuning ratio is defined as C_{Smax}/C_{Smin}.

C_{P1} and C_{P2} represent the circuit and package parasitics from the RF ports to GND:

- In shunt configuration, the total capacitance of the DTC is higher due to parallel combination of C_P and C_S.
- In series configuration, C_S and C_P do not add in parallel and the DTC appears as an impedance transformation network.

Parasitic inductance due to the circuit and package is modeled as L_S and causes the apparent capacitance of the DTC to increase with frequency until it reaches the self-resonant frequency (SRF). The SRF value depends on the state and is approximately inversely proportional to the square root of the capacitance.

The DTC overall dissipative losses are modeled by the R_S, R_{P1}, and R_{P2} resistors. The R_S parameter represents the equivalent series resistance (ESR) of the tuning core and depends on the state. R_{P1} and R_{P2} represent losses due to the parasitic and biasing networks.

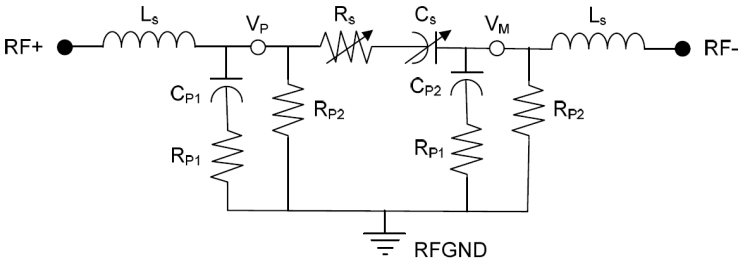


Figure 14. Equivalent circuit model schematic

Table 6. Equivalent circuit model parameters

Variable	Equation (state = 0, 1, 2 ...31)	Unit
C_S	0.394 × state + 1.456	pF
R_S	15 / (state + 15 / (state + 0.4)) + 0.4	Ω
C_{P1}	-0.0026 × state + 0.4155	pF
C_{P2}	0.0029 × state + 0.4914	pF
R_{P1}	4	Ω
R_{P2}	22000 + 6 × (state)^3	Ω
L_S	0.4	nH

Table 7. Maximum operating RF voltage

Condition	Limit
V_P to V_M	6 V_{PK}
V_P to RFGND	6 V_{PK}
V_M to RFGND	6 V_{PK}

Table 8. Equivalent circuit data

State		DTC core		Parasitic elements				
Binary	Decimal	CS (pF)	RS (Ω)	CP1 (pF)	CP2 (pF)	RP2 (kΩ)	LS (nH)	RP1 (Ω)
00000	0	1.40	0.80	0.42	0.49	22.0	0.40	4.0
00001	1	1.79	1.68	0.41	0.49	22.0		
00010	2	2.19	2.22	0.41	0.50	22.0		
00011	3	2.58	2.42	0.41	0.50	22.2		
00100	4	2.98	2.42	0.41	0.50	22.4		
00101	5	3.37	2.33	0.40	0.51	22.8		
00110	6	3.76	2.20	0.40	0.51	23.3		
00111	7	4.16	2.06	0.40	0.51	24.1		
01000	8	4.55	1.93	0.39	0.51	25.1		
01001	9	4.95	1.82	0.39	0.52	26.4		
01010	10	5.34	1.71	0.39	0.52	28.0		
01011	11	5.73	1.62	0.39	0.52	30.0		
01100	12	6.13	1.54	0.38	0.53	32.4		
01101	13	6.52	1.46	0.38	0.53	35.2		
01110	14	6.92	1.40	0.38	0.53	38.5		
01111	15	7.31	1.34	0.38	0.53	42.3		
10000	16	7.70	1.29	0.37	0.54	46.6		
10001	17	8.10	1.24	0.37	0.54	51.5		
10010	18	8.49	1.20	0.37	0.54	55.0		
10011	19	8.89	1.16	0.37	0.55	63.2		
10100	20	9.28	1.12	0.36	0.55	70.0		
10101	21	9.67	1.09	0.36	0.55	77.6		
10110	22	10.07	1.06	0.36	0.56	85.9		
10111	23	10.46	1.03	0.36	0.56	95.0		
11000	24	10.86	1.01	0.35	0.56	104.9		
11001	25	11.25	0.99	0.35	0.56	115.8		
11010	26	11.64	0.96	0.35	0.57	127.5		
11011	27	12.04	0.94	0.35	0.57	140.1		
11100	28	12.43	0.93	0.34	0.57	153.7		
11101	29	12.83	0.91	0.34	0.58	168.3		

State		DTC core		Parasitic elements				
Binary	Decimal	CS (pF)	RS (Ω)	CP1 (pF)	CP2 (pF)	RP2 (kΩ)	LS (nH)	RP1 (Ω)
11110	30	13.22	0.89	0.34	0.58	184.0	0.40	4.0
11111	31	13.61	0.88	0.33	0.57	200.7		

Evaluation kit

pSemi designed the PE64102 evaluation board to accurately measure the DTC impedance and loss. Two configurations are available:

- 1-port shunt (J3), and
- 2-port series (J4, J5)

Three calibration standards are provided. The open (J2) and short (J1) standards (104 ps delay) are used to perform port extensions and account for electrical length and transmission line loss. Use the Thru (J9, J10) standard to estimate the PCB transmission line losses for scalar de-embedding of the 2-port series configuration (J4, J5).

The board consists of a 4-layer stack with 2 outer layers made of Rogers 4350B (εr = 3.48) and two inner layers of FR4 (εr = 4.80). The total thickness of this board is 62 mils (1.57 mm). The inner layers provide a ground plane for the transmission lines. Each transmission line is designed using a coplanar waveguide with ground plane (CPWG) model using a trace width of 32 mils (0.813 mm), gap of 15 mils (0.381 mm), and a metal thickness of 1.4 mils (0.036 mm).

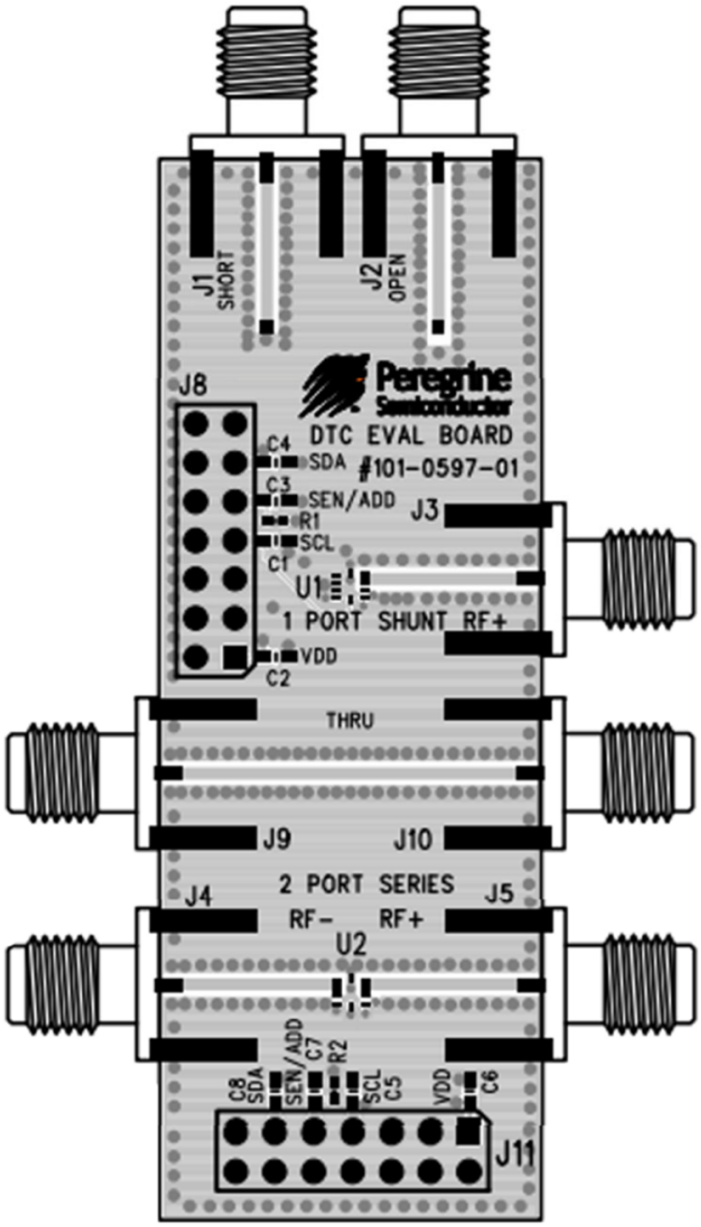


Figure 15. Evaluation board layout

Evaluation board schematic

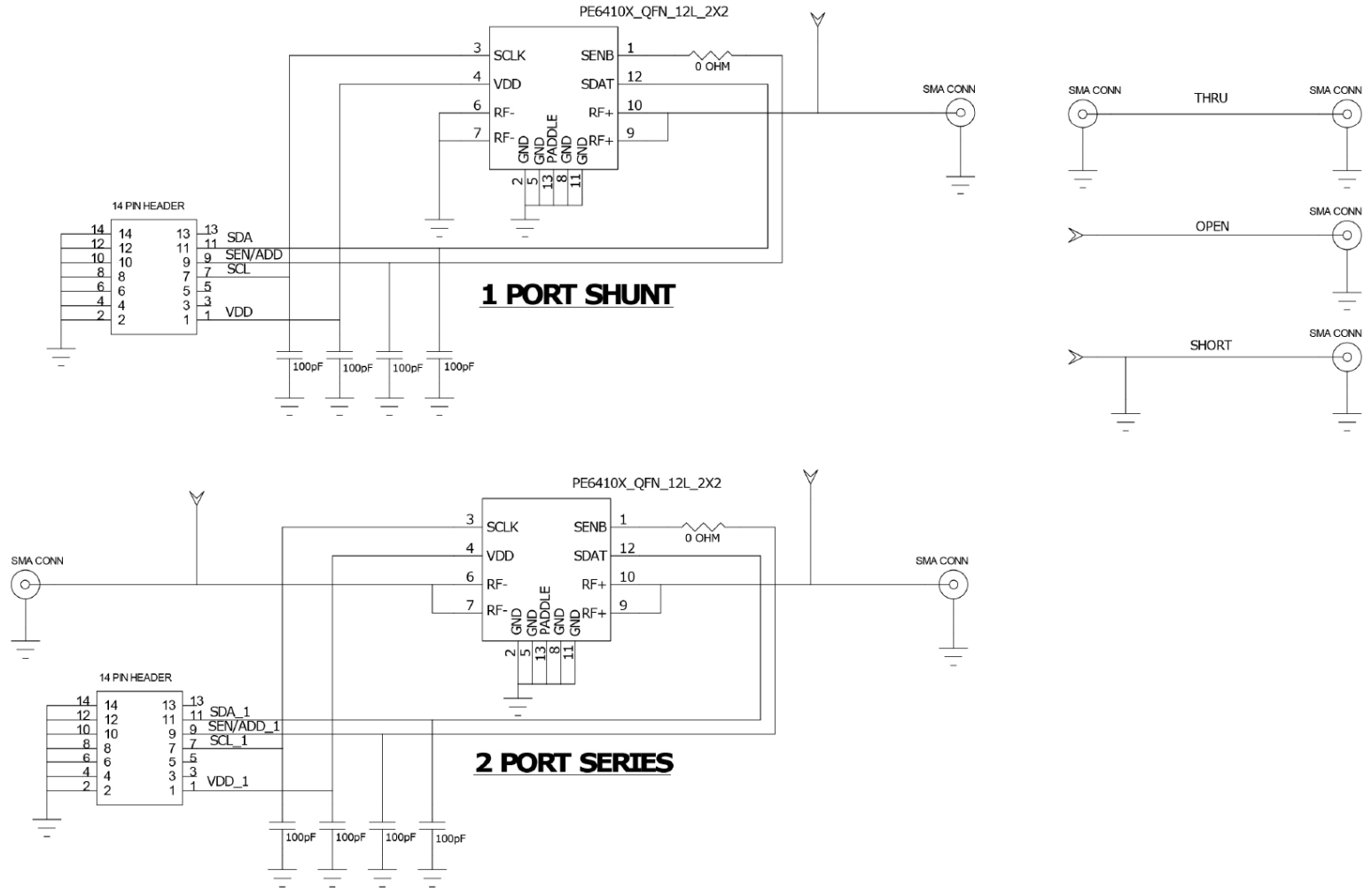


Figure 16. Evaluation board schematic

Pin information

Figure 17 shows the PE64102 pin map for the 12-lead 2 × 2 × 0.55 mm QFN package, and Table 9 lists the description for each pin.

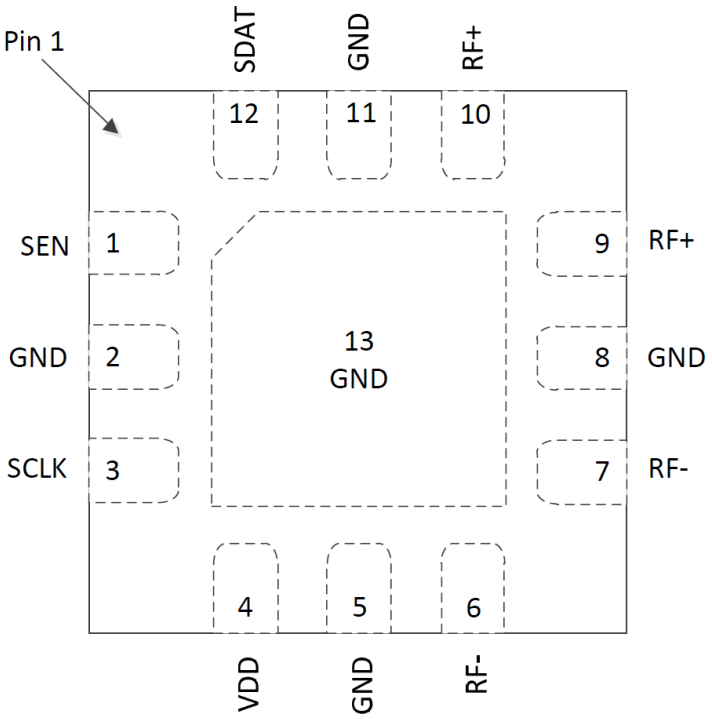


Figure 16. Pin configuration (top view)

Table 9. PE64102 pin descriptions

Pin no.	Pin name	Description
1	SEN	Serial enable
2, 5, 8, 11, 13(1)	GND	Digital and RF ground
3	SCLK	Serial interface clock input
4	VDD	Power voltage
6, 7(2)	RF-	Negative RF ports
9, 10(3)	RF+	Positive RF ports
12	SDAT	Serial interface data input

1. Connect GND pins 2, 5, 8, 11, and 13 together on the PCB.
2. To reduce inductance, tie RF- pins 6 and 7 together on the PCB.
3. To reduce inductance, tie RF+ pins 9 and 10 together on the PCB.

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE64102 moisture sensitivity level rating for the 12-lead 2 × 2 × 0.55 mm QFN package is MSL1.

Package drawing

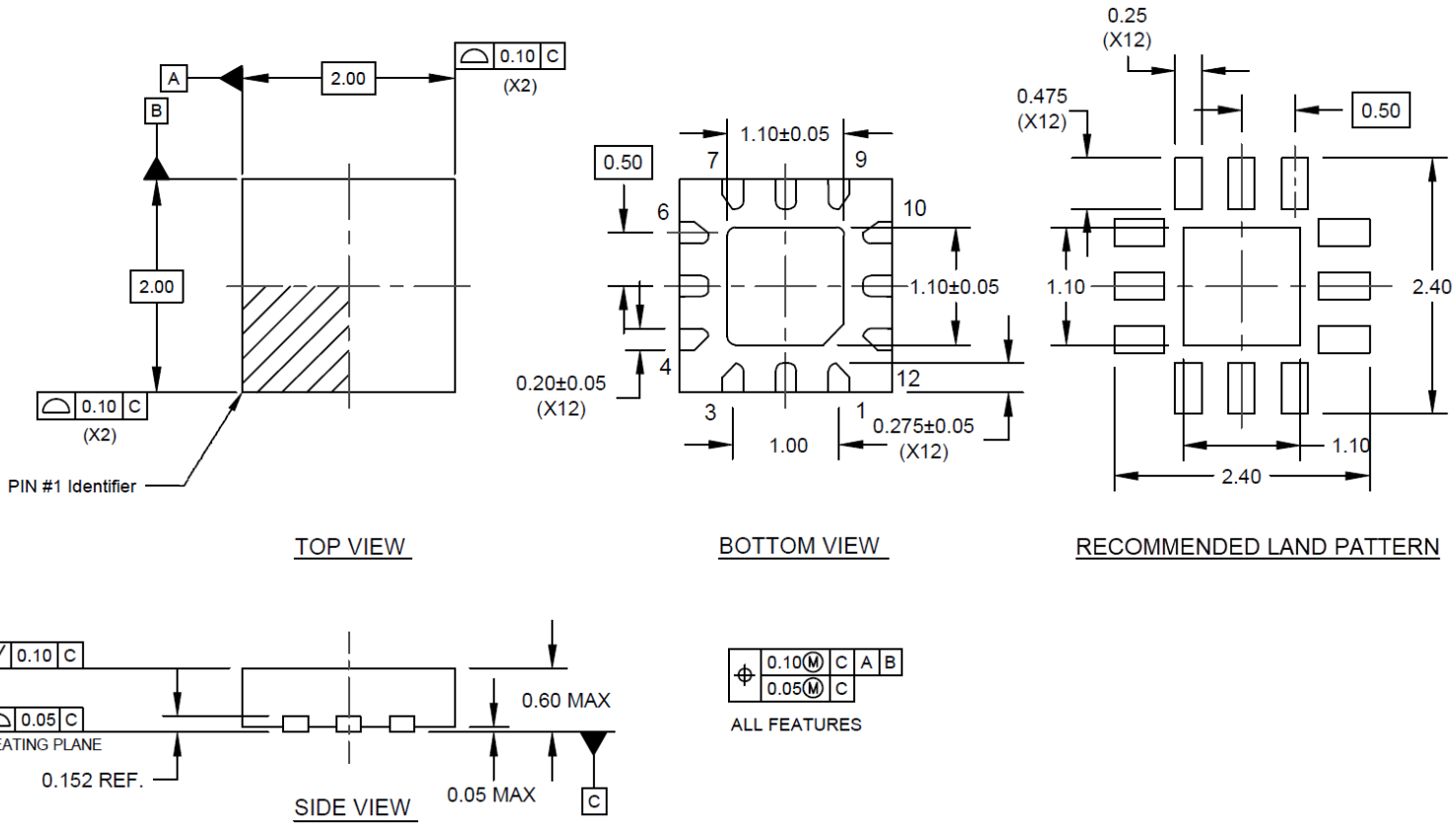
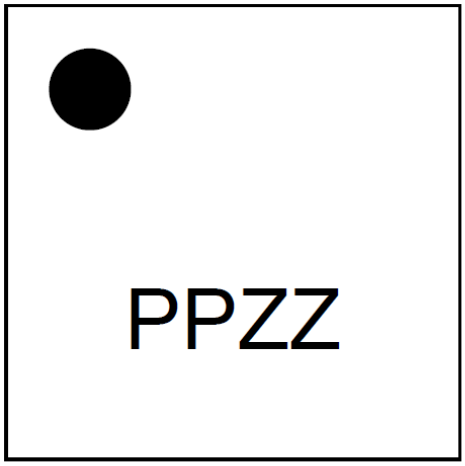


Figure 18. Package mechanical drawing for the 12-lead 2 × 2 × 0.55 mm QFN package

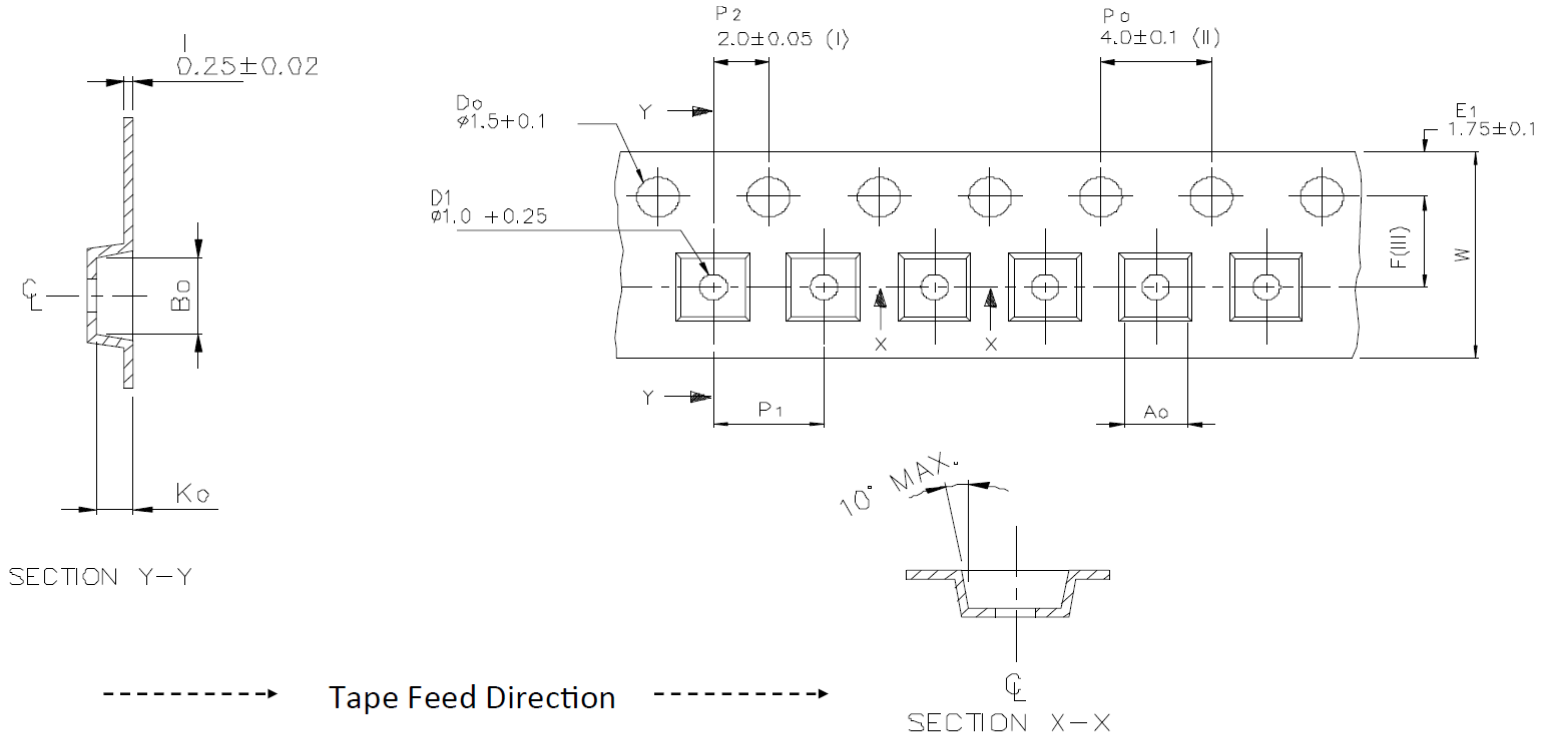
Top-marking specification

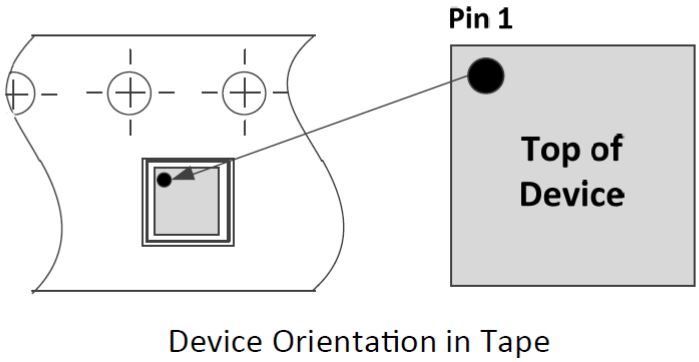


Marking Spec Symbol	Package Marking	Definition
PP	CS	Part number marking for PE64102
ZZ	00-99	Last two digits of lot code
Y	0-9	Last digit of year, starting from 2009 (0 for 2010, 1 for 2011, etc)
WW	01-53	Work week

Figure 19. PE64102 package marking specification

Tape and reel specification





Device Orientation in Tape

Figure 20. Tape and reel specification for the 12-lead 2 × 2 × 0.55 mm QFN package

- The diagram is not drawn to scale.
- The units are in millimeters (mm).
- The maximum cavity angle is five degrees.
- The bumped die are oriented active side down.

Ordering information

Order code	Description	Packaging	Shipping method
PE64102B-Z	PE64102 UltraCMOS® digitally tunable capacitor	12-lead 2 × 2 × 0.55 mm QFN	3000 units/T&R
EK64102-12	PE64102 evaluation kit	Evaluation kit	1/box

Document categories

Advance Information	The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.
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