muRata
INNOVATOR IN ELECTRONICS

DNT24MCA
DNT24MPA

Low Cost 2.4 GHz FHSS Transceiver Modules with I/O

- 2.4 GHz Frequency Hopping Spread Spectrum Transceivers
- Direct Peer-to-peer Low Latency Communication
- Transmitter RF Power Configurable - 6.3 or 63 mW
- Built-in Chip Antenna
- 250 kbps RF Data Rate
- Serial Port Data Rate up to 250 kbps, SPI Port Data Rate up to 500 kbps
- 128-Bit AES Encryption
- Separate Serial Port for Diagnostics
- Analog and Digital I/O for Sensor Applications
- FCC, Canadian IC and ETSI Certified for Unlicensed Operation

The DNT24MCA and DNT24MPA FHSS transceiver modules provide a low-cost, versatile solution for wireless data communications in the 2.4 GHz ISM band. Direct peer-to-peer communication provides very low transmission latency between all modules in a network. The DNT24MCA/MPA RF output power can be set at 6.3 or 63 mW. The DNT24MCA/MPA modules include analog, digital and serial I/O, providing the flexibility to serve applications ranging from cable replacements to sensor networks. The built-in chip antenna makes these modules very easy to integrate.

DNT24MCA/MPA Absolute Maximum Ratings

Rating	Value	Units
Power Supply Input	-0.5 to +6.5	V
All Input/Output Pins	-0.5 to +3.3	V
Input Power to RFIO Port	0	dBm

DNT24MCA/MPA Electrical Characteristics

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
RF Communication Topology				Direct Peer-to-Peer		
Spread Spectrum Mode				Frequency Hopping		
Operating Frequency Range			2406		2475	MHz
Number of RF Channels		1		15		
Number of Hopping Patterns				64		
Hop Duration		1	8		100	ms
Modulation				FSK		
RF Data Transmission Rate				250		kbps
Packet Transmission Time Including FHSS Synchronization and Acknowledgement				16		ms
Receiver Sensitivity @ 10^{-5} BER				-100		dBm
Transmitter RF Output Power		1		6.3 or 63 mW		mW
Antenna				Dielectric Chip Antenna		Ω

DNT24MCA/MPA Electrical Characteristics

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
ADC Input Range			0		2.7	V
ADC Input Resolution					12	bits
ADC Sample Rate				100		Hz
Signal Source Impedance for ADC Reading					10	KΩ
ADC External Reference Voltage Range			1.0		2.7	V
DAC Output Range			0		3.3	V
DAC Output Resolution					12	bits
Primary and Diagnostic Serial Port Baud Rates			1.2, 2.4, 4.8, 9.6, 14.4, 19.2, 28.8, 38.4, 57.6, 115.2, 230.4, 250.0			kbps
Master Serial Peripheral Interface Data Rate			125	250	500	kbps
Slave Serial Peripheral Interface Data Rate					4000	kbps
Digital I/O:						
Logic Low Input Level			-0.5		0.8	V
Logic High Input Level			2.45		3.3	V
Logic Input Internal Pull-up Resistor				20		KΩ
Power Supply Voltage Range	V_{CC}		+3.3		+5.5	Vdc
Power Supply Voltage Ripple					10	mV_{P-P}
Peak Transmit Mode Current, 63 mW Output					140	mA
Operating Receive Current				40		mA
Sleep Current		2		3	6	µA
DNT24MCA Mounting			Reflow Soldering			
DNT24MPA Mounting			Socket			
Operating Temperature Range			-40		85	°C
Operating Relative Humidity Range, Non-condensing			10		90	%

Notes:

1. The DNT24MCA/MPA achieves regulatory certification under FHSS rules.
2. Maximum sleep current occurs at +85 °C.

CAUTION: Electrostatic Sensitive Device. Observe precautions when handling.

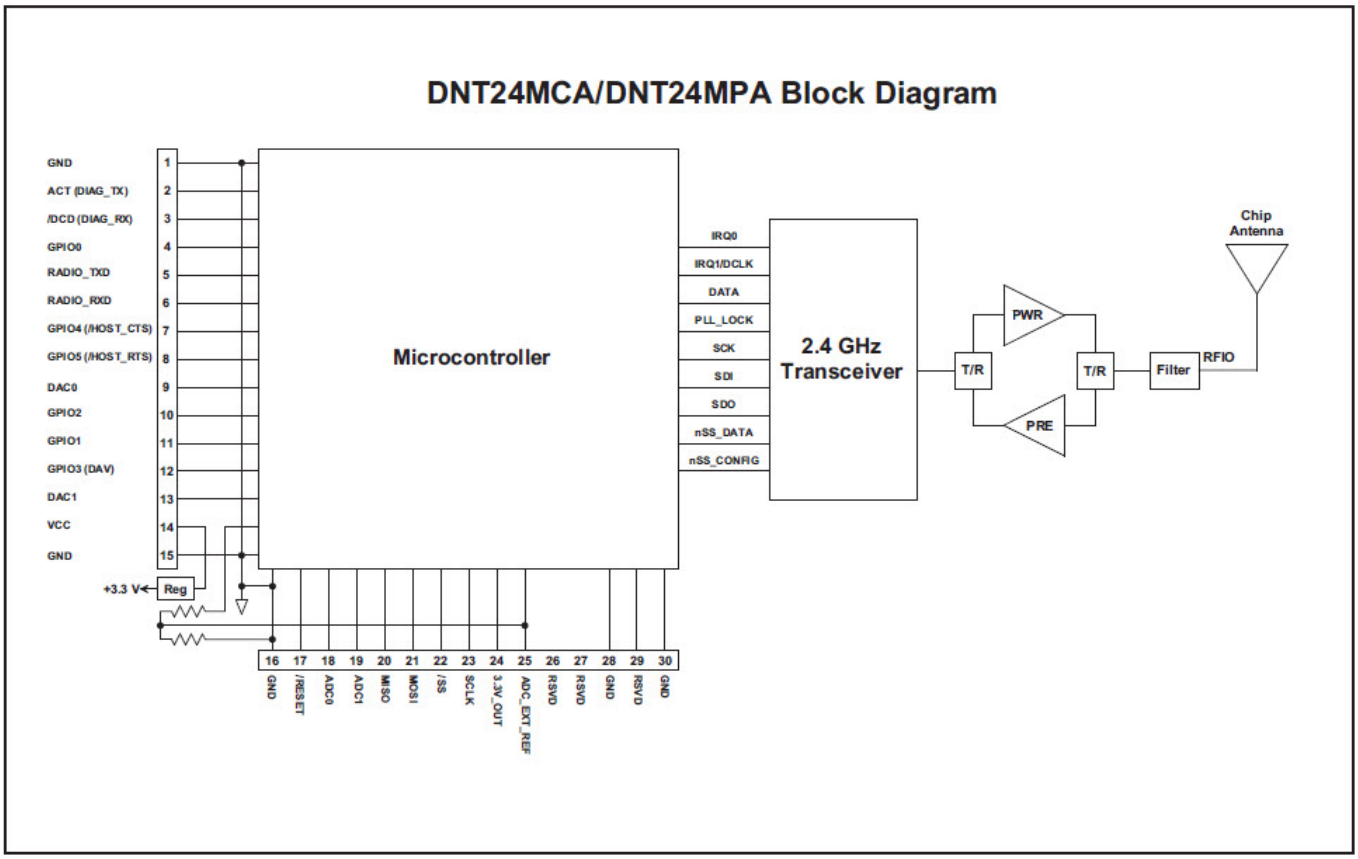

Figure 1

DNT24MCA/MPA Hardware

The major components of the DNT24MCA/MPA include a 2.4 GHz FHSS transceiver and a low current 8-bit microcontroller. The DNT24MCA/MPA hops across 15 frequency channels in the 2.4 GHz ISM band on one of 64 selectable hopping patterns. The DNT24MCA/MPA has two selectable RF output power levels: 6.3 mW and 63 mW. The built-in chip antenna makes these modules very easy to integrate.

The DNT24MCA/MPA provides a variety of hardware interfaces. There are two serial ports plus one SPI port. Either the primary serial port or the SPI port can be selected for data communications. The second serial port is dedicated to diagnostics. The primary and diagnostic serial ports support most standard baud rates up to 250.0 kbps. The SPI port supports data rates up to 500 kbps. The DNT24MCA/MPA also includes three ADC inputs, two DAC outputs, and six general-purpose digital I/O ports. Four of the digital I/O ports support an optional interrupt-from-sleep mode when configured as inputs. The radio is available in two mounting configurations. The DNT24MCA is designed for solder reflow mounting. The DNT24MPA is designed for plug-in connector mounting.

DNT24MCA/MPA Firmware

DNT24MCA/MPA firmware implements *direct peer-to-peer* data transmissions that provide very low transmission latency between all DNT24MCA/MPA radios in a network. In addition, efficient point-to-point and point-to-multipoint networks are readily configured using direct peer-to-peer transmissions.

DNT24MCA/MPA firmware provides the user with a rich set of configuration options including a choice of hopping patterns, serial and/or SPI data port operation, serial and SPI data rate selection, RF output power selection, plus configurable analog and digital I/O lines.

Data integrity is protected by 24-bit error detection, with optional ACK and automatic transmission retries or redundant transmissions. 128-bit AES encryption provides a high level of data security for sensitive applications. Sensor networks can take advantage of timer or event-based data reporting and remote node sleep cycling for extended battery life.

DNT24MCA/MPA I/O Descriptions

Pin	Name	I/O	Description
1	GND	-	Power supply and signal ground. Connect to the host circuit board ground.
2	ACT (DIAG_TX)	O (O)	This pin's default configuration is transmitter activity (ACT) output. The ACT signal is asserted whenever any data packet other than just an ACK is transmitted. The alternate function for this pin is the diagnostic serial port output.
3	/DCD (DIAG_RX)	O (I)	The /DCD signal is asserted when a DNT24MA receives a valid packet. If a radio is transmitting data and receiving ACKs, both the ACT and /DCD signals will be asserted. If a radio is receiving packets only, the /DCD signal will be asserted. The alternate function for this pin is the diagnostic serial port input.
4	GPIO0	I/O	Configurable digital I/O port 0. When configured as an input, an internal pull-up resistor can be selected and direct interrupt from sleep can be invoked. When configured as an output, the power-on state is configurable. In sleep mode the pin direction, input pull-up selection or output state are also separately configurable.
5	RADIO_TXD	O	Serial data output from the radio.
6	RADIO_RXD	I	Serial data input to the radio.
7	GPOI4 (/HOST_CTS)	I/O (O)	Default pin function is GPIO4 with the same configuration options as GPIO0. Alternate pin function is UART/SPI flow control output. The module sets this line low when it is ready to accept data from the host on the RADIO_RXD or MOSI input. When the line goes high, the host must stop sending data.
8	GPOI5 (/HOST_RTS)	I/O (I)	Default pin function is GPIO5 with the same configuration options as GPIO0. Alternate pin function is UART/SPI flow control input. The host sets this line low to allow data to flow from the module on the RADIO_TXD pin. When the host sets this line high, the module will stop sending data to the host.
9	DAC0	O	12-bit DAC 0 output. Full scale output can be referenced to the voltage at pin 25 or the 3.3 V regulated module bus voltage.
10	GPIO2	I/O	Configurable digital I/O port 2. Same configuration options as GPIO0.
11	GPIO1	I/O	Configurable digital I/O port 1. Same configuration options as GPIO0.
12	GPIO3 (DAV)	I/O (O)	Default pin function is GPIO3 with the same configuration options as GPIO0. When SPI slave mode operation is enabled, a logic high on this pin indicates when data is available to be clocked out by the SPI master.
13	DAC1	O	12-bit DAC 1 output. Same specifications and configuration options as DAC0.
14	VCC	I	Power supply input, +3.3 to +5.5 Vdc.
15	GND	-	Power supply and signal ground. Connect to the host circuit board ground.
16	GND	-	Power supply and signal ground. Connect to the host circuit board ground.
17	/RESET	I	Active low module hardware reset.
18	ADC0	I	ADC input 0. This pin is a direct ADC input when the ADC is operating in single-ended mode, or the differential negative input for positive inputs applied to ADC1 or ADC2 when the ADC is operating in differential mode. Full-scale reading can be referenced to Pin 25 for ratiometric measurements. For absolute measurements, the ADC can use either the regulated supply voltage divided by 1.6 (about 2.06 V), or an external voltage applied to Pin 25. In single-ended mode, ADC measurements are 11-bit unsigned values with full scale nominally 2.7 V when referenced to a 2.7 V input on Pin 27. In differential mode, ADC measurements are 12-bit signed values.
19	ADC1	I	ADC input 1. Direct input when the ADC is operating in single-ended mode, positive differential input relative to ADC0 when the ADC is operating in differential mode.
20	MISO	I/O	This pin is the SPI master mode input or slave mode output.
21	MOSI	I/O	This pin is the SPI master mode output or slave mode input.
22	/SS	I/O	SPI active low slave select. This pin is an output when the module is operating as a master, and an input when it is operating as a slave.
23	SCLK	I/O	SPI clock signal. This pin is an output when operating as a master, and an input when operating as a slave.

Pin	Name	I/O	Description
24	ADC2	I	ADC input 2. Direct input when the ADC is operating in single-ended mode, positive differential input relative to ADC0 when the ADC is operating in differential mode.
25	ADC_EXT_REF	I/O	ADC external reference voltage pin. The voltage at this pin can be used by the ADCs as a reference for ratiometric measurements. With no external voltage or load applied, this pin presents a nominal 2.7 V output through a 2.126 K source resistance. A low impedance external reference voltage in the range of 1 to 2.7 V may be applied to this pin as an option.
26	RSVD	-	Reserved pin. Leave unconnected.
27	RSVD	-	Reserved pin. Leave unconnected.
28	GND	-	Connect to the host circuit board ground plane.
29	RSVD	-	Reserved pin. Leave unconnected.
30	GND	-	Connect to the host circuit board ground plane.

DNT24MCA Outline and Mounting Dimensions

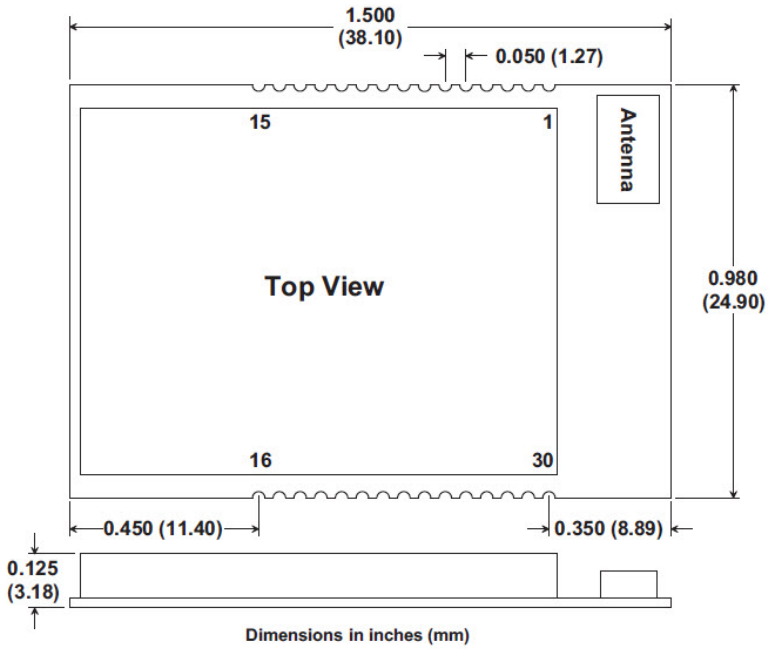

Figure 2

DNT24MCA Solder Pad Dimensions

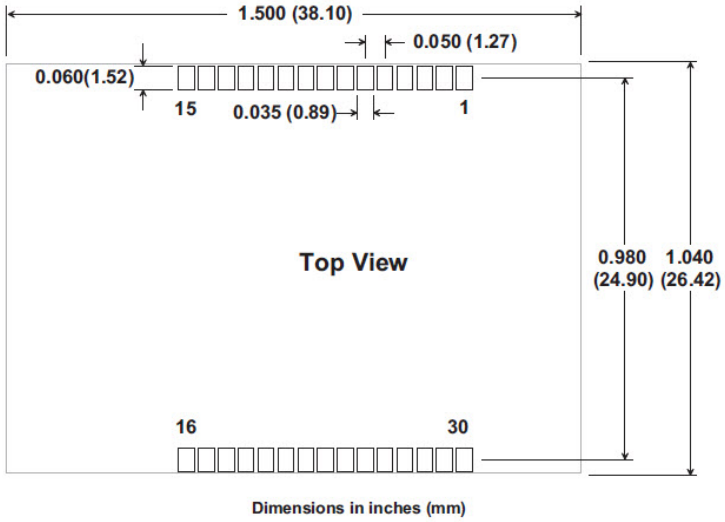

Figure 3

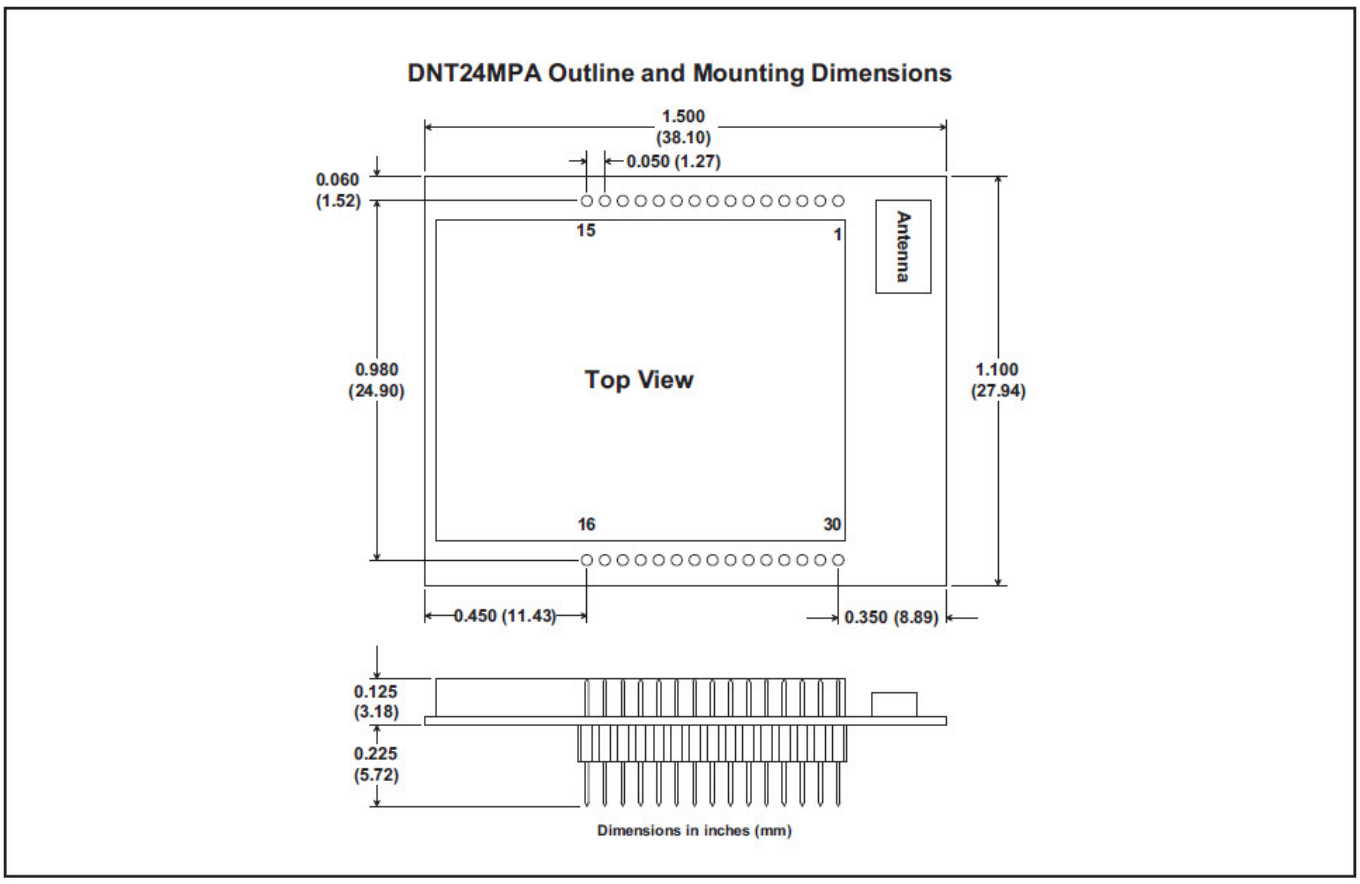

Figure 4

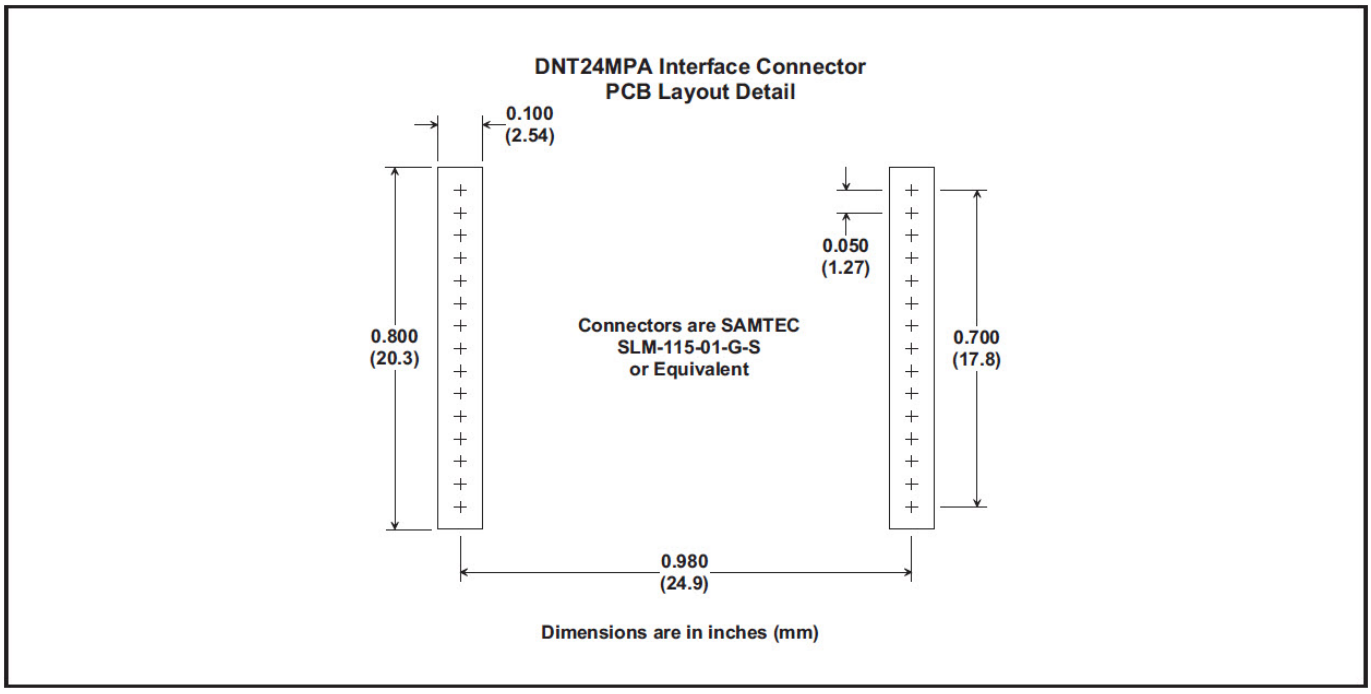

Figure 5

Note: Specifications subject to change without notice.