

## Smart Codec with Low-Power Audio DSP

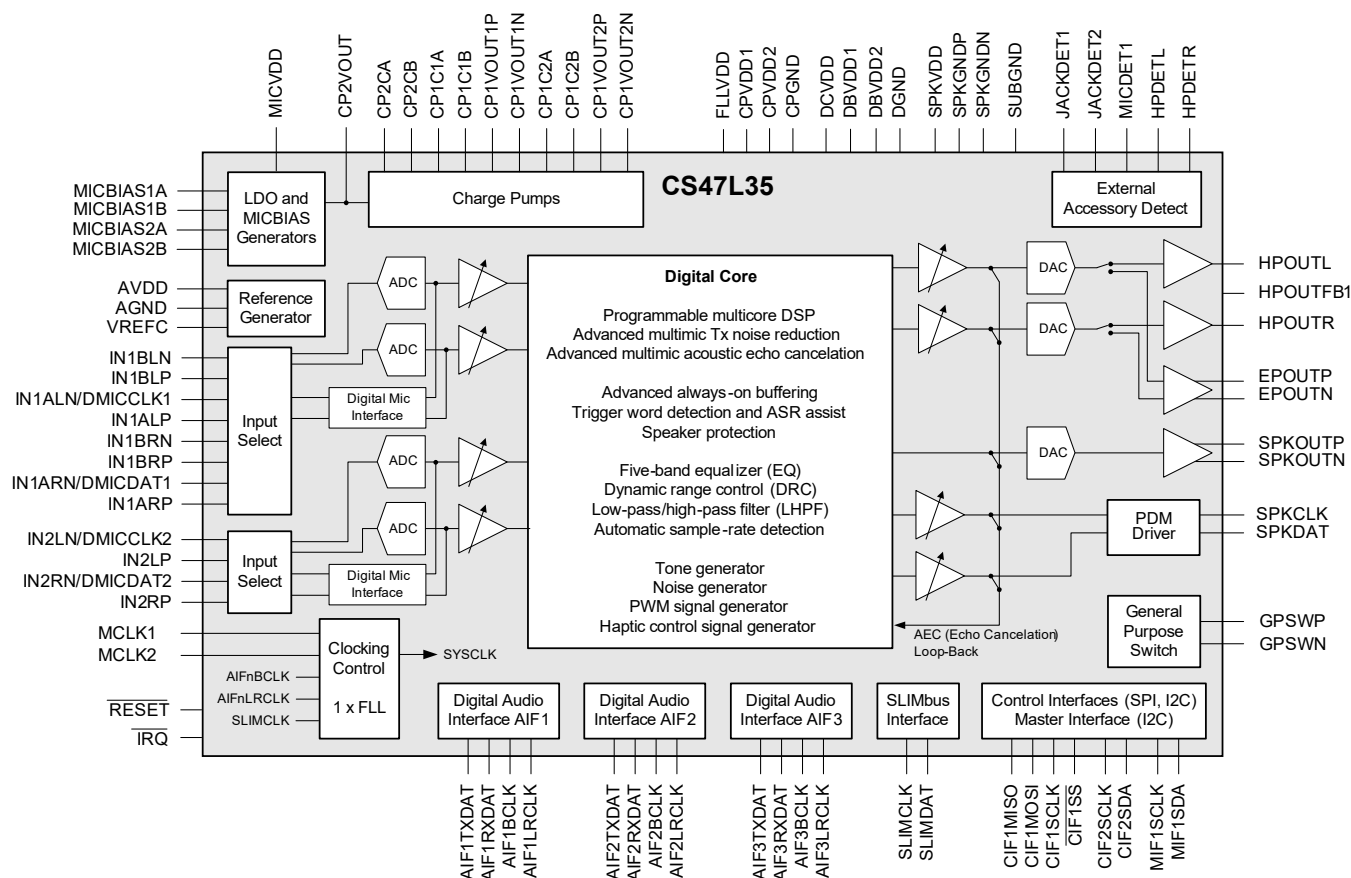
### Features

- 450 MIPS, 450 MMAC multicore audio-signal processor
- Programmable wideband, multimic audio processing
  - Transmit-path noise reduction and echo cancellation
  - Wind-noise, side-tone, and other programmable filters
- Integrated multichannel 24-bit hi-fi audio hub codec
  - 101-dB signal-to-noise ratio (SNR) mic input (48 kHz)
  - 122-dB SNR headphone playback (48 kHz)
- Up to six analog or four digital microphone (DMIC) inputs
- Stereo headphone/earpiece/line output driver: 30 mW into 32- $\Omega$  load at 0.1% total harmonic distortion + noise (THD+N)
- Class D speaker and digital (pulse-density modulation, PDM) output interfaces
- SLIMbus® audio and control interface

- Three full digital-audio interfaces
  - Standard sample rates from 8 to 192 kHz
  - Multichannel time-division multiplexing (TDM) support on AIF1
- Flexible clocking, derived from MCLK<sub>n</sub>, AIF<sub>n</sub>, or SLIMbus
- Low-power frequency-locked loop (FLL) supports reference clocks down to 32 kHz
- Configurable functions on up to 16 general-purpose input/output (GPIO) pins
- Sensor-hub connectivity, with event time-stamp functions
- Integrated regulators and charge pumps
- Small WLCSP package, 0.4-mm ball array

### Applications

- Smartphones and multimedia handsets
- Tablets and mobile Internet devices



---

## Description

The CS47L35 is a highly integrated, low-power audio hub for smartphones, tablets, and other portable audio devices. It combines an advanced DSP feature set with a flexible, high-performance audio hub codec. The CS47L35 combines three programmable DSP cores with a variety of power-efficient fixed-function audio processors. Flexible GPIO and an I2C master interface are also incorporated, enabling sensor-hub connectivity.

The DSP cores support multiple concurrent audio features, including multimic wideband noise reduction, high-performance acoustic-echo cancellation (AEC), speech enhancement, advanced media enhancement, and many more. The DSP cores are supported by a fully flexible, all-digital mixing and routing engine with sample-rate converters, for wide use-case flexibility. Support for third-party DSP programming provides far-reaching opportunities for product differentiation.

A SLIMbus interface supports multichannel audio paths and host control register access. Three further digital audio interfaces are provided, each supporting a wide range of standard audio sample rates and serial interface formats. Automatic sample-rate detection enables seamless wideband/narrowband voice-call handover.

The stereo headphone driver provides ground-referenced output, with noise levels as low as  $0.8 \mu\text{V}_{\text{RMS}}$  for hi-fi quality line or headphone output. The CS47L35 also features a mono bridge-tied load (BTL) earpiece output, mono 2.7-W Class D speaker driver, two channels of stereo PDM output, and an IEC-60958-3-compatible S/PDIF transmitter. A signal generator for controlling haptics devices is included; vibrate actuators can connect directly to the Class D speaker output, or via an external driver on the PDM output interface.

The CS47L35 supports up to six analog inputs, and up to four PDM digital inputs. Microphone activity detection with interrupt is available. A smart accessory interface supports most standard 3.5-mm accessories. Impedance sensing and measurement is provided for external accessory and push-button detection (Android™ headset specification compliant).

The CS47L35 is configured using the SLIMbus, SPI™, or I2C interfaces. The integrated FLL provides support for a wide range of system-clock frequencies. The device is powered from 1.8- and 1.2-V supplies. (A separate 4.2-V battery supply is typically required for the Class D speaker drivers). The power, clocking, and output driver architectures are designed to maximize battery life in voice, music, and standby modes. Low-power (10  $\mu\text{A}$ ) Sleep Mode is supported, with configurable wake-up events.

## Table of Contents

|                                                                                 |           |                                                                |            |
|---------------------------------------------------------------------------------|-----------|----------------------------------------------------------------|------------|
| <b>1 Pin Descriptions</b>                                                       | <b>4</b>  | 4.4 DSP Firmware Control                                       | 77         |
| 1.1 WLCSP Pinout                                                                | 4         | 4.5 DSP Peripheral Control                                     | 88         |
| 1.2 Pin Descriptions                                                            | 5         | 4.6 Digital Audio Interface                                    | 107        |
| <b>2 Typical Connection Diagram</b>                                             | <b>9</b>  | 4.7 Digital Audio Interface Control                            | 114        |
| <b>3 Characteristics and Specifications</b>                                     | <b>10</b> | 4.8 SLIMbus Interface                                          | 123        |
| Table 3-1. Parameter Definitions                                                | 10        | 4.9 SLIMbus Control Sequences                                  | 125        |
| Table 3-2. Absolute Maximum Ratings                                             | 10        | 4.10 SLIMbus Interface Control                                 | 128        |
| Table 3-3. Recommended Operating Conditions                                     | 11        | 4.11 Output Signal Path                                        | 134        |
| Table 3-4. Analog Input Signal Level—<br>IN1AL, IN1BL, IN1AR, IN1BR, IN2L, IN2R | 11        | 4.12 External Accessory Detection                              | 148        |
| Table 3-5. Analog Input Pin Characteristics                                     | 11        | 4.13 Low Power Sleep Configuration                             | 163        |
| Table 3-6. Analog Input Gain—Programmable Gain Amplifiers (PGAs)                | 11        | 4.14 General-Purpose I/O                                       | 164        |
| Table 3-7. Digital Input Signal Level—DMICDAT1, DMICDAT2                        | 12        | 4.15 Interrupts                                                | 172        |
| Table 3-8. Output Characteristics                                               | 12        | 4.16 Clocking and Sample Rates                                 | 186        |
| Table 3-9. Input/Output Path Characteristics                                    | 12        | 4.17 Control Interface                                         | 206        |
| Table 3-10. Digital Input/Output                                                | 15        | 4.18 Control-Write Sequencer                                   | 210        |
| Table 3-11. Miscellaneous Characteristics                                       | 16        | 4.19 Charge Pumps, Regulators, and Voltage Reference           | 218        |
| Table 3-12. Device Reset Thresholds                                             | 17        | 4.20 JTAG Interface                                            | 223        |
| Table 3-13. System Clock and Frequency-Locked Loop (FLL)                        | 17        | 4.21 Thermal, Short-Circuit, and Timer-Controlled Protection   | 223        |
| Table 3-14. Digital Microphone (DMIC) Interface Timing                          | 18        | 4.22 Power-On Reset (POR)                                      | 224        |
| Table 3-15. Digital Speaker (PDM) Interface Timing                              | 18        | 4.23 Hardware Reset, Software Reset, Wake-Up,<br>and Device ID | 226        |
| Table 3-16. Digital Audio Interface—Master Mode                                 | 19        | <b>5 Applications</b>                                          | <b>228</b> |
| Table 3-17. Digital Audio Interface—Slave Mode                                  | 20        | 5.1 Recommended External Components                            | 228        |
| Table 3-18. Digital Audio Interface Timing—TDM Mode                             | 20        | 5.2 Resets Summary                                             | 237        |
| Table 3-19. Control Interface Timing—Two-Wire (I <sup>2</sup> C) Mode           | 21        | 5.3 Output-Signal Drive-Strength Control                       | 237        |
| Table 3-20. Control Interface Timing—Four-Wire (SPI) Mode                       | 22        | 5.4 Digital Audio Interface Clocking Configurations            | 239        |
| Table 3-21. SLIMbus Interface Timing                                            | 23        | 5.5 PCB Layout Considerations                                  | 243        |
| Table 3-22. JTAG Interface Timing                                               | 24        | <b>6 Register Map</b>                                          | <b>243</b> |
| Table 3-23. Typical Power Consumption                                           | 25        | <b>7 Thermal Characteristics</b>                               | <b>297</b> |
| Table 3-24. Typical Signal Latency                                              | 25        | <b>8 Package Dimensions</b>                                    | <b>298</b> |
| <b>4 Functional Description</b>                                                 | <b>26</b> | <b>9 Ordering Information</b>                                  | <b>299</b> |
| 4.1 Overview                                                                    | 26        | <b>10 References</b>                                           | <b>299</b> |
| 4.2 Input Signal Path                                                           | 29        | <b>11 Revision History</b>                                     | <b>299</b> |
| 4.3 Digital Core                                                                | 39        |                                                                |            |

# 1 Pin Descriptions

## 1.1 WLCSP Pinout

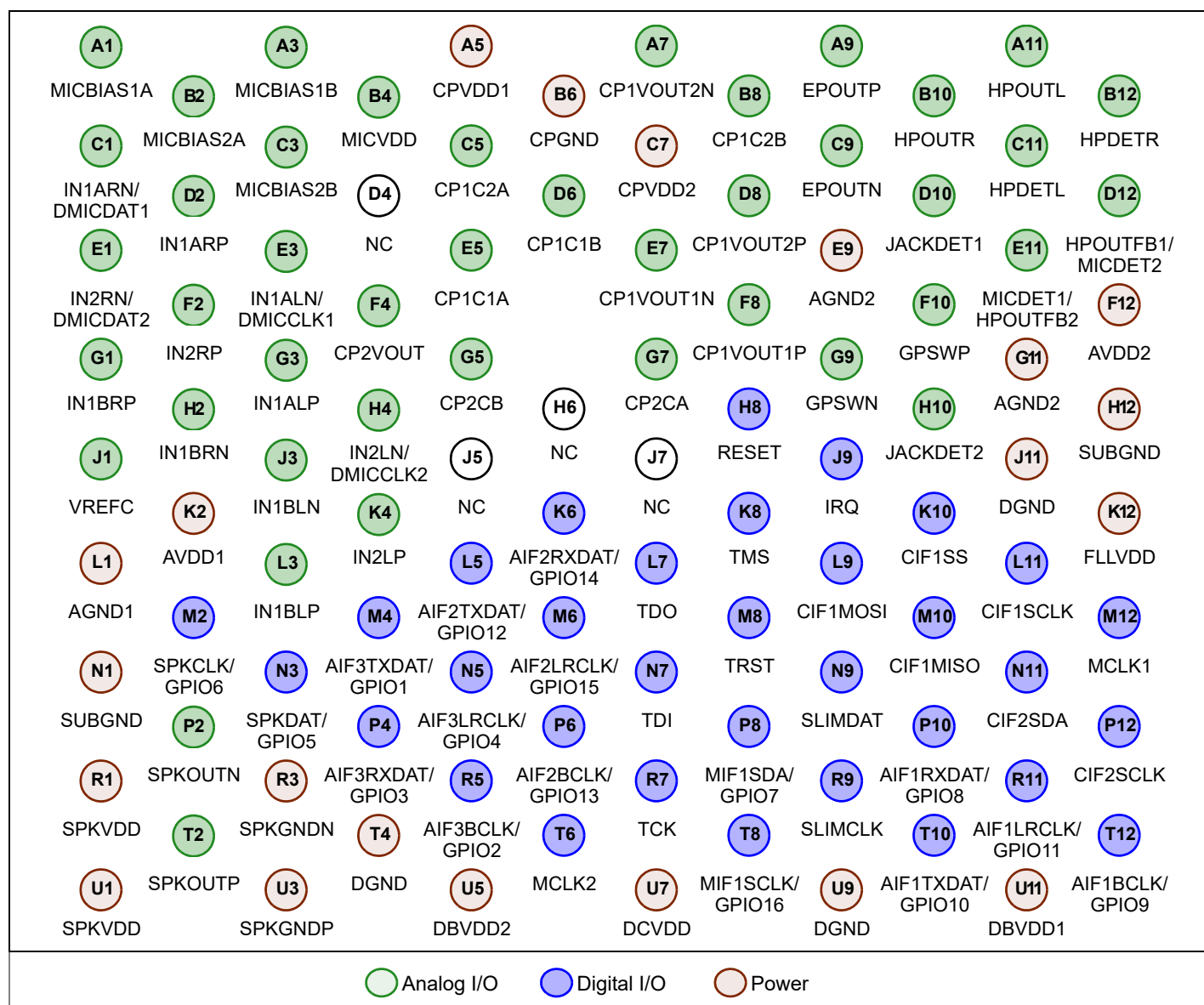


Figure 1-1. Top-Down (Through-Package) View—101-Ball WLCSP Package

## 1.2 Pin Descriptions

Table 1-1 describes each pin on the CS47L35. Note that pins that share a common name should be tied together on the printed circuit board (PCB). All digital output pins are CMOS outputs, unless otherwise stated.

**Table 1-1. Pin Descriptions**

| Name              | Ball # | Power Supply                    | I/O | Description                                                                                                                                                  |
|-------------------|--------|---------------------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Analog I/O</b> |        |                                 |     |                                                                                                                                                              |
| CP1C1A            | E5     | —                               | O   | Charge Pump 1 fly-back capacitor 1 pin                                                                                                                       |
| CP1C1B            | D6     | —                               | O   | Charge Pump 1 fly-back capacitor 1 pin                                                                                                                       |
| CP1C2A            | C5     | —                               | O   | Charge Pump 1 fly-back capacitor 2 pin                                                                                                                       |
| CP1C2B            | B8     | —                               | O   | Charge Pump 1 fly-back capacitor 2 pin                                                                                                                       |
| CP1VOUT1N         | E7     | —                               | O   | Charge Pump 1 negative output 1 decoupling pin                                                                                                               |
| CP1VOUT1P         | F8     | —                               | O   | Charge Pump 1 positive output 1 decoupling pin                                                                                                               |
| CP1VOUT2N         | A7     | —                               | O   | Charge Pump 1 negative output 2 decoupling pin                                                                                                               |
| CP1VOUT2P         | D8     | —                               | O   | Charge Pump 1 positive output 2 decoupling pin                                                                                                               |
| CP2CA             | G7     | —                               | O   | Charge Pump 2 fly-back capacitor pin                                                                                                                         |
| CP2CB             | G5     | —                               | O   | Charge Pump 2 fly-back capacitor pin                                                                                                                         |
| CP2VOUT           | F4     | —                               | O   | Charge Pump 2 output decoupling pin/supply for LDO2                                                                                                          |
| EPOUTN            | C9     | —                               | O   | Earpiece negative output                                                                                                                                     |
| EPOUTP            | A9     | —                               | O   | Earpiece positive output                                                                                                                                     |
| GPSWN             | G9     | —                               | I/O | General-purpose bidirectional switch contact                                                                                                                 |
| GPSWP             | F10    | —                               | I/O | General-purpose bidirectional switch contact                                                                                                                 |
| HPDETL            | C11    | —                               | I   | Headphone left (HPOUTL) sense input                                                                                                                          |
| HPDETR            | B12    | —                               | I   | Headphone right (HPOUTR) sense input                                                                                                                         |
| HPOUTFB1/MICDET2  | D12    | —                               | I   | HPOUTL and HPOUTR ground feedback pin 1/mic and accessory sense input 2                                                                                      |
| HPOUTL            | A11    | —                               | O   | Left headphone output                                                                                                                                        |
| HPOUTR            | B10    | —                               | O   | Right headphone output                                                                                                                                       |
| IN1ALN/DMICCLK1   | E3     | MICVDD or MICBIAS <sub>Nx</sub> | I/O | Left-channel negative differential mic/line input /DMIC Clock Output 1                                                                                       |
| IN1ALP            | G3     | MICVDD                          | I   | Left-channel single-ended mic/line input/left-channel positive differential mic/line input                                                                   |
| IN1ARN/DMICDAT1   | C1     | MICVDD or MICBIAS <sub>Nx</sub> | I   | Right-channel negative differential mic/line input/DMIC Data Input 1                                                                                         |
| IN1ARP            | D2     | MICVDD                          | I   | Right-channel single-ended mic/line input/right-channel positive differential mic/line input                                                                 |
| IN1BLN            | J3     | MICVDD                          | I   | Left-channel negative differential mic/line input. Also suitable for connection to external accessory interfaces.                                            |
| IN1BLP            | L3     | MICVDD                          | I   | Left-channel single-ended mic/line input/left-channel positive differential mic/line input. Also suitable for connection to external accessory interfaces.   |
| IN1BRN            | H2     | MICVDD                          | I   | Right-channel negative differential mic/line input. Also suitable for connection to external accessory interfaces.                                           |
| IN1BRP            | G1     | MICVDD                          | I   | Right-channel single-ended mic/line input/right-channel positive differential mic/line input. Also suitable for connection to external accessory interfaces. |
| IN2LN/DMICCLK2    | H4     | MICVDD or MICBIAS <sub>Nx</sub> | I/O | Left-channel negative differential mic/line input/DMIC Clock Output 2                                                                                        |

**Table 1-1. Pin Descriptions (Cont.)**

| Name               | Ball # | Power Supply                    | I/O | Description                                                                                                                    |
|--------------------|--------|---------------------------------|-----|--------------------------------------------------------------------------------------------------------------------------------|
| IN2LP              | K4     | MICVDD                          | I   | Left-channel single-ended mic/line input/left-channel positive differential mic/line input                                     |
| IN2RN/DMICDAT2     | E1     | MICVDD or MICBIAS <sub>Nx</sub> | I   | Right-channel negative differential mic/line input/DMIC Data Input 2                                                           |
| IN2RP              | F2     | MICVDD                          | I   | Right-channel single-ended mic/line input/right-channel positive differential mic/line input                                   |
| JACKDET1           | D10    | AVDD                            | I   | Jack detect input 1                                                                                                            |
| JACKDET2           | H10    | AVDD                            | I   | Jack detect input 2                                                                                                            |
| MICBIAS1A          | A1     | —                               | O   | Microphone bias 1A                                                                                                             |
| MICBIAS1B          | A3     | —                               | O   | Microphone bias 1B                                                                                                             |
| MICBIAS2A          | B2     | —                               | O   | Microphone bias 2A                                                                                                             |
| MICBIAS2B          | C3     | —                               | O   | Microphone bias 2B                                                                                                             |
| MICDET1/HPOUTFB2   | E11    | —                               | I   | Microphone and accessory sense input 1/HPOUTL and HPOUTR ground feedback pin 2                                                 |
| MICVDD             | B4     | —                               | O   | LDO2 output decoupling pin (generated internally by CS47L35). (Can also be used as reference/supply for external microphones.) |
| SPKOUTN            | P2     | —                               | O   | Speaker negative output                                                                                                        |
| SPKOUTP            | T2     | —                               | O   | Speaker positive output                                                                                                        |
| VREFC              | J1     | —                               | O   | Band-gap reference external capacitor connection                                                                               |
| <b>Digital I/O</b> |        |                                 |     |                                                                                                                                |
| AIF1BCLK/GPIO9     | T12    | DBVDD1                          | I/O | Audio interface 1 bit clock/GPIO. GPIO output is selectable CMOS or open drain; BCLK output is CMOS.                           |
| AIF1LRCLK/GPIO11   | R11    | DBVDD1                          | I/O | Audio interface 1 left/right clock/GPIO. GPIO output is selectable CMOS or open drain; LRCLK output is CMOS.                   |
| AIF1RXDAT/GPIO8    | P10    | DBVDD1                          | I/O | Audio interface 1 RX digital audio data/GPIO. GPIO output is selectable CMOS or open drain.                                    |
| AIF1TXDAT/GPIO10   | T10    | DBVDD1                          | I/O | Audio interface 1 TX digital audio data/GPIO. GPIO output is selectable CMOS or open drain; TXDAT output is CMOS.              |
| AIF2BCLK/GPIO13    | P6     | DBVDD2                          | I/O | Audio interface 2 bit clock/GPIO. GPIO output is selectable CMOS or open drain; BCLK output is CMOS.                           |
| AIF2LRCLK/GPIO15   | M6     | DBVDD2                          | I/O | Audio interface 2 left/right clock/GPIO. GPIO output is selectable CMOS or open drain; LRCLK output is CMOS.                   |
| AIF2RXDAT/GPIO14   | K6     | DBVDD2                          | I/O | Audio interface 2 RX digital audio data/GPIO. GPIO output is selectable CMOS or open drain.                                    |
| AIF2TXDAT/GPIO12   | L5     | DBVDD2                          | I/O | Audio interface 2 TX digital audio data/GPIO. GPIO output is selectable CMOS or open drain; TXDAT output is CMOS.              |
| AIF3BCLK/GPIO2     | R5     | DBVDD2                          | I/O | Audio interface 3 bit clock/GPIO. GPIO output is selectable CMOS or open drain; BCLK output is CMOS.                           |
| AIF3LRCLK/GPIO4    | N5     | DBVDD2                          | I/O | Audio interface 3 left/right clock/GPIO. GPIO output is selectable CMOS or open drain; LRCLK output is CMOS.                   |
| AIF3RXDAT/GPIO3    | P4     | DBVDD2                          | I/O | Audio interface 3 RX digital audio data/GPIO. GPIO output is selectable CMOS or open drain.                                    |
| AIF3TXDAT/GPIO1    | M4     | DBVDD2                          | I/O | Audio interface 3 TX digital audio data/GPIO. GPIO output is selectable CMOS or open drain; TXDAT output is CMOS.              |
| CIF1MISO           | M10    | DBVDD1                          | O   | Control interface 1 (SPI) Master In Slave Out data. The CIFMISO is high impedance if CIF1SS is not asserted.                   |
| CIF1MOSI           | L9     | DBVDD1                          | I   | Control interface 1 (SPI) Master Out Slave In data                                                                             |
| CIF1SCLK           | L11    | DBVDD1                          | I   | Control interface 1 (SPI) clock input                                                                                          |
| CIF1SS             | K10    | DBVDD1                          | I   | Control interface 1 (SPI) slave select (SS)                                                                                    |
| CIF2SCLK           | P12    | DBVDD1                          | I   | Control interface 2 (I <sup>2</sup> C) clock input                                                                             |

**Table 1-1. Pin Descriptions (Cont.)**

| Name                      | Ball #  | Power Supply | I/O | Description                                                                                                                               |
|---------------------------|---------|--------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------|
| CIF2SDA                   | N11     | DBVDD1       | I/O | Control interface 2 (I <sup>2</sup> C) data input and output. The SDA output is open drain.                                               |
| $\overline{\text{IRQ}}$   | J9      | DBVDD1       | O   | Interrupt request output (default is active low). The pin configuration is selectable CMOS or open drain.                                 |
| MCLK1                     | M12     | DBVDD1       | I   | Master clock 1                                                                                                                            |
| MCLK2                     | T6      | DBVDD2       | I   | Master clock 2                                                                                                                            |
| MIF1SCLK/GPIO16           | T8      | DBVDD1       | I/O | Master (I <sup>2</sup> C) Interface 1 clock output/GPIO. GPIO output is selectable CMOS or open drain; SCLK output is open drain.         |
| MIF1SDA/GPIO7             | P8      | DBVDD1       | I/O | Master (I <sup>2</sup> C) Interface 1 data input and output/GPIO. GPIO output is selectable CMOS or open drain; SDA output is open drain. |
| $\overline{\text{RESET}}$ | H8      | DBVDD1       | I   | Digital reset input (active low)                                                                                                          |
| SLIMCLK                   | R9      | DBVDD1       | I/O | SLIMbus clock I/O                                                                                                                         |
| SLIMDAT                   | N9      | DBVDD1       | I/O | SLIMbus data I/O                                                                                                                          |
| SPKCLK/GPIO6              | M2      | DBVDD2       | I/O | Digital speaker (PDM) 1 clock output/GPIO. GPIO output is selectable CMOS or open drain; SPKCLK output is CMOS.                           |
| SPKDAT/GPIO5              | N3      | DBVDD2       | I/O | Digital speaker (PDM) 1 data output/GPIO. GPIO output is selectable CMOS or open drain; SPKDAT output is CMOS.                            |
| TCK                       | R7      | DBVDD2       | I   | JTAG clock input. Internal pull-down holds this pin at Logic 0 for normal operation.                                                      |
| TDI                       | N7      | DBVDD2       | I   | JTAG data input. Internal pull-down holds this pin at Logic 0 for normal operation.                                                       |
| TDO                       | L7      | DBVDD2       | O   | JTAG data output                                                                                                                          |
| TMS                       | K8      | DBVDD2       | I   | JTAG mode select input. Internal pull-down holds this pin at Logic 0 for normal operation.                                                |
| TRST                      | M8      | DBVDD2       | I   | JTAG test access port reset (active low). Internal pull-down holds this pin at Logic 0 for normal operation.                              |
| <b>Supply</b>             |         |              |     |                                                                                                                                           |
| AGND1                     | L1      | —            | —   | Analog ground (return path for AVDD1)                                                                                                     |
| AGND2                     | E9, G11 | —            | —   | Analog ground (return path for AVDD2)                                                                                                     |
| AVDD1                     | K2      | —            | —   | Analog supply                                                                                                                             |
| AVDD2                     | F12     | —            | —   | Analog supply                                                                                                                             |
| CPGND                     | B6      | —            | —   | Charge pump ground (return path for CPVDD1, CPVDD2)                                                                                       |
| CPVDD1                    | A5      | —            | —   | Supply for Charge Pump 1 and Charge Pump 2                                                                                                |
| CPVDD2                    | C7      | —            | —   | Secondary supply for Charge Pump 1                                                                                                        |
| DBVDD1                    | U11     | —            | —   | Digital buffer (I/O) supply<br>(core functions, AIF1, CIF1, CIF2, SLIMbus, MIF1)                                                          |
| DBVDD2                    | U5      | —            | —   | Digital buffer (I/O) supply<br>(AIF2, AIF3, PDM, MCLK2, JTAG)                                                                             |

**Table 1-1. Pin Descriptions (Cont.)**

| Name              | Ball #         | Power Supply | I/O | Description                                                 |
|-------------------|----------------|--------------|-----|-------------------------------------------------------------|
| DCVDD             | U7             | —            | —   | Digital core supply                                         |
| DGND              | J11, T4, U9    | —            | —   | Digital ground (return path for DCVDD and DBVDDn)           |
| FLLVDD            | K12            | —            | —   | Analog supply (FLL1)                                        |
| SPKGNDN           | R3             | —            | —   | Speaker driver ground (return path for SPKVDD) <sup>1</sup> |
| SPKGNDP           | U3             | —            | —   | Speaker driver ground (return path for SPKVDD) <sup>1</sup> |
| SPKVDD            | R1, U1         | —            | —   | Speaker driver supply                                       |
| SUBGND            | H12, N1        | —            | —   | Substrate ground                                            |
| <b>No Connect</b> |                |              |     |                                                             |
| NC                | D4, H6, J5, J7 | —            | —   | No connection                                               |

1. Separate P/N ground connections are provided for the Class D speaker output, which provides flexible support for current monitoring and output-protection circuits. If this option is not used, these ground connections should be tied together on the PCB.

## 2 Typical Connection Diagram

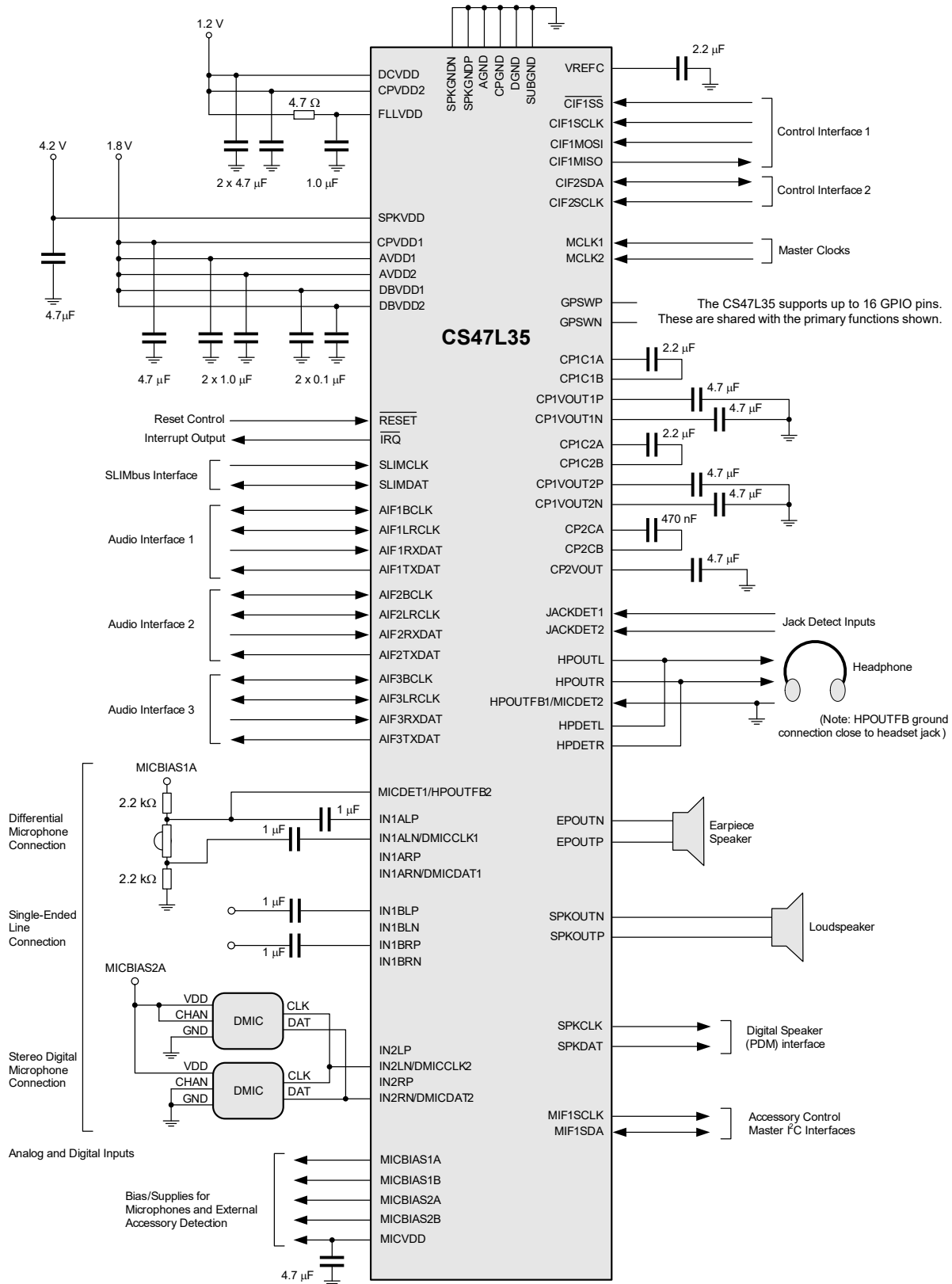


Figure 2-1. Typical Connection Diagram

## 3 Characteristics and Specifications

Table 3-1 defines parameters as they are characterized in this section.

**Table 3-1. Parameter Definitions**

| Parameter                                    | Definition                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Channel separation                           | Left-to-right and right-to-left channel separation is the difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel. |
| Common-mode rejection ratio (CMRR)           | The ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.                                                                                                                                                                                                                                                                     |
| Dynamic range (DR)                           | A measure of the difference between the maximum full scale output signal and the sum of all harmonic distortion products plus noise, with a low-level input signal applied. Typically, an input signal level 60 dB below full scale is used.                                                                                                                                                                   |
| Power-supply rejection ratio (PSRR)          | The ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.                                                                                                                                                                                                                                                   |
| Signal-to-noise ratio (SNR)                  | A measure of the difference in level between the maximum full scale output signal and the output with no input signal applied.                                                                                                                                                                                                                                                                                 |
| Total harmonic distortion (THD)              | The ratio of the RMS sum of the harmonic distortion products in the specified bandwidth <sup>1</sup> relative to the RMS amplitude of the fundamental (i.e., test frequency) output.                                                                                                                                                                                                                           |
| Total harmonic distortion plus noise (THD+N) | The ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth <sup>1</sup> relative to the RMS amplitude of the fundamental (i.e., test frequency) output.                                                                                                                                                                                                                |

1. All performance measurements are specified with a 20-kHz low-pass brick-wall filter and, where noted, an A-weighted filter. The low-pass filter removes out-of-band noise.

**Table 3-2. Absolute Maximum Ratings**

Absolute maximum ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under electrical characteristics at the test conditions specified.

| Parameter                                                      | Symbol                                                                                                                                                                 | Minimum                                                                                                                    | Maximum                                                                                                |
|----------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------|
| Supply voltages                                                | DCVDD <sup>[1]</sup> , FLLVDD <sup>[1]</sup><br>CPVDD1, CPVDD2<br>DBVDD1, DBVDD2, AVDD <sup>[2]</sup> , MICVDD<br>SPKVDD                                               | –0.3 V<br>–0.3 V<br>–0.3 V<br>–0.3 V                                                                                       | 1.6 V<br>2.5 V<br>5.0 V<br>6.0 V                                                                       |
| Voltage range digital inputs<br>DBVDD1 domain<br>DBVDD2 domain | —<br>—                                                                                                                                                                 | SUBGND – 0.3 V<br>SUBGND – 0.3 V                                                                                           | DBVDD1 + 0.3 V<br>DBVDD2 + 0.3 V                                                                       |
| Voltage range analog inputs                                    | IN1Axx, IN2xx<br>IN1Bxx<br>HPOUTFB <sub>n</sub> <sup>3</sup><br>MICDET <sub>n</sub> <sup>3</sup><br>JACKDET1, HPDETL, HPDETR<br>JACKDET2 <sup>[4]</sup> , GPSWP, GPSWN | SUBGND – 0.3 V<br>SUBGND – 0.9 V<br>SUBGND – 0.3 V<br>SUBGND – 0.3 V<br>CP1VOUT2N – 0.3 V <sup>[5]</sup><br>SUBGND – 0.3 V | MICVDD + 0.3 V<br>MICVDD + 0.3 V<br>SUBGND + 0.3 V<br>MICVDD + 0.3 V<br>AVDD + 0.3 V<br>MICVDD + 0.3 V |
| Ground                                                         | AGND <sup>6</sup> , DGND, CPGND, SPKGND                                                                                                                                | SUBGND – 0.3 V                                                                                                             | SUBGND + 0.3 V                                                                                         |
| Operating temperature range                                    | T <sub>A</sub>                                                                                                                                                         | –40°C                                                                                                                      | +85°C                                                                                                  |
| Operating junction temperature                                 | T <sub>J</sub>                                                                                                                                                         | –40°C                                                                                                                      | +125°C                                                                                                 |
| Storage temperature after soldering                            | —                                                                                                                                                                      | –65°C                                                                                                                      | +150°C                                                                                                 |



ESD-sensitive device. The CS47L35 is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device. This device is qualified to current JEDEC ESD standards.

1. The DCVDD and FLLVDD pins should be tied together. The associated power domain is referred to as DCVDD.
2. The AVDD1 and AVDD2 pins should be tied together. The associated power domain is referred to as AVDD.
3. The HPOUTFB<sub>n</sub> and MICDET<sub>n</sub> functions share common pins. The absolute maximum rating varies according to the applicable function of each pin.
4. If AVDD > MICVDD (e.g., if LDO2 is disabled), the maximum JACKDET2 voltage is AVDD + 0.3 V.
5. CP1VOUT2N is an internal supply, generated by the CS47L35 charge pump (CP1). Its voltage can vary between CPGND and –CPVDD1.
6. The AGND1 and AGND2 pins should be tied together. The associated ground domain is referred to as AGND.

**Table 3-3. Recommended Operating Conditions**

| Parameter                                      | Symbol                            | Minimum | Typical | Maximum | Units |
|------------------------------------------------|-----------------------------------|---------|---------|---------|-------|
| Digital supply range <sup>1</sup> Core and FLL | DCVDD [2], FLLVDD [3]             | 1.14    | 1.2     | 1.26    | V     |
| Digital supply range I/O                       | DBVDD1, DBVDD2                    | 1.71    | —       | 3.6 [4] | V     |
| Charge pump supply range CPVDD1                | CPVDD1                            | 1.71    | 1.8     | 1.89    | V     |
| CPVDD2                                         | CPVDD2                            | 1.14    | 1.2     | 1.26    | V     |
| Speaker supply range                           | SPKVDD                            | 2.4     | —       | 5.5     | V     |
| Analog supply range <sup>5,6</sup>             | AVDD                              | 1.71    | 1.8     | 1.89    | V     |
| Mic bias supply <sup>7</sup>                   | MICVDD                            | 0.9     | 2.5     | 3.78    | V     |
| Ground <sup>8</sup>                            | DGND, AGND, CPGND, SPKGND, SUBGND | —       | 0       | —       | V     |
| Power supply rise time <sup>9,10</sup>         | DCVDD                             | 10      | —       | 2000    | μs    |
|                                                | All other supplies                | 10      | —       | —       | μs    |
| Operating temperature range                    | T <sub>A</sub>                    | –40     | —       | 85      | °C    |

**Note:** There are no power sequencing requirements; the supplies may be enabled and disabled in any order.

- The DCVDD and FLLVDD pins should be tied together. The associated power domain is referred to as DCVDD.
- Sleep mode is supported for when DCVDD is below the limits noted, provided that AVDD and DBVDD1 are present.
- It is recommended to connect a 4.7-Ω resistor in series with the FLLVDD pin connection. Note that the minimum voltage limit applies at the supply end of the 4.7-Ω resistor in this case.
- If the SLIMbus interface is enabled, the maximum DBVDD1 voltage is 1.98 V.
- The AVDD1 and AVDD2 pins should be tied together. The associated power domain is referred to as AVDD.
- The AGND1 and AGND2 pins should be tied together. The associated ground domain is referred to as AGND.
- An internal charge pump and LDO (powered by CPVDD1) provide the mic bias supply; the MICVDD pin must not be connected to an external supply.
- The impedance between DGND, AGND, and SUBGND must not exceed 0.1 Ω.  
The impedance between SPKGND and SUBGND must not exceed 0.2 Ω.
- If the DCVDD rise time exceeds 2 ms, RESET must be asserted (low) during the rise and held asserted until after DCVDD is within the recommended operating limits.
- The specified minimum power supply rise times assume a minimum decoupling capacitance of 100 nF per pin. However, Cirrus Logic strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed. The specified minimum power supply rise times also assume a maximum PCB inductance of 10 nH between decoupling capacitor and pin.

**Table 3-4. Analog Input Signal Level—IN1AL, IN1BL, IN1AR, IN1BR, IN2L, IN2R**

Test conditions (unless specified otherwise): AVDD = 1.8V; with the exception of the condition noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

| Parameter                                                                           | Minimum | Typical | Maximum | Units                   |
|-------------------------------------------------------------------------------------|---------|---------|---------|-------------------------|
| Full-scale input signal level (0 dBFS output) Single-ended PGA input, 0 dB PGA gain | —       | 0.5     | —       | V <sub>RMS</sub><br>dBV |
| Differential PGA input, 0 dB PGA gain                                               | —       | –6      | —       | V <sub>RMS</sub><br>dBV |
|                                                                                     | —       | 1       | —       | V <sub>RMS</sub><br>dBV |
|                                                                                     | —       | 0       | —       | V <sub>RMS</sub><br>dBV |

**Notes:**

- The full-scale input signal level is also the maximum analog input level, before clipping occurs.
- The full-scale input signal level changes in proportion with AVDD. For differential input, it is calculated as AVDD/1.8.
- A 1.0V<sub>RMS</sub> differential signal equates to 0.5V<sub>RMS</sub>/–6dBV per input.
- A sinusoidal input signal is assumed.

**Table 3-5. Analog Input Pin Characteristics**

Test conditions (unless specified otherwise): T<sub>A</sub> = +25°C; with the exception of the condition noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

| Parameter                                                      | Minimum | Typical | Maximum | Units |
|----------------------------------------------------------------|---------|---------|---------|-------|
| Input resistance Single-ended PGA input, All PGA gain settings | 9       | 10.5    | —       | kΩ    |
| Differential PGA input, All PGA gain settings                  | 18      | 21      | —       | kΩ    |
| Input capacitance                                              | —       | —       | 5       | pF    |

**Table 3-6. Analog Input Gain—Programmable Gain Amplifiers (PGAs)**

The following electrical characteristics are valid across the full range of recommended operating conditions.

| Parameter                   | Minimum              | Typical | Maximum | Units |
|-----------------------------|----------------------|---------|---------|-------|
| Minimum programmable gain   | —                    | 0       | —       | dB    |
| Maximum programmable gain   | —                    | 31      | —       | dB    |
| Programmable gain step size | Guaranteed monotonic | 1       | —       | dB    |

**Table 3-7. Digital Input Signal Level—DMICDAT1, DMICDAT2**

The following electrical characteristics are valid across the full range of recommended operating conditions.

| Parameter                                     | Minimum   | Typical | Max | Units |      |
|-----------------------------------------------|-----------|---------|-----|-------|------|
| Full-scale input signal level (0 dBFS output) | 0 dB gain | —       | –6  | —     | dBFS |

**Note:** The DMIC input signal level is measured in dBFS, where 0 dBFS is a signal level equal to the full-scale range (FSR) of the PDM input. The FSR is defined as the amplitude of a 1-kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively—this is the largest 1-kHz sine wave that can fit in the digital output range without clipping.

**Table 3-8. Output Characteristics**

The following electrical characteristics are valid across the full range of recommended operating conditions.

| Parameter                                              |                                      | Minimum                                        | Typical | Max | Units |      |
|--------------------------------------------------------|--------------------------------------|------------------------------------------------|---------|-----|-------|------|
| Line/headphone/earpiece output driver (HPOUTL, HPOUTR) | Load resistance                      | Normal operation, Single-Ended Mode            | 6       | —   | —     | Ω    |
|                                                        |                                      | Normal operation, Differential (BTL) Mode      | 15      | —   | —     | Ω    |
|                                                        |                                      | Device survival with load applied indefinitely | 0       | —   | —     | Ω    |
|                                                        | Load capacitance                     | Single-Ended Mode                              | —       | —   | 500   | pF   |
|                                                        |                                      | Differential (BTL) Mode                        | —       | —   | 200   | pF   |
| Earpiece output driver (EPOUT)                         | Load resistance                      | Normal operation                               | 15      | —   | —     | Ω    |
|                                                        |                                      | Device survival with load applied indefinitely | 0       | —   | —     | Ω    |
|                                                        | Load capacitance                     |                                                | —       | —   | 200   | pF   |
| Speaker output driver (SPKOUTP+SPKOUTN)                | Load resistance                      | Normal operation                               | 4       | —   | —     | Ω    |
|                                                        |                                      | Device survival with load applied indefinitely | 0       | —   | —     | Ω    |
|                                                        | Load capacitance                     |                                                | —       | —   | 200   | pF   |
| Digital speaker output (SPKDAT)                        | Full-scale output level <sup>1</sup> | 0 dBFS digital core output, 0 dB gain          | —       | –6  | —     | dBFS |

1. The digital output signal level is measured in dBFS, where 0 dBFS is a signal level equal to the full-scale range (FSR) of the PDM output. The FSR is defined as the amplitude of a 1-kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively—this is the largest 1-kHz sine wave that can fit in the digital output range without clipping.

**Table 3-9. Input/Output Path Characteristics**

Test conditions (unless specified otherwise): DBVDD1 = DBVDD2 = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 2.5 V (powered from internal LDO); SPKVDD = 4.2 V; T<sub>A</sub> = +25°C; 1 kHz sinusoid signal; F<sub>s</sub> = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

| Parameter                                                        |                                                   | Min                                 | Typ | Max | Units |                   |
|------------------------------------------------------------------|---------------------------------------------------|-------------------------------------|-----|-----|-------|-------------------|
| Line/headphone/earpiece output driver (HPOUTL, HPOUTR)           | DC offset at Load                                 | Single-ended mode                   | —   | 50  | —     | μV                |
|                                                                  |                                                   | Differential (BTL) mode             | —   | 75  | —     | μV                |
| Earpiece output driver (EPOUT+EPOUTN)                            | DC offset at Load                                 |                                     | —   | 75  | —     | μV                |
| Speaker output driver (SPKOUTP+SPKOUTN)                          | DC offset at Load                                 |                                     | —   | 300 | —     | μV                |
|                                                                  | SPKVDD leakage current                            |                                     | —   | 1   | —     | μA                |
| Analog input paths (INnL, INnR) to ADC (Differential Input Mode) | SNR (A-weighted), defined in Table 3-1            | 48 kHz sample rate                  | 91  | 101 | —     | dB                |
|                                                                  |                                                   | 16 kHz sample rate (wideband voice) | —   | 105 | —     | dB                |
|                                                                  | THD, defined in Table 3-1                         | –1 dBV input                        | —   | –87 | —     | dB                |
|                                                                  | THD+N, defined in Table 3-1                       | –1 dBV input                        | —   | –86 | –76   | dB                |
|                                                                  | Channel separation (L/R), defined in Table 3-1    | 100 Hz to 10 kHz                    | —   | 100 | —     | dB                |
|                                                                  | Input-referred noise floor                        | A-weighted, PGA gain = +20 dB       | —   | 3.2 | —     | μV <sub>RMS</sub> |
|                                                                  | CMRR, defined in Table 3-1                        | PGA gain = +30 dB                   | —   | 80  | —     | dB                |
|                                                                  |                                                   | PGA gain = 0 dB                     | —   | 70  | —     | dB                |
|                                                                  | PSRR (DBVDDn, CPVDD1, AVDD), defined in Table 3-1 | 100 mV (peak-peak) 217 Hz           | —   | 90  | —     | dB                |
|                                                                  |                                                   | 100 mV (peak-peak) 10 kHz           | —   | 75  | —     | dB                |
| PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1               | 100 mV (peak-peak) 217 Hz                         | —                                   | 95  | —   | dB    |                   |
|                                                                  | 100 mV (peak-peak) 10 kHz                         | —                                   | 90  | —   | dB    |                   |
| PSRR (SPKVDD), defined in Table 3-1                              | 100 mV (peak-peak) 217 Hz                         | —                                   | 100 | —   | dB    |                   |
|                                                                  | 100 mV (peak-peak) 10 kHz                         | —                                   | 95  | —   | dB    |                   |

**Table 3-9. Input/Output Path Characteristics (Cont.)**

Test conditions (unless specified otherwise): DBVDD1 = DBVDD2 = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 2.5 V (powered from internal LDO); SPKVDD = 4.2 V;  $T_A = +25^\circ\text{C}$ ; 1 kHz sinusoid signal;  $F_s = 48\text{ kHz}$ ; PGA gain = 0 dB, 24-bit audio data.

| Parameter                                                          |                                                    | Min | Typ | Max | Units                      |
|--------------------------------------------------------------------|----------------------------------------------------|-----|-----|-----|----------------------------|
| Analog input paths (INnLP, INnRP) to ADC (Single-Ended Input Mode) | SNR (A-weighted), defined in Table 3-1             | 89  | 99  | —   | dB                         |
|                                                                    | 48-kHz sample rate                                 | —   | 102 | —   | dB                         |
|                                                                    | 16-kHz sample rate (wideband voice)                | —   | 102 | —   | dB                         |
|                                                                    | THD, defined in Table 3-1                          | —   | −86 | —   | dB                         |
|                                                                    | −7dB V input                                       | —   | −85 | −75 | dB                         |
|                                                                    | THD+N, defined in Table 3-1                        | —   | −85 | −75 | dB                         |
|                                                                    | Channel separation (L/R), defined in Table 3-1     | —   | 100 | —   | dB                         |
|                                                                    | 100 Hz to 10 kHz                                   | —   | 100 | —   | dB                         |
|                                                                    | Input-referred noise floor                         | —   | 4   | —   | $\mu\text{V}_{\text{RMS}}$ |
| DAC to line output (HPOUTL, HPOUTR; Load = 10 k $\Omega$ , 50 pF)  | A-weighted, PGA gain = +20 dB                      | —   | 77  | —   | dB                         |
|                                                                    | PSRR (DBVDDn, CPVDD1, AVDD), defined in Table 3-1  | —   | 50  | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 217 Hz                          | —   | 95  | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 10 kHz                          | —   | 65  | —   | dB                         |
|                                                                    | PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1 | —   | 100 | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 217 Hz                          | —   | 80  | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 10 kHz                          | —   | 80  | —   | dB                         |
|                                                                    | PSRR (SPKVDD), defined in Table 3-1                | —   | 100 | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 10 kHz                          | —   | 80  | —   | dB                         |
| DAC to headphone output (HPOUTL, HPOUTR; $R_L = 32\ \Omega$ )      | Full-scale output signal level                     | —   | 1   | —   | $V_{\text{RMS}}$           |
|                                                                    | 0 dBFS input                                       | —   | 0   | —   | dBV                        |
|                                                                    | SNR, defined in Table 3-1                          | —   | 122 | —   | dB                         |
|                                                                    | A-weighted, output signal = 1 $V_{\text{RMS}}$     | —   | 122 | —   | dB                         |
|                                                                    | Dynamic range, defined in Table 3-1                | 105 | 115 | —   | dB                         |
|                                                                    | A-weighted, −60 dBFS input                         | —   | −95 | —   | dB                         |
|                                                                    | THD, defined in Table 3-1                          | —   | −95 | —   | dB                         |
|                                                                    | 0 dBFS input                                       | —   | −93 | −83 | dB                         |
|                                                                    | THD+N, defined in Table 3-1                        | —   | −93 | −83 | dB                         |
|                                                                    | 0 dBFS input                                       | —   | −93 | −83 | dB                         |
|                                                                    | Channel separation (L/R), defined in Table 3-1     | —   | 100 | —   | dB                         |
|                                                                    | 100 Hz to 10 kHz                                   | —   | 100 | —   | dB                         |
|                                                                    | Output noise floor                                 | —   | 0.8 | —   | $\mu\text{V}_{\text{RMS}}$ |
|                                                                    | A-weighted                                         | —   | 0.8 | —   | $\mu\text{V}_{\text{RMS}}$ |
| DAC to headphone output (HPOUTL, HPOUTR; $R_L = 16\ \Omega$ )      | PSRR (DBVDDn, CPVDD1, AVDD), defined in Table 3-1  | —   | 100 | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 217 Hz                          | —   | 73  | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 10 kHz                          | —   | 73  | —   | dB                         |
|                                                                    | PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1 | —   | 105 | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 217 Hz                          | —   | 80  | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 10 kHz                          | —   | 80  | —   | dB                         |
|                                                                    | PSRR (SPKVDD), defined in Table 3-1                | —   | 110 | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 217 Hz                          | —   | 100 | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 10 kHz                          | —   | 100 | —   | dB                         |
|                                                                    | Maximum output power                               | —   | 30  | —   | mW                         |
|                                                                    | 0.1% THD+N                                         | —   | 30  | —   | mW                         |
|                                                                    | SNR, defined in Table 3-1                          | —   | 122 | —   | dB                         |
|                                                                    | A-weighted, output signal = 1 $V_{\text{RMS}}$     | —   | 122 | —   | dB                         |
|                                                                    | Dynamic range, defined in Table 3-1                | 105 | 115 | —   | dB                         |
|                                                                    | A-weighted, −60 dBFS input                         | —   | −93 | —   | dB                         |
| DAC to headphone output (HPOUTL, HPOUTR; $R_L = 16\ \Omega$ )      | THD, defined in Table 3-1                          | —   | −93 | —   | dB                         |
|                                                                    | $P_O = 20\text{ mW}$                               | —   | −91 | —   | dB                         |
|                                                                    | THD+N, defined in Table 3-1                        | —   | −91 | —   | dB                         |
|                                                                    | $P_O = 20\text{ mW}$                               | —   | −91 | —   | dB                         |
|                                                                    | THD, defined in Table 3-1                          | —   | −92 | —   | dB                         |
|                                                                    | $P_O = 2\text{ mW}$                                | —   | −92 | —   | dB                         |
|                                                                    | THD+N, defined in Table 3-1                        | —   | −90 | −80 | dB                         |
|                                                                    | $P_O = 2\text{ mW}$                                | —   | −90 | −80 | dB                         |
|                                                                    | Channel separation (L/R), defined in Table 3-1     | —   | 100 | —   | dB                         |
|                                                                    | 100 Hz to 10 kHz                                   | —   | 100 | —   | dB                         |
|                                                                    | Output noise floor                                 | —   | 0.8 | —   | $\mu\text{V}_{\text{RMS}}$ |
|                                                                    | A-weighted                                         | —   | 0.8 | —   | $\mu\text{V}_{\text{RMS}}$ |
|                                                                    | PSRR (DBVDDn, CPVDD1, AVDD), defined in Table 3-1  | —   | 100 | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 217 Hz                          | —   | 73  | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 10 kHz                          | —   | 73  | —   | dB                         |
| DAC to headphone output (HPOUTL, HPOUTR; $R_L = 16\ \Omega$ )      | PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1 | —   | 105 | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 217 Hz                          | —   | 80  | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 10 kHz                          | —   | 80  | —   | dB                         |
|                                                                    | PSRR (SPKVDD), defined in Table 3-1                | —   | 110 | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 217 Hz                          | —   | 100 | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 10 kHz                          | —   | 100 | —   | dB                         |
|                                                                    | Maximum output power                               | —   | 39  | —   | mW                         |
|                                                                    | 0.1% THD+N                                         | —   | 39  | —   | mW                         |
|                                                                    | SNR, defined in Table 3-1                          | —   | 122 | —   | dB                         |
|                                                                    | A-weighted, output signal = 1 $V_{\text{RMS}}$     | —   | 122 | —   | dB                         |
|                                                                    | Dynamic range, defined in Table 3-1                | 105 | 115 | —   | dB                         |
|                                                                    | A-weighted, −60 dBFS input                         | —   | −89 | —   | dB                         |
|                                                                    | THD, defined in Table 3-1                          | —   | −89 | —   | dB                         |
|                                                                    | $P_O = 20\text{ mW}$                               | —   | −88 | —   | dB                         |
|                                                                    | THD+N, defined in Table 3-1                        | —   | −88 | —   | dB                         |
|                                                                    | $P_O = 20\text{ mW}$                               | —   | −88 | —   | dB                         |
|                                                                    | THD, defined in Table 3-1                          | —   | −92 | —   | dB                         |
|                                                                    | $P_O = 2\text{ mW}$                                | —   | −92 | —   | dB                         |
|                                                                    | THD+N, defined in Table 3-1                        | —   | −90 | −80 | dB                         |
|                                                                    | $P_O = 2\text{ mW}$                                | —   | −90 | −80 | dB                         |
|                                                                    | Channel separation (L/R), defined in Table 3-1     | —   | 100 | —   | dB                         |
|                                                                    | 100 Hz to 10 kHz                                   | —   | 100 | —   | dB                         |
|                                                                    | Output noise floor                                 | —   | 0.8 | —   | $\mu\text{V}_{\text{RMS}}$ |
|                                                                    | A-weighted                                         | —   | 0.8 | —   | $\mu\text{V}_{\text{RMS}}$ |
|                                                                    | PSRR (DBVDDn, CPVDD1, AVDD), defined in Table 3-1  | —   | 100 | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 217 Hz                          | —   | 73  | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 10 kHz                          | —   | 73  | —   | dB                         |
|                                                                    | PSRR (DCVDD, FLLVDD, CPVDD2), defined in Table 3-1 | —   | 105 | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 217 Hz                          | —   | 80  | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 10 kHz                          | —   | 80  | —   | dB                         |
|                                                                    | PSRR (SPKVDD), defined in Table 3-1                | —   | 110 | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 217 Hz                          | —   | 100 | —   | dB                         |
|                                                                    | 100 mV (peak-peak) 10 kHz                          | —   | 100 | —   | dB                         |

**Table 3-9. Input/Output Path Characteristics (Cont.)**

Test conditions (unless specified otherwise): DBVDD1 = DBVDD2 = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 2.5 V (powered from internal LDO); SPKVDD = 4.2 V;  $T_A = +25^\circ\text{C}$ ; 1 kHz sinusoid signal;  $F_s = 48\text{ kHz}$ ; PGA gain = 0 dB, 24-bit audio data.

| Parameter                                                               |                                                                         |                                                        | Min                                                                              | Typ         | Max               | Units             |
|-------------------------------------------------------------------------|-------------------------------------------------------------------------|--------------------------------------------------------|----------------------------------------------------------------------------------|-------------|-------------------|-------------------|
| DAC to earpiece output<br>(EPOUTP+EPOUTN,<br>R <sub>L</sub> = 32 Ω BTL) | Maximum output power                                                    | 0.1% THD+N                                             | —                                                                                | 99          | —                 | mW                |
|                                                                         | SNR, defined in Table 3-1                                               | A-weighted, output signal = 1.41 V <sub>RMS</sub>      | —                                                                                | 127         | —                 | dB                |
|                                                                         | Dynamic range, defined in Table 3-1                                     | A-weighted, -60 dBFS input                             | 108                                                                              | 118         | —                 | dB                |
|                                                                         | THD, defined in Table 3-1                                               | P <sub>O</sub> = 75 mW                                 | —                                                                                | -94         | —                 | dB                |
|                                                                         | THD+N, defined in Table 3-1                                             | P <sub>O</sub> = 75 mW                                 | —                                                                                | -92         | —                 | dB                |
|                                                                         | THD, defined in Table 3-1                                               | P <sub>O</sub> = 5 mW                                  | —                                                                                | -94         | —                 | dB                |
|                                                                         | THD+N, defined in Table 3-1                                             | P <sub>O</sub> = 5 mW                                  | —                                                                                | -92         | -82               | dB                |
|                                                                         | Output noise floor                                                      | A-weighted                                             | —                                                                                | 0.6         | —                 | μV <sub>RMS</sub> |
|                                                                         | PSRR (DBVDD <sub>n</sub> , CPVDD1, AVDD),<br>defined in Table 3-1       | 100 mV (peak-peak) 217 Hz<br>100 mV (peak-peak) 10 kHz | —<br>—                                                                           | 125<br>90   | —<br>—            | dB<br>dB          |
|                                                                         | PSRR (DCVDD, FLLVDD, CPVDD2),<br>defined in Table 3-1                   | 100 mV (peak-peak) 217 Hz<br>100 mV (peak-peak) 10 kHz | —<br>—                                                                           | 125<br>90   | —<br>—            | dB<br>dB          |
|                                                                         | PSRR (SPKVDD),<br>defined in Table 3-1                                  | 100 mV (peak-peak) 217 Hz<br>100 mV (peak-peak) 10 kHz | —<br>—                                                                           | 125<br>110  | —<br>—            | dB<br>dB          |
|                                                                         | DAC to earpiece output<br>(EPOUTP+EPOUTN,<br>R <sub>L</sub> = 16 Ω BTL) | Maximum output power                                   | 0.1% THD+N                                                                       | —           | 110               | —                 |
| SNR, defined in Table 3-1                                               |                                                                         | A-weighted, output signal = 1.41 V <sub>RMS</sub>      | —                                                                                | 127         | —                 | dB                |
| Dynamic range, defined in Table 3-1                                     |                                                                         | A-weighted, -60 dBFS input                             | 108                                                                              | 118         | —                 | dB                |
| THD, defined in Table 3-1                                               |                                                                         | P <sub>O</sub> = 75 mW                                 | —                                                                                | -87         | —                 | dB                |
| THD+N, defined in Table 3-1                                             |                                                                         | P <sub>O</sub> = 75 mW                                 | —                                                                                | -85         | —                 | dB                |
| THD, defined in Table 3-1                                               |                                                                         | P <sub>O</sub> = 5 mW                                  | —                                                                                | -92         | —                 | dB                |
| THD+N, defined in Table 3-1                                             |                                                                         | P <sub>O</sub> = 5 mW                                  | —                                                                                | -90         | -80               | dB                |
| Output noise floor                                                      |                                                                         | A-weighted                                             | —                                                                                | 0.6         | —                 | μV <sub>RMS</sub> |
| PSRR (DBVDD <sub>n</sub> , CPVDD1, AVDD),<br>defined in Table 3-1       |                                                                         | 100 mV (peak-peak) 217 Hz<br>100 mV (peak-peak) 10 kHz | —<br>—                                                                           | 125<br>90   | —<br>—            | dB<br>dB          |
| PSRR (DCVDD, FLLVDD, CPVDD2),<br>defined in Table 3-1                   |                                                                         | 100 mV (peak-peak) 217 Hz<br>100 mV (peak-peak) 10 kHz | —<br>—                                                                           | 125<br>90   | —<br>—            | dB<br>dB          |
| PSRR (SPKVDD), defined in Table 3-1                                     |                                                                         | 100 mV (peak-peak) 217 Hz<br>100 mV (peak-peak) 10 kHz | —<br>—                                                                           | 125<br>110  | —<br>—            | dB<br>dB          |
| DAC to speaker output<br>(SPKOUTP+SPKOUTN,<br>Load = 8 Ω, 22 μH, BTL)   |                                                                         | Maximum output power                                   | SPKVDD = 5.0 V, 1% THD+N<br>SPKVDD = 4.2 V, 1% THD+N<br>SPKVDD = 3.6 V, 1% THD+N | —<br>—<br>— | 1.4<br>1.0<br>0.7 | —<br>—<br>—       |
|                                                                         | SNR, defined in Table 3-1                                               | A-weighted, output signal = 2.83 V <sub>RMS</sub>      | —                                                                                | 127         | —                 | dB                |
|                                                                         | Dynamic range, defined in Table 3-1                                     | A-weighted, -60 dBFS input                             | 92                                                                               | 102         | —                 | dB                |
|                                                                         | THD, defined in Table 3-1                                               | P <sub>O</sub> = 1.0 W                                 | —                                                                                | -40         | —                 | dB                |
|                                                                         | THD+N, defined in Table 3-1                                             | P <sub>O</sub> = 1.0 W                                 | —                                                                                | -40         | —                 | dB                |
|                                                                         | THD, defined in Table 3-1                                               | P <sub>O</sub> = 0.5 W                                 | —                                                                                | -70         | —                 | dB                |
|                                                                         | THD+N, defined in Table 3-1                                             | P <sub>O</sub> = 0.5 W                                 | —                                                                                | -70         | -60               | dB                |
|                                                                         | Output noise floor                                                      | A-weighted                                             | —                                                                                | 1.3         | —                 | μV <sub>RMS</sub> |
|                                                                         | PSRR (DBVDD <sub>n</sub> , CPVDD1, AVDD),<br>defined in Table 3-1       | 100 mV (peak-peak) 217 Hz<br>100 mV (peak-peak) 10 kHz | —<br>—                                                                           | 125<br>90   | —<br>—            | dB<br>dB          |
|                                                                         | PSRR (DCVDD, FLLVDD, CPVDD2),<br>defined in Table 3-1                   | 100 mV (peak-peak) 217 Hz<br>100 mV (peak-peak) 10 kHz | —<br>—                                                                           | 125<br>105  | —<br>—            | dB<br>dB          |
|                                                                         | PSRR (SPKVDD), defined in Table 3-1                                     | 100 mV (peak-peak) 217 Hz<br>100 mV (peak-peak) 10 kHz | —<br>—                                                                           | 120<br>90   | —<br>—            | dB<br>dB          |

**Table 3-9. Input/Output Path Characteristics (Cont.)**

Test conditions (unless specified otherwise): DBVDD1 = DBVDD2 = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 2.5 V (powered from internal LDO); SPKVDD = 4.2 V;  $T_A = +25^\circ\text{C}$ ; 1 kHz sinusoid signal;  $F_s = 48\text{ kHz}$ ; PGA gain = 0 dB, 24-bit audio data.

| Parameter                                                                                 |                                                           |                                                   | Min | Typ | Max | Units                      |
|-------------------------------------------------------------------------------------------|-----------------------------------------------------------|---------------------------------------------------|-----|-----|-----|----------------------------|
| DAC to speaker output<br>(SPKOUTP+SPKOUTN,<br>Load = 4 $\Omega$ , 15 $\mu\text{H}$ , BTL) | Maximum output power                                      | SPKVDD = 5.0 V, 1% THD+N                          | —   | 2.7 | —   | W                          |
|                                                                                           |                                                           | SPKVDD = 4.2 V, 1% THD+N                          | —   | 1.9 | —   | W                          |
|                                                                                           |                                                           | SPKVDD = 3.6 V, 1% THD+N                          | —   | 1.4 | —   | W                          |
|                                                                                           | SNR, defined in Table 3-1                                 | A-weighted, output signal = 2.83 $V_{\text{RMS}}$ | —   | 127 | —   | dB                         |
|                                                                                           | Dynamic range, defined in Table 3-1                       | A-weighted, -60 dBFS input                        | —   | 102 | —   | dB                         |
|                                                                                           | THD, defined in Table 3-1                                 | $P_O = 1.0\text{ W}$                              | —   | -71 | —   | dB                         |
|                                                                                           | THD+N, defined in Table 3-1                               | $P_O = 1.0\text{ W}$                              | —   | -70 | —   | dB                         |
|                                                                                           | THD, defined in Table 3-1                                 | $P_O = 0.5\text{ W}$                              | —   | -71 | —   | dB                         |
|                                                                                           | THD+N, defined in Table 3-1                               | $P_O = 0.5\text{ W}$                              | —   | -70 | —   | dB                         |
|                                                                                           | Output noise floor                                        | A-weighted                                        | —   | 1.3 | —   | $\mu\text{V}_{\text{RMS}}$ |
|                                                                                           | PSRR (DBVDD $_n$ , CPVDD1, AVDD),<br>defined in Table 3-1 | 100 mV (peak-peak) 217 Hz                         | —   | 125 | —   | dB                         |
|                                                                                           |                                                           | 100 mV (peak-peak) 10 kHz                         | —   | 90  | —   | dB                         |
|                                                                                           | PSRR (DCVDD, FLLVDD, CPVDD2),<br>defined in Table 3-1     | 100 mV (peak-peak) 217 Hz                         | —   | 125 | —   | dB                         |
|                                                                                           |                                                           | 100 mV (peak-peak) 10 kHz                         | —   | 105 | —   | dB                         |
|                                                                                           | PSRR (SPKVDD),<br>defined in Table 3-1                    | 100 mV (peak-peak) 217 Hz                         | —   | 120 | —   | dB                         |
|                                                                                           |                                                           | 100 mV (peak-peak) 10 kHz                         | —   | 90  | —   | dB                         |

**Table 3-10. Digital Input/Output**

The following electrical characteristics are valid across the full range of recommended operating conditions.

| Parameter                                                           |                                                        |                                                        | Minimum                      | Typical | Maximum                      | Units            |
|---------------------------------------------------------------------|--------------------------------------------------------|--------------------------------------------------------|------------------------------|---------|------------------------------|------------------|
| Digital I/O (except<br>DMICDAT1/2 and<br>DMICCLK1/2) <sup>1,3</sup> | Input HIGH level                                       | $V_{\text{DBVDD}n} = 1.71\text{--}1.98\text{ V}$       | $0.75 \times \text{DBVDD}n$  | —       | —                            | V                |
|                                                                     |                                                        | $V_{\text{DBVDD}n} = 2.5\text{ V} \pm 10\%$            | $0.8 \times \text{DBVDD}n$   | —       | —                            | V                |
|                                                                     |                                                        | $V_{\text{DBVDD}n} = 3.3\text{ V} \pm 10\%$            | $0.7 \times \text{DBVDD}n$   | —       | —                            | V                |
|                                                                     | Input LOW level                                        | $V_{\text{DBVDD}n} = 1.71\text{--}1.98\text{ V}$       | —                            | —       | $0.3 \times \text{DBVDD}n$   | V                |
|                                                                     |                                                        | $V_{\text{DBVDD}n} = 2.5\text{ V} \pm 10\%$            | —                            | —       | $0.25 \times \text{DBVDD}n$  | V                |
|                                                                     |                                                        | $V_{\text{DBVDD}n} = 3.3\text{ V} \pm 10\%$            | —                            | —       | $0.2 \times \text{DBVDD}n$   | V                |
|                                                                     | Output HIGH level<br>( $I_{\text{OH}} = 1\text{ mA}$ ) | $V_{\text{DBVDD}n} = 1.71\text{--}1.98\text{ V}$       | $0.75 \times \text{DBVDD}n$  | —       | —                            | V                |
|                                                                     |                                                        | $V_{\text{DBVDD}n} = 2.5\text{ V} \pm 10\%$            | $0.65 \times \text{DBVDD}n$  | —       | —                            | V                |
|                                                                     |                                                        | $V_{\text{DBVDD}n} = 3.3\text{ V} \pm 10\%$            | $0.7 \times \text{DBVDD}n$   | —       | —                            | V                |
|                                                                     | Output LOW level<br>( $I_{\text{OL}} = 1\text{ mA}$ )  | $V_{\text{DBVDD}n} = 1.71\text{--}1.98\text{ V}$       | —                            | —       | $0.25 \times \text{DBVDD}n$  | V                |
| DMIC I/O<br>(DMICDAT1/2 and<br>DMICCLK1/2) <sup>2,3</sup>           | Input capacitance                                      |                                                        | —                            | —       | 5                            | pF               |
|                                                                     | Input leakage                                          |                                                        | -1                           | —       | 1                            | $\mu\text{A}$    |
|                                                                     | Pull-up/pull-down resistance (where applicable)        |                                                        | 35                           | —       | 55                           | $\text{k}\Omega$ |
|                                                                     | DMICDAT $_n$ input HIGH Level                          |                                                        | $0.65 \times V_{\text{SUP}}$ | —       | —                            | V                |
|                                                                     | DMICDAT $_n$ input LOW Level                           |                                                        | —                            | —       | $0.35 \times V_{\text{SUP}}$ | V                |
|                                                                     | DMICCLK $_n$ output HIGH Level                         | $I_{\text{OH}} = 1\text{ mA}$                          | $0.8 \times V_{\text{SUP}}$  | —       | —                            | V                |
|                                                                     | DMICCLK $_n$ output LOW Level                          | $I_{\text{OL}} = -1\text{ mA}$                         | —                            | —       | $0.2 \times V_{\text{SUP}}$  | V                |
|                                                                     | Input capacitance                                      |                                                        | —                            | 25      | —                            | pF               |
|                                                                     | Input leakage                                          |                                                        | -1                           | —       | 1                            | $\mu\text{A}$    |
|                                                                     | GPIO $_n$                                              | Clock output frequency GPIO pin as OPCLK or FLL output | —                            | —       | 50                           | MHz              |

1. Digital I/O is referenced to DBVDD1 or DBVDD2.

2. DMICDAT1/2 and DMICCLK1/2 are referenced to a selectable supply,  $V_{\text{SUP}}$ , according to the IN $_n$ \_DMIC\_SUP fields.

3. Note that digital input pins should not be left unconnected or floating.

**Table 3-11. Miscellaneous Characteristics**

Test conditions (unless specified otherwise): DBVDD1 = DBVDD2 = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = 2.5 V (powered from internal LDO); SPKVDD = 4.2 V;  $T_A$  = +25°C; 1 kHz sinusoid signal;  $F_s$  = 48 kHz; PGA gain = 0 dB, 24-bit audio data.

| Parameter                                                                 |                                                                                                                                             |                                                                                                                         | Min                                                                                                                                                          | Typ                                                                         | Max                        | Units                            |                       |          |
|---------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|----------------------------|----------------------------------|-----------------------|----------|
| Microphone bias (MICBIAS1A, MICBIAS1B, MICBIAS2A, MICBIAS2B) <sup>1</sup> | Minimum Bias Voltage <sup>2</sup>                                                                                                           |                                                                                                                         | —                                                                                                                                                            | 1.5                                                                         | —                          | V                                |                       |          |
|                                                                           | Maximum Bias Voltage                                                                                                                        |                                                                                                                         | —                                                                                                                                                            | 2.8                                                                         | —                          | V                                |                       |          |
|                                                                           | Bias Voltage output step size                                                                                                               |                                                                                                                         | —                                                                                                                                                            | 0.1                                                                         | —                          | V                                |                       |          |
|                                                                           | Bias Voltage accuracy                                                                                                                       |                                                                                                                         | −5%                                                                                                                                                          | —                                                                           | +5%                        | V                                |                       |          |
|                                                                           | Bias Current <sup>3</sup>                                                                                                                   | Regulator Mode (MICBn_BYPASS = 0), V <sub>MICVDD</sub> − V <sub>MICBIAS</sub> >200 mV<br>Bypass Mode (MICBn_BYPASS = 1) | —                                                                                                                                                            | —                                                                           | 2.4<br>5.0                 | mA<br>mA                         |                       |          |
|                                                                           | Output Noise Density                                                                                                                        | Regulator Mode (MICBn_BYPASS = 0), MICBn_LVL = 0x4,<br>Load current = 1 mA, Measured at 1 kHz                           | —                                                                                                                                                            | 45                                                                          | —                          | nV/√Hz                           |                       |          |
|                                                                           | Integrated noise voltage                                                                                                                    | Regulator Mode (MICBn_BYPASS = 0), MICBn_LVL = 0x4,<br>Load current = 1 mA, 100 Hz to 7 kHz, A-weighted                 | —                                                                                                                                                            | 4                                                                           | —                          | μV <sub>RMS</sub>                |                       |          |
|                                                                           | PSRR (DBVDDn, CPVDD1, AVDD), defined in <a href="#">Table 3-1</a>                                                                           | 100 mV (peak-peak) 217 Hz<br>100 mV (peak-peak) 10 kHz                                                                  | —<br>—                                                                                                                                                       | 105<br>85                                                                   | —<br>—                     | dB<br>dB                         |                       |          |
|                                                                           | PSRR (DCVDD, FLLVDD, CPVDD2), defined in <a href="#">Table 3-1</a>                                                                          | 100 mV (peak-peak) 217 Hz<br>100 mV (peak-peak) 10 kHz                                                                  | —<br>—                                                                                                                                                       | 110<br>90                                                                   | —<br>—                     | dB<br>dB                         |                       |          |
|                                                                           | PSRR (SPKVDD), defined in <a href="#">Table 3-1</a>                                                                                         | 100 mV (peak-peak) 217 Hz<br>100 mV (peak-peak) 10 kHz                                                                  | —<br>—                                                                                                                                                       | 105<br>90                                                                   | —<br>—                     | dB<br>dB                         |                       |          |
| Load capacitance <sup>3</sup>                                             | Regulator Mode (MICBn_BYPASS = 0), MICBn_EXT_CAP = 0<br>Regulator Mode (MICBn_BYPASS = 0), MICBn_EXT_CAP = 1                                | —<br>0.1                                                                                                                | —<br>1.0                                                                                                                                                     | 50<br>10                                                                    | pF<br>μF                   |                                  |                       |          |
| Output discharge resistance                                               |                                                                                                                                             | MICBnx_ENA = 0, MICBnx_DISCH = 1                                                                                        |                                                                                                                                                              | —                                                                           | 2                          | —                                | kΩ                    |          |
| General-purpose switch <sup>4</sup>                                       | Switch resistance                                                                                                                           |                                                                                                                         | Switch closed, I = 1 mA                                                                                                                                      |                                                                             | —                          | 25                               | 40                    | Ω        |
|                                                                           |                                                                                                                                             |                                                                                                                         | Switch open                                                                                                                                                  |                                                                             | —                          | 100                              | —                     | MΩ       |
| External Accessory Detect                                                 | Load impedance detection range:<br>Detection via HPDETL (ACCDDET_MODE = 001)<br>or HPDETR (ACCDDET_MODE = 010)                              |                                                                                                                         | HP_IMPEDANCE_RANGE = 00<br>HP_IMPEDANCE_RANGE = 01<br>HP_IMPEDANCE_RANGE = 10<br>HP_IMPEDANCE_RANGE = 11                                                     | 4<br>8<br>100<br>1000                                                       | —<br>—<br>—<br>—           | 30<br>100<br>1000<br>10000       | Ω<br>Ω<br>Ω<br>Ω      |          |
|                                                                           | Load impedance detection range:<br>Detection via MICDET1 or MICDET2 pin (ACCDDET_MODE = 100)                                                |                                                                                                                         |                                                                                                                                                              | 400                                                                         | —                          | 6000                             | Ω                     |          |
|                                                                           | Load impedance detection accuracy<br>(HP_DACVAL, ACCDET_MODE = 001 or 010)                                                                  |                                                                                                                         | HP_IMPEDANCE_RANGE = 01 or 10<br>HP_IMPEDANCE_RANGE = 00 or 11                                                                                               | −5<br>−10                                                                   | —<br>—                     | +5<br>+10                        | %<br>%                |          |
|                                                                           | Load impedance detection accuracy (HP_LVL, ACCDET_MODE = 001, 010, or 100)                                                                  |                                                                                                                         |                                                                                                                                                              | −20                                                                         | —                          | +20                              | %                     |          |
|                                                                           | Load impedance detection range—Detection via MICDET1 or<br>MICDET2 pin (ACCDDET_MODE = 000); 2.2 kΩ (±2%) MICBIAS<br>resistor. <sup>5</sup> |                                                                                                                         | for MICD_LVL[0] = 1<br>for MICD_LVL[1] = 1<br>for MICD_LVL[2] = 1<br>for MICD_LVL[3] = 1<br>for MICD_LVL[8] = 1                                              | 0<br>110<br>210<br>360<br>1000                                              | —<br>—<br>—<br>—<br>—      | 70<br>180<br>290<br>680<br>30000 | Ω<br>Ω<br>Ω<br>Ω<br>Ω |          |
|                                                                           | Jack-detection input threshold voltage<br>(JACKDETn)                                                                                        |                                                                                                                         | Detection on JACKDET1, Jack insertion<br>Detection on JACKDET1, Jack removal<br>Detection on JACKDET2, Jack insertion<br>Detection on JACKDET2, Jack removal | —<br>—<br>—<br>—                                                            | 0.9<br>1.65<br>0.27<br>0.9 | —<br>—<br>—<br>—                 | V<br>V<br>V<br>V      |          |
|                                                                           | Pull-up resistance (JACKDETn)                                                                                                               |                                                                                                                         |                                                                                                                                                              | —                                                                           | 1                          | —                                | MΩ                    |          |
|                                                                           | MICVDD Charge Pump and Regulator (CP2 and LDO2)                                                                                             | Output voltage                                                                                                          |                                                                                                                                                              |                                                                             | 0.9                        | 2.7                              | 3.3                   | V        |
|                                                                           |                                                                                                                                             | Programmable output voltage step size                                                                                   |                                                                                                                                                              | LDO2_VSEL = 0x00–0x14 (0.9–1.4V )<br>LDO2_VSEL = 0x14 to 0x27 (1.4 V–3.3 V) | —<br>—                     | 25<br>100                        | —<br>—                | mV<br>mV |
| Maximum output current                                                    |                                                                                                                                             |                                                                                                                         | —                                                                                                                                                            | 8                                                                           | —                          | mA                               |                       |          |
| Start-up time                                                             |                                                                                                                                             | 4.7 μF on MICVDD                                                                                                        | —                                                                                                                                                            | 1.5                                                                         | 2.5                        | ms                               |                       |          |
| Frequency-Lock ed Loop (FLL1)                                             | Output frequency                                                                                                                            |                                                                                                                         | FLL output as SYSCLK source<br>FLL output as DSPCLK source                                                                                                   | 90<br>135                                                                   | —<br>—                     | 98.3<br>150                      | MHz<br>MHz            |          |
|                                                                           | Lock Time                                                                                                                                   |                                                                                                                         | F <sub>FREF</sub> = 32 kHz, F <sub>OUT</sub> (DSPCLK source) = 147.456 MHz<br>F <sub>FREF</sub> = 12 MHz, F <sub>OUT</sub> (DSPCLK source) = 147.456 MHz     | —<br>—                                                                      | 10<br>1                    | —<br>—                           | ms<br>ms              |          |
| RESET pin input                                                           | RESET input pulse width <sup>6</sup>                                                                                                        |                                                                                                                         |                                                                                                                                                              | 1                                                                           | —                          | —                                | μs                    |          |

1. No capacitor on MICBIASn. In Regulator Mode, it is required that  $V_{MICVDD} - V_{MICBIAS} > 200$  mV.

2. Regulator Mode (MICBn\_BYPASS = 0), Load current ≤ 1.0 mA.

3. Bias current and load capacitance specifications are per MICBIAS generator (MICBIAS1 or MICBIAS2).

4. The GPSWN pin voltage must not exceed GPSWP + 0.3 V. See Table 3-2 for voltage limits applicable to the GPSWP and GPSWN pins.

5. These characteristics assume no other component is connected to MICDETn.

6. To trigger a hardware reset, the RESET input must be asserted for longer than this duration.

**Table 3-12. Device Reset Thresholds**

The following electrical characteristics are valid across the full range of recommended operating conditions.

| Parameter              | Symbol                      | Minimum | Typical | Maximum | Units |
|------------------------|-----------------------------|---------|---------|---------|-------|
| AVDD reset threshold   | V <sub>AVDD</sub> rising    | —       | —       | 1.66    | V     |
|                        | V <sub>AVDD</sub> falling   | 1.06    | —       | 1.44    | V     |
| DCVDD reset threshold  | V <sub>DCVDD</sub> rising   | —       | —       | 1.04    | V     |
|                        | V <sub>DCVDD</sub> falling  | 0.49    | —       | 0.66    | V     |
| DBVDD1 Reset threshold | V <sub>DBVDD1</sub> rising  | —       | —       | 1.66    | V     |
|                        | V <sub>DBVDD1</sub> falling | 1.06    | —       | 1.44    | V     |

**Note:** The reset thresholds are derived from simulations only, across all operational and process corners. Device performance is not assured outside the voltage ranges defined in [Table 3-3](#).

**Table 3-13. System Clock and Frequency-Locked Loop (FLL)**

The following timing information is valid across the full range of recommended operating conditions.

| Parameter                                       |                                  |                                            | Minimum | Typical | Maximum | Units |
|-------------------------------------------------|----------------------------------|--------------------------------------------|---------|---------|---------|-------|
| Master clock timing (MCLK1, MCLK2) <sup>1</sup> | MCLK cycle time                  | MCLK as input to FLL, FLL1_REFCLK_DIV = 00 | 74      | —       | —       | ns    |
|                                                 |                                  | MCLK as input to FLL, FLL1_REFCLK_DIV = 01 | 37      | —       | —       | ns    |
|                                                 |                                  | MCLK as input to FLL, FLL1_REFCLK_DIV = 10 | 18      | —       | —       | ns    |
|                                                 |                                  | MCLK as input to FLL, FLL1_REFCLK_DIV = 11 | 12.5    | —       | —       | ns    |
|                                                 |                                  | MCLK as direct SYSCLK source               | 40      | —       | —       | ns    |
|                                                 | MCLK duty cycle                  | MCLK as input to FLL                       | 80:20   | —       | 20:80   | %     |
|                                                 |                                  | MCLK as direct SYSCLK source               | 60:40   | —       | 40:60   | %     |
| Frequency-locked loop (FLL1)                    | FLL input frequency              | FLL1_REFCLK_DIV = 00                       | 0.032   | —       | 13.5    | MHz   |
|                                                 |                                  | FLL1_REFCLK_DIV = 01                       | 0.064   | —       | 27      | MHz   |
|                                                 |                                  | FLL1_REFCLK_DIV = 11                       | 0.128   | —       | 54      | MHz   |
|                                                 |                                  | FLL1_REFCLK_DIV = 11                       | 0.256   | —       | 80      | MHz   |
|                                                 | FLL synchronizer input frequency | FLL1_SYNCCLK_DIV = 00                      | 0.032   | —       | 13.5    | MHz   |
|                                                 |                                  | FLL1_SYNCCLK_DIV = 01                      | 0.064   | —       | 27      | MHz   |
|                                                 |                                  | FLL1_SYNCCLK_DIV = 10                      | 0.128   | —       | 54      | MHz   |
|                                                 |                                  | FLL1_SYNCCLK_DIV = 11                      | 0.256   | —       | 80      | MHz   |
| Internal clocking                               | SYSCLK frequency                 | SYSCLK_FREQ = 000, SYSCLK_FRAC = 0         | –1%     | 6.144   | +1%     | MHz   |
|                                                 |                                  | SYSCLK_FREQ = 000, SYSCLK_FRAC = 1         | –1%     | 5.6448  | +1%     | MHz   |
|                                                 |                                  | SYSCLK_FREQ = 001, SYSCLK_FRAC = 0         | –1%     | 12.288  | +1%     | MHz   |
|                                                 |                                  | SYSCLK_FREQ = 001, SYSCLK_FRAC = 1         | –1%     | 11.2896 | +1%     | MHz   |
|                                                 |                                  | SYSCLK_FREQ = 010, SYSCLK_FRAC = 0         | –1%     | 24.576  | +1%     | MHz   |
|                                                 |                                  | SYSCLK_FREQ = 010, SYSCLK_FRAC = 1         | –1%     | 22.5792 | +1%     | MHz   |
|                                                 |                                  | SYSCLK_FREQ = 011, SYSCLK_FRAC = 0         | –1%     | 49.152  | +1%     | MHz   |
|                                                 |                                  | SYSCLK_FREQ = 011, SYSCLK_FRAC = 1         | –1%     | 45.1584 | +1%     | MHz   |
|                                                 |                                  | SYSCLK_FREQ = 100, SYSCLK_FRAC = 0         | –1%     | 98.304  | +1%     | MHz   |
|                                                 |                                  | SYSCLK_FREQ = 100, SYSCLK_FRAC = 1         | –1%     | 90.3168 | +1%     | MHz   |
|                                                 | DSPCLK frequency                 |                                            | 5       | —       | 150     | MHz   |

<sup>1</sup>. If MCLK1 or MCLK2 is selected as a source for SYSCLK (either directly or via the FLL), the frequency must be within 1% of the SYSCLK\_FREQ setting.

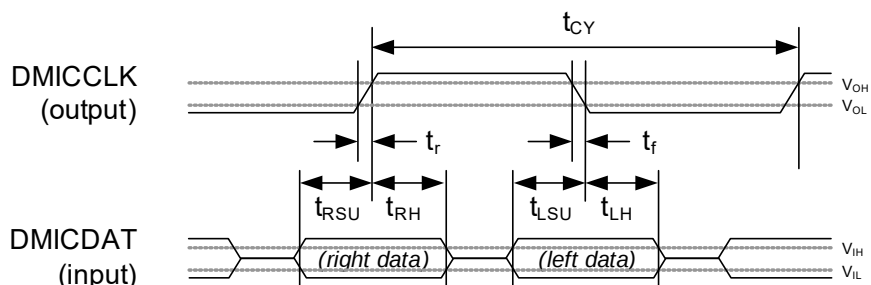
**Table 3-14. Digital Microphone (DMIC) Interface Timing**

The following timing information is valid across the full range of recommended operating conditions.

| Parameter <sup>1</sup>                                 | Symbol     | Minimum | Typical | Maximum | Units |
|--------------------------------------------------------|------------|---------|---------|---------|-------|
| DMICCLK $n$ cycle time                                 | $t_{CY}$   | 160     | 163     | 1432    | ns    |
| DMICCLK $n$ duty cycle                                 | —          | 45      | —       | 55      | %     |
| DMICCLK $n$ rise/fall time (25-pF load, 1.8-V supply)  | $t_r, t_f$ | 5       | —       | 30      | ns    |
| DMICDAT $n$ (Left) setup time to falling DMICCLK edge  | $t_{LSU}$  | 15      | —       | —       | ns    |
| DMICDAT $n$ (Left) hold time from falling DMICCLK edge | $t_{LH}$   | 0       | —       | —       | ns    |
| DMICDAT $n$ (Right) setup time to rising DMICCLK edge  | $t_{RSU}$  | 15      | —       | —       | ns    |
| DMICDAT $n$ (Right) hold time from rising DMICCLK edge | $t_{RH}$   | 0       | —       | —       | ns    |

**Note:** The voltage reference for the IN1 and IN2 DMIC interfaces is selectable, using the IN $n$ \_DMIC\_SUP fields—each interface may be referenced to MICVDD, MICBIAS1B, MICBIAS2A, or MICBIAS2B levels.

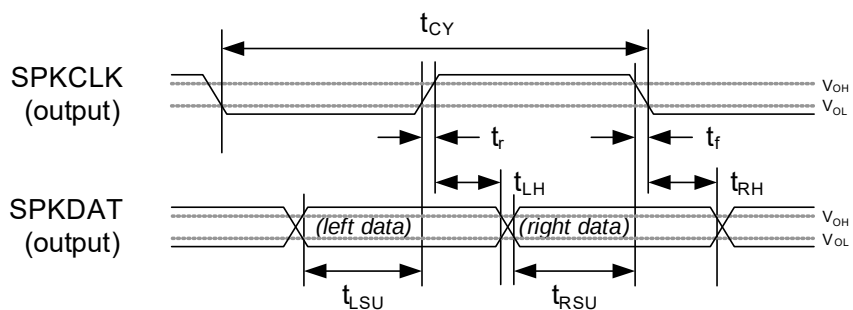
#### 1. DMIC interface timing

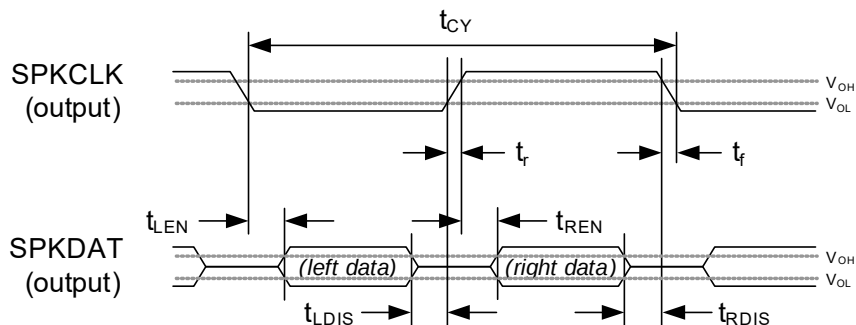

**Table 3-15. Digital Speaker (PDM) Interface Timing**

The following timing information is valid across the full range of recommended operating conditions.

| Parameter           |                                                           | Symbol     | Minimum | Typical | Maximum | Units |
|---------------------|-----------------------------------------------------------|------------|---------|---------|---------|-------|
| Mode A <sup>1</sup> | SPKCLK cycle time                                         | $t_{CY}$   | 160     | 163     | 358     | ns    |
|                     | SPKCLK duty cycle                                         | —          | 45      | —       | 55      | %     |
|                     | SPKCLK rise/fall time (25-pF load)                        | $t_r, t_f$ | 2       | —       | 8       | ns    |
|                     | SPKDAT set-up time to SPKCLK rising edge (left channel)   | $t_{LSU}$  | 30      | —       | —       | ns    |
|                     | SPKDAT hold time from SPKCLK rising edge (left channel)   | $t_{LH}$   | 30      | —       | —       | ns    |
|                     | SPKDAT set-up time to SPKCLK falling edge (right channel) | $t_{RSU}$  | 30      | —       | —       | ns    |
|                     | SPKDAT hold time from SPKCLK falling edge (right channel) | $t_{RH}$   | 30      | —       | —       | ns    |
| Mode B <sup>2</sup> | SPKCLK cycle time                                         | $t_{CY}$   | 160     | 163     | 358     | ns    |
|                     | SPKCLK duty cycle                                         | —          | 45      | —       | 55      | %     |
|                     | SPKCLK rise/fall time (25-pF load)                        | $t_r, t_f$ | 2       | —       | 8       | ns    |
|                     | SPKDAT enable from SPKCLK rising edge (right channel)     | $t_{REN}$  | —       | —       | 15      | ns    |
|                     | SPKDAT disable to SPKCLK falling edge (right channel)     | $t_{RDIS}$ | —       | —       | 5       | ns    |
|                     | SPKDAT enable from SPKCLK falling edge (left channel)     | $t_{LEN}$  | —       | —       | 15      | ns    |
|                     | SPKDAT disable to SPKCLK rising edge (left channel)       | $t_{LDIS}$ | —       | —       | 5       | ns    |

#### 1. Digital speaker (PDM) interface timing—Mode A



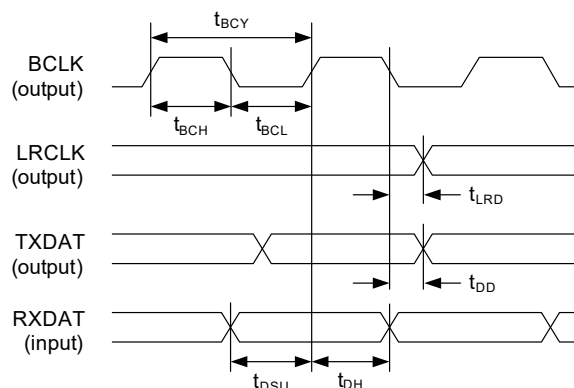
**2. Digital speaker (PDM) interface timing—Mode B**

**Table 3-16. Digital Audio Interface—Master Mode**

Test conditions (unless specified otherwise):  $C_{LOAD} = 25$  pF (output pins); BCLK slew (10% to 90%) = 3.7–5.6 ns; with the exception of the conditions noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

| Parameter <sup>1</sup>   |                                                                 | Symbol     | Minimum | Typical | Maximum | Units |
|--------------------------|-----------------------------------------------------------------|------------|---------|---------|---------|-------|
| Master Mode              | AIFnBCLK cycle time                                             | $t_{BCY}$  | 40      | —       | —       | ns    |
|                          | AIFnBCLK pulse width high                                       | $t_{BCH}$  | 18      | —       | —       | ns    |
|                          | AIFnBCLK pulse width low                                        | $t_{BCL}$  | 18      | —       | —       | ns    |
|                          | AIFnLRCLK propagation delay from BCLK falling edge <sup>2</sup> | $t_{LRD}$  | 0       | —       | 8.3     | ns    |
|                          | AIFnTXDAT propagation delay from BCLK falling edge              | $t_{DD}$   | 0       | —       | 5       | ns    |
|                          | AIFnRXDAT setup time to BCLK rising edge                        | $t_{DSU}$  | 11      | —       | —       | ns    |
|                          | AIFnRXDAT hold time from BCLK rising edge                       | $t_{DH}$   | 0       | —       | —       | ns    |
| Master Mode, Slave LRCLK | AIFnLRCLK setup time to BCLK rising edge                        | $t_{LRSU}$ | 14      | —       | —       | ns    |
|                          | AIFnLRCLK hold time from BCLK rising edge                       | $t_{LRH}$  | 0       | —       | —       | ns    |

**Note:** The descriptions above assume noninverted polarity of AIFnBCLK.

1. Digital audio interface timing—Master Mode. Note that BCLK and LRCLK outputs can be inverted if required; the figure shows the default, noninverted polarity.



2. The timing of the AIFnLRCLK signal is selectable. If the LRCLK advance option is enabled, the LRCLK transition is timed relative to the preceding BCLK edge. Under the required condition that BCLK is inverted in this case, the LRCLK transition is still timed relative to the falling BCLK edge.

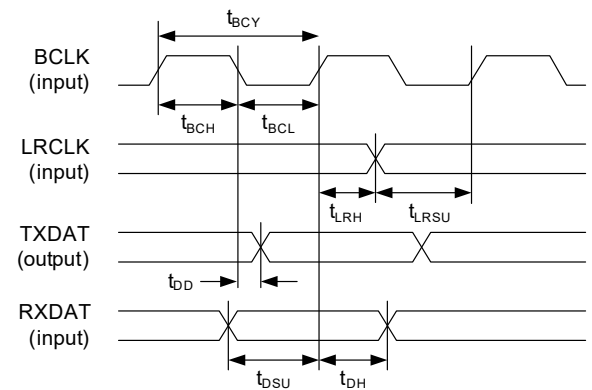
**Table 3-17. Digital Audio Interface—Slave Mode**

The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

| Parameter 1,2                                                   |                                                                  | Symbol     | Min | Typ | Max  | Units |
|-----------------------------------------------------------------|------------------------------------------------------------------|------------|-----|-----|------|-------|
| AIFnBCLK cycle time                                             |                                                                  | $t_{BCY}$  | 40  | —   | —    | ns    |
| AIFnBCLK pulse width high                                       | BCLK as direct SYSCLK source                                     | $t_{BCH}$  | 16  | —   | —    | ns    |
|                                                                 | All other conditions                                             | $t_{BCH}$  | 14  | —   | —    | ns    |
| AIFnBCLK pulse width low                                        | BCLK as direct SYSCLK source                                     | $t_{BCL}$  | 16  | —   | —    | ns    |
|                                                                 | All other conditions                                             | $t_{BCL}$  | 14  | —   | —    | ns    |
| $C_{LOAD} = 15$ pF (output pins),<br>BCLK slew (10%–90%) = 3 ns | AIFnLRCLK set-up time to BCLK rising edge                        | $t_{LRSU}$ | 7   | —   | —    | ns    |
|                                                                 | AIFnLRCLK hold time from BCLK rising edge                        | $t_{LRH}$  | 0   | —   | —    | ns    |
|                                                                 | AIFnTXDAT propagation delay from BCLK falling edge               | $t_{DD}$   | 0   | —   | 12.2 | ns    |
|                                                                 | AIFnRXDAT set-up time to BCLK rising edge                        | $t_{DSU}$  | 2   | —   | —    | ns    |
|                                                                 | AIFnRXDAT hold time from BCLK rising edge                        | $t_{DH}$   | 0   | —   | —    | ns    |
|                                                                 | Master LRCLK, AIFnLRCLK propagation delay from BCLK falling edge | $t_{LRD}$  | —   | —   | 14.8 | ns    |
| $C_{LOAD} = 25$ pF (output pins),<br>BCLK slew (10%–90%) = 6 ns | AIFnLRCLK set-up time to BCLK rising edge                        | $t_{LRSU}$ | 7   | —   | —    | ns    |
|                                                                 | AIFnLRCLK hold time from BCLK rising edge                        | $t_{LRH}$  | 0   | —   | —    | ns    |
|                                                                 | AIFnTXDAT propagation delay from BCLK falling edge               | $t_{DD}$   | 0   | —   | 14.2 | ns    |
|                                                                 | AIFnRXDAT set-up time to BCLK rising edge                        | $t_{DSU}$  | 2   | —   | —    | ns    |
|                                                                 | AIFnRXDAT hold time from BCLK rising edge                        | $t_{DH}$   | 0   | —   | —    | ns    |
|                                                                 | Master LRCLK, AIFnLRCLK propagation delay from BCLK falling edge | $t_{LRD}$  | —   | —   | 15.9 | ns    |

**Note:** The descriptions above assume noninverted polarity of AIFnBCLK.

1. Digital audio interface timing—Slave Mode. Note that BCLK and LRCLK inputs can be inverted if required; the figure shows the default, noninverted polarity.



2. If AIFnBCLK or AIFnLRCLK is selected as a source for SYSCLK (either directly or via the FLL), the frequency must be within 1% of the SYSCLK\_FREQ setting.

**Table 3-18. Digital Audio Interface Timing—TDM Mode**

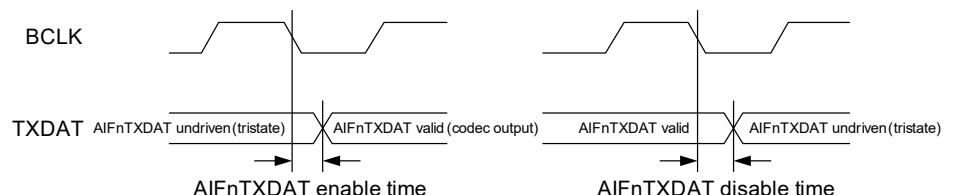
The following timing information is valid across the full range of recommended operating conditions, unless otherwise noted.

| Parameter 1                                                                                |                                               | Min | Typ | Max  | Units |
|--------------------------------------------------------------------------------------------|-----------------------------------------------|-----|-----|------|-------|
| Master Mode— $C_{LOAD}$ (AIFnTXDAT) = 15 to 25 pF. BCLK slew (10%–90%) = 3.7 ns to 5.6 ns. | AIFnTXDAT enable time from BCLK falling edge  | 0   | —   | —    | ns    |
|                                                                                            | AIFnTXDAT disable time from BCLK falling edge | —   | —   | 6    | ns    |
| Slave Mode— $C_{LOAD}$ (AIFnTXDAT) = 15 pF). BCLK slew (10%–90%) = 3 ns                    | AIFnTXDAT enable time from BCLK falling edge  | 2   | —   | —    | ns    |
|                                                                                            | AIFnTXDAT disable time from BCLK falling edge | —   | —   | 12.2 | ns    |
| Slave Mode— $C_{LOAD}$ (AIFnTXDAT) = 25 pF). BCLK slew (10%–90%) = 6 ns                    | AIFnTXDAT enable time from BCLK falling edge  | 2   | —   | —    | ns    |
|                                                                                            | AIFnTXDAT disable time from BCLK falling edge | —   | —   | 14.2 | ns    |

**Note:** If TDM operation is used on the AIFnTXDAT pins, it is important that two devices do not attempt to drive the AIFnTXDAT pin simultaneously. To support this requirement, the AIFnTXDAT pins can be configured to be tristated when not outputting data.

1. Digital audio interface timing—TDM Mode.

The timing of the AIFnTXDAT tristating at the start and end of the data transmission is shown.

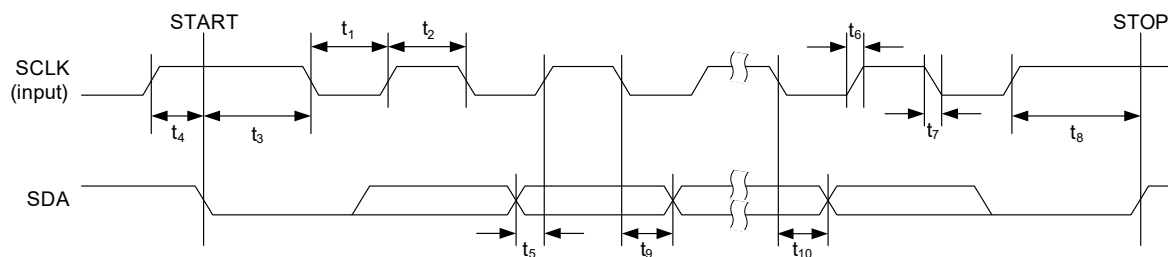


**Table 3-19. Control Interface Timing—Two-Wire (I<sup>2</sup>C) Mode**

The following timing information is valid across the full range of recommended operating conditions.

| Parameter <sup>1</sup>                    | Symbol                                                        | Min      | Typ | Max  | Units |
|-------------------------------------------|---------------------------------------------------------------|----------|-----|------|-------|
| SCLK Frequency                            | —                                                             | —        | —   | 3400 | kHz   |
| SCLK Low Pulse-Width                      | $t_1$                                                         | 160      | —   | —    | ns    |
| SCLK High Pulse-Width                     | $t_2$                                                         | 100      | —   | —    | ns    |
| Hold Time (Start Condition)               | $t_3$                                                         | 160      | —   | —    | ns    |
| Setup Time (Start Condition)              | $t_4$                                                         | 160      | —   | —    | ns    |
| SDA, SCLK Rise Time (10%–90%)             | SCLK frequency > 1.7MHz                                       | $t_6$    | —   | 80   | ns    |
|                                           | SCLK frequency > 1MHz                                         | $t_6$    | —   | 160  | ns    |
|                                           | SCLK frequency ≤ 1MHz                                         | $t_6$    | —   | 2000 | ns    |
| SDA, SCLK Fall Time (90%–10%)             | SCLK frequency > 1.7MHz                                       | $t_7$    | —   | 60   | ns    |
|                                           | SCLK frequency > 1MHz                                         | $t_7$    | —   | 160  | ns    |
|                                           | SCLK frequency ≤ 1MHz                                         | $t_7$    | —   | 200  | ns    |
| Setup Time (Stop Condition)               | $t_8$                                                         | 160      | —   | —    | ns    |
| SDA Setup Time (data input)               | $t_5$                                                         | 40       | —   | —    | ns    |
| SDA Hold Time (data input)                | $t_9$                                                         | 0        | —   | —    | ns    |
| SDA Valid Time (data/ACK output)          | SCLK slew (90%–10%) = 20ns, C <sub>LOAD</sub> (SDA) = 15 pF   | $t_{10}$ | —   | 40   | ns    |
|                                           | SCLK slew (90%–10%) = 60ns, C <sub>LOAD</sub> (SDA) = 100 pF  | $t_{10}$ | —   | 130  | ns    |
|                                           | SCLK slew (90%–10%) = 160ns, C <sub>LOAD</sub> (SDA) = 400 pF | $t_{10}$ | —   | 190  | ns    |
|                                           | SCLK slew (90%–10%) = 200ns, C <sub>LOAD</sub> (SDA) = 550 pF | $t_{10}$ | —   | 220  | ns    |
| Pulse width of spikes that are suppressed | $t_{ps}$                                                      | 0        | —   | 25   | ns    |

1. Control interface timing—I<sup>2</sup>C Mode

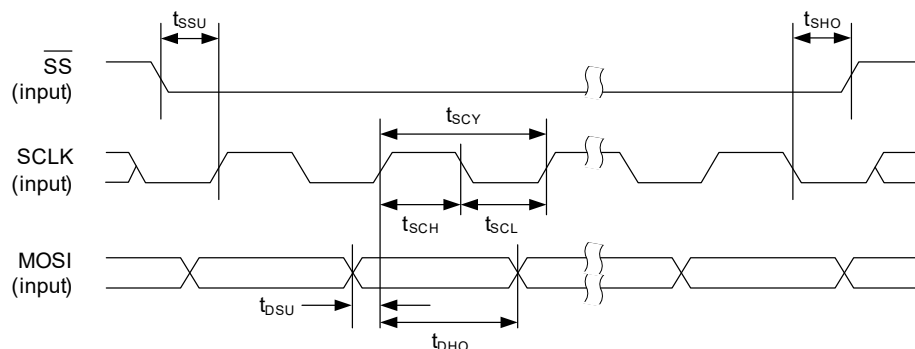


**Table 3-20. Control Interface Timing—Four-Wire (SPI) Mode**

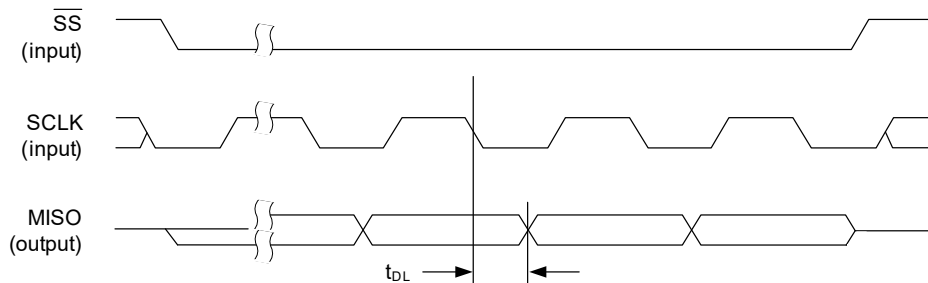
The following timing information is valid across the full range of recommended operating conditions.

| Parameter 1, 2                                                                                                                      | Symbol           | Min  | Typ | Max  | Units |
|-------------------------------------------------------------------------------------------------------------------------------------|------------------|------|-----|------|-------|
| $\overline{\text{SS}}$ falling edge to SCLK rising edge                                                                             | $t_{\text{SSU}}$ | 2.6  | —   | —    | ns    |
| SCLK falling edge to $\overline{\text{SS}}$ rising edge                                                                             | $t_{\text{SHO}}$ | 0    | —   | —    | ns    |
| SCLK pulse cycle time<br>SYSCLK disabled (SYSCLK_ENA = 0)<br>SYSCLK_ENA = 1, SYSCLK_FREQ = 000<br>SYSCLK_ENA = 1, SYSCLK_FREQ > 000 | $t_{\text{SCY}}$ | 50.0 | —   | —    | ns    |
|                                                                                                                                     | $t_{\text{SCY}}$ | 76.8 | —   | —    | ns    |
|                                                                                                                                     | $t_{\text{SCY}}$ | 38.4 | —   | —    | ns    |
| SCLK pulse width low                                                                                                                | $t_{\text{SCL}}$ | 15.3 | —   | —    | ns    |
| SCLK pulse width high                                                                                                               | $t_{\text{SCH}}$ | 15.3 | —   | —    | ns    |
| MOSI to SCLK set-up time                                                                                                            | $t_{\text{DSU}}$ | 1.5  | —   | —    | ns    |
| MOSI to SCLK hold time                                                                                                              | $t_{\text{DHO}}$ | 1.7  | —   | —    | ns    |
| SCLK falling edge to MISO transition<br>SCLK slew (90%–10%) = 5 ns, $C_{\text{LOAD}}$ (MISO) = 25 pF                                | $t_{\text{DL}}$  | 0    | —   | 12.6 | ns    |

1. Control interface timing—SPI Mode (write cycle)



2. Control interface timing—SPI Mode (read cycle)



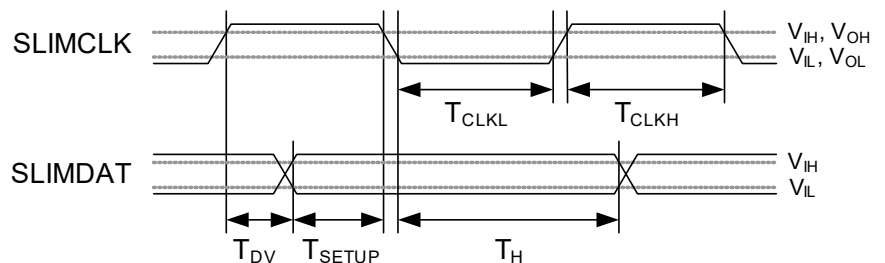
**Table 3-21. SLIMbus Interface Timing**

The following timing information is valid across the full range of recommended operating conditions.

| Parameter 1      |                                             | Symbol                                                                                             | Minimum                  | Typ  | Maximum                  | Units      |
|------------------|---------------------------------------------|----------------------------------------------------------------------------------------------------|--------------------------|------|--------------------------|------------|
| SLIMCLK input    | SLIMCLK cycle time                          | —                                                                                                  | 35                       | —    | —                        | ns         |
|                  | SLIMCLK pulse width high                    | $T_{CLKH}$                                                                                         | 12                       | —    | —                        | ns         |
|                  | SLIMCLK pulse width low                     | $T_{CLKL}$                                                                                         | 12                       | —    | —                        | ns         |
| SLIMCLK output   | SLIMCLK cycle time                          | —                                                                                                  | 40                       | —    | —                        | ns         |
|                  | SLIMCLK pulse width high                    | $T_{CLKH}$                                                                                         | 12                       | —    | —                        | ns         |
|                  | SLIMCLK pulse width low                     | $T_{CLKL}$                                                                                         | 12                       | —    | —                        | ns         |
|                  | SLIMCLK slew rate (20%–80%)                 | $C_{LOAD} = 15\text{ pF}, \text{SLIMCLK\_DRV\_STR} = 0$<br>$SR_{CLK}$                              | $0.09 \times V_{DBVDD1}$ | —    | $0.22 \times V_{DBVDD1}$ | V/ns       |
|                  |                                             | $C_{LOAD} = 70\text{ pF}, \text{SLIMCLK\_DRV\_STR} = 0$<br>$SR_{CLK}$                              | $0.02 \times V_{DBVDD1}$ | —    | $0.05 \times V_{DBVDD1}$ | V/ns       |
| SLIMDAT input    | SLIMDAT setup time to SLIMCLK falling edge  | $T_{SETUP}$                                                                                        | 3.5                      | —    | —                        | ns         |
|                  | SLIMDAT hold time from SLIMCLK falling edge | $T_H$                                                                                              | 2                        | —    | —                        | ns         |
| SLIMDAT output   | SLIMDAT time for data output                | $C_{LOAD} = 15\text{ pF}, \text{SLIMDAT\_DRV\_STR} = 1, \text{DBVDD1} = 1.71\text{ V}$<br>$T_{DV}$ | —                        | 4.7  | 8.1                      | ns         |
|                  |                                             | $C_{LOAD} = 30\text{ pF}, \text{SLIMDAT\_DRV\_STR} = 1, \text{DBVDD1} = 1.71\text{ V}$<br>$T_{DV}$ | —                        | 4.3  | 7.3                      | ns         |
|                  | valid (relative to SLIMCLK rising edge)     | $C_{LOAD} = 30\text{ pF}, \text{SLIMDAT\_DRV\_STR} = 0, \text{DBVDD1} = 1.71\text{ V}$<br>$T_{DV}$ | —                        | 6.8  | 11.8                     | ns         |
|                  |                                             | $C_{LOAD} = 30\text{ pF}, \text{SLIMDAT\_DRV\_STR} = 1, \text{DBVDD1} = 1.71\text{ V}$<br>$T_{DV}$ | —                        | 5.8  | 10.0                     | ns         |
|                  |                                             | $C_{LOAD} = 50\text{ pF}, \text{SLIMDAT\_DRV\_STR} = 0, \text{DBVDD1} = 1.71\text{ V}$<br>$T_{DV}$ | —                        | 9.6  | 16.6                     | ns         |
|                  |                                             | $C_{LOAD} = 50\text{ pF}, \text{SLIMDAT\_DRV\_STR} = 1, \text{DBVDD1} = 1.71\text{ V}$<br>$T_{DV}$ | —                        | 7.9  | 13.7                     | ns         |
|                  |                                             | $C_{LOAD} = 70\text{ pF}, \text{SLIMDAT\_DRV\_STR} = 0, \text{DBVDD1} = 1.71\text{ V}$<br>$T_{DV}$ | —                        | 12.4 | 21.5                     | ns         |
|                  |                                             | $C_{LOAD} = 70\text{ pF}, \text{SLIMDAT\_DRV\_STR} = 1, \text{DBVDD1} = 1.71\text{ V}$<br>$T_{DV}$ | —                        | 10.0 | 17.4                     | ns         |
|                  | SLIMDAT slew rate (20%–80%)                 | $C_{LOAD} = 15\text{ pF}, \text{SLIMDAT\_DRV\_STR} = 0$<br>$SR_{DATA}$                             | —                        | —    | $0.64 \times V_{DBVDD1}$ | V/ns       |
|                  |                                             | $C_{LOAD} = 30\text{ pF}, \text{SLIMDAT\_DRV\_STR} = 0$<br>$SR_{DATA}$                             | —                        | —    | $0.35 \times V_{DBVDD1}$ | V/ns       |
|                  |                                             | $C_{LOAD} = 30\text{ pF}, \text{SLIMDAT\_DRV\_STR} = 1$<br>$SR_{DATA}$                             | —                        | —    | $0.46 \times V_{DBVDD1}$ | V/ns       |
| Other parameters | Driver disable time                         | $T_{DD}$                                                                                           | —                        | —    | 6                        | ns         |
|                  | Bus holder output impedance                 | $0.1 \times V_{DBVDD1} < V < 0.9 \times V_{DBVDD1}$<br>$R_{DATAS}$                                 | 18                       | —    | 50                       | k $\Omega$ |

**Notes:**

- The signal timing information describes the timing requirements of the SLIMbus interface as a whole, not just the CS47L35 device.
- $T_{DV}$  is the propagation delay from the rising SLIMCLK edge (at CS47L35 input) to the SLIMDAT output being achieved at the input to all devices across the bus.
- $T_{SETUP}$  is the set-up time for SLIMDAT input (at CS47L35), relative to the falling SLIMCLK edge (at CS47L35).
- $T_H$  is the hold time for SLIMDAT input (at CS47L35) relative to the falling SLIMCLK edge (at CS47L35).
- For more details of the interface timing, refer to the *MIPI Alliance Specification for Serial Low-power Inter-Chip Media Bus (SLIMbus)*

**1. SLIMbus interface timing.**


$V_{IL}, V_{IH}$  are the 35%/65% levels of the respective inputs

$V_{OL}, V_{OH}$  are the 20%/80% levels of the respective outputs

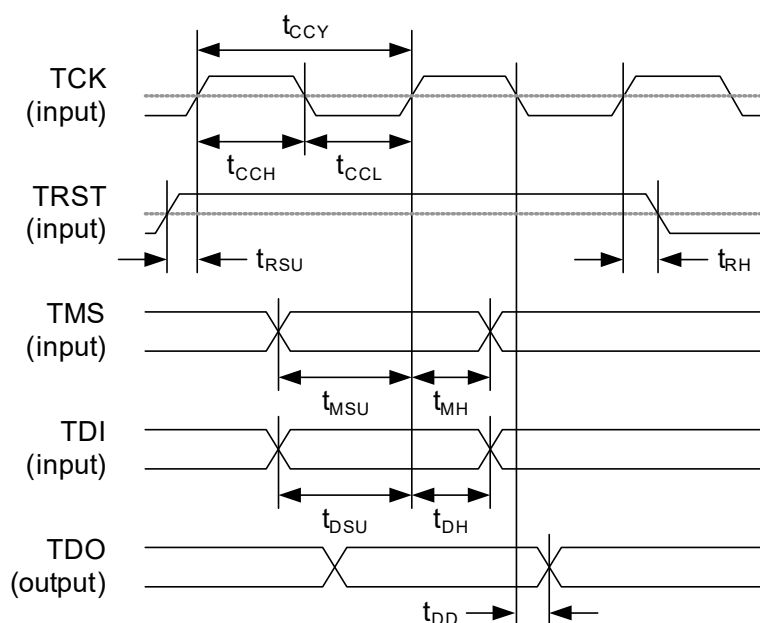
The SLIMDAT output delay ( $T_{DV}$ ) is with respect to the input pads of all receiving devices

**Table 3-22. JTAG Interface Timing**

Test conditions (unless specified otherwise):  $C_{LOAD} = 25$  pF (output pins); TCK slew (20%–80%) = 5 ns; with the exception of the conditions noted, the following electrical characteristics are valid across the full range of recommended operating conditions.

| Parameter <sup>1</sup>                      | Symbol    | Minimum | Typical | Maximum | Units |
|---------------------------------------------|-----------|---------|---------|---------|-------|
| TCK cycle time                              | $T_{CCY}$ | 50      | —       | —       | ns    |
| TCK pulse width high                        | $T_{CCH}$ | 20      | —       | —       | ns    |
| TCK pulse width low                         | $T_{CCL}$ | 20      | —       | —       | ns    |
| TMS setup time to TCK rising edge           | $T_{MSU}$ | 1       | —       | —       | ns    |
| TMS hold time from TCK rising edge          | $T_{MH}$  | 2       | —       | —       | ns    |
| TDI setup time to TCK rising edge           | $T_{DSU}$ | 1       | —       | —       | ns    |
| TDI hold time from TCK rising edge          | $T_{DH}$  | 2       | —       | —       | ns    |
| TDO propagation delay from TCK falling edge | $T_{DD}$  | 0       | —       | 17      | ns    |
| TRST setup time to TCK rising edge          | $T_{RSU}$ | 3       | —       | —       | ns    |
| TRST hold time from TCK rising edge         | $T_{RH}$  | 3       | —       | —       | ns    |
| TRST pulse width low                        | —         | 20      | —       | —       | ns    |

1. JTAG Interface timing



**Table 3-23. Typical Power Consumption**

Test conditions (unless specified otherwise): DBVDD1 = DBVDD2 = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = Off (CP2 and LDO2 disabled); SPKVDD = 4.2 V;  $T_A = +25^\circ\text{C}$ ;  $F_s = 48\text{ kHz}$ ; 24-bit audio data, I<sup>2</sup>S Slave Mode; SYSCLK = 24.576 MHz (direct MCLK1 input).

| Operating Configuration |                                                                                |                                          |           | Typical<br>I <sub>1.2V</sub> (mA) | Typical<br>I <sub>1.8V</sub> (mA) | Typical<br>I <sub>4.2V</sub> (mA) | P <sub>TOT</sub><br>(mW) |
|-------------------------|--------------------------------------------------------------------------------|------------------------------------------|-----------|-----------------------------------|-----------------------------------|-----------------------------------|--------------------------|
| Headphone playback      | AIF1 to DAC to HPOUT (stereo),<br>32-Ω load.                                   | 1-kHz sine wave, P <sub>O</sub> = 10 mW  | Quiescent | 1.00                              | 0.75                              | 0.00                              | 2.54                     |
|                         |                                                                                |                                          |           | 1.06                              | 36.5                              | 0.00                              | 67.0                     |
| Earpiece playback       | AIF1 to DAC to EPOUT,<br>32-Ω load (BTL).                                      | 1-kHz sine wave, P <sub>O</sub> = 30 mW  | Quiescent | 0.86                              | 0.75                              | 0.00                              | 2.38                     |
|                         |                                                                                |                                          |           | 0.86                              | 61.8                              | 0.00                              | 112                      |
| Speaker playback        | AIF1 to DAC to SPKOUT,<br>8-Ω, 22-μH load.                                     | 1-kHz sine wave, P <sub>O</sub> = 700 mW | Quiescent | 0.76                              | 1.03                              | 0.10                              | 3.19                     |
|                         |                                                                                |                                          |           | 0.79                              | 1.10                              | 180                               | 759                      |
| Stereo line record      | Analog line to ADC to AIF1,<br>MICVDD = 1.8V (CP2 and LDO2<br>bypass enabled). | 1-kHz sine wave, -1 dBFS output          |           | 1.23                              | 2.52                              | 0.00                              | 6.01                     |
| Sleep Mode              | Accessory detect enabled (JD1_ENA = 1)                                         |                                          |           | 0.000                             | 0.013                             | 0.000                             | 0.023                    |

**Table 3-24. Typical Signal Latency**

Test conditions (unless specified otherwise): DBVDD1 = DBVDD2 = CPVDD1 = AVDD = 1.8 V, DCVDD = FLLVDD = CPVDD2 = 1.2 V; MICVDD = Off (CP2 and LDO2 disabled); SPKVDD = 4.2 V;  $T_A = +25^\circ\text{C}$ ;  $F_s = 48\text{ kHz}$ ; 24-bit audio data, I<sup>2</sup>S Slave Mode; SYSCLK = 24.576 MHz (direct MCLK1 input).

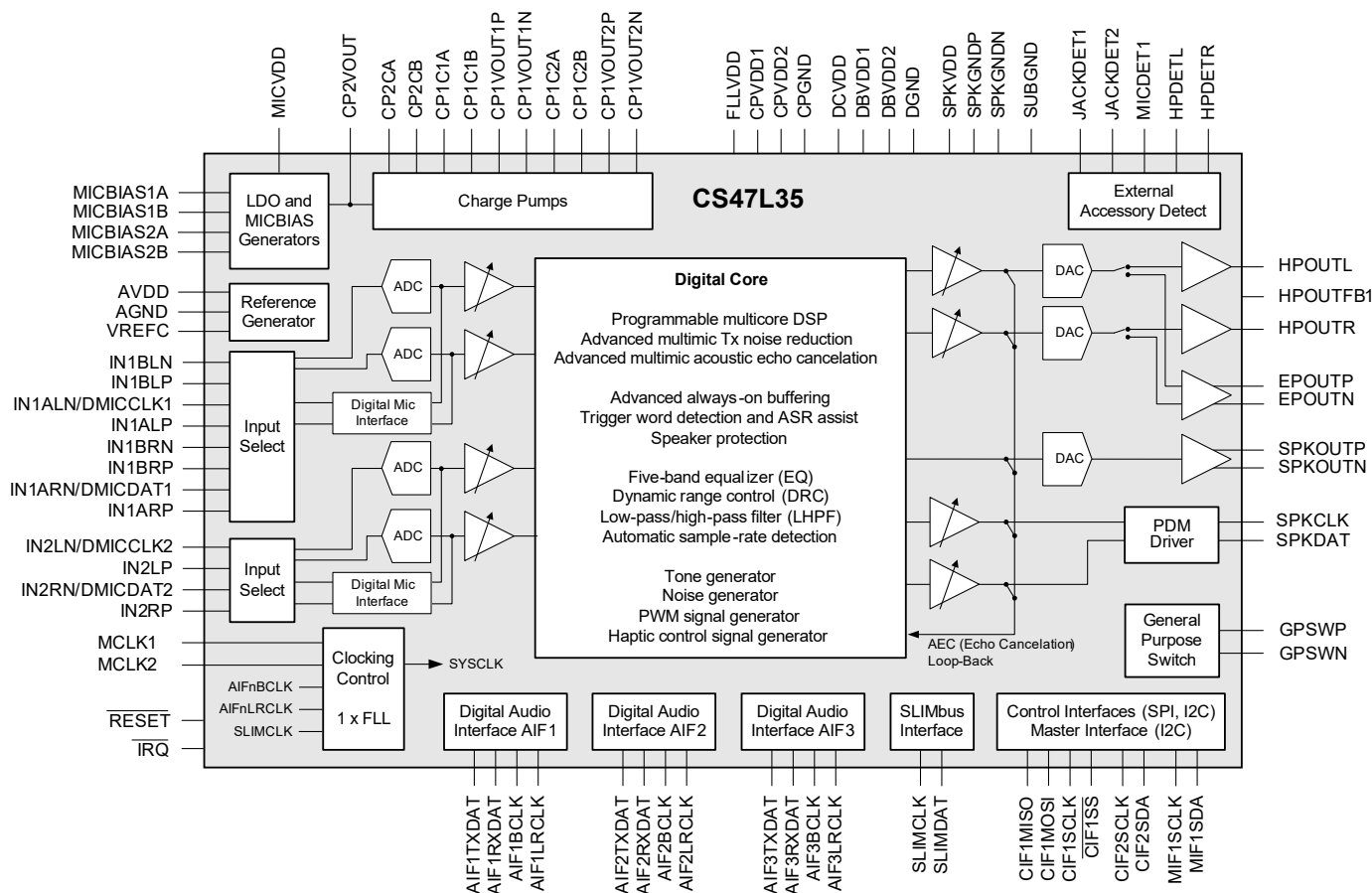
| Operating Configuration |                                                                                                                                                                                            |                                              | Latency (μs) |
|-------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|--------------|
| AIF to DAC path         | Digital input (AIFn) to analog output (HPOUT).<br>Signal is routed via the ISRC function in the<br>asynchronous cases only.                                                                | 48 kHz input, 48 kHz output, Synchronous     | 344          |
|                         |                                                                                                                                                                                            | 44.1 kHz input, 44.1 kHz output, Synchronous | 371          |
|                         |                                                                                                                                                                                            | 16 kHz input, 16 kHz output, Synchronous     | 665          |
|                         |                                                                                                                                                                                            | 8 kHz input, 8 kHz output, Synchronous       | 1105         |
|                         |                                                                                                                                                                                            | 8 kHz input, 48 kHz output, Isochronous      | 1660         |
|                         |                                                                                                                                                                                            | 16 kHz input, 48 kHz output, Isochronous     | 1170         |
| ADC to AIF path         | Analog input (INn) to digital output (AIFn). Digital<br>core high-pass filter is included in the signal path.<br>Signal is routed via the ISRC function in the<br>asynchronous cases only. | 48 kHz input, 48 kHz output, Synchronous     | 210          |
|                         |                                                                                                                                                                                            | 44.1 kHz input, 44.1 kHz output, Synchronous | 225          |
|                         |                                                                                                                                                                                            | 16 kHz input, 16 kHz output, Synchronous     | 620          |
|                         |                                                                                                                                                                                            | 8 kHz input, 8 kHz output, Synchronous       | 1210         |
|                         |                                                                                                                                                                                            | 8 kHz input, 48 kHz output, Isochronous      | 1765         |
|                         |                                                                                                                                                                                            | 16 kHz input, 48 kHz output, Isochronous     | 965          |

## 4 Functional Description

The CS47L35 is a highly integrated, low-power audio hub codec for mobile telephony and portable devices. It provides flexible, high-performance audio interfacing for handheld devices in a small and cost-effective package. It also provides exceptional levels of performance and signal-processing capability, suitable for a wide variety of mobile and handheld devices.

### 4.1 Overview

The CS47L35 block diagram is shown in Fig. 4-1.



**Figure 4-1. CS47L35 Block Diagram**

The CS47L35 digital core provides an extensive capability for signal-processing algorithms, including transmit (TX) path noise reduction, acoustic-echo cancellation (AEC), and other programmable filters. The DSPs are ideally suited to the Cirrus Logic® SoundClear® suite of audio processing algorithms, such as the SoundClear Control always-on voice control software.

The digital core provides signal-processing capability for sensor-hub functions. The integration of external sensors with the programmable DSP enables increased contextual awareness in a variety of advanced user applications.

The CS47L35 digital core supports audio enhancements, such as dynamic range control (DRC) and multiband compression (MBC). Highly flexible digital mixing, including stereo full-duplex isochronous sample-rate conversion, provides use-case flexibility across a broad range of system architectures. A signal generator for controlling haptics vibrate actuators is included.

The CS47L35 provides multiple digital audio interfaces, including SLIMbus, to provide independent isochronous connections to different processors (e.g., application processor, baseband processor, and wireless transceiver).

A flexible clocking arrangement supports a wide variety of external clock references, including clocking derived from the digital audio interface. The frequency-locked loop (FLL) circuit provides additional flexibility.

Unused circuitry can be disabled under software control to save power; low leakage currents enable extended standby/off time in portable battery-powered applications. The CS47L35 always-on circuitry can be used in conjunction with the Apps Processor to wake up the device following a headphone jack-detection event.

Versatile GPIO functionality is provided, including support for external accessory/push-button detection inputs. Comprehensive interrupt functions, with status reporting, are also provided.

### 4.1.1 Hi-Fi Audio Codec

The CS47L35 is a high-performance, low-power audio codec that uses a simple analog architecture. Four ADCs are incorporated, with multiplexers to support up to six analog inputs. Three DACs are incorporated, with two being switchable between the headphone and BTL-earpiece analog output paths.

The analog outputs comprise a 30-mW (122 dB SNR) stereo headphone amplifier with ground-referenced output, a mono (BTL) earpiece driver, and a mono Class D speaker driver capable of delivering 2.7 W into a 4- $\Omega$  load. Six analog inputs are provided (multiplexed into four input channels), each supporting single-ended or differential input modes. In differential mode, the input path SNR is 105 dB (16 kHz sample rate, i.e., wideband voice mode). The ADC input paths can be bypassed, supporting up to four channels of DMIC input.

The audio codec is controlled directly via register access. The simple analog architecture, combined with the integrated tone generator, enables straightforward device configuration and testing, minimizing debug time and reducing software effort.

The CS47L35 output drivers are designed to support a range of different system architectures. Each output path supports independent signal mixing, equalization, filtering, and gain controls. This allows each signal path to be individually tailored for the load characteristics. All outputs have integrated pop and click suppression features.

The headphone and earpiece output drivers are ground-referenced, powered from an integrated charge pump, enabling high quality, power efficient headphone playback without any requirement for DC blocking capacitors. Ground loop feedback is incorporated, providing rejection of noise on the ground connections.

The Class D speaker driver delivers excellent power efficiency. Speaker protection software is supported within the DSP core, enabling maximum audio output without risk of damage to the external speaker. High PSRR, low leakage and optimized supply voltage ranges enable powering from switching regulators or directly from the battery. Battery current consumption is minimized across a wide variety of voice communication and multimedia playback use cases.

The CS47L35 is cost optimized for a wide range of mobile phone applications, and incorporates a mono Class D power amplifier. For applications requiring more than one channel of power amplification (or when using the integrated Class D path to drive a haptics actuator), the PDM output channels can be used to drive external PDM-input speaker drivers. The PDM outputs can ease layout and electromagnetic compatibility by avoiding the need to run the Class D speaker output over a long distance and across interconnects.

### 4.1.2 Digital Audio Core

The CS47L35 uses a core architecture based on all-digital signal routing, making digital audio effects available on all signal paths, regardless of whether the source data input is analog or digital. The digital mixing desk allows different audio effects to be applied simultaneously on many independent paths, while supporting a variety of sample rates. This helps support many new audio use cases. Soft mute and unmute control allows smooth transitions between use cases without interrupting existing audio streams elsewhere.

The CS47L35 digital core provides an extensive capability for programmable signal-processing algorithms. The SoundClear suite of software algorithms enable advanced multimic audio features, such as transmit (TX) path noise reduction, AEC, wind-noise reduction, and other programmable filters. Enhancements such as DRC and MBC are also provided.

The CS47L35 is ideal for mobile telephony, providing enhanced voice communication quality for both near-end and far-end users in a wide variety of applications. The SoundClear Control voice command recognition software is supported, for low-power always-on features. Speaker Protection software is available, using analog input paths to support current monitoring in the speaker output; this allows the Class D output to be continually optimized for the operational limits of the speaker, and enables maximum audio output while ensuring the loudspeakers are fully protected from damage.

The digital core also provides signal-processing capability for sensor-hub functions of the CS47L35. Sensors and accessories can be connected through the master I<sup>2</sup>C interface; the programmable DSP, together with peripheral timer and event logging functions, enables applications to use these inputs to support increased contextual awareness, including advanced motion sensing and navigation functionality.

Highly flexible digital mixing, including mixing between audio interfaces, is possible. The CS47L35 performs multichannel full-duplex isochronous sample-rate conversion, providing use-case flexibility across a broad range of system architectures. Automatic sample-rate detection is provided, enabling seamless wideband/narrowband voice call handover.

DRC functions are available for optimizing audio signal levels. In playback modes, the DRC can be used to maximize loudness, while limiting the signal level to avoid distortion, clipping, or battery droop, for high-power output drivers such as speaker amplifiers. In record modes, the DRC assists in applications where the signal level is unpredictable.

The five-band parametric EQ functions can be used to compensate for the frequency characteristics of the output transducers. EQ functions can be cascaded to provide additional frequency control. Programmable high-pass and low-pass filters are also available for general filtering applications, such as removal of wind and other low-frequency noise.

### 4.1.3 Digital Interfaces

Three serial digital audio interfaces (AIFs) each support PCM, TDM, and I<sup>2</sup>S data formats for compatibility with most industry-standard chipsets. AIF1 supports six input/output channels; AIF2 and AIF3 support two input/output channels each. Bidirectional operation at sample rates up to 192 kHz is supported.

Four digital PDM input channels are available (two stereo interfaces); these are typically used for digital microphones, powered from the integrated MICBIAS power-supply regulators. Two PDM output channels are also available (one stereo interface); these are typically used for external power amplifiers. Embedded mute codes provide a control mechanism for external PDM-input devices.

The CS47L35 features a SLIMbus interface, compliant with the MIPI® SLIMbus specification, providing six channels of audio input/output. Mixed audio sample rates are supported on the SLIMbus interface. The SLIMbus interface also supports read/write access to the CS47L35 control registers.

An IEC-60958-3-compatible S/PDIF transmitter is incorporated, enabling stereo S/PDIF output on a GPIO pin. Standard S/PDIF sample rates of 32–192 kHz are supported.

Control register access and high bandwidth data transfer are supported by a slave SPI interface and a slave I<sup>2</sup>C control interface. The SPI interface operates up to 26 MHz; the I<sup>2</sup>C slave interface operates up to 3.4 MHz. Full access to the register map is also provided via the SLIMbus port.

The CS47L35 incorporates one master I<sup>2</sup>C interface, offering capability for additional sensor/accessory input. Typical sensors include accelerometers, gyroscopes and magnetometers for motion sensing and navigation applications. Other example accessories include barometers, or ambient light sensors, for environmental awareness.

### 4.1.4 Other Features

The CS47L35 incorporates two 1-kHz tone generators that can be used for beep functions through any of the audio signal paths. The phase relationship between the two generators is configurable, providing flexibility in creating differential signals, or for test scenarios.

A white-noise generator is provided that can be routed within the digital core. The noise generator can provide comfort noise in cases where silence (digital mute) is not desirable.

Two pulse-width modulation (PWM) signal generators are incorporated. The duty cycle of each PWM signal can be modulated by an audio source or can be set to a fixed value using a control register setting. The PWM signal generators can be output directly on a GPIO pin.

The CS47L35 supports up to 16 GPIO pins, offering a range of input/output functions for interfacing, for detection of external hardware, and for providing logic outputs to other devices. The GPIOs are multiplexed with other functions. Comprehensive interrupt functionality is also provided for monitoring internal and external event conditions.

A signal generator for controlling haptics devices is included, compatible with both eccentric rotating mass (ERM) and linear resonant actuator (LRA) haptics devices. The haptics signal generator is highly configurable and can execute programmable drive event profiles, including reverse drive control. An external vibrate actuator can be driven directly by the Class D speaker output or

The CS47L35 incorporates four general-purpose timers, providing support for the sensor-hub connectivity. Sensor event logging, and other real time application functions, allows many advanced functions to be implemented with a high degree of autonomy from a host processor.

A smart accessory interface is included, supporting most standard 3.5-mm accessories. Jack detection, accessory sensing, and impedance measurement is provided, for external accessory and push-button detection. Accessory detection can be used as a wake-up trigger from low-power standby. Microphone activity detection with interrupt is also available.

System clocking can be derived from the MCLK1 or MCLK2 input pins. Alternatively, the SLIMbus interface, or the audio interfaces (configured in Slave Mode), can be used to provide a clock reference. The integrated FLL circuit provides support for a wide range of clocking configurations, including the use of a 32-kHz input clock reference.

The CS47L35 can be powered from 1.8- and 1.2-V external supplies. A separate supply (4.2 V) is typically required for the Class D speaker driver. Integrated charge-pump and LDO-regulator circuits are used to generate supply rails for internal functions and to support powering or biasing of external microphones.

## 4.2 Input Signal Path

The CS47L35 provides flexible input channels, supporting up to six analog inputs or up to four digital inputs. Selectable combinations of analog (mic or line) and digital inputs are multiplexed into two stereo input signal paths.

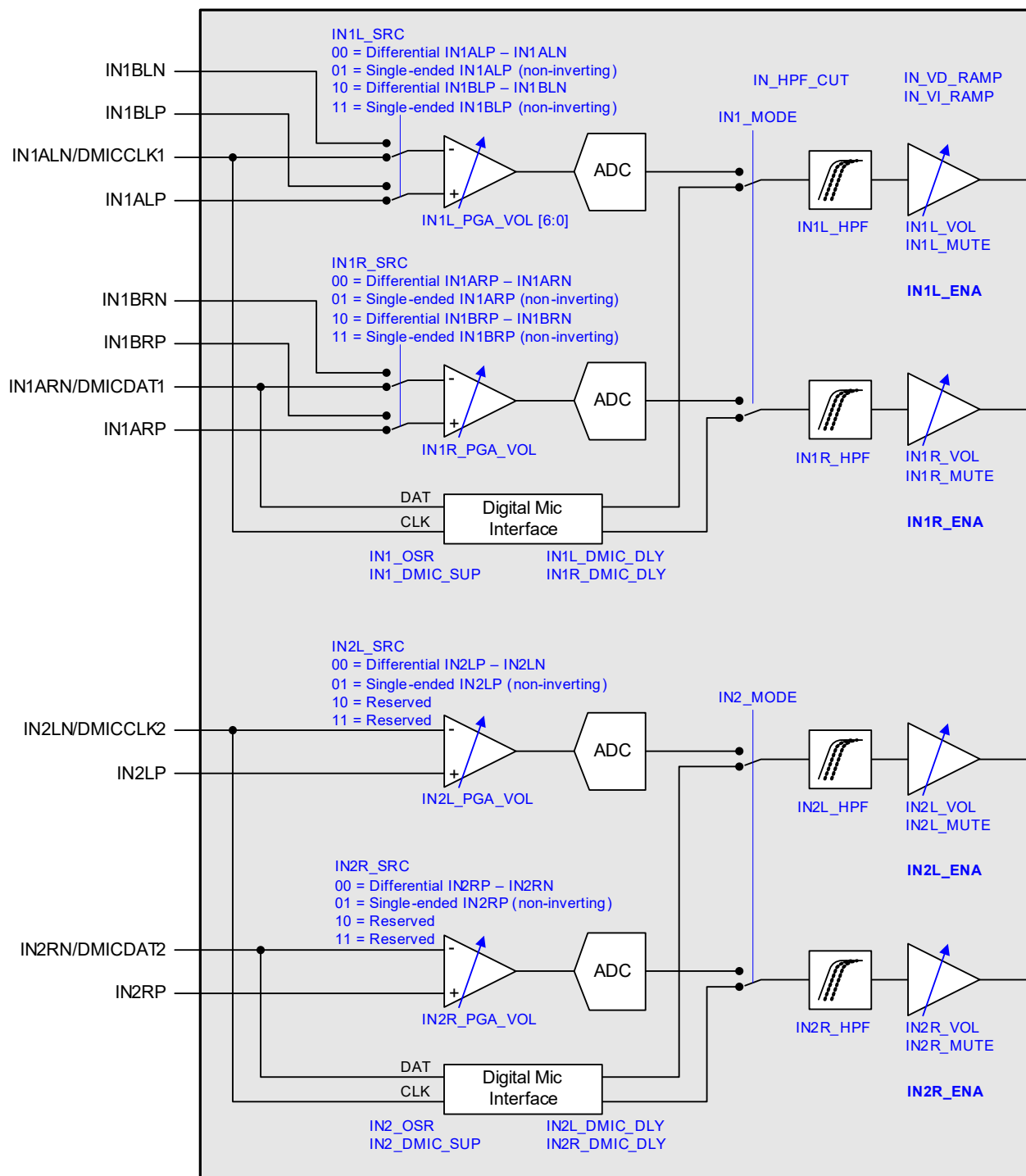
The analog input paths support single-ended and differential modes, programmable gain control, and are digitized using a high performance sigma-delta ADC.

The digital input paths interface directly with external digital microphones; a separate microphone interface clock is provided for two separate stereo pairs of digital microphones. Digital delay can be applied to any of the digital input paths; this can be used for phase adjustment of any digital input, including directional control of multiple microphones.

Two microphone bias (MICBIAS) generators provide a low-noise reference for biasing electret condenser microphones (ECMs) or for use as a low-noise supply for MEMS microphones and digital microphones. Switchable outputs from the MICBIAS generators allow four separate reference/supply outputs to be independently controlled.

Digital volume control is available on all inputs (analog and digital), with programmable ramp control for smooth, glitch-free operation.

The IN1 and IN2 signal paths and control fields are shown in [Fig. 4-2](#).



**Figure 4-2. Input Signal Paths**

### 4.2.1 Analog Microphone Input

Up to six analog microphones can be connected to the CS47L35, either in single-ended or differential mode. The applicable mode, and input pin selection, is controlled using  $IN_{nx\_SRC}$ , as described in [Section 4.2.6](#).

The CS47L35 includes external accessory-detection circuits that can report the presence of a microphone and the status of a hook switch or other push buttons. When using this function, it is recommended to use the IN1BLP or IN1BRP analog microphone input paths to ensure best immunity to electrical transients arising from the push buttons.

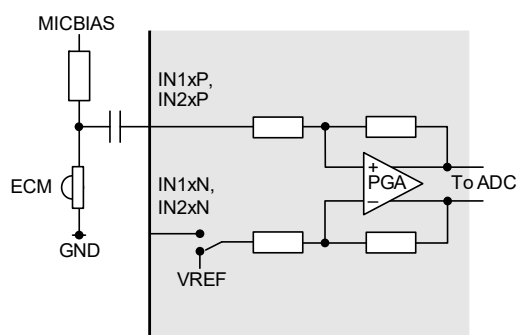
For single-ended input, the microphone signal is connected to the noninverting input of the PGAs (IN<sub>n</sub>LP or IN<sub>n</sub>RP). The inverting inputs of the PGAs are connected to an internal reference in this configuration.

For differential input, the noninverted microphone signal is connected to the noninverting input of the PGAs (IN<sub>n</sub>LP or IN<sub>n</sub>RP), while the inverted (or noisy ground) signal is connected to the inverting input pins (IN<sub>n</sub>LN or IN<sub>n</sub>RN).

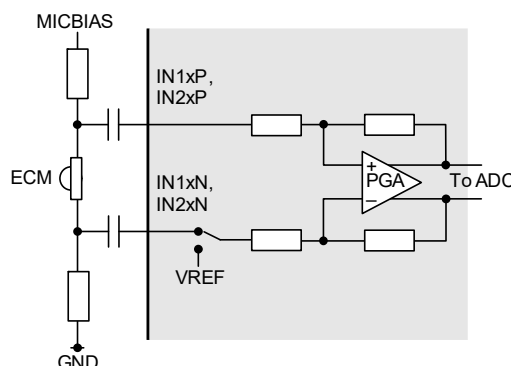
**Note:** Pseudodifferential connection is also possible—this is similar to the configuration shown in Fig. 4-4, but the GND connection is directly to the microphone (and IN<sub>n</sub>xN capacitor), instead of via a resistor. This is the recommended configuration if the external accessory detection functions on the CS47L35 are used. The IN<sub>n</sub>x\_SRC field settings are the same for pseudodifferential connection as for differential.

The gain of the input PGAs is controlled via register settings, as defined in Section 4.2.6. Note that the input impedance of the analog input paths is fixed across all PGA gain settings.

The ECM analog input configurations are shown in Fig. 4-3 and Fig. 4-4. The integrated MICBIAS generators provide a low noise reference for biasing the ECMs.

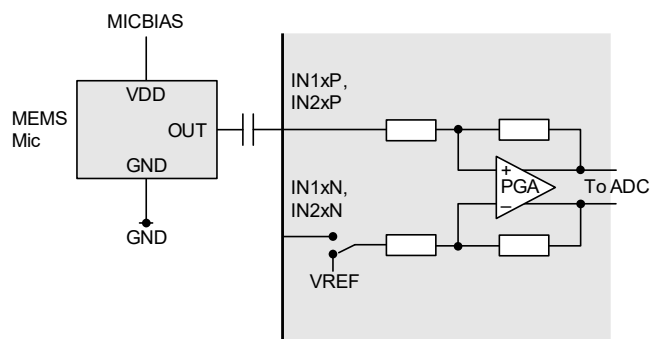


**Figure 4-3. Single-Ended ECM Input**

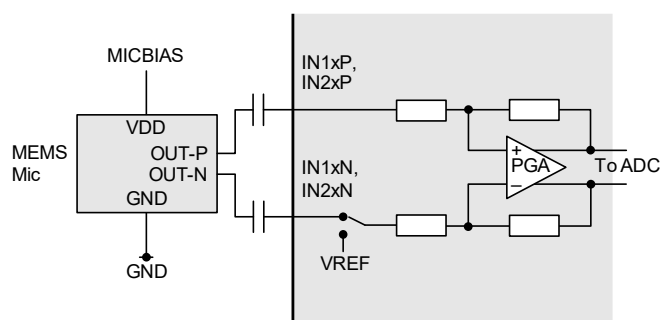


**Figure 4-4. Differential ECM Input**

Analog MEMS microphones can be connected to the CS47L35 in a similar manner to the ECM configurations. Typical configurations are shown in Fig. 4-5 and Fig. 4-6. In this configuration, the integrated MICBIAS generators provide a low-noise power supply for the microphones.



**Figure 4-5. Single-Ended MEMS Input**



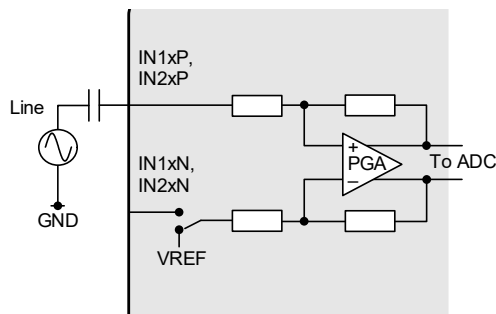
**Figure 4-6. Differential MEMS Input**

**Note:** The MICVDD pin can also be used (instead of MICBIAS) as a reference or power supply for external microphones. The MICBIAS outputs are recommended, because they offer better noise performance and independent enable/disable control.

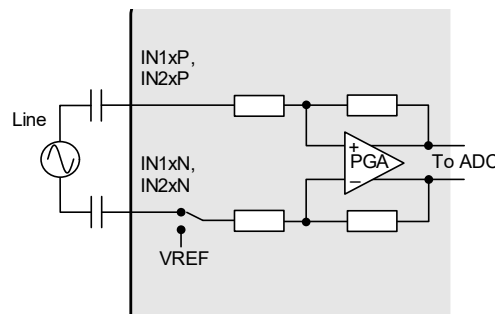
## 4.2.2 Analog Line Input

Line inputs can be connected to the CS47L35 in a similar manner to the mic inputs. Single-ended and differential modes are supported on each analog input path. The mode is selected using IN<sub>n</sub>x\_SRC, as described in Section 4.2.6.

The analog line input configurations are shown in [Fig. 4-7](#) and [Fig. 4-8](#). Note that the microphone bias (MICBIAS) is not used for line input connections.



**Figure 4-7. Single-Ended Line Input**



**Figure 4-8. Differential Line Input**

### 4.2.3 DMIC Input

As many as four digital microphones can be connected to the CS47L35. DMIC operation on input paths IN1 and IN2 is selected using `INn_MODE`, as described in [Section 4.2.6](#).

In DMIC mode, two channels of audio data are multiplexed on the associated `DMICDATn` pin. Each stereo DMIC interface is clocked using the respective `DMICCLKn` pin.

If DMIC input is enabled, the CS47L35 outputs a clock signal on the applicable `DMICCLKn` pins. The `DMICCLKn` frequency is controlled by the respective `INn_OSR` field, as described in [Table 4-1](#) and [Table 4-3](#).

Note that, if the 384- or 768-kHz `DMICCLKn` frequency is selected for one or more of the DMIC input paths, the maximum valid input path sample rate (all input paths) is affected as described in [Table 4-1](#).

The `DMICCLKn` frequencies in [Table 4-1](#) assume that the `SYSCCLK` frequency is a multiple of 6.144 MHz (`SYSCCLK_FRAC` = 0). If the `SYSCCLK` frequency is a multiple of 5.6448 MHz (`SYSCCLK_FRAC` = 1), the `DMICCLKn` frequencies are scaled accordingly.

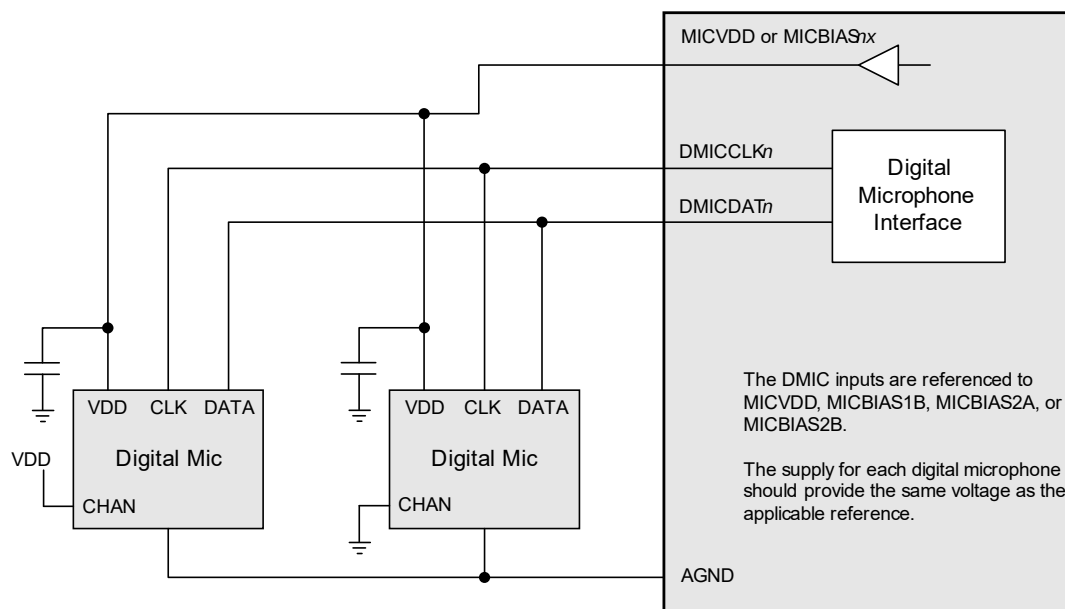
**Table 4-1. DMICCLK Frequency**

| Condition                  | DMICCLKn Frequency | Valid Sample Rates | Signal Passband |
|----------------------------|--------------------|--------------------|-----------------|
| <code>INn_OSR</code> = 010 | 384 kHz            | Up to 48 kHz       | Up to 4 kHz     |
| <code>INn_OSR</code> = 011 | 768 kHz            | Up to 96 kHz       | Up to 8 kHz     |
| <code>INn_OSR</code> = 100 | 1.536 MHz          | Up to 192 kHz      | Up to 20 kHz    |
| <code>INn_OSR</code> = 101 | 3.072 MHz          | Up to 192 kHz      | Up to 20 kHz    |
| <code>INn_OSR</code> = 110 | 6.144 MHz          | Up to 192 kHz      | Up to 96 kHz    |

The voltage reference for the IN1 and IN2 DMIC interfaces is selectable, using `INn_DMIC_SUP`; each interface may be referenced to `MICVDD` or to the `MICBIAS1B`, `MICBIAS2A`, or `MICBIAS2B` levels. The voltage reference for each digital input path should be set equal to the applicable power supply of the respective microphones.

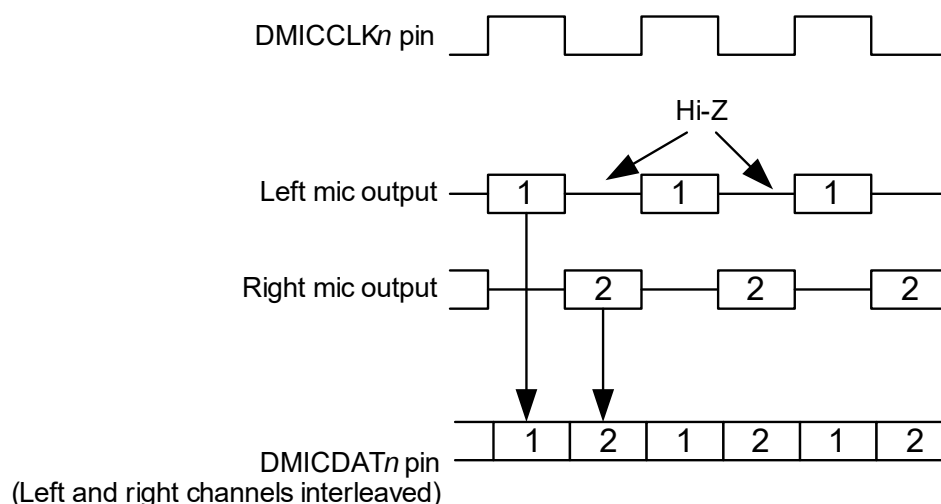
A pair of digital microphones is connected as shown in [Fig. 4-9](#). The microphones must be configured to ensure that the left mic transmits a data bit when `DMICCLK` is high and the right mic transmits a data bit when `DMICCLK` is low. The CS47L35 samples the DMIC data at the end of each `DMICCLK` phase. Each microphone must tristate its data output when the other microphone is transmitting.

Note that the CS47L35 provides integrated pull-down resistors on the `DMICDATn` pins. This provides a flexible capability for interfacing with other devices.



**Figure 4-9. DMIC Input**

Two DMIC channels are interleaved on DMICDAT $n$ . The DMIC interface timing is shown in [Fig. 4-10](#). Each microphone must tristate its data output when the other microphone is transmitting.



**Figure 4-10. DMIC Interface Timing**

When DMIC input is enabled, the CS47L35 outputs a clock signal on the applicable DMICCLK pins. The DMICCLK frequency is selectable, as described in [Table 4-1](#).

Note that SYSCLK must be present and enabled when using the DMIC inputs; see [Section 4.16](#) for details regarding SYSCLK and the associated registers.

#### 4.2.4 Input Signal Path Enable

The input signal paths are enabled using the bits described in [Table 4-2](#). The respective bits must be enabled for analog or digital input on the respective input paths.

The input signal paths are muted by default. It is recommended that deselecting the mute should be the final step of the path enable control sequence. Similarly, the mute should be selected as the first step of the path-disable control sequence. The input signal path mute functions are controlled using the bits described in [Table 4-4](#).

The MICVDD power domain must be enabled when using the analog input signal paths. This power domain is provided using an internal charge pump (CP2) and LDO regulator (LDO2). See [Section 4.19](#) for details of these circuits.

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The input signal paths should be kept disabled (IN<sub>n</sub>X\_ENA = 0) if SYSCLK is not enabled. The 32-kHz clock may also be required, depending on the path configuration. See [Section 4.16](#) for details of the system clocks (including requirements for reconfiguring SYSCLK while audio paths are enabled).

The CS47L35 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the input signal paths and associated ADCs. If the frequency is too low, an attempt to enable an input signal path fails. Note that active signal paths are not affected under such circumstances.

The status bits in Register R769 indicate the status of each of the input signal paths. If an underclocked error condition occurs, these bits indicate which input signal paths have been enabled.

**Table 4-2. Input Signal Path Enable**

| Register Address                      | Bit | Label        | Default | Description                                                       |
|---------------------------------------|-----|--------------|---------|-------------------------------------------------------------------|
| R768 (0x0300)<br>Input_Enables        | 3   | IN2L_ENA     | 0       | Input Path 2 (left) enable<br>0 = Disabled<br>1 = Enabled         |
|                                       | 2   | IN2R_ENA     | 0       | Input Path 2 (right) enable<br>0 = Disabled<br>1 = Enabled        |
|                                       | 1   | IN1L_ENA     | 0       | Input Path 1 (left) enable<br>0 = Disabled<br>1 = Enabled         |
|                                       | 0   | IN1R_ENA     | 0       | Input Path 1 (right) enable<br>0 = Disabled<br>1 = Enabled        |
| R769 (0x0301)<br>Input_Enables_Status | 3   | IN2L_ENA_STS | 0       | Input Path 2 (left) enable status<br>0 = Disabled<br>1 = Enabled  |
|                                       | 2   | IN2R_ENA_STS | 0       | Input Path 2 (right) enable status<br>0 = Disabled<br>1 = Enabled |
|                                       | 1   | IN1L_ENA_STS | 0       | Input Path 1 (left) enable status<br>0 = Disabled<br>1 = Enabled  |
|                                       | 0   | IN1R_ENA_STS | 0       | Input Path 1 (right) enable status<br>0 = Disabled<br>1 = Enabled |

### 4.2.5 Input Signal Path Sample-Rate Control

The input signal paths may be selected as input to the digital mixers or signal-processing functions within the CS47L35 digital core. The sample rate for the input signal paths is configured using IN\_RATE; see [Table 4-21](#).

Note that sample-rate conversion is required when routing the input signal paths to any signal chain that is configured for a different sample rate.

### 4.2.6 Input Signal Path Configuration

The CS47L35 supports up to six analog inputs or up to four digital inputs. Selectable combinations of analog (mic or line) and digital inputs are multiplexed into two stereo input signal paths.

Input paths IN1 and IN2 can be configured as single-ended, differential, or DMIC configuration. The input signal path configuration is selected using IN $n$ \_MODE and IN $n$ x\_SRC.

A configurable high-pass filter (HPF) is provided on the left and right channels of each input path. The applicable cut-off frequency is selected using IN\_HPFCUT. The filter can be enabled on each path independently using the IN $n$ x\_HPFBITS.

The analog input signal paths (single-ended or differential) each incorporate a PGA to provide gain in the range 0 dB to +31 dB in 1-dB steps. Note that these PGAs do not provide pop suppression functions; it is recommended that the gain should not be adjusted while the respective signal path is enabled.

The analog input PGA gain is controlled using IN $n$ L\_PGA\_VOL and IN $n$ R\_PGA\_VOL. Note that separate volume control is provided for the left and right channels of each stereo pair.

If the IN1 or IN2 input signal path is configured for DMIC input, the voltage reference for the associated input/output pins is selectable using the IN $n$ \_DMIC\_SUP fields—each interface may be referenced to MICVDD, or to the MICBIAS1B, MICBIAS2A, or MICBIAS2B levels. The voltage reference for each digital input path should be set equal to the applicable power supply of the respective microphones.

When the input signal path is configured for DMIC input, the respective DMICCLK $n$  frequency can be configured using the IN $n$ \_OSR bits.

A digital delay may be applied to any of the DMIC input channels. This feature can be used for phase adjustment of any digital input, including directional control of multiple microphones. The delay is controlled using IN $n$ L\_DMIC\_DLY and IN $n$ R\_DMIC\_DLY.

The MICVDD voltage is generated by an internal charge pump and LDO regulator. The MICBIAS $n$ x outputs are derived from MICVDD; see [Section 4.19](#).

The input signal paths are configured using the fields described in [Table 4-3](#).

**Table 4-3. Input Signal Path Configuration**

| Register Address                       | Bit   | Label              | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----------------------------------------|-------|--------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R780 (0x030C)<br>HPF_Control           | 2:0   | IN_HPFCUT[2:0]     | 010     | Input Path HPF Select. Controls the cut-off frequency of the input path HPF circuits.<br>000 = 2.5 Hz                      010 = 10 Hz                      100 = 40 Hz<br>001 = 5 Hz                      011 = 20 Hz                      All other codes are reserved                                                                                                                                                           |
| R784 (0x0310)<br>IN1L_Control          | 15    | IN1L_HPFBITS       | 0       | Input Path 1 (Left) HPF Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                      |
|                                        | 12:11 | IN1_DMIC_SUP[1:0]  | 00      | Input Path 1 DMIC Reference Select (sets the DMICDAT1 and DMICCLK1 logic levels)<br>00 = MICVDD                      10 = MICBIAS2A<br>01 = MICBIAS1B                      11 = MICBIAS2B                                                                                                                                                                                                                                          |
|                                        | 10    | IN1_MODE           | 00      | Input Path 1 Mode<br>0 = Analog input<br>1 = Digital input                                                                                                                                                                                                                                                                                                                                                                         |
|                                        | 7:1   | IN1L_PGA_VOL[6:0]  | 0x40    | Input Path 1 (Left) PGA Volume (applicable to analog inputs only)<br>0x00 to 0x3F = Reserved                      0x42 = 2 dB                      0x60 to 0x7F = Reserved<br>0x40 = 0 dB                      ... (1-dB steps)<br>0x41 = 1 dB                      0x5F = 31 dB                                                                                                                                                   |
| R785 (0x0311)<br>ADC_Digital_Volume_1L | 14:13 | IN1L_SRC[1:0]      | 00      | Input Path 1 (Left) Source<br>00 = Differential (IN1ALP–IN1ALN)                      10 = Differential (IN1BP–IN1BN)<br>01 = Single-ended (IN1ALP)                      11 = Single-ended (IN1BP)                                                                                                                                                                                                                                  |
| R786 (0x0312)<br>DMIC1L_Control        | 10:8  | IN1_OSR[2:0]       | 101     | Input Path 1 DMIC Oversample Rate (applicable to digital inputs only).<br>000 = Reserved                      011 = 768 kHz                      110 = 6.144 MHz<br>001 = Reserved                      100 = 1.536 MHz                      111 = Reserved<br>010 = 384 kHz                      101 = 3.072 MHz<br>If IN1_OSR=010 or 011, the maximum Input Path sample rate (all input paths) is 48 kHz or 96 kHz respectively. |
|                                        | 5:0   | IN1L_DMIC_DLY[5:0] | 0x00    | Input Path 1 (Left) Digital Delay (applicable to digital input only)<br>LSB = 1 sample, Range is 0 to 63.<br>(Sample rate is controlled by IN1_OSR.)                                                                                                                                                                                                                                                                               |

**Table 4-3. Input Signal Path Configuration (Cont.)**

| Register Address                       | Bit   | Label              | Default | Description                                                                                                                                                                                                                                                                                                                                        |
|----------------------------------------|-------|--------------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R788 (0x0314)<br>IN1R_Control          | 15    | IN1R_HPFP          | 0       | Input Path 1 (Right) HPF Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                     |
|                                        | 7:1   | IN1R_PGA_VOL[6:0]  | 0x40    | Input Path 1 (Right) PGA Volume (applicable to analog inputs only)<br>0x00 to 0x3F = Reserved      0x42 = 2 dB      0x60 to 0x7F = Reserved<br>0x40 = 0 dB      ... (1-dB steps)<br>0x41 = 1 dB      0x5F = 31 dB                                                                                                                                  |
| R789 (0x0315)<br>ADC_Digital_Volume_1R | 14:13 | IN1R_SRC[1:0]      | 00      | Input Path 1 (Right) Source<br>00 = Differential (IN1ARP–IN1ARN)      10 = Differential (IN1BRP–IN1BRN)<br>01 = Single-ended (IN1ARP)      11 = Single-ended (IN1BRP)                                                                                                                                                                              |
| R790 (0x0316)<br>DMIC1R_Control        | 5:0   | IN1R_DMIC_DLY[5:0] | 0x00    | Input Path 1 (Right) Digital Delay (applicable to digital input only)<br>LSB = 1 sample, Range is 0 to 63.<br>(Sample rate is controlled by IN1_OSR.)                                                                                                                                                                                              |
| R792 (0x0318)<br>IN2L_Control          | 15    | IN2L_HPFP          | 0       | Input Path 2 (Left) HPF Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                      |
|                                        | 12:11 | IN2_DMIC_SUP[1:0]  | 00      | Input Path 2 DMIC Reference Select (sets the DMICDAT2 and DMICCLK2 logic levels)<br>00 = MICVDD      10 = MICBIAS2A<br>01 = MICBIAS1B      11 = MICBIAS2B                                                                                                                                                                                          |
|                                        | 10    | IN2_MODE           | 00      | Input Path 2 Mode<br>0 = Analog input<br>1 = Digital input                                                                                                                                                                                                                                                                                         |
|                                        | 7:1   | IN2L_PGA_VOL[6:0]  | 0x40    | Input Path 2 (Left) PGA Volume (applicable to analog inputs only)<br>0x00 to 0x3F = Reserved      0x42 = 2 dB      0x60 to 0x7F = Reserved<br>0x40 = 0 dB      ... (1-dB steps)<br>0x41 = 1 dB      0x5F = 31 dB                                                                                                                                   |
| R793 (0x0319)<br>ADC_Digital_Volume_2L | 14:13 | IN2L_SRC[1:0]      | 00      | Input Path 2 (Left) Source<br>00 = Differential (IN2LP–IN2LN)      10 = Reserved<br>01 = Single-ended (IN2LP)      11 = Reserved                                                                                                                                                                                                                   |
| R794 (0x031A)<br>DMIC2L_Control        | 10:8  | IN2_OSR[2:0]       | 101     | Input Path 2 DMIC Oversample Rate (applicable to digital inputs only).<br>000 = Reserved      011 = 768 kHz      110 = 6.144 MHz<br>001 = Reserved      100 = 1.536 MHz      111 = Reserved<br>010 = 384 kHz      101 = 3.072 MHz<br>If IN2_OSR=010 or 011, the maximum Input Path sample rate (all input paths) is 48 kHz or 96 kHz respectively. |
|                                        | 5:0   | IN2L_DMIC_DLY[5:0] | 0x00    | Input Path 2 (Left) Digital Delay (applicable to digital input only)<br>LSB = 1 sample, Range is 0 to 63.<br>(Sample rate is controlled by IN2_OSR.)                                                                                                                                                                                               |
| R796 (0x031C)<br>IN2R_Control          | 15    | IN2R_HPFP          | 0       | Input Path 2 (Right) HPF Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                     |
|                                        | 7:1   | IN2R_PGA_VOL[6:0]  | 0x40    | Input Path 2 (Right) PGA Volume (applicable to analog inputs only)<br>0x00 to 0x3F = Reserved      0x42 = 2 dB      0x60 to 0x7F = Reserved<br>0x40 = 0 dB      ... (1-dB steps)<br>0x41 = 1 dB      0x5F = 31 dB                                                                                                                                  |
| R797 (0x0319)<br>ADC_Digital_Volume_2R | 14:13 | IN2R_SRC[1:0]      | 00      | Input Path 2 (Right) Source<br>00 = Differential (IN2RP–IN2RN)      10 = Reserved<br>01 = Single-ended (IN2ARP)      11 = Reserved                                                                                                                                                                                                                 |
| R798 (0x031E)<br>DMIC2R_Control        | 5:0   | IN2R_DMIC_DLY[5:0] | 0x00    | Input Path 2 (Right) Digital Delay (applicable to digital input only)<br>LSB = 1 sample, Range is 0 to 63.<br>(Sample rate is controlled by IN2_OSR.)                                                                                                                                                                                              |

## 4.2.7 Input Signal Path Digital Volume Control

A digital volume control is provided on each input signal path, providing –64 dB to +31.5 dB gain control in 0.5-dB steps. An independent mute control is also provided for each input signal path.

Whenever the gain or mute setting is changed, the signal path gain is ramped up or down to the new settings at a programmable rate. For increasing gain (or unmute), the rate is controlled by IN\_VI\_RAMP. For decreasing gain (or mute), the rate is controlled by IN\_VD\_RAMP.

**Note:** The IN\_VI\_RAMP and IN\_VD\_RAMP fields should not be changed while a volume ramp is in progress.

The IN\_VU bits control the loading of the input signal path digital volume and mute controls. When IN\_VU is cleared, the digital volume and mute settings are loaded into the respective control register, but do not change the signal path gain. The digital volume and mute settings on all of the input signal paths are updated when a 1 is written to IN\_VU. This makes it possible to update the gain of multiple signal paths simultaneously.

Note that, although the digital-volume controls provide 0.5-dB steps, the internal circuits provide signal gain adjustment in 0.125-dB steps. This allows a very high degree of gain control and smooth volume ramping under all operating conditions.

**Note:** The 0 dBFS level of the IN1/IN2 digital input paths is not equal to the 0 dBFS level of the CS47L35 digital core. The maximum digital input signal level is –6 dBFS (see [Table 3-7](#)). Under 0 dB gain conditions, a –6 dBFS input signal corresponds to a 0 dBFS input to the CS47L35 digital core functions.

The digital volume control registers are described in [Table 4-4](#) and [Table 4-5](#).

**Table 4-4. Input Signal Path Digital Volume Control**

| Register Address                       | Bit | Label           | Default        | Description                                                                                                                                                                                                                                                                                                                                                  |
|----------------------------------------|-----|-----------------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R777 (0x0309)<br>Input_Volume_Ramp     | 6:4 | IN_VD_RAMP[2:0] | 010            | Input Volume Decreasing Ramp Rate (seconds/6 dB)<br>This field should not be changed while a volume ramp is in progress.<br>000 = 0 ms                      011 = 2 ms                      110 = 15 ms<br>001 = 0.5 ms                      100 = 4 ms                      111 = 30 ms<br>010 = 1 ms                      101 = 8 ms                       |
|                                        | 2:0 | IN_VI_RAMP[2:0] | 010            | Input Volume Increasing Ramp Rate (seconds/6 dB)<br>This field should not be changed while a volume ramp is in progress.<br>000 = 0 ms                      011 = 2 ms                      110 = 15 ms<br>001 = 0.5 ms                      100 = 4 ms                      111 = 30 ms<br>010 = 1 ms                      101 = 8 ms                       |
| R785 (0x0311)<br>ADC_Digital_Volume_1L | 9   | IN_VU           | See Footnote 1 | Input Signal Paths Volume and Mute Update. Writing 1 to this bit causes the Input Signal Paths Volume and Mute settings to be updated simultaneously                                                                                                                                                                                                         |
|                                        | 8   | IN1L_MUTE       | 1              | Input Path 1 (Left) Digital Mute<br>0 = Unmute<br>1 = Mute                                                                                                                                                                                                                                                                                                   |
|                                        | 7:0 | IN1L_VOL[7:0]   | 0x80           | Input Path 1 (Left) Digital Volume (see <a href="#">Table 4-5</a> for volume register definition).<br>–64 dB to +31.5 dB in 0.5-dB steps<br>0x00 = –64dB                      0x80 = 0 dB                      0xC0 to 0xFF = Reserved<br>0x01 = –63.5dB                      ... (0.5-dB steps)<br>... (0.5-dB steps)                      0xBF = +31.5 dB  |
| R789 (0x0315)<br>ADC_Digital_Volume_1R | 9   | IN_VU           | See Footnote 1 | Input Signal Paths Volume and Mute Update. Writing 1 to this bit causes the Input Signal Paths Volume and Mute settings to be updated simultaneously                                                                                                                                                                                                         |
|                                        | 8   | IN1R_MUTE       | 1              | Input Path 1 (Right) Digital Mute<br>0 = Unmute<br>1 = Mute                                                                                                                                                                                                                                                                                                  |
|                                        | 7:0 | IN1R_VOL[7:0]   | 0x80           | Input Path 1 (Right) Digital Volume (see <a href="#">Table 4-5</a> for volume register definition).<br>–64 dB to +31.5 dB in 0.5-dB steps<br>0x00 = –64dB                      0x80 = 0 dB                      0xC0 to 0xFF = Reserved<br>0x01 = –63.5dB                      ... (0.5-dB steps)<br>... (0.5-dB steps)                      0xBF = +31.5 dB |

**Table 4-4. Input Signal Path Digital Volume Control (Cont.)**

| Register Address                       | Bit | Label         | Default        | Description                                                                                                                                                                                                                                                                                                                                  |
|----------------------------------------|-----|---------------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R793 (0x0319)<br>ADC_Digital_Volume_2L | 9   | IN_VU         | See Footnote 1 | Input Signal Paths Volume and Mute Update. Writing 1 to this bit causes the Input Signal Paths Volume and Mute settings to be updated simultaneously                                                                                                                                                                                         |
|                                        | 8   | IN2L_MUTE     | 1              | Input Path 2 (Left) Digital Mute<br>0 = Unmute<br>1 = Mute                                                                                                                                                                                                                                                                                   |
|                                        | 7:0 | IN2L_VOL[7:0] | 0x80           | Input Path 2 (Left) Digital Volume (see Table 4-5 for volume register definition).<br>–64 dB to +31.5 dB in 0.5-dB steps<br>0x00 = –64dB                      0x80 = 0 dB                      0xC0 to 0xFF = Reserved<br>0x01 = –63.5dB                      ... (0.5-dB steps)<br>... (0.5-dB steps)                      0xBF = +31.5 dB  |
| R797 (0x031D)<br>ADC_Digital_Volume_2R | 9   | IN_VU         | See Footnote 1 | Input Signal Paths Volume and Mute Update. Writing 1 to this bit causes the Input Signal Paths Volume and Mute settings to be updated simultaneously                                                                                                                                                                                         |
|                                        | 8   | IN2R_MUTE     | 1              | Input Path 2 (Right) Digital Mute<br>0 = Unmute<br>1 = Mute                                                                                                                                                                                                                                                                                  |
|                                        | 7:0 | IN2R_VOL[7:0] | 0x80           | Input Path 2 (Right) Digital Volume (see Table 4-5 for volume register definition).<br>–64 dB to +31.5 dB in 0.5-dB steps<br>0x00 = –64dB                      0x80 = 0 dB                      0xC0 to 0xFF = Reserved<br>0x01 = –63.5dB                      ... (0.5-dB steps)<br>... (0.5-dB steps)                      0xBF = +31.5 dB |

1. Default is not applicable to these write-only bits

Table 4-5 lists the input signal path digital volume settings.

**Table 4-5. Input Signal Path Digital Volume Range**

| Input Volume Register | Volume (dB) | Input Volume Register | Volume (dB) | Input Volume Register | Volume (dB) | Input Volume Register | Volume (dB) |
|-----------------------|-------------|-----------------------|-------------|-----------------------|-------------|-----------------------|-------------|
| 0x00                  | –64.0       | 0x31                  | –39.5       | 0x62                  | –15.0       | 0x93                  | 9.5         |
| 0x01                  | –63.5       | 0x32                  | –39.0       | 0x63                  | –14.5       | 0x94                  | 10.0        |
| 0x02                  | –63.0       | 0x33                  | –38.5       | 0x64                  | –14.0       | 0x95                  | 10.5        |
| 0x03                  | –62.5       | 0x34                  | –38.0       | 0x65                  | –13.5       | 0x96                  | 11.0        |
| 0x04                  | –62.0       | 0x35                  | –37.5       | 0x66                  | –13.0       | 0x97                  | 11.5        |
| 0x05                  | –61.5       | 0x36                  | –37.0       | 0x67                  | –12.5       | 0x98                  | 12.0        |
| 0x06                  | –61.0       | 0x37                  | –36.5       | 0x68                  | –12.0       | 0x99                  | 12.5        |
| 0x07                  | –60.5       | 0x38                  | –36.0       | 0x69                  | –11.5       | 0x9A                  | 13.0        |
| 0x08                  | –60.0       | 0x39                  | –35.5       | 0x6A                  | –11.0       | 0x9B                  | 13.5        |
| 0x09                  | –59.5       | 0x3A                  | –35.0       | 0x6B                  | –10.5       | 0x9C                  | 14.0        |
| 0x0A                  | –59.0       | 0x3B                  | –34.5       | 0x6C                  | –10.0       | 0x9D                  | 14.5        |
| 0x0B                  | –58.5       | 0x3C                  | –34.0       | 0x6D                  | –9.5        | 0x9E                  | 15.0        |
| 0x0C                  | –58.0       | 0x3D                  | –33.5       | 0x6E                  | –9.0        | 0x9F                  | 15.5        |
| 0x0D                  | –57.5       | 0x3E                  | –33.0       | 0x6F                  | –8.5        | 0xA0                  | 16.0        |
| 0x0E                  | –57.0       | 0x3F                  | –32.5       | 0x70                  | –8.0        | 0xA1                  | 16.5        |
| 0x0F                  | –56.5       | 0x40                  | –32.0       | 0x71                  | –7.5        | 0xA2                  | 17.0        |
| 0x10                  | –56.0       | 0x41                  | –31.5       | 0x72                  | –7.0        | 0xA3                  | 17.5        |
| 0x11                  | –55.5       | 0x42                  | –31.0       | 0x73                  | –6.5        | 0xA4                  | 18.0        |
| 0x12                  | –55.0       | 0x43                  | –30.5       | 0x74                  | –6.0        | 0xA5                  | 18.5        |
| 0x13                  | –54.5       | 0x44                  | –30.0       | 0x75                  | –5.5        | 0xA6                  | 19.0        |
| 0x14                  | –54.0       | 0x45                  | –29.5       | 0x76                  | –5.0        | 0xA7                  | 19.5        |
| 0x15                  | –53.5       | 0x46                  | –29.0       | 0x77                  | –4.5        | 0xA8                  | 20.0        |
| 0x16                  | –53.0       | 0x47                  | –28.5       | 0x78                  | –4.0        | 0xA9                  | 20.5        |
| 0x17                  | –52.5       | 0x48                  | –28.0       | 0x79                  | –3.5        | 0xAA                  | 21.0        |
| 0x18                  | –52.0       | 0x49                  | –27.5       | 0x7A                  | –3.0        | 0xAB                  | 21.5        |
| 0x19                  | –51.5       | 0x4A                  | –27.0       | 0x7B                  | –2.5        | 0xAC                  | 22.0        |
| 0x1A                  | –51.0       | 0x4B                  | –26.5       | 0x7C                  | –2.0        | 0xAD                  | 22.5        |

**Table 4-5. Input Signal Path Digital Volume Range (Cont.)**

| Input Volume Register | Volume (dB) | Input Volume Register | Volume (dB) | Input Volume Register | Volume (dB) | Input Volume Register | Volume (dB) |
|-----------------------|-------------|-----------------------|-------------|-----------------------|-------------|-----------------------|-------------|
| 0x1B                  | -50.5       | 0x4C                  | -26.0       | 0x7D                  | -1.5        | 0xAE                  | 23.0        |
| 0x1C                  | -50.0       | 0x4D                  | -25.5       | 0x7E                  | -1.0        | 0xAF                  | 23.5        |
| 0x1D                  | -49.5       | 0x4E                  | -25.0       | 0x7F                  | -0.5        | 0xB0                  | 24.0        |
| 0x1E                  | -49.0       | 0x4F                  | -24.5       | 0x80                  | 0.0         | 0xB1                  | 24.5        |
| 0x1F                  | -48.5       | 0x50                  | -24.0       | 0x81                  | 0.5         | 0xB2                  | 25.0        |
| 0x20                  | -48.0       | 0x51                  | -23.5       | 0x82                  | 1.0         | 0xB3                  | 25.5        |
| 0x21                  | -47.5       | 0x52                  | -23.0       | 0x83                  | 1.5         | 0xB4                  | 26.0        |
| 0x22                  | -47.0       | 0x53                  | -22.5       | 0x84                  | 2.0         | 0xB5                  | 26.5        |
| 0x23                  | -46.5       | 0x54                  | -22.0       | 0x85                  | 2.5         | 0xB6                  | 27.0        |
| 0x24                  | -46.0       | 0x55                  | -21.5       | 0x86                  | 3.0         | 0xB7                  | 27.5        |
| 0x25                  | -45.5       | 0x56                  | -21.0       | 0x87                  | 3.5         | 0xB8                  | 28.0        |
| 0x26                  | -45.0       | 0x57                  | -20.5       | 0x88                  | 4.0         | 0xB9                  | 28.5        |
| 0x27                  | -44.5       | 0x58                  | -20.0       | 0x89                  | 4.5         | 0xBA                  | 29.0        |
| 0x28                  | -44.0       | 0x59                  | -19.5       | 0x8A                  | 5.0         | 0xBB                  | 29.5        |
| 0x29                  | -43.5       | 0x5A                  | -19.0       | 0x8B                  | 5.5         | 0xBC                  | 30.0        |
| 0x2A                  | -43.0       | 0x5B                  | -18.5       | 0x8C                  | 6.0         | 0xBD                  | 30.5        |
| 0x2B                  | -42.5       | 0x5C                  | -18.0       | 0x8D                  | 6.5         | 0xBE                  | 31.0        |
| 0x2C                  | -42.0       | 0x5D                  | -17.5       | 0x8E                  | 7.0         | 0xBF                  | 31.5        |
| 0x2D                  | -41.5       | 0x5E                  | -17.0       | 0x8F                  | 7.5         | 0xC0-0xFF             | Reserved    |
| 0x2E                  | -41.0       | 0x5F                  | -16.5       | 0x90                  | 8.0         |                       |             |
| 0x2F                  | -40.5       | 0x60                  | -16.0       | 0x91                  | 8.5         |                       |             |
| 0x30                  | -40.0       | 0x61                  | -15.5       | 0x92                  | 9.0         |                       |             |

## 4.2.8 DMIC Pin Configuration

DMIC operation on input paths IN1 and IN2 is selected using `INn_MODE`, as described in [Table 4-3](#). If DMIC is selected, the respective `DMICCLKn` and `DMICDATn` pins are configured as digital outputs and inputs, respectively.

The CS47L35 provides integrated pull-down resistors on each of the `DMICDATn` pins. This provides a flexible capability for interfacing with other devices.

The `DMICDAT1` and `DMICDAT2` pull-down resistors can be configured independently using the bits described in [Table 4-6](#). Note that, if the `DMICDATn` DMIC input paths are disabled, the pull-down is disabled on the respective pin.

**Table 4-6. DMIC Interface Pull-Down Control**

| Register Address                  | Bit | Label       | Default | Description                                               |
|-----------------------------------|-----|-------------|---------|-----------------------------------------------------------|
| R840 (0x0348)<br>Dig_Mic_Pad_Ctrl | 1   | DMICDAT2_PD | 0       | DMICDAT2 Pull-Down Control<br>0 = Disabled<br>1 = Enabled |
|                                   | 0   | DMICDAT1_PD | 0       | DMICDAT1 Pull-Down Control<br>0 = Disabled<br>1 = Enabled |

## 4.3 Digital Core

The CS47L35 digital core provides extensive mixing and processing capabilities for multiple signal paths. The configuration is highly flexible, and virtually every conceivable input/output connection can be supported between the available processing blocks.

The digital core provides parametric equalization (EQ) functions, DRC, low-/high-pass filters (LHPF), and programmable DSP capability. The DSP can support functions such as wind-noise, side-tone, or other programmable filters, also dynamic range control and compression, or virtual surround sound and other audio enhancements.

The CS47L35 supports multiple signal paths through the digital core. Stereo full-duplex sample-rate conversion is provided to allow digital audio to be routed between input (ADC) paths, output (DAC) paths, Digital Audio Interfaces (AIF1–AIF3) and SLIMbus paths operating at different sample rates.

The DSP functions are highly programmable, using application-specific control sequences. Note that the DSP configuration data is lost whenever the DCVDD power domain is removed; the DSP configuration data must be downloaded to the CS47L35 each time the device is powered up.

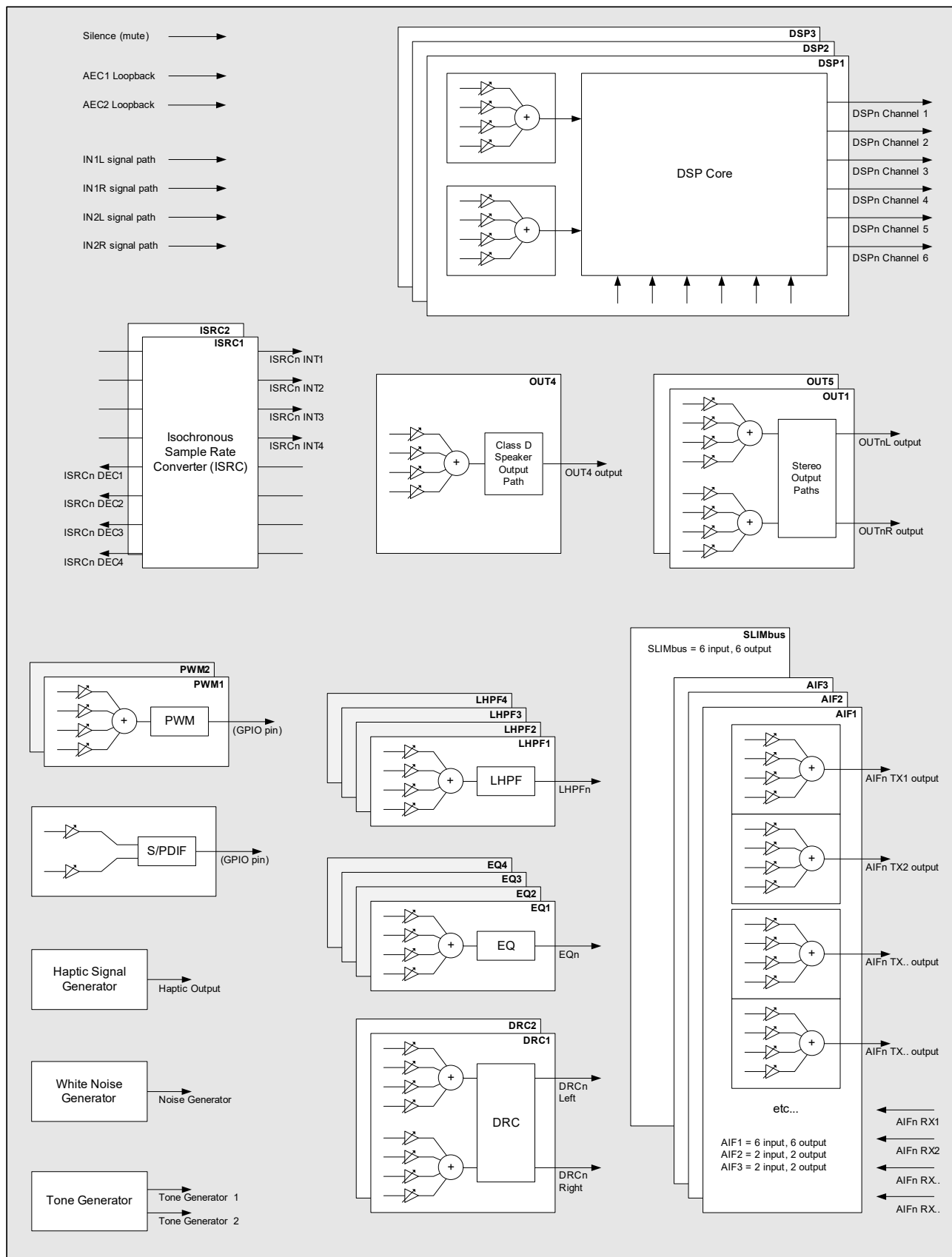
The procedure for configuring the CS47L35 DSP functions is tailored to each customer's application; please contact your Cirrus Logic representative for more details.

The digital core incorporates a S/PDIF transmitter that can provide a stereo S/PDIF output on a GPIO pin. Standard sample rates of 32–192 kHz can be supported. The CS47L35 incorporates a tone generator that can be used for beep functions through any of the audio signal paths. A white-noise generator is incorporated, to provide comfort noise in cases where silence (digital mute) is not desirable.

A haptic signal generator is provided, for use with external haptic devices (e.g., mechanical vibration actuators). Two pulse-width modulation (PWM) signal generators are also provided; the PWM waveforms can be modulated by an audio source within the digital core, and can be output on a GPIO pin.

An overview of the digital-core mixing and signal-processing functions is provided in [Fig. 4-11](#).

The control registers associated with the digital-core signal paths are shown in [Fig. 4-12](#) through [Fig. 4-27](#). The full list of digital mixer control registers (R1600–R2936) is provided in [Section 6](#). Generic register field definitions are provided in [Table 4-7](#).



**Figure 4-11. Digital Core**

### 4.3.1 Digital-Core Mixers

The CS47L35 provides an extensive digital mixing capability. The digital-core mixing and signal-processing blocks are shown in [Fig. 4-11](#). A four-input digital mixer is associated with many of these functions, as shown. The digital mixer circuit is identical in each instance, providing up to four selectable input sources, with independent volume control on each input.

The control registers associated with the digital-core signal paths are shown in [Fig. 4-12–Fig. 4-27](#). The full list of digital mixer control registers (R1600–R2936) is provided in [Section 6](#).

Further description of the associated control registers is provided throughout [Section 4.3](#). Generic register field definitions are provided in [Table 4-7](#).

The digital mixer input sources are selected using the associated `x_SRCn` fields; the volume control is implemented via the associated `x_VOLn` fields.

The ISRC and DSP auxiliary input functions support selectable input sources, but do not incorporate any digital mixing. The respective input source (`x_SRCn`) fields are identical to those of the digital mixers.

The `x_SRCn` fields select the input sources for the respective mixer or signal-processing block. Note that the selected input sources must be configured for the same sample rate as the blocks to which they are connected. Sample-rate conversion functions are available to support flexible interconnectivity; see [Section 4.3.14](#).

The `x_SRCn` fields for all digital core functions should be held at 0x00 if SYSCLK is not enabled—SYSCLK must be present and enabled before selecting other values for these fields. See [Section 4.16.4](#) for further details (including requirements for reconfiguring SYSCLK while digital core mixers are enabled).

A status bit is associated with each configurable input source. If an underclocked error condition occurs, these bits indicate which signal paths have been enabled.

The generic register field definition for the digital mixers is provided in [Table 4-7](#).

**Table 4-7. Digital-Core Mixer Control Registers**

| Register Address                       | Bit | Label                                                                                                            | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|----------------------------------------|-----|------------------------------------------------------------------------------------------------------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1600 (0x0640)<br>to<br>R2936 (0x0B78) | 15  | x_STS <i>n</i><br>Valid for every digital core function input (digital mixers, DSP aux inputs, and ISRC inputs). | 0       | [Digital Core function] input <i>n</i> status<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                                        | 7:1 | x_VOL <i>n</i><br>Valid for every digital mixer input.                                                           | 0x40    | [Digital Core mixer] input <i>n</i> volume. (–32 dB to +16 dB in 1-dB steps)<br>0x00 to 0x20 = –32 dB ... (1-dB steps) 0x50 = +16 dB<br>0x21 = –31 dB 0x40 = 0 dB 0x51 to 0x7F = +16 dB<br>0x22 = –30 dB ... (1-dB steps)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|                                        | 7:0 | x_SRC <i>n</i><br>Valid for every digital core function input (digital mixers, DSP aux inputs, and ISRC inputs). | 0x00    | [Digital Core function] input <i>n</i> source select<br>0x00 = Silence (mute) 0x3C = SLIMbus RX5 0x75 = DSP2 Channel 6<br>0x04 = Tone generator 1 0x3D = SLIMbus RX6 0x78 = DSP3 Channel 1<br>0x05 = Tone generator 2 0x50 = EQ1 0x79 = DSP3 Channel 2<br>0x06 = Haptic generator 0x51 = EQ2 0x7A = DSP3 Channel 3<br>0x08 = AEC Loop-Back 1 0x52 = EQ3 0x7B = DSP3 Channel 4<br>0x09 = AEC Loop-Back 2 0x53 = EQ4 0x7C = DSP3 Channel 5<br>0x0D = Noise generator 0x58 = DRC1 Left 0x7D = DSP3 Channel 6<br>0x10 = IN1L signal path 0x59 = DRC1 Right 0xA0 = ISRC1 INT1<br>0x11 = IN1R signal path 0x5A = DRC2 Left 0xA1 = ISRC1 INT2<br>0x12 = IN2L signal path 0x5B = DRC2 Right 0xA2 = ISRC1 INT3<br>0x13 = IN2R signal path 0x60 = LHPF1 0xA3 = ISRC1 INT4<br>0x20 = AIF1 RX1 0x61 = LHPF2 0xA4 = ISRC1 DEC1<br>0x21 = AIF1 RX2 0x62 = LHPF3 0xA5 = ISRC1 DEC2<br>0x22 = AIF1 RX3 0x63 = LHPF4 0xA6 = ISRC1 DEC3<br>0x23 = AIF1 RX4 0x68 = DSP1 Channel 1 0xA7 = ISRC1 DEC4<br>0x24 = AIF1 RX5 0x69 = DSP1 Channel 2 0xA8 = ISRC2 INT1<br>0x25 = AIF1 RX6 0x6A = DSP1 Channel 3 0xA9 = ISRC2 INT2<br>0x28 = AIF2 RX1 0x6B = DSP1 Channel 4 0xAA = ISRC2 INT3<br>0x29 = AIF2 RX2 0x6C = DSP1 Channel 5 0xAB = ISRC2 INT4<br>0x30 = AIF3 RX1 0x6D = DSP1 Channel 6 0xAC = ISRC2 DEC1<br>0x31 = AIF3 RX2 0x70 = DSP2 Channel 1 0xAD = ISRC2 DEC2<br>0x38 = SLIMbus RX1 0x71 = DSP2 Channel 2 0xAE = ISRC2 DEC3<br>0x39 = SLIMbus RX2 0x72 = DSP2 Channel 3 0xAF = ISRC2 DEC4<br>0x3A = SLIMbus RX3 0x73 = DSP2 Channel 4<br>0x3B = SLIMbus RX4 0x74 = DSP2 Channel 5 |

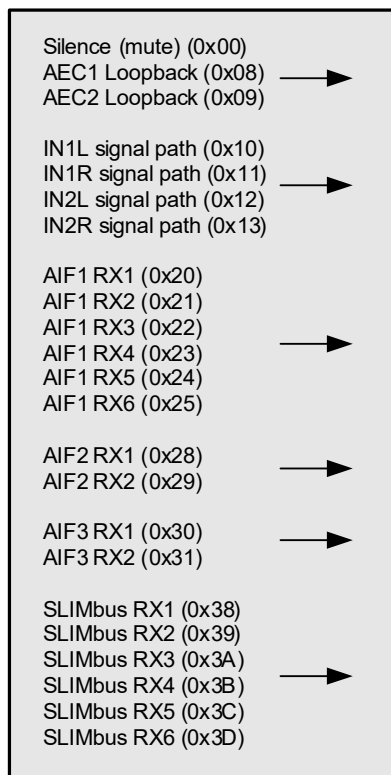
### 4.3.2 Digital-Core Inputs

The digital core comprises multiple input paths, as shown in [Fig. 4-12](#). Any of these inputs may be selected as a source to the digital mixers or signal-processing functions within the CS47L35 digital core.

Note that the outputs from other blocks within the digital core may also be selected as input to the digital mixers or signal-processing functions within the CS47L35 digital core. Those input sources, which are not shown in [Fig. 4-12](#), are described separately throughout [Section 4.3](#).

The hexadecimal numbers in [Fig. 4-12](#) indicate the corresponding x\_SRC*n* setting for selection of that signal as an input to another digital-core function.

The sample rate for the input signal paths is configured by using the applicable IN\_RATE, AIF*n*\_RATE, or SLIMRX*n*\_RATE field; see [Table 4-21](#). Note that sample-rate conversion is required when routing the input signal paths to any signal chain that is configured for a different sample rate.



**Figure 4-12. Digital-Core Inputs**

### 4.3.3 Digital-Core Output Mixers

The digital core comprises multiple output paths. The output paths associated with AIF1–AIF3 are shown in [Fig. 4-13](#). The output paths associated with OUT1, OUT4, and OUT5 are shown in [Fig. 4-14](#). The output paths associated with the SLIMbus interface are shown in [Fig. 4-15](#).

A four-input mixer is associated with each output. The four input sources are selectable in each case, and independent volume control is provided for each path.

The AIF1–AIF3 output mixer control fields (see [Fig. 4-13](#)) are located at register addresses R1792–R1935 (0x0700–0x078F). The OUT1, OUT4, and OUT5 output mixer control fields (see [Fig. 4-14](#)) are located at addresses R1664–R1743 (0x0680–0x06CF). The SLIMbus output mixer control fields (see [Fig. 4-15](#)) are located at addresses R1984–R2031 (0x07C0–0x07EF).

The full list of digital mixer control registers (R1600–R2936) is provided in [Section 6](#). Generic register field definitions are provided in [Table 4-7](#).

The `x_SRCn` fields select the input sources for the respective mixers. Note that the selected input sources must be configured for the same sample rate as the mixer to which they are connected. Sample-rate conversion functions are available to support flexible interconnectivity; see [Section 4.3.14](#).

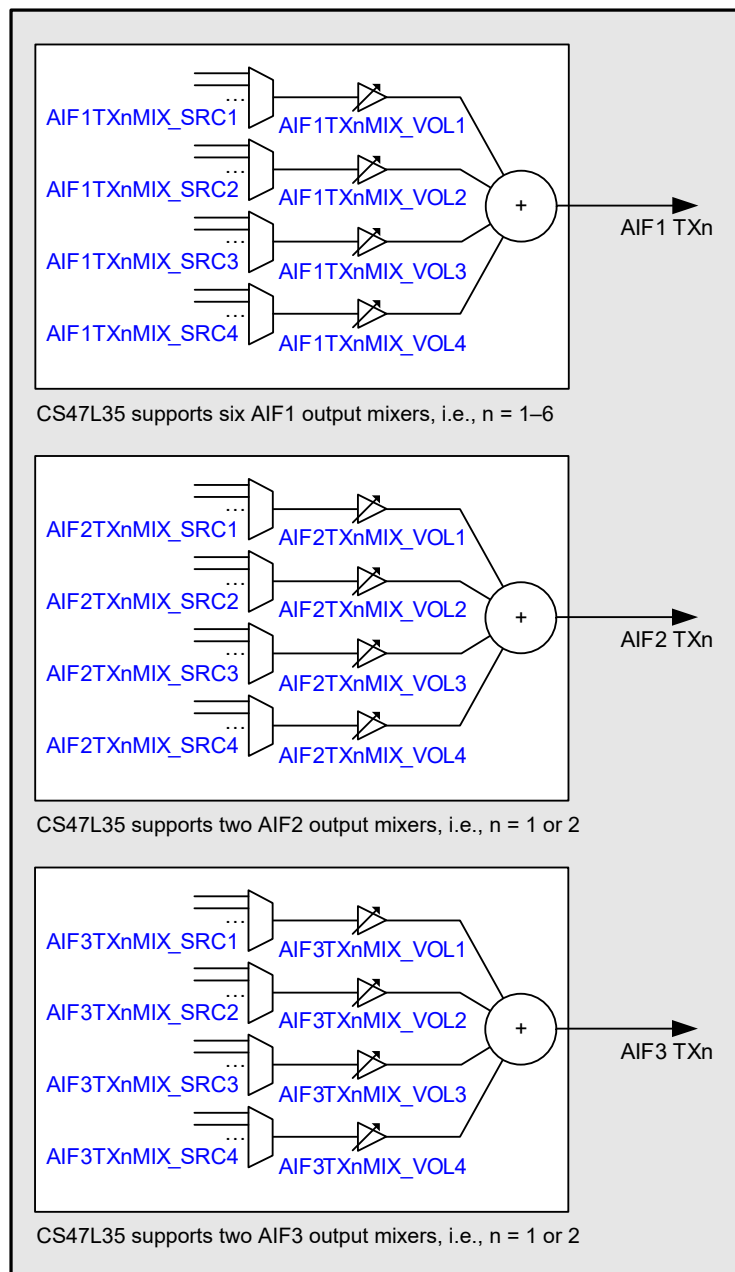
The `x_SRCn` fields for all digital core functions should be held at 0x00 if SYSCLK is not enabled—SYSCLK must be present and enabled before selecting other values for these fields. See [Section 4.16.4](#) for further details (including requirements for reconfiguring SYSCLK while digital core mixers are enabled).

The sample rate for the output signal paths is configured using the applicable `OUT_RATE`, `AIFn_RATE`, or `SLIMTXn_RATE` fields; see [Table 4-21](#). Note that sample-rate conversion is required when routing the output signal paths to any signal chain that is configured for a different sample rate.

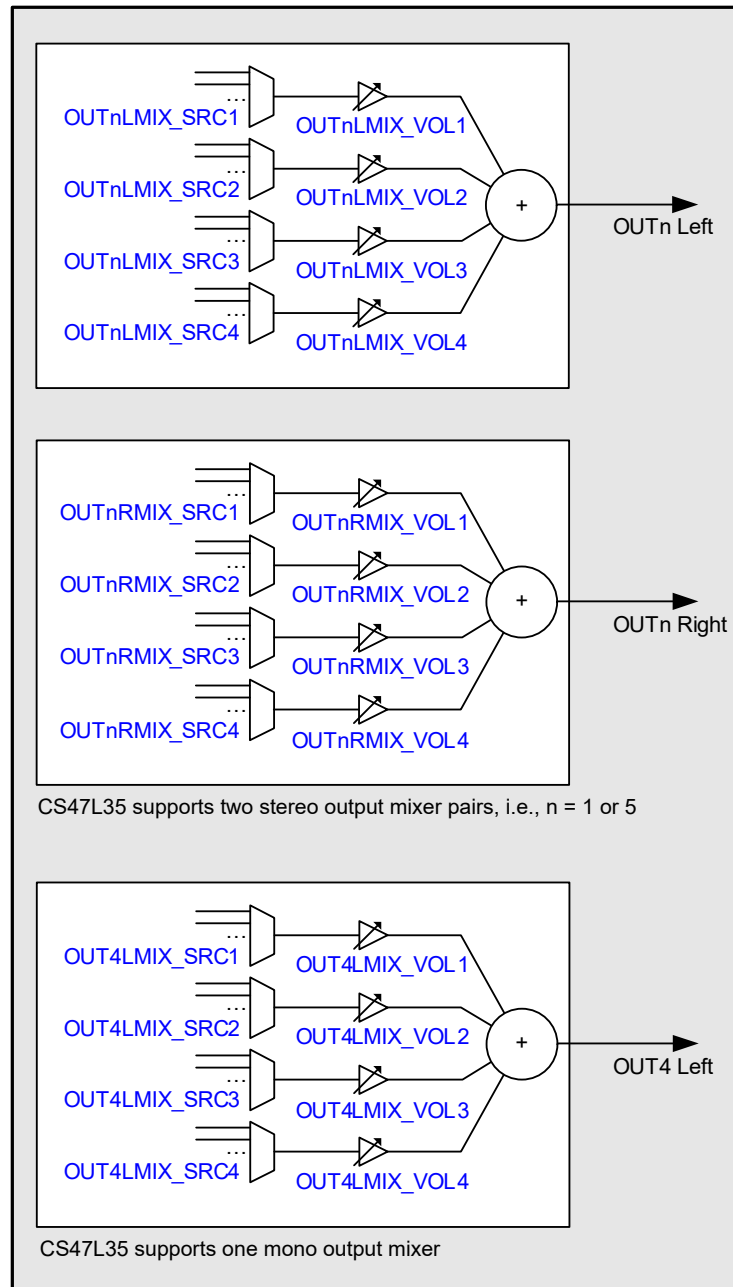
The OUT\_RATE, AIFn\_RATE, or SLIMTXn\_RATE fields must not be changed if any of the respective x\_SRCn fields is nonzero. The associated x\_SRCn fields must be cleared before writing new values to OUT\_RATE, AIFn\_RATE, or SLIMTXn\_RATE. A minimum delay of 125  $\mu$ s must be allowed between clearing the x\_SRCn fields and writing to the associated OUT\_RATE, AIFn\_RATE, or SLIMTXn\_RATE fields. See [Table 4-21](#) for details.

The CS47L35 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the output mixer paths. If the frequency is too low, an attempt to enable an output mixer path fails. Note that active signal paths are not affected under such circumstances.

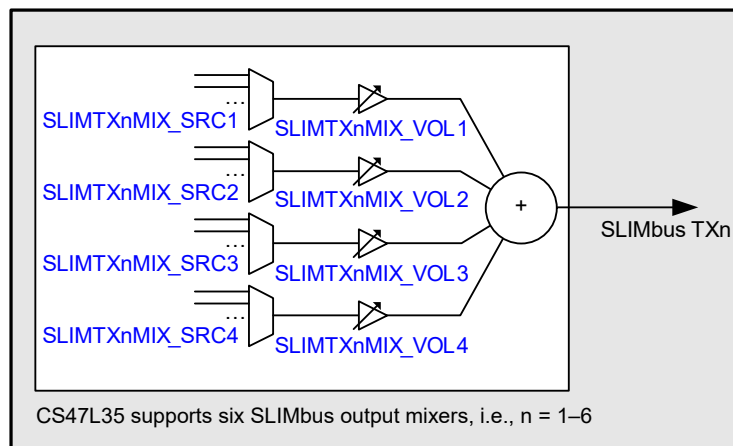
The status bits in registers R1600–R2936 indicate the status of each of the digital mixers. If an underclocked error condition occurs, these bits indicate which mixers have been enabled.



**Figure 4-13. Digital-Core AIF Outputs**



**Figure 4-14. Digital-Core OUTn Outputs**



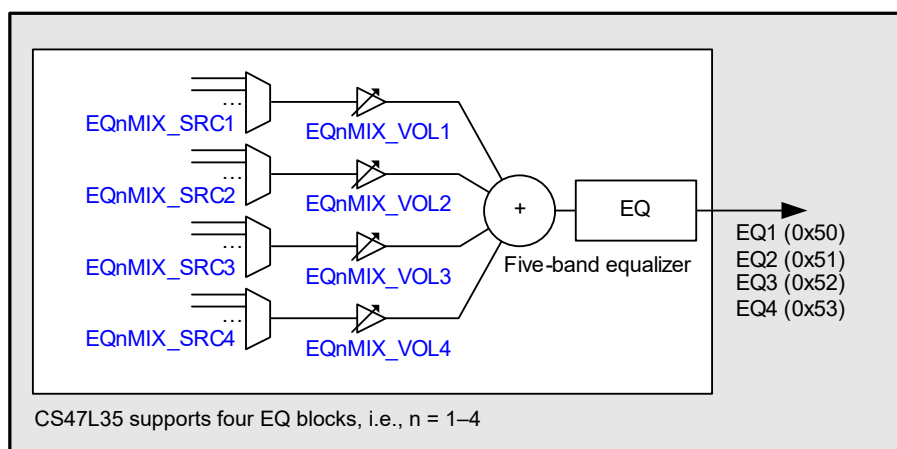
**Figure 4-15. Digital-Core SLIMbus Outputs**

### 4.3.4 Five-Band Parametric Equalizer (EQ)

The digital core provides four EQ processing blocks as shown in Fig. 4-16. A four-input mixer is associated with each EQ. The four input sources are selectable in each case, and independent volume control is provided for each path. Each EQ block supports one output.

The EQ provides selective control of five frequency bands as follows:

- The low-frequency band (Band 1) filter can be configured as a peak filter or as a shelving filter. If configured as a shelving filter, it provides adjustable gain below the Band 1 cut-off frequency. As a peak filter, it provides adjustable gain within a defined frequency band that is centered on the Band 1 frequency.
- The midfrequency bands (Band 2–Band 4) filters are peak filters that provide adjustable gain around the respective center frequency.
- The high-frequency band (Band 5) filter is a shelving filter that provides adjustable gain above the Band 5 cut-off frequency.



**Figure 4-16. Digital-Core EQ Blocks**

The EQ1–EQ4 mixer control fields (see Fig. 4-16) are located at register addresses R2176–R2207 (0x0880–0x089F).

The full list of digital-mixer control registers (R1600–R2936) is provided in Section 6. Generic register field definitions are provided in Table 4-7.

The  $x\_SRCn$  fields select the input sources for the respective EQ processing blocks. Note that the selected input sources must be configured for the same sample rate as the EQ to which they are connected. Sample-rate conversion functions are available to support flexible interconnectivity; see Section 4.3.14.

The hexadecimal numbers in [Fig. 4-16](#) indicate the corresponding x\_SRCn setting for selection of that signal as an input to another digital-core function.

The EQ blocks should be kept disabled (EQn\_ENA = 0) if SYSCLK is not enabled. The x\_SRCn fields for all digital core functions should be held at 0x00 if SYSCLK is not enabled. SYSCLK must be present and enabled before selecting other values for these fields. See [Section 4.16.4](#) for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The sample rate for the EQ function is configured using FX\_RATE; see [Table 4-21](#). Note that the EQ, DRC, and LHPF functions must be configured for the same sample rate. Sample-rate conversion is required when routing the EQ signal paths to any signal chain that is configured for a different sample rate.

The FX\_RATE field must not be changed if any of the associated x\_SRCn fields is nonzero. The associated x\_SRCn fields must be cleared before writing a new value to FX\_RATE. A minimum delay of 125  $\mu$ s must be allowed between clearing the x\_SRCn fields and writing to FX\_RATE. See [Table 4-21](#) for details.

The cut-off or center frequencies for the five-band EQ are set by using the coefficients held in the registers identified in [Table 4-8](#). These coefficients are derived using tools provided in Cirrus Logic's WISCE™ evaluation-board control software; please contact your Cirrus Logic representative for details.

**Table 4-8. EQ Coefficient Registers**

| EQ  | Register Addresses               |
|-----|----------------------------------|
| EQ1 | R3602 (0x0E10) to R3620 (0x0E24) |
| EQ2 | R3624 (0x0E28) to R3642 (0x0E3A) |
| EQ3 | R3646 (0x0E3E) to R3664 (0x0E53) |
| EQ4 | R3668 (0x0E54) to R3686 (0x0E66) |

The control registers associated with the EQ functions are described in [Table 4-9](#).

**Table 4-9. EQ Enable and Gain Control**

| Register Address                    | Bit   | Label                                                    | Default | Description                                                                                                                                                                                                                                                                                                                                                                   |
|-------------------------------------|-------|----------------------------------------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R3585 (0x0E01)<br>FX_Ctrl2          | 15:4  | FX_STS[11:0]                                             | 0x00    | LHPF, DRC, EQ Enable Status. Indicates the status of each of the respective signal-processing functions. Each bit is coded as follows:<br>0 = Disabled<br>1 = Enabled<br>[11] = EQ4<br>[10] = EQ3<br>[9] = EQ2<br>[8] = EQ1<br>[7] = DRC2 (Right)<br>[6] = DRC2 (Left)<br>[5] = DRC1 (Right)<br>[4] = DRC1 (Left)<br>[3] = LHPF4<br>[2] = LHPF3<br>[1] = LHPF2<br>[0] = LHPF1 |
| R3600 (0x0E10)<br>EQ1_1             | 15:11 | EQ1_B1_GAIN[4:0]                                         | 0x0C    | EQ1 Band 1 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                                                                                                                                                                                                                                                                                 |
|                                     | 10:6  | EQ1_B2_GAIN[4:0]                                         | 0x0C    | EQ1 Band 2 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                                                                                                                                                                                                                                                                                 |
|                                     | 5:1   | EQ1_B3_GAIN[4:0]                                         | 0x0C    | EQ1 Band 3 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                                                                                                                                                                                                                                                                                 |
|                                     | 0     | EQ1_ENA                                                  | 0       | EQ1 Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                     |
| R3601 (0x0E11)<br>EQ1_2             | 15:11 | EQ1_B4_GAIN[4:0]                                         | 0x0C    | EQ1 Band 4 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                                                                                                                                                                                                                                                                                 |
|                                     | 10:6  | EQ1_B5_GAIN[4:0]                                         | 0x0C    | EQ1 Band 5 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                                                                                                                                                                                                                                                                                 |
|                                     | 0     | EQ1_B1_MODE                                              | 0       | EQ1 Band 1 Mode<br>0 = Shelving filter<br>1 = Peak filter                                                                                                                                                                                                                                                                                                                     |
| R3602 (0x0E12) to<br>R3620 (0x0E24) | 15:0  | EQ1_B1_*<br>EQ1_B2_*<br>EQ1_B3_*<br>EQ1_B4_*<br>EQ1_B5_* | —       | EQ1 Frequency Coefficients. Refer to WISCE evaluation board control software for the derivation of these field values.                                                                                                                                                                                                                                                        |

**Table 4-9. EQ Enable and Gain Control (Cont.)**

| Register Address                    | Bit   | Label                                                    | Default | Description                                                                                                              |
|-------------------------------------|-------|----------------------------------------------------------|---------|--------------------------------------------------------------------------------------------------------------------------|
| R3622 (0x0E26)<br>EQ2_1             | 15:11 | EQ2_B1_GAIN[4:0]                                         | 0x0C    | EQ2 Band 1 Gain <sup>1</sup><br>–12 dB to +12 dB in 1-dB steps                                                           |
|                                     | 10:6  | EQ2_B2_GAIN[4:0]                                         | 0x0C    | EQ2 Band 2 Gain <sup>1</sup><br>–12 dB to +12 dB in 1-dB steps                                                           |
|                                     | 5:1   | EQ2_B3_GAIN[4:0]                                         | 0x0C    | EQ2 Band 3 Gain <sup>1</sup><br>–12 dB to +12 dB in 1-dB steps                                                           |
|                                     | 0     | EQ2_ENA                                                  | 0       | EQ2 Enable<br>0 = Disabled<br>1 = Enabled                                                                                |
| R3623 (0x0E27)<br>EQ2_2             | 15:11 | EQ2_B4_GAIN[4:0]                                         | 0x0C    | EQ2 Band 4 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                            |
|                                     | 10:6  | EQ2_B5_GAIN[4:0]                                         | 0x0C    | EQ2 Band 5 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                            |
|                                     | 0     | EQ2_B1_MODE                                              | 0       | EQ2 Band 1 Mode<br>0 = Shelving filter<br>1 = Peak filter                                                                |
| R3624 (0x0E28) to<br>R3642 (0x0E3A) | 15:0  | EQ2_B1_*<br>EQ2_B2_*<br>EQ2_B3_*<br>EQ2_B4_*<br>EQ2_B5_* | —       | EQ2 Frequency Coefficients. Refer to WISCE evaluation board control software for the derivation of these field values.   |
| R3644 (0x0E3C)<br>EQ3_1             | 15:11 | EQ3_B1_GAIN[4:0]                                         | 0x0C    | EQ3 Band 1 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                            |
|                                     | 10:6  | EQ3_B2_GAIN[4:0]                                         | 0x0C    | EQ3 Band 2 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                            |
|                                     | 5:1   | EQ3_B3_GAIN[4:0]                                         | 0x0C    | EQ3 Band 3 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                            |
|                                     | 0     | EQ3_ENA                                                  | 0       | EQ3 Enable<br>0 = Disabled<br>1 = Enabled                                                                                |
| R3645 (0x0E3D)<br>EQ3_2             | 15:11 | EQ3_B4_GAIN[4:0]                                         | 0x0C    | EQ3 Band 4 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                            |
|                                     | 10:6  | EQ3_B5_GAIN[4:0]                                         | 0x0C    | EQ3 Band 5 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                            |
|                                     | 0     | EQ3_B1_MODE                                              | 0       | EQ3 Band 1 Mode<br>0 = Shelving filter<br>1 = Peak filter                                                                |
| R3646 (0x0E3E) to<br>R3664 (0x0E50) | 15:0  | EQ3_B1_*<br>EQ3_B2_*<br>EQ3_B3_*<br>EQ3_B4_*<br>EQ3_B5_* | —       | EQ3 Frequency Coefficients. Refer to WISCE evaluation board control software for the derivation of these field values.   |
| R3666 (0x0E52)<br>EQ4_1             | 15:11 | EQ4_B1_GAIN[4:0]                                         | 0x0C    | EQ4 Band 1 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                            |
|                                     | 10:6  | EQ4_B2_GAIN[4:0]                                         | 0x0C    | EQ4 Band 2 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                            |
|                                     | 5:1   | EQ4_B3_GAIN[4:0]                                         | 0x0C    | EQ4 Band 3 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                            |
|                                     | 0     | EQ4_ENA                                                  | 0       | EQ4 Enable<br>0 = Disabled<br>1 = Enabled                                                                                |
| R3667 (0x0E53)<br>EQ4_2             | 15:11 | EQ4_B4_GAIN[4:0]                                         | 0x0C    | EQ4 Band 4 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                            |
|                                     | 10:6  | EQ4_B5_GAIN[4:0]                                         | 0x0C    | EQ4 Band 5 Gain <sup>1</sup> (–12 dB to +12 dB in 1-dB steps)                                                            |
|                                     | 0     | EQ4_B1_MODE                                              | 0       | EQ4 Band 1 Mode<br>0 = Shelving filter<br>1 = Peak filter                                                                |
| R3668 (0x0E54) to<br>R3686 (0x0E66) | 15:0  | EQ4_B1_*<br>EQ4_B2_*<br>EQ4_B3_*<br>EQ4_B4_*<br>EQ4_B5_* | —       | EQ4 Frequency Coefficients<br>Refer to WISCE evaluation board control software for the derivation of these field values. |

1. See Table 4-10 for gain range.

Table 4-10 lists the EQ gain control settings.

**Table 4-10. EQ Gain-Control Range**

| EQ Gain Setting | Gain (dB) | EQ Gain Setting | Gain (dB) |
|-----------------|-----------|-----------------|-----------|
| 00000           | –12       | 01101           | +1        |
| 00001           | –11       | 01110           | +2        |
| 00010           | –10       | 01111           | +3        |
| 00011           | –9        | 10000           | +4        |
| 00100           | –8        | 10001           | +5        |
| 00101           | –7        | 10010           | +6        |
| 00110           | –6        | 10011           | +7        |
| 00111           | –5        | 10100           | +8        |
| 01000           | –4        | 10101           | +9        |
| 01001           | –3        | 10110           | +10       |
| 01010           | –2        | 10111           | +11       |
| 01011           | –1        | 11000           | +12       |
| 01100           | 0         | 11001–11111     | Reserved  |

The CS47L35 automatically checks to confirm whether the SYSCLK frequency is high enough to support the commanded EQ and digital mixing functions. If an attempt is made to enable an EQ signal path, and there are insufficient SYSCLK cycles to support it, the attempt does not succeed. Note that any signal paths that are already active are not affected under such circumstances.

The FX\_STS field in register R3585 indicates the status of each of the EQ, DRC, and LHPF signal paths. If an underclocked error condition occurs, this field indicates which EQ, DRC, or LHPF signal paths have been enabled.

The status bits in registers R1600–R2936 indicate the status of each of the digital mixers. If an underclocked error condition occurs, these bits indicate which mixers have been enabled.

### 4.3.5 Dynamic Range Control (DRC)

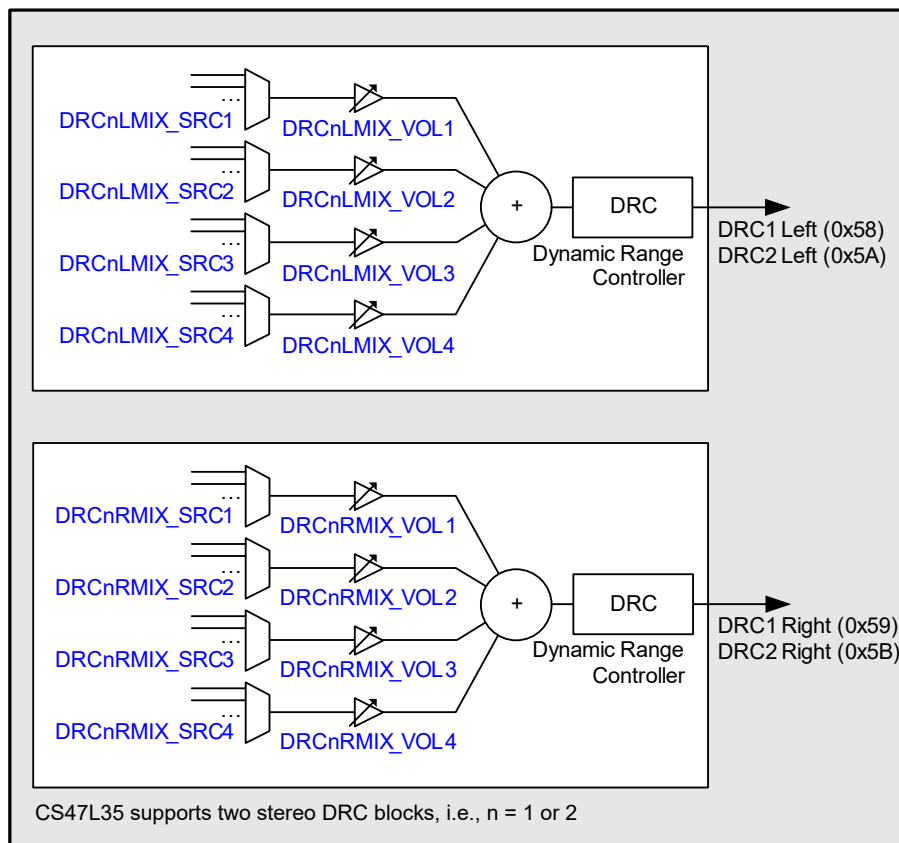
The digital core provides two stereo DRC processing blocks, as shown in [Fig. 4-17](#). A four-input mixer is associated with each DRC input channel. The input sources are selectable in each case, and independent volume control is provided for each path. The stereo DRC blocks support two outputs each.

The function of the DRC is to adjust the signal gain in conditions where the input amplitude is unknown or varies over a wide range, for example, when recording from microphones built into a handheld system or to restrict the dynamic range of an output signal path.

To improve intelligibility in the presence of loud impulsive noises, the DRC can apply compression and automatic level control to the signal path. It incorporates anticlip and quick-release features for handling transients.

The DRC also incorporates a noise-gate function that provides additional attenuation of very low-level input signals. This means that the signal path is quiet when no signal is present, giving an improvement in background noise level under these conditions.

A signal-detect function is provided within the DRC; this can be used to detect the presence of an audio signal and to trigger other events. It can also be used as an interrupt event or to trigger the control-write sequencer. Note that DRC triggering of the control-write sequencer is supported for DRC1 only.



**Figure 4-17. Dynamic Range Control (DRC) Block**

The DRC1 and DRC2 mixer control fields (see Fig. 4-17) are located at register addresses R2240–R2271 (0x08C0–0x08DF).

The full list of digital mixer control registers (R1600–R2936) is provided in Section 6. Generic register field definitions are provided in Table 4-7.

The  $x\_SRCn$  fields select the input sources for the respective DRC processing blocks. Note that the selected input sources must be configured for the same sample rate as the DRC to which they are connected. Sample-rate conversion functions are available to support flexible interconnectivity; see Section 4.3.14.

The hexadecimal numbers in Fig. 4-17 indicate the corresponding  $x\_SRCn$  setting for selection of that signal as an input to another digital-core function.

The DRC blocks should be kept disabled ( $DRCnx\_ENA = 0$ ) if SYSCLK is not enabled. The  $x\_SRCn$  fields for all digital core functions should be held at 0x00 if SYSCLK is not enabled. SYSCLK must be present and enabled before selecting other values for these fields. See Section 4.16.4 for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The sample rate for the DRC function is configured using  $FX\_RATE$ ; see Table 4-21. Note that the EQ, DRC, and LHPF functions must all be configured for the same sample rate. Sample-rate conversion is required when routing the DRC signal paths to any signal chain that is configured for a different sample rate.

The  $FX\_RATE$  field must not be changed if any of the associated  $x\_SRCn$  fields is nonzero. The associated  $x\_SRCn$  fields must be cleared before writing a new value to  $FX\_RATE$ . A minimum delay of 125  $\mu s$  must be allowed between clearing the  $x\_SRCn$  fields and writing to  $FX\_RATE$ . See Table 4-21 for details.

The DRC functions are enabled using the control registers described in Table 4-11.

**Table 4-11. DRC Enable**

| Register Address             | Bit | Label     | Default | Description                                        |
|------------------------------|-----|-----------|---------|----------------------------------------------------|
| R3712 (0x0E80)<br>DRC1_ctrl1 | 1   | DRC1L_ENA | 0       | DRC1 (left) enable<br>0 = Disabled<br>1 = Enabled  |
|                              | 0   | DRC1R_ENA | 0       | DRC1 (right) enable<br>0 = Disabled<br>1 = Enabled |
| R3720 (0x0E88)<br>DRC2_ctrl1 | 1   | DRC2L_ENA | 0       | DRC2 (left) enable<br>0 = Disabled<br>1 = Enabled  |
|                              | 0   | DRC2R_ENA | 0       | DRC2 (right) enable<br>0 = Disabled<br>1 = Enabled |

The following description of the DRC is applicable to each of the DRCs. The associated control fields are described in [Table 4-13](#) and [Table 4-14](#) for DRC1 and DRC2.

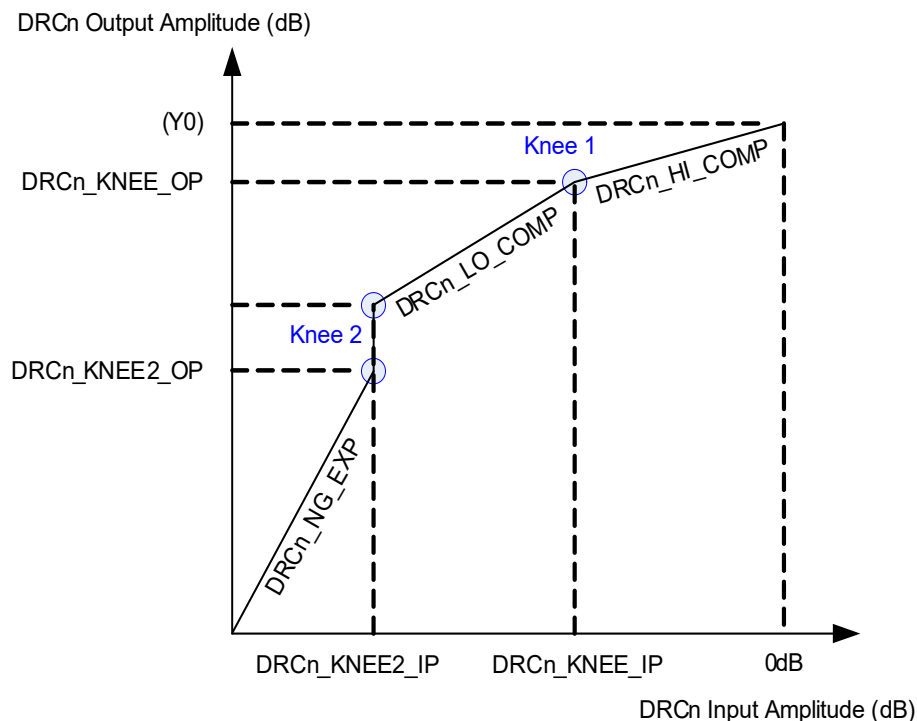
#### 4.3.5.1 DRC Compression, Expansion, and Limiting

The DRC supports two different compression regions, separated by a knee at a specific input amplitude. In the region above the knee, the compression slope  $DRCn\_HI\_COMP$  applies; in the region below the knee, the compression slope  $DRCn\_LO\_COMP$  applies. Note that  $n$  identifies the applicable DRC 1 or 2.

The DRC also supports a noise-gate region, where low-level input signals are heavily attenuated. This function can be enabled or disabled according to the application requirements. The DRC response in this region is defined by the expansion slope  $DRCn\_NG\_EXP$ .

For additional attenuation of signals in the noise-gate region, an additional knee can be defined (shown as Knee 2 in [Fig. 4-18](#)). When this knee is enabled, this introduces an infinitely steep drop-off in the DRC response pattern between the  $DRCn\_LO\_COMP$  and  $DRCn\_NG\_EXP$  regions.

The overall DRC compression characteristic in steady state (i.e., where the input amplitude is near constant) is shown in [Fig. 4-18](#).



**Figure 4-18. DRC Response Characteristic**

The slope of the DRC response is determined by `DRCn_HI_COMP` and `DRCn_LO_COMP`. A slope of 1 indicates constant gain in this region. A slope less than 1 represents compression (i.e., a change in input amplitude produces only a smaller change in output amplitude). A slope of 0 indicates that the target output amplitude is the same across a range of input amplitudes; this is infinite compression.

When the noise gate is enabled, the DRC response in this region is determined by `DRCn_NG_EXP`. A slope of 1 indicates constant gain in this region. A slope greater than 1 represents expansion (i.e., a change in input amplitude produces a larger change in output amplitude).

When the `DRCn_KNEE2_OP` knee is enabled (Knee 2 in [Fig. 4-18](#)), this introduces the vertical line in the response pattern shown, resulting in infinitely steep attenuation at this point in the response.

The DRC parameters are listed in [Table 4-12](#).

**Table 4-12. DRC Response Parameters**

| Parameters | Parameter                  | Description                    |
|------------|----------------------------|--------------------------------|
| 1          | <code>DRCn_KNEE_IP</code>  | Input level at Knee 1 (dB)     |
| 2          | <code>DRCn_KNEE_OP</code>  | Output level at Knee 2 (dB)    |
| 3          | <code>DRCn_HI_COMP</code>  | Compression ratio above Knee 1 |
| 4          | <code>DRCn_LO_COMP</code>  | Compression ratio below Knee 1 |
| 5          | <code>DRCn_KNEE2_IP</code> | Input level at Knee 2 (dB)     |
| 6          | <code>DRCn_NG_EXP</code>   | Expansion ratio below Knee 2   |
| 7          | <code>DRCn_KNEE2_OP</code> | Output level at Knee 2 (dB)    |

The noise gate is enabled by setting `DRCn_NG_ENA`. When the noise gate is not enabled, Parameters 5–7 (see [Table 4-12](#)) are ignored, and the `DRCn_LO_COMP` slope applies to all input signal levels below Knee 1.

The `DRCn_KNEE2_OP` knee is enabled by setting `DRCn_KNEE2_OP_ENA`. If this bit is not set, Parameter 7 is ignored and the Knee 2 position always coincides with the low end of the `DRCn_LO_COMP` region.

The Knee 1 point in [Fig. 4-18](#) is determined by `DRCn_KNEE_IP` and `DRCn_KNEE_OP`.

Parameter Y0, the output level for a 0 dB input, is not specified directly but can be calculated from the other parameters using [Eq. 4-1](#).

$$Y0 = \text{DRCn\_KNEE\_OP} - (\text{DRCn\_KNEE\_IP} \times \text{DRCn\_HI\_COMP})$$

**Equation 4-1. DRC Compression Calculation**

#### 4.3.5.2 Gain Limits

The minimum and maximum gain applied by the DRC is set by `DRCn_MINGAIN`, `DRCn_MAXGAIN`, and `DRCn_NG_MINGAIN`. These limits can be used to alter the DRC response from that shown in [Fig. 4-18](#). If the range between maximum and minimum gain is reduced, the extent of the dynamic range control is reduced.

The minimum gain in the compression regions of the DRC response is set by `DRCn_MINGAIN`. The minimum gain in the noise-gate region is set by `DRCn_NG_MINGAIN`. The minimum gain limit prevents excessive attenuation of the signal path.

The maximum gain limit set by `DRCn_MAXGAIN` prevents quiet signals (or silence) from being excessively amplified.

#### 4.3.5.3 Dynamic Characteristics

The dynamic behavior determines how quickly the DRC responds to changing signal levels. Note that the DRC responds to the average (RMS) signal amplitude over a period of time.

The `DRCn_ATK` determines how quickly the DRC gain decreases when the signal amplitude is high. The `DRCn_DCY` determines how quickly the DRC gain increases when the signal amplitude is low.

These fields are described in [Table 4-13](#). The register defaults are suitable for general-purpose microphone use.

#### 4.3.5.4 Anticlip Control

The DRC includes an anticlip feature to avoid signal clipping when the input amplitude rises very quickly. This feature uses a feed-forward technique for early detection of a rising signal level. Signal clipping is avoided by dynamically increasing the gain attack rate when required. The anticlip feature is enabled using the `DRCn_ANTICLIP` bit.

Note that the feed-forward processing increases the latency in the input signal path.

Note that the anticlip feature operates entirely in the digital domain. It cannot be used to prevent signal clipping in the analog domain nor in the source signal. Analog clipping can only be prevented by reducing the analog signal gain or by adjusting the source signal.

#### 4.3.5.5 Quick Release Control

The DRC includes a quick-release feature to handle short transient peaks that are not related to the intended source signal. For example, in handheld microphone recording, transient signal peaks sometimes occur due to user handling, key presses or accidental tapping against the microphone. The quick-release feature ensures that these transients do not cause the intended signal to be masked by the longer time constant of `DRCn_DCY`.

The quick-release feature is enabled by setting the `DRCn_QR` bit. When this bit is enabled, the DRC measures the crest factor (peak to RMS ratio) of the input signal. A high crest factor is indicative of a transient peak that may not be related to the intended source signal. If the crest factor exceeds the level set by `DRCn_QR_THR`, the normal decay rate (`DRCn_DCY`) is ignored and a faster decay rate (`DRCn_QR_DCY`) is used instead.

#### 4.3.5.6 Signal Activity Detect

The DRC incorporates a configurable signal-detect function, allowing the signal level at the DRC input to be monitored and to be used to trigger other events. This can be used to detect the presence of a microphone signal on an ADC or DMIC channel, or can be used to detect an audio signal received over the digital audio interface.

Note that signal detection is supported on DRC1 and DRC2, but the triggering of the control-write sequencer is available on DRC1 only.

The DRC1 control registers are described in [Table 4-13](#).

### Table 4-13. DRC1 Control Registers

| Register Address             | Bit   | Label                 | Default | Description                                                                                                                                                                                                                                                                                                                                           |
|------------------------------|-------|-----------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R3585 (0x0E01)<br>FX_Ctrl2   | 15:4  | FX_STS[11:0]          | 0x00    | LHPF, DRC, EQ enable status. Indicates the status of each of the respective signal-processing functions. Each bit is coded as follows:<br>0 = Disabled<br>1 = Enabled<br>[11] = EQ4 [7] = DRC2 (Right) [3] = LHPF4<br>[10] = EQ3 [6] = DRC2 (Left) [2] = LHPF3<br>[9] = EQ2 [5] = DRC1 (Right) [1] = LHPF2<br>[8] = EQ1 [4] = DRC1 (Left) [0] = LHPF1 |
| R3712 (0x0E80)<br>DRC1_ctrl1 | 15:11 | DRC1_SIG_DET_RMS[4:0] | 0x00    | DRC1 Signal-Detect RMS Threshold. RMS signal level for signal-detect to be indicated when DRC1_SIG_DET_MODE = 1.<br>0x00 = -30 dB .... (1.5-dB steps) 0x1F = -76.5 dB<br>0x01 = -31.5 dB 0x1E = -75 dB                                                                                                                                                |
|                              | 10:9  | DRC1_SIG_DET_PK[1:0]  | 00      | DRC1 Signal-Detect Peak Threshold. This is the Peak/RMS ratio, or Crest Factor, level for signal-detect to be indicated when DRC1_SIG_DET_MODE = 0.<br>00 = 12 dB 10 = 24 dB<br>01 = 18 dB 11 = 30 dB                                                                                                                                                 |
|                              | 8     | DRC1_NG_ENA           | 0       | DRC1 Noise-Gate Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                 |
|                              | 7     | DRC1_SIG_DET_MODE     | 0       | DRC1 Signal-Detect Mode<br>0 = Peak threshold mode<br>1 = RMS threshold mode                                                                                                                                                                                                                                                                          |
|                              | 6     | DRC1_SIG_DET          | 0       | DRC1 Signal-Detect Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                              |
|                              | 5     | DRC1_KNEE2_OP_ENA     | 0       | DRC1 KNEE2_OP Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                   |
|                              | 4     | DRC1_QR               | 1       | DRC1 Quick-release Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                              |
|                              | 3     | DRC1_ANTICLIP         | 1       | DRC1 Anticlip Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                   |
|                              | 2     | DRC1_WSEQ_SIG_DET_ENA | 0       | DRC1 Signal-Detect Write Sequencer Select<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                              |

**Table 4-13. DRC1 Control Registers (Cont.)**

| Register Address             | Bit   | Label                | Default | Description                                                                                                                                                                                                                                                                                                                                 |
|------------------------------|-------|----------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R3713 (0x0E81)<br>DRC1_ctrl2 | 12:9  | DRC1_ATK[3:0]        | 0100    | DRC1 Gain attack rate (seconds/6 dB)<br>0000 = Reserved      0101 = 2.9 ms      1010 = 92.8 ms<br>0001 = 181 $\mu$ s      0110 = 5.8 ms      1011 = 185.6 ms<br>0010 = 363 $\mu$ s      0111 = 11.6 ms      1100 to 1111 = Reserved<br>0011 = 726 $\mu$ s      1000 = 23.2 ms<br>0100 = 1.45 ms      1001 = 46.4 ms                         |
|                              | 8:5   | DRC1_DCY[3:0]        | 1001    | DRC1 Gain decay rate (seconds/6 dB)<br>0000 = 1.45 ms      0101 = 46.5 ms      1010 = 1.49 s<br>0001 = 2.9 ms      0110 = 93 ms      1011 = 2.97 s<br>0010 = 5.8 ms      0111 = 186 ms      1100 to 1111 = Reserved<br>0011 = 11.6 ms      1000 = 372 ms<br>0100 = 23.25 ms      1001 = 743 ms                                              |
|                              | 4:2   | DRC1_MINGAIN[2:0]    | 100     | DRC1 Minimum gain to attenuate audio signals<br>000 = 0 dB      011 = -24 dB      11X = Reserved<br>001 = -12 dB      100 = -36 dB<br>010 = -18 dB      101 = Reserved                                                                                                                                                                      |
|                              | 1:0   | DRC1_MAXGAIN[1:0]    | 11      | DRC1 Maximum gain to boost audio signals (dB)<br>00 = 12 dB      10 = 24 dB<br>01 = 18 dB      11 = 36 dB                                                                                                                                                                                                                                   |
| R3714 (0x0E82)<br>DRC1_ctrl3 | 15:12 | DRC1_NG_MINGAIN[3:0] | 0000    | DRC1 Minimum gain to attenuate audio signals when the Noise Gate is active.<br>0000 = -36 dB      0101 = -6 dB      1010 = 24 dB<br>0001 = -30 dB      0110 = 0 dB      1011 = 30 dB<br>0010 = -24 dB      0111 = 6 dB      1100 = 36 dB<br>0011 = -18 dB      1000 = 12 dB      1101 to 1111 = Reserved<br>0100 = -12 dB      1001 = 18 dB |
|                              | 11:10 | DRC1_NG_EXP[1:0]     | 00      | DRC1 Noise-Gate slope<br>00 = 1 (no expansion)      10 = 4<br>01 = 2      11 = 8                                                                                                                                                                                                                                                            |
|                              | 9:8   | DRC1_QR_THR[1:0]     | 00      | DRC1 Quick-release threshold (crest factor in dB)<br>00 = 12 dB      10 = 24 dB<br>01 = 18 dB      11 = 30 dB                                                                                                                                                                                                                               |
|                              | 7:6   | DRC1_QR_DCY[1:0]     | 00      | DRC1 Quick-release decay rate (seconds/6 dB)<br>00 = 0.725 ms      10 = 5.8 ms<br>01 = 1.45 ms      11 = Reserved                                                                                                                                                                                                                           |
|                              | 5:3   | DRC1_HI_COMP[2:0]    | 011     | DRC1 Compressor slope (upper region)<br>000 = 1 (no compression)      011 = 1/8      110 = Reserved<br>001 = 1/2      100 = 1/16      111 = Reserved<br>010 = 1/4      101 = 0                                                                                                                                                              |
|                              | 2:0   | DRC1_LO_COMP[2:0]    | 000     | DRC1 Compressor slope (lower region)<br>000 = 1 (no compression)      011 = 1/8      11X = Reserved<br>001 = 1/2      100 = 0<br>010 = 1/4      101 = Reserved                                                                                                                                                                              |
| R3715 (0x0E83)<br>DRC1_ctrl4 | 10:5  | DRC1_KNEE_IP[5:0]    | 0x00    | DRC1 Input signal level at the compressor knee.<br>0x00 = 0 dB      0x02 = -1.5 dB      0x3C = -45 dB<br>0x01 = -0.75 dB      ... (-0.75-dB steps)      0x3D--0x3F = Reserved                                                                                                                                                               |
|                              | 4:0   | DRC1_KNEE_OP[4:0]    | 0x00    | DRC1 Output signal at the compressor knee.<br>0x00 = 0 dB      0x02 = -1.5 dB      0x1E = -22.5 dB<br>0x01 = -0.75 dB      ... (-0.75 dB steps)      0x1F = Reserved                                                                                                                                                                        |
| R3716 (0x0E84)<br>DRC1_ctrl5 | 9:5   | DRC1_KNEE2_IP[4:0]   | 0x00    | DRC1 Input signal level at the noise-gate threshold Knee 2.<br>0x00 = -36 dB      0x02 = -39 dB      0x1E = -81 dB<br>0x01 = -37.5 dB      ... (-1.5-dB steps)      0x1F = -82.5 dB<br>Applicable if DRC1_NG_ENA = 1.                                                                                                                       |
|                              | 4:0   | DRC1_KNEE2_OP[4:0]   | 0x00    | DRC1 Output signal at the noise-gate threshold Knee 2.<br>0x00 = -30 dB      0x02 = -33 dB      0x1E = -75 dB<br>0x01 = -31.5 dB      ... (-1.5dB steps)      0x1F = -76.5 dB<br>Applicable only if DRC1_KNEE2_OP_ENA = 1.                                                                                                                  |

The DRC2 control registers are described in [Table 4-14](#).

**Table 4-14. DRC2 Control Registers**

| Register Address             | Bit   | Label                 | Default | Description                                                                                                                                                                                                                                                                                                                                           |
|------------------------------|-------|-----------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R3585 (0x0E01)<br>FX_Ctrl2   | 15:4  | FX_STS[11:0]          | 0x00    | LHPF, DRC, EQ Enable Status. Indicates the status of each of the respective signal-processing functions. Each bit is coded as follows:<br>0 = Disabled<br>1 = Enabled<br>[11] = EQ4 [7] = DRC2 (Right) [3] = LHPF4<br>[10] = EQ3 [6] = DRC2 (Left) [2] = LHPF3<br>[9] = EQ2 [5] = DRC1 (Right) [1] = LHPF2<br>[8] = EQ1 [4] = DRC1 (Left) [0] = LHPF1 |
| R3720 (0x0E88)<br>DRC2_ctrl1 | 15:11 | DRC2_SIG_DET_RMS[4:0] | 0x00    | DRC2 Signal-Detect RMS Threshold. This is the RMS signal level for signal-detect to be indicated when DRC2_SIG_DET_MODE = 1.<br>0x00 = -30 dB .... (1.5-dB steps) 0x1F = -76.5 dB<br>0x01 = -31.5 dB 0x1E = -75 dB                                                                                                                                    |
|                              | 10:9  | DRC2_SIG_DET_PK[1:0]  | 00      | DRC2 Signal-Detect Peak Threshold. Peak/RMS ratio, or Crest Factor, level for signal-detect to be indicated when DRC2_SIG_DET_MODE = 0.<br>00 = 12 dB 10 = 24 dB<br>01 = 18 dB 11 = 30 dB                                                                                                                                                             |
|                              | 8     | DRC2_NG_ENA           | 0       | DRC2 Noise-Gate Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                 |
|                              | 7     | DRC2_SIG_DET_MODE     | 0       | DRC2 Signal-Detect Mode<br>0 = Peak threshold mode<br>1 = RMS threshold mode                                                                                                                                                                                                                                                                          |
|                              | 6     | DRC2_SIG_DET          | 0       | DRC2 Signal-Detect Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                              |
|                              | 5     | DRC2_KNEE2_OP_ENA     | 0       | DRC2 KNEE2_OP Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                   |
|                              | 4     | DRC2_QR               | 1       | DRC2 Quick-release Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                              |
|                              | 3     | DRC2_ANTICLIP         | 1       | DRC2 Anticlip Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                   |
| R3721 (0x0E89)<br>DRC2_ctrl2 | 12:9  | DRC2_ATK[3:0]         | 0100    | DRC2 Gain attack rate (seconds/6 dB)<br>0000 = Reserved 0101 = 2.9 ms 1010 = 92.8 ms<br>0001 = 181 $\mu$ s 0110 = 5.8 ms 1011 = 185.6 ms<br>0010 = 363 $\mu$ s 0111 = 11.6 ms 1100 to 1111 = Reserved<br>0011 = 726 $\mu$ s 1000 = 23.2 ms<br>0100 = 1.45 ms 1001 = 46.4 ms                                                                           |
|                              | 8:5   | DRC2_DCY[3:0]         | 1001    | DRC2 Gain decay rate (seconds/6 dB)<br>0000 = 1.45 ms 0101 = 46.5 ms 1010 = 1.49 s<br>0001 = 2.9 ms 0110 = 93 ms 1011 = 2.97 s<br>0010 = 5.8 ms 0111 = 186 ms 1100 to 1111 = Reserved<br>0011 = 11.6 ms 1000 = 372 ms<br>0100 = 23.25 ms 1001 = 743 ms                                                                                                |
|                              | 4:2   | DRC2_MINGAIN[2:0]     | 100     | DRC2 Minimum gain to attenuate audio signals<br>000 = 0 dB 011 = -24 dB 11X = Reserved<br>001 = -12 dB (default) 100 = -36 dB<br>010 = -18 dB 101 = Reserved                                                                                                                                                                                          |
|                              | 1:0   | DRC2_MAXGAIN[1:0]     | 11      | DRC2 Maximum gain to boost audio signals (dB)<br>00 = 12 dB 10 = 24 dB<br>01 = 18 dB 11 = 36 dB                                                                                                                                                                                                                                                       |

**Table 4-14. DRC2 Control Registers (Cont.)**

| Register Address             | Bit   | Label                | Default | Description                                                                                                                                                                                                                                                                                                                                 |
|------------------------------|-------|----------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R3722 (0x0E8A)<br>DRC2_ctrl3 | 15:12 | DRC2_NG_MINGAIN[3:0] | 0000    | DRC2 Minimum gain to attenuate audio signals when the Noise Gate is active.<br>0000 = –36 dB      0101 = –6 dB      1010 = 24 dB<br>0001 = –30 dB      0110 = 0 dB      1011 = 30 dB<br>0010 = –24 dB      0111 = 6 dB      1100 = 36 dB<br>0011 = –18 dB      1000 = 12 dB      1101 to 1111 = Reserved<br>0100 = –12 dB      1001 = 18 dB |
|                              | 11:10 | DRC2_NG_EXP[1:0]     | 00      | DRC2 Noise-Gate slope<br>00 = 1 (no expansion)<br>01 = 2<br>10 = 4<br>11 = 8                                                                                                                                                                                                                                                                |
|                              | 9:8   | DRC2_QR_THR[1:0]     | 00      | DRC2 Quick-release threshold (crest factor in dB)<br>00 = 12 dB<br>01 = 18 dB<br>10 = 24 dB<br>11 = 30 dB                                                                                                                                                                                                                                   |
|                              | 7:6   | DRC2_QR_DCY[1:0]     | 00      | DRC2 Quick-release decay rate (seconds/6 dB)<br>00 = 0.725 ms<br>01 = 1.45 ms<br>10 = 5.8 ms<br>11 = Reserved                                                                                                                                                                                                                               |
|                              | 5:3   | DRC2_HI_COMP[2:0]    | 011     | DRC2 Compressor slope (upper region)<br>000 = 1 (no compression)      011 = 1/8      110–111 = Reserved<br>001 = 1/2      100 = 1/16<br>010 = 1/4      101 = 0                                                                                                                                                                              |
|                              | 2:0   | DRC2_LO_COMP[2:0]    | 000     | DRC2 Compressor slope (lower region)<br>000 = 1 (no compression)      010 = 1/4      100 = 0<br>001 = 1/2      011 = 1/8      101–11X = Reserved                                                                                                                                                                                            |
| R3723 (0x0E8B)<br>DRC2_ctrl4 | 10:5  | DRC2_KNEE_IP[5:0]    | 0x00    | DRC2 Input signal level at the compressor knee.<br>0x00 = 0 dB      0x02 = –1.5 dB      0x3C = –45 dB<br>0x01 = –0.75 dB      ... (–0.75-dB steps)      0x3D–0x3F = Reserved                                                                                                                                                                |
|                              | 4:0   | DRC2_KNEE_OP[4:0]    | 0x00    | DRC2 Output signal at the compressor knee.<br>0x00 = 0 dB      0x02 = –1.5 dB      0x1E = –22.5 dB<br>0x01 = –0.75 dB      ... (–0.75 dB steps)      0x1F = Reserved                                                                                                                                                                        |
| R3724 (0x0E8C)<br>DRC2_ctrl5 | 9:5   | DRC2_KNEE2_IP[4:0]   | 0x00    | DRC2 Input signal level at the noise-gate threshold Knee 2.<br>0x00 = –36 dB      0x02 = –39 dB      0x1E = –81 dB<br>0x01 = –37.5 dB      ... (–1.5-dB steps)      0x1F = –82.5 dB<br>Applicable only if DRC2_NG_ENA = 1.                                                                                                                  |
|                              | 4:0   | DRC2_KNEE2_OP[4:0]   | 0x00    | DRC2 Output signal at the noise-gate threshold Knee 2.<br>0x00 = –30 dB      0x02 = –33 dB      0x1E = –75 dB<br>0x01 = –31.5 dB      ... (–1.5dB steps)      0x1F = –76.5 dB<br>Applicable only if DRC2_KNEE2_OP_ENA = 1.                                                                                                                  |

The CS47L35 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded DRC and digital mixing functions. If the frequency is too low, an attempt to enable a DRC signal path fails. Note that active signal paths are not affected under such circumstances.

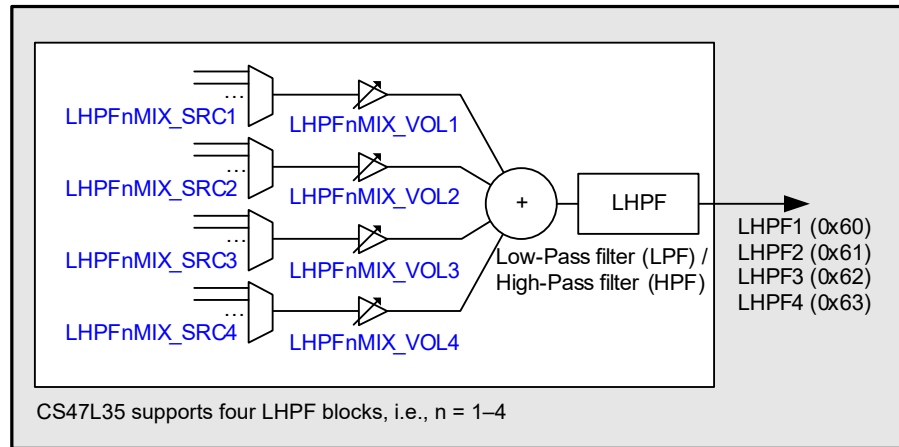
The FX\_STS field in register R3585 indicates the status of each of the EQ, DRC, and LHPF signal paths. If an underclocked error condition occurs, this field indicates which EQ, DRC, or LHPF signal paths have been enabled.

The status bits in registers R1600–R2936 indicate the status of each of the digital mixers. If an underclocked error condition occurs, these bits indicate which mixers have been enabled.

### 4.3.6 Low-/High-Pass Digital Filter (LHPF)

The digital core provides four LHPF processing blocks as shown in Fig. 4-19. A four-input mixer is associated with each filter. The four input sources are selectable in each case, and independent volume control is provided for each path. Each LHPF block supports one output.

The LHPF /HPF can be used to remove unwanted out-of-band noise from a signal path. Each filter can be configured either as a low-pass filter (LPF) or a high-pass filter (HPF).



**Figure 4-19. Digital-Core LPF/HPF Blocks**

The LHPF1–LHPF4 mixer control fields, shown in Fig. 4-19, are located at register addresses R2304–R2335 (0x0900–0x091F).

The full list of digital mixer control registers (R1600–R2936) is provided in Section 6. Generic register field definitions are provided in Table 4-7.

The x\_SRCn fields select the input sources for the respective LHPF processing blocks. Note that the selected input sources must be configured for the same sample rate as the LHPF to which they are connected. Sample-rate conversion functions are available to support flexible interconnectivity; see Section 4.3.14.

The hexadecimal numbers in Fig. 4-19 indicate the corresponding x\_SRCn setting for selection of that signal as an input to another digital-core function.

The LHPF blocks should be kept disabled (LHPFn\_ENA = 0) if SYSCLK is not enabled. The x\_SRCn fields for all digital core functions should be held at 0x00 if SYSCLK is not enabled. SYSCLK must be present and enabled before selecting other values for these fields. See Section 4.16.4 for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The sample rate for the LHPF function is configured using FX\_RATE; see Table 4-21. Note that the EQ, DRC, and LHPF functions must all be configured for the same sample rate. Sample-rate conversion is required when routing the LHPF signal paths to any signal chain that is configured for a different sample rate.

The FX\_RATE field must not be changed if any of the associated x\_SRCn fields is nonzero. The associated x\_SRCn fields must be cleared before writing a new value to FX\_RATE. A minimum delay of 125 μs must be allowed between clearing the x\_SRCn fields and writing to FX\_RATE. See Table 4-21 for details.

The control registers associated with the LHPF functions are described in Table 4-15.

The cut-off frequencies for the LHPF blocks are set using the coefficients held in registers R3777, R3781, R3785, and R3789 for LHPF1, LHPF2, LHPF3 and LHPF4 respectively. These coefficients are derived using tools provided in Cirrus Logic's WISCE evaluation board control software; please contact your Cirrus Logic representative for details.

**Table 4-15. Low-Pass Filter/High-Pass Filter**

| Register Address           | Bit  | Label             | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|----------------------------|------|-------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R3585 (0x0E01)<br>FX_Ctrl2 | 15:4 | FX_STS[11:0]      | 0x00    | LHPF, DRC, EQ Enable Status. Indicates the status of the respective signal-processing functions. Each bit is coded as follows:<br>0 = Disabled<br>1 = Enabled<br>[11] = EQ4                      [7] = DRC2 (Right)                      [3] = LHPF4<br>[10] = EQ3                      [6] = DRC2 (Left)                      [2] = LHPF3<br>[9] = EQ2                      [5] = DRC1 (Right)                      [1] = LHPF2<br>[8] = EQ1                      [4] = DRC1 (Left)                      [0] = LHPF1 |
| R3776 (0x0EC0)<br>HPLPF1_1 | 1    | LHPF1_MODE        | 0       | Low-/High-Pass Filter 1 Mode<br>0 = Low Pass<br>1 = High Pass                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                            | 0    | LHPF1_ENA         | 0       | Low-/High-Pass Filter 1 Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| R3777 (0x0EC1)<br>HPLPF1_2 | 15:0 | LHPF1_COEFF[15:0] | 0x0000  | Low-/High-Pass Filter 1 Frequency Coefficient<br>Refer to WISCE evaluation board control software for the derivation of this field value.                                                                                                                                                                                                                                                                                                                                                                             |
| R3780 (0x0EC4)<br>HPLPF2_1 | 1    | LHPF2_MODE        | 0       | Low-/High-Pass Filter 2 Mode<br>0 = Low Pass<br>1 = High Pass                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                            | 0    | LHPF2_ENA         | 0       | Low-/High-Pass Filter 2 Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| R3781 (0x0EC5)<br>HPLPF2_2 | 15:0 | LHPF2_COEFF[15:0] | 0x0000  | Low-/High-Pass Filter 2 Frequency Coefficient<br>Refer to WISCE evaluation board control software for the derivation of this field value.                                                                                                                                                                                                                                                                                                                                                                             |
| R3784 (0x0EC8)<br>HPLPF3_1 | 1    | LHPF3_MODE        | 0       | Low-/High-Pass Filter 3 Mode<br>0 = Low Pass<br>1 = High Pass                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                            | 0    | LHPF3_ENA         | 0       | Low-/High-Pass Filter 3 Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| R3785 (0x0EC9)<br>HPLPF3_2 | 15:0 | LHPF3_COEFF[15:0] | 0x0000  | Low-/High-Pass Filter 3 Frequency Coefficient<br>Refer to WISCE evaluation board control software for the derivation of this field value.                                                                                                                                                                                                                                                                                                                                                                             |
| R3788 (0x0ECC)<br>HPLPF4_1 | 1    | LHPF4_MODE        | 0       | Low-/High-Pass Filter 4 Mode<br>0 = Low Pass<br>1 = High Pass                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                            | 0    | LHPF4_ENA         | 0       | Low-/High-Pass Filter 4 Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| R3789 (0x0ECD)<br>HPLPF4_2 | 15:0 | LHPF4_COEFF[15:0] | 0x0000  | Low-/High-Pass Filter 4 Frequency Coefficient<br>Refer to WISCE evaluation board control software for the derivation of this field value.                                                                                                                                                                                                                                                                                                                                                                             |

The CS47L35 performs automatic checks to confirm whether the SYSCLK frequency is high enough to support the commanded LHPF and digital mixing functions. If the frequency is too low, an attempt to enable an LHPF signal path fails. Note that active signal paths are not affected under such circumstances.

The FX\_STS field in register R3585 indicates the status of each of the EQ, DRC, and LHPF signal paths. If an underclocked error condition occurs, this field indicates which EQ, DRC, or LHPF signal paths have been enabled.

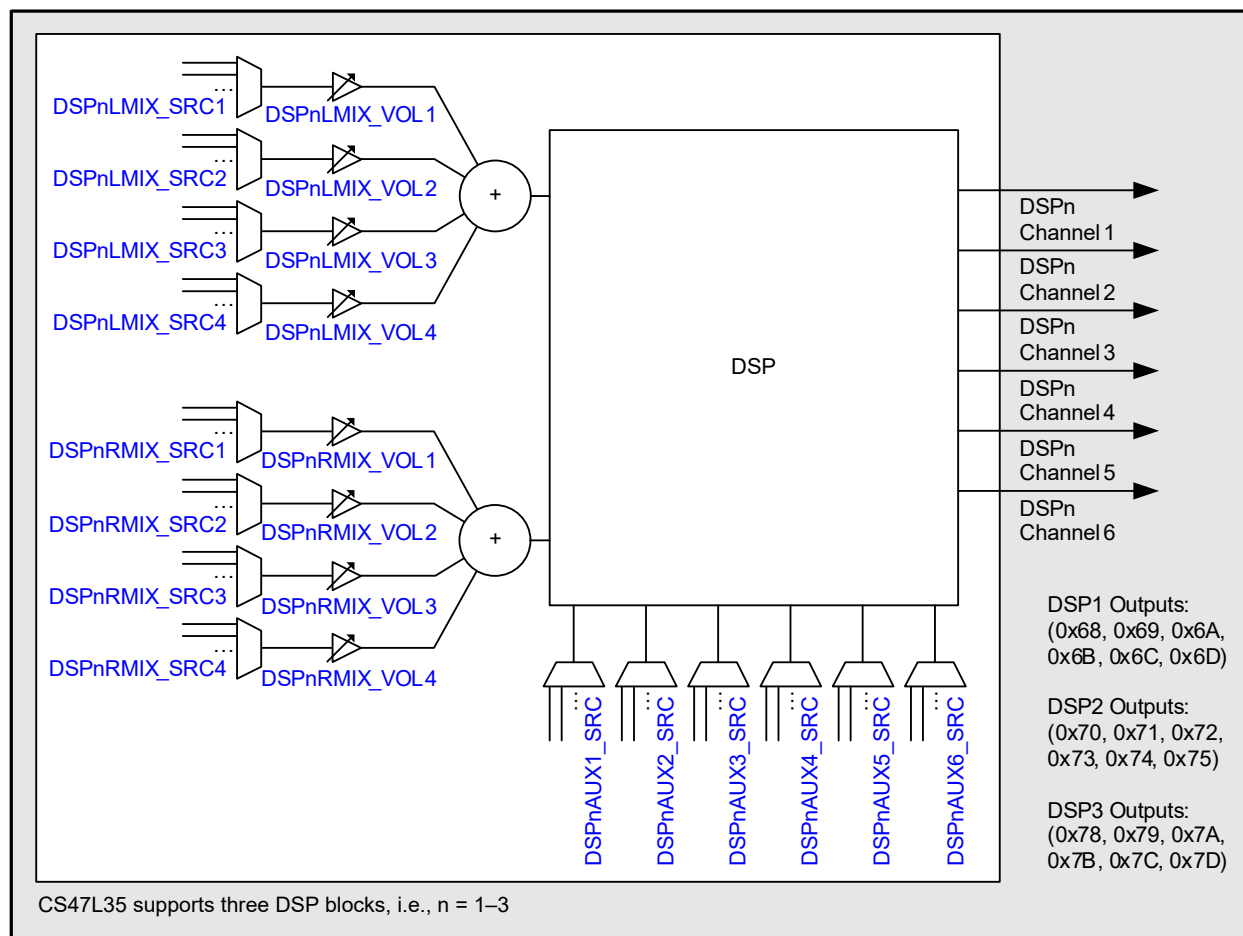
The status bits in registers R1600–R2936 indicate the status of each of the digital mixers. If an underclocked error condition occurs, these bits indicate which mixers have been enabled.

### 4.3.7 Digital-Core DSP

The digital core provides three programmable DSP processing blocks as shown in Fig. 4-20. Each block supports eight inputs (Left, Right, Aux1, Aux2, ... Aux6). A four-input mixer is associated with the left and right inputs, providing further expansion of the number of input paths. Each of the input sources is selectable, and independent volume control is provided for left and right input mixer channels. Each DSP block supports six outputs.

The functionality of the DSP processing blocks is not fixed, and a wide range of audio enhancements algorithms may be performed. The procedure for configuring the CS47L35 DSP functions is tailored to each customer's application; please contact your Cirrus Logic representative for details.

For details of the DSP firmware requirements relating to clocking, register access, and code execution, refer to Section 4.4.2.



**Figure 4-20. Digital-Core DSP Blocks**

The DSPn mixer input control fields (see Fig. 4-20) are located at register addresses R2368–R2511 (0x0940–0x09CF).

The full list of digital mixer control registers (R1600–R2936) is provided in Section 6. Generic register field definitions are provided in Table 4-7.

The x\_SRCn fields select the input sources for the respective DSP processing blocks. Note that the selected input sources must be configured for the same sample rate as the DSP to which they are connected. Sample-rate conversion functions are available to support flexible interconnectivity; see Section 4.3.14.

The hexadecimal numbers in Fig. 4-20 indicate the corresponding x\_SRCn setting for selection of that signal as an input to another digital-core function.

The `x_SRCn` fields for all digital core functions should be held at 0x00 if SYSCCLK is not enabled—SYSCCLK must be present and enabled before selecting other values for these fields. See [Section 4.16.4](#) for further details (including requirements for reconfiguring SYSCCLK while digital core mixers are enabled).

The sample rate for each of the DSP functions is configured using the respective `DSPn_RATE` field; see [Table 4-21](#). Sample-rate conversion is required when routing the `DSPn` signal paths to any signal chain that is configured for a different sample rate.

The `DSPn_RATE` fields must not be changed if any of the respective `x_SRCn` fields is nonzero. The associated `x_SRCn` fields must be cleared before writing new values to `DSPn_RATE`. A minimum delay of 125  $\mu$ s must be allowed between clearing the `x_SRCn` fields and writing to the associated `DSPn_RATE` fields. See [Table 4-21](#) for details.

The CS47L35 performs automatic checks to confirm that the SYSCCLK frequency is high enough to support the required DSP mixing functions. If the frequency is too low, an attempt to enable a DSP mixer path fails. Note that active signal paths are not affected under such circumstances.

The status bits in registers R1600–R2936 indicate the status of each of the digital mixers. If an underclocked error condition occurs, these bits indicate which mixers have been enabled.

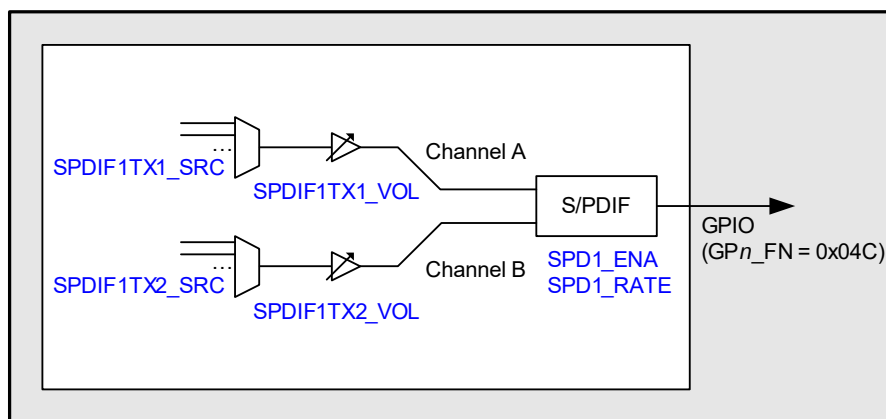
### 4.3.8 S/PDIF Output Generator

The CS47L35 incorporates an IEC-60958-3-compatible S/PDIF output generator, as shown in [Fig. 4-21](#); this provides a stereo S/PDIF output on a GPIO pin. The S/PDIF transmitter allows full control over the S/PDIF validity bits and channel status information.

The input sources to the S/PDIF transmitter are selectable for each channel, and independent volume control is provided for each path. The `*TX1` and `*TX2` fields control Channels A and B (respectively) of the S/PDIF output.

The S/PDIF signal can be output directly on a GPIO pin. See [Section 4.14](#) to configure a GPIO pin for this function.

Note that the S/PDIF signal cannot be selected as input to the digital mixers or signal-processing functions within the CS47L35 digital core.



**Figure 4-21. Digital-Core S/PDIF Output Generator**

The S/PDIF input control fields (see [Fig. 4-21](#)) are located at register addresses R2048–R2057 (0x0800–0x0809).

The full list of digital mixer control registers (R1600–R2936) is provided in [Section 6](#). Generic register field definitions are provided in [Table 4-7](#).

The `x_SRCn` fields select the input sources for the two S/PDIF channels. Note that the selected input sources must be synchronized to the SYSCCLK clocking domain, and configured for the same sample rate as the S/PDIF generator. Sample-rate conversion functions are available to support flexible interconnectivity; see [Section 4.3.14](#).

The S/PDIF output generator should be kept disabled (SPD1\_ENA = 0) if SYSCLK is not enabled. The x\_SRCn fields for all digital core functions should be held at 0x00 if SYSCLK is not enabled. SYSCLK must be present and enabled before selecting other values for these fields. See [Section 4.16.4](#) for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The sample rate of the S/PDIF generator is configured using SPD1\_RATE; see [Table 4-21](#). The S/PDIF transmitter supports sample rates in the range 32–192 kHz. Note that sample-rate conversion is required when linking the S/PDIF generator to any signal chain that is configured for a different sample rate.

The SPD1\_RATE field must not be changed if any of the associated x\_SRCn fields is nonzero. The associated x\_SRCn fields must be cleared before writing a new value to SPD1\_RATE. A minimum delay of 125  $\mu$ s must be allowed between clearing the x\_SRCn fields and writing to SPD1\_RATE. See [Table 4-21](#) for details.

The S/PDIF generator is enabled by setting SPD1\_ENA, as described in [Table 4-16](#).

The S/PDIF output contains audio data derived from the selected sources. Audio samples up to 24-bit width can be accommodated. The validity bits and the channel status bits in the S/PDIF data are configured using the corresponding fields in registers R1474 (0x5C2) to R1477 (0x5C5).

Refer to the S/PDIF specification (IEC 60958-3 Digital Audio Interface - Consumer) for full details of the S/PDIF protocol and configuration parameters.

**Table 4-16. S/PDIF Output Generator Control**

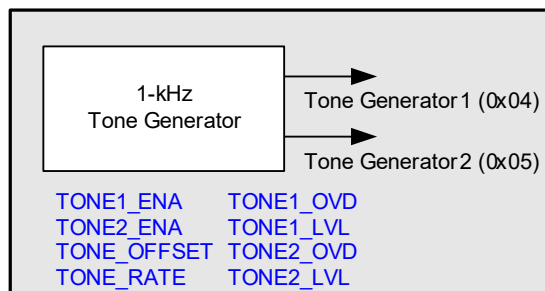
| Register Address                           | Bit   | Label              | Default | Description                                            |
|--------------------------------------------|-------|--------------------|---------|--------------------------------------------------------|
| R1474 (0x05C2)<br>SPD1_TX_Control          | 13    | SPD1_VAL2          | 0       | S/PDIF Validity (Subframe B)                           |
|                                            | 12    | SPD1_VAL1          | 0       | S/PDIF Validity (Subframe A)                           |
|                                            | 0     | SPD1_ENA           | 0       | S/PDIF Generator Enable<br>0 = Disabled<br>1 = Enabled |
| R1475 (0x05C3)<br>SPD1_TX_Channel_Status_1 | 15:8  | SPD1_CATCODE[7:0]  | 0x00    | S/PDIF Category code                                   |
|                                            | 7:6   | SPD1_CHSTMODE[1:0] | 00      | S/PDIF Channel Status mode                             |
|                                            | 5:3   | SPD1_PREAMPH[2:0]  | 000     | S/PDIF Preemphasis mode                                |
|                                            | 2     | SPD1_NOCOPY        | 0       | S/PDIF Copyright status                                |
|                                            | 1     | SPD1_NOAUDIO       | 0       | S/PDIF Audio/nonaudio indication                       |
|                                            | 0     | SPD1_PRO           | 0       | S/PDIF Consumer Mode/Professional Mode                 |
| R1476 (0x05C4)<br>SPD1_TX_Channel_Status_2 | 15:12 | SPD1_FREQ[3:0]     | 0000    | S/PDIF Indicated sample frequency                      |
|                                            | 11:8  | SPD1_CHNUM2[3:0]   | 1011    | S/PDIF Channel number (Subframe B)                     |
|                                            | 7:4   | SPD1_CHNUM1[3:0]   | 0000    | S/PDIF Channel number (Subframe A)                     |
|                                            | 3:0   | SPD1_SRCNUM[3:0]   | 0001    | S/PDIF Source number                                   |
| R1477 (0x05C5)<br>SPD1_TX_Channel_Status_3 | 11:8  | SPD1_ORGSAMP[3:0]  | 0000    | S/PDIF Original sample frequency                       |
|                                            | 7:5   | SPD1_TXWL[2:0]     | 000     | S/PDIF Audio sample word length                        |
|                                            | 4     | SPD1_MAXWL         | 0       | S/PDIF Maximum audio sample word length                |
|                                            | 3:2   | SPD1_SC31_30[1:0]  | 00      | S/PDIF Channel Status [31:30]                          |
|                                            | 1:0   | SPD1_CLKACU[1:0]   | 00      | Transmitted Clock accuracy                             |

The CS47L35 automatically checks to confirm whether the SYSCLK frequency is high enough to support the digital mixer paths. If an attempt is made to enable the S/PDIF generator, and there are insufficient SYSCLK cycles to support it, the attempt does not succeed. Note that any active signal paths are unaffected under such circumstances.

The status bits in registers R1600–R2936 indicate the status of each of the digital mixers. If an underclocked error condition occurs, these bits indicate which mixers have been enabled.

### 4.3.9 Tone Generator

The CS47L35 incorporates a tone generator that can be used for beep functions through any of the audio signal paths. The tone generator provides two 1-kHz outputs, with configurable phase relationship, offering flexibility to create differential signals or test scenarios.



**Figure 4-22. Digital-Core Tone Generator**

The tone generators can be selected as input to any of the digital mixers or signal-processing functions within the CS47L35 digital core. The hexadecimal numbers in [Fig. 4-22](#) indicate the corresponding x\_SRCn setting for selection of that signal as an input to another digital-core function.

The sample rate for the tone generators is configured using TONE\_RATE. See [Table 4-21](#). Note that sample-rate conversion is required when routing the tone generator outputs to any signal chain that is configured for a different sample rate.

The tone generators are enabled by setting the TONE1\_ENA and TONE2\_ENA bits as described in [Table 4-17](#). The phase relationship is configured using TONE\_OFFSET.

The tone generators can also provide a configurable DC signal level, for use as a test signal. The DC output is selected using the TONEn\_OVD bits, and the DC signal amplitude is configured using the TONEn\_LVL fields, as described in [Table 4-17](#).

SYSCLOCK must be present and enabled before setting the TONEn\_ENA bits. The tone generators should be kept disabled (TONEn\_ENA = 0) if SYSCLOCK is not enabled. See [Section 4.16.4](#) for further details (including requirements for reconfiguring SYSCLOCK while digital core functions are enabled).

**Table 4-17. Tone Generator Control**

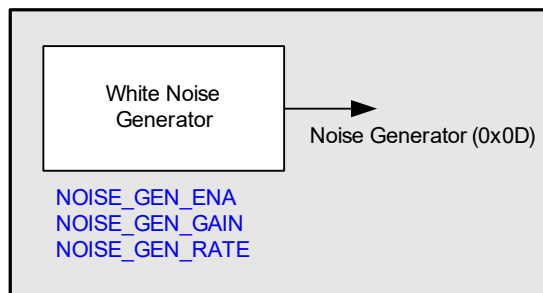
| Register Address                 | Bit  | Label            | Default | Description                                                                                                                                                                                                                                             |
|----------------------------------|------|------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R32 (0x0020)<br>Tone_Generator_1 | 9:8  | TONE_OFFSET[1:0] | 00      | Tone Generator Phase Offset. Sets the phase of Tone Generator 2 relative to Tone Generator 1<br>00 = 0 degrees (in phase)<br>01 = 90 degrees ahead<br>10 = 180 degrees ahead<br>11 = 270 degrees ahead                                                  |
|                                  | 5    | TONE2_OVD        | 0       | Tone Generator 2 Override<br>0 = Disabled (1-kHz tone output)<br>1 = Enabled (DC signal output)<br>The DC signal level, when selected, is configured using TONE2_LVL[23:0]                                                                              |
|                                  | 4    | TONE1_OVD        | 0       | Tone Generator 1 Override<br>0 = Disabled (1-kHz tone output)<br>1 = Enabled (DC signal output)<br>The DC signal level, when selected, is configured using TONE1_LVL[23:0]                                                                              |
|                                  | 1    | TONE2_ENA        | 0       | Tone Generator 2 Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                  |
|                                  | 0    | TONE1_ENA        | 0       | Tone Generator 1 Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                  |
| R33 (0x0021)<br>Tone_Generator_2 | 15:0 | TONE1_LVL[23:8]  | 0x1000  | Tone Generator 1 DC output level<br>TONE1_LVL[23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion.<br>The digital core 0 dBFS level corresponds to 0x10_0000 (+1) or 0xF0_0000 (–1). |

**Table 4-17. Tone Generator Control (Cont.)**

| Register Address                 | Bit  | Label           | Default | Description                                                                                                                                                                                                                                             |
|----------------------------------|------|-----------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R34 (0x0022)<br>Tone_Generator_3 | 7:0  | TONE1_LVL[7:0]  | 0x00    | Tone Generator 1 DC output level<br>TONE1_LVL[23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion.<br>The digital core 0 dBFS level corresponds to 0x10_0000 (+1) or 0xF0_0000 (–1). |
| R35 (0x0023)<br>Tone_Generator_4 | 15:0 | TONE2_LVL[23:8] | 0x1000  | Tone Generator 2 DC output level<br>TONE2_LVL[23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion.<br>The digital core 0 dBFS level corresponds to 0x10_0000 (+1) or 0xF0_0000 (–1). |
| R36 (0x0024)<br>Tone_Generator_5 | 7:0  | TONE2_LVL[7:0]  | 0x00    | Tone Generator 2 DC output level<br>TONE2_LVL[23:8] is coded as 2's complement. Bits [23:20] contain the integer portion; bits [19:0] contain the fractional portion.<br>The digital core 0 dBFS level corresponds to 0x10_0000 (+1) or 0xF0_0000 (–1). |

### 4.3.10 Noise Generator

The CS47L35 incorporates a white-noise generator that can be routed within the digital core. The main purpose of the noise generator is to provide comfort noise in cases where silence (digital mute) is not desirable.


**Figure 4-23. Digital-Core Noise Generator**

The noise generator can be selected as input to any of the digital mixers or signal-processing functions within the CS47L35 digital core. The hexadecimal number (0x0D) in [Fig. 4-23](#) indicates the corresponding x\_SRCn setting for selection of the noise generator as an input to another digital-core function.

The sample rate for the noise generator is configured using the NOISE\_GEN\_RATE field. See [Table 4-21](#). Note that sample-rate conversion is required when routing the noise generator output to any signal chain that is configured for a different sample rate.

The noise generator is enabled by setting NOISE\_GEN\_ENA, described in [Table 4-18](#). The signal level is configured using NOISE\_GEN\_GAIN.

SYSCLK must be present and enabled before setting NOISE\_GEN\_ENA. The noise generator should be kept disabled (NOISE\_GEN\_ENA = 0) if SYSCLK is not enabled. See [Section 4.16.4](#) for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

**Table 4-18. Noise Generator Control**

| Register Address                         | Bit | Label               | Default | Description                                                                                                                                                         |
|------------------------------------------|-----|---------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R160 (0x00A0)<br>Comfort_Noise_Generator | 5   | NOISE_GEN_ENA       | 0       | Noise Generator Enable<br>0 = Disabled<br>1 = Enabled                                                                                                               |
|                                          | 4:0 | NOISE_GEN_GAIN[4:0] | 0x00    | Noise generator signal level<br>0x00 = –114 dBFS ... (6-dB steps) All other codes are reserved<br>0x01 = –108 dBFS 0x11 = –6 dBFS<br>0x02 = –102 dBFS 0x12 = 0 dBFS |

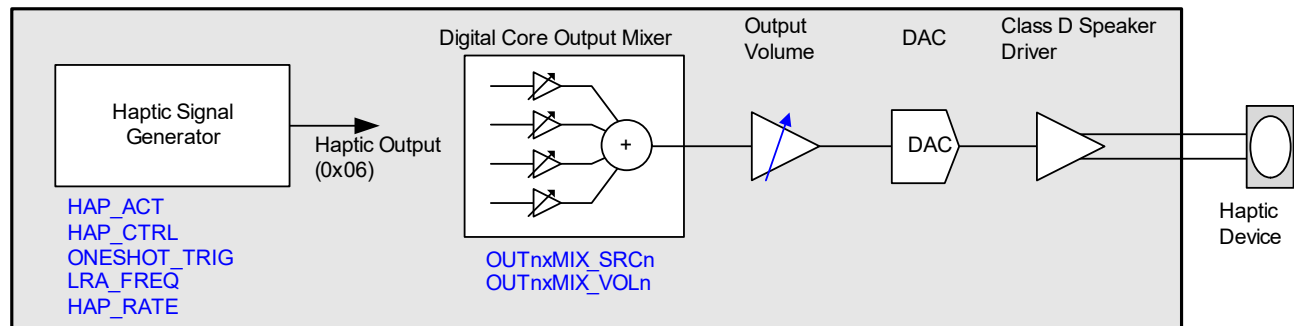
### 4.3.11 Haptic Signal Generator

The CS47L35 incorporates a signal generator for use with haptic devices (e.g., mechanical vibration actuators). The haptic signal generator is compatible with both eccentric rotating mass (ERM) and linear resonant actuator (LRA) haptic devices.

The haptic signal generator is highly configurable, and includes the capability to execute a programmable event profile comprising three distinct operating phases.

The resonant frequency of the haptic signal output (for LRA devices) is selectable, providing support for many different actuator components.

The haptic signal generator is a digital signal generator, which is incorporated within the digital core of the CS47L35. The haptic signal may be routed via the digital-core output mixers to the Class D speaker output for connection to the external haptic device, as shown in Fig. 4-24. Note that the digital PDM output paths may also be used for haptic signal output.



**Figure 4-24. Digital-Core Haptic Signal Generator**

The hexadecimal number (0x06) in Fig. 4-24 indicates the corresponding `x_SRCn` setting for selection of the haptic signal generator as an input to another digital-core function.

The haptic signal generator is selected as input to one of the digital-core output mixers by setting the `x_SRCn` field of the applicable output mixer to 0x06.

SYSCLK must be present and enabled before setting `HAP_CTRL > 00`. The haptic signal generator should be kept disabled (`HAP_CTRL = 00`) if SYSCLK is not enabled. See Section 4.16.4 for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The sample rate for the haptic signal generator is configured using the `HAP_RATE` field. See Table 4-19. Note that sample-rate conversion is required when routing the haptic signal generator output to any signal chain that is configured for a different sample rate.

The haptic signal generator is configured for an ERM or LRA actuator using the `HAP_ACT` bit. The required resonant frequency is configured using the `LRA_FREQ` field. Note that the resonant frequency is only applicable to LRA actuators.

The signal generator can be enabled in continuous mode or configured for one-shot mode using the `HAP_CTRL` field, as described in Table 4-19. In one-shot mode, the output is triggered by writing to the `ONESHOT_TRIG` bit.

In one-shot mode, the signal generator profile comprises the distinct phases (1, 2, 3). The duration and intensity of each output phase is programmable.

In continuous mode, the signal intensity is controlled using the `PHASE2_INTENSITY` field only.

In the case of an ERM actuator (`HAP_ACT = 0`), the haptic output is a DC signal level, which may be positive or negative, as selected by the `x_INTENSITY` fields.

For an LRA actuator (`HAP_ACT = 1`), the haptic output is an AC signal; selecting a negative signal level corresponds to a 180° phase inversion. In some applications, phase inversion may be desirable during the final phase, to halt the physical motion of the haptic device.

**Table 4-19. Haptic Signal Generator Control**

| Register Address                                  | Bit  | Label                 | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|---------------------------------------------------|------|-----------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R144 (0x0090)<br>Haptics_Control_1                | 4    | ONESHOT_TRIG          | 0       | Haptic One-Shot Trigger. Writing 1 starts the one-shot profile (i.e., Phase 1, Phase 2, Phase 3)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|                                                   | 3:2  | HAP_CTRL[1:0]         | 00      | Haptic Signal Generator Control<br>00 = Disabled                      10 = One-Shot<br>01 = Continuous                  11 = Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|                                                   | 1    | HAP_ACT               | 0       | Haptic Actuator Select<br>0 = Eccentric rotating mass (ERM)<br>1 = Linear resonant actuator (LRA)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| R145 (0x0091)<br>Haptics_Control_2                | 14:0 | LRA_FREQ[14:0]        | 0x7FFF  | Haptic Resonant Frequency. Selects the haptic signal frequency (LRA actuator only, HAP_ACT = 1)<br>Haptic Frequency (Hz) = System Clock/(2 x (LRA_FREQ+1)), where System Clock = 6.144 MHz or 5.6448 MHz, derived by division from SYSCLK.<br>Valid for haptic frequency in the range 100–250 Hz<br>For 6.144-MHz System Clock:                      For 5.6448-MHz System Clock:<br>0x77FF = 100 Hz                                      0x6E3F = 100 Hz<br>0x4491 = 175 Hz                                      0x3EFF = 175 Hz<br>0x2FFF = 250 Hz                                      0x2C18 = 250 Hz |
| R146 (0x0092)<br>Haptics_phase_1_intensity        | 7:0  | PHASE1_INTENSITY[7:0] | 0x00    | Haptic Output Level (Phase 1). Selects the signal intensity of Phase 1 in one-shot mode.<br>Coded as 2's complement. Range is ± Full Scale (FS).<br>For ERM actuator, this selects the DC signal level for the haptic output.<br>For LRA actuator, this selects the AC peak amplitude; negative values correspond to a 180° phase shift.                                                                                                                                                                                                                                                                  |
| R147 (0x0093)<br>Haptics_Control_phase_1_duration | 8:0  | PHASE1_DURATION[8:0]  | 0x000   | Haptic Output Duration (Phase 1). Selects the duration of Phase 1 in one-shot mode.<br>0x000 = 0 ms                      0x002 = 1.25 ms                      0x1FF = 319.375 ms<br>0x001 = 0.625 ms                      ... (0.625-ms steps)                                                                                                                                                                                                                                                                                                                                                            |
| R148 (0x0094)<br>Haptics_phase_2_intensity        | 7:0  | PHASE2_INTENSITY[7:0] | 0x00    | Haptic Output Level (Phase 2)<br>Selects the signal intensity in Continuous mode or Phase 2 of one-shot mode.<br>Coded as 2's complement. Range is ± Full Scale (FS).<br>For ERM actuator, this selects the DC signal level for the haptic output.<br>For LRA actuator, this selects the AC peak amplitude; negative values correspond to a 180° phase shift.                                                                                                                                                                                                                                             |
| R149 (0x0095)<br>Haptics_phase_2_duration         | 10:0 | PHASE2_DURATION[10:0] | 0x000   | Haptic Output Duration (Phase 2). Selects the duration of Phase 2 in one-shot mode.<br>0x000 = 0 ms                      0x002 = 1.25 ms                      0x7FF = 1279.375 ms<br>0x001 = 0.625 ms                      ... (0.625-ms steps)                                                                                                                                                                                                                                                                                                                                                           |
| R150 (0x0096)<br>Haptics_phase_3_intensity        | 7:0  | PHASE3_INTENSITY[7:0] | 0x00    | Haptic Output Level (Phase 3). Selects the signal intensity of Phase 3 in one-shot mode.<br>Coded as 2's complement. Range is ± Full Scale (FS).<br>For ERM actuator, this selects the DC signal level for the haptic output.<br>For LRA actuator, this selects the AC peak amplitude; negative values correspond to a 180° phase shift.                                                                                                                                                                                                                                                                  |
| R151 (0x0097)<br>Haptics_phase_3_duration         | 8:0  | PHASE3_DURATION[8:0]  | 0x000   | Haptic Output Duration (Phase 3). Selects the duration of Phase 3 in one-shot mode.<br>0x000 = 0 ms                      0x002 = 1.25 ms                      0x1FF = 319.375 ms<br>0x001 = 0.625 ms                      ... (0.625-ms steps)                                                                                                                                                                                                                                                                                                                                                            |
| R152 (0x0098)<br>Haptics_Status                   | 0    | ONESHOT_STS           | 0       | Haptic One-Shot status<br>0 = One-Shot event not in progress<br>1 = One-Shot event in progress                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

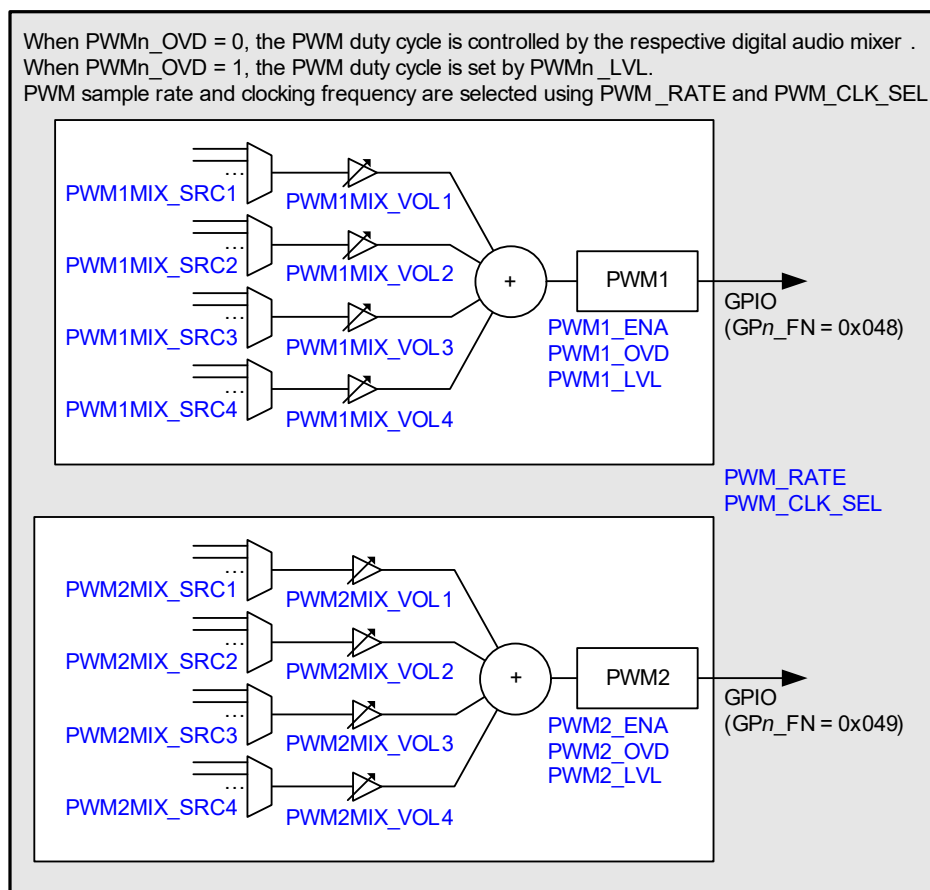
### 4.3.12 PWM Generator

The CS47L35 incorporates two PWM signal generators as shown in [Fig. 4-25](#). The duty cycle of each PWM signal can be modulated by an audio source, or can be set to a fixed value using a control register setting.

A four-input mixer is associated with each PWM generator. The four input sources are selectable in each case, and independent volume control is provided for each path.

PWM signal generators can be output directly on a GPIO pin. See [Section 4.14](#) to configure a GPIO pin for this function.

Note that the PWM signal generators cannot be selected as input to the digital mixers or signal-processing functions within the CS47L35 digital core.



**Figure 4-25. Digital-Core PWM Generator**

The PWM1 and PWM2 mixer control fields (see Fig. 4-25) are located at register addresses R1600–R1615 (0x0640–0x064F).

The full list of digital mixer control registers (R1600–R2936) is provided in Section 6. Generic register field definitions are provided in Table 4-7.

The x\_SRCn fields select the input sources for the respective mixers. Note that the selected input sources must be configured for the same sample rate as the mixer to which they are connected. Sample-rate conversion functions are available to support flexible interconnectivity; see Section 4.3.14.

The PWM generators should be kept disabled (PWMn\_ENA = 0) if SYSCLK is not enabled. The x\_SRCn fields for all digital core functions should be held at 0x00 if SYSCLK is not enabled. SYSCLK must be present and enabled before selecting other values for these fields. See Section 4.16.4 for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The PWM sample rate (cycle time) is configured using PWM\_RATE. See Table 4-21. Note that sample-rate conversion is required when linking the PWM generators to any signal chain that is configured for a different sample rate.

The PWM\_RATE field must not be changed if any of the associated x\_SRCn fields is nonzero. The associated x\_SRCn fields must be cleared before writing a new value to PWM\_RATE. A minimum delay of 125 μs must be allowed between clearing the x\_SRCn fields and writing to PWM\_RATE. See Table 4-21 for details.

The PWM generators are enabled by setting PWM1\_ENA and PWM2\_ENA, respectively, as described in Table 4-20.

Under default conditions (PWMn\_OVD = 0), the duty cycle of the PWM generators is controlled by an audio signal path; a 4-input mixer is associated with each PWM generator, as shown in Fig. 4-25.

When the PWM<sub>n</sub>\_OVD bit is set, the duty cycle of the respective PWM generator is set to a fixed ratio; in this case, the duty cycle ratio is configurable using the PWM<sub>n</sub>\_LVL fields.

The PWM generator clock frequency is selected using PWM\_CLK\_SEL. For best performance, the highest available setting should be used. Note that the PWM generator clock must not be set to a higher frequency than SYSCLK.

**Table 4-20. PWM Generator Control**

| Register Address            | Bit  | Label            | Default | Description                                                                                                                                                                                                                                                                                                                                                                                             |
|-----------------------------|------|------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R48 (0x0030)<br>PWM_Drive_1 | 10:8 | PWM_CLK_SEL[2:0] | 000     | PWM Clock Select<br>000 = 6.144 MHz (5.6448 MHz)<br>001 = 12.288 MHz (11.2896 MHz)<br>010 = 24.576 MHz (22.5792 MHz)<br>All other codes are reserved.<br>The frequencies in brackets apply for 44.1 kHz–related sample rates only.<br>PWM_CLK_SEL controls the resolution of the PWM generator; higher settings correspond to higher resolution.<br>The PWM Clock must be less than or equal to SYSCLK. |
|                             | 5    | PWM2_OVD         | 0       | PWM2 Generator Override<br>0 = Disabled (PWM duty cycle is controlled by audio source)<br>1 = Enabled (PWM duty cycle is controlled by PWM2_LVL).                                                                                                                                                                                                                                                       |
|                             | 4    | PWM1_OVD         | 0       | PWM1 Generator Override<br>0 = Disabled (PWM1 duty cycle is controlled by audio source)<br>1 = Enabled (PWM1 duty cycle is controlled by PWM1_LVL).                                                                                                                                                                                                                                                     |
|                             | 1    | PWM2_ENA         | 0       | PWM2 Generator Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                    |
|                             | 0    | PWM1_ENA         | 0       | PWM1 Generator Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                    |
| R49 (0x0031)<br>PWM_Drive_2 | 9:0  | PWM1_LVL[9:0]    | 0x100   | PWM1 Override Level. Sets the PWM1 duty cycle when PWM1_OVD = 1.<br>Coded as 2's complement.<br>0x000 = 50% duty cycle<br>0x200 = 0% duty cycle                                                                                                                                                                                                                                                         |
| R50 (0x0032)<br>PWM_Drive_3 | 9:0  | PWM2_LVL[9:0]    | 0x100   | PWM2 Override Level. Sets the PWM2 duty cycle when PWM2_OVD = 1.<br>Coded as 2's complement.<br>0x000 = 50% duty cycle<br>0x200 = 0% duty cycle                                                                                                                                                                                                                                                         |

The CS47L35 automatically checks to confirm that the SYSCLK frequency is high enough to support the digital mixer paths. If an attempt is made to enable a PWM signal mixer path, without sufficient SYSCLK cycles to support it, the attempt fails. Note that any signal paths that are already active are not affected under such circumstances.

The status bits in registers R1600–R2936 indicate the status of each of the digital mixers. If an underclocked error condition occurs, these bits indicate which mixers have been enabled.

### 4.3.13 Sample-Rate Control

The CS47L35 supports multiple signal paths through the digital core. Stereo full-duplex sample-rate conversion is provided to allow digital audio to be routed between interfaces operating at different sample rates.

The master clock reference for the audio signal paths is SYSCLK, as described in [Section 4.16](#). Every digital signal path must be synchronized to SYSCLK.

Up to three different sample rates may be in use at any time on the CS47L35; all of these sample rates must be synchronized to SYSCLK.

Sample-rate conversion is required when routing any audio path between digital functions that are configured for different sample rates.

There are two isochronous sample-rate converters: ISRC1 and ISRC2. Each ISRC supports two-way, four-channel conversion paths between sample rates on the SYSCLK domain. The ISRCs are described in [Section 4.3.14](#).

The sample rate of different blocks within the CS47L35 digital core are controlled as shown in [Fig. 4-26](#). The x\_RATE fields select the applicable sample rate for each respective group of digital functions.

The x\_RATE fields must not be changed if any of the x\_SRCn fields associated with the respective functions is nonzero. The associated x\_SRCn fields must be cleared before writing new values to the x\_RATE fields. A minimum delay of 125  $\mu$ s must be allowed between clearing the x\_SRCn fields and writing to the associated x\_RATE fields. See [Table 4-21](#) for details.

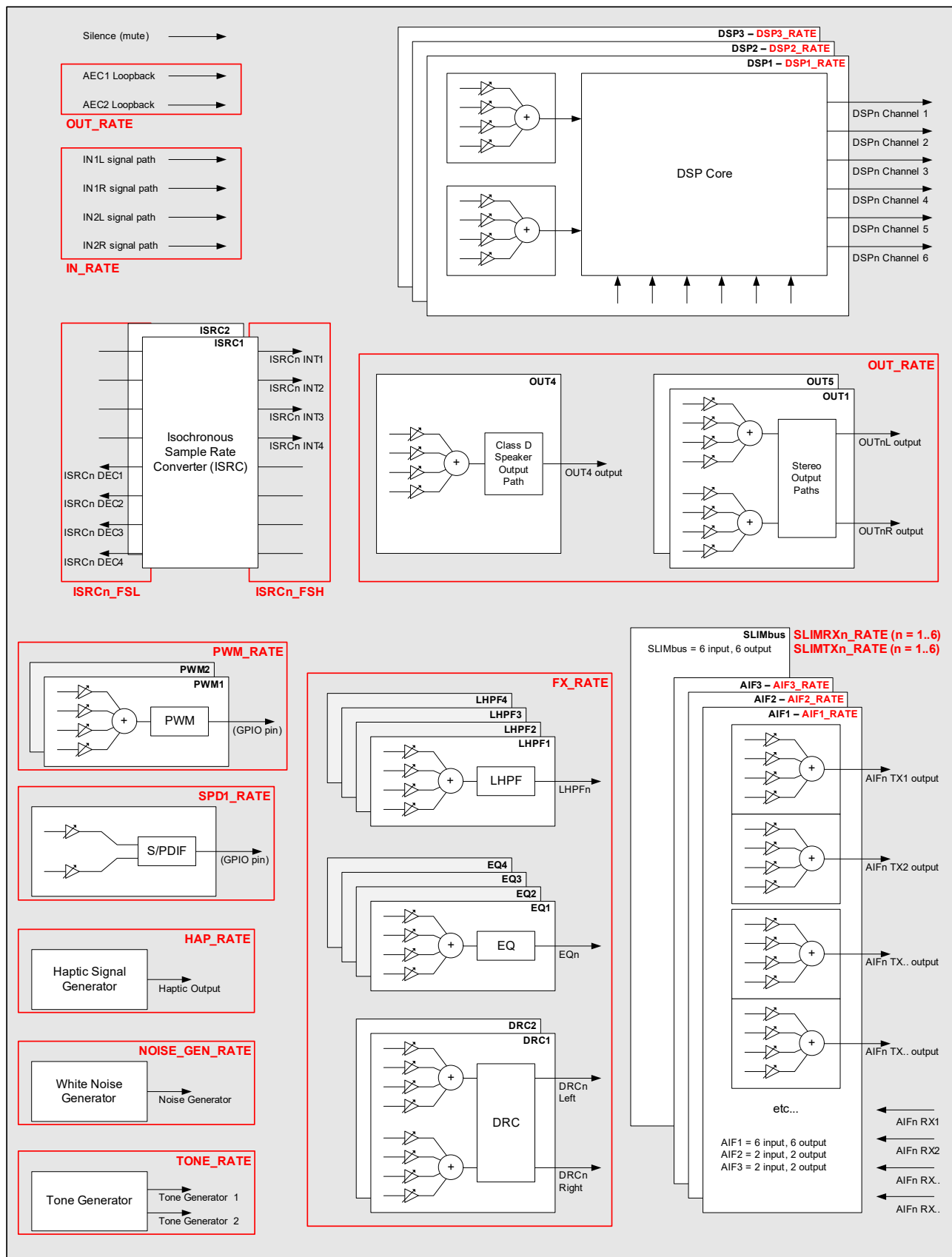


Figure 4-26. Digital-Core Sample-Rate Control

The input signal paths may be selected as input to the digital mixers or signal-processing functions. The sample rate for the input signal paths is configured using the IN\_RATE field.

The output signal paths are derived from the respective output mixers. The sample rate for the output signal paths is configured using OUT\_RATE. The sample rate of the AEC loop-back path is also set by OUT\_RATE.

The AIF $n$  RX inputs may be selected as input to the digital mixers or signal-processing functions. The AIF $n$  TX outputs are derived from the respective output mixers. The sample rates for digital audio interfaces (AIF1–AIF3) are configured using the AIF $n$ \_RATE fields (where  $n$  identifies the applicable AIF 1, 2, or 3) respectively.

The SLIMbus interface supports up to six input channels and six output channels. The sample rate of each channel can be configured independently, using SLIMTX $n$ \_RATE and SLIMRX $n$ \_RATE.

The EQ, DRC, and LHPF functions can be enabled in any signal path within the digital core. The sample rate for these functions is configured using FX\_RATE. Note that the EQ, DRC, and LHPF functions must all be configured for the same sample rate.

The DSP $n$  functions can be enabled in any signal path within the digital core. The applicable sample rates are configured using the DSP $n$ \_RATE fields (where  $n$  identifies the applicable DSP block, 1 to 3) respectively.

The S/PDIF transmitter can be enabled on a GPIO pin. Stereo inputs to this function can be configured from any of the digital-core inputs, mixers, or signal-processing functions. The sample rate of the S/PDIF transmitter is configured using SPD1\_RATE.

The tone generators and noise generator can be selected as input to any of the digital mixers or signal-processing functions. The sample rates for these sources are configured using the TONE\_RATE and NOISE\_GEN\_RATE fields, respectively.

The haptic signal generator can be used to control an external vibrate actuator, which can be driven directly by the Class D speaker output or The sample rate for the haptic signal generator is configured using HAP\_RATE.

The PWM signal generators can be modulated by an audio source, derived from the associated signal mixers. The sample rate (cycle time) for the PWM signal generators is configured using PWM\_RATE.

The sample-rate control registers are described in [Table 4-21](#). Refer to the field descriptions for details of the valid selections in each case. The control registers associated with the ISRCs are described in [Table 4-22](#).

Note that 32-bit register addressing is used from R12888 (0x3000) upwards; 16-bit format is used otherwise. The registers noted in [Table 4-21](#) contain a mixture of 16-bit and 32-bit register addresses.

**Table 4-21. Digital-Core Sample-Rate Control**

| Register Address                   | Bit   | Label          | Default | Description                                                                                                                                                                                                                                                            |
|------------------------------------|-------|----------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R32 (0x0020)<br>Tone_Generator_1   | 14:11 | TONE_RATE[3:0] | 0000    | Tone Generator Sample Rate<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 8–192 kHz.                                                                       |
| R48 (0x0030)<br>PWM_Drive_1        | 14:11 | PWM_RATE[3:0]  | 0000    | PWM Frequency (sample rate)<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 8–192 kHz.<br>All PWMnMIX_SRCm fields must be cleared before changing PWM_RATE. |
| R144 (0x0090)<br>Haptics_Control_1 | 14:11 | HAP_RATE[3:0]  | 0000    | Haptic Signal Generator Sample Rate<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 8–192 kHz.                                                              |

**Table 4-21. Digital-Core Sample-Rate Control (Cont.)**

| Register Address                         | Bit   | Label               | Default | Description                                                                                                                                                                                                                                                                                                                                                             |
|------------------------------------------|-------|---------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R160 (0x00A0)<br>Comfort_Noise_Generator | 14:11 | NOISE_GEN_RATE[3:0] | 0000    | Noise Generator Sample Rate<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 8–192 kHz.                                                                                                                                                                       |
| R776 (0x0308)<br>Input_Rate              | 14:11 | IN_RATE[3:0]        | 0000    | Input Signal Paths Sample Rate<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 8kHz to 192kHz.<br>If 384 kHz/768 kHz DMIC rate is selected on any of the input paths (INn_OSR = 01X), the input paths sample rate is valid up to 48 kHz/96 kHz respectively. |
| R1032 (0x0408)<br>Output_Rate_1          | 14:11 | OUT_RATE[3:0]       | 0000    | Output Signal Paths Sample Rate<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 8–192 kHz.<br>All OUTnMIX_SRCm fields must be cleared before changing OUT_RATE.                                                                                              |
| R1283 (0x0503)<br>AIF1_Rate_Ctrl         | 14:11 | AIF1_RATE[3:0]      | 0000    | AIFn Audio Interface Sample Rate<br>0000 = SAMPLE_RATE_1                                                                                                                                                                                                                                                                                                                |
| R1347 (0x0543)<br>AIF2_Rate_Ctrl         | 14:11 | AIF2_RATE[3:0]      | 0000    | 0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3                                                                                                                                                                                                                                                                                                                            |
| R1411 (0x0583)<br>AIF3_Rate_Ctrl         | 14:11 | AIF3_RATE[3:0]      | 0000    | All other codes are reserved.<br>The selected sample rate is valid in the range 8–192 kHz.<br>All AIFnTXMIX_SRCm fields must be cleared before changing AIFn_RATE.                                                                                                                                                                                                      |
| R1474 (0x05C2)<br>SPD1_TX_Control        | 7:4   | SPD1_RATE[3:0]      | 0000    | S/PDIF Transmitter Sample Rate<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 32–192 kHz.<br>All SPDIF1TXn_SRC fields must be cleared before changing SPD1_RATE.                                                                                            |
| R1509 (0x05E5)<br>SLIMbus_Rates_1        | 14:11 | SLIMRX2_RATE[3:0]   | 0000    | SLIMbus RX Channel n Sample Rate<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 8–192 kHz.                                                                                                                                                                  |
|                                          | 6:3   | SLIMRX1_RATE[3:0]   | 0000    |                                                                                                                                                                                                                                                                                                                                                                         |
| R1510 (0x05E6)<br>SLIMbus_Rates_2        | 14:11 | SLIMRX4_RATE[3:0]   | 0000    |                                                                                                                                                                                                                                                                                                                                                                         |
|                                          | 6:3   | SLIMRX3_RATE[3:0]   | 0000    |                                                                                                                                                                                                                                                                                                                                                                         |
| R1511 (0x05E7)<br>SLIMbus_Rates_3        | 14:11 | SLIMRX6_RATE[3:0]   | 0000    |                                                                                                                                                                                                                                                                                                                                                                         |
|                                          | 6:3   | SLIMRX5_RATE[3:0]   | 0000    |                                                                                                                                                                                                                                                                                                                                                                         |
| R1513 (0x05E9)<br>SLIMbus_Rates_5        | 14:11 | SLIMTX2_RATE[3:0]   | 0000    | SLIMbus TX Channel n Sample Rate<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 8–192 kHz.<br>All SLIMTXnMIX_SRCm fields must be cleared before changing SLIMTXn_RATE.                                                                                      |
|                                          | 6:3   | SLIMTX1_RATE[3:0]   | 0000    |                                                                                                                                                                                                                                                                                                                                                                         |
| R1514 (0x05EA)<br>SLIMbus_Rates_6        | 14:11 | SLIMTX4_RATE[3:0]   | 0000    |                                                                                                                                                                                                                                                                                                                                                                         |
|                                          | 6:3   | SLIMTX3_RATE[3:0]   | 0000    |                                                                                                                                                                                                                                                                                                                                                                         |
| R1515 (0x05EB)<br>SLIMbus_Rates_7        | 14:11 | SLIMTX6_RATE[3:0]   | 0000    |                                                                                                                                                                                                                                                                                                                                                                         |
|                                          | 6:3   | SLIMTX5_RATE[3:0]   | 0000    |                                                                                                                                                                                                                                                                                                                                                                         |

**Table 4-21. Digital-Core Sample-Rate Control (Cont.)**

| Register Address                          | Bit   | Label          | Default | Description                                                                                                                                                                                                                                                                                              |
|-------------------------------------------|-------|----------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R3584 (0x0E00)<br>FX_Ctrl1                | 14:11 | FX_RATE[3:0]   | 0000    | FX Sample Rate (EQ, LHPF, DRC)<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 8–192 kHz.<br>All EQnMIX_SRCm, DRCnMIX_SRCm, and LHPFnMIX_SRCm fields must be cleared before changing FX_RATE. |
| R1048064 (0x0F_<br>FE00)<br>DSP1_Config_1 | 14:11 | DSP1_RATE[3:0] | 0000    | DSP1 Sample Rate<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 8–192 kHz.                                                                                                                   |
| R1572352 (0x17_<br>FE00)<br>DSP2_Config_1 | 14:11 | DSP2_RATE[3:0] | 0000    | All DSPnMIX_SRCm fields must be cleared before changing DSPn_RATE.                                                                                                                                                                                                                                       |
| R2096640 (0x1F_<br>FE00)<br>DSP3_Config_1 | 14:11 | DSP3_RATE[3:0] | 0000    |                                                                                                                                                                                                                                                                                                          |

#### 4.3.14 Isochronous Sample-Rate Converter (ISRC)

The CS47L35 supports multiple signal paths through the digital core. The ISRCs provide sample-rate conversion between synchronized sample rates on the SYSCLK clock domain.

There are two ISRCs on the CS47L35. Each ISRC provides four signal paths between two different sample rates, as shown in [Fig. 4-27](#). The sample rates associated with each ISRC can each be set equal to SAMPLE\_RATE\_1, SAMPLE\_RATE\_2, or SAMPLE\_RATE\_3. See [Section 4.16](#) for details of the sample-rate control registers.

Each ISRC supports sample rates in the range 8–192 kHz. The higher of the sample rates associated with each ISRC must be an integer multiple of the lower sample rate; all possible integer ratios are supported (i.e., up to 24).

Each ISRC converts between a sample rate selected by ISRCn\_FSL and a sample rate selected by ISRCn\_FSH, (where *n* identifies the applicable ISRC 1 or 2). Note that, in each case, the higher of the two sample rates must be selected by ISRCn\_FSH.

The ISRCn\_FSL and ISRCn\_FSH fields must not be changed if any of the respective x\_SRCn fields is nonzero. The associated x\_SRCn fields must be cleared before writing new values to ISRCn\_FSL or ISRCn\_FSH. A minimum delay of 125 μs must be allowed between clearing the x\_SRCn fields and writing to the associated ISRCn\_FSL or ISRCn\_FSH fields. See [Table 4-22](#) for details.

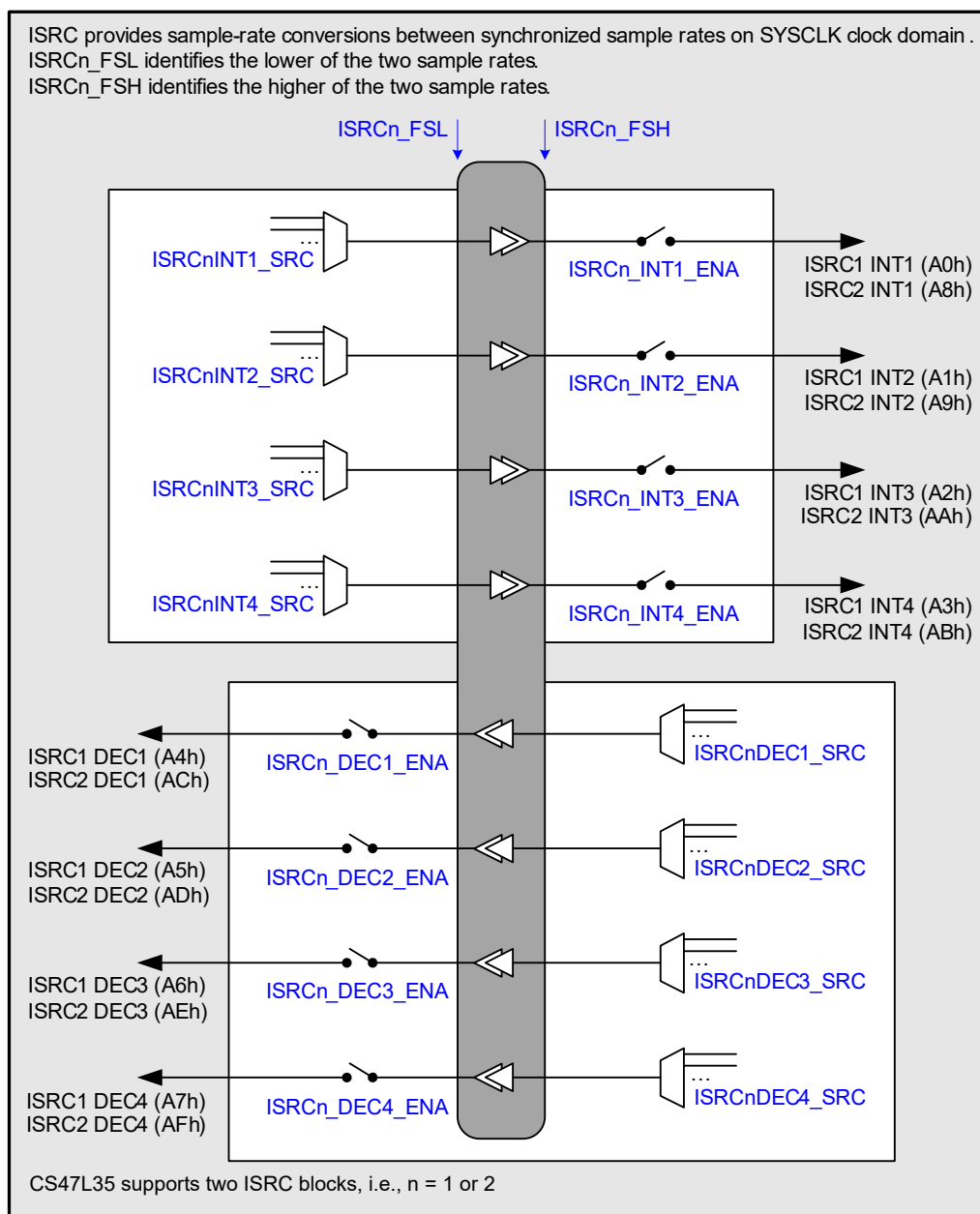
The ISRC signal paths are enabled using the ISRCn\_INTm\_ENA and ISRCn\_DECm\_ENA bits, as follows:

- The ISRCn interpolation paths (increasing sample rate) are enabled by setting the ISRCn\_INTm\_ENA bits, (where *m* identifies the applicable channel).
- The ISRCn decimation paths (decreasing sample rate) are enabled by setting the ISRCn\_DECm\_ENA bits.

The CS47L35 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded ISRC and digital mixing functions. If the frequency is too low, an attempt to enable an ISRC signal path fails. Note that active signal paths are not affected under such circumstances.

The status bits in registers R1600–R2936 indicate the status of each of the digital mixers. If an underclocked error condition occurs, these bits indicate which mixers have been enabled.

The ISRC signal paths and control registers are shown in [Fig. 4-27](#).



**Figure 4-27. Isochronous Sample-Rate Converters (ISRCs)**

The ISRC input control fields (see [Fig. 4-27](#)) are located at register addresses R2816–R2936 (0x0B00–0x0B78).

The full list of digital mixer control registers (R1600–R2936) is provided in [Section 6](#). Generic register field definitions are provided in [Table 4-7](#).

The x\_SRC fields select the input sources for the respective ISRC processing blocks. Note that the selected input sources must be configured for the same sample rate as the ISRC to which they are connected.

The hexadecimal numbers in [Fig. 4-27](#) indicate the corresponding x\_SRC setting for selection of that signal as an input to another digital-core function.

The ISRC paths should be kept disabled (ISRCn\_INTm\_ENA = 0, ISRCn\_DECm\_ENA = 0) if SYSCLK is not enabled. The x\_SRCn fields for all digital core functions should be held at 0x00 if SYSCLK is not enabled. SYSCLK must be present and enabled before selecting other values for these fields. See [Section 4.16.4](#) for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The register bits associated with the ISRCs are described in [Table 4-22](#).

**Table 4-22. Digital-Core ISRC Control**

| Register Address               | Bit   | Label          | Default | Description                                                                                                                                                                                                                                                                                                             |
|--------------------------------|-------|----------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R3824 (0x0EF0)<br>ISRC1_CTRL_1 | 14:11 | ISRC1_FSH[3:0] | 0000    | ISRC1 High Sample Rate (Sets the higher of the ISRC1 sample rates)<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 8 kHz to 192 kHz.<br>All ISRC1_DECn_SRC fields must be cleared before changing ISRC1_FSH. |
| R3825 (0x0EF1)<br>ISRC1_CTRL_2 | 14:11 | ISRC1_FSL[3:0] | 0000    | ISRC1 Low Sample Rate (Sets the lower of the ISRC1 sample rates)<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 8 kHz to 192 kHz.<br>All ISRC1_INTn_SRC fields must be cleared before changing ISRC1_FSL.   |
| R3826 (0x0EF2)<br>ISRC1_CTRL_3 | 15    | ISRC1_INT1_ENA | 0       | ISRC1 INT1 Enable (Interpolation Channel 1 path from ISRC1_FSL rate to ISRC1_FSH rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                   |
|                                | 14    | ISRC1_INT2_ENA | 0       | ISRC1 INT2 Enable (Interpolation Channel 2 path from ISRC1_FSL rate to ISRC1_FSH rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                   |
|                                | 13    | ISRC1_INT3_ENA | 0       | ISRC1 INT3 Enable (Interpolation Channel 3 path from ISRC1_FSL rate to ISRC1_FSH rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                   |
|                                | 12    | ISRC1_INT4_ENA | 0       | ISRC1 INT4 Enable (Interpolation Channel 4 path from ISRC1_FSL rate to ISRC1_FSH rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                   |
|                                | 9     | ISRC1_DEC1_ENA | 0       | ISRC1 DEC1 Enable (Decimation Channel 1 path from ISRC1_FSH rate to ISRC1_FSL rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                      |
|                                | 8     | ISRC1_DEC2_ENA | 0       | ISRC1 DEC2 Enable (Decimation Channel 2 path from ISRC1_FSH rate to ISRC1_FSL rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                      |
|                                | 7     | ISRC1_DEC3_ENA | 0       | ISRC1 DEC3 Enable (Decimation Channel 3 path from ISRC1_FSH rate to ISRC1_FSL rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                      |
|                                | 6     | ISRC1_DEC4_ENA | 0       | ISRC1 DEC4 Enable (Decimation Channel 4 path from ISRC1_FSH rate to ISRC1_FSL rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                      |
| R3827 (0x0EF3)<br>ISRC2_CTRL_1 | 14:11 | ISRC2_FSH[3:0] | 0000    | ISRC2 High Sample Rate (Sets the higher of the ISRC2 sample rates)<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 8 kHz to 192 kHz.<br>All ISRC2_DECn_SRC fields must be cleared before changing ISRC2_FSH. |

**Table 4-22. Digital-Core ISRC Control (Cont.)**

| Register Address               | Bit   | Label          | Default | Description                                                                                                                                                                                                                                                                                                           |
|--------------------------------|-------|----------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R3828 (0x0EF4)<br>ISRC2_CTRL_2 | 14:11 | ISRC2_FSL[3:0] | 0000    | ISRC2 Low Sample Rate (Sets the lower of the ISRC2 sample rates)<br>0000 = SAMPLE_RATE_1<br>0001 = SAMPLE_RATE_2<br>0010 = SAMPLE_RATE_3<br>All other codes are reserved.<br>The selected sample rate is valid in the range 8 kHz to 192 kHz.<br>All ISRC2_INTn_SRC fields must be cleared before changing ISRC2_FSL. |
| R3829 (0x0EF5)<br>ISRC2_CTRL_3 | 15    | ISRC2_INT1_ENA | 0       | ISRC2 INT1 Enable (Interpolation Channel 1 path from ISRC2_FSL rate to ISRC2_FSH rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                 |
|                                | 14    | ISRC2_INT2_ENA | 0       | ISRC2 INT2 Enable (Interpolation Channel 2 path from ISRC2_FSL rate to ISRC2_FSH rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                 |
|                                | 13    | ISRC2_INT3_ENA | 0       | ISRC2 INT3 Enable (Interpolation Channel 3 path from ISRC2_FSL rate to ISRC2_FSH rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                 |
|                                | 12    | ISRC2_INT4_ENA | 0       | ISRC2 INT4 Enable (Interpolation Channel 4 path from ISRC2_FSL rate to ISRC2_FSH rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                 |
|                                | 9     | ISRC2_DEC1_ENA | 0       | ISRC2 DEC1 Enable (Decimation Channel 1 path from ISRC2_FSH rate to ISRC2_FSL rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                    |
|                                | 8     | ISRC2_DEC2_ENA | 0       | ISRC2 DEC2 Enable (Decimation Channel 2 path from ISRC2_FSH rate to ISRC2_FSL rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                    |
|                                | 7     | ISRC2_DEC3_ENA | 0       | ISRC2 DEC3 Enable (Decimation Channel 3 path from ISRC2_FSH rate to ISRC2_FSL rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                    |
|                                | 6     | ISRC2_DEC4_ENA | 0       | ISRC2 DEC4 Enable (Decimation Channel 4 path from ISRC2_FSH rate to ISRC2_FSL rate)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                    |

## 4.4 DSP Firmware Control

The CS47L35 digital core incorporates three DSP processing blocks, capable of running a wide range of audio-enhancement functions. Different firmware configurations can be loaded onto each DSP, enabling the CS47L35 to be highly customized for specific application requirements. Full read/write access to the device register map is supported from each DSP core, including access to the firmware registers of the other DSPs. Synchronization of different DSPs is supported, and shared data memory space is provided for the DSP2 and DSP3 blocks; these features enable enhanced processing capabilities for the associated DSPs.

Examples of the DSP functions include multiband compressor (MBC), and the SoundClear™ suite of audio processing algorithms. Note that it is possible to implement more than one type of audio enhancement function on a single DSP; the precise combinations of functions vary from one firmware configuration to another.

The DSP blocks each employ the same internal architecture and provide an equivalent processing capability. Note that the DSPs differ in terms of the firmware memory sizes associated with each. The DSPs can be clocked at up to 150MHz, corresponding to 150 MIPS each.

DSP firmware can be configured using software packages provided by Cirrus Logic. A software programming guide can also be provided to assist users in developing their own software algorithms—please contact your Cirrus Logic representative for further information.

To use the DSP blocks, the required firmware configuration must first be loaded onto the device by writing the appropriate files to the CS47L35 register map. The firmware configuration comprises program, data, and coefficient content. In some cases, the coefficient content must be derived using tools provided in the WISCE evaluation board control software.

Details of the DSP firmware memory registers are provided in [Section 4.4.1](#). Note that the WISCE evaluation board control software provides support for easy loading of program, data, and coefficient content onto the CS47L35. Please contact your Cirrus Logic representative for more details of the WISCE evaluation board control software.

After loading the DSP firmware, the DSP functions must be enabled using the associated control fields.

The audio signal paths to and from the DSP processing blocks are configured as described in [Section 4.3](#). Note that the DSP firmware must be loaded and enabled before audio signal paths can be enabled.

### 4.4.1 DSP Firmware Memory and Register Mapping

The DSP firmware memory is programmed by writing to the registers referenced in [Table 4-23](#). Note that clocking is not required for access to the firmware registers by the host processor.

The CS47L35 program, data, and coefficient register memory space is described in [Table 4-23](#). The full register map listing is provided in [Section 6](#). The shared DSP2/DSP3 memory space is implemented at two different register address locations; reading or writing at either address accesses the same memory data.

If multiple DSPs write to a shared-memory address at the same time, the address at which the collision occurred is reported in the DSP2\_DUALMEM\_COLLISION\_ADDR and DSP3\_DUALMEM\_COLLISION\_ADDR fields. Note that these fields are coded in 24-bit DSP data word units, and are defined relative to the base address of the shared-memory area. The DSP2\_DUALMEM\_COLLISION\_ADDR and DSP3\_DUALMEM\_COLLISION\_ADDR fields provide the same information.

The DSP memory controller provides an input to the interrupt control circuit. An interrupt event is triggered if a memory collision occurs. Note that the DSP software should be written to ensure this never happens; the interrupt is intended for development purposes only. See [Section 4.15](#) for details of the interrupt-event handling.

The program firmware parameters are formatted as 40-bit words. For this reason, 3 x 32-bit register addresses are required for every 2 x 40-bit words.

**Table 4-23. DSP Program, Data, and Coefficient Registers**

| DSP Number | Description                      | Register Address    | Number of Registers | DSP Memory Size    |
|------------|----------------------------------|---------------------|---------------------|--------------------|
| DSP1       | Program memory                   | 0x08_0000–0x08_5FFE | 12288               | 8k x 40-bit words  |
|            | X-Data memory                    | 0x0A_0000–0x0A_7FFE | 16384               | 16k x 24-bit words |
|            | Y-Data memory                    | 0x0C_0000–0x0C_1FFE | 4096                | 4k x 24-bit words  |
|            | Coefficient memory               | 0x0E_0000–0x0E_1FFE | 4096                | 4k x 24-bit words  |
| DSP2       | Program memory                   | 0x10_0000–0x10_EFFE | 30720               | 20k x 40-bit words |
|            | X-Data memory                    | 0x12_0000–0x12_BFFE | 24576               | 24k x 24-bit words |
|            | X-Data memory (Shared DSP2/DSP3) | 0x13_6000–0x13_7FFE | 4096                | 4k x 24-bit words  |
|            | Y-Data memory                    | 0x14_0000–0x14_BFFE | 24576               | 24k x 24-bit words |
|            | Coefficient memory               | 0x16_0000–0x16_1FFE | 4096                | 4k x 24-bit words  |
| DSP3       | Program memory                   | 0x18_0000–0x18_EFFE | 30720               | 20k x 40-bit words |
|            | X-Data memory                    | 0x1A_0000–0x1B_1FFE | 36864               | 36k x 24-bit words |
|            | X-Data memory (Shared DSP2/DSP3) | 0x1B_6000–0x1B_7FFE | 4096                | 4k x 24-bit words  |
|            | Y-Data memory                    | 0x1C_0000–0x1C_BFFE | 24576               | 24k x 24-bit words |
|            | Coefficient memory               | 0x1E_0000–0x1E_1FFE | 4096                | 4k x 24-bit words  |

The X-memory on each DSP supports read/write access to all register fields throughout the device, including the codec control registers, and the firmware memory of all of the integrated DSP cores. Access to the register address space is supported using a number of register windows within the X-memory on each DSP.

The register window space is additional to the X-data memory sizes described in [Table 4-23](#). Note that the X-memory addresses of these register windows are the same for all DSP cores, regardless of the different X-memory sizes.

Addresses 0xC000 to 0xDFFF in X-memory map directly to addresses 0x0000 to 0x1FFF in the device register space. This fixed register window contains primarily the codec control registers; it also includes the virtual DSP control registers (described in [Section 4.4.6](#)). Each X-memory address within this window maps onto one 16-bit register in the codec memory space.

Four movable register windows are also provided, starting at X-memory addresses 0xF000, 0xF400, 0xF800, and 0xFC00 respectively. Each window represents 1024 addresses in the X-memory space. The start address, within the corresponding device register space, for each window is configured using DSP<sub>n</sub>\_EXT\_[A/B/C/D]\_PAGE (where A defines the first window, B defines the second window, etc.).

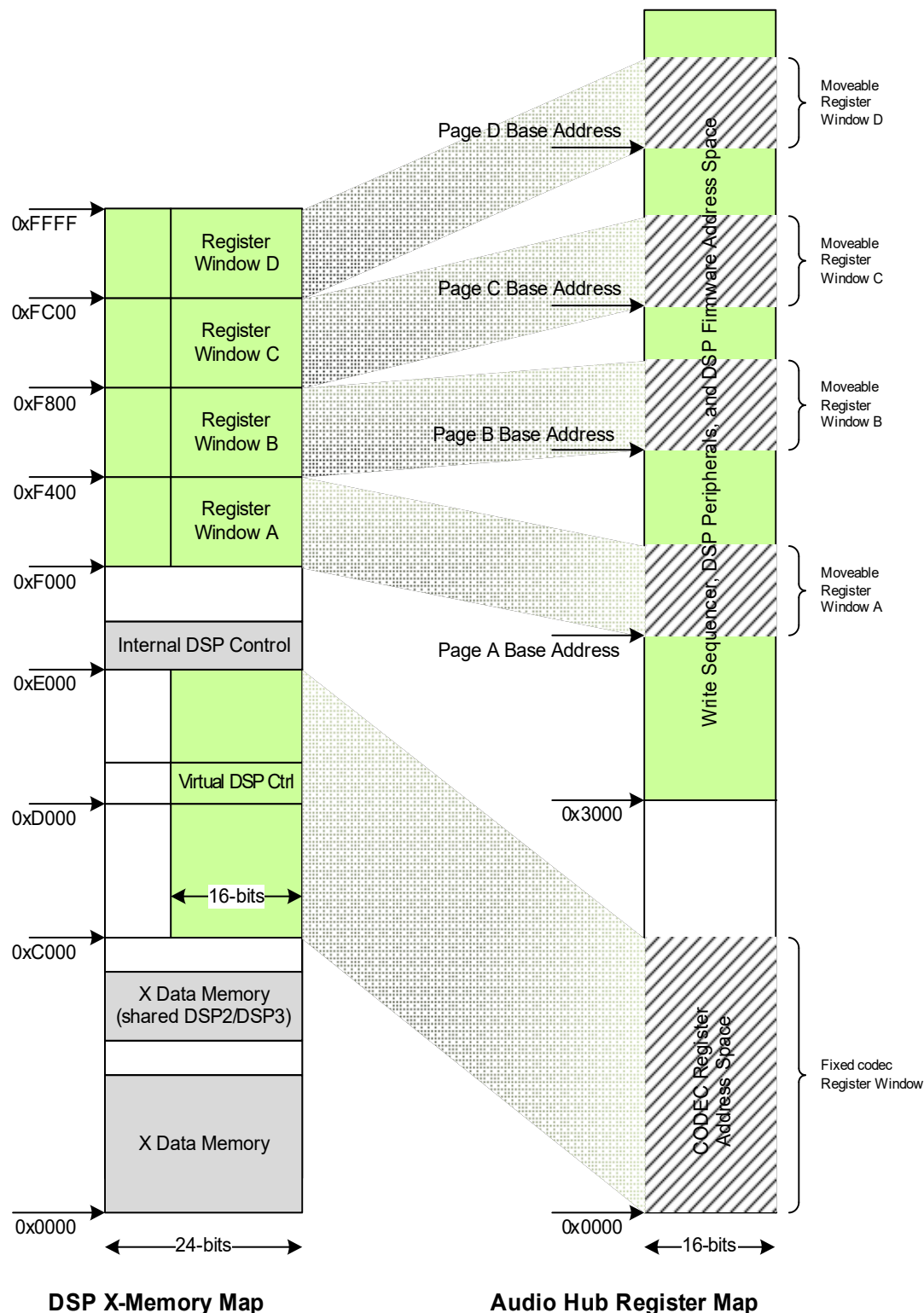
Two mapping modes are supported and are selected using the DSP<sub>n</sub>\_EXT\_[A/B/C/D]\_PSIZE16 bits for the respective window. In 16-Bit Mode, each address within the window maps onto one 16-bit register in the device memory space; the window equates to 1024 x 16-bit registers. In 32-Bit Mode, each address within the window maps onto two 16-bit registers in the device memory space; the window equates to 1024 x 32-bit registers.

Note that the X-memory is only 24-bits wide; as a result, the upper 8 bits of the odd-numbered register addresses are not mapped, and cannot be accessed, in 32-Bit Mode.

The DSP<sub>n</sub>\_EXT\_[A/B/C/D]\_PAGE fields are defined with an LSB = 512. Accordingly, the base address of each window must be aligned with 512-word boundaries. Note that the base addresses are entirely independent of each other; for example, overlapping windows are permissible if required, and there is no requirement for the A/B/C/D windows to be at incremental locations.

The register map window functions are shown in [Fig. 4-28](#). Further information on the definition and usage of the DSP firmware memories is provided in the software programming guide; contact your Cirrus Logic representative if required.

Note that SYSCLK must be present and enabled, if the DSP firmware requires read or write access to control registers below address 0x40000. See [Section 4.16](#) for further details of the CS47L35 system clocks.



**Figure 4-28. X-Data Memory Map**

Note that the full CS47L35 register space is shown here as 16-bit width. (SPI/I<sup>2</sup>C/SLIMbus register access uses 32-bit data width at 0x3000 and above.) However, the window base address fields (DSPn\_EXT\_[A/B/C/D]\_PAGE) are referenced to 16-bit width, and 16-bit register mapping is shown. Hence, the device register map is shown here entirely as 16-bit width for ease of explanation.

The control registers associated with the register map window functions are described in [Table 4-24](#).

**Table 4-24. X-Data Memory and Clocking Control**

| Register Address                                                                                                                 | Bit  | Label                 | Default | Description                                                                                                                           |
|----------------------------------------------------------------------------------------------------------------------------------|------|-----------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------|
| DSP1 Base Address = R1048064 (0x0F_FE00)<br>DSP2 Base Address = R1572352 (0x17_FE00)<br>DSP3 Base Address = R2096640 (0x1F_FE00) |      |                       |         |                                                                                                                                       |
| Base address + 0x54<br>DSPn_Ext_window_A                                                                                         | 31   | DSPn_EXT_A_PSIZE16    | 0       | Register Window A page width select<br>0 = 32-bit<br>1 = 16-bit<br>Note that, in 32-Bit Mode, only the lower 24 bits can be accessed. |
|                                                                                                                                  | 15:0 | DSPn_EXT_A_PAGE[15:0] | 0x0000  | Sets the Base Address of Register Window A in X-memory.<br>Coded as LSB = 512 (0x200)                                                 |
| Base address + 0x56<br>DSPn_Ext_window_B                                                                                         | 31   | DSPn_EXT_B_PSIZE16    | 0       | Register Window B page width select<br>0 = 32-bit<br>1 = 16-bit<br>Note that, in 32-Bit Mode, only the lower 24 bits can be accessed. |
|                                                                                                                                  | 15:0 | DSPn_EXT_B_PAGE[15:0] | 0x0000  | Sets the Base Address of Register Window B in X-memory.<br>Coded as LSB = 512 (0x200)                                                 |
| Base address + 0x58<br>DSPn_Ext_window_C                                                                                         | 31   | DSPn_EXT_C_PSIZE16    | 0       | Register Window C page width select<br>0 = 32-bit<br>1 = 16-bit<br>Note that, in 32-Bit Mode, only the lower 24 bits can be accessed. |
|                                                                                                                                  | 15:0 | DSPn_EXT_C_PAGE[15:0] | 0x0000  | Sets the Base Address of Register Window C in X-memory.<br>Coded as LSB = 512 (0x200)                                                 |
| Base address + 0x5A<br>DSPn_Ext_window_D                                                                                         | 31   | DSPn_EXT_D_PSIZE16    | 0       | Register Window D page width select<br>0 = 32-bit<br>1 = 16-bit<br>Note that, in 32-Bit Mode, only the lower 24 bits can be accessed. |
|                                                                                                                                  | 15:0 | DSPn_EXT_D_PAGE[15:0] | 0x0000  | Sets the Base Address of Register Window D in X-memory.<br>Coded as LSB = 512 (0x200)                                                 |

## 4.4.2 DSP Firmware Control

The configuration and control of the DSP firmware is described in the following subsections.

### 4.4.2.1 DSP Memory

The DSP memory (program, X-data, Y-data, and coefficient) is enabled by setting DSPn\_MEM\_ENA for the respective DSP. This memory must be enabled (DSPn\_MEM\_ENA = 1) for read/write access, code execution, and DMA functions. The DSP memory is disabled, and the contents lost, whenever the respective DSPn\_MEM\_ENA bit is cleared.

The DSPn\_MEM\_ENA bits are not affected by software reset; these bits remain in their previous state under software reset conditions. Accordingly, the DSP memory contents are maintained through software reset, provided DCVDD is held above its reset threshold.

The DSP firmware memory is always cleared under power-on reset, hardware reset, and Sleep Mode conditions. See [Section 5](#) for a summary of the CS47L35 reset behavior.

### 4.4.2.2 DSP Clocking

Clocking is required for each of the DSP processing blocks, when executing software or when supporting DMA functions. (Note that clocking is not required for access to the firmware registers by the host processor.)

Clocking within each DSP is enabled and disabled automatically, as required by the respective DSP core and DMA channel status.

The clock source for each DSP is derived from DSPCLK. See [Section 4.16](#) for details of how to configure DSPCLK.

The clock frequency for each DSP is selected using the DSPn\_CLK\_SEL field (where *n* identifies the applicable DSP block, 1 to 3). The DSP clock frequency must be less than or equal to the DSPCLK frequency.

Note that the `DSPn_CLK_SEL` fields select a range of frequencies for each valid decode value. The clock frequency for each DSP is derived as `DSPCLK` divided by 1, 2, 4, 8, or 16. The required division ratios, within the selected DSP clock frequency ranges, are configured automatically for each DSP core.

The `DSPn_CLK_SEL_STS` fields indicate the clock frequency range for the respective DSP cores. These can be used to confirm the clock frequency, in cases where code execution has a minimum clock frequency requirement. The `DSPn_CLK_SEL_STS` field is only valid when the respective core is running code; typical usage of this field would be for the DSP core itself to read the clock status and to take action as applicable, in particular, if the available clock does not meet the application requirements.

Note that the `DSPn_CLK_SEL_STS` fields indicate a range of frequencies for each decode value. The exact clock frequency for each DSP cannot be provided directly by the CS47L35, but can be derived using knowledge of the `DSPCLK` frequency, if available.

#### 4.4.2.3 DSP Code Execution

After the DSP firmware has been loaded, and the clocks configured, the DSP blocks are enabled by setting the `DSPn_CORE_ENA` bits. When the DSP is configured and enabled, the firmware execution can be started by writing 1 to the respective `DSPn_START` bit.

Alternative methods to trigger the firmware execution can also be configured using the `DSPn_START_IN_SEL` fields. Note that this provides the capability to synchronously trigger multiple DSP blocks.

Using the `DSPn_START_IN_SEL` fields, the DSP firmware execution can be linked to the respective DMA function, the `IRQ2` status, `DSPn` start signals from another DSP, or to the `FIFO` status in one of the event loggers:

- **DMA function:** firmware execution commences when all enabled DSP input (WDMA) channel buffers have been filled, and all enabled DSP output (RDMA) channel buffers have been emptied
- **DSPn start signals:** firmware execution commences when the respective start signal is triggered in the selected DSP core
- **IRQ2:** firmware execution commences when one or more of the unmasked `IRQ2` events has occurred
- **Event logger status:** firmware execution commences when the `FIFO` not-empty status is asserted within the respective event logger

To enable firmware execution on the respective DSP block, the `DSPn_CORE_ENA` bit must be set. Note that the usage of the `DSPn_START` bit may vary depending on the particular firmware that is being executed: in some applications (e.g., when an alternative trigger is selected using `DSPn_START_IN_SEL`), writing to the `DSPn_START` bit is not required.

The `DSPCLK` system clock must be configured and enabled before any DSP processing core is enabled. The DSP blocks should be kept disabled (`DSPn_CORE_ENA` = 0) if `DSPCLK` is not enabled. See [Section 4.16](#) for details of the system clocks (including requirements for reconfiguring `DSPCLK` while DSP cores are enabled).

#### 4.4.2.4 DSP Control Registers

The DSP memory, clocking, and code-execution control registers are described in [Table 4-25](#).

The audio signal paths connecting to/from the DSP processing blocks are configured as described in [Section 4.3](#). Note that the DSP firmware must be loaded and enabled before audio signal paths can be enabled.

**Table 4-25. DSP Memory and Clocking Control**

| Register Address                                                                                                                 | Bit   | Label                             | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|----------------------------------------------------------------------------------------------------------------------------------|-------|-----------------------------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DSP1 Base Address = R1048064 (0x0F_FE00)<br>DSP2 Base Address = R1572352 (0x17_FE00)<br>DSP3 Base Address = R2096640 (0x1F_FE00) |       |                                   |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| Base address<br>DSPn_Config_1                                                                                                    | 18:16 | DSPn_CLK_SEL[2:0]                 | 000     | DSPn clock frequency select<br>000 = 5.5 MHz to 9.375 MHz<br>001 = 9.375 MHz to 18.75 MHz<br>010 = 18.75 MHz to 37.5 MHz<br>011 = 37.5 MHz to 75 MHz<br>100 = 75 MHz to 150 MHz<br>All other codes are reserved.<br>Note that, because DSPCLK could be any frequency (within the valid ranges), it is not possible to quote exact frequencies in this field definition. The DSPn Clock must be less than or equal to the DSPCLK frequency. The exact frequency is derived as DSPCLK divided by 1, 2, 4, 8, or 16.                                                                                                                                        |
|                                                                                                                                  | 4     | DSPn_MEM_ENA                      | 0       | DSPn memory control<br>0 = Disabled<br>1 = Enabled<br>The DSPn memory contents are lost when DSPn_MEM_ENA = 0. Note that this bit is not affected by software reset; it remains in its previous condition.                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                                                                                                                                  | 1     | DSPn_CORE_ENA                     | 0       | DSPn enable. Controls the DSPn firmware execution<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                                                                                                                                  | 0     | DSPn_START                        | —       | DSPn start<br>Write 1 to start DSPn firmware execution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Base address +0x06<br>DSPn_Status_2                                                                                              | 31:16 | DSPn_DUALMEM_COLLISION_ADDR[15:0] | 0x0000  | DSPn dual memory collision address. In the event of a DSPn memory access collision, this field reports the address at which the collision occurred. The address is defined relative to the base address of the shared data memory. The LSB represents one 24-bit DSP memory word.<br><b>Note:</b> Valid for DSP2 and DSP3 only.                                                                                                                                                                                                                                                                                                                          |
|                                                                                                                                  | 3:1   | DSPn_CLK_SEL_STS[2:0]             | 000     | DSPn clock frequency (read only). Valid only when the respective DSP Core is enabled.<br>000 = 5.5 MHz to 9.375 MHz<br>001 = 9.375 MHz to 18.75 MHz<br>010 = 18.75 MHz to 37.5 MHz<br>011 = 37.5 MHz to 75 MHz<br>100 = 75 MHz to 150 MHz<br>All other codes are reserved<br>Note that, because DSPCLK could be any frequency (within the valid ranges), it is not possible to quote exact frequencies in this field definition. The exact frequency is derived as DSPCLK divided by 1, 2, 4, 8, or 16.                                                                                                                                                  |
|                                                                                                                                  | 0     | DSPn_CLK_AVAIL                    | 0       | DSPn clock availability (read only)<br>0 = No Clock<br>1 = Clock Available<br>This bit exists for legacy software support only; it is not recommended for future designs—it may be unreliable on the latest device architectures.                                                                                                                                                                                                                                                                                                                                                                                                                        |
| Base address +0x38<br>DSPn_External_Start                                                                                        | 4:0   | DSPn_START_IN_SEL[4:0]            | 0x00    | DSPn firmware execution control. Selects the trigger for DSPn firmware execution.<br>0x00 = DMA                      0x04 = DSP2 Start 2                      0x10 = Event Logger 1<br>0x01 = DSP1 Start 1                      0x05 = DSP3 Start 1                      0x11 = Event Logger 2<br>0x02 = DSP1 Start 2                      0x06 = DSP3 Start 2                      0x12 = Event Logger 3<br>0x03 = DSP2 Start 1                      0x0B = IRQ2                      0x13 = Event Logger 4<br>All other codes are reserved.<br>Note that the DSPn_START bit also starts the DSPn firmware execution, regardless of this field setting. |

#### 4.4.3 DSP Direct Memory Access (DMA) Control

Each DSP provides a multichannel DMA function; this is configured using the registers described in [Table 4-26](#).

There are eight WDMA (DSP input) and six RDMA (DSP output) channels for each DSP; these are enabled using the `DSPn_WDMA_CHANNEL_ENABLE` and `DSPn_RDMA_CHANNEL_ENABLE` fields. The status of each WDMA channel is indicated in `DSPn_WDMA_ACTIVE_CHANNELS`.

The DMA can access the X-data memory or Y-data memory associated with the respective DSP. The applicable memory is selected using bit [15] of the respective `x_START_ADDRESS` field for each DMA channel.

The start address of each DMA channel is configured as described in [Table 4-26](#). Note that the required address is defined relative to the base address of the selected (X-data or Y-data) memory.

The buffer length of the DMA channels is configured using the `DSPn_DMA_BUFFER_LENGTH` field. The selected buffer length applies to all enabled DMA channels.

Note that the start-address fields and buffer-length fields are defined in 24-bit DSP data word units. This means that the LSB of these fields represents one 24-bit DSP memory word. This differs from the CS47L35 register map layout described in [Table 4-23](#).

The parameters of a DMA channel (i.e., start address or offset address) must not be changed while the respective DMA is enabled. All of the DMA channels must be disabled before changing the DMA buffer length.

Each DMA channel uses a twin buffer mechanism to support uninterrupted data flow through the DSP. The buffers are called *ping* and *pong*, and are of configurable size, as noted above. Data is transferred to/from each of the buffers in turn.

When the ping input data buffer is full, the `DSPn_PING_FULL` bit is set, and a DSP start signal is generated. The start signal from the DMA is typically used to start firmware execution, as noted in [Table 4-25](#). Meanwhile, further DSP input data fills up the pong buffer.

When the pong input buffer is full, the `DSPn_PONG_FULL` bit is set, and another DSP start signal is generated. The DSP firmware must take care to read the input data from the applicable buffer, in accordance with the `DSPn_PING_FULL` and `DSPn_PONG_FULL` status bits.

Twin buffers are also used on the DSP output (RDMA) channels. The output ping buffers are emptied at the same time as the input ping buffers are filled; the output pong buffers are emptied at the same time that the input pong buffers are filled.

The DSP cores support 24-bit signal processing. Under default conditions, the DSP audio data is in 2's complement Q3.20 format (i.e., 0xF00000 corresponds to the -1.0 level, and 0x100000 corresponds to the +1.0 level; a sine wave with peak values of  $\pm 1.0$  corresponds to the 0 dBFS level). If `DSPn_DMA_WORD_SEL` is set, audio data is transferred to and from DSP<sub>n</sub> in Q0.23 format. The applicable format should be set according to the requirements of the specific DSP firmware.

Note that the DSP cores are optimized for Q3.20 audio data processing; Q0.23 data can be supported, but the firmware implementation may incur a reduction in power efficiency due to the higher MIPS required for arithmetic operations in non-native data word format.

The DSPCLK system clock must be configured and enabled before any DMA channel is enabled. The DMA channels should be kept disabled (`DSPn_[WDMA/RDMA]_CHANNEL_ENABLE = 0x00`) if DSPCLK is not enabled. See [Section 4.16](#) for details of the system clocks (including requirements for reconfiguring DSPCLK while DMA channels are enabled).

The DMA function is an input to the interrupt control circuit—see [Section 4.4.4](#). The respective interrupt event is triggered if all enabled input (WDMA) channel buffers have been filled and all enabled output (RDMA) channel buffers have been emptied.

Further details of the DMA are provided in the software programming guide; contact your Cirrus Logic representative if required.

**Table 4-26. DMA Control**

| Register Address                                                                                                                 | Bit   | Label                                  | Default | Description                                                                                                                                                                                                                                                                                                                                                                    |
|----------------------------------------------------------------------------------------------------------------------------------|-------|----------------------------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DSP1 Base Address = R1048064 (0x0F_FE00)<br>DSP2 Base Address = R1572352 (0x17_FE00)<br>DSP3 Base Address = R2096640 (0x1F_FE00) |       |                                        |         |                                                                                                                                                                                                                                                                                                                                                                                |
| Base address +0x04<br>DSPn_Status_1                                                                                              | 31    | DSPn_PING_FULL                         | 0       | DSPn WDMA Ping Buffer Status<br>0 = Not Full<br>1 = Full                                                                                                                                                                                                                                                                                                                       |
|                                                                                                                                  | 30    | DSPn_PONG_FULL                         | 0       | DSPn WDMA Pong Buffer Status<br>0 = Not Full<br>1 = Full                                                                                                                                                                                                                                                                                                                       |
|                                                                                                                                  | 23:16 | DSPn_WDMA_ACTIVE_CHANNELS[7:0]         | 0x00    | DSPn WDMA Channel Status<br>There are eight WDMA channels; each bit of this field indicates the status of the respective WDMA channel.<br>Each bit is coded as follows:<br>0 = Inactive<br>1 = Active                                                                                                                                                                          |
| Base address +0x10<br>DSPn_WDMA_Buffer_1                                                                                         | 31:16 | DSPn_START_ADDRESS_WDMA_BUFFER_1[15:0] | 0x0000  | DSPn WDMA Channel 1 Start Address<br>Bit [15] = Memory select<br>0 = X-data memory<br>1 = Y-data memory<br>Bits [14:0] = Address select<br>The address is defined relative to the base address of the applicable data memory. The LSB represents one 24-bit DSP memory word.<br>Note that the start address is also controlled by the respective DSPn_WDMA_CHANNEL_OFFSET bit. |
|                                                                                                                                  | 15:0  | DSPn_START_ADDRESS_WDMA_BUFFER_0[15:0] | 0x0000  | DSPn WDMA Channel 0 Start Address<br>Field description is as above.                                                                                                                                                                                                                                                                                                            |
| Base address +0x12<br>DSPn_WDMA_Buffer_2                                                                                         | 31:16 | DSPn_START_ADDRESS_WDMA_BUFFER_3[15:0] | 0x0000  | DSPn WDMA Channel 3 Start Address<br>Field description is as above.                                                                                                                                                                                                                                                                                                            |
|                                                                                                                                  | 15:0  | DSPn_START_ADDRESS_WDMA_BUFFER_2[15:0] | 0x0000  | DSPn WDMA Channel 2 Start Address<br>Field description is as above.                                                                                                                                                                                                                                                                                                            |
| Base address +0x14<br>DSPn_WDMA_Buffer_3                                                                                         | 31:16 | DSPn_START_ADDRESS_WDMA_BUFFER_5[15:0] | 0x0000  | DSPn WDMA Channel 5 Start Address<br>Field description is as above.                                                                                                                                                                                                                                                                                                            |
|                                                                                                                                  | 15:0  | DSPn_START_ADDRESS_WDMA_BUFFER_4[15:0] | 0x0000  | DSPn WDMA Channel 4 Start Address<br>Field description is as above.                                                                                                                                                                                                                                                                                                            |
| Base address +0x16<br>DSPn_WDMA_Buffer_4                                                                                         | 31:16 | DSPn_START_ADDRESS_WDMA_BUFFER_7[15:0] | 0x0000  | DSPn WDMA Channel 7 Start Address<br>Field description is as above.                                                                                                                                                                                                                                                                                                            |
|                                                                                                                                  | 15:0  | DSPn_START_ADDRESS_WDMA_BUFFER_6[15:0] | 0x0000  | DSPn WDMA Channel 6 Start Address<br>Field description is as above.                                                                                                                                                                                                                                                                                                            |
| Base address +0x20<br>DSPn_RDMA_Buffer_1                                                                                         | 31:16 | DSPn_START_ADDRESS_RDMA_BUFFER_1[15:0] | 0x0000  | DSPn RDMA Channel 1 Start Address<br>Bit [15] = Memory select<br>0 = X-data memory<br>1 = Y-data memory<br>Bits [14:0] = Address select<br>The address is defined relative to the base address of the applicable data memory. The LSB represents one 24-bit DSP memory word.<br>Note that the start address is also controlled by the respective DSPn_RDMA_CHANNEL_OFFSET bit. |
|                                                                                                                                  | 15:0  | DSPn_START_ADDRESS_RDMA_BUFFER_0[15:0] | 0x0000  | DSPn RDMA Channel 0 Start Address<br>Field description is as above.                                                                                                                                                                                                                                                                                                            |
| Base address +0x22<br>DSPn_RDMA_Buffer_2                                                                                         | 31:16 | DSPn_START_ADDRESS_RDMA_BUFFER_3[15:0] | 0x0000  | DSPn RDMA Channel 3 Start Address<br>Field description is as above.                                                                                                                                                                                                                                                                                                            |
|                                                                                                                                  | 15:0  | DSPn_START_ADDRESS_RDMA_BUFFER_2[15:0] | 0x0000  | DSPn RDMA Channel 2 Start Address<br>Field description is as above.                                                                                                                                                                                                                                                                                                            |

**Table 4-26. DMA Control (Cont.)**

| Register Address                         | Bit   | Label                                  | Default | Description                                                                                                                                                                                                                                |
|------------------------------------------|-------|----------------------------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Base address +0x24<br>DSPn_RDMA_Buffer_3 | 31:16 | DSPn_START_ADDRESS_RDMA_BUFFER_5[15:0] | 0x0000  | DSPn RDMA Channel 5 Start Address<br>Field description is as above.                                                                                                                                                                        |
|                                          | 15:0  | DSPn_START_ADDRESS_RDMA_BUFFER_4[15:0] | 0x0000  | DSPn RDMA Channel 4 Start Address<br>Field description is as above.                                                                                                                                                                        |
| Base address +0x30<br>DSPn_DMA_Config_1  | 23:16 | DSPn_WDMA_CHANNEL_ENABLE[7:0]          | 0x00    | DSPn WDMA Channel Enable<br>There are eight WDMA channels; each bit of this field enables the respective WDMA channel.<br>Each bit is coded as follows:<br>0 = Disabled<br>1 = Enabled                                                     |
|                                          | 13:0  | DSPn_DMA_BUFFER_LENGTH[13:0]           | 0x0000  | DSPn DMA Buffer Length<br>Selects the amount of data transferred in each DMA channel. The LSB represents one 24-bit DSP memory word.                                                                                                       |
| Base address +0x32<br>DSPn_DMA_Config_2  | 7:0   | DSPn_WDMA_CHANNEL_OFFSET[7:0]          | 0x00    | DSPn WDMA Channel Offset<br>There are eight WDMA channels; each bit of this field offsets the start Address of the respective WDMA channel.<br>Each bit is coded as follows:<br>0 = No offset<br>1 = Offset by 0x8000                      |
| Base address +0x34<br>DSPn_DMA_Config_3  | 21:16 | DSPn_RDMA_CHANNEL_OFFSET[5:0]          | 0x00    | DSPn RDMA Channel Offset<br>There are six RDMA channels; each bit of this field offsets the start Address of the respective RDMA channel.<br>Each bit is coded as follows:<br>0 = No offset<br>1 = Offset by 0x8000                        |
|                                          | 5:0   | DSPn_RDMA_CHANNEL_ENABLE[5:0]          | 0x00    | DSPn RDMA Channel Enable<br>There are six RDMA channels; each bit of this field enables the respective RDMA channel.<br>Each bit is coded as follows:<br>0 = Disabled<br>1 = Enabled                                                       |
| Base address +0x36<br>DSPn_DMA_Config_4  | 0     | DSPn_DMA_WORD_SEL                      | 0       | DSPn Data Word Format<br>0 = Q3.20 format (4 integer bits, 20 fractional bits)<br>1 = Q0.23 format (1 integer bit, 23 fractional bits)<br>The data word format should be set according to the requirements of the applicable DSP firmware. |

#### 4.4.4 DSP Interrupts

The DSP cores provide inputs to the interrupt circuit and can be used to trigger an interrupt event when the associated conditions occur. For each DSP, the following interrupts are provided:

- DMA interrupt—Asserted when all enabled DSP input (WDMA) channel buffers have been filled, and all enabled DSP output (RDMA) channel buffers have been emptied
- DSP Start 1, DSP Start 2 interrupts—Asserted when the respective start signal is triggered
- DSP Busy interrupt—Asserted when the DSP is busy (i.e., when firmware execution or DMA processes are started)

The CS47L35 also provides 16 control bits that allow the DSP cores to generate programmable interrupt events. When a 1 is written to these bits (see [Table 4-27](#)), the respective DSP interrupt (DSP\_IRQn\_EINTx) is triggered. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal.

See [Section 4.15](#) for further details.

**Table 4-27. DSP Interrupts**

| Register Address | Bit | Label     | Default | Description                                                  |
|------------------|-----|-----------|---------|--------------------------------------------------------------|
| R5632 (0x1600)   | 1   | DSP_IRQ2  | 0       | DSP IRQ2. Write 1 to trigger the DSP_IRQ2_EINTn interrupt.   |
| ADSP2_IRQ0       | 0   | DSP_IRQ1  | 0       | DSP IRQ1. Write 1 to trigger the DSP_IRQ1_EINTn interrupt.   |
| R5633 (0x1601)   | 1   | DSP_IRQ4  | 0       | DSP IRQ4. Write 1 to trigger the DSP_IRQ4_EINTn interrupt.   |
| ADSP2_IRQ1       | 0   | DSP_IRQ3  | 0       | DSP IRQ3. Write 1 to trigger the DSP_IRQ3_EINTn interrupt.   |
| R5634 (0x1602)   | 1   | DSP_IRQ6  | 0       | DSP IRQ6. Write 1 to trigger the DSP_IRQ6_EINTn interrupt.   |
| ADSP2_IRQ2       | 0   | DSP_IRQ5  | 0       | DSP IRQ5. Write 1 to trigger the DSP_IRQ5_EINTn interrupt.   |
| R5635 (0x1603)   | 1   | DSP_IRQ8  | 0       | DSP IRQ8. Write 1 to trigger the DSP_IRQ8_EINTn interrupt.   |
| ADSP2_IRQ3       | 0   | DSP_IRQ7  | 0       | DSP IRQ7. Write 1 to trigger the DSP_IRQ7_EINTn interrupt.   |
| R5636 (0x1604)   | 1   | DSP_IRQ10 | 0       | DSP IRQ10. Write 1 to trigger the DSP_IRQ10_EINTn interrupt. |
| ADSP2_IRQ4       | 0   | DSP_IRQ9  | 0       | DSP IRQ9. Write 1 to trigger the DSP_IRQ9_EINTn interrupt.   |
| R5637 (0x1605)   | 1   | DSP_IRQ12 | 0       | DSP IRQ12. Write 1 to trigger the DSP_IRQ12_EINTn interrupt. |
| ADSP2_IRQ5       | 0   | DSP_IRQ11 | 0       | DSP IRQ11. Write 1 to trigger the DSP_IRQ11_EINTn interrupt. |
| R5638 (0x1606)   | 1   | DSP_IRQ14 | 0       | DSP IRQ14. Write 1 to trigger the DSP_IRQ14_EINTn interrupt. |
| ADSP2_IRQ6       | 0   | DSP_IRQ13 | 0       | DSP IRQ13. Write 1 to trigger the DSP_IRQ13_EINTn interrupt. |
| R5639 (0x1607)   | 1   | DSP_IRQ16 | 0       | DSP IRQ16. Write 1 to trigger the DSP_IRQ16_EINTn interrupt. |
| ADSP2_IRQ7       | 0   | DSP_IRQ15 | 0       | DSP IRQ15. Write 1 to trigger the DSP_IRQ15_EINTn interrupt. |

### 4.4.5 DSP Debug Support

General-purpose registers are provided for each DSP. These have no assigned function and can be used to assist in algorithm development.

The JTAG interface provides test and debug access to the CS47L35, as described in [Section 4.20](#). The JTAG interface clock can be enabled independently for each DSP core using the DSPn\_DBG\_CLK\_ENA bits. Note that, when the JTAG interface is used to access any DSP core, the respective DSPn\_CORE\_ENA bit must also be set.

**Table 4-28. DSP Debug Support**

| Register Address                                                                                                                 | Bit           | Label                                        | Default          | Description                                            |
|----------------------------------------------------------------------------------------------------------------------------------|---------------|----------------------------------------------|------------------|--------------------------------------------------------|
| DSP1 Base Address = R1048064 (0x0F_FE00)<br>DSP2 Base Address = R1572352 (0x17_FE00)<br>DSP3 Base Address = R2096640 (0x1F_FE00) |               |                                              |                  |                                                        |
| Base address<br>DSPn_Config_1                                                                                                    | 3             | DSPn_DBG_CLK_ENA                             | 0                | DSPn Debug Clock Enable<br>0 = Disabled<br>1 = Enabled |
| Base address +0x40<br>DSPn_Scratch_1                                                                                             | 31:16<br>15:0 | DSPn_SCRATCH_1[15:0]<br>DSPn_SCRATCH_0[15:0] | 0x0000<br>0x0000 | DSPn Scratch Register 1<br>DSPn Scratch Register 0     |
| Base address +0x42<br>DSPn_Scratch_2                                                                                             | 31:16<br>15:0 | DSPn_SCRATCH_3[15:0]<br>DSPn_SCRATCH_2[15:0] | 0x0000<br>0x0000 | DSPn Scratch Register 3<br>DSPn Scratch Register 2     |

### 4.4.6 Virtual DSP Registers

The DSP control registers, described throughout [Section 4.4](#) are implemented for each DSP core. Each control register has a unique location within the CS47L35 register map.

An additional set of DSP control registers is also defined, which can be used in firmware to access any of the DSPs: the virtual DSP (or DSP 0) registers are defined at address R4096 (0x1000) in the device register map. The full register map listing is provided in [Section 6](#).

Note that read/write access to the virtual DSP registers is only possible via firmware running on the integrated DSP cores. When DSP firmware accesses the virtual registers, the registers are automatically mapped onto the control registers corresponding to whichever DSP core is making the read/write access. For example, if DSP1 accesses these registers, they are mapped onto the DSP1 control registers. If DSP2 accesses the virtual registers, they are mapped onto the DSP2 control registers.

The virtual DSP registers are designed to allow software to be transferable to any of the DSPs without modification to the software code.

The virtual DSP registers are defined at register addresses R4096–R4192 (0x1000–0x1060) in the device register map. Note that these registers cannot be accessed directly at the addresses shown; they can be only accessed through DSP firmware code, using the register window function shown in [Fig. 4-28](#). The virtual DSP registers are located at address 0xD000 in the X-data memory map.

## 4.5 DSP Peripheral Control

The CS47L35 incorporates a suite of DSP peripheral functions that can be integrated together to support the sensor-hub capability. A master I<sup>2</sup>C interface is provided for external sensor connectivity. Configurable event log functions provide multichannel monitoring of internal and external signals. The general-purpose timers provide time-stamp data for the event logs and support watchdog and other miscellaneous time-based functions. Maskable GPIO provides an efficient mechanism for multiple DSPs to access the respective input and output signals.

The DSP peripherals are designed to provide a comprehensive sensor-hub capability, operating with a high degree of autonomy from the host processor.

### 4.5.1 Master Interface (MIF)

The CS47L35 incorporates an I<sup>2</sup>C master interface, offering a flexible capability for additional sensor/accessory input.

#### 4.5.1.1 Overview

The master interface (MIF1) can support single- and multiple-master I<sup>2</sup>C operation up to 1 MHz. The master interface supports 7- and 10-bit slave addressing modes. Master device arbitration algorithms are implemented, in accordance with the standard I<sup>2</sup>C protocol. A watchdog timer is provided for detecting interface error conditions.

The master interface is ideally suited for connection to external sensors such as accelerometers, gyroscopes, and magnetometers for motion-sensing and navigation applications. Other example accessories include barometers, and ambient light sensors, for environmental awareness. Flow-control bits for the TX and RX data buffers enable easy integration with external devices and with internal DSP functions.

#### 4.5.1.2 Clocking Configuration

Clocking for the master interface is derived from DSPCLK, which must be enabled and present when using the MIF function. Standard I<sup>2</sup>C bus rates can be supported for typical DSPCLK frequencies using the register settings described in [Table 4-29](#).

**Table 4-29. Master Interface Clock Configuration**

| Register Address  | Condition                     | Value       |
|-------------------|-------------------------------|-------------|
| R262144 (0x40000) | —                             | 0x0000_0006 |
| R262208 (0x40040) | —                             | 0x0000_0000 |
| R262210 (0x40042) | 10 kHz I <sup>2</sup> C Mode  | 0x01CC_01CC |
|                   | 100 kHz I <sup>2</sup> C Mode | 0x002E_002E |
|                   | 400 kHz I <sup>2</sup> C Mode | 0x000C_000C |
|                   | 1 MHz I <sup>2</sup> C Mode   | 0x0005_0005 |

**Note:** It is assumed that the DSPCLK frequency is one of the nominal (typical) frequencies specified in [Table 4-93](#).

The DSPCLK system clock must be configured and enabled before a Master Interface transaction is scheduled. The Master Interfaces should be kept idle if DSPCLK is not enabled. See [Section 4.16](#) for details of the system clocks (including requirements for reconfiguring DSPCLK while DSP peripherals are enabled).

#### 4.5.1.3 Transmit and Receive Data Buffers

The transmit (master write) and receive (master read) actions are each supported by 16-byte data buffers, allowing I<sup>2</sup>C transfers of up to 2,097,152 data bytes (2 MB). The number of data bytes transferred in each I<sup>2</sup>C operation is selected using MIF1\_TX\_LENGTH or MIF1\_RX\_LENGTH.

Data to be transmitted is managed using the TX data buffers; the application software must load data into the buffer registers (MIF1\_TX\_BYTE<sub>n</sub>) and then write 1 to the MIF1\_TX\_DONE bit to commit that data for transmission. The MIF1\_TX\_REQUEST bit indicates when the buffer registers are ready for loading new data. Internal buffering of the TX data enables uninterrupted I<sup>2</sup>C writes. If new data is not ready for transmission, SCLK halts until the buffer registers have been filled.

Data received on the interface is managed using the RX data buffers; the MIF1\_RX\_REQUEST bit indicates when the buffer registers contain new data. The application software must read the buffer registers (MIF1\_RX\_BYTE<sub>n</sub>), and then write 1 to the MIF1\_RX\_DONE bit to confirm the data has been read. Internal buffering of the RX data enables uninterrupted I<sup>2</sup>C reads. If the buffers are not ready to receive new data, SCLK halts until the buffer registers have been read.

The master interface divides each I<sup>2</sup>C transaction into one or more data blocks. The block length is configurable using the MIF1\_TX\_BLOCK\_LENGTH and MIF1\_RX\_BLOCK\_LENGTH fields. The block length is equal to the number of bytes transmitted/received for each TX\_DONE/RX\_DONE action. The maximum block length is 16 bytes, corresponding to the size of the TX and RX data buffers.

**Note:** The order in which the data bytes in the TX/RX buffers are transferred depends on the selected MIF1\_WORD\_SIZE setting. Correct setting of the word size ensures that each data word is transmitted/received most-significant byte first.

The Master Interface is configured for Read (RX) or Write (TX) operation using the MIF1\_READ\_WRITE\_SEL bit. Each I<sup>2</sup>C transfer is started by writing 1 to the MIF1\_START bit. In the case of a Master Write, data must be committed to the TX data buffers using the TX\_DONE bit, to enable the transfer to proceed—note that the first block of transmit data can be committed to the TX buffers before or after writing to the START bit for the respective transfer.

#### 4.5.1.4 Interrupts and Status Bits

The MIF1\_BUSY\_STS bit indicates when the master interface is executing an I<sup>2</sup>C transaction. This bit is set during each I<sup>2</sup>C transaction, and cleared on completion. An interrupt event is also triggered on completion of the I<sup>2</sup>C transfer, if the corresponding MIF1\_DONE\_EINT<sub>x</sub> is unmasked as an input to the IRQ circuit.

Additional status bits are provided to indicate watchdog timeout, loss of bus arbitration, or a NACK error signal received. [Table 4-30](#) describes these bits.

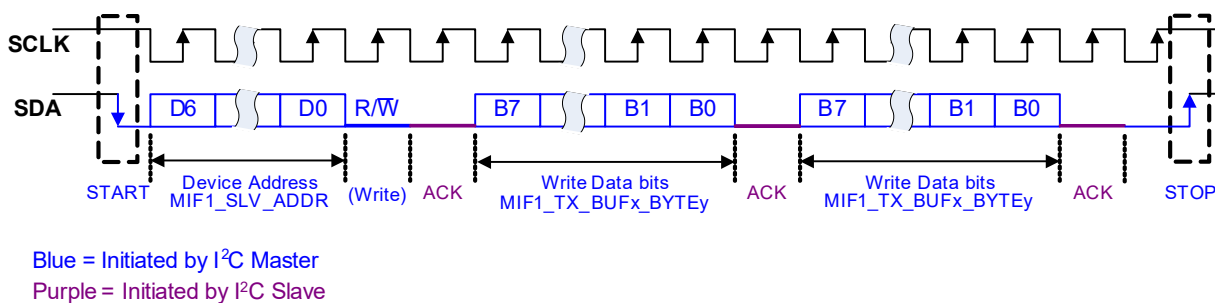
Note that the MIF done indication is asserted each time an I<sup>2</sup>C transfer completes, including when an error condition has occurred. It is recommended that the master interface status bits be checked after each I<sup>2</sup>C transaction, so corrective action can be taken when necessary.

The master interface provides inputs to the interrupt control circuit. An interrupt event is triggered on completion of each TX/RX block, and on completion of the I<sup>2</sup>C transaction; see [Section 4.15](#).

#### 4.5.1.5 External Connections

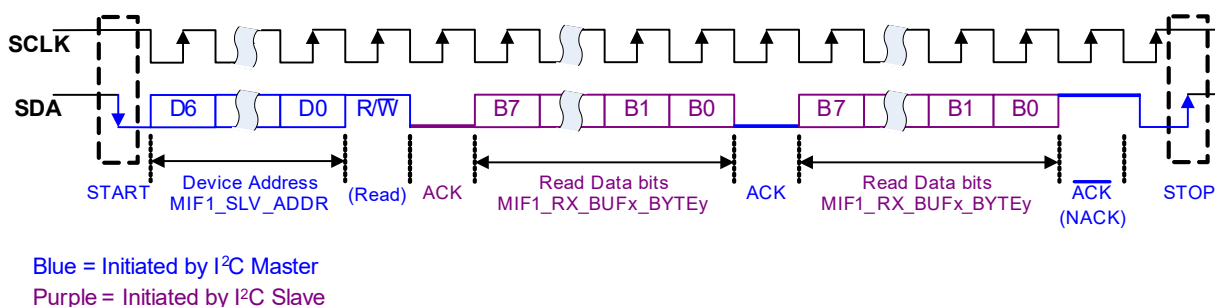
The external connections associated with the I<sup>2</sup>C master interface (MIF) are implemented on multi-function GPIO pins, which must be configured for the respective MIF functions when required. The MIF1SCLK and MIF1SDA connections are pin-specific alternative functions available on specific GPIO pins only. See [Section 4.14](#) to configure the GPIO pins for the MIF operation.

Fig. 4-29 shows a typical master I<sup>2</sup>C write transfer.



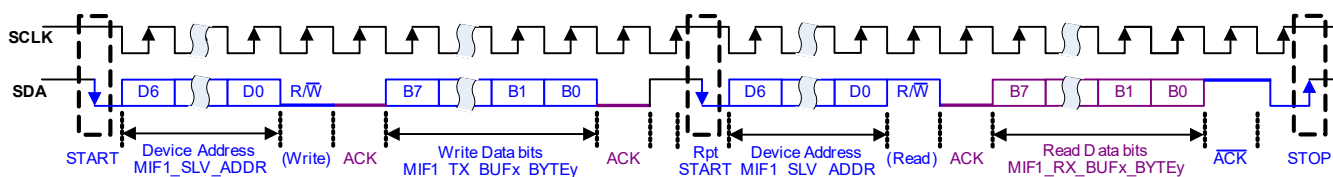
**Figure 4-29. Master I<sup>2</sup>C Write**

Fig. 4-30 shows a typical master I<sup>2</sup>C read transfer.



**Figure 4-30. Master I<sup>2</sup>C Read**

Fig. 4-31 shows a typical master I<sup>2</sup>C write/read transfer; the read transaction is preceded by a repeated start.



**Figure 4-31. Master I<sup>2</sup>C Write and Read**

#### 4.5.1.6 Master Interface Control Registers

The MIF control registers are described in [Table 4-30](#).

**Table 4-30. Master Interface (MIF1) Control**

| Register Address                       | Bit  | Label              | Default | Description                                                                                             |
|----------------------------------------|------|--------------------|---------|---------------------------------------------------------------------------------------------------------|
| R262146 (0x40002)<br>MIF1_I2C_CONFIG_2 | 10:1 | MIF1_SLV_ADDR[9:0] | 0x000   | Address of Slave on which transactions are executed.<br>For 7-Bit Mode, lower 7 bits of field are used. |
|                                        | 0    | MIF1_ADDR_MODE     | 0       | Selects the addressing mode of I <sup>2</sup> C Master<br>0 = 7-Bit Mode<br>1 = 10-Bit Mode             |

**Table 4-30. Master Interface (MIF1) Control (Cont.)**

| Register Address                       | Bit   | Label                | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|----------------------------------------|-------|----------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R262148 (0x40004)<br>MIF1_I2C_CONFIG_3 | 3     | MIF1_NACK_RESPONSE   | 0       | Selects the action taken if NACK is received from Slave.<br>0 = Stop Condition sent.<br>1 = Stop Condition not sent; next transaction commences with a Repeated Start.<br><br>Note that, if the Stop Condition is not sent, the master retains control of the bus until a subsequent action is scheduled. The next transaction commences with a Repeated Start in this case.                                                                                                                                                                                                                         |
|                                        | 2     | MIF1_SCL_MON_ENA     | 1       | Enables bus monitoring functions on SCLK<br>0 = Disabled<br>1 = Enabled<br><br>This feature enables support for clock stretching by slave devices, and enables bus synchronization as part of multimaster operation.                                                                                                                                                                                                                                                                                                                                                                                 |
|                                        | 1     | MIF1_RPT_START       | 0       | Selects the action taken on completion of a bus transaction.<br>0 = Stop Condition sent.<br>1 = Stop Condition not sent; next transaction commences with a Repeated Start.<br><br>Note that, if the Stop Condition is not sent, the master retains control of the bus until a subsequent action is scheduled. The next transaction commences with a Repeated Start in this case.                                                                                                                                                                                                                     |
|                                        | 0     | MIF1_START_BYTE_ENA  | 0       | Selects whether a Start Byte is transmitted before an I <sup>2</sup> C transaction.<br>0 = Disabled<br>1 = Enabled<br><br>The Start Byte is a dummy transaction that provides support for bus devices that use low-frequency polling to detect I <sup>2</sup> C activity. The Start Byte, when enabled, is transmitted before the Slave Address bytes. It is not acknowledged on the bus by any device.                                                                                                                                                                                              |
| R262152 (0x40008)<br>MIF1_I2C_CONFIG_5 | 0     | MIF1_WDT_ENA         | 0       | Watchdog Timer (WDT) control<br>0 = Disabled<br>1 = Enabled<br><br>When bus monitoring functions are enabled (MIF1_SCL_MON_ENA = 1), the watchdog timer is used to detect the SCLK line being pulled low for a prolonged duration.                                                                                                                                                                                                                                                                                                                                                                   |
| R262272 (0x40080)<br>MIF1_I2C_STATUS_1 | 2     | MIF1_WDT_TIMEOUT_STS | 0       | Watchdog Timer (WDT) Error Status. This bit, when set, indicates that the WDT expired during the I <sup>2</sup> C transaction.<br>This bit is latched when set; it is only cleared on next I <sup>2</sup> C transaction.                                                                                                                                                                                                                                                                                                                                                                             |
|                                        | 1     | MIF1_ARBIT_LOST_STS  | 0       | Arbitration Error Status. This bit, when set, indicates that arbitration was lost during the I <sup>2</sup> C transaction.<br>This bit is latched when set; it is only cleared on next I <sup>2</sup> C transaction.                                                                                                                                                                                                                                                                                                                                                                                 |
|                                        | 0     | MIF1_NACK_STS        | 0       | NACK Error Status. This bit, when set, indicates that a NACK Error signal was received during the I <sup>2</sup> C transaction.<br>This bit is latched when set; it is only cleared on next I <sup>2</sup> C transaction.                                                                                                                                                                                                                                                                                                                                                                            |
| R262400 (0x40100)<br>MIF1_CONFIG_1     | 0     | MIF1_START           | 0       | Starts the I <sup>2</sup> C transaction<br>Write 1 to start.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| R262404 (0x40104)<br>MIF1_CONFIG_3     | 17:16 | MIF1_WORD_SIZE[1:0]  | 00      | Selects the data word format. I <sup>2</sup> C transactions are made up of 1-Byte data words; the sequence order of these words differs according to the applicable word format.<br>Correct setting of the MIF1_WORD_SIZE field ensures that each data word is transmitted/received as MSB first.<br>00 = 8-bit (1, 2, 3, 4, 5, 6, 7, 8, etc)<br>01 = 16-bit (2, 1, 4, 3, 6, 5, 8, 7, etc)<br>10 = 32-bit (4, 3, 2, 1, 8, 7, 6, 5, etc)<br><br>The bracketed numbers describe the order in which applicable MIF1_[TX]RX[_BYTE]x fields are transmitted/received over the I <sup>2</sup> C interface. |
|                                        | 0     | MIF1_READ_WRITE_SEL  | 0       | Selects the I <sup>2</sup> C Command type<br>0 = Master Write<br>1 = Master Read                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

**Table 4-30. Master Interface (MIF1) Control (Cont.)**

| Register Address                   | Bit   | Label                     | Default   | Description                                                                                                                                                                                                                                                                                                             |
|------------------------------------|-------|---------------------------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R262406 (0x40106)<br>MIF1_CONFIG_4 | 20:0  | MIF1_TX_LENGTH[20:0]      | 0x00_0000 | Selects the total number of data bytes in an I <sup>2</sup> C Write operation.<br>0x00_0000 = 1 byte<br>0x00_0001 = 2 bytes<br>0x00_0002 = 3 bytes<br>...<br>0x1F_FFFF = 2,097,152 bytes                                                                                                                                |
| R262416 (0x40110)<br>MIF1_CONFIG_5 | 20:0  | MIF1_RX_LENGTH[20:0]      | 0x00_0000 | Selects the total number of data bytes in an I <sup>2</sup> C Read operation.<br>0x00_0000 = 1 byte<br>0x00_0001 = 2 bytes<br>0x00_0002 = 3 bytes<br>...<br>0x1F_FFFF = 2,097,152 bytes                                                                                                                                 |
| R262418 (0x40112)<br>MIF1_CONFIG_6 | 7:0   | MIF1_TX_BLOCK_LENGTH[7:0] | 0x10      | Selects the interval at which the MIF1_BLOCK Interrupt is triggered during I <sup>2</sup> C Write operations.<br>0x00 = 1 byte<br>0x01 = 1 byte<br>0x02 = 2 bytes<br>...<br>0x10 = 16 bytes<br>All other codes are reserved                                                                                             |
| R262420 (0x40114)<br>MIF1_CONFIG_7 | 7:0   | MIF1_RX_BLOCK_LENGTH[7:0] | 0x10      | Selects the interval at which the MIF1_BLOCK Interrupt is triggered during I <sup>2</sup> C Read operations.<br>0x00 = 1 byte<br>0x01 = 1 byte<br>0x02 = 2 bytes<br>...<br>0x10 = 16 bytes<br>All other codes are reserved                                                                                              |
| R262422 (0x40116)<br>MIF1_CONFIG_8 | 4     | MIF1_RX_DONE              | 0         | RX Buffer access control bit. Write 1 to indicate that data in the RX Buffer has been read.<br>In normal operation, a 1 is written after reading the RX buffer. This causes the MIF1_RX_REQUEST bit to be cleared. (Note that, if further data is available to read, the MIF1_RX_REQUEST bit remains set in this case.) |
|                                    | 0     | MIF1_TX_DONE              | 0         | TX Buffer access control bit. Write 1 to indicate the TX Buffer has been filled with data for transmission.<br>In normal operation, a 1 is written after writing the TX buffer. This causes the MIF1_TX_REQUEST bit to be cleared.                                                                                      |
| R262528 (0x40180)<br>MIF1_STATUS_1 | 8     | MIF1_BUSY_STS             | 0         | MIF Busy Status.<br>This bit, when set, indicates that the master interface is executing an I <sup>2</sup> C transaction.                                                                                                                                                                                               |
|                                    | 8     | MIF1_RX_REQUEST           | 0         | RX Buffer flow control bit<br>0 = No data available to read<br>1 = Buffer data is available to read                                                                                                                                                                                                                     |
|                                    | 1     | MIF1_TX_REQUEST           | 0         | TX Buffer flow control bit<br>0 = TX buffer not available to write<br>1 = TX buffer is available to write                                                                                                                                                                                                               |
| R262530 (0x40182)<br>MIF1_STATUS_2 | 20:0  | MIF1_BYTE_COUNT[20:0]     | 0x00_0000 | Number of data bytes transferred in current transaction.<br>Note that this field is cleared on completion of the I <sup>2</sup> C transaction.                                                                                                                                                                          |
| R262656 (0x40200)<br>MIF1_TX_1     | 31:24 | MIF1_TX_BYTE4[7:0]        | 0x00      | TX Byte 4                                                                                                                                                                                                                                                                                                               |
|                                    | 23:16 | MIF1_TX_BYTE3[7:0]        | 0x00      | TX Byte 3                                                                                                                                                                                                                                                                                                               |
|                                    | 15:8  | MIF1_TX_BYTE2[7:0]        | 0x00      | TX Byte 2                                                                                                                                                                                                                                                                                                               |
|                                    | 7:0   | MIF1_TX_BYTE1[7:0]        | 0x00      | TX Byte 1                                                                                                                                                                                                                                                                                                               |
| R262658 (0x40202)<br>MIF1_TX_2     | 31:24 | MIF1_TX_BYTE8[7:0]        | 0x00      | TX Byte 8                                                                                                                                                                                                                                                                                                               |
|                                    | 23:16 | MIF1_TX_BYTE7[7:0]        | 0x00      | TX Byte 7                                                                                                                                                                                                                                                                                                               |
|                                    | 15:8  | MIF1_TX_BYTE6[7:0]        | 0x00      | TX Byte 6                                                                                                                                                                                                                                                                                                               |
|                                    | 7:0   | MIF1_TX_BYTE5[7:0]        | 0x00      | TX Byte 5                                                                                                                                                                                                                                                                                                               |

**Table 4-30. Master Interface (MIF1) Control (Cont.)**

| Register Address               | Bit   | Label               | Default | Description |
|--------------------------------|-------|---------------------|---------|-------------|
| R262660 (0x40204)<br>MIF1_TX_3 | 31:24 | MIF1_TX_BYTE12[7:0] | 0x00    | TX Byte 12  |
|                                | 23:16 | MIF1_TX_BYTE11[7:0] | 0x00    | TX Byte 11  |
|                                | 15:8  | MIF1_TX_BYTE10[7:0] | 0x00    | TX Byte 10  |
|                                | 7:0   | MIF1_TX_BYTE9[7:0]  | 0x00    | TX Byte 9   |
| R262662 (0x40206)<br>MIF1_TX_4 | 31:24 | MIF1_TX_BYTE16[7:0] | 0x00    | TX Byte 16  |
|                                | 23:16 | MIF1_TX_BYTE15[7:0] | 0x00    | TX Byte 15  |
|                                | 15:8  | MIF1_TX_BYTE14[7:0] | 0x00    | TX Byte 14  |
|                                | 7:0   | MIF1_TX_BYTE13[7:0] | 0x00    | TX Byte 13  |
| R262912 (0x40300)<br>MIF1_RX_1 | 31:24 | MIF1_RX_BYTE4[7:0]  | 0x00    | RX Byte 4   |
|                                | 23:16 | MIF1_RX_BYTE3[7:0]  | 0x00    | RX Byte 3   |
|                                | 15:8  | MIF1_RX_BYTE2[7:0]  | 0x00    | RX Byte 2   |
|                                | 7:0   | MIF1_RX_BYTE1[7:0]  | 0x00    | RX Byte 1   |
| R262914 (0x40302)<br>MIF1_RX_2 | 31:24 | MIF1_RX_BYTE8[7:0]  | 0x00    | RX Byte 8   |
|                                | 23:16 | MIF1_RX_BYTE7[7:0]  | 0x00    | RX Byte 7   |
|                                | 15:8  | MIF1_RX_BYTE6[7:0]  | 0x00    | RX Byte 6   |
|                                | 7:0   | MIF1_RX_BYTE5[7:0]  | 0x00    | RX Byte 5   |
| R262916 (0x40304)<br>MIF1_RX_3 | 31:24 | MIF1_RX_BYTE12[7:0] | 0x00    | RX Byte 12  |
|                                | 23:16 | MIF1_RX_BYTE11[7:0] | 0x00    | RX Byte 11  |
|                                | 15:8  | MIF1_RX_BYTE10[7:0] | 0x00    | RX Byte 10  |
|                                | 7:0   | MIF1_RX_BYTE9[7:0]  | 0x00    | RX Byte 9   |
| R262918 (0x40306)<br>MIF1_RX_4 | 31:24 | MIF1_RX_BYTE16[7:0] | 0x00    | RX Byte 16  |
|                                | 23:16 | MIF1_RX_BYTE15[7:0] | 0x00    | RX Byte 15  |
|                                | 15:8  | MIF1_RX_BYTE14[7:0] | 0x00    | RX Byte 14  |
|                                | 7:0   | MIF1_RX_BYTE13[7:0] | 0x00    | RX Byte 13  |

## 4.5.2 Event Loggers

The CS47L35 provides four event log functions, supporting multichannel, edge-sensitive monitoring and recording of internal or external signals.

### 4.5.2.1 Overview

The event loggers allow status information to be captured from a large number of sources, to be prioritized and acted upon as required. For the purposes of the event loggers, an event is recorded when a logic transition (edge) is detected on a selected signal source.

The logged events are held in a FIFO buffer, which is managed by the application software. A 32-bit time stamp, derived from one of the general-purpose timers, is associated and recorded with each FIFO index, to provide a comprehensive record of the detected events.

Each event logger must be associated with one of the general-purpose timers. The selected timer is the source of time stamp data for any logged events. If DSPCLK is disabled, the timer also provides the clock source for the event logger. (If DSPCLK is enabled, DSPCLK is used as the clock source instead.)

A maximum of one event per cycle of the clock source can be logged. If more than one event occurs within the cycle time, the highest priority (lowest channel number) event is logged at the rising edge of the clock. In this case, any lower priority events is queued, and is logged as soon as no higher priority events are pending. It is possible for recurring events on a high-priority channel to be logged, while low-priority ones remain queued. Note that recurring instances of events that are queued would not be logged.

The event logger can use a slow clock (e.g., 32 kHz), but higher clock frequencies may also be commonly used, depending on the application and use case. The clock frequency determines the maximum possible event logging rate.

### 4.5.2.2 Event Logger Control

The event logger is enabled by setting EVENTLOG $_n$ \_ENA (where  $n$  identifies the respective event logger, 1–4).

The event logger can be reset by writing 1 to `EVENTLOGn_RST`. Executing this function clears all the event logger status flags and clears the contents of the FIFO buffer.

The associated timer (and time-stamp source) is selected using `EVENTLOGn_TIME_SEL`. Note that the event logger must be disabled (`EVENTLOGn_ENA = 0`) when selecting the timer source.

#### 4.5.2.3 Input Channel Configuration

The event logger allows up to 16 input channels to be configured for detection and logging. The `EVENTLOGn_CHx_SEL` field selects the applicable input source for each channel (where *x* identifies the channel number, 1 to 16). The polarity selection and debounce options are configured using the `EVENTLOGn_CHx_POL` and `EVENTLOGn_CHx_DB` bits respectively.

The input channels can be enabled or disabled freely, using `EVENTLOGn_CHx_ENA`, without having to disable the event logger entirely. An input channel must be disabled whenever the associated `x_SEL`, `x_POL`, or `x_DB` fields are written. It is possible to reconfigure input channels while the event logger is enabled, provided the channels being reconfigured are disabled when doing so.

The available input sources include GPIO inputs, external accessory status (jack, mic, sensors), and signals generated by the integrated DSP cores. A list of the valid input sources for the event loggers is provided in [Table 4-32](#). Note that, to log both rising and falling events from any source, two separate input channels must be configured—one for each polarity.

If an input channel is configured for rising edge detection (`EVENTLOGn_CHx_POL = 0`), and the corresponding input signal is asserted (Logic 1) at the time when the event logger is enabled, an event is logged in respect of this initial state. Similarly, if an input channel is configured for falling edge detection, and is deasserted (Logic 0) when the event logger is enabled, a corresponding event is logged. If rising and falling edges are both configured for detection, an event is always logged in respect of the initial condition.

#### 4.5.2.4 FIFO Buffer

Each event (signal transition) that meets the criteria of an enabled channel is written to the 16-stage FIFO buffer. The buffer is filled cyclically, but does not overwrite unread data when full. An error condition occurs if the buffer fills up completely.

Note that the FIFO behavior is not enforced or fully implemented in the device hardware, but assumes that a compatible software implementation is in place. New events are written to the buffer in a cyclic manner, but the data can be read out in any order, if desired. The designed FIFO behavior requires the software to update the read pointer (RPTR) in the intended manner for smooth operation.

The entire contents of the 16-stage FIFO buffer can be accessed directly in the register map. Each FIFO index (*y* = 0 to 15) comprises the `EVENTLOGn_FIFOy_ID` (identifying the source signal of the associated log event), the `EVENTLOGn_FIFOy_POL` (the polarity of the respective event transition), and the `EVENTLOGn_FIFOy_TIME` field (containing the 32-bit time stamp from the associated timer).

The FIFO buffer is managed using `EVENTLOGn_FIFO_WPTR` and `EVENTLOGn_FIFO_RPTR`. The write pointer (WPTR) field identifies the index location (0 to 15) in which the next event is logged. The read pointer (RPTR) field identifies the index location of the first set of unread data, if any exists. Both of these fields are initialized to 0 when the event logger is reset.

- If `RPTR ≠ WPTR`, the buffer contains new data. The number of new events is equal to the difference between the two pointer values (`WPTR – RPTR`, allowing for wraparound beyond Index 15). For example, if `WPTR = 12` and `RPTR = 8`, this means that there are four unread data sets in the buffer, at index locations 8, 9, 10, and 11.  
After reading the new data from the buffer, the `RPTR` value should be incremented by the corresponding amount (e.g., increment by 4, in the example described above). Note that the `RPTR` value can either be incremented once for each read, or can be incremented in larger steps after a batch read.
- If `RPTR = WPTR`, the buffer is either empty (0 events) or full (16 events). In this case, the status bits described in [Section 4.5.2.5](#) confirm the current status of the buffer.

#### 4.5.2.5 Status Bits

The EVENTLOG $n$ \_NOT\_EMPTY bit indicates whether the FIFO buffer is empty. When this bit is set, it indicates one or more new sets of data in the FIFO.

The EVENTLOG $n$ \_WMARK\_STS bit indicates when the number of FIFO index locations available for new events reaches a configurable threshold, known as the watermark level. The watermark level is held in the EVENTLOG $n$ \_FIFO\_WMARK field.

The EVENTLOG $n$ \_FULL bit indicates when the FIFO buffer is full. When this bit is set, it indicates that there are 16 sets of new event data in the FIFO. Note that this does not mean that a buffer overflow condition has occurred, but further events are not logged or indicated until the buffer has been cleared.

**Note:** Following a buffer full condition, the FIFO operation resumes as soon as the RPTR field has been updated to a new value. Writing the same value to RPTR does not restart the FIFO operation, even if the entire buffer contents have been read. After all of the required data has been read from the buffer, the RPTR value should be set equal to the WPTR value; an intermediate (different) value must also be written to the RPTR field in order to clear the buffer full status and restart the FIFO operation.

#### 4.5.2.6 Interrupts, GPIO, Write Sequencer, and DSP Firmware Control

The control-write sequencer is automatically triggered whenever the NOT\_EMPTY status of the event log buffer is asserted. A different control sequence may be configured for each event logger; see [Section 4.18](#) for further details.

The event log status flags are inputs to the interrupt control circuit and can be used to trigger an interrupt event when the respective FIFO condition (full, not empty, or watermark level) occurs; see [Section 4.15](#).

The event log status can be output directly on a GPIO pin as an external indication of the event logger; see [Section 4.14](#) to configure a GPIO pin for this function.

The event log NOT\_EMPTY status can also be selected as a start trigger for DSP firmware execution; see [Section 4.4](#).

#### 4.5.2.7 Event Logger Control Registers

The event logger control registers are described in [Table 4-31](#).

**Table 4-31. Event Logger (EVENTLOG $n$ ) Control**

| Register Address                                                                                                                                                                                 | Bit | Label                         | Default | Description                                                                                                                                                                                      |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------------------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Event Log 1 Base Address = R294912 (0x4_8000)<br>Event Log 2 Base Address = R295424 (0x4_8200)<br>Event Log 3 Base Address = R295936 (0x4_8400)<br>Event Log 4 Base Address = R296448 (0x4_8600) |     |                               |         |                                                                                                                                                                                                  |
| base address<br>EVENTLOG $n$ _CONTROL                                                                                                                                                            | 1   | EVENTLOG $n$ _RST             | 0       | Event Log Reset<br>Write 1 to reset the status outputs and clear the FIFO buffer.                                                                                                                |
|                                                                                                                                                                                                  | 0   | EVENTLOG $n$ _ENA             | 0       | Event Log Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                  |
| Base address +0x04<br>EVENTLOG $n$ _TIMER_SEL                                                                                                                                                    | 1:0 | EVENTLOG $n$ _TIMER_SEL[1:0]  | 00      | Event Log Timer Source Select<br>00 = Timer 1<br>01 = Timer 2<br>10 = Timer 3<br>11 = Timer 4<br>Note that the event log must be disabled when updating this field                               |
| Base address +0x0C<br>EVENTLOG $n$ _FIFO_CONTROL1                                                                                                                                                | 3:0 | EVENTLOG $n$ _FIFO_WMARK[3:0] | 0x1     | Event Log FIFO Watermark. The watermark status output is asserted when the number of FIFO locations available for new events is less than or equal to the FIFO watermark.<br>Valid from 0 to 15. |

**Table 4-31. Event Logger (EVENTLOG<sub>n</sub>) Control (Cont.)**

| Register Address                                               | Bit  | Label                                     | Default | Description                                                                                                                                                                                                            |
|----------------------------------------------------------------|------|-------------------------------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Base address +0x0E<br>EVENTLOG <sub>n</sub> _FIFO_<br>POINTER1 | 18   | EVENTLOG <sub>n</sub> _FULL               | 0       | Event Log FIFO Full Status. This bit, when set, indicates that the FIFO buffer is full. It is cleared when a new value is written to the FIFO read pointer, or when the event log is Reset.                            |
|                                                                | 17   | EVENTLOG <sub>n</sub> _WMARK_STS          | 0       | Event Log FIFO Watermark Status. This bit, when set, indicates that the FIFO space available for new events to be logged is less than or equal to the watermark threshold.                                             |
|                                                                | 16   | EVENTLOG <sub>n</sub> _NOT_EMPTY          | 0       | Event Log FIFO Not Empty Status. This bit, when set, indicates one or more new sets of logged event data in the FIFO.                                                                                                  |
|                                                                | 11:8 | EVENTLOG <sub>n</sub> _FIFO_<br>WPTR[3:0] | 0x0     | Event Log FIFO Write Pointer. Indicates the FIFO index location in which the next event is logged.<br>This is a read-only field.                                                                                       |
|                                                                | 3:0  | EVENTLOG <sub>n</sub> _FIFO_<br>RPTR[3:0] | 0x0     | Event Log FIFO Read Pointer. Indicates the FIFO index location of the first set of unread data, if any exists. For the intended FIFO behavior, this field must be incremented after the respective data has been read. |
| Base address +0x20<br>EVENTLOG <sub>n</sub> _CH_ENABLE         | 15   | EVENTLOG <sub>n</sub> _CH16_ENA           | 0       | Event Log Channel 16 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                               |
|                                                                | 14   | EVENTLOG <sub>n</sub> _CH15_ENA           | 0       | Event Log Channel 15 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                               |
|                                                                | 13   | EVENTLOG <sub>n</sub> _CH14_ENA           | 0       | Event Log Channel 14 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                               |
|                                                                | 12   | EVENTLOG <sub>n</sub> _CH13_ENA           | 0       | Event Log Channel 13 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                               |
|                                                                | 11   | EVENTLOG <sub>n</sub> _CH12_ENA           | 0       | Event Log Channel 12 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                               |
|                                                                | 10   | EVENTLOG <sub>n</sub> _CH11_ENA           | 0       | Event Log Channel 11 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                               |
|                                                                | 9    | EVENTLOG <sub>n</sub> _CH10_ENA           | 0       | Event Log Channel 10 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                               |
|                                                                | 8    | EVENTLOG <sub>n</sub> _CH9_ENA            | 0       | Event Log Channel 9 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                                |
|                                                                | 7    | EVENTLOG <sub>n</sub> _CH8_ENA            | 0       | Event Log Channel 8 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                                |
|                                                                | 6    | EVENTLOG <sub>n</sub> _CH7_ENA            | 0       | Event Log Channel 7 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                                |
|                                                                | 5    | EVENTLOG <sub>n</sub> _CH6_ENA            | 0       | Event Log Channel 6 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                                |
|                                                                | 4    | EVENTLOG <sub>n</sub> _CH5_ENA            | 0       | Event Log Channel 5 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                                |
|                                                                | 3    | EVENTLOG <sub>n</sub> _CH4_ENA            | 0       | Event Log Channel 4 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                                |
|                                                                | 2    | EVENTLOG <sub>n</sub> _CH3_ENA            | 0       | Event Log Channel 3 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                                |
|                                                                | 1    | EVENTLOG <sub>n</sub> _CH2_ENA            | 0       | Event Log Channel 2 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                                |
|                                                                | 0    | EVENTLOG <sub>n</sub> _CH1_ENA            | 0       | Event Log Channel 1 Enable<br>0 = Disabled, 1 = Enabled                                                                                                                                                                |
| Base address +0x40<br>EVENTLOG <sub>n</sub> _CH1_DEFINE        | 15   | EVENTLOG <sub>n</sub> _CH1_DB             | 0       | Event Log Channel 1 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                                                                                               |
|                                                                | 14   | EVENTLOG <sub>n</sub> _CH1_POL            | 0       | Event Log Channel 1 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field                                                                   |
|                                                                | 8:0  | EVENTLOG <sub>n</sub> _CH1_SEL[8:0]       | 0x000   | Event Log Channel 1 source <sup>1</sup><br>Note that channel must be disabled when updating this field                                                                                                                 |

**Table 4-31. Event Logger (EVENTLOG<sub>n</sub>) Control (Cont.)**

| Register Address                                        | Bit | Label                               | Default | Description                                                                                                                                          |
|---------------------------------------------------------|-----|-------------------------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| Base address +0x42<br>EVENTLOG <sub>n</sub> _CH2_DEFINE | 15  | EVENTLOG <sub>n</sub> _CH2_DB       | 0       | Event Log Channel 2 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                             |
|                                                         | 14  | EVENTLOG <sub>n</sub> _CH2_POL      | 0       | Event Log Channel 2 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field |
|                                                         | 8:0 | EVENTLOG <sub>n</sub> _CH2_SEL[8:0] | 0x000   | Event Log Channel 2 source <sup>1</sup><br>Field description is as above.                                                                            |
| Base address +0x44<br>EVENTLOG <sub>n</sub> _CH3_DEFINE | 15  | EVENTLOG <sub>n</sub> _CH3_DB       | 0       | Event Log Channel 3 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                             |
|                                                         | 14  | EVENTLOG <sub>n</sub> _CH3_POL      | 0       | Event Log Channel 3 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field |
|                                                         | 8:0 | EVENTLOG <sub>n</sub> _CH3_SEL[8:0] | 0x000   | Event Log Channel 3 source <sup>1</sup><br>Field description is as above.                                                                            |
| Base address +0x46<br>EVENTLOG <sub>n</sub> _CH4_DEFINE | 15  | EVENTLOG <sub>n</sub> _CH4_DB       | 0       | Event Log Channel 4 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                             |
|                                                         | 14  | EVENTLOG <sub>n</sub> _CH4_POL      | 0       | Event Log Channel 4 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field |
|                                                         | 8:0 | EVENTLOG <sub>n</sub> _CH4_SEL[8:0] | 0x000   | Event Log Channel 4 source <sup>1</sup><br>Field description is as above.                                                                            |
| Base address +0x48<br>EVENTLOG <sub>n</sub> _CH5_DEFINE | 15  | EVENTLOG <sub>n</sub> _CH5_DB       | 0       | Event Log Channel 5 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                             |
|                                                         | 14  | EVENTLOG <sub>n</sub> _CH5_POL      | 0       | Event Log Channel 5 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field |
|                                                         | 8:0 | EVENTLOG <sub>n</sub> _CH5_SEL[8:0] | 0x000   | Event Log Channel 5 source <sup>1</sup><br>Field description is as above.                                                                            |
| Base address +0x4A<br>EVENTLOG <sub>n</sub> _CH6_DEFINE | 15  | EVENTLOG <sub>n</sub> _CH6_DB       | 0       | Event Log Channel 6 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                             |
|                                                         | 14  | EVENTLOG <sub>n</sub> _CH6_POL      | 0       | Event Log Channel 6 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field |
|                                                         | 8:0 | EVENTLOG <sub>n</sub> _CH6_SEL[8:0] | 0x000   | Event Log Channel 6 source <sup>1</sup><br>Field description is as above.                                                                            |
| Base address +0x4C<br>EVENTLOG <sub>n</sub> _CH7_DEFINE | 15  | EVENTLOG <sub>n</sub> _CH7_DB       | 0       | Event Log Channel 7 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                             |
|                                                         | 14  | EVENTLOG <sub>n</sub> _CH7_POL      | 0       | Event Log Channel 7 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field |
|                                                         | 8:0 | EVENTLOG <sub>n</sub> _CH7_SEL[8:0] | 0x000   | Event Log Channel 7 source <sup>1</sup><br>Field description is as above.                                                                            |
| Base address +0x4E<br>EVENTLOG <sub>n</sub> _CH8_DEFINE | 15  | EVENTLOG <sub>n</sub> _CH8_DB       | 0       | Event Log Channel 8 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                             |
|                                                         | 14  | EVENTLOG <sub>n</sub> _CH8_POL      | 0       | Event Log Channel 8 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field |
|                                                         | 8:0 | EVENTLOG <sub>n</sub> _CH8_SEL[8:0] | 0x000   | Event Log Channel 8 source <sup>1</sup><br>Field description is as above.                                                                            |

**Table 4-31. Event Logger (EVENTLOG<sub>n</sub>) Control (Cont.)**

| Register Address                                         | Bit | Label                                | Default | Description                                                                                                                                           |
|----------------------------------------------------------|-----|--------------------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| Base address +0x50<br>EVENTLOG <sub>n</sub> _CH9_DEFINE  | 15  | EVENTLOG <sub>n</sub> _CH9_DB        | 0       | Event Log Channel 9 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                              |
|                                                          | 14  | EVENTLOG <sub>n</sub> _CH9_POL       | 0       | Event Log Channel 9 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field  |
|                                                          | 8:0 | EVENTLOG <sub>n</sub> _CH9_SEL[8:0]  | 0x000   | Event Log Channel 9 source <sup>1</sup><br>Field description is as above.                                                                             |
| Base address +0x52<br>EVENTLOG <sub>n</sub> _CH10_DEFINE | 15  | EVENTLOG <sub>n</sub> _CH10_DB       | 0       | Event Log Channel 10 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                             |
|                                                          | 14  | EVENTLOG <sub>n</sub> _CH10_POL      | 0       | Event Log Channel 10 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field |
|                                                          | 8:0 | EVENTLOG <sub>n</sub> _CH10_SEL[8:0] | 0x000   | Event Log Channel 10 source <sup>1</sup><br>Field description is as above.                                                                            |
| Base address +0x54<br>EVENTLOG <sub>n</sub> _CH11_DEFINE | 15  | EVENTLOG <sub>n</sub> _CH11_DB       | 0       | Event Log Channel 11 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                             |
|                                                          | 14  | EVENTLOG <sub>n</sub> _CH11_POL      | 0       | Event Log Channel 11 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field |
|                                                          | 8:0 | EVENTLOG <sub>n</sub> _CH11_SEL[8:0] | 0x000   | Event Log Channel 11 source <sup>1</sup><br>Field description is as above.                                                                            |
| Base address +0x56<br>EVENTLOG <sub>n</sub> _CH12_DEFINE | 15  | EVENTLOG <sub>n</sub> _CH12_DB       | 0       | Event Log Channel 12 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                             |
|                                                          | 14  | EVENTLOG <sub>n</sub> _CH12_POL      | 0       | Event Log Channel 12 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field |
|                                                          | 8:0 | EVENTLOG <sub>n</sub> _CH12_SEL[8:0] | 0x000   | Event Log Channel 12 source <sup>1</sup><br>Field description is as above.                                                                            |
| Base address +0x58<br>EVENTLOG <sub>n</sub> _CH13_DEFINE | 15  | EVENTLOG <sub>n</sub> _CH13_DB       | 0       | Event Log Channel 13 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                             |
|                                                          | 14  | EVENTLOG <sub>n</sub> _CH13_POL      | 0       | Event Log Channel 13 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field |
|                                                          | 8:0 | EVENTLOG <sub>n</sub> _CH13_SEL[8:0] | 0x000   | Event Log Channel 13 source <sup>1</sup><br>Field description is as above.                                                                            |
| Base address +0x5A<br>EVENTLOG <sub>n</sub> _CH14_DEFINE | 15  | EVENTLOG <sub>n</sub> _CH14_DB       | 0       | Event Log Channel 14 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                             |
|                                                          | 14  | EVENTLOG <sub>n</sub> _CH14_POL      | 0       | Event Log Channel 14 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field |
|                                                          | 8:0 | EVENTLOG <sub>n</sub> _CH14_SEL[8:0] | 0x000   | Event Log Channel 14 source <sup>1</sup><br>Field description is as above.                                                                            |
| Base address +0x5C<br>EVENTLOG <sub>n</sub> _CH15_DEFINE | 15  | EVENTLOG <sub>n</sub> _CH15x_DB      | 0       | Event Log Channel 15 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                             |
|                                                          | 14  | EVENTLOG <sub>n</sub> _CH15_POL      | 0       | Event Log Channel 15 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field |
|                                                          | 8:0 | EVENTLOG <sub>n</sub> _CH15_SEL[8:0] | 0x000   | Event Log Channel 15 source <sup>1</sup><br>Field description is as above.                                                                            |

**Table 4-31. Event Logger (EVENTLOGn) Control (Cont.)**

| Register Address                                | Bit  | Label                          | Default         | Description                                                                                                                                           |
|-------------------------------------------------|------|--------------------------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| Base address +0x5E<br>EVENTLOGn_CH16_<br>DEFINE | 15   | EVENTLOGn_CH16_DB              | 0               | Event Log Channel 16 debounce<br>0 = Disabled, 1 = Enabled<br>Note that channel must be disabled when updating this field                             |
|                                                 | 14   | EVENTLOGn_CH16_POL             | 0               | Event Log Channel 16 polarity<br>0 = Rising edge triggered, 1 = Falling edge triggered<br>Note that channel must be disabled when updating this field |
|                                                 | 8:0  | EVENTLOGn_CH16_SEL[8:0]        | 0x000           | Event Log Channel 16 source <sup>1</sup><br>Field description is as above.                                                                            |
| Base address +0x80<br>EVENTLOGn_FIFO0_READ      | 12   | EVENTLOGn_FIFO0_POL            | 0               | Event Log FIFO Index 0 polarity<br>0 = Rising edge, 1 = Falling edge                                                                                  |
|                                                 | 8:0  | EVENTLOGn_FIFO0_ID[8:0]        | 0x000           | Event Log FIFO Index 0 source <sup>1</sup>                                                                                                            |
| Base address +0x82<br>EVENTLOGn_FIFO0_TIME      | 31:0 | EVENTLOGn_FIFO0_<br>TIME[31:0] | 0x0000<br>_0000 | Event Log FIFO Index 0 Time                                                                                                                           |
| Base address +0x84<br>EVENTLOGn_FIFO1_READ      | 12   | EVENTLOGn_FIFO1_POL            | 0               | Event Log FIFO Index 1 polarity<br>0 = Rising edge, 1 = Falling edge                                                                                  |
|                                                 | 8:0  | EVENTLOGn_FIFO1_ID[8:0]        | 0x000           | Event Log FIFO Index 1 source <sup>1</sup>                                                                                                            |
| Base address +0x86<br>EVENTLOGn_FIFO1_TIME      | 31:0 | EVENTLOGn_FIFO1_<br>TIME[31:0] | 0x0000<br>_0000 | Event Log FIFO Index 1 Time                                                                                                                           |
| Base address +0x88<br>EVENTLOGn_FIFO2_READ      | 12   | EVENTLOGn_FIFO2_POL            | 0               | Event Log FIFO Index 2 polarity<br>0 = Rising edge, 1 = Falling edge                                                                                  |
|                                                 | 8:0  | EVENTLOGn_FIFO2_ID[8:0]        | 0x000           | Event Log FIFO Index 2 source <sup>1</sup>                                                                                                            |
| Base address +0x8A<br>EVENTLOGn_FIFO2_TIME      | 31:0 | EVENTLOGn_FIFO2_<br>TIME[31:0] | 0x0000<br>_0000 | Event Log FIFO Index 2 Time                                                                                                                           |
| Base address +0x8C<br>EVENTLOGn_FIFO3_READ      | 12   | EVENTLOGn_FIFO3_POL            | 0               | Event Log FIFO Index 3 polarity<br>0 = Rising edge, 1 = Falling edge                                                                                  |
|                                                 | 8:0  | EVENTLOGn_FIFO3_ID[8:0]        | 0x000           | Event Log FIFO Index 3 source <sup>1</sup>                                                                                                            |
| Base address +0x8E<br>EVENTLOGn_FIFO3_TIME      | 31:0 | EVENTLOGn_FIFO3_<br>TIME[31:0] | 0x0000<br>_0000 | Event Log FIFO Index 3 Time                                                                                                                           |
| Base address +0x90<br>EVENTLOGn_FIFO4_READ      | 12   | EVENTLOGn_FIFO4_POL            | 0               | Event Log FIFO Index 4 polarity<br>0 = Rising edge, 1 = Falling edge                                                                                  |
|                                                 | 8:0  | EVENTLOGn_FIFO4_ID[8:0]        | 0x000           | Event Log FIFO Index 4 source <sup>1</sup>                                                                                                            |
| Base address +0x92<br>EVENTLOGn_FIFO4_TIME      | 31:0 | EVENTLOGn_FIFO4_<br>TIME[31:0] | 0x0000<br>_0000 | Event Log FIFO Index 4 Time                                                                                                                           |
| Base address +0x94<br>EVENTLOGn_FIFO5_READ      | 12   | EVENTLOGn_FIFO5_POL            | 0               | Event Log FIFO Index 5 polarity<br>0 = Rising edge, 1 = Falling edge                                                                                  |
|                                                 | 8:0  | EVENTLOGn_FIFO5_ID[8:0]        | 0x000           | Event Log FIFO Index 5 source <sup>1</sup>                                                                                                            |
| Base address +0x96<br>EVENTLOGn_FIFO5_TIME      | 31:0 | EVENTLOGn_FIFO5_<br>TIME[31:0] | 0x0000<br>_0000 | Event Log FIFO Index 5 Time                                                                                                                           |
| Base address +0x98<br>EVENTLOGn_FIFO6_READ      | 12   | EVENTLOGn_FIFO6_POL            | 0               | Event Log FIFO Index 6 polarity<br>0 = Rising edge, 1 = Falling edge                                                                                  |
|                                                 | 8:0  | EVENTLOGn_FIFO6_ID[8:0]        | 0x000           | Event Log FIFO Index 6 source <sup>1</sup>                                                                                                            |
| Base address +0x9A<br>EVENTLOGn_FIFO6_TIME      | 31:0 | EVENTLOGn_FIFO6_<br>TIME[31:0] | 0x0000<br>_0000 | Event Log FIFO Index 6 Time                                                                                                                           |
| Base address +0x9C<br>EVENTLOGn_FIFO7_READ      | 12   | EVENTLOGn_FIFO7_POL            | 0               | Event Log FIFO Index 7 polarity<br>0 = Rising edge, 1 = Falling edge                                                                                  |
|                                                 | 8:0  | EVENTLOGn_FIFO7_ID[8:0]        | 0x000           | Event Log FIFO Index 7 source <sup>1</sup>                                                                                                            |
| Base address +0x9E<br>EVENTLOGn_FIFO7_TIME      | 31:0 | EVENTLOGn_FIFO7_<br>TIME[31:0] | 0x0000<br>_0000 | Event Log FIFO Index 7 Time                                                                                                                           |
| Base address +0xA0<br>EVENTLOGn_FIFO8_READ      | 12   | EVENTLOGn_FIFO8_POL            | 0               | Event Log FIFO Index 8 polarity<br>0 = Rising edge, 1 = Falling edge                                                                                  |
|                                                 | 8:0  | EVENTLOGn_FIFO8_ID[8:0]        | 0x000           | Event Log FIFO Index 8 source <sup>1</sup>                                                                                                            |
| Base address +0xA2<br>EVENTLOGn_FIFO8_TIME      | 31:0 | EVENTLOGn_FIFO8_<br>TIME[31:0] | 0x0000<br>_0000 | Event Log FIFO Index 8 Time                                                                                                                           |
| Base address +0xA4<br>EVENTLOGn_FIFO9_READ      | 12   | EVENTLOGn_FIFO9_POL            | 0               | Event Log FIFO Index 9 polarity<br>0 = Rising edge, 1 = Falling edge                                                                                  |
|                                                 | 8:0  | EVENTLOGn_FIFO9_ID[8:0]        | 0x000           | Event Log FIFO Index 9 source <sup>1</sup>                                                                                                            |

**Table 4-31. Event Logger (EVENTLOG<sub>n</sub>) Control (Cont.)**

| Register Address                                         | Bit  | Label                                    | Default     | Description                                                           |
|----------------------------------------------------------|------|------------------------------------------|-------------|-----------------------------------------------------------------------|
| Base address +0xA6<br>EVENTLOG <sub>n</sub> _FIFO9_TIME  | 31:0 | EVENTLOG <sub>n</sub> _FIFO9_TIME[31:0]  | 0x0000_0000 | Event Log FIFO Index 9 Time                                           |
| Base address +0xA8<br>EVENTLOG <sub>n</sub> _FIFO10_READ | 12   | EVENTLOG <sub>n</sub> _FIFO10_POL        | 0           | Event Log FIFO Index 10 polarity<br>0 = Rising edge, 1 = Falling edge |
|                                                          | 8:0  | EVENTLOG <sub>n</sub> _FIFO10_ID[8:0]    | 0x000       | Event Log FIFO Index 10 source <sup>1</sup>                           |
| Base address +0xAA<br>EVENTLOG <sub>n</sub> _FIFO10_TIME | 31:0 | EVENTLOG <sub>n</sub> _FIFO10_TIME[31:0] | 0x0000_0000 | Event Log FIFO Index 10 Time                                          |
| Base address +0xAC<br>EVENTLOG <sub>n</sub> _FIFO11_READ | 12   | EVENTLOG <sub>n</sub> _FIFO11_POL        | 0           | Event Log FIFO Index 11 polarity<br>0 = Rising edge, 1 = Falling edge |
|                                                          | 8:0  | EVENTLOG <sub>n</sub> _FIFO11_ID[8:0]    | 0x000       | Event Log FIFO Index 11 source <sup>1</sup>                           |
| Base address +0xAE<br>EVENTLOG <sub>n</sub> _FIFO11_TIME | 31:0 | EVENTLOG <sub>n</sub> _FIFO11_TIME[31:0] | 0x0000_0000 | Event Log FIFO Index 11 Time                                          |
| Base address +0xB0<br>EVENTLOG <sub>n</sub> _FIFO12_READ | 12   | EVENTLOG <sub>n</sub> _FIFO12_POL        | 0           | Event Log FIFO Index 12 polarity<br>0 = Rising edge, 1 = Falling edge |
|                                                          | 8:0  | EVENTLOG <sub>n</sub> _FIFO12_ID[8:0]    | 0x000       | Event Log FIFO Index 12 source <sup>1</sup>                           |
| Base address +0xB2<br>EVENTLOG <sub>n</sub> _FIFO12_TIME | 31:0 | EVENTLOG <sub>n</sub> _FIFO12_TIME[31:0] | 0x0000_0000 | Event Log FIFO Index 12 Time                                          |
| Base address +0xB4<br>EVENTLOG <sub>n</sub> _FIFO13_READ | 12   | EVENTLOG <sub>n</sub> _FIFO13_POL        | 0           | Event Log FIFO Index 13 polarity<br>0 = Rising edge, 1 = Falling edge |
|                                                          | 8:0  | EVENTLOG <sub>n</sub> _FIFO13_ID[8:0]    | 0x000       | Event Log FIFO Index 13 source <sup>1</sup>                           |
| Base address +0xB6<br>EVENTLOG <sub>n</sub> _FIFO13_TIME | 31:0 | EVENTLOG <sub>n</sub> _FIFO13_TIME[31:0] | 0x0000_0000 | Event Log FIFO Index 13 Time                                          |
| Base address +0xB8<br>EVENTLOG <sub>n</sub> _FIFO14_READ | 12   | EVENTLOG <sub>n</sub> _FIFO14_POL        | 0           | Event Log FIFO Index 14 polarity<br>0 = Rising edge, 1 = Falling edge |
|                                                          | 8:0  | EVENTLOG <sub>n</sub> _FIFO14_ID[8:0]    | 0x000       | Event Log FIFO Index 14 source <sup>1</sup>                           |
| Base address +0xBA<br>EVENTLOG <sub>n</sub> _FIFO14_TIME | 31:0 | EVENTLOG <sub>n</sub> _FIFO14_TIME[31:0] | 0x0000_0000 | Event Log FIFO Index 14 Time                                          |
| Base address +0xBC<br>EVENTLOG <sub>n</sub> _FIFO15_READ | 12   | EVENTLOG <sub>n</sub> _FIFO15_POL        | 0           | Event Log FIFO Index 15 polarity<br>0 = Rising edge, 1 = Falling edge |
|                                                          | 8:0  | EVENTLOG <sub>n</sub> _FIFO15_ID[8:0]    | 0x000       | Event Log FIFO Index 15 source <sup>1</sup>                           |
| Base address +0xBE<br>EVENTLOG <sub>n</sub> _FIFO15_TIME | 31:0 | EVENTLOG <sub>n</sub> _FIFO15_TIME[31:0] | 0x0000_0000 | Event Log FIFO Index 15 Time                                          |

1. See [Table 4-32](#) for valid channel source selections

### 4.5.2.8 Event Logger Input Sources

A list of the valid input sources for the event loggers is provided in [Table 4-32](#).

The EDGE type noted is coded as *S* (single edge) or *D* (dual edge). Note that a single-edge input source only provides valid input to the event logger in the default (rising edge triggered) polarity.

Take care when enabling IRQ1 or IRQ2 as an input source for the event loggers; a recursive loop, where the IRQ<sub>n</sub> signal is also an output from the same event logger, must be avoided.

**Table 4-32. Event Logger Input Sources**

| ID | Description      | Edge | ID  | Description   | Edge | ID  | Description      | Edge |
|----|------------------|------|-----|---------------|------|-----|------------------|------|
| 3  | irq1             | D    | 173 | dsp_irq14     | S    | 323 | Timer4           | S    |
| 4  | irq2             | D    | 174 | dsp_irq15     | S    | 336 | event1_not_empty | S    |
| 9  | sysclk_fail      | S    | 175 | dsp_irq16     | S    | 337 | event2_not_empty | S    |
| 24 | fl1_lock         | D    | 176 | hp1l_sc       | S    | 338 | event3_not_empty | S    |
| 32 | frame_start_g1r1 | S    | 177 | hp1r_sc       | S    | 339 | event4_not_empty | S    |
| 33 | frame_start_g1r2 | S    | 178 | hp2l_sc       | S    | 352 | event1_full      | S    |
| 34 | frame_start_g1r3 | S    | 179 | hp2r_sc       | S    | 353 | event2_full      | S    |
| 80 | hpdet            | S    | 182 | spkoutl_short | D    | 354 | event3_full      | S    |
| 88 | micdet           | S    | 224 | spk_shutdown  | D    | 355 | event4_full      | S    |
| 96 | jd1_rise         | S    | 225 | spk_overheat  | S    | 368 | event1_wmark     | S    |

**Table 4-32. Event Logger Input Sources (Cont.)**

| ID  | Description     | Edge | ID  | Description       | Edge | ID  | Description  | Edge |
|-----|-----------------|------|-----|-------------------|------|-----|--------------|------|
| 97  | jd1_fall        | S    | 226 | spk_overheat_warn | S    | 369 | event2_wmark | S    |
| 98  | jd2_rise        | S    | 256 | gpio1             | D    | 370 | event3_wmark | S    |
| 99  | jd2_fall        | S    | 257 | gpio2             | D    | 371 | event4_wmark | S    |
| 100 | micd_clamp_rise | S    | 258 | gpio3             | D    | 384 | dsp1_dma     | S    |
| 101 | micd_clamp_fall | S    | 259 | gpio4             | D    | 385 | dsp2_dma     | S    |
| 128 | drc1_sig_det    | D    | 260 | gpio5             | D    | 386 | dsp3_dma     | S    |
| 129 | drc2_sig_det    | D    | 261 | gpio6             | D    | 416 | dsp1_start1  | S    |
| 160 | dsp_irq1        | S    | 262 | gpio7             | D    | 417 | dsp2_start1  | S    |
| 161 | dsp_irq2        | S    | 263 | gpio8             | D    | 418 | dsp3_start1  | S    |
| 162 | dsp_irq3        | S    | 264 | gpio9             | D    | 432 | dsp1_start2  | S    |
| 163 | dsp_irq4        | S    | 265 | gpio10            | D    | 433 | dsp2_start2  | S    |
| 164 | dsp_irq5        | S    | 266 | gpio11            | D    | 434 | dsp3_start2  | S    |
| 165 | dsp_irq6        | S    | 267 | gpio12            | D    | 448 | dsp1_start   | S    |
| 166 | dsp_irq7        | S    | 268 | gpio13            | D    | 449 | dsp2_start   | S    |
| 167 | dsp_irq8        | S    | 269 | gpio14            | D    | 450 | dsp3_start   | S    |
| 168 | dsp_irq9        | S    | 270 | gpio15            | D    | 464 | dsp1_busy    | D    |
| 169 | dsp_irq10       | S    | 271 | gpio16            | D    | 465 | dsp2_busy    | D    |
| 170 | dsp_irq11       | S    | 320 | Timer1            | S    | 466 | dsp3_busy    | D    |
| 171 | dsp_irq12       | S    | 321 | Timer2            | S    | 480 | mif1_done    | S    |
| 172 | dsp_irq13       | S    | 322 | Timer3            | S    | 496 | mif1_block   | S    |

### 4.5.3 General-Purpose Timers

The CS47L35 incorporates four general-purpose timers, which support a wide variety of uses. In particular, these timers provide essential support for the sensor-hub capability.

#### 4.5.3.1 Overview

The timers allow time stamp information to be associated with external sensor activity, and other system events, enabling real time data to be more easily integrated into user applications. The timers allow many advanced functions to be implemented with a high degree of autonomy from a host processor.

The timers can use either internal system clocks, or external clock signals, as a reference. The selected reference is scaled down, using configurable dividers, to the required clock count frequency.

#### 4.5.3.2 Timer Control

The reference clock for each timer is selected using `TIMERn_REFCLK_SRC`, (where *n* identifies the applicable timer, 1–4).

If `SYSCLK` or `DSPCLK` is selected, a lower clock frequency, derived from the applicable system clock, can be selected using the `TIMERn_REFCLK_FREQ_SEL` field. The applicable division ratio is determined automatically, assuming the respective clock source has been correctly configured as described in [Section 4.16](#).

If any source other than `DSPCLK` is selected, the clock can be further divided using `TIMERn_REFCLK_DIV`. Division ratios in the range 1 to 128 can be selected.

Note that, if `DSPCLK` is enabled, the CS47L35 synchronizes the selected reference clock to `DSPCLK`. As a result of this, if a non-`DSPCLK` is selected as source, the following additional constraints must be observed: the reference clock frequency (after `TIMERn_REFCLK_FREQ_SEL` and after `TIMERn_REFCLK_DIV`) must be less than `DSPCLK / 3`, and must be less than 12 MHz; it must also be close to 50% duty cycle. The `TIMERn_REFCLK_DIV` field can be used to ensure that these criteria are met.

One final division, controlled by `TIMERn_PRESCALE`, determines the timer count frequency. This field is valid for all clock reference sources; division ratios in the range 1 to 128 can be selected. The output from this division corresponds to the frequency at which the `TIMERn_COUNT` fields are incremented (or decremented).

The maximum count value of the timer is determined by the `TIMERn_MAX_COUNT` field. This is the final count value (when counting up), or the initial count value (when counting down). The current value of the timer counter can be read from the `TIMERn_CUR_COUNT` field.

The timer is started by writing 1 to `TIMERn_START`. Note that, if the timer is already running, it restarts from its initial value. The timer is stopped by writing 1 to `TIMERn_STOP`. The count direction (up or down) is selected using the `TIMERn_DIR` bit.

The `TIMERn_CONTINUOUS` bit selects whether the timer automatically restarts after the end-of-count condition has been reached. The `TIMERn_RUNNING_STS` indicates whether the timer is running, or if it has stopped.

Note that the timers should be stopped before making any changes to the respective configuration registers. The timer configuration should only be changed when `TIMERn_RUNNING_STS` = 0.

The reference clock for each Timer should be configured and enabled before starting the Timer, and whenever the Timer is running. If the reference clock is interrupted while the Timer is running, the Timer operation pauses, and resumes again when the clock restarts. See [Section 4.16](#) for details of the system clocks (including requirements for reconfiguring DSPCLK while DSP peripherals are enabled).

### 4.5.3.3 Interrupts, GPIO, and Class D Speaker Driver Control

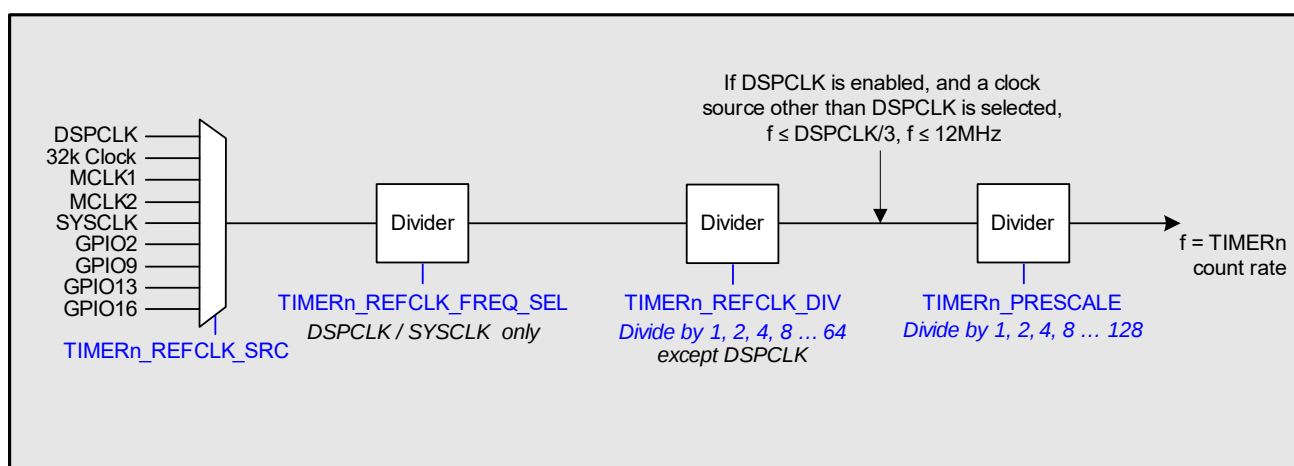
The timer status is an input to the interrupt control circuit and can be used to trigger an interrupt event after the final count value is reached; see [Section 4.15](#). Note that the interrupt does not occur immediately when the final count value is reached; the interrupt is triggered at the point when the next update to the timer count value would be due.

The timer status can be output directly on a GPIO pin as an external indication of the timer activity. See [Section 4.14](#) to configure a GPIO pin for this function.

The timers can be used as a watchdog function to trigger a shutdown of the Class D speaker drivers. See [Section 4.21](#) to configure this function.

### 4.5.3.4 Timer Block Diagram and Control Registers

The timer block is shown in [Fig. 4-32](#).



**Figure 4-32. General-Purpose Timer**

The timer control registers are described in [Table 4-33](#).

**Table 4-33. General-Purpose Timer (TIMERn) Control**

| Register Address                            | Bit   | Label                       | Default     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|---------------------------------------------|-------|-----------------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Timer 1 Base Address = R311296 (0x4_C000)   |       |                             |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Timer 2 Base Address = R311424 (0x4_C080)   |       |                             |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Timer 3 Base Address = R311552 (0x4_C100)   |       |                             |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Timer 4 Base Address = R311680 (0x4_C180)   |       |                             |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Base address<br>Timern_Control              | 21    | TIMERn_CONTINUOUS           | 0           | Timer Continuous Mode select<br>0 = Single mode<br>1 = Continuous mode<br>Timer must be stopped (TIMERn_RUNNING_STS = 0) when updating this field                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|                                             | 20    | TIMERn_DIR                  | 0           | Timer Count Direction<br>0 = Down<br>1 = Up<br>Timer must be stopped (TIMERn_RUNNING_STS = 0) when updating this field                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|                                             | 18:16 | TIMERn_PRESCALE[2:0]        | 000         | Timer Count Rate Prescale<br>000 = Divide by 1                  011 = Divide by 8                  110 = Divide by 64<br>001 = Divide by 2                  100 = Divide by 16                111 = Divide by 128<br>010 = Divide by 4                  101 = Divide by 32<br>Timer must be stopped (TIMERn_RUNNING_STS = 0) when updating this field                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|                                             | 14:12 | TIMERn_REFCLK_DIV[2:0]      | 000         | Timer Reference Clock Divide<br>(Not valid for DSPCLK source).<br>000 = Divide by 1                  011 = Divide by 8                  110 = Divide by 64<br>001 = Divide by 2                  100 = Divide by 16                111 = Divide by 128<br>010 = Divide by 4                  101 = Divide by 32<br>If DSPCLK is enabled, and DSPCLK is not selected as source, the output frequency from this divider must be set less than or equal to DSPCLK/3, and less than or equal to 12 MHz.<br>If DSPCLK is disabled, the output of this divider is used as clock reference for any associated event logger. In this case, the divider output corresponds to the frequency of event logging opportunities on the respective modules.<br>Timer must be stopped (TIMERn_RUNNING_STS = 0) when updating this field |
|                                             | 10:8  | TIMERn_REFCLK_FREQ_SEL[2:0] | 000         | Timer Reference Frequency Select<br>Only valid when SYSCLK or DSPCLK is the source. The selected frequency must be less than or equal to the frequency of the respective source.<br>All other codes are reserved<br>Note that, because DSPCLK could be any frequency (within the valid ranges), it is not possible to quote exact frequencies in this field definition. The exact frequency is derived as DSPCLK divided by 1, 2, 4, 8, or 16.<br>Timer must be stopped (TIMERn_RUNNING_STS=0) when updating this field.                                                                                                                                                                                                                                                                                                |
|                                             | 3:0   | TImERN_refclk_SRC[3:0]      | 0000        | SYSCLK Source:<br>000 = 6.144 MHz (5.6448 MHz)<br>001 = 12.288 MHz (11.2896 MHz)<br>010 = 24.576 MHz (22.5792 MHz)<br>011 = 49.152 MHz (45.1584 MHz)<br>All other codes are reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                                             |       |                             |             | DSPCLK Source:<br>000 = 5.5 MHz to 9.375 MHz<br>001 = 9.375 MHz to 18.75 MHz<br>010 = 18.75 MHz to 37.5 MHz<br>011 = 37.5 MHz to 75 MHz                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| Base address +0x02<br>Timern_Count_Preset   | 31:0  | TIMERn_MAX_COUNT[31:0]      | 0x0000_0000 | Timer Maximum Count<br>Final count value (when counting up)<br>Starting count value (when counting down)<br>Timer must be stopped (TIMERn_RUNNING_STS = 0) when updating this field                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| Base address +0x06<br>Timern_Start_and_Stop | 4     | TIMERn_STOP                 | 0           | Timer Stop Control<br>Write 1 to stop.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|                                             | 0     | TIMERn_START                | 0           | Timer Start Control<br>Write 1 to start.<br>If the timer is already running, it restarts from its initial value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

**Table 4-33. General-Purpose Timer (TIMER<sub>n</sub>) Control (Cont.)**

| Register Address                               | Bit  | Label                               | Default | Description                                                    |
|------------------------------------------------|------|-------------------------------------|---------|----------------------------------------------------------------|
| Base address<br>+0x08<br>Timern_Status         | 0    | TIMER <sub>n</sub> _RUNNING_STS     | 0       | Timer Running Status<br>0 = Timer stopped<br>1 = Timer running |
| Base address<br>+0x0A<br>Timern_Count_Readback | 31:0 | TIMER <sub>n</sub> _CUR_COUNT[31:0] | 0x0000  | Timer Current Count value                                      |

## 4.5.4 DSP GPIO

The DSP GPIO function provides an advanced I/O capability, supporting the requirements of the CS47L35 as a multipurpose sensor hub.

### 4.5.4.1 Overview

The CS47L35 supports up to 16 GPIO pins; these are implemented as alternate functions to a pin-specific capability.

The GPIOs can be used to provide status outputs and control signals to external hardware; the supported functions include interrupt output, FLL clock output, accessory detection status, and S/PDIF or PWM-coded audio channels; see [Section 4.14](#).

The GPIOs can support miscellaneous logic input and output, interfacing directly with the integrated DSPs, or with the Host Application software. A basic level of I/O functionality is described in [Section 4.14](#), under the configuration where GP<sub>n</sub>\_FN = 0x001. The GP<sub>n</sub>\_FN field selects the functionality for the respective pin, GPIO<sub>n</sub>.

The DSP GPIO pins are accessed using maskable sets of I/O control registers; this allows the selected combinations of GPIOs to be controlled with ease, regardless of how the allocation of GPIO pins has been implemented in hardware. In a typical use case, one GPIO mask is defined for each DSP, or for each functional process; this provides a highly efficient mechanism for each DSP to independently access the respective input and output signals.

### 4.5.4.2 DSP GPIO Control

The DSP GPIO function is selected by setting GP<sub>n</sub>\_FN = 0x002 for the respective GPIO pin (where *n* identifies the applicable GPIO<sub>n</sub> pin).

Each DSP GPIO is controlled using bits that determine the direction (input/output) and the logic state (0/1) of the pin. These bits are replicated in four control sets; each which can determine the logic level of any DSP GPIO.

Mask bits are provided within each control set, to determine which of the control sets has control of each DSP GPIO. To avoid logic contention, a DSP GPIO output must be controlled (unmasked) in a maximum of one control set at any time.

Note that write access to the direction control bits (DSPGP<sub>n</sub>\_SET<sub>x</sub>\_DIR) and level control bits (DSPGP<sub>n</sub>\_SET<sub>x</sub>\_LVL) is only valid when the channel (DSPGP<sub>n</sub>) is unmasked in the respective control set. Writes to these fields are implemented for the unmasked DSP GPIOs, and are ignored in respect of the masked DSP GPIOs. Note that the level control bits (DSPGP<sub>n</sub>\_SET<sub>x</sub>\_LVL) provide output level control only—they cannot be used to read the status of DSP GPIO inputs.

The logic level of the unmasked DSP GPIO outputs in any control set can be configured using a single register write. Writing to the output level control registers determines the logic level of the unmasked DSP GPIOs in that set only; all other outputs are unaffected.

DSP GPIO status bits are provided, indicating the logic level of every input or output pin that is configured as a DSP GPIO. The DSPGP<sub>n</sub>\_STS bits also provide logic-level indication for any pin that is configured as a GPIO input, with GP<sub>n</sub>\_FN = 0x001. Note that there is only one set of DSP GPIO status bits.

The status bits indicate the logic level of the DSP GPIO outputs. The respective pins are driven as outputs if configured as a DSP GPIO output, and unmasked in one of the control sets. Note that a DSP GPIO continues to be driven as an output, even if the mask bit is subsequently asserted in that set. The pin only ceases to be driven if it is configured as a DSP GPIO input and is unmasked in one of the control sets, or if the pin is configured as an input under a different GP<sub>n</sub>\_FN field selection.

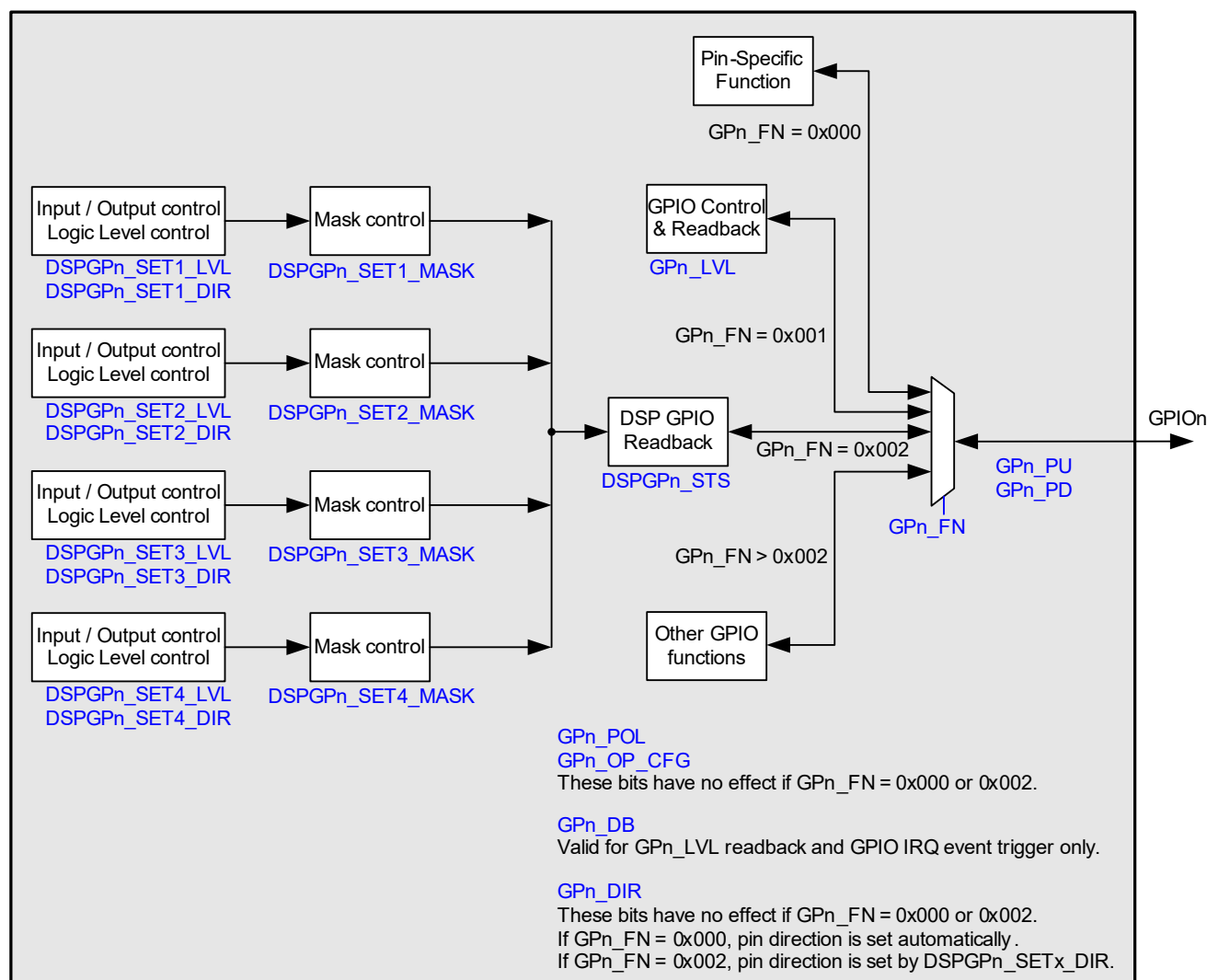
### 4.5.4.3 Common Functions to Standard GPIOs

The DSP GPIO functions are implemented alongside the standard GPIO capability, providing an alternative method of maskable I/O control for all of the GPIO pins. The DSP GPIO control bits in the register map are implemented in a manner that supports efficient read/write access for multiple GPIOs at once.

The DSP GPIO logic is shown in [Fig. 4-33](#), which also shows the control fields relating to the standard GPIO.

The DSP GPIO function is selected by setting  $GPn\_FN = 0x002$  for the respective GPIO pin. Integrated pull-up and pull-down resistors are provided on each of the GPIO pins, which are also valid for DSP GPIO function. A bus keeper function is supported on the GPIO pins; this is enabled using the respective pull-up and pull-down control bits. The bus keeper function holds the logic level unchanged whenever the pin is undriven (e.g., if the signal is tristated). See [Table 4-83](#) for details of the GPIO pull-up and pull-down control bits.

### 4.5.4.4 DSP GPIO Block Diagram and Control Registers



**Figure 4-33. DSP GPIO Control**

The control registers associated with the DSP GPIO are described in [Table 4-34](#).

**Table 4-34. DSP GPIO Control**

| Register Address                                                                                                                                                                             | Bit | Label             | Default | Description                                                                                                                      |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-------------------|---------|----------------------------------------------------------------------------------------------------------------------------------|
| R315392 (0x4_D000)<br>DSPGP_Status_1                                                                                                                                                         | 15  | DSPGP16_STS       | 0       | DSPGP16 Status<br>Valid for DSPGP input and output                                                                               |
|                                                                                                                                                                                              | 14  | DSPGP15_STS       | 0       | DSPGP15 Status                                                                                                                   |
|                                                                                                                                                                                              | 13  | DSPGP14_STS       | 0       | DSPGP14 Status                                                                                                                   |
|                                                                                                                                                                                              | 12  | DSPGP13_STS       | 0       | DSPGP13 Status                                                                                                                   |
|                                                                                                                                                                                              | 11  | DSPGP12_STS       | 0       | DSPGP12 Status                                                                                                                   |
|                                                                                                                                                                                              | 10  | DSPGP11_STS       | 0       | DSPGP11 Status                                                                                                                   |
|                                                                                                                                                                                              | 9   | DSPGP10_STS       | 0       | DSPGP10 Status                                                                                                                   |
|                                                                                                                                                                                              | 8   | DSPGP9_STS        | 0       | DSPGP9 Status                                                                                                                    |
|                                                                                                                                                                                              | 7   | DSPGP8_STS        | 0       | DSPGP8 Status                                                                                                                    |
|                                                                                                                                                                                              | 6   | DSPGP7_STS        | 0       | DSPGP7 Status                                                                                                                    |
|                                                                                                                                                                                              | 5   | DSPGP6_STS        | 0       | DSPGP6 Status                                                                                                                    |
|                                                                                                                                                                                              | 4   | DSPGP5_STS        | 0       | DSPGP5 Status                                                                                                                    |
|                                                                                                                                                                                              | 3   | DSPGP4_STS        | 0       | DSPGP4 Status                                                                                                                    |
|                                                                                                                                                                                              | 2   | DSPGP3_STS        | 0       | DSPGP3 Status                                                                                                                    |
|                                                                                                                                                                                              | 1   | DSPGP2_STS        | 0       | DSPGP2 Status                                                                                                                    |
|                                                                                                                                                                                              | 0   | DSPGP1_STS        | 0       | DSPGP1 Status                                                                                                                    |
| R315424 (0x4_D020)<br>DSPGP_SET1_Mask_1<br>R315456 (0x4_D040)<br>DSPGP_SET2_Mask_1<br>R315488 (0x4_D060)<br>DSPGP_SET3_Mask_1<br>R315520 (0x4_D080)<br>DSPGP_SET4_Mask_1                     | 15  | DSPGP16_SETn_MASK | 1       | DSP SETn GPIO16 Mask Control<br>0 = Unmasked<br>1 = Masked<br>A GPIO pin should be unmasked in a maximum of one SET at any time. |
|                                                                                                                                                                                              | 14  | DSPGP15_SETn_MASK | 1       | DSP SETn GPIO15 Mask Control                                                                                                     |
|                                                                                                                                                                                              | 13  | DSPGP14_SETn_MASK | 1       | DSP SETn GPIO14 Mask Control                                                                                                     |
|                                                                                                                                                                                              | 12  | DSPGP13_SETn_MASK | 1       | DSP SETn GPIO13 Mask Control                                                                                                     |
|                                                                                                                                                                                              | 11  | DSPGP12_SETn_MASK | 1       | DSP SETn GPIO12 Mask Control                                                                                                     |
|                                                                                                                                                                                              | 10  | DSPGP11_SETn_MASK | 1       | DSP SETn GPIO11 Mask Control                                                                                                     |
|                                                                                                                                                                                              | 9   | DSPGP10_SETn_MASK | 1       | DSP SETn GPIO10 Mask Control                                                                                                     |
|                                                                                                                                                                                              | 8   | DSPGP9_SETn_MASK  | 1       | DSP SETn GPIO9 Mask Control                                                                                                      |
|                                                                                                                                                                                              | 7   | DSPGP8_SETn_MASK  | 1       | DSP SETn GPIO8 Mask Control                                                                                                      |
|                                                                                                                                                                                              | 6   | DSPGP7_SETn_MASK  | 1       | DSP SETn GPIO7 Mask Control                                                                                                      |
|                                                                                                                                                                                              | 5   | DSPGP6_SETn_MASK  | 1       | DSP SETn GPIO6 Mask Control                                                                                                      |
|                                                                                                                                                                                              | 4   | DSPGP5_SETn_MASK  | 1       | DSP SETn GPIO5 Mask Control                                                                                                      |
|                                                                                                                                                                                              | 3   | DSPGP4_SETn_MASK  | 1       | DSP SETn GPIO4 Mask Control                                                                                                      |
|                                                                                                                                                                                              | 2   | DSPGP3_SETn_MASK  | 1       | DSP SETn GPIO3 Mask Control                                                                                                      |
|                                                                                                                                                                                              | 1   | DSPGP2_SETn_MASK  | 1       | DSP SETn GPIO2 Mask Control                                                                                                      |
|                                                                                                                                                                                              | 0   | DSPGP1_SETn_MASK  | 1       | DSP SETn GPIO1 Mask Control                                                                                                      |
| R315432 (0x4_D028)<br>DSPGP_SET1_Direction_1<br>R315464 (0x4_D048)<br>DSPGP_SET2_Direction_1<br>R315496 (0x4_D068)<br>DSPGP_SET3_Direction_1<br>R315528 (0x4_D088)<br>DSPGP_SET4_Direction_1 | 15  | DSPGP16_SETn_DIR  | 1       | DSP SETn GPIO16 Direction Control<br>0 = Output<br>1 = Input                                                                     |
|                                                                                                                                                                                              | 14  | DSPGP15_SETn_DIR  | 1       | DSP SETn GPIO15 Direction Control                                                                                                |
|                                                                                                                                                                                              | 13  | DSPGP14_SETn_DIR  | 1       | DSP SETn GPIO14 Direction Control                                                                                                |
|                                                                                                                                                                                              | 12  | DSPGP13_SETn_DIR  | 1       | DSP SETn GPIO13 Direction Control                                                                                                |
|                                                                                                                                                                                              | 11  | DSPGP12_SETn_DIR  | 1       | DSP SETn GPIO12 Direction Control                                                                                                |
|                                                                                                                                                                                              | 10  | DSPGP11_SETn_DIR  | 1       | DSP SETn GPIO11 Direction Control                                                                                                |
|                                                                                                                                                                                              | 9   | DSPGP10_SETn_DIR  | 1       | DSP SETn GPIO10 Direction Control                                                                                                |
|                                                                                                                                                                                              | 8   | DSPGP9_SETn_DIR   | 1       | DSP SETn GPIO9 Direction Control                                                                                                 |
|                                                                                                                                                                                              | 7   | DSPGP8_SETn_DIR   | 1       | DSP SETn GPIO8 Direction Control                                                                                                 |
|                                                                                                                                                                                              | 6   | DSPGP7_SETn_DIR   | 1       | DSP SETn GPIO7 Direction Control                                                                                                 |
|                                                                                                                                                                                              | 5   | DSPGP6_SETn_DIR   | 1       | DSP SETn GPIO6 Direction Control                                                                                                 |
|                                                                                                                                                                                              | 4   | DSPGP5_SETn_DIR   | 1       | DSP SETn GPIO5 Direction Control                                                                                                 |
|                                                                                                                                                                                              | 3   | DSPGP4_SETn_DIR   | 1       | DSP SETn GPIO4 Direction Control                                                                                                 |
|                                                                                                                                                                                              | 2   | DSPGP3_SETn_DIR   | 1       | DSP SETn GPIO3 Direction Control                                                                                                 |
|                                                                                                                                                                                              | 1   | DSPGP2_SETn_DIR   | 1       | DSP SETn GPIO2 Direction Control                                                                                                 |
|                                                                                                                                                                                              | 0   | DSPGP1_SETn_DIR   | 1       | DSP SETn GPIO1 Direction Control                                                                                                 |

**Table 4-34. DSP GPIO Control (Cont.)**

| Register Address                         | Bit | Label            | Default | Description                                                |
|------------------------------------------|-----|------------------|---------|------------------------------------------------------------|
| R315440 (0x4_D030)<br>DSPGP_SET1_Level_1 | 15  | DSPGP16_SETn_LVL | 0       | DSP SETn GPIO16 Output Level<br>0 = Logic 0<br>1 = Logic 1 |
| R315472 (0x4_D050)<br>DSPGP_SET2_Level_1 | 14  | DSPGP15_SETn_LVL | 0       | DSP SETn GPIO15 Output Level                               |
| R315504 (0x4_D070)<br>DSPGP_SET3_Level_1 | 13  | DSPGP14_SETn_LVL | 0       | DSP SETn GPIO14 Output Level                               |
| R315536 (0x4_D090)<br>DSPGP_SET4_Level_1 | 12  | DSPGP13_SETn_LVL | 0       | DSP SETn GPIO13 Output Level                               |
|                                          | 11  | DSPGP12_SETn_LVL | 0       | DSP SETn GPIO12 Output Level                               |
|                                          | 10  | DSPGP11_SETn_LVL | 0       | DSP SETn GPIO11 Output Level                               |
|                                          | 9   | DSPGP10_SETn_LVL | 0       | DSP SETn GPIO10 Output Level                               |
|                                          | 8   | DSPGP9_SETn_LVL  | 0       | DSP SETn GPIO9 Output Level                                |
|                                          | 7   | DSPGP8_SETn_LVL  | 0       | DSP SETn GPIO8 Output Level                                |
|                                          | 6   | DSPGP7_SETn_LVL  | 0       | DSP SETn GPIO7 Output Level                                |
|                                          | 5   | DSPGP6_SETn_LVL  | 0       | DSP SETn GPIO6 Output Level                                |
|                                          | 4   | DSPGP5_SETn_LVL  | 0       | DSP SETn GPIO5 Output Level                                |
|                                          | 3   | DSPGP4_SETn_LVL  | 0       | DSP SETn GPIO4 Output Level                                |
|                                          | 2   | DSPGP3_SETn_LVL  | 0       | DSP SETn GPIO3 Output Level                                |
|                                          | 1   | DSPGP2_SETn_LVL  | 0       | DSP SETn GPIO2 Output Level                                |
|                                          | 0   | DSPGP1_SETn_LVL  | 0       | DSP SETn GPIO1 Output Level                                |

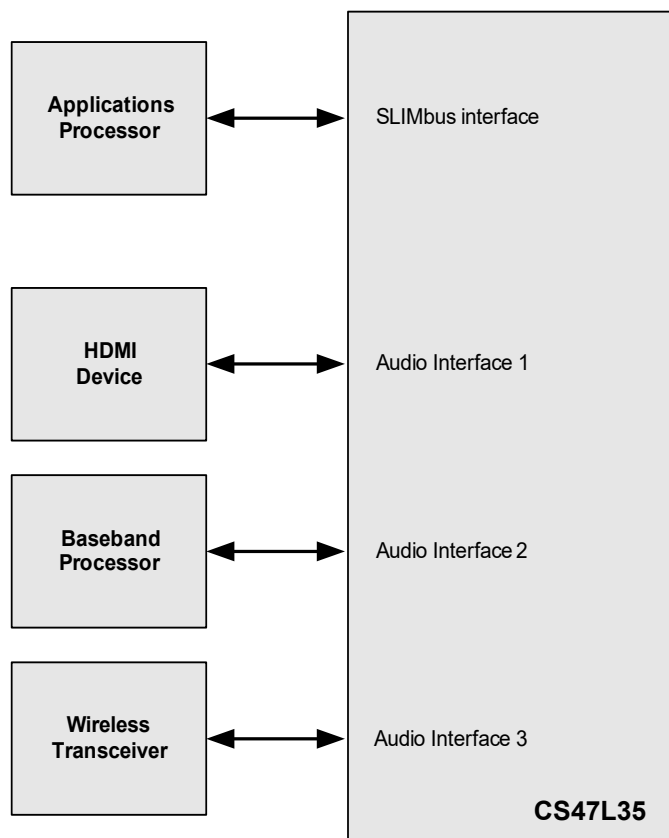
## 4.6 Digital Audio Interface

The CS47L35 provides three audio interfaces, AIF1, AIF2, and AIF3. Each of these is independently configurable on the respective transmit (TX) and receive (RX) paths. AIF1 supports up to six channels of input and output signal paths; AIF2 and AIF3 support up to two channels of input and output signal paths.

The data sources for the audio interface transmit (TX) paths can be selected from any of the CS47L35 input signal paths, or from the digital-core processing functions. The audio interface receive (RX) paths can be selected as inputs to any of the digital-core processing functions or digital-core outputs. See [Section 4.3](#) for details of the digital-core routing options.

The digital audio interfaces provide flexible connectivity for multiple processors and other audio devices. Typical connections include applications processor, baseband processor, and wireless transceiver. Note that the SLIMbus interface also provides digital audio input/output paths, providing options for additional interfaces. A typical configuration is shown in [Fig. 4-34](#).

The audio interface AIF1 is referenced to DBVDD1; interfaces AIF2 and AIF3 are referenced to DBVDD2. This enables the CS47L35 to connect easily between application subsystems on different voltage domains.



**Figure 4-34. Typical AIF Connections**

In the general case, the digital audio interface uses four pins:

- TXDAT: data output
- RXDAT: data input
- BCLK: bit clock, for synchronization
- LRCLK: left/right data-alignment clock

In Master Mode, the clock signals BCLK and LRCLK are outputs from the CS47L35. In Slave Mode, these signals are inputs, as shown in [Section 4.6.1](#).

The following interface formats are supported on AIF1–AIF3:

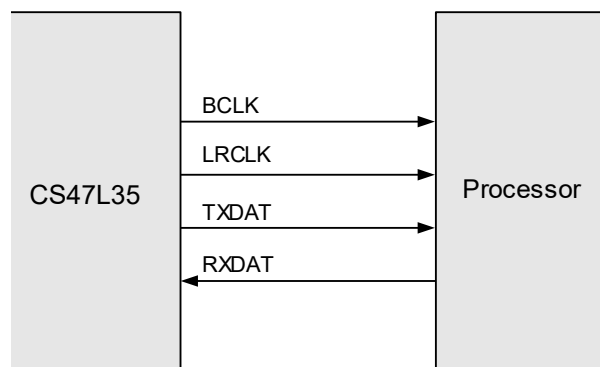
- DSP Mode A.
- DSP Mode B
- I2S
- Left-justified

The left-justified and DSP-B formats are valid in Master Mode only (i.e., BCLK and LRCLK are outputs from the CS47L35). These modes cannot be supported in Slave Mode.

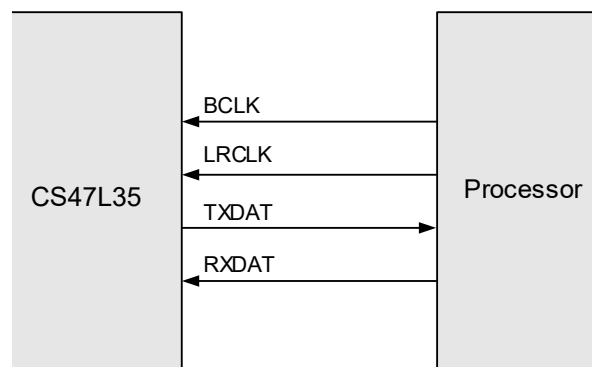
The audio interface formats are described in [Section 4.6.2](#). The bit order is MSB-first in each case; data words are encoded in 2's complement format. Mono PCM operation can be supported using the DSP modes. Refer to [Table 3-16](#) through [Table 3-18](#) for signal timing information.

### 4.6.1 Master and Slave Mode Operation

The CS47L35 digital audio interfaces can operate as a master or slave, as shown in [Fig. 4-35](#) and [Fig. 4-36](#). The associated control bits are described in [Section 4.7](#).



**Figure 4-35. Master Mode**



**Figure 4-36. Slave Mode**

### 4.6.2 Audio Data Formats

The CS47L35 digital audio interfaces can be configured to operate in I<sup>2</sup>S, left-justified, DSP-A, or DSP-B interface modes. Note that left-justified and DSP-B modes are valid in Master Mode only (i.e., BCLK and LRCLK are outputs from the CS47L35).

The digital audio interfaces also provide flexibility to support multiple slots of audio data within each LRCLK frame. This flexibility allows multiple audio channels to be supported within a single LRCLK frame.

The data formats described in this section are generic descriptions, assuming only one stereo pair of audio samples per LRCLK frame. In these cases, the AIF is configured to transmit (or receive) in the first available position in each frame (i.e., the Slot 0 position).

The options for multichannel operation are described in [Section 4.6.3](#).

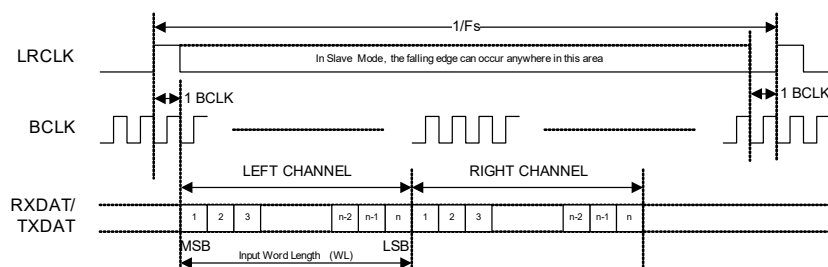
The audio data modes supported by the CS47L35 are described as follows. Note that the BCLK and LRCLK signals are configurable—the polarity of these signals can be inverted if required, and the timing of the LRCLK transition can also be adjusted. The following descriptions all assume the default configuration (noninverted polarity, normal timing) of these signals.

- In DSP modes, the left channel MSB is available on either the first (Mode B) or second (Mode A) rising edge of BCLK following a rising edge of LRCLK. Right-channel data immediately follows left channel data. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In Master Mode, the LRCLK output resembles the frame pulse shown in [Fig. 4-37](#) and [Fig. 4-38](#). In Slave Mode, it is possible to use any length of frame pulse less than 1/F<sub>s</sub>, providing the falling edge of the frame pulse occurs at least one BCLK period before the rising edge of the next frame pulse.

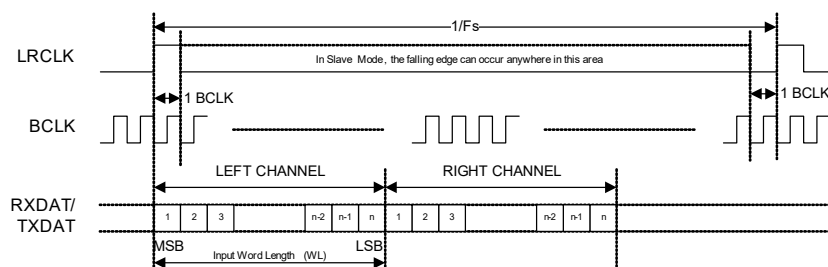
PCM operation is supported in DSP interface mode. CS47L35 data that is output on the left channel is read as mono data by the receiving equipment. Mono PCM data received by the CS47L35 is treated as left-channel data. This may be routed to the left/right playback paths using the control fields described in [Section 4.3](#).

DSP Mode A data format is shown in [Fig. 4-37](#).



**Figure 4-37. DSP Mode A Data Format**

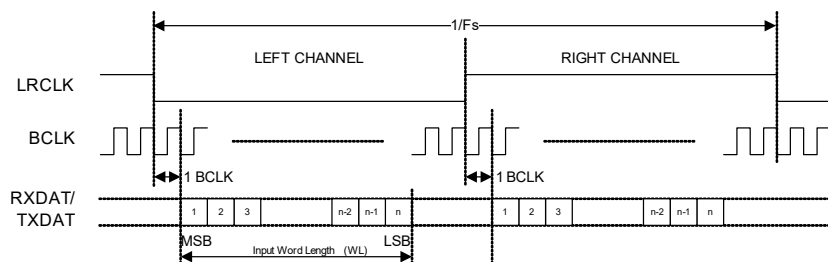
DSP Mode B data format is shown in [Fig. 4-38](#).



**Figure 4-38. DSP Mode B Data Format**

- In I<sup>2</sup>S Mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

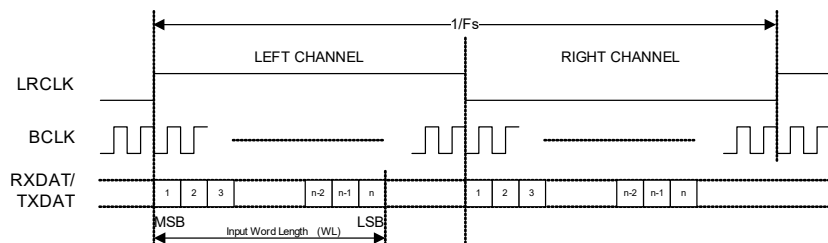
I<sup>2</sup>S Mode data format is shown in [Fig. 4-39](#).



**Figure 4-39. I<sup>2</sup>S Data Format (Assuming n-Bit Word Length)**

- In Left-Justified Mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles before each LRCLK transition.

Left-Justified Mode data format is shown in [Fig. 4-40](#).



**Figure 4-40. Left-Justified Data Format (Assuming n-Bit Word Length)**

### 4.6.3 AIF Time-Slot Configuration

Digital audio interface AIF1 supports multichannel operation, with up to six channels of input and output in each case. A high degree of flexibility is provided to define the position of the audio samples within each LRCLK frame; the audio channel samples may be arranged in any order within the frame.

AIF2 and AIF3 also provide flexible configuration options, but these interfaces support only one stereo input and one stereo output path.

Note that, on each interface, all input and output channels must operate at the same sample rate ( $F_s$ ).

Each of the audio channels can be enabled or disabled independently on the transmit (TX) and receive (RX) signal paths. For each enabled channel, the audio samples are assigned to one time slot within the LRCLK frame.

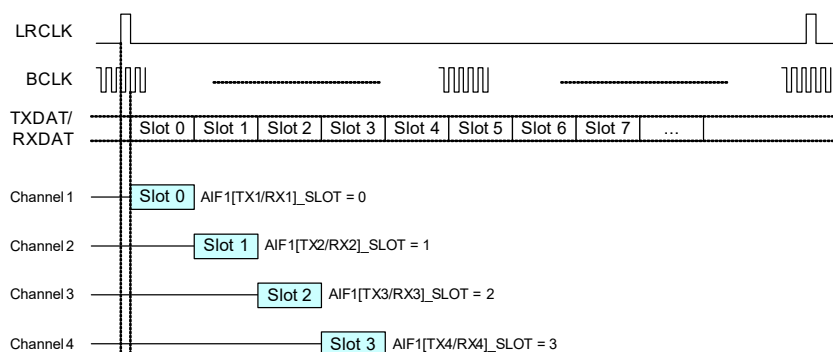
In DSP modes, the time slots are ordered consecutively from the start of the LRCLK frame. In I<sup>2</sup>S and left-justified modes, the even-numbered time slots are arranged in the first half of the LRCLK frame, and the odd-numbered time slots are arranged in the second half of the frame.

The time slots are assigned independently for the transmit (TX) and receive (RX) signal paths. There is no requirement to assign every available time slot to an audio sample; slots may be left unused, if desired. Care is required, however, to ensure that no time slot is allocated to more than one audio channel.

The number of BCLK cycles within a slot is configurable; this is the slot-length. The number of valid data bits within a slot is also configurable; this is the word length. The number of BCLK cycles per LRCLK frame must be configured; it must be ensured that there are enough BCLK cycles within each LRCLK frame to transmit or receive all of the enabled audio channels.

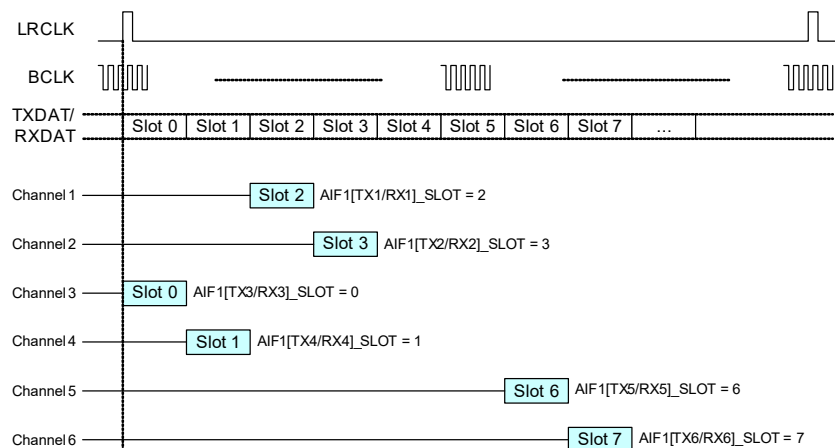
Examples of the AIF time-slot configurations are shown in Fig. 4-41 through Fig. 4-44. One example is shown for each of the four possible data formats.

Fig. 4-41 shows an example of DSP Mode A format. Four enabled audio channels are shown, allocated to time slots 0 through 3.



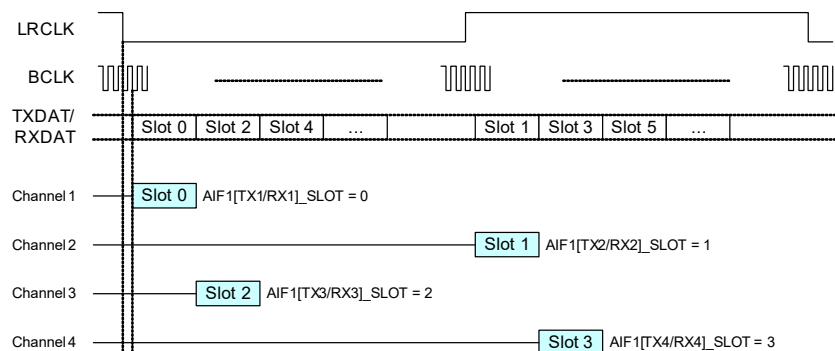
**Figure 4-41. DSP Mode A Example**

Fig. 4-42 shows an example of DSP Mode B format. Six enabled audio channels are shown, with time slots 4 and 5 unused.



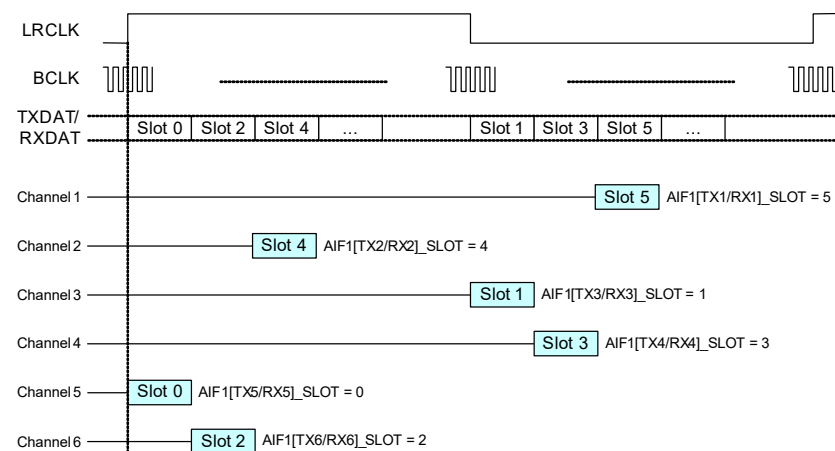
**Figure 4-42. DSP Mode B Example**

Fig. 4-43 shows an example of I<sup>2</sup>S format. Four enabled channels are shown, allocated to time slots 0 through 3.



**Figure 4-43. I<sup>2</sup>S Example**

Fig. 4-44 shows an example of left-justified format. Six enabled channels are shown.



**Figure 4-44. Left-Justified Example**

#### 4.6.4 TDM Operation Between Three or More Devices

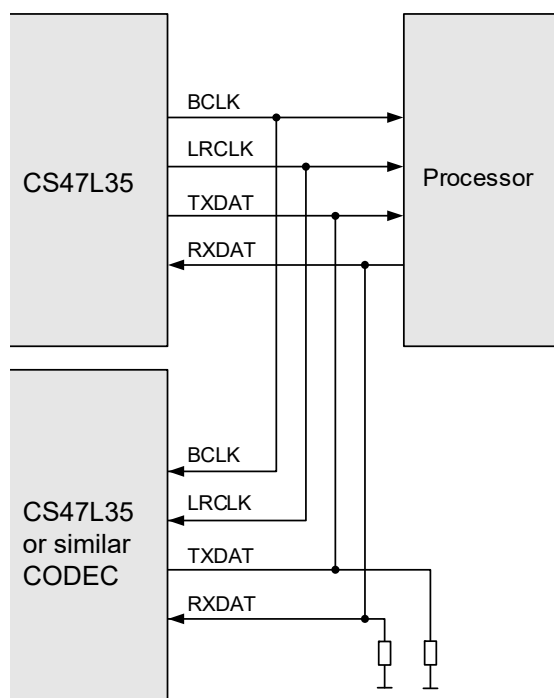
The AIF operation described in [Section 4.6.3](#) illustrates how multiple audio channels can be interleaved on a single TXDAT or RXDAT pin. The interface uses TDM to allocate time periods to each of the audio channels in turn.

This form of TDM is implemented between two devices, using the electrical connections shown [Fig. 4-35](#) or [Fig. 4-36](#).

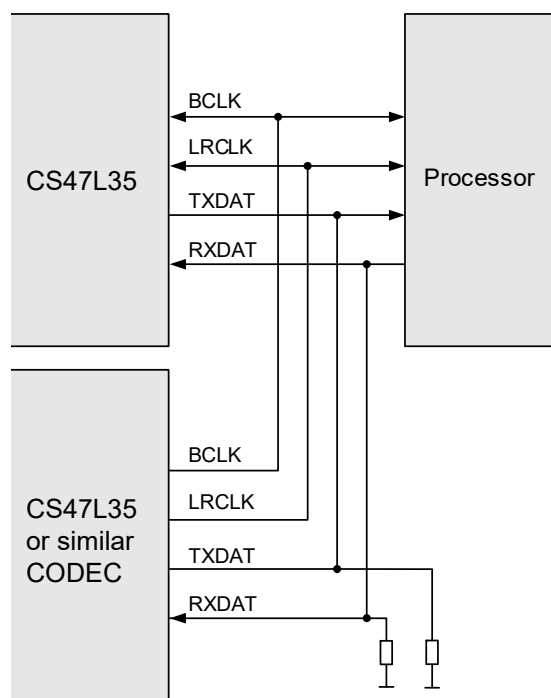
It is also possible to implement TDM between three or more devices. This allows one codec to receive audio data from two other devices simultaneously on a single audio interface, as shown in [Fig. 4-45](#), [Fig. 4-46](#), and [Fig. 4-47](#).

The CS47L35 provides full support for TDM operation. The TXDAT pin can be tristated when not transmitting data, in order to allow other devices to transmit on the same wire. The behavior of the TXDAT pin is configurable, to allow maximum flexibility to interface with other devices in this way.

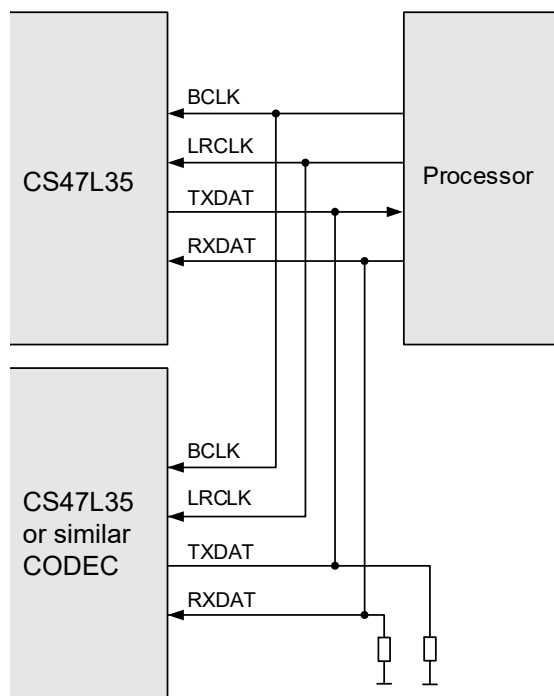
Typical configurations of TDM operation between three devices are shown in [Fig. 4-45](#), [Fig. 4-46](#), and [Fig. 4-47](#).



**Figure 4-45. TDM with CS47L35 as Master**



**Figure 4-46. TDM with Other Codec as Master**



**Figure 4-47. TDM with Processor as Master**

**Note:** The CS47L35 is a 24-bit device. If the user operates the CS47L35 in 32-Bit Mode, the 8 LSBs are ignored on the receiving side and not driven on the transmitting side. It is therefore recommended to add a pull-down resistor if necessary to the RXDAT line and the TXDAT line in TDM mode.

## 4.7 Digital Audio Interface Control

This section describes the configuration of the CS47L35 digital audio interface paths.

AIF1 supports up to six input signal paths and up to six output signal paths; AIF2 and AIF3 support up to two channels of input and output signal paths. The digital audio interfaces can be configured as master or slave interfaces; mixed master/slave configurations are also possible.

Each input and output signal path can be independently enabled or disabled. The AIF output (TX) and AIF input (RX) paths use shared BCLK and LRCLK control signals.

The digital audio interface supports flexible data formats, selectable word length, configurable time-slot allocations, and TDM tristate control.

The audio interfaces can be reconfigured while enabled, including changes to the LRCLK frame length and the channel time-slot configurations. Care is required to ensure that any on-the-fly reconfiguration does not cause corruption to the active signal paths. Wherever possible, it is recommended to disable all channels before changing the AIF configuration.

### 4.7.1 AIF Sample-Rate Control

The AIF RX inputs may be selected as input to the digital mixers or signal-processing functions within the CS47L35 digital core. The AIF TX outputs are derived from the respective output mixers.

The sample rate for each digital audio interface AIF $n$  is configured using the respective AIF $n$ \_RATE field—see [Table 4-21](#).

Note that sample-rate conversion is required when routing the AIF paths to any signal chain that is configured for a different sample rate.

### 4.7.2 AIF Pin Configuration

The external connections associated with each digital audio interface (AIF) are implemented on multi-function GPIO pins, which must be configured for the respective AIF functions when required. The AIF connections are pin-specific alternative functions available on specific GPIO pins. See [Section 4.14](#) to configure the GPIO pins for AIF operation.

Integrated pull-up and pull-down resistors can be enabled on the AIF<sub>n</sub>LRCLK, AIF<sub>n</sub>BCLK and AIF<sub>n</sub>RXDAT pins. This is provided as part of the GPIO functionality, and provides a flexible capability for interfacing with other devices. Each of the pull-up and pull-down resistors can be configured independently using the fields described in [Table 4-83](#).

If the pull-up and pull-down resistors are both enabled, the CS47L35 provides a bus keeper function on the respective pin. The bus-keeper function holds the logic level unchanged whenever the pin is undriven (e.g., if the signal is tristated).

### 4.7.3 AIF Master/Slave Control

The digital audio interfaces can operate in master or slave modes and also in mixed master/slave configurations. In Master Mode, the BCLK and LRCLK signals are generated by the CS47L35 when any of the respective digital audio interface channels is enabled. In Slave Mode, these outputs are disabled by default to allow another device to drive these pins.

Master Mode is selected on the AIF<sub>n</sub>BCLK pin by setting AIF<sub>n</sub>\_BCLK\_MSTR. In Master Mode, the AIF<sub>n</sub>BCLK signal is generated by the CS47L35 when one or more AIF<sub>n</sub> channels is enabled.

When the AIF<sub>n</sub>\_BCLK\_FRC bit is set in BCLK Master Mode, the AIF<sub>n</sub>BCLK signal is output at all times, including when none of the AIF<sub>n</sub> channels is enabled. The AIF<sub>n</sub>\_BCLK\_FRC bit should be held at 0 if SYSCLK is not enabled. SYSCLK must be present and enabled before setting the AIF<sub>n</sub>\_BCLK\_FRC bit. See [Section 4.16.4](#) for further details (including requirements for reconfiguring SYSCLK while AIF clock signals are enabled).

The AIF<sub>n</sub>BCLK signal can be inverted in master or slave modes using the AIF<sub>n</sub>\_BCLK\_INV bit.

Master Mode is selected on the AIF<sub>n</sub>LRCLK pin by setting AIF<sub>n</sub>\_LRCLK\_MSTR. In Master Mode, the AIF<sub>n</sub>LRCLK signal is generated by the CS47L35 when one or more AIF<sub>n</sub> channels is enabled.

When AIF<sub>n</sub>\_LRCLK\_FRC is set in LRCLK Master Mode, the AIF<sub>n</sub>LRCLK signal is output at all times, including when none of the AIF<sub>n</sub> channels is enabled. Note that AIF<sub>n</sub>LRCLK is derived from AIF<sub>n</sub>BCLK, and an internal or external AIF<sub>n</sub>BCLK signal must be present to generate AIF<sub>n</sub>LRCLK. The AIF<sub>n</sub>\_LRCLK\_FRC bit should be held at 0 if SYSCLK is not enabled. SYSCLK must be present and enabled before setting the AIF<sub>n</sub>\_LRCLK\_FRC bit. See [Section 4.16.4](#) for further details (including requirements for reconfiguring SYSCLK while AIF clock signals are enabled).

The AIF<sub>n</sub>LRCLK signal can be inverted in master or slave modes using the AIF<sub>n</sub>\_LRCLK\_INV bit.

The timing of the AIF<sub>n</sub>LRCLK signal is selectable using AIF<sub>n</sub>\_LRCLK\_ADV. If this bit is set, the LRCLK signal transition is advanced to the previous BCLK phase (as compared with the default behavior). Further details of this option, and conditions for valid use cases, are described in [Section 4.7.3.1](#).

The AIF1 master/slave control registers are described in [Table 4-35](#).

**Table 4-35. AIF1 Master/Slave Control**

| Register Address                 | Bit | Label          | Default | Description                                                                                          |
|----------------------------------|-----|----------------|---------|------------------------------------------------------------------------------------------------------|
| R1280 (0x0500)<br>AIF1_BCLK_Ctrl | 7   | AIF1_BCLK_INV  | 0       | AIF1 Audio Interface BCLK Invert<br>0 = AIF1BCLK not inverted<br>1 = AIF1BCLK inverted               |
|                                  | 6   | AIF1_BCLK_FRC  | 0       | AIF1 Audio Interface BCLK Output Control<br>0 = Normal<br>1 = AIF1BCLK always enabled in Master Mode |
|                                  | 5   | AIF1_BCLK_MSTR | 0       | AIF1 Audio Interface BCLK Master Select<br>0 = AIF1BCLK Slave Mode<br>1 = AIF1BCLK Master Mode       |

**Table 4-35. AIF1 Master/Slave Control (Cont.)**

| Register Address                   | Bit | Label           | Default | Description                                                                                                         |
|------------------------------------|-----|-----------------|---------|---------------------------------------------------------------------------------------------------------------------|
| R1282 (0x0502)<br>AIF1_Rx_Pin_Ctrl | 3   | AIF1_LRCLK_ADV  | 0       | AIF1 Audio Interface LRCLK Advance<br>0 = Normal<br>1 = AIF1LRCLK transition is advanced to the previous BCLK phase |
|                                    | 2   | AIF1_LRCLK_INV  | 0       | AIF1 Audio Interface LRCLK Invert<br>0 = AIF1LRCLK not inverted<br>1 = AIF1LRCLK inverted                           |
|                                    | 1   | AIF1_LRCLK_FRC  | 0       | AIF1 Audio Interface LRCLK Output Control<br>0 = Normal<br>1 = AIF1LRCLK always enabled in Master Mode              |
|                                    | 0   | AIF1_LRCLK_MSTR | 0       | AIF1 Audio Interface LRCLK Master Select<br>0 = AIF1LRCLK Slave Mode<br>1 = AIF1LRCLK Master Mode                   |

The AIF2 master/slave control registers are described in [Table 4-36](#).

**Table 4-36. AIF2 Master/Slave Control**

| Register Address                   | Bit | Label           | Default | Description                                                                                                         |
|------------------------------------|-----|-----------------|---------|---------------------------------------------------------------------------------------------------------------------|
| R1344 (0x0540)<br>AIF2_BCLK_Ctrl   | 7   | AIF2_BCLK_INV   | 0       | AIF2 Audio Interface BCLK Invert<br>0 = AIF2BCLK not inverted<br>1 = AIF2BCLK inverted                              |
|                                    | 6   | AIF2_BCLK_FRC   | 0       | AIF2 Audio Interface BCLK Output Control<br>0 = Normal<br>1 = AIF2BCLK always enabled in Master Mode                |
|                                    | 5   | AIF2_BCLK_MSTR  | 0       | AIF2 Audio Interface BCLK Master Select<br>0 = AIF2BCLK Slave Mode<br>1 = AIF2BCLK Master Mode                      |
| R1346 (0x0542)<br>AIF2_Rx_Pin_Ctrl | 3   | AIF2_LRCLK_ADV  | 0       | AIF2 Audio Interface LRCLK Advance<br>0 = Normal<br>1 = AIF2LRCLK transition is advanced to the previous BCLK phase |
|                                    | 2   | AIF2_LRCLK_INV  | 0       | AIF2 Audio Interface LRCLK Invert<br>0 = AIF2LRCLK not inverted<br>1 = AIF2LRCLK inverted                           |
|                                    | 1   | AIF2_LRCLK_FRC  | 0       | AIF2 Audio Interface LRCLK Output Control<br>0 = Normal<br>1 = AIF2LRCLK always enabled in Master Mode              |
|                                    | 0   | AIF2_LRCLK_MSTR | 0       | AIF2 Audio Interface LRCLK Master Select<br>0 = AIF2LRCLK Slave Mode<br>1 = AIF2LRCLK Master Mode                   |

The AIF3 master/slave control registers are described in [Table 4-37](#).

**Table 4-37. AIF3 Master/Slave Control**

| Register Address                 | Bit | Label          | Default | Description                                                                                          |
|----------------------------------|-----|----------------|---------|------------------------------------------------------------------------------------------------------|
| R1408 (0x0580)<br>AIF3_BCLK_Ctrl | 7   | AIF3_BCLK_INV  | 0       | AIF3 Audio Interface BCLK Invert<br>0 = AIF3BCLK not inverted<br>1 = AIF3BCLK inverted               |
|                                  | 6   | AIF3_BCLK_FRC  | 0       | AIF3 Audio Interface BCLK Output Control<br>0 = Normal<br>1 = AIF3BCLK always enabled in Master Mode |
|                                  | 5   | AIF3_BCLK_MSTR | 0       | AIF3 Audio Interface BCLK Master Select<br>0 = AIF3BCLK Slave Mode<br>1 = AIF3BCLK Master Mode       |

**Table 4-37. AIF3 Master/Slave Control (Cont.)**

| Register Address                   | Bit | Label           | Default | Description                                                                                                         |
|------------------------------------|-----|-----------------|---------|---------------------------------------------------------------------------------------------------------------------|
| R1410 (0x0582)<br>AIF3_Rx_Pin_Ctrl | 3   | AIF3_LRCLK_ADV  | 0       | AIF3 Audio Interface LRCLK Advance<br>0 = Normal<br>1 = AIF3LRCLK transition is advanced to the previous BCLK phase |
|                                    | 2   | AIF3_LRCLK_INV  | 0       | AIF3 Audio Interface LRCLK Invert<br>0 = AIF3LRCLK not inverted<br>1 = AIF3LRCLK inverted                           |
|                                    | 1   | AIF3_LRCLK_FRC  | 0       | AIF3 Audio Interface LRCLK Output Control<br>0 = Normal<br>1 = AIF3LRCLK always enabled in Master Mode              |
|                                    | 0   | AIF3_LRCLK_MSTR | 0       | AIF3 Audio Interface LRCLK Master Select<br>0 = AIF3LRCLK Slave Mode<br>1 = AIF3LRCLK Master Mode                   |

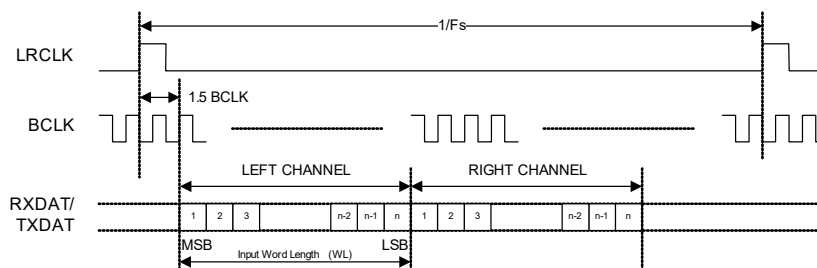
#### 4.7.3.1 LRCLK Advance

The timing of the AIF<sub>n</sub>LRCLK signal can be adjusted using AIF<sub>n</sub>\_LRCLK\_ADV. If this bit is set, the LRCLK signal transition is advanced to the previous BCLK phase (as compared with the default behavior).

The LRCLK-advance option (AIF<sub>n</sub>\_LRCLK\_ADV = 1) is valid for DSP-A mode only, operating in Master Mode.

**Note:** BCLK inversion must be enabled (AIF<sub>n</sub>\_BCLK\_INV = 1) if the LRCLK-advance option is enabled.

The adjusted interface timing (AIF<sub>n</sub>\_LRCLK\_ADV = 1), is shown in Fig. 4-48. The left-channel MSB is available on the second rising edge of BCLK, 1.5 BCLK cycles after the LRCLK rising edge—assuming the BCLK output is inverted.


**Figure 4-48. LRCLK advance—DSP-A Master Mode**

#### 4.7.4 AIF Signal Path Enable

The AIF1 interface supports up to six input (RX) channels and up to six output (TX) channels. Each channel is enabled or disabled using the bits defined in Table 4-38.

The AIF2 and AIF3 interfaces support up to two input (RX) channels and up to two output (TX) channels. Each channel is enabled or disabled using the bits defined in Table 4-39 and Table 4-40.

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The AIF signal paths should be kept disabled (AIF<sub>n</sub>\_TX<sub>m</sub>\_ENA = 0, AIF<sub>n</sub>\_RX<sub>m</sub>\_ENA = 0) if SYSCLK is not enabled. See Section 4.16 for details of the system clocks (including requirements for reconfiguring SYSCLK while audio paths are enabled).

The audio interfaces can be reconfigured if enabled, including changes to the LRCLK frame length and the channel time-slot configurations. Care is required to ensure that this on-the-fly reconfiguration does not cause corruption to the active signal paths. Wherever possible, it is recommended to disable all channels before changing the AIF configuration.

The CS47L35 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded signal paths and processing functions. If the frequency is too low, an attempt to enable an AIF signal path fails. Note that active signal paths are not affected under such circumstances.

The AIF1 signal-path-enable bits are described in [Table 4-38](#).

**Table 4-38. AIF1 Signal Path Enable**

| Register Address                  | Bit | Label       | Default | Description                                                             |
|-----------------------------------|-----|-------------|---------|-------------------------------------------------------------------------|
| R1305 (0x0519)<br>AIF1_Tx_Enables | 5   | AIF1TX6_ENA | 0       | AIF1 Audio Interface TX Channel 6 Enable<br>0 = Disabled<br>1 = Enabled |
|                                   | 4   | AIF1TX5_ENA | 0       | AIF1 Audio Interface TX Channel 5 Enable<br>0 = Disabled<br>1 = Enabled |
|                                   | 3   | AIF1TX4_ENA | 0       | AIF1 Audio Interface TX Channel 4 Enable<br>0 = Disabled<br>1 = Enabled |
|                                   | 2   | AIF1TX3_ENA | 0       | AIF1 Audio Interface TX Channel 3 Enable<br>0 = Disabled<br>1 = Enabled |
|                                   | 1   | AIF1TX2_ENA | 0       | AIF1 Audio Interface TX Channel 2 Enable<br>0 = Disabled<br>1 = Enabled |
|                                   | 0   | AIF1TX1_ENA | 0       | AIF1 Audio Interface TX Channel 1 Enable<br>0 = Disabled<br>1 = Enabled |
| R1306 (0x051A)<br>AIF1_Rx_Enables | 5   | AIF1RX6_ENA | 0       | AIF1 Audio Interface RX Channel 6 Enable<br>0 = Disabled<br>1 = Enabled |
|                                   | 4   | AIF1RX5_ENA | 0       | AIF1 Audio Interface RX Channel 5 Enable<br>0 = Disabled<br>1 = Enabled |
|                                   | 3   | AIF1RX4_ENA | 0       | AIF1 Audio Interface RX Channel 4 Enable<br>0 = Disabled<br>1 = Enabled |
|                                   | 2   | AIF1RX3_ENA | 0       | AIF1 Audio Interface RX Channel 3 Enable<br>0 = Disabled<br>1 = Enabled |
|                                   | 1   | AIF1RX2_ENA | 0       | AIF1 Audio Interface RX Channel 2 Enable<br>0 = Disabled<br>1 = Enabled |
|                                   | 0   | AIF1RX1_ENA | 0       | AIF1 Audio Interface RX Channel 1 Enable<br>0 = Disabled<br>1 = Enabled |

The AIF2 signal-path-enable bits are described in [Table 4-39](#).

**Table 4-39. AIF2 Signal Path Enable**

| Register Address                  | Bit | Label       | Default | Description                                                             |
|-----------------------------------|-----|-------------|---------|-------------------------------------------------------------------------|
| R1369 (0x0559)<br>AIF2_Tx_Enables | 1   | AIF2TX2_ENA | 0       | AIF2 Audio Interface TX Channel 2 Enable<br>0 = Disabled<br>1 = Enabled |
|                                   | 0   | AIF2TX1_ENA | 0       | AIF2 Audio Interface TX Channel 1 Enable<br>0 = Disabled<br>1 = Enabled |
| R1370 (0x055A)<br>AIF2_Rx_Enables | 1   | AIF2RX2_ENA | 0       | AIF2 Audio Interface RX Channel 2 Enable<br>0 = Disabled<br>1 = Enabled |
|                                   | 0   | AIF2RX1_ENA | 0       | AIF2 Audio Interface RX Channel 1 Enable<br>0 = Disabled<br>1 = Enabled |

The AIF3 signal-path-enable bits are described in [Table 4-40](#).

**Table 4-40. AIF3 Signal Path Enable**

| Register Address                  | Bit | Label       | Default | Description                                                             |
|-----------------------------------|-----|-------------|---------|-------------------------------------------------------------------------|
| R1433 (0x0599)<br>AIF3_Tx_Enables | 1   | AIF3TX2_ENA | 0       | AIF3 Audio Interface TX Channel 2 Enable<br>0 = Disabled<br>1 = Enabled |
|                                   | 0   | AIF3TX1_ENA | 0       | AIF3 Audio Interface TX Channel 1 Enable<br>0 = Disabled<br>1 = Enabled |
| R1434 (0x059A)<br>AIF3_Rx_Enables | 1   | AIF3RX2_ENA | 0       | AIF3 Audio Interface RX Channel 2 Enable<br>0 = Disabled<br>1 = Enabled |
|                                   | 0   | AIF3RX1_ENA | 0       | AIF3 Audio Interface RX Channel 1 Enable<br>0 = Disabled<br>1 = Enabled |

### 4.7.5 AIF BCLK and LRCLK Control

The AIF $n$ BCLK frequency is selected using the AIF $n$ \_BCLK\_FREQ field. For each setting of this field, the actual frequency depends on whether AIF $n$  is configured for a 48-kHz-related sample rate (SAMPLE\_RATE\_ $n$  = 01XXX or 10XXX) or a 44.1kHz-related sample rate (SAMPLE\_RATE\_ $n$  = 10XXX), as described in [Table 4-41](#) through [Table 4-43](#).

The selected AIF $n$ BCLK rate must be less than or equal to SYSCLK/2. See [Section 4.16](#) for details of SYSCLK clock domain, and the associated control registers.

The AIF $n$ LRCLK frequency is controlled relative to AIF $n$ BCLK by the AIF $n$ \_BCPF divider.

Note that the BCLK rate must be configured in master or slave modes, using the AIF $n$ \_BCLK\_FREQ fields. The LRCLK rates only require to be configured in Master Mode.

The AIF1 BCLK/LRCLK control fields are described in [Table 4-41](#).

**Table 4-41. AIF1 BCLK and LRCLK Control**

| Register Address                    | Bit  | Label               | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------------------------------|------|---------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1280 (0x0500)<br>AIF1_BCLK_Ctrl    | 4:0  | AIF1_BCLK_FREQ[4:0] | 0x0C    | AIF1BCLK Rate. The AIF1BCLK rate must be less than or equal to SYSCLK/2.<br>0x00–0x01 = Reserved      0x07 = 384 kHz (352.8 kHz)      0x0D = 3.072 MHz (2.8824 MHz)<br>0x02 = 64 kHz (58.8 kHz)      0x08 = 512 kHz (470.4 kHz)      0x0E = 4.096 MHz (3.7632 MHz)<br>0x03 = 96 kHz (88.2 kHz)      0x09 = 768 kHz (705.6 kHz)      0x0F = 6.144 MHz (5.6448 MHz)<br>0x04 = 128 kHz (117.6 kHz)      0x0A = 1.024 MHz (940.8 kHz)      0x10 = 8.192 MHz (7.5264 MHz)<br>0x05 = 192 kHz (176.4 kHz)      0x0B = 1.536 MHz (1.4112 MHz)      0x11 = 12.288 MHz (11.2896 MHz)<br>0x06 = 256 kHz (235.2 kHz)      0x0C = 2.048 MHz (1.8816 MHz)      0x12 = 24.576 MHz (22.5792 MHz)<br>The frequencies in brackets apply for 44.1 kHz–related sample rates only (SAMPLE_RATE_ $n$ = 01XXX). |
| R1286 (0x0506)<br>AIF1_Rx_BCLK_Rate | 12:0 | AIF1_BCPF[12:0]     | 0x0040  | AIF1LRCLK Rate. Selects the number of BCLK cycles per AIF1LRCLK frame. AIF1LRCLK clock = AIF1BCLK/AIF1_BCPF.<br>Integer (LSB = 1), Valid from 8 to 8191.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

The AIF2 BCLK/LRCLK control fields are described in [Table 4-42](#).

**Table 4-42. AIF2 BCLK and LRCLK Control**

| Register Address                       | Bit  | Label               | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|----------------------------------------|------|---------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1344<br>(0x0540)<br>AIF2_BCLK_Ctrl    | 4:0  | AIF2_BCLK_FREQ[4:0] | 0x0C    | AIF2BCLK Rate. The AIF2BCLK rate must be less than or equal to SYSCLK/2.<br>0x00–0x01 = Reserved      0x07 = 384 kHz (352.8 kHz)      0x0D = 3.072 MHz (2.8824 MHz)<br>0x02 = 64 kHz (58.8 kHz)      0x08 = 512 kHz (470.4 kHz)      0x0E = 4.096 MHz (3.7632 MHz)<br>0x03 = 96 kHz (88.2 kHz)      0x09 = 768 kHz (705.6 kHz)      0x0F = 6.144 MHz (5.6448 MHz)<br>0x04 = 128 kHz (117.6 kHz)      0x0A = 1.024 MHz (940.8 kHz)      0x10 = 8.192 MHz (7.5264 MHz)<br>0x05 = 192 kHz (176.4 kHz)      0x0B = 1.536 MHz (1.4112 MHz)      0x11 = 12.288 MHz (11.2896 MHz)<br>0x06 = 256 kHz (235.2 kHz)      0x0C = 2.048 MHz (1.8816 MHz)      0x12 = 24.576 MHz (22.5792 MHz)<br>The frequencies in brackets apply for 44.1 kHz–related sample rates only (SAMPLE_RATE_n = 01XXX). |
| R1350<br>(0x0546)<br>AIF2_Rx_BCLK_Rate | 12:0 | AIF2_BCPF[12:0]     | 0x0040  | AIF2LRCLK Rate. Selects the number of BCLK cycles per AIF2LRCLK frame. AIF2LRCLK clock = AIF2BCLK/AIF2_BCPF.<br>Integer (LSB = 1), Valid from 8 to 8191.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

The AIF3 BCLK/LRCLK control fields are described in [Table 4-43](#).

**Table 4-43. AIF3 BCLK and LRCLK Control**

| Register Address                       | Bit  | Label               | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|----------------------------------------|------|---------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1408<br>(0x0580)<br>AIF3_BCLK_Ctrl    | 4:0  | AIF3_BCLK_FREQ[4:0] | 0x0C    | AIF3BCLK Rate. The AIF3BCLK rate must be less than or equal to SYSCLK/2.<br>0x00–0x01 = Reserved      0x07 = 384 kHz (352.8 kHz)      0x0D = 3.072 MHz (2.8824 MHz)<br>0x02 = 64 kHz (58.8 kHz)      0x08 = 512 kHz (470.4 kHz)      0x0E = 4.096 MHz (3.7632 MHz)<br>0x03 = 96 kHz (88.2 kHz)      0x09 = 768 kHz (705.6 kHz)      0x0F = 6.144 MHz (5.6448 MHz)<br>0x04 = 128 kHz (117.6 kHz)      0x0A = 1.024 MHz (940.8 kHz)      0x10 = 8.192 MHz (7.5264 MHz)<br>0x05 = 192 kHz (176.4 kHz)      0x0B = 1.536 MHz (1.4112 MHz)      0x11 = 12.288 MHz (11.2896 MHz)<br>0x06 = 256 kHz (235.2 kHz)      0x0C = 2.048 MHz (1.8816 MHz)      0x12 = 24.576 MHz (22.5792 MHz)<br>The frequencies in brackets apply for 44.1 kHz–related sample rates only (SAMPLE_RATE_n = 01XXX). |
| R1414<br>(0x0586)<br>AIF3_Rx_BCLK_Rate | 12:0 | AIF3_BCPF[12:0]     | 0x0040  | AIF3LRCLK Rate. Selects the number of BCLK cycles per AIF3LRCLK frame. AIF3LRCLK clock = AIF3BCLK/AIF3_BCPF.<br>Integer (LSB = 1), Valid from 8 to 8191.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

## 4.7.6 AIF Digital Audio Data Control

The fields controlling the audio data format, word length, and slot configurations for AIF1, AIF2, and AIF3 are described in [Table 4-44](#), [Table 4-45](#), and [Table 4-46](#) respectively.

Note that left-justified and DSP-B modes are valid in Master Mode only (i.e., BCLK and LRCLK are outputs from the CS47L35).

The AIF<sub>n</sub> slot length is the number of BCLK cycles in one time slot within the overall LRCLK frame. The word length is the number of valid data bits within each time slot. If the word length is less than the slot length, there are unused BCLK cycles at the end of each time slot. The AIF<sub>n</sub> word length and slot length is independently selectable for the input (RX) and output (TX) paths.

For each AIF input (RX) and AIF output (TX) channel, the position of the audio data sample within the LRCLK frame is configurable. The x\_SLOT fields define the time-slot position of the audio sample for the associated audio channel. Valid selections are Slot 0 upwards. The time slots are numbered as shown in [Fig. 4-41](#) through [Fig. 4-44](#).

Note that, in DSP modes, the time slots are ordered consecutively from the start of the LRCLK frame. In I<sup>2</sup>S and left-justified modes, the even-numbered time slots are arranged in the first half of the LRCLK frame, and the odd-numbered time slots are arranged in the second half of the frame.

The AIF1 data control fields are described in [Table 4-44](#).

**Table 4-44. AIF1 Digital Audio Data Control**

| Register Address                       | Bit  | Label                | Default | Description                                                                                                                                     |
|----------------------------------------|------|----------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| R1284 (0x0504)<br>AIF1_Format          | 2:0  | AIF1_FMT[2:0]        | 000     | AIF1 Audio Interface Format<br>000 = DSP Mode A<br>001 = DSP Mode B<br>010 = I2S mode<br>011 = Left-Justified mode<br>Other codes are reserved. |
| R1287 (0x0507)<br>AIF1_Frame_Ctrl_1    | 13:8 | AIF1TX_WL[5:0]       | 0x18    | AIF1 TX Word Length (Number of valid data bits per slot)<br>Integer (LSB = 1); Valid from 16 to 32                                              |
|                                        | 7:0  | AIF1TX_SLOT_LEN[7:0] | 0x18    | AIF1 TX Slot Length (Number of BCLK cycles per slot)<br>Integer (LSB = 1); Valid from 16 to 128                                                 |
| R1288 (0x0508)<br>AIF1_Frame_Ctrl_2    | 13:8 | AIF1RX_WL[5:0]       | 0x18    | AIF1 RX Word Length (Number of valid data bits per slot)<br>Integer (LSB = 1); Valid from 16 to 32                                              |
|                                        | 7:0  | AIF1RX_SLOT_LEN[7:0] | 0x18    | AIF1 RX Slot Length (Number of BCLK cycles per slot)<br>Integer (LSB = 1); Valid from 16 to 128                                                 |
| R1289 (0x0509)<br>to<br>R1294 (0x050E) | 5:0  | AIF1TX1_SLOT[5:0]    | 0x0     | AIF1 TX Channel n Slot position<br>Defines the TX time slot position of the Channel n audio sample<br>Integer (LSB=1); Valid from 0 to 63       |
|                                        | 5:0  | AIF1TX2_SLOT[5:0]    | 0x1     |                                                                                                                                                 |
|                                        | 5:0  | AIF1TX3_SLOT[5:0]    | 0x2     |                                                                                                                                                 |
|                                        | 5:0  | AIF1TX4_SLOT[5:0]    | 0x3     |                                                                                                                                                 |
|                                        | 5:0  | AIF1TX5_SLOT[5:0]    | 0x4     |                                                                                                                                                 |
|                                        | 5:0  | AIF1TX6_SLOT[5:0]    | 0x5     |                                                                                                                                                 |
| R1297 (0x0511)<br>to<br>R1302 (0x0516) | 5:0  | AIF1RX1_SLOT[5:0]    | 0x0     | AIF1 RX Channel n Slot position<br>Defines the RX time slot position of the Channel n audio sample<br>Integer (LSB=1); Valid from 0 to 63       |
|                                        | 5:0  | AIF1RX2_SLOT[5:0]    | 0x1     |                                                                                                                                                 |
|                                        | 5:0  | AIF1RX3_SLOT[5:0]    | 0x2     |                                                                                                                                                 |
|                                        | 5:0  | AIF1RX4_SLOT[5:0]    | 0x3     |                                                                                                                                                 |
|                                        | 5:0  | AIF1RX5_SLOT[5:0]    | 0x4     |                                                                                                                                                 |
|                                        | 5:0  | AIF1RX6_SLOT[5:0]    | 0x5     |                                                                                                                                                 |

The AIF2 data control fields are described in [Table 4-45](#).

**Table 4-45. AIF2 Digital Audio Data Control**

| Register Address                    | Bit  | Label                | Default | Description                                                                                                                                     |
|-------------------------------------|------|----------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| R1348 (0x0544)<br>AIF2_Format       | 2:0  | AIF2_FMT[2:0]        | 000     | AIF2 Audio Interface Format<br>000 = DSP Mode A<br>001 = DSP Mode B<br>010 = I2S mode<br>011 = Left-Justified mode<br>Other codes are reserved. |
| R1351 (0x0547)<br>AIF2_Frame_Ctrl_1 | 13:8 | AIF2TX_WL[5:0]       | 0x18    | AIF2 TX Word Length<br>(Number of valid data bits per slot)<br>Integer (LSB = 1); Valid from 16 to 32                                           |
|                                     | 7:0  | AIF2TX_SLOT_LEN[7:0] | 0x18    | AIF2 TX Slot Length<br>(Number of BCLK cycles per slot)<br>Integer (LSB = 1); Valid from 16 to 128                                              |
| R1352 (0x0548)<br>AIF2_Frame_Ctrl_2 | 13:8 | AIF2RX_WL[5:0]       | 0x18    | AIF2 RX Word Length<br>(Number of valid data bits per slot)<br>Integer (LSB = 1); Valid from 16 to 32                                           |
|                                     | 7:0  | AIF2RX_SLOT_LEN[7:0] | 0x18    | AIF2 RX Slot Length<br>(Number of BCLK cycles per slot)<br>Integer (LSB = 1); Valid from 16 to 128                                              |
| R1353 (0x0549)<br>AIF2_Frame_Ctrl_3 | 5:0  | AIF2TX1_SLOT[5:0]    | 0x0     | AIF2 TX Channel 1 Slot position<br>Defines the TX time slot position of the Channel 1 audio sample<br>Integer (LSB=1); Valid from 0 to 63       |

**Table 4-45. AIF2 Digital Audio Data Control (Cont.)**

| Register Address                     | Bit | Label             | Default | Description                                                                                                                               |
|--------------------------------------|-----|-------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------|
| R1354 (0x054A)<br>AIF2_Frame_Ctrl_4  | 5:0 | AIF2TX2_SLOT[5:0] | 0x1     | AIF2 TX Channel 2 Slot position<br>Defines the TX time slot position of the Channel 2 audio sample<br>Integer (LSB=1); Valid from 0 to 63 |
| R1361 (0x0551)<br>AIF2_Frame_Ctrl_11 | 5:0 | AIF2RX1_SLOT[5:0] | 0x0     | AIF2 RX Channel 1 Slot position<br>Defines the RX time slot position of the Channel 1 audio sample<br>Integer (LSB=1); Valid from 0 to 63 |
| R1362 (0x0552)<br>AIF2_Frame_Ctrl_12 | 5:0 | AIF2RX2_SLOT[5:0] | 0x1     | AIF2 RX Channel 2 Slot position<br>Defines the RX time slot position of the Channel 2 audio sample<br>Integer (LSB=1); Valid from 0 to 63 |

The AIF3 data control fields are described in [Table 4-46](#).

**Table 4-46. AIF3 Digital Audio Data Control**

| Register Address                     | Bit  | Label                | Default | Description                                                                                                                                                  |
|--------------------------------------|------|----------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1412 (0x0584)<br>AIF3_Format        | 2:0  | AIF3_FMT[2:0]        | 000     | AIF3 Audio Interface Format<br>000 = DSP Mode A<br>001 = DSP Mode B<br>010 = I <sup>2</sup> S mode<br>011 = Left-Justified mode<br>Other codes are reserved. |
| R1415 (0x0587)<br>AIF3_Frame_Ctrl_1  | 13:8 | AIF3TX_WL[5:0]       | 0x18    | AIF3 TX Word Length (Number of valid data bits per slot)<br>Integer (LSB = 1); Valid from 16 to 32                                                           |
|                                      | 7:0  | AIF3TX_SLOT_LEN[7:0] | 0x18    | AIF3 TX Slot Length (Number of BCLK cycles per slot)<br>Integer (LSB = 1); Valid from 16 to 128                                                              |
| R1416 (0x0588)<br>AIF3_Frame_Ctrl_2  | 13:8 | AIF3RX_WL[5:0]       | 0x18    | AIF3 RX Word Length (Number of valid data bits per slot)<br>Integer (LSB = 1); Valid from 16 to 32                                                           |
|                                      | 7:0  | AIF3RX_SLOT_LEN[7:0] | 0x18    | AIF3 RX Slot Length (Number of BCLK cycles per slot)<br>Integer (LSB = 1); Valid from 16 to 128                                                              |
| R1417 (0x0589)<br>AIF3_Frame_Ctrl_3  | 5:0  | AIF3TX1_SLOT[5:0]    | 0x0     | AIF3 TX Channel 1 Slot position<br>Defines the TX time slot position of the Channel 1 audio sample<br>Integer (LSB=1); Valid from 0 to 63                    |
| R1418 (0x058A)<br>AIF3_Frame_Ctrl_4  | 5:0  | AIF3TX2_SLOT[5:0]    | 0x1     | AIF3 TX Channel 2 Slot position<br>Defines the TX time slot position of the Channel 2 audio sample<br>Integer (LSB=1); Valid from 0 to 63                    |
| R1425 (0x0591)<br>AIF3_Frame_Ctrl_11 | 5:0  | AIF3RX1_SLOT[5:0]    | 0x0     | AIF3 RX Channel 1 Slot position<br>Defines the RX time slot position of the Channel 1 audio sample<br>Integer (LSB=1); Valid from 0 to 63                    |
| R1426 (0x0592)<br>AIF3_Frame_Ctrl_12 | 5:0  | AIF3RX2_SLOT[5:0]    | 0x1     | AIF3 RX Channel 2 Slot position<br>Defines the RX time slot position of the Channel 2 audio sample<br>Integer (LSB=1); Valid from 0 to 63                    |

### 4.7.7 AIF TDM and Tristate Control

The AIF<sub>n</sub> output pins are tristated when the AIF<sub>n</sub>\_TRI bit is set. Note that this function only affects output pins configured for the respective AIF<sub>n</sub> function—a GPIO pin that is configured for a different function is not affected by AIF<sub>n</sub>\_TRI. See [Section 4.14](#) to configure the GPIO pins.

Under default conditions, the AIF<sub>n</sub>TXDAT output is held at Logic 0 when the CS47L35 is not transmitting data (i.e., during time slots that are not enabled for output by the CS47L35). If the AIF<sub>n</sub>TX\_DAT\_TRI bit is set, the CS47L35 tristates the respective AIF<sub>n</sub>TXDAT pin when not transmitting data, allowing other devices to drive the AIF<sub>n</sub>TXDAT connection.

The AIF1 TDM and tristate control fields are described in [Table 4-47](#).

**Table 4-47. AIF1 TDM and Tristate Control**

| Register Address                   | Bit | Label          | Default | Description                                                                                                                                                                       |
|------------------------------------|-----|----------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1281 (0x0501)<br>AIF1_Tx_Pin_Ctrl | 5   | AIF1TX_DAT_TRI | 0       | AIF1TXDAT Tristate Control<br>0 = Logic 0 during unused time slots<br>1 = Tristated during unused time slots                                                                      |
| R1283 (0x0503)<br>AIF1_Rate_Ctrl   | 6   | AIF1_TRI       | 0       | AIF1 Audio Interface Tristate Control<br>0 = Normal<br>1 = AIF1 Outputs are tristated<br>Note that this bit only affects output pins configured for the respective AIF1 function. |

The AIF2 TDM and tristate control fields are described in [Table 4-48](#).

**Table 4-48. AIF2 TDM and Tristate Control**

| Register Address                   | Bit | Label          | Default | Description                                                                                                                                                                       |
|------------------------------------|-----|----------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1345 (0x0541)<br>AIF2_Tx_Pin_Ctrl | 5   | AIF2TX_DAT_TRI | 0       | AIF2TXDAT Tristate Control<br>0 = Logic 0 during unused time slots<br>1 = Tristated during unused time slots                                                                      |
| R1347 (0x0543)<br>AIF2_Rate_Ctrl   | 6   | AIF2_TRI       | 0       | AIF2 Audio Interface Tristate Control<br>0 = Normal<br>1 = AIF2 Outputs are tristated<br>Note that this bit only affects output pins configured for the respective AIF2 function. |

The AIF3 TDM and tristate control fields are described in [Table 4-49](#).

**Table 4-49. AIF3 TDM and Tristate Control**

| Register Address                   | Bit | Label          | Default | Description                                                                                                                                                                       |
|------------------------------------|-----|----------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1409 (0x0581)<br>AIF3_Tx_Pin_Ctrl | 5   | AIF3TX_DAT_TRI | 0       | AIF3TXDAT Tristate Control<br>0 = Logic 0 during unused time slots<br>1 = Tristated during unused time slots                                                                      |
| R1411 (0x0583)<br>AIF3_Rate_Ctrl   | 6   | AIF3_TRI       | 0       | AIF3 Audio Interface Tristate Control<br>0 = Normal<br>1 = AIF3 Outputs are tristated<br>Note that this bit only affects output pins configured for the respective AIF3 function. |

## 4.8 SLIMbus Interface

The SLIMbus protocol is highly configurable and adaptable, supporting multiple audio signal paths, and mixed sample rates simultaneously. It also supports control messaging and associated communications between devices.

### 4.8.1 SLIMbus Devices

The SLIMbus components comprise different device classes (manager, framer, interface, generic). Each component on the bus has an interface device, which provides bus management services for the respective component. One or more components on the bus provide manager and framer device functions; the manager has the capabilities to administer the bus, although the framer is responsible for driving the CLK line and for driving the DATA required to establish the frame structure on the bus. Note that only one manager and one framer device is active at any time. The framer function can be transferred between devices when required. Generic devices provide the basic SLIMbus functionality for the associated ports, and for the transport protocol by which audio signal paths are established on the bus.

### 4.8.2 SLIMbus Frame Structure

The SLIMbus bit stream is formatted within a defined structure of cells, slots, subframes, frames, and superframes:

- A single data bit is known as a cell.
- Four cells make a slot.

- A frame consists of 192 slots.
- Eight frames make a superframe.

The bit stream structure is configurable to some extent, but the superframe definition always comprises 1536 slots. The transmitted/received bit rate can be configured according to system requirements and can be changed dynamically without interruption to active audio paths.

The SLIMbus CLK frequency (also the bus bit rate) is defined by a root frequency (RF) and a clock gear (CG). In the top clock gear (Gear 10), the CLK frequency is equal to the root frequency. Each reduction in the clock gear halves the CLK frequency, and doubles the duration of the superframe.

The SLIMbus bandwidth typically comprises control space (for bus messages, synchronization, etc.) and data space (for audio paths). The precise allocation is configurable and can be entirely control space, if required.

The subframe definition comprises the number of slots per subframe (6, 8, 24 or 32 slots) and the number of these slots per subframe allocated as control space. The applicable combination of subframe length and control space width are defined by the Subframe Mode (SM) parameter.

The SLIMbus frame always comprises 192 slots, regardless of the subframe definition. A number of slots are allocated to control space, as noted above; the remaining slots are allocated to data space. Some of the control space is required for framing information and for the guide channel (see [Section 4.8.3](#)); the remainder of the control space are allocated to the message channel.

### 4.8.3 Control Space

Framing information is provided in slots 0 and 96 of every frame. Slot 0 contains a 4-bit synchronization code; slot 96 contains the 32-bit framing information, transmitted 4 bits at a time over the eight frames that make up the SLIMbus superframe. The clock gear, root frequency, subframe configuration, along with some other parameters, are encoded within the framing information.

The guide channel occupies two slots within Frame 0. This provides the necessary information for a SLIMbus component to acquire and verify the frame synchronization. The guide channel occupies the first two control space slots within the first frame of the bit stream, excluding the framing information slots. Note that the exact slot allocation depends upon the applicable subframe mode.

The message channel is allocated all of the control space not used by the framing information or the guide channel. The message channel enables SLIMbus devices to communicate with each other, using a priority-based mechanism defined in the MIPI specification.

Messages may be broadcast to all devices on the bus, or can be addressed to specific devices using their allocated logical address (LA) or enumeration address (EA). Note that, device-specific messages are directed to a particular device (i.e., manager, framer, interface, or generic) within a component on the bus.

### 4.8.4 Data Space

The data space can be organized into a maximum of 256 data channels. Each channel, identified by a unique channel number (CN), is a stream of one or more contiguous slots, organized in a consistent data structure that repeats at a fixed interval.

A data channel is defined by its segment length (SL, number of contiguous slots allocated), segment interval (spacing between the first slots of successive segments), and segment offset (the slot number of the first allocated slot within the superframe). The segment interval and segment offset are collectively defined by a segment distribution (SD), by which the SLIMbus manager may configure or reconfigure any data channel.

Each segment may comprise TAG, AUX, and DATA portions. Any of these portions may have a length of zero; the exact composition depends on the transport protocol (TP) for the associated channel. The DATA portion must be wide enough to accommodate one full word of the data channel contents. Data words cannot be spread across multiple segments.

The segment interval for each data channel represents the minimum spacing between consecutive data samples for that channel. (Note that the minimum spacing applies if every allocated segment is populated with new data; in many cases, additional bandwidth is allocated and not every allocated segment is used.)

The segment interval gives rise to segment windows for each data channel, aligned to the start of every superframe. The segment window boundaries define the times within which each new data sample must be buffered, ready for transmission—adherence to these fixed boundaries allows slot allocations to be moved within a segment window, without altering the signal latency. The segment interval may be either shorter or longer than the frame length, but there is always an integer number of segment windows per superframe.

The TP defines the flow control or handshaking method used by the ports associated with a data channel. The applicable flow control modes depend on the relationship between the audio sample rate (flow rate) and the SLIMbus CLK frequency. If the two rates are synchronized and integer related, no flow control is needed. In other cases, the flow may be regulated by the use of a presence bit, which can be set by the source device (pushed protocol), or by the sink device (pulled protocol).

The data-channel structure is defined in terms of the TP, SD, and SL parameters.

The data-channel content definition includes a presence rate (PR) parameter (describing the nominal sample rate for the audio channel) and a frequency locked (FL) bit (identifying whether the data source is synchronized to the SLIMbus CLK). The data length (DL) parameter defines the size of each data sample (number of slots). The auxiliary bits format (AF) and data type (DT) parameters provide support for non-PCM encoded data channels; the channel link (CL) parameter is an indicator that channel CN is related to the previous channel, CN-1.

For a given root frequency and clock gear, the SL and SD parameters define the amount of SLIMbus bandwidth that is allocated to a given data channel. The minimum bandwidth requirements of a data channel are represented by the presence rate (PR) and data length (DL) parameters. The allocated SLIMbus bandwidth must be equal to or greater than the bandwidth of the data to be transferred.

The segment interval defines the repetition rate of the SLIMbus slots allocated to consecutive data samples for a given data channel. The presence rate (PR) is the nominal sample rate of the audio path. The segment rate (determined by the segment interval value) must be equal to or greater than the presence rate for a given data channel. The following constraints must be observed when configuring a SLIMbus channel:

- If pushed or pulled transport protocol is selected, the segment rate must be greater than the presence rate to ensure that samples are not dropped as a result of clock drift.
- If isochronous transport protocol is selected, the segment rate must be equal to the presence rate. Isochronous transport protocol should be selected only if the data source is frequency locked to the SLIMbus CLK (i.e., the data source is synchronized to the SLIMbus framer device).

## 4.9 SLIMbus Control Sequences

This section describes the messages and general protocol associated with the SLIMbus system.

**Note:** The SLIMbus specification permits flexibility in core message support for different components. See [Section 4.10](#) for details regarding which messages are supported on each of the SLIMbus devices present on the CS47L35.

### 4.9.1 Device Management and Configuration

This section describes the SLIMbus messages associated with configuring all devices on the SLIMbus interface.

When the SLIMbus interface starts up, it is required that only one component provides the manager and framer device functions. Other devices can request connection to the bus after they have gained synchronization.

The REPORT\_PRESENT (DC, DCV) message may be issued by devices attempting to connect to the bus. The payload of this message contains the device class (DC) and device class version (DCV) parameters, describing the type of device that is attempting to connect. This message may be issued autonomously by the connecting device, or else in response to a REQUEST\_SELF\_ANNOUNCEMENT message from the manager device.

After positively acknowledging the REPORT\_PRESENT message, the manager device then issues the ASSIGN\_LOGICAL\_ADDRESS (LA) message to allow the other device to connect to the bus. The payload of this message contains the logical address (LA) parameter only; this is the unique address by which the connected device sends and receives SLIMbus messages. The device is then said to be enumerated.

Once a device has been successfully connected to the bus, the logical address (LA) parameter can be changed at any time using the CHANGE\_LOGICAL\_ADDRESS (LA) message.

The RESET\_DEVICE message commands an individual SLIMbus device to perform its reset procedure. As part of the reset, all associated ports are reset, and any associated data channels are canceled. Note that, if the RESET\_DEVICE command is issued to an interface device, it causes a component reset (i.e., all devices within the associated component are reset). Under a component reset, every associated device releases its logical address, and the component becomes disconnected from the bus.

## 4.9.2 Information Management

A memory map of information elements is defined for each device. This is arranged in 3 x 1-kB blocks, comprising core value elements, device class-specific value elements, and user value elements respectively, as described in the MIPI specification. Note that the contents of the user information portion for each CS47L35 SLIMbus device are reserved.

Read/write access is implemented using the messages described as follows. Specific elements within the information map are identified using the element code (EC) parameter. In the case of read access, a unique transaction ID (TID) is assigned to each message relating to a particular read/write request.

- The REQUEST\_INFORMATION (TID, EC) message is used to instruct a device to respond with the indicated information. The payload of this message contains the transaction ID (TID) and the element code (EC).
- The REQUEST\_CLEAR\_INFORMATION (TID, EC, CM) message is used to instruct a device to respond with the indicated information, and also to clear all, or parts, of the same information slice. The payload of this message contains the transaction ID (TID), element code (EC), and clear mask (CM). The clear mask field is used to select which elements are to be cleared as part of the instruction.
- The REPLY\_INFORMATION (TID, IS) message is used to provide output of a requested parameter. The payload of this message contains the transaction ID (TID) and the information slice (IS). The information slice bytes contain the value of the requested parameter.
- The CLEAR\_INFORMATION (EC, CM) message is used to clear all, or parts, of the indicated information slice. The payload of this message contains the element code (EC) and clear mask (CM). The clear mask field is used to select which elements are to be cleared as part of the instruction.
- The REPORT\_INFORMATION (EC, IS) message is used to inform other devices about a change in a specified element in the information map. The payload of this message contains the element code (EC) and the information slice (IS). The information slice bytes contain the new value of the applicable parameter.

## 4.9.3 Value Management (Including Register Access)

A memory map of value elements is defined for each device. This is arranged in 3 x 1-kB blocks, comprising core value elements, device class-specific value elements, and user value elements respectively, as described in the MIPI specification. These elements are typically parameters used to configure device behavior.

The user value elements of the interface device are used on CS47L35 to support read/write access to the register map. Details of how to access specific registers are described in [Section 4.10](#).

Note that, with the exception of the user value elements of the interface device, the contents of the user value portion for each CS47L35 SLIMbus device are reserved.

Read/write access is implemented using the messages described as follows. Specific elements within the value map are identified using the element code (EC) parameter. In the case of read access, a unique transaction ID (TID) is assigned to each message relating to a particular read/write request.

- The REQUEST\_VALUE (TID, EC) message is used to instruct a device to respond with the indicated information. The payload of this message contains the transaction ID (TID) and the element code (EC).
- The REPLY\_VALUE (TID, VS) message is used to provide output of a requested parameter. The payload of this message contains the transaction ID (TID) and the value slice (VS). The value slice bytes contain the value of the requested parameter.

- The CHANGE\_VALUE (EC, VU) message is used to write data to a specified element in the value map. The payload of this message contains the element code (EC) and the value update (VU). The value update bytes contain the new value of the applicable parameter.

#### 4.9.4 Frame and Clocking Management

This section describes the SLIMbus messages associated with changing the frame or clocking configuration. One or more configuration messages may be issued as part of a reconfiguration sequence; all of the updated parameters become active at once, when the reconfiguration boundary is reached.

- The BEGIN\_RECONFIGURATION message is issued to define a reconfiguration boundary point: subsequent NEXT\_\* messages become active at the first valid superframe boundary following receipt of the RECONFIGURE\_NOW message. (A valid boundary must be at least two slots after the end of the RECONFIGURE\_NOW message.) Both of these messages have no payload content.
- The NEXT\_ACTIVE\_FRAMER (LAIF, NCo, NCi) message is used to select a new device as the active framer. The payload of this message includes the logical address, incoming framer (LAIF). Two other fields (NCo, NCi) define the number of clock cycles for which the CLK line shall be inactive during the handover.
- The NEXT\_SUBFRAME\_MODE (SM) and NEXT\_CLOCK\_GEAR (CG) messages are used to reconfigure the SLIMbus clocking or framing definition. The payload of each is the respective subframe mode (SM) or clock gear (CG) respectively.
- The NEXT\_PAUSE\_CLOCK (RT) message instructs the active framer to pause the bus. The payload of the message contains the restart time (RT), which indicates whether the interruption is to be of a specified time and/or phase duration.
- The NEXT\_RESET\_BUS message instructs all components on the bus to be reset. In this case, all devices on the bus are reset and are disconnected from the bus. Subsequent reconnection to the bus follows the same process as when the bus is first initialized.
- The NEXT\_SHUTDOWN\_BUS message instructs all devices that the bus is to be shut down.

#### 4.9.5 Data Channel Configuration

This section describes the SLIMbus messages associated with configuring a SLIMbus data channel. Note that the manager device is responsible for allocating the available bandwidth as required for each data channel.

- The CONNECT\_SOURCE (PN, CN) and CONNECT\_SINK (PN, CN) messages are issued to the respective devices, defining the ports between which a data channel is to be established. Note that multiple destinations (sinks) can be configured for a channel, if required. The payload of each message contains the port number (PN) and the channel number (CN) parameters.
- The BEGIN\_RECONFIGURATION message is issued to define a Reconfiguration Boundary point: subsequent NEXT\_\* messages become active at the first valid superframe boundary following receipt of the RECONFIGURE\_NOW message. A valid boundary must be at least two slots after the end of the RECONFIGURE\_NOW message.
- The NEXT\_DEFINE\_CHANNEL (CN, TP, SD, SL) message informs the associated devices of the structure of the data channel. The payload of this message contains the channel number (CN), TP, SD, and SL parameters for the data channel.
- The NEXT\_DEFINE\_CONTENT (CN, FL, PR, AF, DT, CL, DL), or CHANGE\_CONTENT (CN, FL, PR, AF, DT, CL, DL) message provides more detailed information about the data channel contents. The payload of this message contains the channel number (CN), frequency locked (FL), presence rate (PR), auxiliary bits format (AF), data type (DT), channel link (CL), and data length (DL) parameters.
- The NEXT\_ACTIVATE\_CHANNEL (CN) message instructs the channel to be activated at the next reconfiguration boundary. The payload of this message contains the channel number (CN) only.
- The RECONFIGURE\_NOW message completes the reconfiguration sequence, causing all of the NEXT\_\* messages since the BEGIN\_RECONFIGURATION to become active at the next valid superframe boundary. (A valid boundary must be at least two slots after the end of the RECONFIGURE\_NOW message.)

- Active channels can be reconfigured using the CHANGE\_CONTENT, NEXT\_DEFINE\_CONTENT, or NEXT\_DEFINE\_CHANNEL messages. Note that these changes can be effected without interrupting the data channel; the NEXT\_DEFINE\_CHANNEL, for example, may be used to change a segment distribution, in order to reallocate the SLIMbus bandwidth.
- An active channel can be paused using the NEXT\_DEACTIVATE\_CHANNEL message and reinstated using the NEXT\_ACTIVATE\_CHANNEL message.
- Data channels can be disconnected using the DISCONNECT\_PORT or NEXT\_REMOVE\_CHANNEL messages. These messages provide equivalent functionality, but use different parameters (PN or CN respectively) to identify the affected signal path.

## 4.10 SLIMbus Interface Control

The CS47L35 features a MIPI-compliant SLIMbus interface, providing six channels of audio input and six channels of audio output. Mixed audio sample rates are supported on the SLIMbus interface. The SLIMbus interface also supports read/write access to the CS47L35 control registers.

The SLIMbus interface on CS47L35 comprises a generic device and an interface device. A maximum of 12 ports can be configured, providing up to six input (RX) channels and up to six output (TX) channels.

The audio paths associated with the SLIMbus interface are described in [Section 4.3](#).

The SLIMbus interface supports read/write access to the CS47L35 control registers, as described in [Section 4.10.6](#).

The SLIMbus clocking rate and channel allocations are controlled by the manager device. The message channel and data channel bandwidth may be dynamically adjusted according to the application requirements. Note that the manager device functions are not implemented on the CS47L35, and these bandwidth allocation requirements are outside the scope of this data sheet.

### 4.10.1 SLIMbus Device Parameters

The SLIMbus interface on the CS47L35 comprises two devices. The enumeration address of each device within the SLIMbus interface is derived from the parameters noted in [Table 4-50](#).

**Table 4-50. SLIMbus Device Parameters**

| Description | Manufacturer ID | Product Code | Device ID | Instance Value | Enumeration Address |
|-------------|-----------------|--------------|-----------|----------------|---------------------|
| Generic     | 0x01FA          | 0x6360       | 0x00      | 0x00           | 01FA_6360_0000      |
| Interface   | 0x01FA          | 0x6360       | 0x7F      | 0x00           | 01FA_6360_7F00      |

### 4.10.2 SLIMbus Message Support

The SLIMbus interface on the CS47L35 supports bus messages as noted in [Table 4-51](#).

Additional notes regarding SLIMbus message support are noted below, and also in [Table 4-52](#).

**Table 4-51. SLIMbus Message Support**

| Category                         | Message Code MC[6:0] | Description                                 | Generic | Interface |
|----------------------------------|----------------------|---------------------------------------------|---------|-----------|
| Device Management Messages       | 0x01                 | REPORT_PRESENT (DC, DCV)                    | S       | S         |
|                                  | 0x02                 | ASSIGN_LOGICAL_ADDRESS (LA)                 | D       | D         |
|                                  | 0x04                 | RESET_DEVICE ()                             | D       | D         |
|                                  | 0x08                 | CHANGE_LOGICAL_ADDRESS (LA)                 | D       | D         |
|                                  | 0x09                 | CHANGE_ARBITRATION_PRIORITY (AP)            | —       | —         |
|                                  | 0x0C                 | REQUEST_SELF_ANNOUNCEMENT ()                | D       | D         |
|                                  | 0x0F                 | REPORT_ABSENT ()                            | —       | —         |
| Data Channel Management Messages | 0x10                 | CONNECT_SOURCE (PN, CN)                     | D       | —         |
|                                  | 0x11                 | CONNECT_SINK (PN, CN)                       | D       | —         |
|                                  | 0x14                 | DISCONNECT_PORT (PN)                        | D       | —         |
|                                  | 0x18                 | CHANGE_CONTENT (CN, FL, PR, AF, DT, CL, DL) | D       | —         |

**Table 4-51. SLIMbus Message Support (Cont.)**

| Category                        | Message Code MC[6:0] | Description                                      | Generic | Interface |
|---------------------------------|----------------------|--------------------------------------------------|---------|-----------|
| Information Management Messages | 0x20                 | REQUEST_INFORMATION (TID, EC)                    | D       | D         |
|                                 | 0x21                 | REQUEST_CLEAR_INFORMATION (TID, EC, CM)          | D       | D         |
|                                 | 0x24                 | REPLY_INFORMATION (TID, IS)                      | S       | S         |
|                                 | 0x28                 | CLEAR_INFORMATION (EC, CM)                       | D       | D         |
|                                 | 0x29                 | REPORT_INFORMATION (EC, IS)                      | —       | S         |
| Reconfiguration Messages        | 0x40                 | BEGIN_RECONFIGURATION ()                         | D       | D         |
|                                 | 0x44                 | NEXT_ACTIVE_FRAMER (LAIF, NCo, NCi)              | —       | —         |
|                                 | 0x45                 | NEXT_SUBFRAME_MODE (SM)                          | —       | D         |
|                                 | 0x46                 | NEXT_CLOCK_GEAR (CG)                             | —       | —         |
|                                 | 0x47                 | NEXT_ROOT_FREQUENCY (RF)                         | —       | —         |
|                                 | 0x4A                 | NEXT_PAUSE_CLOCK (RT)                            | —       | —         |
|                                 | 0x4B                 | NEXT_RESET_BUS ()                                | —       | —         |
|                                 | 0x4C                 | NEXT_SHUTDOWN_BUS ()                             | —       | —         |
|                                 | 0x50                 | NEXT_DEFINE_CHANNEL (CN, TP, SD, SL)             | D       | —         |
|                                 | 0x51                 | NEXT_DEFINE_CONTENT (CN, FL, PR, AF, DT, CL, DL) | D       | —         |
|                                 | 0x54                 | NEXT_ACTIVATE_CHANNEL (CN)                       | D       | —         |
|                                 | 0x55                 | NEXT_DEACTIVATE_CHANNEL (CN)                     | D       | —         |
|                                 | 0x58                 | NEXT_REMOVE_CHANNEL (CN)                         | D       | —         |
|                                 | 0x5F                 | RECONFIGURE_NOW ()                               | D       | D         |
|                                 | 0x60                 | REQUEST_VALUE (TID, EC)                          | —       | D         |
| Value Management Messages       | 0x61                 | REQUEST_CHANGE_VALUE (TID, EC, VU)               | —       | —         |
|                                 | 0x64                 | REPLY_VALUE (TID, VS)                            | —       | S         |
|                                 | 0x68                 | CHANGE_VALUE (EC, VU)                            | —       | D         |

**Notes:**

- S = Supported as a source device only.
- D = Supported as a destination device only.

The CS47L35 SLIMbus component must be reset prior to scheduling a hardware reset or power-on reset. This can be achieved using the RESET\_DEVICE message (issued to the CS47L35 interface device), or else using the NEXT\_RESET\_BUS message.

**Table 4-52. SLIMbus Parameter Support**

| Parameter Code | Description                            | Comments                                                                                                                                                                                                                                                               |
|----------------|----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AF             | Auxiliary Bits Format                  | —                                                                                                                                                                                                                                                                      |
| CG             | Clock Gear                             | —                                                                                                                                                                                                                                                                      |
| CL             | Channel Link                           | —                                                                                                                                                                                                                                                                      |
| CM             | Clear Mask                             | CS47L35 does not fully support this function. The CM bytes of the REQUEST_CLEAR_INFORMATION or CLEAR_INFORMATION messages must not be sent to CS47L35 Devices. When either of these messages is received, all bits within the specified Information Slice are cleared. |
| CN             | Channel Number                         | —                                                                                                                                                                                                                                                                      |
| DC             | Device Class                           | —                                                                                                                                                                                                                                                                      |
| DCV            | Device Class Variation                 | —                                                                                                                                                                                                                                                                      |
| DL             | Data Length                            | —                                                                                                                                                                                                                                                                      |
| DT             | Data Type                              | CS47L35 supports the following DT codes:<br>0x0 = Not indicated<br>0x1 = LPCM audio<br>Note that 2's complement PCM can be supported with DT = 0x0.                                                                                                                    |
| EC             | Element Code                           | —                                                                                                                                                                                                                                                                      |
| FL             | Frequency Locked                       | —                                                                                                                                                                                                                                                                      |
| IS             | Information Slice                      | —                                                                                                                                                                                                                                                                      |
| LA             | Logical Address                        | —                                                                                                                                                                                                                                                                      |
| LAIF           | Logical Address, Incoming Framer       | —                                                                                                                                                                                                                                                                      |
| NCi            | Number of Incoming Framer Clock Cycles | —                                                                                                                                                                                                                                                                      |
| NCo            | Number of Outgoing Framer Clock Cycles | —                                                                                                                                                                                                                                                                      |
| PN             | Port Number                            | Note that the Port Numbers of the CS47L35 SLIMbus paths are register-configurable, as described in <a href="#">Table 4-53</a> .                                                                                                                                        |

**Table 4-52. SLIMbus Parameter Support (Cont.)**

| Parameter Code | Description          | Comments                                                                                                                                                                                                                           |
|----------------|----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PR             | Presence Rate        | Note that the Presence Rate must be the same as the sample rate selected for the associated CS47L35 SLIMbus path.                                                                                                                  |
| RF             | Root Frequency       | —                                                                                                                                                                                                                                  |
| RT             | Restart Time         | CS47L35 supports the following RT codes:<br>0x0 = Fast Recovery<br>0x2 = Unspecified Delay<br>When either of these values is specified, the CS47L35 resumes toggling the CLK line within four cycles of the CLK line frequency.    |
| SD             | Segment Distribution | Note that any data channels that are assigned the same SAMPLE_RATE_ <i>n</i> value must also be assigned the same Segment Interval.                                                                                                |
| SL             | Segment Length       | —                                                                                                                                                                                                                                  |
| SM             | Subframe Mode        | —                                                                                                                                                                                                                                  |
| TID            | Transaction ID       | —                                                                                                                                                                                                                                  |
| TP             | Transport Protocol   | CS47L35 supports the following TP codes for TX channels:<br>0x0 = Isochronous Protocol<br>0x1 = Pushed Protocol<br>CS47L35 supports the following TP codes for RX channels:<br>0x0 = Isochronous Protocol<br>0x2 = Pulled Protocol |
| VS             | Value Slice          | —                                                                                                                                                                                                                                  |
| VU             | Value Update         | —                                                                                                                                                                                                                                  |

### 4.10.3 SLIMbus Port Number Control

The CS47L35 SLIMbus interface supports up to six input (RX) channels and up to six output (TX) channels. The SLIMbus port numbers for these audio channels are configurable using the fields described in [Table 4-53](#).

**Table 4-53. SLIMbus Port Number Control**

| Register Address  | Bit  | Label                  | Default | Description                                                |
|-------------------|------|------------------------|---------|------------------------------------------------------------|
| R1490 (0x05D2)    | 13:8 | SLIMRX2_PORT_ADDR[5:0] | 1       | SLIMbus RX Channel <i>n</i> Port number<br>Valid from 0–31 |
| SLIMbus_RX_Ports0 | 5:0  | SLIMRX1_PORT_ADDR[5:0] | 0       |                                                            |
| R1491 (0x05D3)    | 13:8 | SLIMRX4_PORT_ADDR[5:0] | 3       |                                                            |
| SLIMbus_RX_Ports1 | 5:0  | SLIMRX3_PORT_ADDR[5:0] | 2       |                                                            |
| R1492 (0x05D4)    | 13:8 | SLIMRX6_PORT_ADDR[5:0] | 5       |                                                            |
| SLIMbus_RX_Ports2 | 5:0  | SLIMRX5_PORT_ADDR[5:0] | 4       |                                                            |
| R1494 (0x05D6)    | 13:8 | SLIMTX2_PORT_ADDR[5:0] | 9       | SLIMbus TX Channel <i>n</i> Port number<br>Valid from 0–31 |
| SLIMbus_TX_Ports0 | 5:0  | SLIMTX1_PORT_ADDR[5:0] | 8       |                                                            |
| R1495 (0x05D7)    | 13:8 | SLIMTX4_PORT_ADDR[5:0] | 11      |                                                            |
| SLIMbus_TX_Ports1 | 5:0  | SLIMTX3_PORT_ADDR[5:0] | 10      |                                                            |
| R1496 (0x05D8)    | 13:8 | SLIMTX6_PORT_ADDR[5:0] | 13      |                                                            |
| SLIMbus_TX_Ports2 | 5:0  | SLIMTX5_PORT_ADDR[5:0] | 12      |                                                            |

### 4.10.4 SLIMbus Sample-Rate Control

The SLIMbus RX inputs may be selected as input to the digital mixers or signal-processing functions within the CS47L35 digital core. The SLIMbus TX outputs are derived from the respective output mixers.

The sample rate for each SLIMbus channel is configured using SLIMRX<sub>*n*</sub>\_RATE and SLIMTX<sub>*n*</sub>\_RATE—see [Table 4-21](#) within the [Digital Core](#) section.

Sample-rate conversion is required when routing the SLIMbus paths to any signal chain that is configured for a different sample rate.

### 4.10.5 SLIMbus Signal Path Enable

The SLIMbus interface supports up to six input (RX) channels and up to six output (TX) channels. Each of these channels can be enabled or disabled using the fields defined in [Table 4-54](#).

**Note:** SLIMbus audio channels can be supported only when the corresponding ports have been enabled by the manager device (i.e., in addition to setting the respective enable bits). The status bits in Registers R1527 and R1528 indicate the status of each of the SLIMbus ports.

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The SLIMbus audio paths should be kept disabled (SLIMRX $n$ \_ENA = 0, SLIMTX $n$ \_ENA = 0) if SYSCLK is not enabled. See [Section 4.16](#) for details of the system clocks (including requirements for reconfiguring SYSCLK while audio paths are enabled).

**Table 4-54. SLIMbus Signal Path Enable**

| Register Address                                | Bit | Label            | Default | Description                                                                                  |
|-------------------------------------------------|-----|------------------|---------|----------------------------------------------------------------------------------------------|
| R1525 (0x05F5)<br>SLIMbus_RX_<br>Channel_Enable | 5   | SLIMRX6_ENA      | 0       | SLIMbus RX Channel n Enable<br>0 = Disabled<br>1 = Enabled                                   |
|                                                 | 4   | SLIMRX5_ENA      | 0       |                                                                                              |
|                                                 | 3   | SLIMRX4_ENA      | 0       |                                                                                              |
|                                                 | 2   | SLIMRX3_ENA      | 0       |                                                                                              |
|                                                 | 1   | SLIMRX2_ENA      | 0       |                                                                                              |
|                                                 | 0   | SLIMRX1_ENA      | 0       |                                                                                              |
| R1526 (0x05F6)<br>SLIMbus_TX_<br>Channel_Enable | 5   | SLIMTX6_ENA      | 0       | SLIMbus TX Channel n Enable<br>0 = Disabled<br>1 = Enabled                                   |
|                                                 | 4   | SLIMTX5_ENA      | 0       |                                                                                              |
|                                                 | 3   | SLIMTX4_ENA      | 0       |                                                                                              |
|                                                 | 2   | SLIMTX3_ENA      | 0       |                                                                                              |
|                                                 | 1   | SLIMTX2_ENA      | 0       |                                                                                              |
|                                                 | 0   | SLIMTX1_ENA      | 0       |                                                                                              |
| R1527 (0x05F7)<br>SLIMbus_RX_<br>Port_Status    | 5   | SLIMRX6_PORT_STS | 0       | SLIMbus RX Channel n Port Status<br>(Read only)<br>0 = Disabled<br>1 = Configured and active |
|                                                 | 4   | SLIMRX5_PORT_STS | 0       |                                                                                              |
|                                                 | 3   | SLIMRX4_PORT_STS | 0       |                                                                                              |
|                                                 | 2   | SLIMRX3_PORT_STS | 0       |                                                                                              |
|                                                 | 1   | SLIMRX2_PORT_STS | 0       |                                                                                              |
|                                                 | 0   | SLIMRX1_PORT_STS | 0       |                                                                                              |
| R1528 (0x05F8)<br>SLIMbus_TX_<br>Port_Status    | 5   | SLIMTX6_PORT_STS | 0       | SLIMbus TX Channel n Port Status<br>(Read only)<br>0 = Disabled<br>1 = Configured and active |
|                                                 | 4   | SLIMTX5_PORT_STS | 0       |                                                                                              |
|                                                 | 3   | SLIMTX4_PORT_STS | 0       |                                                                                              |
|                                                 | 2   | SLIMTX3_PORT_STS | 0       |                                                                                              |
|                                                 | 1   | SLIMTX2_PORT_STS | 0       |                                                                                              |
|                                                 | 0   | SLIMTX1_PORT_STS | 0       |                                                                                              |

#### 4.10.6 SLIMbus Control Register Access

Control register access is supported via the SLIMbus interface. Full read/write access to all registers is possible, via the user value elements portion of the value map.

If the SLIMbus interface is used to access the DSP firmware memory registers, a system clocking constraint must be observed: the DSPCLK frequency, if enabled, must be greater than 1.3 x RF, where RF is the SLIMbus root frequency. Note that, if DSPCLK is disabled (DSP\_CLK\_ENA = 0), or if accessing other areas of the register map, the timing constraint is not applicable. See [Section 4.4](#) for details of the DSP Firmware memory. See [Section 4.16](#) for details of the DSPCLK signal.

Register write operations are implemented using the CHANGE\_VALUE message. A maximum of two messages may be required, depending on circumstances: the first CHANGE\_VALUE message selects the register page (bits [23:8] of the control register address); the second message contains the data and bits [7:0] of the register address. The first message may be omitted if the register page is unchanged from the previous read or write operation.

The required SLIMbus parameters are described in [Table 4-55](#) and [Table 4-56](#), for the generic case of writing the value 0xVVVV to control register address 0xYYYYZZ. Note that it is also possible to write blocks of up to 16 bytes (to consecutive register addresses), as described below.

**Table 4-55. Register Write Message (1)—CHANGE\_VALUE**

| Parameter           | Value  | Description                                                                                                                                                   |
|---------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Source Address      | 0xSS   | SS is the 8-bit logical address of the message source. This could be any active device on the bus, but is typically the manager device (0xFF).                |
| Destination Address | 0xLL   | LL is the 8-bit logical address of the message destination (i.e., the CS47L35 SLIMbus interface device). The value is assigned by the SLIMbus manager device. |
| Access Mode         | 0b1    | Selects byte-based access mode.                                                                                                                               |
| Byte Address        | 0x800  | Identifies the user value element for selecting the control register page address.                                                                            |
| Slice Size          | 0b001  | Selects 2-byte slice size                                                                                                                                     |
| Value Update        | 0xYYYY | YYYY is bits [23:8] of the applicable control register address.                                                                                               |

**Table 4-56. Register Write Message (2)—CHANGE\_VALUE**

| Parameter           | Value  | Description                                                                                                                                                   |
|---------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Source Address      | 0xSS   | SS is the 8-bit logical address of the message source. This could be any active device on the bus, but is typically the manager device (0xFF).                |
| Destination Address | 0xLL   | LL is the 8-bit logical address of the message destination (i.e., the CS47L35 SLIMbus interface device). The value is assigned by the SLIMbus manager device. |
| Access Mode         | 0b1    | Selects byte-based access mode.                                                                                                                               |
| Byte Address        | 0xUUU  | Specifies the value map address, calculated as $0xA00 + (2 \times 0xZZ)$ , where ZZ is bits [7:0] of the applicable control register address.                 |
| Slice Size          | 0b001  | Selects 2-byte slice size                                                                                                                                     |
| Value Update        | 0xVVVV | VVVV is the 16-bit data to be written.                                                                                                                        |

**Note:** The first message may be omitted if its contents are unchanged from the previous CHANGE\_VALUE message sent to the CS47L35.

Write transfers of up to 16 bytes can be configured using the slice size parameter in the second message (see [Table 4-56](#)). Additional value update words can be appended to the message in this case, with the applicable data contents. For compatibility with the CS47L35 register map, the selected number of bytes must always be an even number.

When a 2-byte transfer is selected, these bytes are written to the register address 0xYYYYZZ (using the same naming conventions as above). When more than 2 bytes are written in a single transfer, the destination register address is automatically incremented as described in [Table 4-57](#).

**Table 4-57. SLIMbus Register Write Sequence—16-Bit Register Space (< 0x3000)**

| Register Address (<0x3000) | Byte Sequence          |
|----------------------------|------------------------|
| Base Address (0xYYYYZZ)    | Bytes 2 and 1 (0xVVVV) |
| Base address + 1           | Bytes 4 and 3          |
| Base address + 2           | Bytes 6 and 5          |
| Base address + 3           | Bytes 8 and 7          |
| Base address + 4           | Bytes 10 and 9         |
| Base address + 5           | Bytes 12 and 11        |
| Base address + 6           | Bytes 14 and 13        |
| Base address + 7           | Bytes 16 and 15        |

**Note:** Register addresses from R12288 (0x3000) upwards are formatted as 32-bit words. When writing to these addresses, the slice size should be a multiple of 4 bytes and the byte address should be aligned with the 32-bit data word boundaries (i.e., an even number). The byte ordering for these register addresses is described in [Table 4-58](#).

**Table 4-58. SLIMbus Register Write Sequence—32-Bit Register Space (≥ 0x3000)**

| Register Address (≥0x3000) | Byte Sequence        |
|----------------------------|----------------------|
| Base Address (0xYYYYZZ)    | Bytes 4, 3, 2, 1     |
| Base address + 2           | Bytes 8, 7, 6, 5     |
| Base Address + 4           | Bytes 12, 11, 10, 9  |
| Base Address + 6           | Bytes 16, 15, 14, 13 |

Register read operations are implemented using the CHANGE\_VALUE and REQUEST\_VALUE messages. A maximum of two messages may be required, depending on circumstances: the CHANGE\_VALUE message selects the register page (bits [23:8] of the control register address); the REQUEST\_VALUE message contains bits [7:0] of the register address. The first message may be omitted if the register page is unchanged from the previous read or write operation.

The required SLIMbus parameters are described in [Table 4-59](#) and [Table 4-60](#), for the generic case of reading the contents of control register address 0xYYYYZZ.

**Table 4-59. Register Read Message (1)—CHANGE\_VALUE**

| Parameter           | Value  | Description                                                                                                                                                   |
|---------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Source Address      | 0xSS   | SS is the 8-bit logical address of the message source. This could be any active device on the bus, but is typically the manager device (0xFF).                |
| Destination Address | 0xLL   | LL is the 8-bit logical address of the message destination (i.e., the CS47L35 SLIMbus interface device). The value is assigned by the SLIMbus manager device. |
| Access Mode         | 0b1    | Selects byte-based access mode.                                                                                                                               |
| Byte Address        | 0x800  | Identifies the user value element for selecting the control register page address.                                                                            |
| Slice Size          | 0b001  | Selects 2-byte slice size                                                                                                                                     |
| Value Update        | 0xYYYY | YYYY is bits [23:8] of the applicable control register address.                                                                                               |

The CS47L35 SLIMbus interface supports register read operations of 2 bytes (i.e., one 16-bit data word) only. Register addresses from R12288 (0x3000) upwards are formatted as 32-bit words; when reading from these addresses, the 2-byte data slice represents the 2 lower bytes of the selected 32-bit word. The 2 upper bytes of the respective register can be accessed by adding '2' to the Byte Address value described in [Table 4-60](#).

**Table 4-60. Register Read Message (2)—REQUEST\_VALUE**

| Parameter           | Value  | Description                                                                                                                                                   |
|---------------------|--------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Source Address      | 0xSS   | SS is the 8-bit logical address of the message source. This could be any active device on the bus, but is typically the manager device (0xFF).                |
| Destination Address | 0xLL   | LL is the 8-bit logical address of the message destination (i.e., the CS47L35 SLIMbus interface device). The value is assigned by the SLIMbus manager device. |
| Access Mode         | 0b1    | Selects byte-based access mode.                                                                                                                               |
| Byte Address        | 0xUUU  | Specifies the value map address, calculated as $0xA00 + (2 \times 0xZZ)$ , where ZZ is bits [7:0] of the applicable control register address.                 |
| Slice Size          | 0b001  | Selects 2-byte slice size                                                                                                                                     |
| Transaction ID      | 0xTTTT | TTTT is the 16-bit transaction ID for the message. The value is assigned by the SLIMbus manager device.                                                       |

**Note:** The first message may be omitted if its contents are unchanged from the previous CHANGE\_VALUE message sent to the CS47L35.

The CS47L35 responds to the register read commands in accordance with the normal SLIMbus protocols.

Note that the CS47L35 assumes that sufficient control space slots are available in which to provide its response before the next REQUEST\_VALUE message is received. The CS47L35 response is made using a REPLY\_VALUE message; the SLIMbus manager should wait until the REPLY\_VALUE message has been received before sending the next REQUEST\_VALUE message. If additional REQUEST\_VALUE messages are received before the CS47L35 response has been made, the earlier REQUEST\_VALUE messages are ignored (i.e., only the last REQUEST\_VALUE message is serviced).

### 4.10.7 SLIMbus Clocking Control

The clock frequency of the SLIMbus interface is not fixed, and may be set according to the application requirements. The clock frequency can be reconfigured dynamically as required.

The CS47L35 SLIMbus interface does not include a framer device. Accordingly, the SLIMCLK pin is always an input pin on the CS47L35. The framer function can be transferred from one device to another; this is known as framer handover, and is controlled by the manager device.

The supported root frequencies are as defined in the MIPI Alliance specification for SLIMbus.

Under normal operating conditions, the SLIMbus interface operates with a fixed root frequency (RF); dynamic updates to the bus rate are applied using a selectable clock gear (CG) function. The root frequency and the clock gear setting are controlled by the manager device; these parameters are transmitted in every SLIMbus superframe to all devices on the bus.

In Gear 10 (the highest clock gear setting), the SLIMCLK input frequency is equal to the root frequency. In lower gears, the SLIMCLK frequency is reduced by increasing powers of 2.

The clock gear definition is shown in [Table 4-61](#).

**Note:** The 24.576-MHz root frequency is an example only; other frequencies are also supported.

**Table 4-61. SLIMbus Clock Gear Selection**

| Clock Gear | Description   | SLIMCLK Frequency <sup>1</sup> |
|------------|---------------|--------------------------------|
| 10         | Divide by 1   | 24.576 MHz                     |
| 9          | Divide by 2   | 12.288 MHz                     |
| 8          | Divide by 4   | 6.144 MHz                      |
| 7          | Divide by 8   | 3.072 MHz                      |
| 6          | Divide by 16  | 1.536 MHz                      |
| 5          | Divide by 32  | 768 kHz                        |
| 4          | Divide by 64  | 384 kHz                        |
| 3          | Divide by 128 | 192 kHz                        |
| 2          | Divide by 256 | 96 kHz                         |
| 1          | Divide by 512 | 48 kHz                         |

1. Assuming 24.576-MHz root frequency

The SLIMCLK input can be used to provide a reference source for the FLL. The frequency of this reference is controlled using SLIMCLK\_REF\_GEAR, as described in [Table 4-62](#).

The input clock reference for the FLL is selected by using FLL1\_REFCLK\_SRC. If SLIMbus is selected as the clock source, the reference signal is generated using an adaptive divider on the SLIMCLK input. The divider automatically adapts to the SLIMbus clock gear (CG). If the clock gear on the bus is lower than the SLIMCLK\_REF\_GEAR, the selected reference frequency cannot be supported, and the SLIMbus clock reference is disabled.

See [Section 4.16](#) for details of system clocking and the FLL.

**Table 4-62. SLIMbus Clock Reference Control**

| Register Address                              | Bit | Label                     | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----------------------------------------------|-----|---------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1507 (0x05E3)<br>SLIMbus_Framer_<br>Ref_Gear | 3:0 | SLIMCLK_REF_<br>GEAR[3:0] | 0x0     | SLIMbus Clock Reference control. Sets the SLIMbus reference clock relative to the SLIMbus Root Frequency (RF).<br>0x0 = Clock stopped    0x4 = Gear 4. (RF/64)    0x8 = Gear 8. (RF/4)<br>0x1 = Gear 1. (RF/512)    0x5 = Gear 5. (RF/32)    0x9 = Gear 9. (RF/2)<br>0x2 = Gear 2. (RF/256)    0x6 = Gear 6. (RF/16)    0xA = Gear 10. (RF)<br>0x3 = Gear 3. (RF/128)    0x7 = Gear 7. (RF/8)    All other codes are reserved |

## 4.11 Output Signal Path

The CS47L35 provides three audio output signal paths. These outputs comprise ground-referenced headphone/earpiece drivers, differential speaker driver, and a digital output interface suitable for external speaker drivers. The output signal paths are summarized in [Table 4-63](#).

**Table 4-63. Output Signal Path Summary**

| Signal Path  | Descriptions                                | Output Pins                      |
|--------------|---------------------------------------------|----------------------------------|
| OUT1L, OUT1R | Ground-referenced headphone/earpiece output | HPOUTL, HPOUTR or EPOUTP, EPOUTN |
| OUT4L        | Differential speaker output                 | SPKOUTN, SPKOUTP                 |
| OUT5L, OUT5R | Digital speaker (PDM) output                | SPKDAT, SPKCLK                   |

The analog output paths incorporate high performance 24-bit sigma-delta DACs.

The headphone/earpiece output path is configurable as a stereo headphone driver (HPOUTL and HPOUTR pins), or as a differential earpiece driver (EPOUTP and EPOUTN pins). The ground-referenced headphone output path incorporates a common mode feedback path for rejection of system-related noise. The headphone and earpiece outputs each support direct connection to external loads, with no requirement for AC coupling capacitors.

The speaker output path is configured to drive a differential (BTL) output. The Class D design offers high efficiency at large signal levels. With a suitable choice of external speaker, the Class D output can drive a loudspeaker directly, without any additional filter components.

The digital output path provides a stereo pulse-density modulation (PDM) output interface, for connection to external audio devices. A total of two digital output channels are provided.

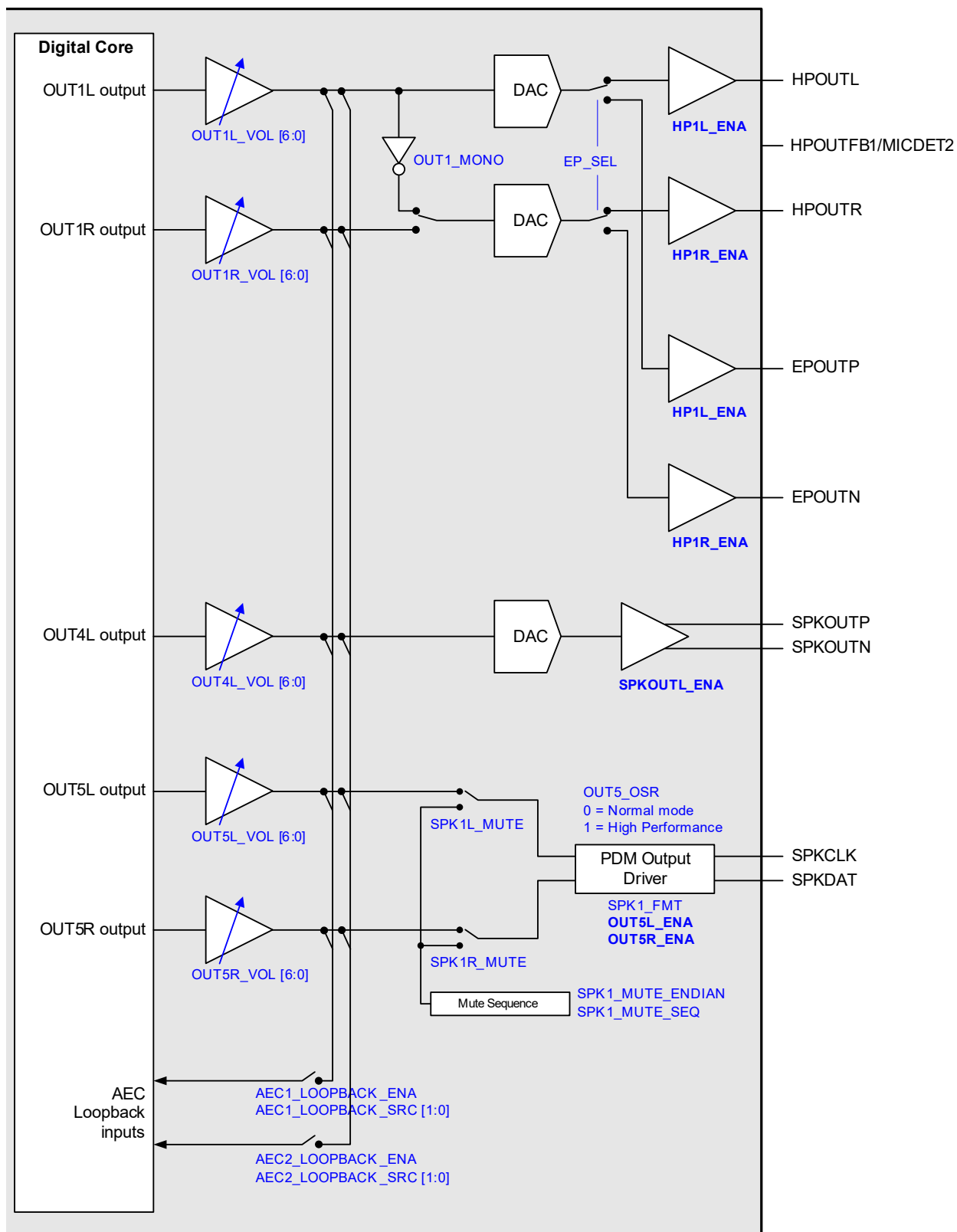
Digital volume control is available on all outputs (analog and digital), with programmable ramp control for smooth, glitch-free operation. A configurable noise-gate function is available on each of the output signal paths. Any two of the output signal paths may be selected as input to the AEC loop-back paths.

The CS47L35 incorporates thermal protection functions, and provides short-circuit detection on the Class D speaker and headphone/earpiece output paths. The general-purpose timers (see [Section 4.5.3](#)) can also be used as a watchdog function, to trigger a shutdown of the Class D speaker drivers; see [Section 4.21](#).

The Class D speaker output is designed to support monitoring of external loudspeakers, giving real-time feedback for algorithms such as Cirrus Logic's speaker-protection software, running on one of the DSP cores. This enables loudspeakers to be protected against damage from excessive signal levels and other electro-mechanical constraints. This feature requires additional external component connections, as described in [Section 4.11.8](#).

The CS47L35 output signal paths are shown in [Fig. 4-49](#).

The OUT2, OUT3, and OUT4R paths are not implemented on this device.



**Figure 4-49. Output Signal Paths**

### 4.11.1 Output Signal Path Enable

The output signal paths are enabled using the bits described in [Table 4-64](#). The respective bits must be enabled for analog or digital output on the respective output paths.

The OUT1 path is associated with the headphone and the earpiece output drivers. The HP1L\_ENA and HP1R\_ENA bits control either the HPOUT or EPOUT drivers, depending on the EP\_SEL register bit selection. See [Table 4-66](#) for details of the EP\_SEL register.

The output signal paths are muted by default. It is recommended that deselecting the mute should be the final step of the path enable control sequence. Similarly, the mute should be selected as the first step of the path disable control sequence. The output signal path mute functions are controlled using the bits described in [Table 4-64](#).

The supply rails for the OUT1 outputs (HPOUT and EPOUT) are generated using an integrated dual-mode charge pump, CP1. The charge pump is enabled automatically by the CS47L35 when required by the output drivers; see [Section 4.19](#).

The CS47L35 schedules a pop-suppressed control sequence to enable or disable the OUT1 and OUT4L signal paths. This is automatically managed by the control-write sequencer in response to setting the respective HPnX\_ENA or SPKOUTL\_ENA bits; see [Section 4.18](#) for further details.

The output signal path enable/disable control sequences are inputs to the interrupt circuit and can be used to trigger an interrupt event when a sequence completes; see [Section 4.15](#).

The system clock, SYSCLK, must be configured and enabled before any audio path is enabled. The output signal paths should be kept disabled (HP1x\_ENA = 0, SPKOUTL\_ENA = 0, OUT5x\_ENA = 0) if SYSCLK is not enabled. See [Section 4.16](#) for details of the system clocks (including requirements for reconfiguring SYSCLK while audio paths are enabled).

The CS47L35 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the output signal paths and associated DACs. If the frequency is too low, an attempt to enable an output signal path fails. Note that active signal paths are not affected under such circumstances.

The status bits in Register R1025 and R1030 indicate the status of each of the output signal paths. If an underclocked error condition occurs, these bits indicate which signal paths have been enabled.

**Table 4-64. Output Signal Path Enable**

| Register Address                   | Bit | Label       | Default | Description                                                                                                                                                                                 |
|------------------------------------|-----|-------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1024 (0x0400)<br>Output_Enables_1 | 9   | OUT5L_ENA   | 0       | Output Path 5 (left) enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                  |
|                                    | 8   | OUT5R_ENA   | 0       | Output Path 5 (right) enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                 |
|                                    | 7   | SPKOUTL_ENA | 0       | Output Path 4 (left) enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                  |
|                                    | 1   | HP1L_ENA    | 0       | Output Path 1 (left) enable<br>When EP_SEL = 0, this bit controls the HPOUTL output driver.<br>When EP_SEL = 1, this bit controls the EPOUTP output driver.<br>0 = Disabled<br>1 = Enabled  |
|                                    | 0   | HP1R_ENA    | 0       | Output Path 1 (right) enable<br>When EP_SEL = 0, this bit controls the HPOUTR output driver.<br>When EP_SEL = 1, this bit controls the EPOUTN output driver.<br>0 = Disabled<br>1 = Enabled |

**Table 4-64. Output Signal Path Enable (Cont.)**

| Register Address                      | Bit | Label         | Default | Description                                                        |
|---------------------------------------|-----|---------------|---------|--------------------------------------------------------------------|
| R1025 (0x0401)<br>Output_Status_1     | 9   | OUT5L_ENA_STS | 0       | Output Path 5 (left) enable status<br>0 = Disabled<br>1 = Enabled  |
|                                       | 8   | OUT5R_ENA_STS | 0       | Output Path 5 (right) enable status<br>0 = Disabled<br>1 = Enabled |
|                                       | 7   | OUT4L_ENA_STS | 0       | Output Path 4 (left) enable status<br>0 = Disabled<br>1 = Enabled  |
| R1030 (0x0406)<br>Raw_Output_Status_1 | 1   | OUT1L_ENA_STS | 0       | Output Path 1 (left) enable status<br>0 = Disabled<br>1 = Enabled  |
|                                       | 0   | OUT1R_ENA_STS | 0       | Output Path 1 (right) enable status<br>0 = Disabled<br>1 = Enabled |

### 4.11.2 Output Signal Path Sample-Rate Control

The output signal paths are derived from the respective output mixers within the CS47L35 digital core. The sample rate for the output signal paths is configured using OUT\_RATE—see [Table 4-21](#).

Note that sample-rate conversion is required when routing the output signal paths to any signal chain that is configured for a different sample rate.

### 4.11.3 Output Signal Path Control

The OUT1 path is associated with the headphone and the earpiece output drivers. The EP\_SEL bit controls which of these outputs can be used—it is not possible to enable the headphone and earpiece drivers simultaneously.

Under default register conditions, the OUT1 path is configured for stereo output. The path can be configured for mono differential (BTL) output using the OUT1\_MONO bit; this is ideal for driving an earpiece or hearing aid coil.

When the OUT1\_MONO bit is set, the respective right channel output is an inverted copy of the left channel output signal; this creates a differential output between the respective outputs. The left and right channel output drivers must both be enabled in Mono Mode; both channels should be enabled simultaneously using the fields described in [Table 4-64](#).

The mono (BTL) signal paths are shown in [Fig. 4-49](#). Note that, in Mono Mode, the effective gain of the signal path is increased by 6 dB.

For stereo output on HPOUTL and HPOUTR, the required settings are as follows:

- EP\_SEL = 0
- OUT1\_MONO = 0

For mono differential output on EPOUTP and EPOUTN, the required settings are as follows:

- EP\_SEL = 1
- OUT1\_MONO = 1

Note that the EP\_SEL and OUT1\_MONO bits should not be changed while the headphone or earpiece drivers are enabled. These bits should be configured before enabling the respective drivers, and should remain unchanged until after the drivers have been disabled. The HPOUT and EPOUT drivers are enabled using the HP1L\_ENA and HP1R\_ENA bits, as described in [Table 4-64](#).

The SPKCLK frequency of the PDM output path (OUT5) is controlled by OUT5\_OSR, as described in [Table 4-65](#). When the OUT5\_OSR bit is set, the audio performance is improved, but power consumption is also increased.

Note that the SPKCLK frequencies noted in [Table 4-65](#) assume that the SYSCLK frequency is a multiple of 6.144 MHz (SYSCLK\_FRAC=0). If the SYSCLK frequency is a multiple of 5.6448 MHz (SYSCLK\_FRAC = 1), the SPKCLK frequency is scaled accordingly.

**Table 4-65. SPKCLK Frequency**

| Condition    | SPKCLK Frequency |
|--------------|------------------|
| OUT5_OSR = 0 | 3.072 MHz        |
| OUT5_OSR = 1 | 6.144 MHz        |

The output signal path control registers are defined in [Table 4-66](#).

**Table 4-66. Output Signal Path Control**

| Register Address                            | Bit | Label     | Default | Description                                                                                                                                                                                         |
|---------------------------------------------|-----|-----------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1024 (0x0400)<br>Output_Enables_1          | 15  | EP_SEL    | 0       | Output Path 1 Output Driver select<br>0 = HPOUTL and HPOUTR<br>1 = EPOUTP and EPOUTN                                                                                                                |
| R1040 (0x0410)<br>Output_Path_<br>Config_1L | 12  | OUT1_MONO | 0       | Output Path 1 Mono Mode (Configures HPOUT and EPOUT as a mono differential output.)<br>0 = Disabled<br>1 = Enabled<br>The gain of the signal path is increased by 6 dB in differential (mono) mode. |
| R1072 (0x0430)<br>Output_Path_<br>Config_5L | 13  | OUT5_OSR  | 0       | Output Path 5 Oversample Rate<br>0 = Normal mode<br>1 = High Performance mode                                                                                                                       |

#### 4.11.4 Output Signal Path Digital Volume Control

A digital volume control is provided on each of the output signal paths, providing –64 to +31.5 dB gain control in 0.5-dB steps. An independent mute control is also provided for each output signal path.

Whenever the gain or mute setting is changed, the signal path gain is ramped up or down to the new settings at a programmable rate. For increasing gain (or unmute), the rate is controlled by OUT\_VI\_RAMP. For decreasing gain (or mute), the rate is controlled by OUT\_VD\_RAMP.

**Note:** The OUT\_VI\_RAMP and OUT\_VD\_RAMP fields should not be changed while a volume ramp is in progress.

The OUT\_VU bits control the loading of the output signal path digital volume and mute controls. When OUT\_VU is cleared, the digital volume and mute settings are loaded into the respective control register, but does not actually change the signal path gain. The digital volume and mute settings on all of the output signal paths are updated when a 1 is written to OUT\_VU. This makes it possible to update the gain of multiple signal paths simultaneously.

Note that, although the digital-volume controls provide 0.5-dB steps, the internal circuits provide signal gain adjustment in 0.125-dB steps. This allows a very high degree of gain control—smooth volume ramping under all operating conditions.

**Note:** The 0 dBFS level of the OUT5 digital output path is not equal to the 0 dBFS level of the CS47L35 digital core. The maximum digital output level is –6 dBFS (see [Table 3-8](#)). Under 0 dB gain conditions, a 0 dBFS output from the digital core corresponds to a –6 dBFS level in the PDM output.

The digital volume control registers are described in [Table 4-67](#) and [Table 4-68](#).

**Table 4-67. Output Signal Path Digital Volume Control**

| Register Address                            | Bit | Label            | Default        | Description                                                                                                                                                                                                                                                                                                                                    |
|---------------------------------------------|-----|------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1033 (0x0409)<br>Output_Volume_<br>Ramp    | 6:4 | OUT_VD_RAMP[2:0] | 010            | Output Volume Decreasing Ramp Rate (seconds/6 dB)<br>This field should not be changed while a volume ramp is in progress.<br>000 = 0 ms                      011 = 2 ms                      110 = 15 ms<br>001 = 0.5 ms                      100 = 4 ms                      111 = 30 ms<br>010 = 1 ms                      101 = 8 ms        |
|                                             | 2:0 | OUT_VI_RAMP[2:0] | 010            | Output Volume Increasing Ramp Rate (seconds/6 dB)<br>This field should not be changed while a volume ramp is in progress.<br>000 = 0 ms                      011 = 2 ms                      110 = 15 ms<br>001 = 0.5 ms                      100 = 4 ms                      111 = 30 ms<br>010 = 1 ms                      101 = 8 ms        |
| R1041 (0x0411)<br>DAC_Digital_<br>Volume_1L | 9   | OUT_VU           | See Footnote 1 | Output Signal Paths Volume Update. Writing 1 to this bit causes the Output Signal Paths Volume and Mute settings to be updated simultaneously                                                                                                                                                                                                  |
|                                             | 8   | OUT1L_MUTE       | 1              | Output Path 1 (Left) Digital Mute<br>0 = Unmute<br>1 = Mute                                                                                                                                                                                                                                                                                    |
|                                             | 7:0 | OUT1L_VOL[7:0]   | 0x80           | Output Path 1 (Left) Digital Volume (see Table 4-68 for volume register definition).<br>–64 dB to +31.5 dB in 0.5-dB steps<br>0x00 = –64dB                      0x80 = 0 dB                      0xC0 to 0xFF = Reserved<br>0x01 = –63.5dB                      ... (0.5-dB steps)<br>... (0.5-dB steps)                      0xBF = +31.5 dB  |
| R1045 (0x0415)<br>DAC_Digital_<br>Volume_1R | 9   | OUT_VU           | See Footnote 1 | Output Signal Paths Volume Update. Writing 1 to this bit causes the Output Signal Paths Volume and Mute settings to be updated simultaneously                                                                                                                                                                                                  |
|                                             | 8   | OUT1R_MUTE       | 1              | Output Path 1 (Right) Digital Mute<br>0 = Unmute<br>1 = Mute                                                                                                                                                                                                                                                                                   |
|                                             | 7:0 | OUT1R_VOL[7:0]   | 0x80           | Output Path 1 (Right) Digital Volume (see Table 4-68 for volume register definition).<br>–64 dB to +31.5 dB in 0.5-dB steps<br>0x00 = –64dB                      0x80 = 0 dB                      0xC0 to 0xFF = Reserved<br>0x01 = –63.5dB                      ... (0.5-dB steps)<br>... (0.5-dB steps)                      0xBF = +31.5 dB |
| R1065 (0x0429)<br>DAC_Digital_<br>Volume_4L | 9   | OUT_VU           | See Footnote 1 | Output Signal Paths Volume Update. Writing 1 to this bit causes the Output Signal Paths Volume and Mute settings to be updated simultaneously                                                                                                                                                                                                  |
|                                             | 8   | OUT4L_MUTE       | 1              | Output Path 4 (Left) Digital Mute<br>0 = Unmute<br>1 = Mute                                                                                                                                                                                                                                                                                    |
|                                             | 7:0 | OUT4L_VOL[7:0]   | 0x80           | Output Path 4 (Left) Digital Volume (see Table 4-68 for volume register definition).<br>–64 dB to +31.5 dB in 0.5-dB steps<br>0x00 = –64dB                      0x80 = 0 dB                      0xC0 to 0xFF = Reserved<br>0x01 = –63.5dB                      ... (0.5-dB steps)<br>... (0.5-dB steps)                      0xBF = +31.5 dB  |
| R1073 (0x0431)<br>DAC_Digital_<br>Volume_5R | 9   | OUT_VU           | See Footnote 1 | Output Signal Paths Volume Update. Writing 1 to this bit causes the Output Signal Paths Volume and Mute settings to be updated simultaneously                                                                                                                                                                                                  |
|                                             | 8   | OUT5L_MUTE       | 1              | Output Path 5 (Left) Digital Mute<br>0 = Unmute<br>1 = Mute                                                                                                                                                                                                                                                                                    |
|                                             | 7:0 | OUT5L_VOL[7:0]   | 0x80           | Output Path 5 (Left) Digital Volume (see Table 4-68 for volume register definition).<br>–64 dB to +31.5 dB in 0.5-dB steps<br>0x00 = –64dB                      0x80 = 0 dB                      0xC0 to 0xFF = Reserved<br>0x01 = –63.5dB                      ... (0.5-dB steps)<br>... (0.5-dB steps)                      0xBF = +31.5 dB  |

**Table 4-67. Output Signal Path Digital Volume Control (Cont.)**

| Register Address                        | Bit | Label          | Default        | Description                                                                                                                                                                                                                                                                                                                                    |
|-----------------------------------------|-----|----------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1077 (0x0435)<br>DAC_Digital_Volume_5R | 9   | OUT_VU         | See Footnote 1 | Output Signal Paths Volume Update. Writing 1 to this bit causes the Output Signal Paths Volume and Mute settings to be updated simultaneously                                                                                                                                                                                                  |
|                                         | 8   | OUT5R_MUTE     | 1              | Output Path 5 (Right) Digital Mute<br>0 = Unmute<br>1 = Mute                                                                                                                                                                                                                                                                                   |
|                                         | 7:0 | OUT5R_VOL[7:0] | 0x80           | Output Path 5 (Right) Digital Volume (see Table 4-68 for volume register definition).<br>–64 dB to +31.5 dB in 0.5-dB steps<br>0x00 = –64dB                      0x80 = 0 dB                      0xC0 to 0xFF = Reserved<br>0x01 = –63.5dB                      ... (0.5-dB steps)<br>... (0.5-dB steps)                      0xBF = +31.5 dB |

1. Default is not applicable to these write-only bits

Table 4-68 lists the output signal path digital volume settings.

**Table 4-68. Output Signal Path Digital Volume Range**

| Output Volume Register | Volume (dB) | Output Volume Register | Volume (dB) | Output Volume Register | Volume (dB) | Output Volume Register | Volume (dB) |
|------------------------|-------------|------------------------|-------------|------------------------|-------------|------------------------|-------------|
| 0x00                   | –64.0       | 0x31                   | –39.5       | 0x62                   | –15.0       | 0x93                   | 9.5         |
| 0x01                   | –63.5       | 0x32                   | –39.0       | 0x63                   | –14.5       | 0x94                   | 10.0        |
| 0x02                   | –63.0       | 0x33                   | –38.5       | 0x64                   | –14.0       | 0x95                   | 10.5        |
| 0x03                   | –62.5       | 0x34                   | –38.0       | 0x65                   | –13.5       | 0x96                   | 11.0        |
| 0x04                   | –62.0       | 0x35                   | –37.5       | 0x66                   | –13.0       | 0x97                   | 11.5        |
| 0x05                   | –61.5       | 0x36                   | –37.0       | 0x67                   | –12.5       | 0x98                   | 12.0        |
| 0x06                   | –61.0       | 0x37                   | –36.5       | 0x68                   | –12.0       | 0x99                   | 12.5        |
| 0x07                   | –60.5       | 0x38                   | –36.0       | 0x69                   | –11.5       | 0x9A                   | 13.0        |
| 0x08                   | –60.0       | 0x39                   | –35.5       | 0x6A                   | –11.0       | 0x9B                   | 13.5        |
| 0x09                   | –59.5       | 0x3A                   | –35.0       | 0x6B                   | –10.5       | 0x9C                   | 14.0        |
| 0x0A                   | –59.0       | 0x3B                   | –34.5       | 0x6C                   | –10.0       | 0x9D                   | 14.5        |
| 0x0B                   | –58.5       | 0x3C                   | –34.0       | 0x6D                   | –9.5        | 0x9E                   | 15.0        |
| 0x0C                   | –58.0       | 0x3D                   | –33.5       | 0x6E                   | –9.0        | 0x9F                   | 15.5        |
| 0x0D                   | –57.5       | 0x3E                   | –33.0       | 0x6F                   | –8.5        | 0xA0                   | 16.0        |
| 0x0E                   | –57.0       | 0x3F                   | –32.5       | 0x70                   | –8.0        | 0xA1                   | 16.5        |
| 0x0F                   | –56.5       | 0x40                   | –32.0       | 0x71                   | –7.5        | 0xA2                   | 17.0        |
| 0x10                   | –56.0       | 0x41                   | –31.5       | 0x72                   | –7.0        | 0xA3                   | 17.5        |
| 0x11                   | –55.5       | 0x42                   | –31.0       | 0x73                   | –6.5        | 0xA4                   | 18.0        |
| 0x12                   | –55.0       | 0x43                   | –30.5       | 0x74                   | –6.0        | 0xA5                   | 18.5        |
| 0x13                   | –54.5       | 0x44                   | –30.0       | 0x75                   | –5.5        | 0xA6                   | 19.0        |
| 0x14                   | –54.0       | 0x45                   | –29.5       | 0x76                   | –5.0        | 0xA7                   | 19.5        |
| 0x15                   | –53.5       | 0x46                   | –29.0       | 0x77                   | –4.5        | 0xA8                   | 20.0        |
| 0x16                   | –53.0       | 0x47                   | –28.5       | 0x78                   | –4.0        | 0xA9                   | 20.5        |
| 0x17                   | –52.5       | 0x48                   | –28.0       | 0x79                   | –3.5        | 0xAA                   | 21.0        |
| 0x18                   | –52.0       | 0x49                   | –27.5       | 0x7A                   | –3.0        | 0xAB                   | 21.5        |
| 0x19                   | –51.5       | 0x4A                   | –27.0       | 0x7B                   | –2.5        | 0xAC                   | 22.0        |
| 0x1A                   | –51.0       | 0x4B                   | –26.5       | 0x7C                   | –2.0        | 0xAD                   | 22.5        |
| 0x1B                   | –50.5       | 0x4C                   | –26.0       | 0x7D                   | –1.5        | 0xAE                   | 23.0        |
| 0x1C                   | –50.0       | 0x4D                   | –25.5       | 0x7E                   | –1.0        | 0xAF                   | 23.5        |
| 0x1D                   | –49.5       | 0x4E                   | –25.0       | 0x7F                   | –0.5        | 0xB0                   | 24.0        |
| 0x1E                   | –49.0       | 0x4F                   | –24.5       | 0x80                   | 0.0         | 0xB1                   | 24.5        |
| 0x1F                   | –48.5       | 0x50                   | –24.0       | 0x81                   | 0.5         | 0xB2                   | 25.0        |
| 0x20                   | –48.0       | 0x51                   | –23.5       | 0x82                   | 1.0         | 0xB3                   | 25.5        |
| 0x21                   | –47.5       | 0x52                   | –23.0       | 0x83                   | 1.5         | 0xB4                   | 26.0        |
| 0x22                   | –47.0       | 0x53                   | –22.5       | 0x84                   | 2.0         | 0xB5                   | 26.5        |
| 0x23                   | –46.5       | 0x54                   | –22.0       | 0x85                   | 2.5         | 0xB6                   | 27.0        |

**Table 4-68. Output Signal Path Digital Volume Range (Cont.)**

| Output Volume Register | Volume (dB) | Output Volume Register | Volume (dB) | Output Volume Register | Volume (dB) | Output Volume Register | Volume (dB) |
|------------------------|-------------|------------------------|-------------|------------------------|-------------|------------------------|-------------|
| 0x24                   | −46.0       | 0x55                   | −21.5       | 0x86                   | 3.0         | 0xB7                   | 27.5        |
| 0x25                   | −45.5       | 0x56                   | −21.0       | 0x87                   | 3.5         | 0xB8                   | 28.0        |
| 0x26                   | −45.0       | 0x57                   | −20.5       | 0x88                   | 4.0         | 0xB9                   | 28.5        |
| 0x27                   | −44.5       | 0x58                   | −20.0       | 0x89                   | 4.5         | 0xBA                   | 29.0        |
| 0x28                   | −44.0       | 0x59                   | −19.5       | 0x8A                   | 5.0         | 0xBB                   | 29.5        |
| 0x29                   | −43.5       | 0x5A                   | −19.0       | 0x8B                   | 5.5         | 0xBC                   | 30.0        |
| 0x2A                   | −43.0       | 0x5B                   | −18.5       | 0x8C                   | 6.0         | 0xBD                   | 30.5        |
| 0x2B                   | −42.5       | 0x5C                   | −18.0       | 0x8D                   | 6.5         | 0xBE                   | 31.0        |
| 0x2C                   | −42.0       | 0x5D                   | −17.5       | 0x8E                   | 7.0         | 0xBF                   | 31.5        |
| 0x2D                   | −41.5       | 0x5E                   | −17.0       | 0x8F                   | 7.5         | 0xC0–0xFF              | Reserved    |
| 0x2E                   | −41.0       | 0x5F                   | −16.5       | 0x90                   | 8.0         |                        |             |
| 0x2F                   | −40.5       | 0x60                   | −16.0       | 0x91                   | 8.5         |                        |             |
| 0x30                   | −40.0       | 0x61                   | −15.5       | 0x92                   | 9.0         |                        |             |

### 4.11.5 Output Signal Path Noise-Gate Control

The CS47L35 provides a digital noise-gate function for each of the output signal paths. The noise gate ensures best noise performance when the signal path is idle. When the noise gate is enabled, and the applicable signal level is below the noise-gate threshold, the noise gate is activated, causing the signal path to be muted.

The noise-gate function is enabled by setting NGATE\_ENA, as described in [Table 4-69](#).

For each output path, the noise gate may be associated with one or more of the signal path threshold detection functions using the x\_NGATE\_SRC fields. When more than one signal threshold is selected, the output-path noise gate is only activated (i.e., muted) when all of the respective signal thresholds are satisfied.

For example, if the OUT1L noise gate is associated with the OUT1L and OUT1R signal paths, the OUT1L signal path is only muted if both the OUT1L and OUT1R signal levels are below the respective thresholds.

The noise-gate threshold (the signal level below which the noise gate is activated) is set using NGATE\_THR. Note that, for each output path, the noise-gate threshold represents the signal level at the respective output pins; the threshold is therefore independent of the digital volume and PGA gain settings.

Note that, although there is only one noise-gate threshold level (NGATE\_THR), each of the output-path noise gates may be activated independently, according to the respective signal content and the associated threshold configurations.

To prevent erroneous triggering, a time delay is applied before the gate is activated; the noise gate is only activated (i.e., muted) when the output levels are below the applicable signal level thresholds for longer than the noise-gate hold time. The hold time is set using the NGATE\_HOLD field.

When the noise gate is activated, the CS47L35 gradually attenuates the respective signal path at the rate set by OUT\_VD\_RAMP (see [Table 4-67](#)). When the noise gate is deactivated, the output volume increases at the rate set by OUT\_VI\_RAMP.

**Table 4-69. Output Signal Path Noise-Gate Control**

| Register Address                       | Bit  | Label                 | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|----------------------------------------|------|-----------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1043 (0x0413)<br>Noise_Gate_Select_1L | 11:0 | OUT1L_NGATE_SRC[11:0] | 0x001   | Output Signal Path Noise-Gate Source. Enables one of more signal paths as inputs to the respective noise gate. If more than one signal path is enabled as an input, the noise gate is only activated (i.e., muted) when all of the respective signal thresholds are satisfied.<br>Each bit is coded as 0 = Disabled, 1 = Enabled<br>[11] = Reserved [7] = Reserved [3] = Reserved<br>[10] = Reserved [6] = OUT4L [2] = Reserved<br>[9] = OUT5R [5] = Reserved [1] = OUT1R<br>[8] = OUT5L [4] = Reserved [0] = OUT1L |
| R1047 (0x0417)<br>Noise_Gate_Select_1R | 11:0 | OUT1R_NGATE_SRC[11:0] | 0x002   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| R1067 (0x042B)<br>Noise_Gate_Select_4L | 11:0 | OUT4L_NGATE_SRC[11:0] | 0x040   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| R1075 (0x0433)<br>Noise_Gate_Select_5L | 11:0 | OUT5L_NGATE_SRC[11:0] | 0x100   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| R1079 (0x0437)<br>Noise_Gate_Select_5R | 11:0 | OUT5R_NGATE_SRC[11:0] | 0x200   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| R1112 (0x0458)<br>Noise_Gate_Control   | 5:4  | NGATE_HOLD[1:0]       | 00      | Output Signal Path Noise-Gate Hold Time (delay before noise gate is activated)<br>00 = 30 ms 10 = 250 ms<br>01 = 120 ms 11 = 500 ms                                                                                                                                                                                                                                                                                                                                                                                 |
|                                        | 3:1  | NGATE_THR[2:0]        | 000     | Output Signal Path Noise-Gate Threshold<br>000 = -78 dB 011 = -96 dB 110 = -114 dB<br>001 = -84 dB 100 = -102 dB 111 = -120 dB<br>010 = -90 dB 101 = -108 dB                                                                                                                                                                                                                                                                                                                                                        |
|                                        | 0    | NGATE_ENA             | 0       | Output Signal Path Noise-Gate Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

### 4.11.6 Output Signal Path AEC Loop-Back

The CS47L35 incorporates two loop-back signal paths, which are ideally suited as a reference for AEC processing. Any two of the output signal paths may be selected as the AEC loop-back sources.

When configured with suitable DSP firmware, the CS47L35 can provide an integrated AEC capability. The AEC loop-back feature also enables convenient hook-up to an external device for implementing the required signal-processing algorithms.

The AEC loop-back source is connected after the respective digital volume controls, as shown in [Fig. 4-49](#). The AEC loop-back signals can be selected as input to any of the digital mixers within the CS47L35 digital core. The sample rate for the AEC loop-back paths is configured using OUT\_RATE—see [Table 4-21](#).

The AEC loop-back function is enabled using the AEC<sub>n</sub>\_LOOPBACK\_ENA bits (where *n* identifies the applicable path, AEC1 or AEC2). The source signals for the Transmit Path AEC function are selected using the AEC<sub>n</sub>\_LOOPBACK\_SRC bits.

The CS47L35 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the AEC loop-back function. If the frequency is too low, an attempt to enable this function fails. Note that active signal paths are not affected under such circumstances.

The AEC<sub>n</sub>\_ENA\_STS bits indicate the status of the AEC loop-back functions. If an underclocked error condition occurs, these bits indicate whether the AEC loop-back function has been enabled.

**Table 4-70. Output Signal Path AEC Loop-Back Control**

| Register Address                    | Bit | Label                  | Default | Description                                                                                                                           |
|-------------------------------------|-----|------------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------|
| R1104 (0x0450)<br>DAC_AEC_Control_1 | 5:2 | AEC1_LOOPBACK_SRC[3:0] | 0000    | Input source for Tx AEC1 function<br>0000 = OUT1L 0110 = OUT4L 1001 = OUT5R<br>0001 = OUT1R 1000 = OUT5L All other codes are reserved |
|                                     | 1   | AEC1_ENA_STS           | 0       | Transmit (Tx) Path AEC1 Control Status<br>0 = Disabled<br>1 = Enabled                                                                 |
|                                     | 0   | AEC1_LOOPBACK_ENA      | 0       | Transmit (Tx) Path AEC1 Control<br>0 = Disabled<br>1 = Enabled                                                                        |

**Table 4-70. Output Signal Path AEC Loop-Back Control (Cont.)**

| Register Address                        | Bit | Label                      | Default | Description                                                                                                                                       |
|-----------------------------------------|-----|----------------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| R1105 (0x0451)<br>DAC_AEC_<br>Control_2 | 5:2 | AEC2_LOOPBACK_<br>SRC[3:0] | 0000    | Input source for Tx AEC2 function<br>0000 = OUT1L    0110 = OUT4L    1001 = OUT5R<br>0001 = OUT1R    1000 = OUT5L    All other codes are reserved |
|                                         | 1   | AEC2_ENA_STS               | 0       | Transmit (Tx) Path AEC2 Control Status<br>0 = Disabled<br>1 = Enabled                                                                             |
|                                         | 0   | AEC2_LOOPBACK_<br>ENA      | 0       | Transmit (Tx) Path AEC2 Control<br>0 = Disabled<br>1 = Enabled                                                                                    |

### 4.11.7 Headphone and Earpiece Outputs

The headphone/earpiece driver outputs, HPOUTL, HPOUTR, EPOUTP, and EPOUTN, are suitable for direct connection to external headphones and earpieces. The outputs are ground referenced, eliminating any requirement for AC coupling capacitors.

The headphone output incorporates a common mode, or ground loop, feedback path that provides rejection of system-related ground noise. The feedback pin must be connected to ground for normal operation of the headphone outputs.

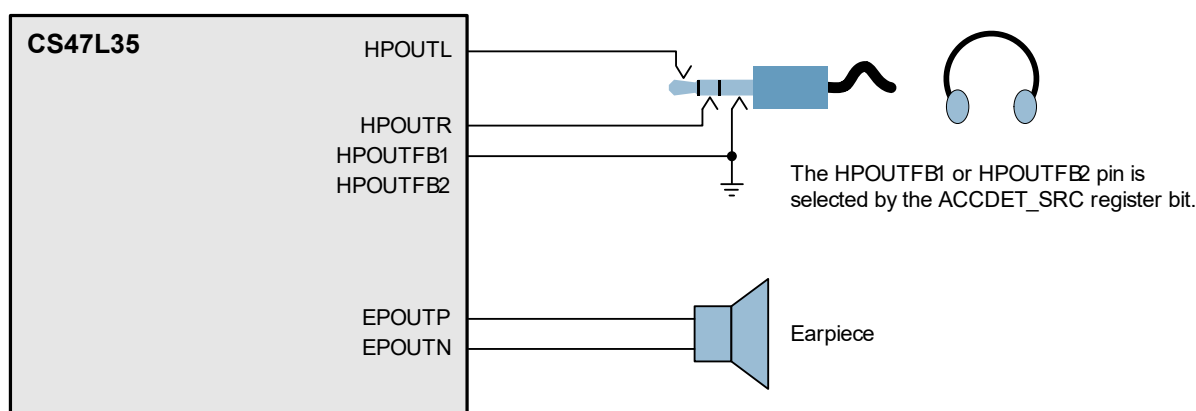
The ground feedback path for HPOUTL and HPOUTR is provided via the HPOUTFB1 or HPOUTFB2 pins; the applicable connection must be selected using ACCDET\_SRC, as described in [Table 4-71](#).

Note that the selected feedback pin should be connected to GND as close as possible to the respective headphone jack ground pin, as shown in [Fig. 4-50](#). In mono (differential) mode, the feedback pin should be connected to the ground plane that is closest to the earpiece output PCB tracks.

**Table 4-71. Headphone Output (HPOUT) Ground Feedback Control**

| Register Address                             | Bit | Label      | Default | Description                                                                                                                                                                                        |
|----------------------------------------------|-----|------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R659 (0x0293)<br>Accessory_<br>Detect_Mode_1 | 13  | ACCDET_SRC | 0       | Accessory Detect/Headphone Feedback pin select<br>0 = Accessory detect on MICDET1; Headphone ground feedback on HPOUTFB1<br>1 = Accessory detect on MICDET2; Headphone ground feedback on HPOUTFB2 |

The headphone and earpiece connections are shown in [Fig. 4-50](#).


**Figure 4-50. Headphone and Earpiece Connection**

### 4.11.8 Speaker Outputs (Analog)

The speaker driver outputs SPKOUTP and SPKOUTN provide differential (BTL) outputs suitable for direct connection to an external loudspeaker. The integrated Class D speaker driver provides high efficiency at large signal levels.

The speaker driver signal paths incorporate a boost function that shifts the signal levels between the AVDD and SPKVDD voltage domains. The boost is preconfigured (+12 dB) for the recommended AVDD and SPKVDD operating voltages (see [Table 3-3](#)).

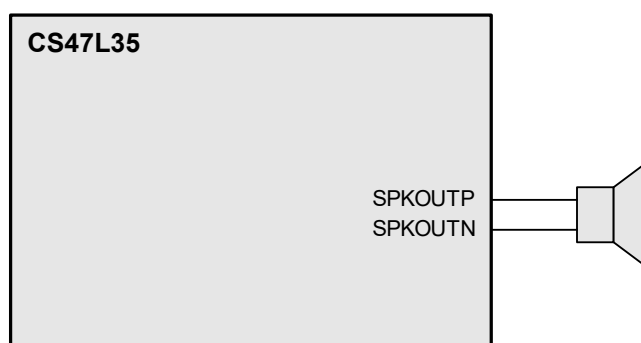
Ultralow leakage and high PSRR allow the speaker supply SPKVDD to be connected directly to a lithium battery.

Note that SYSCLK must be present and enabled when using the Class D speaker output; see [Section 4.16](#) for details of SYSCLK and the associated control fields.

The OUT4L output signal path is associated with the analog outputs SPKOUTP and SPKOUTN.

The Class D speaker output is a pulse-width modulated signal, and requires external filtering in order to recreate the audio signal. With a suitable choice of external speakers, the speakers themselves can provide the necessary filtering. See [Section 5](#) for further information on Class D speaker connections.

The external speaker connection is shown in [Fig. 4-51](#), assuming a suitable speaker is chosen to provide the PWM filtering.



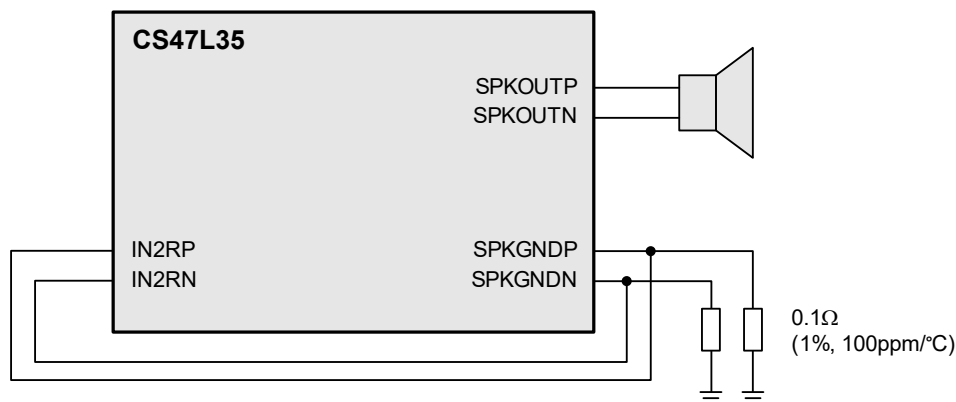
**Figure 4-51. Speaker Connection**

The speaker output path is designed to support monitoring of external loudspeakers, giving real-time feedback for algorithms such as Cirrus Logic's speaker protection software. Specific external connections are necessary when using this feature, as detailed below.

The Speaker Protection software, implemented on one of the integrated DSP cores, enables loudspeakers to be protected from excessive signal levels and other electro-mechanical constraints. The monitoring circuit enables the operational limits to be continually optimized for the particular loudspeaker and the prevailing conditions. Factors such as cone excursion, resonance, and thermal behavior of the loudspeaker are modeled in the Speaker Protection software. As a result, the maximum audio output can be achieved, while ensuring the loudspeakers are also fully protected from damage.

Separate P/N ground connections are provided for the speaker driver; these pins relate to the positive/negative output transistors respectively, to allow comprehensive current monitoring in the output paths, as an input to the speaker protection algorithms.

The external speaker connections, incorporating the output current monitoring requirements, are shown in [Fig. 4-52](#). Note that, if output current monitoring is not required, these connections should be tied directly to ground on the PCB.



**Figure 4-52. Speaker Output Current Monitoring Connections (Speaker Protection)**

Please contact your Cirrus Logic representative for further information on the Speaker Protection software.

### 4.11.9 Speaker Outputs (Digital PDM)

The CS47L35 supports a two-channel pulse-density modulation (PDM) digital speaker interface; the PDM outputs are associated with the OUT5L and OUT5R output signal paths.

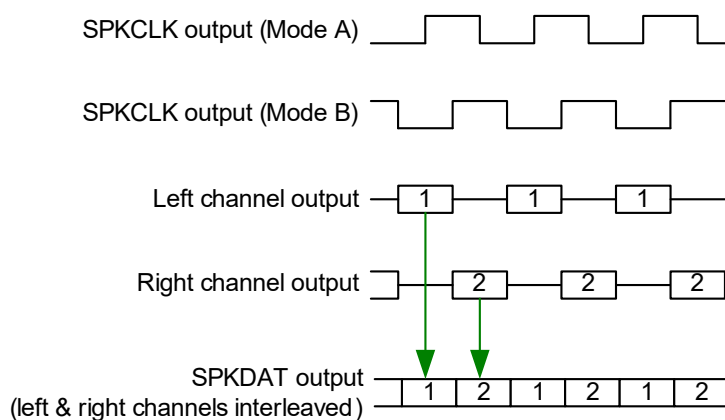
The external connections associated with the PDM outputs are implemented on multi-function GPIO pins, which must be configured for the respective PDM functions when required. The PDM output connections are pin-specific alternative functions available on specific GPIO pins. See [Section 4.14](#) to configure the GPIO pins for the PDM output.

The PDM digital speaker interface is a stereo interface; the OUT5L and OUT5R output signal paths are interleaved on the SPKDAT output, and clocked using SPKCLK.

Note that the PDM interface supports two different operating modes; these are selected using SPK1\_FMT. See [Table 3-15](#) for detailed timing information in both modes.

- If SPK1\_FMT = 0 (Mode A), the Left PDM channel is valid at the rising edge of SPKCLK; the Right PDM channel is valid at the falling edge of SPKCLK.
- If SPK1\_FMT = 1 (Mode B), the Left PDM channel is valid during the low phase of SPKCLK; the Right PDM channel is valid during the high phase of SPKCLK.

The PDM interface timing is shown in [Fig. 4-53](#).



**Figure 4-53. Digital Speaker (PDM) Interface Timing**

Clocking for the PDM interface is derived from SYSCLK. Note that SYSCLK\_ENA must also be set. See [Section 4.16](#) for further details of the system clocks and control registers.

When the OUT5L or OUT5R output signal path is enabled, the PDM interface clock signal is output on the SPKCLK pin.

The output signal paths support normal and high performance operating modes, as described in [Section 4.11.3](#). The SPKCLK frequency is set according to the operating mode of the relevant output path, as described in [Table 4-72](#). The OUT5\_OSR bit is defined in [Table 4-66](#).

Note that the SPKCLK frequencies noted in [Table 4-72](#) assume that the SYSCLK frequency is a multiple of 6.144 MHz (SYSCLK\_FRAC = 0). If the SYSCLK frequency is a multiple of 5.6448 MHz (SYSCLK\_FRAC=1), the SPKCLK frequency is scaled accordingly.

**Table 4-72. SPKCLK Frequency**

| OUT5_OSR | Description           | SPKCLK Frequency |
|----------|-----------------------|------------------|
| 0        | Normal mode           | 3.072 MHz        |
| 1        | High Performance mode | 6.144 MHz        |

The PDM output channels can be independently muted. When muted, the default output on each channel is a DSD-compliant silent stream (0110\_1001b). The mute output code can be programmed to other values if required, using the SPK1\_MUTE\_SEQ field. The mute output code can be transmitted MSB-first or LSB-first; this is selectable using the SPK1\_MUTE\_ENDIAN bit.

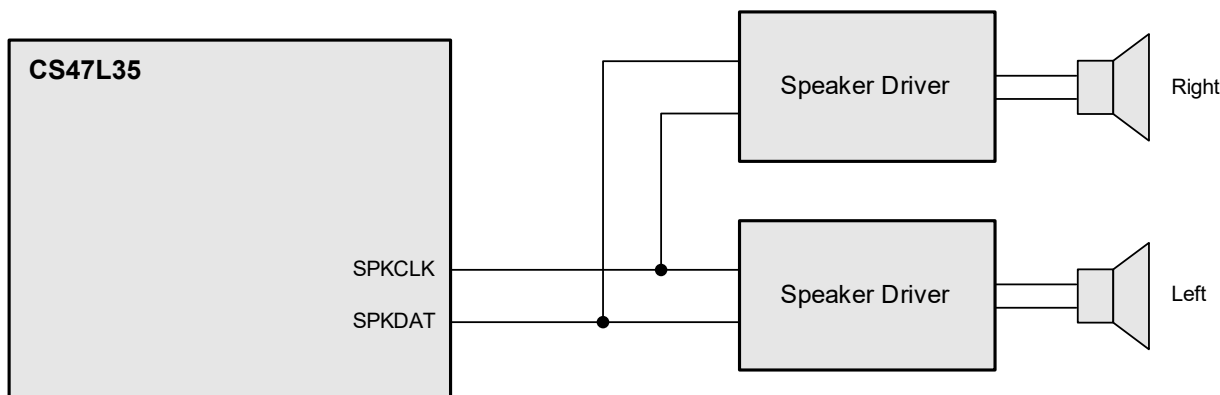
Note that the PDM Mute function is not a soft-mute; the audio output is interrupted immediately when the PDM mute is asserted. It is recommended to use the output signal path mute function before applying the PDM mute. See [Table 4-67](#) for details of the OUT5L\_MUTE and OUT5R\_MUTE bits.

The PDM output interface registers are described in [Table 4-73](#).

**Table 4-73. Digital Speaker (PDM) Output Control**

| Register Address                  | Bit | Label              | Default | Description                                                                                                                                                                      |
|-----------------------------------|-----|--------------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R1168 (0x0490)<br>PDM_SPK1_CTRL_1 | 13  | SPK1R_MUTE         | 0       | PDM Speaker Output 1 (Right) Mute<br>0 = Audio output (OUT5R)<br>1 = Mute Sequence output                                                                                        |
|                                   | 12  | SPK1L_MUTE         | 0       | PDM Speaker Output 1 (Left) Mute<br>0 = Audio output (OUT5L)<br>1 = Mute Sequence output                                                                                         |
|                                   | 8   | SPK1_MUTE_ENDIAN   | 0       | PDM Speaker Output 1 Mute Sequence Control<br>0 = Mute sequence is LSB first<br>1 = Mute sequence output is MSB first                                                            |
|                                   | 7:0 | SPK1_MUTE_SEQ[7:0] | 0x69    | PDM Speaker Output 1 Mute Sequence<br>Defines the 8-bit code that is output on SPKDAT (left) or SPKDAT (right) when muted.                                                       |
| R1169 (0x0491)<br>PDM_SPK1_CTRL_2 | 0   | SPK1_FMT           | 0       | PDM Speaker Output 1 timing format<br>0 = Mode A (PDM data is valid at the rising/falling edges of SPKCLK)<br>1 = Mode B (PDM data is valid during the high/low phase of SPKCLK) |

The digital speaker (PDM) outputs SPKDAT and SPKCLK are intended for direct connection to a compatible external speaker driver. A typical configuration is shown in [Fig. 4-54](#).



**Figure 4-54. Digital Speaker (PDM) Connection**

## 4.12 External Accessory Detection

The CS47L35 provides external accessory detection functions that can sense the presence and impedance of external components. This can be used to detect the insertion or removal of an external headphone or headset, and to provide an indication of key/button push events.

Jack insertion is detected using the JACKDET1 and JACKDET2 pins, which must be connected to a switch contact within the jack sockets. An interrupt event is generated whenever a jack insertion or jack removal event is detected.

Suppression of pops and clicks caused by jack insertion or removal is provided using the MICDET clamp function. This function can also be used to trigger interrupt events, and/or to trigger the control-write sequencer. The integrated general-purpose switch can be synchronized with the MICDET clamp, to provide additional pop suppression capability.

Microphones, push buttons, and other accessories can be detected via the MICDET1 or MICDET2 pins. The presence of a microphone, and the status of a hook switch can be detected. This feature can also be used to detect push-button operation.

Headphone impedance can be detected via the HPDETL and HPDETR pins; this can be used to set different gain levels or other configuration settings according to the type of load connected. For example, different settings may be applicable to headphone or line output loads.

The MICVDD power domain must be enabled when using the microphone detect function. (Note that MICVDD is not required for the jack detect or headphone detect functions.) The MICVDD power domain is provided using an internal charge pump (CP2) and LDO regulator (LDO2). See [Section 4.19](#) for details of these circuits.

The internal 32-kHz clock must be present and enabled when using the microphone detect or headphone detect functions; the 32-kHz clock is also required for the jack detect function, assuming input debounce is enabled. See [Section 4.16](#) for details of the internal 32-kHz clock and associated control fields.

### 4.12.1 Jack Detect

The CS47L35 provides support for jack insertion switch detection. The jack insertion status can be read using the relevant register status bits. A jack insertion or removal can also be used to trigger an interrupt event.

The jack-detect interrupt (IRQ) functionality is maintained in Sleep Mode (see [Section 4.13](#)). This enables a jack insertion event to be used to trigger a wake-up of the CS47L35.

Jack insertion and removal is detected using the JACKDET1 and JACKDET2 pins. The recommended external connections are shown in [Fig. 4-55](#). Note that the logic thresholds associated with the two JACKDET differ from each other, as described in [Table 3-11](#)—this provides support for different jack switch configurations.

The jack detect feature is enabled using the JD $n$ \_ENA bits (where  $n = 1$  or  $2$  for JACKDET1 or JACKDET2 respectively); the jack insertion status can be read using JD $n$ \_STS $x$ . Note that the JD $n$ \_STS1 and JD $n$ \_STS2 bits provide the same information in respect of the applicable JACKDET $n$  input.

The jack detect input debounce is selected using the JD<sub>n</sub>\_DB bits, as described in [Table 4-74](#). Note that, under normal operating conditions, the debounce circuit uses the 32-kHz clock, which must be enabled whenever input debounce functions are required. Input debounce is not provided in Sleep Mode; the JD<sub>n</sub>\_DB bits have no effect in Sleep Mode.

Note that the jack detect signals, JD1 and JD2, can be used as inputs to the MICDET clamp function—this provides additional functionality relating to jack insertion and removal events.

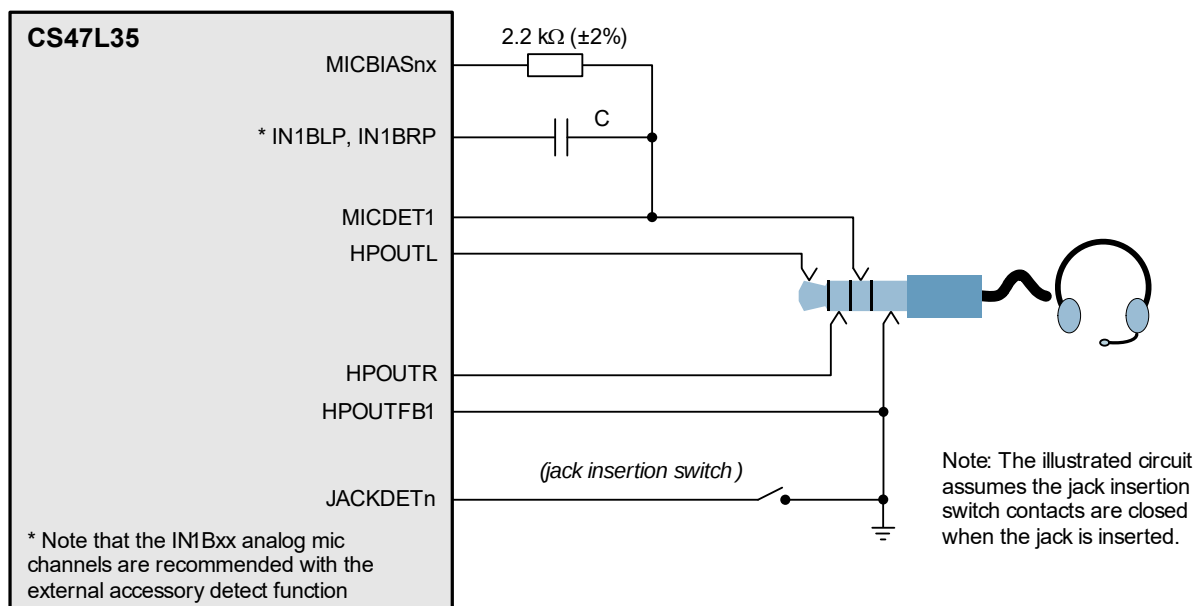
An interrupt request (IRQ) event is generated whenever a jack insertion or jack removal is detected (see [Section 4.15](#)). Separate mask bits are provided, to allow IRQ events on the rising and/or falling edges of the JD1 or JD2 signals.

The control registers associated with the jack detect function are described in [Table 4-74](#).

**Table 4-74. Jack Detect Control**

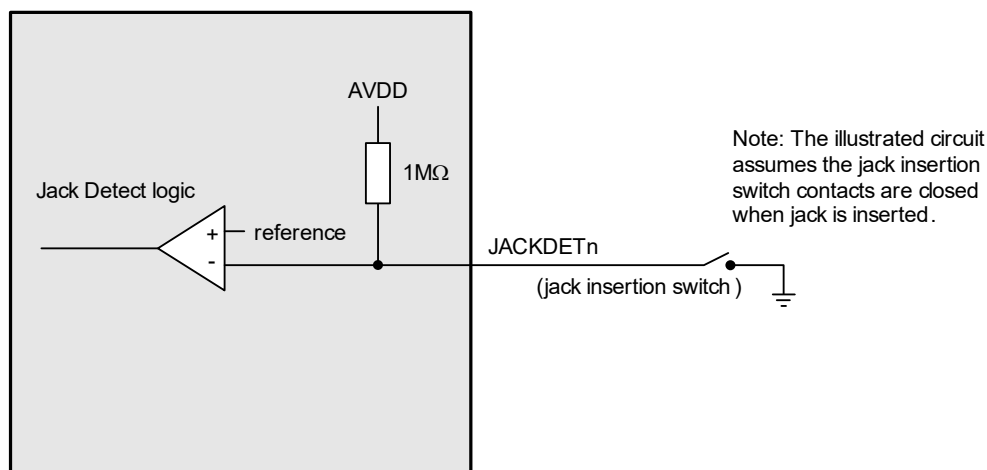
| Register Address                       | Bit | Label    | Default | Description                                                                                                                           |
|----------------------------------------|-----|----------|---------|---------------------------------------------------------------------------------------------------------------------------------------|
| R723 (0x02D3)<br>Jack_detect_analog    | 1   | JD2_ENA  | 0       | JACKDET2 enable<br>0 = Disabled<br>1 = Enabled                                                                                        |
|                                        | 0   | JD1_ENA  | 0       | JACKDET1 enable<br>0 = Disabled<br>1 = Enabled                                                                                        |
| R6278 (0x1886)<br>IRQ1_Raw_Status_7    | 2   | JD2_STS1 | 0       | JACKDET2 input status<br>0 = Jack not detected<br>1 = Jack is detected<br>(Assumes the JACKDET2 pin is pulled low on jack insertion.) |
|                                        | 0   | JD1_STS1 | 0       | JACKDET1 input status<br>0 = Jack not detected<br>1 = Jack is detected<br>(Assumes the JACKDET1 pin is pulled low on jack insertion.) |
| R6534 (0x1986)<br>IRQ2_Raw_Status_7    | 2   | JD2_STS2 | 0       | JACKDET2 input status<br>0 = Jack not detected<br>1 = Jack is detected<br>(Assumes the JACKDET2 pin is pulled low on jack insertion.) |
|                                        | 0   | JD1_STS2 | 0       | JACKDET1 input status<br>0 = Jack not detected<br>1 = Jack is detected<br>(Assumes the JACKDET1 pin is pulled low on jack insertion.) |
| R6662 (0x1A06)<br>Interrupt_Debounce_7 | 2   | JD2_DB   | 0       | JACKDET2 input debounce<br>0 = Disabled<br>1 = Enabled                                                                                |
|                                        | 0   | JD1_DB   | 0       | JACKDET1 input debounce<br>0 = Disabled<br>1 = Enabled                                                                                |

A recommended connection circuit, including headphone output on HPOUT and microphone connections, is shown in [Fig. 4-55](#). See [Section 5.1](#) for details of recommended external components.



**Figure 4-55. Jack Detect and External Accessory Connections**

The internal comparator circuit used to detect the JACKDET $n$  status is shown in Fig. 4-56. The threshold voltages for the jack detect circuit are noted in Table 3-11. Note that separate thresholds are defined for jack insertion and removal.



**Figure 4-56. Jack Detect Comparator**

### 4.12.2 Jack Pop Suppression (MICDET Clamp and GP Switch)

Under typical configuration of a 3.5-mm headphone/accessory jack connection, there is a risk of pops and clicks arising from jack insertion or removal. This can occur when the headphone load makes momentary contact with the MICBIAS output when the jack is not fully inserted.

The CS47L35 provides a MICDET clamp function to suppress pops and clicks caused by jack insertion or removal. It can be controlled directly, or can be activated by a configurable logic function derived from external logic inputs. The clamp status can be read using the relevant register status bit. The clamp status can also be used to trigger an interrupt (IRQ) event or to trigger the control-write sequencer.

### 4.12.2.1 MICDET Clamp Control

The MICDET clamp function can be configured using the MICD\_CLAMP\_MODE field; the selectable logic conditions (derived from the JD1 and/or JD2 signals; see [Table 4-74](#)) provide support for different jack detect circuit configurations. The MICD\_CLAMP\_OVD bit, when set, activates the MICDET clamp, regardless of other conditions.

**Note:** The MICD\_CLAMP\_OVD bit is enabled by default; the MICDET clamp is always active following power-on reset, hardware reset, or software reset.

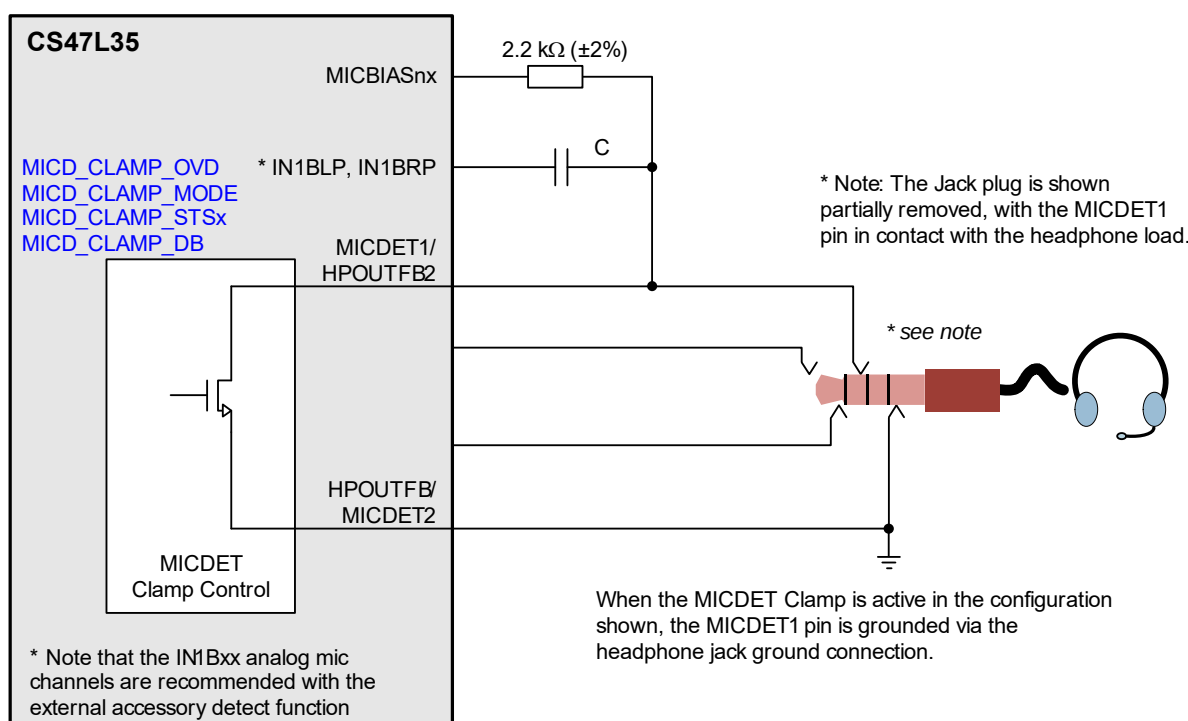
The MICDET clamp functionality (including the external IRQ) is maintained in Sleep Mode (see [Section 4.13](#)). This enables a jack insertion event to be used to trigger a wake-up of the CS47L35. A summary of the jack detect and MICDET clamp functionality, and their recommended usage in typical applications, is described in [Section 4.12.2.5](#).

When the MICDET clamp is active, the MICDET1/HPOUTFB2 and HPOUTFB1/MICDET2 pins are short-circuited together. The grounding of the MICDET pin is achieved via the applicable HPOUTFB pin; note that it is assumed that the HPOUTFB connection is grounded externally, as shown in [Fig. 4-57](#).

The configurable logic provides flexibility in selecting the appropriate conditions for activating the MICDET clamp. The clamp status can be read using the MICD\_CLAMP\_STSx bits. Note that the MICD\_CLAMP\_STS1 and MICD\_CLAMP\_STS2 bits provide the same information.

The MICDET clamp debounce is selected by setting MICD\_CLAMP\_DB, as described in [Table 4-75](#). Note that, under normal operating conditions, the debounce circuit uses the 32-kHz clock, which must be enabled whenever input debounce functions are required. Input debounce is not provided in Sleep Mode; the MICD\_CLAMP\_DB bit has no effect in Sleep Mode.

The MICDET clamp function is shown in [Fig. 4-57](#). Note that the jack plug is shown partially removed, with the MICDET1 pin in contact with the headphone load.



**Figure 4-57. MICDET Clamp Circuit**

### 4.12.2.2 Interrupts and Write-Sequencer Control

An interrupt request (IRQ) event is generated whenever the MICDET clamp is asserted or deasserted; see [Section 4.15](#). Separate mask bits are provided to enable IRQ events on the rising and/or falling edge of the MICDET clamp status.

The control-write sequencer can be triggered by the MICDET clamp status. This is enabled using the WSEQ\_ENA\_MICD\_CLAMP\_FALL and WSEQ\_ENA\_MICD\_CLAMP\_RISE bits; see [Section 4.18](#) for further details.

### 4.12.2.3 Pop Suppression using General-Purpose Switch

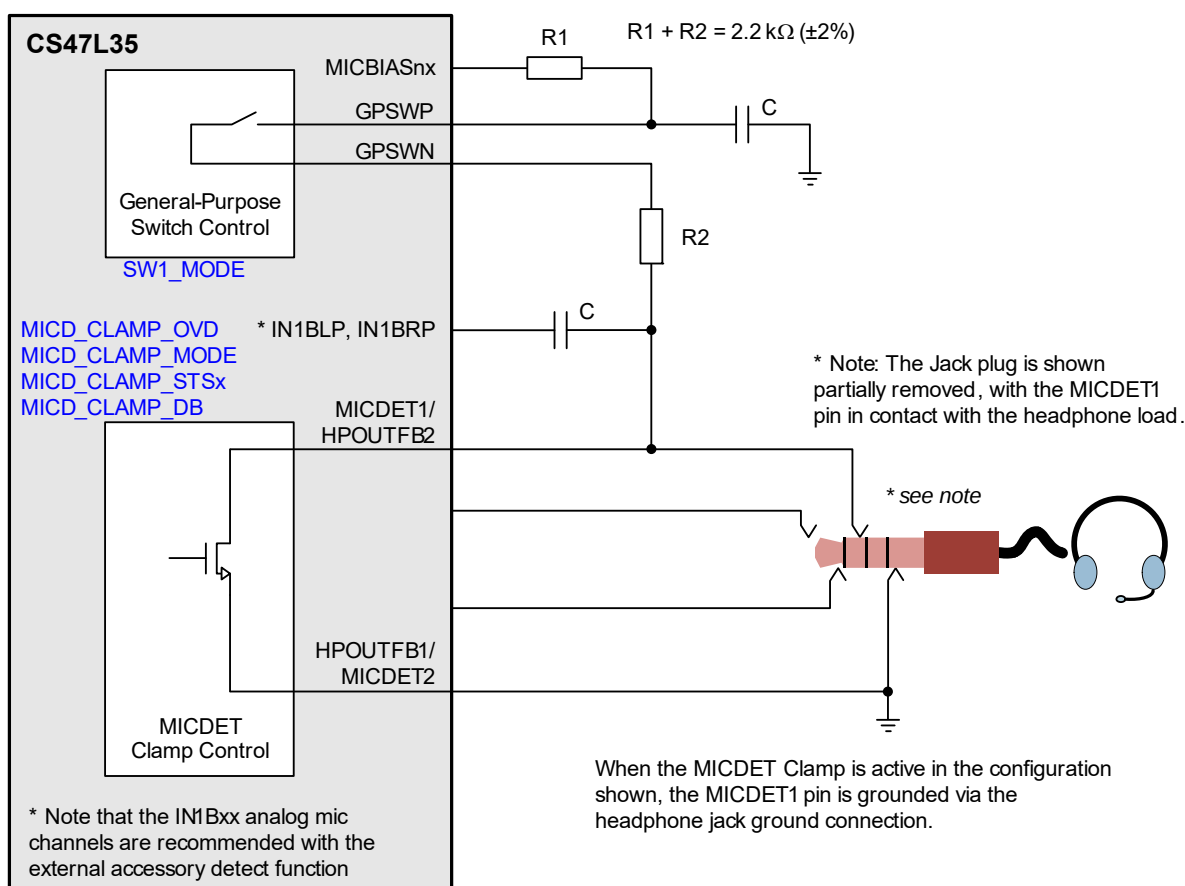
In applications where a large decoupling capacitance is present on the MICBIAS output, the MICDET clamp function alone may be unable to discharge the capacitor sufficiently to eliminate pops and clicks associated with jack insertion and removal. In this case, it may be desirable to use the general-purpose switch within the CS47L35 to provide isolation from the MICBIAS output; an example circuit is shown in [Fig. 4-58](#).

The general-purpose switch is configured using SW1\_MODE. This field allows the switch to be disabled, enabled, or synchronized to the MICDET clamp status, as described in [Table 4-75](#).

For jack pop suppression, it is recommended to set SW1\_MODE = 11. In this case, the switch contacts are open whenever the MICDET clamp is active, and the switch contacts are closed whenever the MICDET clamp is inactive.

Normal accessory functions are supported when the switch contacts (GPSWP and GPSWN) are closed, and the MICDET clamp is inactive. Ground clamping of MICDET, and isolation of MICBIAS are achieved when the switch contacts are open, and the MICDET clamp is active.

Note that the MICDET clamp function must also be configured appropriately when using this method of pop suppression control.



**Figure 4-58. General-Purpose Switch Circuit**

### 4.12.2.4 MICDET Clamp Control Registers

The control registers associated with the MICDET clamp and general-purpose switch functions are described in [Table 4-75](#).

**Table 4-75. MICDET Clamp and General-Purpose Switch Control**

| Register Address                           | Bit | Label                            | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------------------------------------|-----|----------------------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R65 (0x0041)<br>Sequence_<br>control       | 7   | WSEQ_ENA_<br>MICD_<br>CLAMP_FALL | 0       | MICDET Clamp (Falling) Write Sequencer Select<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|                                            | 6   | WSEQ_ENA_<br>MICD_<br>CLAMP_RISE | 0       | MICDET Clamp (Rising) Write Sequencer Select<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| R710 (0x02C6)<br>Micd_Clamp_<br>control    | 4   | MICD_<br>CLAMP_OVD               | 1       | MICDET Clamp Override<br>0 = Disabled<br>1 = Enabled (clamp active)                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|                                            | 3:0 | MICD_<br>CLAMP_<br>MODE[3:0]     | 0000    | MICDET Clamp Mode<br>0x0 = Disabled<br>0x1 = Active (MICDET1 and MICDET2 are shorted together)<br>0x2–0x3 = Reserved<br>0x4 = Active when JD1=0<br>0x5 = Active when JD1=1<br>0x6 = Active when JD2=0<br>0x7 = Active when JD2=1<br>0x8 = Active when JD1=0 or JD2=0<br>0x9 = Active when JD1=0 or JD2=1<br>0xA = Active when JD1=1 or JD2=0<br>0xB = Active when JD1=1 or JD2=1<br>0xC = Active when JD1=0 and JD2=0<br>0xD = Active when JD1=0 and JD2=1<br>0xE = Active when JD1=1 and JD2=0<br>0xF = Active when JD1=1 and JD2=1 |
| R712 (0x02C8)<br>GP_Switch_1               | 1:0 | SW1_<br>MODE[1:0]                | 00      | General-purpose Switch control<br>00 = Disabled (open)    10 = Enabled when MICDET clamp is active<br>01 = Enabled (closed)    11 = Enabled when MICDET clamp is not active                                                                                                                                                                                                                                                                                                                                                          |
| R6278 (0x1886)<br>IRQ1_Raw_<br>Status_7    | 4   | MICD_<br>CLAMP_STS1              | 0       | MICDET Clamp status<br>0 = Clamp not active<br>1 = Clamp active                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| R6534 (0x1986)<br>IRQ2_Raw_<br>Status_7    | 4   | MICD_<br>CLAMP_STS2              | 0       | MICDET Clamp status<br>0 = Clamp not active<br>1 = Clamp active                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| R6662 (0x1A06)<br>Interrupt_<br>Debounce_7 | 4   | MICD_<br>CLAMP_DB                | 0       | MICDET Clamp debounce<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

#### 4.12.2.5 Control Sequence for Jack Detect and MICDET Clamp

A summary of the jack detect and MICDET clamp functionality, and the recommended usage in typical applications, is described as follows.

- On device power-up, and following reset, the MICDET clamp is active, due to the default setting of MICD\_CLAMP\_OVD; this ensures no spurious output can occur during jack insertion. It is recommended to keep the MICDET clamp active (MICD\_CLAMP\_OVD = 1) until after a jack insertion has been detected.  
The MICDET\_CLAMP\_MODE field should be set according to the applicable JD1/JD2 signal configuration (configured to assert the clamp when jack is removed).
- Jack insertion is indicated using the JD1/JD2 signals (assuming that the MICDET\_CLAMP\_MODE field has been correctly set for the applicable JD1/JD2 signal configuration); the associated status bits can be read directly, or associated signals can be unmasked as inputs to the interrupt controller.  
After jack insertion has been detected, the applicable headset functions (headphone, microphone, accessory detect) may then be enabled.  
If the headset function requires MICBIAS to be enabled on the respective jack, the MICDET clamp should be disabled (MICD\_CLAMP\_OVD = 0) immediately before enabling the MICBIAS (or immediately before enabling MICD\_ENA). Note that, if MICBIAS is not required on the respective jack, the clamp should not be disabled (e.g., for headphone-only operation).
- Jack removal is also indicated using the JD1/JD2 signals. The JD1/JD2 status bits can be read directly, or can be unmasked as inputs to the interrupt controller. In this event, the MICDET clamp ensures fast and automatic silencing of the jack outputs.

Under typical use cases, the respective MICBIAS generator and headset audio paths should all be disabled following jack removal.

After jack removal has been detected, the MICDET clamp override bit should be asserted (MICD\_CLAMP\_OVD = 1), to make the system ready for a jack insertion.

The recommended control sequence for jack detect and MICDET clamp is summarized in [Table 4-76](#).

**Table 4-76. Control Sequence for Jack Detect and MICDET Clamp**

| Event             | Device Actions                                                | Recommended User Actions                                                                                                                                                         |
|-------------------|---------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Initial condition | Clamp asserted by default                                     | Configure MICDET_CLAMP_MODE                                                                                                                                                      |
| Jack insertion    | Jack insertion signaled via IRQ                               | For headphone-only operation:<br>Enable output signal paths<br>For other use cases:<br>Disable clamp, MICD_CLAMP_OVD = 0<br>Enable MICBIAS and MICDET<br>Enable I/O signal paths |
| Jack removal      | Jack removal signaled via IRQ<br>Clamp asserted automatically | Disable MICBIAS and MICDET<br>Disable I/O signal paths<br>Enable clamp MICD_CLAMP_OVD = 1                                                                                        |

### 4.12.3 Microphone Detect

The CS47L35 microphone detection circuit measures the impedance of an external load connected to one of the MICDET pins. This feature can be used to detect the presence of a microphone, and the status of the associated hook switch. It can also be used to detect push-button status or the connection of other external accessories.

#### 4.12.3.1 Microphone Detect Control

The microphone detection circuit measures the impedance connected to MICDET1 or MICDET2. In the discrete measurement mode (ACCDDET\_MODE = 000), the function reports whether the measured impedance lies within one of eight predefined levels. In the ADC measurement mode (ACCDDET\_MODE = 111), a more specific result is provided in the form of a 7-bit ADC output.

The microphone detection circuit typically uses one of the MICBIAS outputs as a reference. The CS47L35 automatically enables the appropriate MICBIAS generator when required by the detection function; this allows the detection function to be supported in low-power standby operating conditions.

Note that the MICVDD power domain must be enabled when using the microphone detection function. This power domain is provided using an internal charge pump (CP2) and LDO regulator (LDO2). See [Section 4.19](#) for details of these circuits. The internal 32-kHz clock must be present and enabled when using the microphone detection function; see [Section 4.16](#) for details.

To select microphone detection on one of the MICDET pins, ACCDET\_MODE must be set to 000 or 111 (depending on the desired measurement mode). The ACCDET\_MODE field is defined in [Table 4-77](#).

The CS47L35 can only support one headphone or microphone detection function at any time. When the detection function is not in use, it is recommended to set ACCDET\_MODE = 000.

The microphone detection circuit can be enabled on the MICDET1 pin or the MICDET2 pin, selected by using the ACCDET\_SRC bit.

The microphone detection circuit uses MICVDD, MICBIAS1A, MICBIAS1B, or MICBIAS2A as a reference. The applicable source is configured using the MICD\_BIAS\_SRC field. Note that MICBIAS2B is not a valid reference source for the microphone detection function.

When ACCDET\_MODE is set to 000 or 111, microphone detection is enabled by setting MICD\_ENA.

When microphone detection is enabled, the CS47L35 performs a number of measurements in order to determine the MICDET impedance. The measurement process is repeated at a cyclic rate controlled by MICD\_RATE. The MICD\_RATE field selects the delay between completion of one measurement and the start of the next. When the microphone detection result has settled, the CS47L35 indicates valid data by setting MICD\_VALID.

The discrete measurement mode and ADC measurement mode provide different capabilities for microphone detection. The control requirements and the measurement indication mechanisms differ according to the selected mode, as follows:

- In the discrete measurement mode (ACCDDET\_MODE = 000), the measured impedance is only deemed valid after more than one successive measurement has produced the same result. The MICD\_DBTIME field provides control of the debounce period; this can be either two measurements or four measurements.

When the microphone detection result has settled (i.e., after the applicable debounce period), the CS47L35 indicates valid data by setting the MICD\_VALID bit. The measured impedance is indicated using the MICD\_LVL and MICD\_STS bits, as described in [Table 4-77](#).

The MICD\_VALID bit, when set, remains asserted for as long as the microphone detection function is enabled (i.e., while MICD\_ENA = 1). If the detected impedance changes, the MICD\_LVL and MICD\_STS fields change, but the MICD\_VALID bit remains set, indicating valid data at all times.

The detection circuit supports up to eight impedance levels (including the no-accessory-detected level), enabling detection of a typical microphone and up to six push buttons. Each measurement level can be enabled or disabled independently; this provides flexibility according to the required thresholds, and offers a faster measurement time in some applications. The MICD\_LVL\_SEL field is described in [Section 4.12.3.3](#). The default configuration supports a maximum of four push buttons, in accordance with the Android headset specification for accessory push-button operation.

Note that, for typical headset detection, the choice of external resistance values must take into account the impedance of the microphone—the detected impedance corresponds to the combined parallel resistance of the microphone and any asserted push button. Examples of suitable external components are described in [Section 5.1.8](#).

- In the ADC measurement mode (ACCDDET\_MODE = 111), the detection function generates two output results, contained within the MICDET\_ADCVAL and MICDET\_ADCVAL\_DIFF fields. These fields contain the most recent measurement value (MICDET\_ADCVAL) and the measurement difference value (MICDET\_ADCVAL\_DIFF). The difference value indicates the difference between the latest measurement and the previous measurement; this can be used to determine whether the measurement is stable and reliable.

In ADC measurement mode, the detection function must be disabled before the measurement can be read. When the CS47L35 indicates valid data (MICD\_VALID = 1), the detection must be disabled by setting MICD\_ENA = 0.

Note that MICDET\_ADCVAL and MICDET\_ADCVAL\_DIFF do not follow a linear coding. The appropriate test condition for accepting the measurement value (or for rescheduling the measurement) varies depending on the application requirements, and depending on the expected impedance value.

The microphone detection function is an input to the interrupt control circuit and can be used to trigger an interrupt event every time an accessory insertion, removal, or impedance change is detected; see [Section 4.15](#).

The fields associated with microphone detection (or other accessories) are described in [Table 4-77](#). The external circuit configuration is shown in [Fig. 4-59](#).

**Table 4-77. Microphone Detect Control**

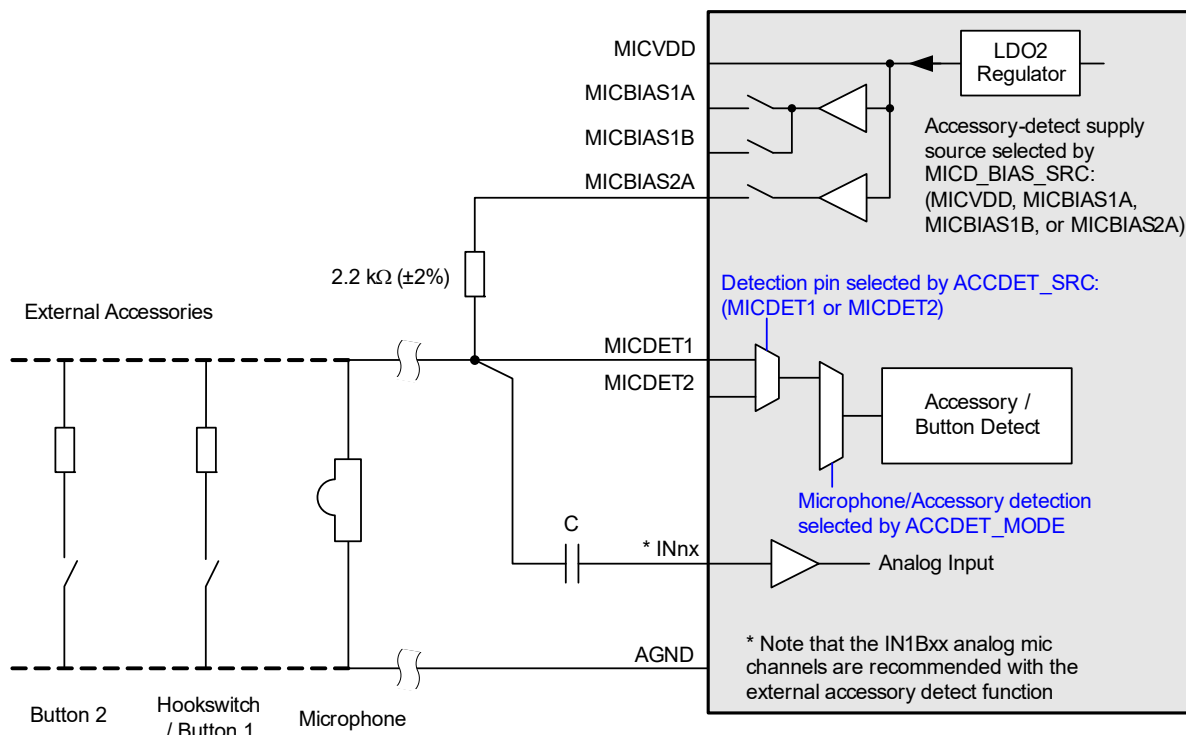
| Register Address                         | Bit | Label             | Default | Description                                                                                                                                                                                                                                                                                                                                                                                         |
|------------------------------------------|-----|-------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R659 (0x0293)<br>Accessory_Detect_Mode_1 | 13  | ACCDDET_SRC       | 0       | Accessory Detect/Headphone Feedback pin select<br>0 = Accessory detect on MICDET1; Headphone ground feedback on HPOUTFB1<br>1 = Accessory detect on MICDET2; Headphone ground feedback on HPOUTFB2                                                                                                                                                                                                  |
|                                          | 2:0 | ACCDDET_MODE[2:0] | 000     | Accessory Detect Mode Select<br>000 = Mic detect (MICDETn, discrete mode) 100 = Headphone detect (MICDETn)<br>001 = Headphone detect (HPDETL) 101 = Reserved<br>010 = Headphone detect (HPDETR) 110 = Reserved<br>011 = Reserved 111 = Mic detect (MICDETn, ADC mode)<br>Note that the MICDETn measurements are implemented on either the MICDET1 or MICDET2 pins, depending on the ACCDET_SRC bit. |

**Table 4-77. Microphone Detect Control (Cont.)**

| Register Address              | Bit   | Label                    | Default     | Description                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------------------------------|-------|--------------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R675 (0x02A3)<br>Mic_Detect_1 | 15:12 | MICD_BIAS_STARTTIME[3:0] | 0001        | Mic Detect Bias Start-up Delay (If MICBIAS is not enabled, this field selects the delay time allowed for MICBIAS to start-up before performing the MICDET function.)<br>0000 = 0 ms (continuous)      0101 = 4 ms      1010 = 128 ms<br>0001 = 0.25 ms      0110 = 8 ms      1011 = 256 ms<br>0010 = 0.5 ms      0111 = 16 ms      1100 to 1111 = 512 ms<br>0011 = 1 ms      1000 = 32 ms<br>0100 = 2 ms      1001 = 64 ms |
|                               | 11:8  | MICD_RATE[3:0]           | 0001        | Mic Detect Rate (Selects the delay between successive MICDET measurements.)<br>0000 = 0 ms (continuous)      0101 = 4 ms      1010 = 128 ms<br>0001 = 0.25 ms      0110 = 8 ms      1011 = 256 ms<br>0010 = 0.5 ms      0111 = 16 ms      1100 to 1111 = 512 ms<br>0011 = 1 ms      1000 = 32 ms<br>0100 = 2 ms      1001 = 64 ms                                                                                          |
|                               | 6:4   | MICD_BIAS_SRC[2:0]       | 000         | Accessory Detect (MICDET) reference select<br>000 = MICVDD      010 = MICBIAS1B      All other codes are reserved<br>001 = MICBIAS1A      011 = MICBIAS2A                                                                                                                                                                                                                                                                  |
|                               | 1     | MICD_DBTIME              | 1           | Mic Detect Debounce<br>0 = 2 measurements<br>1 = 4 measurements<br>Only valid when ACCDET_MODE = 000.                                                                                                                                                                                                                                                                                                                      |
|                               | 0     | MICD_ENA                 | 0           | Mic Detect Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                           |
| R676 (0x02A4)<br>Mic_Detect_2 | 7:0   | MICD_LVL_SEL[7:0]        | 1001_1111   | Mic Detect Level Select (enables mic/accessory detection in specific impedance ranges)<br>[7] = Enable >1 kΩ detection      [3] = Not used<br>[6] = Not used      [2] = Enable 360–680 Ω detection<br>[5] = Not used      [1] = Enable 210–290 Ω detection<br>[4] = Not used      [0] = Enable 110–180 Ω detection<br>Only valid when ACCDET_MODE = 000.                                                                   |
| R677 (0x02A5)<br>Mic_Detect_3 | 10:2  | MICD_LVL[8:0]            | 0_0000_0000 | Mic Detect Level (indicates the measured impedance)<br>[8] = >475 Ω, <30 kΩ      [3] = 360–680 Ω<br>[7] = Not used      [2] = 210–290 Ω<br>[6] = Not used      [1] = 110–180 Ω<br>[5] = Not used      [0] = 0–70 Ω<br>[4] = Not used<br>Only valid when ACCDET_MODE = 000.                                                                                                                                                 |
|                               | 1     | MICD_VALID               | 0           | Mic Detect Data Valid<br>0 = Not Valid<br>1 = Valid                                                                                                                                                                                                                                                                                                                                                                        |
|                               | 0     | MICD_STS                 | 0           | Mic Detect Status<br>0 = No mic/accessory present (impedance is >30 kΩ)<br>1 = Mic/accessory is present (impedance is <30 kΩ)<br>Only valid when ACCDET_MODE = 000.                                                                                                                                                                                                                                                        |
| R683 (0x02AB)<br>Mic_Detect_4 | 15:8  | MICDET_ADCVAL_DIFF[7:0]  | 0x00        | Mic Detect ADC Level (Difference)<br>Only valid when ACCDET_MODE = 111.                                                                                                                                                                                                                                                                                                                                                    |
|                               | 6:0   | MICDET_ADCVAL[6:0]       | 0x00        | Mic Detect ADC Level<br>Only valid when ACCDET_MODE = 111.                                                                                                                                                                                                                                                                                                                                                                 |

The external connections for the microphone detect circuit are shown in [Fig. 4-59](#). In typical applications, it can be used to detect a microphone or button press.

Note that, when using the microphone detect circuit, it is recommended to use the IN1BLP or IN1BRP analog microphone input paths to ensure best immunity to electrical transients arising from the external accessory.



**Figure 4-59. Microphone- and Accessory-Detect Interface**

#### 4.12.3.2 MICBIAS Reference Control

The voltage reference for the microphone detection is configured using the MICD\_BIAS\_SRC field, as described in [Table 4-77](#). The microphone detection function automatically enables the applicable reference when required for MICDET impedance measurement.

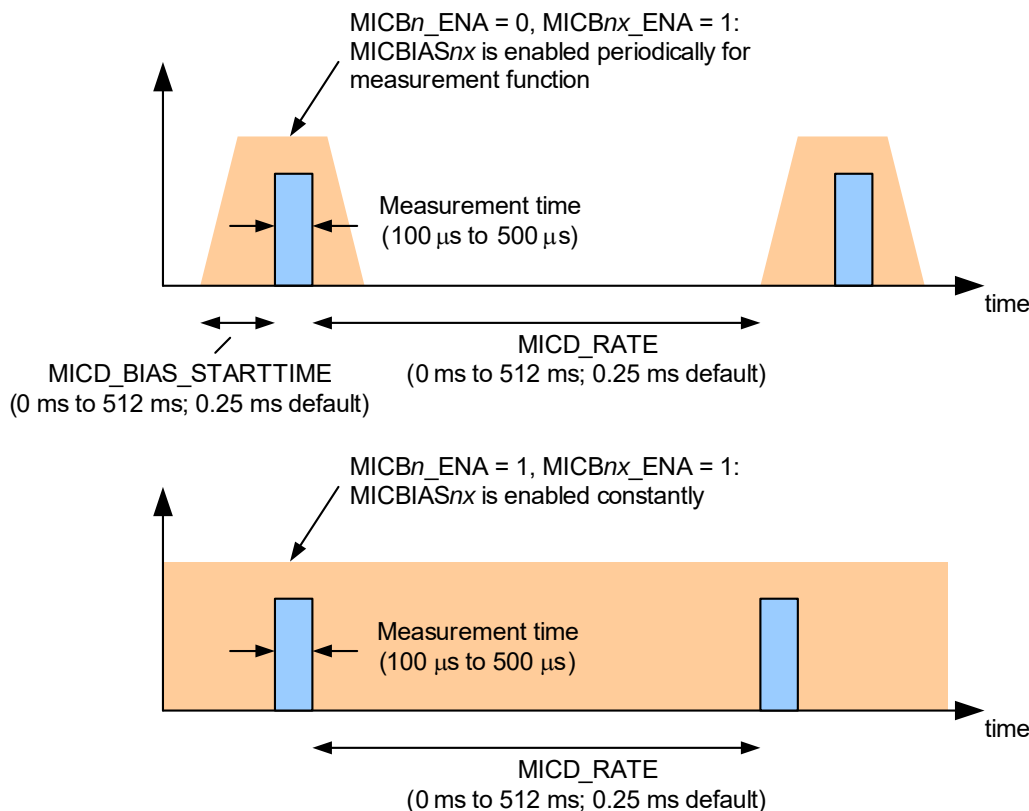
If the selected reference (MICBIAS<sub>*Snx*</sub>) is not already enabled, the microphone detect circuit automatically enables the respective MICBIAS output for short periods of time only, every time the impedance measurement is scheduled. To allow time for the MICBIAS source to start-up, a time delay is applied before the measurement is performed; this is configured using MICD\_BIAS\_STARTTIME, as described in [Table 4-77](#).

**Note:** The microphone detection automatically enables the applicable MICBIASx generator (MICBIAS1 or MICBIAS2), every time the impedance measurement is scheduled. The respective MICBIAS output switches are not controlled automatically—the applicable switches must be enabled using the MICB1A\_ENA, MICB1B\_ENA or and MICB2A\_ENA bits, as described in [Table 4-112](#).

The MICD\_BIAS\_STARTTIME field should be set to 16 ms or more if MICBn\_RATE = 1 (pop-free start-up/shutdown). MICD\_BIAS\_STARTTIME should be set to 0.25 ms or more if MICBn\_RATE = 0 (fast start-up/shutdown).

The timing of the microphone detect function is shown in [Fig. 4-60](#). Two different cases are shown, according to whether MICBIAS<sub>nx</sub> is enabled periodically by the impedance measurement function, or is enabled at all times.

If the selected reference (MICBIAS $n_x$ ) is not enabled continuously, the respective MICBIAS $n_x$  discharge bits should be cleared. The MICBIAS control registers are described in [Section 4.19](#).



**Figure 4-60. Microphone- and Accessory-Detect Timing**

### 4.12.3.3 Measurement Range Control

When the discrete measurement mode is selected (`ACCDDET_MODE` = 000), the `MICD_LVL_SEL[7:0]` bits allow each of the impedance measurement levels to be enabled or disabled independently. This allows the function to be tailored to the particular application requirements.

If one or more bits `MICD_LVL_SEL` is cleared, the corresponding impedance level is disabled. Any measured impedance which lies in a disabled level is reported as the next lowest, enabled level.

For example, the `MICD_LVL_SEL[2]` bit enables the detection of a 360–680  $\Omega$  impedance. If `MICD_LVL_SEL[2]` = 0, an external impedance in this range is indicated in the next lowest detection range (210–290  $\Omega$ ); this would be reported in the `MICD_LVL` field as `MICD_LVL[2]` = 1.

With default register configuration, and all measurement levels enabled, the CS47L35 can detect the presence of a typical microphone and up to four push buttons. It is possible to configure the detection circuit for up to eight push buttons, by adjusting the impedance detection thresholds. However, adjustment of the detection thresholds is outside the scope of this datasheet—please contact your local Cirrus Logic representative for further information, if required.

The measurement time varies between 100–500  $\mu$ s, depending on the impedance of the external load, and depending on how many impedance measurement levels are enabled. A high impedance is measured faster than a low impedance.

### 4.12.3.4 External Components

The external connections for the microphone detect circuit are shown in [Fig. 4-59](#). Examples of suitable external components are described in [Section 5.1.8](#).

The accuracy of the microphone detect function is assured whenever the connected load is within the applicable limits specified in [Table 3-11](#). It is required that a 2.2-k $\Omega$  (2%) resistor must also be connected between `MICDET` and the selected `MICBIAS` reference—different resistor values lead to inaccuracy in the impedance measurement.

Note that, for typical headset detection, the choice of external resistance values must take into account the impedance of the microphone—the detected impedance corresponds to the combined parallel resistance of the microphone and any asserted push button.

## 4.12.4 Headphone Detect

The CS47L35 headphone detection circuit measures the impedance of an external headphone load. This feature can be used to set different gain levels or to apply other configuration settings according to the type of load connected. Separate monitor pins are provided for headphone detection on the left and right channels of HPOUT.

### 4.12.4.1 Headphone Detection Control

Headphone detection can be enabled on the HPDETL pin or the HPDETR pin. Under recommended configuration, these pins provide measurement of the HPOUTL and HPOUTR loads respectively.

The headphone detect function can also be enabled on the MICDET1 pin or the MICDET2 pin. Note that, in this configuration, any MICBIAS output that is connected to the selected MICDET pin must be disabled and floating (MICBnx\_ENA = 0, MICBnx\_DISCH = 0).

The applicable headphone detection pin is selected using the ACCDET\_MODE field. When MICDET $n$  is selected (ACCDET\_MODE = 100), the applicable MICDET $n$  pin is determined by the ACCDET\_SRC bit, as described in [Table 4-80](#).

The CS47L35 can only support one headphone or microphone detection function at any time. When the detection function is not in use, it is recommended to set ACCDET\_MODE = 000.

Headphone detection on the selected channel is commanded by writing 1 to HP\_POLL.

The impedance measurement range is configured using HP\_IMPEDANCE\_RANGE. This field should be set in accordance with the expected load impedance. Note that a number of separate measurements are typically required to determine the load impedance; the recommended control requirements are described in [Section 4.12.4.2](#).

**Note:** Setting HP\_IMPEDANCE\_RANGE is not required for detection on the MICDET $n$  pins (ACCDET\_MODE = 100). The impedance measurement range, and measurement accuracy, in this mode are different to the HPDETL and HPDETR measurement modes.

For correct operation, the respective output drivers must be disabled when headphone detection is commanded on HPOUTL or HPOUTR. The required settings are shown in [Table 4-78](#).

**Table 4-78. Output Configuration for Headphone Detect**

| Description                  | Requirement  |
|------------------------------|--------------|
| HPOUTL Impedance measurement | HP1L_ENA = 0 |
| HPOUTR Impedance measurement | HP1R_ENA = 0 |

**Note:** The applicable headphone outputs configuration must be maintained until after the headphone detection has completed. See [Table 4-64](#) for details of the HP1L\_ENA and HP1R\_ENA bits.

When headphone detection is commanded, the CS47L35 uses an adjustable current source to determine the connected impedance. A sweep of measurement currents is applied. The rate of this sweep can be adjusted using HP\_CLK\_DIV and HP\_RATE.

### 4.12.4.2 Measurement Output

The headphone detection process typically comprises a number of separate measurements (for different impedance ranges). Completion of each measurement is indicated by HP\_DONE. When this bit is set, the measurement result can be read from the HP\_DACVAL and HP\_DACVAL\_DOWN fields, and decoded as described in [Eq. 4-2](#).

$$\text{Impedance } (\Omega) = \frac{C_0 + (C_1 \times \text{Offset})}{\left[ \frac{(((\text{HP\_DACVAL} + \text{HP\_DACVAL\_DOWN})/2) + 0.5)}{C_2} \right] - \left[ \frac{1}{C_3(1 + (C_4 \times \text{Gradient}))} \right]} - C_5$$

**Equation 4-2. Headphone Impedance Calculation**

The associated parameters for decoding the measurement result are defined [Table 4-79](#). The applicable values are dependent on the HP\_IMPEDANCE\_RANGE setting in each case. The Offset and Gradient values are derived from register fields that are factory-calibrated for each device.

**Table 4-79. Headphone Measurement Decode Parameters**

| Parameter      | HP_IMPEDANCE_RANGE = 00 | HP_IMPEDANCE_RANGE = 01 | HP_IMPEDANCE_RANGE = 10 | HP_IMPEDANCE_RANGE = 11 |
|----------------|-------------------------|-------------------------|-------------------------|-------------------------|
| C <sub>0</sub> | 1.007                   | 1.007                   | 9.696                   | 100.684                 |
| C <sub>1</sub> | -0.0072                 | -0.0072                 | -0.0795                 | -0.9494                 |
| C <sub>2</sub> | 4003                    | 7975                    | 7300                    | 7300                    |
| C <sub>3</sub> | 69.3                    | 69.6                    | 62.9                    | 63.2                    |
| C <sub>4</sub> | 0.0055                  | 0.0055                  | 0.0055                  | 0.0055                  |
| C <sub>5</sub> | 0.25                    | 0.25                    | 0.25                    | 0.25                    |
| Offset         | HP_OFFSET_00            | HP_OFFSET_01            | HP_OFFSET_10            | HP_OFFSET_11            |
| Gradient       | HP_GRADIENT_0X          | HP_GRADIENT_0X          | HP_GRADIENT_1X          | HP_GRADIENT_1X          |

Note that, to achieve the specified measurement accuracy, the above equation must be calculated to an accuracy of at least 5 decimal places throughout.

The impedance measurement result is valid when  $169 \leq \text{HP\_DACVAL} \leq 1017$ . (In case of any contradiction with the HP\_IMPEDANCE\_RANGE description, the HP\_DACVAL validity takes precedence.)

If the external impedance is entirely unknown (i.e., it could lie in any of the HP\_IMPEDANCE\_RANGE regions), it is recommended to test initially with HP\_IMPEDANCE\_RANGE = 00. If the resultant HP\_DACVAL is < 169, the impedance is higher than the selected measurement range, so the test should be scheduled again, after incrementing HP\_IMPEDANCE\_RANGE.

Each measurement is triggered by writing 1 to HP\_POLL. Completion of each measurement is indicated by HP\_DONE. Note that, after HP\_DONE has been asserted, it remains asserted until the next measurement has been commanded.

**Note:** A simpler, but less accurate, procedure for headphone impedance measurement is also supported, using the HP\_LVL field. When the HP\_DONE bit is set, indicating completion of a measurement, the impedance can be read directly from the HP\_LVL field, provided that the value lies within the range of the applicable HP\_IMPEDANCE\_RANGE setting.

Note that, for detection using one of the MICDET<sub>n</sub> pins, the HP\_LVL field is the only supported measurement output option. The HP\_IMPEDANCE\_RANGE field is not valid for detection on the MICDET<sub>n</sub> pins. See [Table 4-80](#) for further description of the HP\_LVL field.

The headphone detection function is an input to the interrupt control circuit and can be used to trigger an interrupt event on completion of the headphone detection; see [Section 4.15](#).

The fields associated with headphone detection are described in [Table 4-80](#). The external circuit configuration is shown [Fig. 4-61](#).

Note that 32-bit register addressing is used from R12888 (0x3000) upwards; 16-bit format is used otherwise. The registers noted in [Table 4-80](#) contain a mixture of 16- and 32-bit register addresses.

**Table 4-80. Headphone Detect Control**

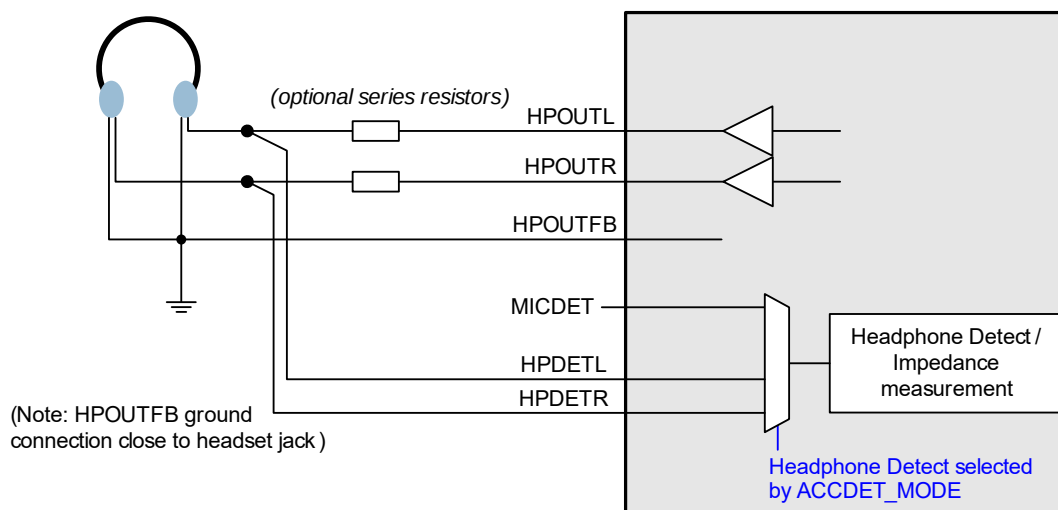
| Register Address                         | Bit   | Label                   | Default        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------------------------------------------|-------|-------------------------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R12792 (0x31F8)<br>OTP_HPDET_Cal_1       | 31:24 | HP_OFFSET_11[7:0]       | See Footnote 1 | Headphone Detect Calibration field.<br>Signed number, LSB = 0.25.<br>Range is –31.75 to +31.75.<br>Default value is factory-set per device.                                                                                                                                                                                                                                                                                                 |
|                                          | 23:16 | HP_OFFSET_10[7:0]       | See Footnote 1 | Headphone Detect Calibration field.<br>Signed number, LSB = 0.25.<br>Range is –31.75 to +31.75.<br>Default value is factory-set per device.                                                                                                                                                                                                                                                                                                 |
|                                          | 15:8  | HP_OFFSET_01[7:0]       | See Footnote 1 | Headphone Detect Calibration field.<br>Signed number, LSB = 0.25.<br>Range is –31.75 to +31.75.<br>Default value is factory-set per device.                                                                                                                                                                                                                                                                                                 |
|                                          | 7:0   | HP_OFFSET_00[7:0]       | See Footnote 1 | Headphone Detect Calibration field.<br>Signed number, LSB = 0.25.<br>Range is –31.75 to +31.75.<br>Default value is factory-set per device.                                                                                                                                                                                                                                                                                                 |
| R12794 (0x31FA)<br>OTP_HPDET_Cal_2       | 15:8  | HP_GRADIENT_1X[7:0]     | See Footnote 1 | Headphone Detect Calibration field.<br>Signed number, LSB = 0.25.<br>Range is –31.75 to +31.75.<br>Default value is factory-set per device.                                                                                                                                                                                                                                                                                                 |
|                                          | 7:0   | HP_GRADIENT_0X[7:0]     | See Footnote 1 | Headphone Detect Calibration field.<br>Signed number, LSB = 0.25.<br>Range is –31.75 to +31.75.<br>Default value is factory-set per device.                                                                                                                                                                                                                                                                                                 |
| R659 (0x0293)<br>Accessory_Detect_Mode_1 | 13    | ACCDDET_SRC             | 0              | Accessory Detect/Headphone Feedback pin select<br>0 = Accessory detect on MICDET1, Headphone ground feedback on HPOUTFB1<br>1 = Accessory detect on MICDET2, Headphone ground feedback on HPOUTFB2                                                                                                                                                                                                                                          |
|                                          | 2:0   | ACCDDET_MODE[2:0]       | 00             | Accessory Detect Mode Select.<br>000 = Mic detect (MICDET <sub>n</sub> , discrete mode) 100 = Headphone detect (MICDET <sub>n</sub> )<br>001 = Headphone detect (HPDETL) 101–110 = Reserved<br>010 = Headphone detect (HPDETR) 111 = Mic detect (MICDET <sub>n</sub> , ADC mode)<br>011 = Reserved<br>Note that the MICDET <sub>n</sub> measurements are implemented on either the MICDET1 or MICDET2 pins, depending on the ACCDET_SRC bit |
| R667 (0x029B)<br>Headphone_Detect_1      | 10:9  | HP_IMPEDANCE_RANGE[1:0] | 00             | Headphone Detect Range<br>00 = 4 Ω to 30 Ω<br>01 = 8 Ω to 100 Ω<br>10 = 100 Ω to 1 kΩ<br>11 = 1 kΩ to 10 kΩ<br>Only valid when ACCDET_MODE = 001 or ACCDET_MODE = 010.                                                                                                                                                                                                                                                                      |
|                                          | 4:3   | HP_CLK_DIV[1:0]         | 00             | Headphone Detect Clock Rate (Selects the clocking rate of the headphone detect adjustable current source. Decreasing the clock rate gives a slower measurement time.)<br>00 = 32 kHz<br>01 = 16 kHz<br>10 = 8 kHz<br>11 = 4 kHz                                                                                                                                                                                                             |
|                                          | 2:1   | HP_RATE[1:0]            | 00             | Headphone Detect Sweep Rate<br>(Selects the step size between successive measurements. Increasing the step size gives a faster measurement time.)<br>00 = 1<br>01 = 2<br>10 = 4<br>11 = Reserved                                                                                                                                                                                                                                            |
|                                          | 0     | HP_POLL                 | 0              | Headphone Detect Enable<br>Write 1 to start HP Detect function                                                                                                                                                                                                                                                                                                                                                                              |

**Table 4-80. Headphone Detect Control (Cont.)**

| Register Address                        | Bit  | Label               | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----------------------------------------|------|---------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R668 (0x029C)<br>Headphone_<br>Detect_2 | 15   | HP_DONE             | 0       | Headphone Detect Status<br>0 = HP Detect not complete<br>1 = HP Detect done                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                                         | 14:0 | HP_LVL[14:0]        | 0x0000  | Headphone Detect Level<br>LSB = 0.5 $\Omega$<br>8 = 4 $\Omega$ or less<br>9 = 4.5 $\Omega$<br>10 = 5 $\Omega$<br>11 = 5.5 $\Omega$<br>...<br>20,000 = 10 k $\Omega$ or more<br>For HPDETL or HPDETR measurement (ACCDDET_MODE = 001 or 010), HPD_LVL is valid from 4 $\Omega$ to 10 k $\Omega$ , within the range selected by HP_IMPEDANCE_RANGE.<br>For MICDETn measurement (ACCDDET_MODE = 100), HPD_LVL is valid from 400 $\Omega$ to 6 k $\Omega$ only.<br>If HP_LVL reports a value outside the selected range, the range should be adjusted and the measurement repeated. A 0- $\Omega$ result may be reported if the measurement is less than the minimum value for the selected range. |
| R669 (0x029D)<br>Headphone_<br>Detect_3 | 9:0  | HP_DACVAL[9:0]      | 0x000   | Headphone Detect Level (Coded as integer, LSB = 1. See separate description for full decode information.)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| R671 (0x029F)<br>Headphone_<br>Detect_5 | 9:0  | HP_DACVAL_DOWN[9:0] | 0x000   | Headphone Detect Level (Coded as integer, LSB = 1. See separate description for full decode information.)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

1. Default value is factory-set per device.

The external connections for the headphone detect circuit are shown in Fig. 4-61.


**Figure 4-61. Headphone Detect Interface**

Note that, where external resistors are connected in series with the headphone load, as shown, it is recommended that the HPDETLn connection is to the headphone side of the resistors. If the HPDETLn connection is made to the CS47L35 end of these resistors, this leads to a corresponding offset in the measured impedance.

Under default conditions, the measurement time varies between 17–244 ms, depending on the impedance of the external load. A high impedance is measured faster than a low impedance.

## 4.13 Low Power Sleep Configuration

The CS47L35 supports a low-power Sleep Mode, in which most functions are disabled and power consumption is minimized. The CS47L35 enters Sleep Mode when the DCVDD supply is removed. Note that the AVDD and DBVDD1 supplies must be present throughout the Sleep Mode duration.

In Sleep Mode, the CS47L35 can generate an interrupt event in response to a change in voltage on the JACKDET1 or JACKDET2 pins. This enables a jack insertion event (or other digital logic transition) to be used to trigger a wake-up of the CS47L35.

The system clocks (SYSCLK, DSPCLK) should be disabled before selecting Sleep Mode. The external clock input (MCLK<sub>n</sub>) may also be stopped, if desired.

The functionality and control fields associated with Sleep Mode are supported via an internal always-on supply domain.

The always-on control registers are listed in [Table 4-81](#). These fields are maintained (i.e., not reset) in Sleep Mode.

Note that the control interface is not supported in Sleep Mode; read/write access to the always-on registers is not possible. Access to the register map using any of the control interfaces should be ceased before selecting Sleep Mode.

**Table 4-81. Sleep Mode Always-On Control Registers**

| Register Address | Label                    | Reference                        |
|------------------|--------------------------|----------------------------------|
| R710 (0x02C6)    | MICD_CLAMP_OVD           | See <a href="#">Section 4.12</a> |
|                  | MICD_CLAMP_MODE[3:0]     |                                  |
| R723 (0x02D3)    | JD2_ENA                  |                                  |
|                  | JD1_ENA                  |                                  |
| R6150 (0x1806)   | MICD_CLAMP_FALL_EINT1    | See <a href="#">Section 4.15</a> |
|                  | MICD_CLAMP_RISE_EINT1    |                                  |
|                  | JD2_FALL_EINT1           |                                  |
|                  | JD2_RISE_EINT1           |                                  |
|                  | JD1_FALL_EINT1           |                                  |
|                  | JD1_RISE_EINT1           |                                  |
| R6214 (0x1846)   | IM_MICD_CLAMP_FALL_EINT1 |                                  |
|                  | IM_MICD_CLAMP_RISE_EINT1 |                                  |
|                  | IM_JD2_FALL_EINT1        |                                  |
|                  | IM_JD2_RISE_EINT1        |                                  |
|                  | IM_JD1_FALL_EINT1        |                                  |
|                  | IM_JD1_RISE_EINT1        |                                  |
| R6784 (0x1A80)   | IM_IRQ1                  |                                  |
|                  | IRQ_POL                  |                                  |
|                  | IRQ_OP_CFG               |                                  |
| R6864 (0x1AD0)   | RESET_PU                 | See <a href="#">Section 4.23</a> |
|                  | RESET_PD                 |                                  |

The always-on digital I/O pins are listed in [Table 4-82](#). All other digital input pins have no effect in Sleep Mode; all other digital output pins are undriven (floating).

The  $\overline{\text{IRQ}}$  output is normally deasserted in Sleep Mode. In Sleep Mode, the  $\overline{\text{IRQ}}$  output can be asserted only in response to the JACKDET1 or JACKDET2 inputs. If the  $\overline{\text{IRQ}}$  output is asserted in Sleep Mode, it can be deasserted only after a wake-up transition.

Output drivers and bus keepers are disabled in Sleep Mode, for all pins not on the always-on domain; this means that the logic level on these pins is undefined. If a defined logic state is required during Sleep Mode (e.g., as input to another device), an external pull resistor may be required. If an external pull resistor is connected to a pin that also supports a bus keeper function, the pull resistance should be chosen carefully, taking into account the resistance of the bus keeper. See [Section 4.14.1](#) for specific notes concerning the GPIO pins.

**Table 4-82. Sleep Mode Always-On Digital Input/Output Pins**

| Pin Name                  | Description                      | Reference                        |
|---------------------------|----------------------------------|----------------------------------|
| $\overline{\text{IRQ}}$   | Interrupt Request output         | See <a href="#">Section 4.15</a> |
| JACKDET1                  | Jack Detect input 1              | See <a href="#">Section 4.12</a> |
| JACKDET2                  | Jack Detect input 2              | See <a href="#">Section 4.12</a> |
| $\overline{\text{RESET}}$ | Digital Reset input (active low) | See <a href="#">Section 4.23</a> |

The always-on functionality includes the JD1 and JD2 control signals, which provide support for the low-power Sleep Mode. The MICDET clamp status signal is also supported; this is controlled by a selectable logic function, derived from JD1 and/or JD2.

The JD1, JD2 and MICDET clamp status signals are derived from the JACKDET1 and JACKDET2 inputs, and can be used to trigger the interrupt controller.

- The JD1 and JD2 signals are derived from the jack detect function (see [Section 4.12](#)). These inputs can be used to trigger a response to a jack insertion or jack removal detection.

When these signals are enabled, the JD1 and JD2 signals indicate the status of the JACKDET1 and JACKDET2 input pins respectively. See [Table 4-74](#) for details of the associated control fields.

- The MICDET clamp status is controlled by the JD1 and/or JD2 signals (see [Section 4.12](#)). The configurable logic provides flexibility in selecting the appropriate conditions for activating the MICDET clamp. The clamp status can be used to trigger a response to a jack insertion or jack removal detection.

The MICDET clamp function is configured using MICD\_CLAMP\_MODE, as described in [Table 4-75](#).

The interrupt functionality associated with these signals is part of the always-on functionality, enabling the CS47L35 to provide indication of jack insertion or jack removal to the host processor in Sleep Mode; see [Section 4.15](#).

Note that the JACKDET1 and JACKDET2 inputs do not result in a wake-up transition directly; a wake-up transition only occurs by reapplication of DCVDD. In a typical application, the JACKDET $n$  inputs provide a signal to the applications processor, via the  $\overline{\text{IRQ}}$  output; if a wake-up transition is required, this is triggered by the applications processor enabling the DCVDD supply.

## 4.14 General-Purpose I/O

The CS47L35 provides a number of GPIO functions to enable interfacing and detection of external hardware and to provide logic outputs to other devices. The GPIO input functions can be used to generate an interrupt (IRQ) event. The GPIO and interrupt circuits support the following functions:

- Pin-specific alternative functions for external interfaces (AIF, DMIC, PDM, MIF)
- Logic input/button detect (GPIO input)
- Logic 1 and Logic 0 output (GPIO output)
- Interrupt (IRQ) status output
- Clock output
- Frequency-locked loop (FLL) status output
- FLL clock output
- IEC-60958-3-compatible S/PDIF output
- Pulse-width modulation (PWM) signal output
- Overtemperature, speaker short-circuit protection, and speaker shutdown status output
- General-purpose timer status output
- Event logger FIFO buffer status output

Note that the GPIO pins are referenced to different power domains (DBVDD1 or DBVDD2), as indicated in [Table 1-1](#).

Logic input and output (GPIO) can be supported in two different ways on the CS47L35. The standard mechanism described in this section provides a comprehensive suite of options including input debounce, and selectable output drive configuration. The DSP GPIO circuit is tailored towards more advanced requirements typically demanded by DSP software features. The DSP GPIO functions are described in [Section 4.5.4](#).

The CS47L35 also incorporates a general-purpose switch feature, which can be used as a controllable analog switch, as described in [Section 4.14.16](#).

#### 4.14.1 GPIO Control

For each GPIO, the selected function is determined by the  $GPn\_FN$  field, where  $n$  identifies the GPIO pin (1–16). The pin direction, set by  $GPn\_DIR$ , must be set according to function selected by  $GPn\_FN$ .

If a pin is configured as a GPIO input ( $GPn\_DIR = 1$ ,  $GPn\_FN = 0x001$ ), the logic level at the pin can be read from the respective  $GPn\_LVL$  bit. Note that  $GPn\_LVL$  is not affected by the  $GPn\_POL$  bit.

A debounce circuit can be enabled on any GPIO input, to avoid false event triggers. This is enabled on each pin by setting the respective  $GPn\_DB$  bit. The debounce circuit uses the 32-kHz clock, which must be enabled whenever input debounce functions are required. The debounce time is configurable using the  $GP\_DBTIME$  field. See [Section 4.16](#) for further details of the CS47L35 clocking configuration.

Each of the GPIO pins is an input to the interrupt control circuit and can be used to trigger an interrupt event. An interrupt event is triggered on the rising and falling edges of the GPIO input. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See [Section 4.15](#) for details of the interrupt event handling.

Integrated pull-up and pull-down resistors are provided on each of the GPIO pins; these can be configured independently using the  $GPn\_PU$  and  $GPn\_PD$  fields. When the pull-up and pull-down control bits are both enabled, the CS47L35 provides a bus keeper function on the respective pin. The bus keeper function holds the logic level unchanged whenever the pin is undriven (e.g., if the signal is tristated).

**Note:** The bus keeper is enabled by default on all GPIO pins and, if not actively driven, may result in either a Logic 0 or Logic 1 at the respective input on start-up. If an external pull resistor is connected (e.g., to control the logic level in Sleep Mode), the chosen resistance should take account of the bus keeper resistance (see [Table 3-10](#)). A strong pull resistor (e.g., 10 k $\Omega$ ) is required, if a specific start-up condition is to be forced by the external pull component.

If a pin is configured as a GPIO output ( $GPn\_DIR = 0$ ,  $GPn\_FN = 0x001$ ), its level can be set to Logic 0 or Logic 1 using the  $GPn\_LVL$  field. Note that the  $GPn\_LVL$  bits are write-only when the respective GPIO pin is configured as an output.

If a pin is configured as an output ( $GPn\_DIR = 0$ ), the polarity can be inverted using the  $GPn\_POL$  bit. When  $GPn\_POL = 1$ , the selected output function is inverted. In the case of logic level output ( $GPn\_FN = 0x001$ ), the external output is the opposite logic level to  $GPn\_LVL$  when  $GPn\_POL = 1$ . Note that, if  $GPn\_FN = 0x000$  or  $0x002$ , the  $GPn\_POL$  bit has no effect on the respective GPIO pin.

A GPIO output can be either CMOS driven or open drain. This is selected on each pin using the respective  $GPn\_OP\_CFG$  bit. Note that if  $GPn\_FN = 0x000$  the  $GPn\_OP\_CFG$  bit has no effect on the respective GPIO pin—see [Table 4-83](#) for further details. If  $GPn\_FN = 0x002$ , the respective pin output is CMOS.

The register fields that control the GPIO pins are described in [Table 4-83](#).

**Table 4-83. GPIO Control**

| Register Address                                                        | Bit | Label          | Default        | Description                                                                                                                                                                                                                                                                                                                                  |
|-------------------------------------------------------------------------|-----|----------------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R5888 (0x1700)<br>GPIO1_CTRL_1<br>to<br>R5918 (0x171E)<br>GPIO16_CTRL_1 | 15  | GPn_LVL        | See Footnote 2 | GPIO <sub>n</sub> level. Write to this bit to set a GPIO output. Read from this bit to read GPIO input level.<br>For output functions only, if GPn_POL is set, the GPn_LVL bit is the opposite logic level to the external pin.<br>Note that, if GPn_DIR = 0, the GPn_LVL bit is write-only.                                                 |
|                                                                         | 14  | GPn_OP_CFG     | 0              | GPIO <sub>n</sub> Output Configuration<br>0 = CMOS<br>1 = Open drain<br>Note that, if GPn_FN = 0x000 or 0x002, this bit has no effect on the GPIO <sub>n</sub> output. If GPn_FN = 0x000, the pin configuration is set according to the applicable pin-specific function (see Table 4-85). If GPn_FN = 0x002, the pin configuration is CMOS. |
|                                                                         | 13  | GPn_DB         | 1              | GPIO <sub>n</sub> Input Debounce<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                              |
|                                                                         | 12  | GPn_POL        | 0              | GPIO <sub>n</sub> Output Polarity Select<br>0 = Noninverted (Active High)<br>1 = Inverted (Active Low)<br>Note that, if GPn_FN = 0x000 or 0x002, this bit has no effect on the GPIO <sub>n</sub> output.                                                                                                                                     |
|                                                                         | 8:0 | GPn_FN[8:0]    | 0x001          | GPIO <sub>n</sub> Pin Function<br>(see Table 4-84 for details)                                                                                                                                                                                                                                                                               |
| R5889 (0x1701)<br>GPIO1_CTRL_2<br>to<br>R5919 (0x171F)<br>GPIO16_CTRL_2 | 15  | GPn_DIR        | 1              | GPIO <sub>n</sub> Pin Direction<br>0 = Output<br>1 = Input<br>The GPn_DIR bit has no effect if GPn_FN = 0x000 or 0x002. If GPn_FN = 0x000, the pin direction is set according to the applicable pin-specific function (see Table 4-85). If GPn_FN = 0x002, the pin direction is set according to the DSP GPIO configuration.                 |
|                                                                         | 14  | GPn_PU         | 1              | GPIO <sub>n</sub> Pull-Up Enable<br>0 = Disabled<br>1 = Enabled<br><b>Note:</b> If GPn_PD and GPn_PU are both set, a bus keeper function is enabled on the respective GPIO <sub>n</sub> pin.                                                                                                                                                 |
|                                                                         | 13  | GPn_PD         | 1              | GPIO <sub>n</sub> Pull-Down Enable<br>0 = Disabled<br>1 = Enabled<br><b>Note:</b> If GPn_PD and GPn_PU are both set, a bus keeper function is enabled on the respective GPIO <sub>n</sub> pin.                                                                                                                                               |
| R6848 (0x1AC0)<br>GPIO_Debounce_<br>Config                              | 3:0 | GP_DBTIME[3:0] | 0000           | GPIO Input debounce time<br>0x0 = 100 μs<br>0x1 = 1.5 ms<br>0x2 = 3 ms<br>0x3 = 6 ms<br>0x4 = 12 ms<br>0x5 = 24 ms<br>0x6 = 48 ms<br>0x7 = 96 ms<br>0x8 = 192 ms<br>0x9 = 384 ms<br>0xA = 768 ms<br>0xB to 0xF = Reserved                                                                                                                    |

1. *n* is a number (1–16) that identifies the individual GPIO.

2. The default value of GPn\_LVL depends upon whether the pin is actively driven by another device. If the pin is actively driven, the bus keeper maintains this logic level. If the pin is not actively driven, the bus keeper may establish either a Logic 1 or Logic 0 as the initial input level.

### 4.14.2 GPIO Function Select

The available GPIO functions are described in [Table 4-84](#). The function of each GPIO is set using  $GPn\_FN$ , where  $n$  identifies the GPIO pin (1–16). Note that the respective  $GPn\_DIR$  must also be set according to whether the function is an input or output.

**Table 4-84. GPIO Function Select**

| <b><math>GPn\_FN</math></b> | <b>Description</b>                     | <b>Comments</b>                                                                                                                                                     |
|-----------------------------|----------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x000                       | Pin-specific alternate function        | Alternate functions supporting digital microphone, digital audio interface, master control interface, and PDM output functions.                                     |
| 0x001                       | Button-detect input/logic-level output | $GPn\_DIR = 0$ : GPIO pin logic level is set by $GPn\_LVL$ .<br>$GPn\_DIR = 1$ : Button detect or logic level input.                                                |
| 0x002                       | DSP GPIO                               | Low latency input/output for DSP functions.                                                                                                                         |
| 0x003                       | IRQ1 output                            | Interrupt (IRQ1) output<br>0 = IRQ1 not asserted<br>1 = IRQ1 asserted                                                                                               |
| 0x004                       | IRQ2 output                            | Interrupt (IRQ2) output<br>0 = IRQ2 not asserted<br>1 = IRQ2 asserted                                                                                               |
| 0x010                       | FLL1 clock                             | Clock output from FLL1                                                                                                                                              |
| 0x018                       | FLL1 lock                              | Indicates FLL1 lock status<br>0 = Not locked<br>1 = Locked                                                                                                          |
| 0x040                       | OPCLK clock output                     | Configurable clock output derived from SYSCLK                                                                                                                       |
| 0x048                       | PWM1 output                            | Configurable PWM output PWM1                                                                                                                                        |
| 0x049                       | PWM2 output                            | Configurable PWM output PWM2                                                                                                                                        |
| 0x04C                       | S/PDIF output                          | IEC-60958-3-compatible S/PDIF output                                                                                                                                |
| 0x0B6                       | SPKOUTL short circuit status           | SPKOUT short circuit status<br>0 = Normal<br>1 = Short Circuit detected                                                                                             |
| 0x0E0                       | Speaker shutdown status                | Speaker shutdown status<br>0 = Normal<br>1 = Speaker shutdown completed (due to overheat temperature, short-circuit protection, or general-purpose timer condition) |
| 0x0E1                       | Speaker overheat shutdown              | Indicates shutdown temperature status<br>0 = Temperature is below shutdown level<br>1 = Temperature is above shutdown level                                         |
| 0x0E2                       | Speaker overheat warning               | Indicates warning temperature status<br>0 = Temperature is below warning level<br>1 = Temperature is above warning level                                            |
| 0x140                       | Timer 1 status                         | Timer $n$ status<br>A pulse is output after the respective timer reaches its final count value.                                                                     |
| 0x141                       | Timer 2 status                         |                                                                                                                                                                     |
| 0x142                       | Timer 3 status                         |                                                                                                                                                                     |
| 0x143                       | Timer 4 status                         |                                                                                                                                                                     |
| 0x150                       | Event Log 1 FIFO not-empty status      | Event Log $n$ FIFO Not-Empty status<br>0 = FIFO Empty<br>1 = FIFO Not Empty                                                                                         |
| 0x151                       | Event Log 2 FIFO not-empty status      |                                                                                                                                                                     |
| 0x152                       | Event Log 3 FIFO not-empty status      |                                                                                                                                                                     |
| 0x153                       | Event Log 4 FIFO not-empty status      |                                                                                                                                                                     |

### 4.14.3 Pin-Specific Alternative Function— $GPn\_FN = 0x000$

The CS47L35 GPIO capability is multiplexed with the pin-specific functions listed in [Table 4-85](#). The alternate functions are selected by setting the respective  $GPn\_FN$  fields to 0x000, as described in [Section 4.14.1](#). Note that each function is unique to the associated pin and can be supported only on that pin.

If the alternate function is selected on a GPIO pin, the pin direction (input or output) and the output driver configuration (CMOS or open drain) are set automatically as described in [Table 4-85](#). The respective  $GPn\_DIR$  and  $GPn\_OP\_CFG$  bits have no effect in this case.

**Table 4-85. GPIO Alternate Functions**

| Name             | Condition       | Description                                 | Direction      | Output Driver Configuration |
|------------------|-----------------|---------------------------------------------|----------------|-----------------------------|
| AIF1BCLK/GPIO9   | GP9_FN = 0x000  | Audio Interface 1 bit clock                 | Digital I/O    | CMOS                        |
| AIF1LRCLK/GPIO11 | GP11_FN = 0x000 | Audio Interface 1 left/right clock          | Digital I/O    | CMOS                        |
| AIF1RXDAT/GPIO8  | GP8_FN = 0x000  | Audio Interface 1 RX digital audio data     | Digital input  | CMOS                        |
| AIF1TXDAT/GPIO10 | GP10_FN = 0x000 | Audio Interface 1 TX digital audio data     | Digital output | CMOS                        |
| AIF2BCLK/GPIO13  | GP13_FN = 0x000 | Audio Interface 2 bit clock                 | Digital I/O    | CMOS                        |
| AIF2LRCLK/GPIO15 | GP15_FN = 0x000 | Audio Interface 2 left/right clock          | Digital I/O    | CMOS                        |
| AIF2RXDAT/GPIO14 | GP14_FN = 0x000 | Audio Interface 2 RX digital audio data     | Digital input  | CMOS                        |
| AIF2TXDAT/GPIO12 | GP12_FN = 0x000 | Audio Interface 2 TX digital audio data     | Digital output | CMOS                        |
| AIF3BCLK/GPIO2   | GP2_FN = 0x000  | Audio Interface 3 bit clock                 | Digital I/O    | CMOS                        |
| AIF3LRCLK/GPIO4  | GP4_FN = 0x000  | Audio Interface 3 left/right clock          | Digital I/O    | CMOS                        |
| AIF3RXDAT/GPIO3  | GP3_FN = 0x000  | Audio Interface 3 RX digital audio data     | Digital input  | CMOS                        |
| AIF3TXDAT/GPIO1  | GP1_FN = 0x000  | Audio Interface 3 TX digital audio data     | Digital output | CMOS                        |
| MIF1SCLK/GPIO16  | GP16_FN = 0x000 | Master (I <sup>2</sup> C) Interface 1 clock | Digital output | Open drain                  |
| MIF1SDA/GPIO7    | GP7_FN = 0x000  | Master (I <sup>2</sup> C) Interface 1 data  | Digital I/O    | Open drain                  |
| SPKCLK/GPIO6     | GP6_FN = 0x000  | Digital speaker (PDM) clock                 | Digital output | CMOS                        |
| SPKDAT/GPIO5     | GP5_FN = 0x000  | Digital speaker (PDM) data                  | Digital output | CMOS                        |

#### 4.14.4 Button Detect (GPIO Input)—GPn\_FN = 0x001

Button-detect functionality can be selected on a GPIO pin by setting the respective GPIO fields as described in [Section 4.14.1](#). The same functionality can be used to support a jack-detect input function.

It is recommended to enable the GPIO input debounce feature when using GPIOs as button input or jack-detect input.

The GPn\_LVL fields may be read to determine the logic levels on a GPIO input, after the selectable debounce controls. Note that GPn\_LVL is not affected by the GPn\_POL bit.

The debounced GPIO signals are also inputs to the interrupt-control circuit. An interrupt event is triggered on the rising and falling edges of the GPIO input. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See [Section 4.15](#) for details of the interrupt event handling.

#### 4.14.5 Logic 1 and Logic 0 Output (GPIO Output)—GPn\_FN = 0x001

The CS47L35 can be programmed to drive a logic high or logic low level on a GPIO pin by selecting the GPIO Output function as described in [Section 4.14.1](#).

The output logic level is selected using the respective GPn\_LVL bit. Note that, if a GPIO pin is configured as an output, the respective GPn\_LVL bits are write-only.

The polarity of the GPIO output can be inverted using the GPn\_POL bits. If GPn\_POL = 1, the external output is the opposite logic level to GPn\_LVL.

#### 4.14.6 DSP GPIO (Low-Latency DSP Input/Output)—GPn\_FN = 0x002

The DSP GPIO function provides an advanced I/O capability, supporting the requirements of the CS47L35 as a multipurpose sensor hub. The DSP GPIO pins are accessed using maskable sets of I/O control registers; this allows the selected combinations of GPIOs to be controlled with ease, regardless of how the allocation of GPIO pins has been implemented in hardware.

The DSP GPIO function is selected by setting the respective GPIO fields as described in [Section 4.14.1](#).

A full description of the DSP GPIO function is provided in [Section 4.5.4](#).

Note that, if GPn\_FN is set to 0x002, the respective pin direction (input or output) is set according to the DSP GPIO configuration for that pin—the GPn\_DIR control bit has no effect in this case.

#### 4.14.7 Interrupt (IRQ) Status Output—GPn\_FN = 0x003, 0x004

The CS47L35 has an interrupt controller, which can be used to indicate when any selected interrupt events occur. Individual interrupts may be masked in order to configure the interrupt as required. See [Section 4.15](#) for full definition of all supported interrupt events.

The interrupt controller supports two separate interrupt request (IRQ) outputs. The IRQ1 or IRQ2 status may be output directly on a GPIO pin by setting the respective GPIO fields as described in [Section 4.14.1](#).

Note that the IRQ1 status is output on the  $\overline{\text{IRQ}}$  pin at all times.

#### 4.14.8 Frequency-Locked Loop (FLL) Clock Output—GPn\_FN = 0x010

A clock output derived from the FLL may be output on a GPIO pin. The GPIO output from the FLL is controlled by FLL1\_GPCLK\_DIV and FLL1\_GPCLK\_ENA, as described in [Table 4-86](#).

It is recommended to disable the clock output (FLL1\_GPCLK\_ENA = 0) before making any change to the FLL1\_GPCLK\_DIV field.

Note that FLL1\_GPCLK\_DIV and FLL1\_GPCLK\_ENA affect the GPIO outputs only; they do not affect the FLL frequency. The maximum output frequency supported for GPIO output is noted in [Table 3-10](#).

The FLL clock output may be output directly on a GPIO pin by setting the respective GPIO fields as described in [Section 4.14.1](#).

See [Section 4.16](#) for details of the CS47L35 system clocking and how to configure the FLL.

**Table 4-86. FLL Clock Output Control**

| Register Address                 | Bit | Label               | Default | Description                                                                                                                                                                                                                                 |
|----------------------------------|-----|---------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R392 (0x0188)<br>FLL1_GPIO_Clock | 7:1 | FLL1_GPCLK_DIV[6:0] | 0x06    | FLL1 GPIO Clock Divider<br>0x00 to 0x05 = Reserved<br>0x06 = Divide by 6<br>0x07 = Divide by 7<br>0x08 = Divide by 8<br>0x09 = Divide by 9<br>...<br>0x7F = Divide by 127<br>( $F_{\text{GPIO}} = F_{\text{VCO}}/\text{FLL1\_GPCLK\_DIV}$ ) |
|                                  | 0   | FLL1_GPCLK_ENA      | 0       | FLL1 GPIO Clock Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                       |

#### 4.14.9 Frequency-Locked Loop (FLL) Status Output—GPn\_FN = 0x018

The CS47L35 provides an FLL status flag, which may be used to control other events. The FLL lock signal indicates whether FLL lock has been achieved. See [Section 4.16.9](#) for details of the FLL.

The FLL lock signal may be output directly on a GPIO pin by setting the respective GPIO fields as described in [Section 4.14.1](#).

The FLL lock signal is an input to the interrupt controller circuit. An interrupt event is triggered on the rising and falling edges of this signal. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See [Section 4.15](#) for details of the interrupt event handling.

#### 4.14.10 OPCLK Clock Output—GPn\_FN = 0x040

A clock output (OPCLK) derived from SYSCLK can be output on a GPIO pin. The OPCLK frequency is controlled by OPCLK\_DIV and OPCLK\_SEL. The OPCLK output is enabled by setting OPCLK\_ENA, as described in [Table 4-87](#).

It is recommended to disable the clock output (OPCLK\_ENA = 0) before making any change to OPCLK\_DIV or OPCLK\_SEL.

The OPCLK output should be kept disabled (OPCLK\_ENA = 0) if SYSCLK is not enabled. SYSCLK must be present and enabled before setting the OPCLK\_ENA bit. See [Section 4.16.4](#) for further details (including requirements for reconfiguring SYSCLK while digital core functions are enabled).

The OPCLK clock can be output directly on a GPIO pin by setting the respective GPIO fields as described in [Section 4.14.1](#).

Note that the OPCLK source frequency cannot be higher than the SYSCLK frequency. The maximum output frequency supported for GPIO output is noted in [Table 3-10](#).

See [Section 4.16](#) for details of the SYSCLK system clock.

**Table 4-87. OPCLK Control**

| Register Address                         | Bit | Label          | Default | Description                                                                                                                                                                                                                                                                                                                                                                               |
|------------------------------------------|-----|----------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R329 (0x0149)<br>Output_system_<br>clock | 15  | OPCLK_ENA      | 0       | OPCLK Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                               |
|                                          | 7:3 | OPCLK_DIV[4:0] | 0x00    | OPCLK Divider<br>0x02 = Divide by 2<br>0x04 = Divide by 4<br>0x06 = Divide by 6<br>... (even numbers only)<br>0x1E = Divide by 30<br>Note that only even numbered divisions (2, 4, 6, etc.) are valid selections.<br>All other codes are reserved when the OPCLK signal is enabled.                                                                                                       |
|                                          | 2:0 | OPCLK_SEL[2:0] | 000     | OPCLK Source Frequency<br>000 = 6.144 MHz (5.6448 MHz)<br>001 = 12.288 MHz (11.2896 MHz)<br>010 = 24.576 MHz (22.5792 MHz)<br>011 = 49.152 MHz (45.1584 MHz)<br>All other codes are reserved<br>The frequencies in brackets apply for 44.1 kHz–related SYSCLK rates only (i.e., SAMPLE_RATE_n = 01XXX).<br>The OPCLK Source Frequency must be less than or equal to the SYSCLK frequency. |

#### 4.14.11 Pulse-Width Modulation (PWM) Signal Output—GPn\_FN = 0x048, 0x049

The CS47L35 incorporates two PWM signal generators, which can be enabled as GPIO outputs. The duty cycle of each PWM signal can be modulated by an audio source, or can be set to a fixed value using a control register setting.

The PWM outputs may be output directly on a GPIO pin by setting the respective GPIO fields as described in [Section 4.14.1](#).

See [Section 4.3.12](#) for details of how to configure the PWM signal generators.

#### 4.14.12 S/PDIF Audio Output—GPn\_FN = 0x04C

The CS47L35 incorporates an IEC-60958-3–compatible S/PDIF transmitter, which can be selected as a GPIO output. The S/PDIF transmitter supports stereo audio channels and allows full control over the S/PDIF validity bits and channel status information.

The S/PDIF signal may be output directly on a GPIO pin by setting the respective GPIO fields as described in [Section 4.14.1](#).

See [Section 4.3.8](#) for details of how to configure the S/PDIF output generator.

#### 4.14.13 Overtemperature, Short-Circuit Protection, and Speaker Shutdown Status Output— GPn\_FN = 0x0B6, 0x0E0, 0x0E1, 0x0E2.

The CS47L35 incorporates a temperature sensor, which detects when the device temperature is within normal limits or if the device is approaching a hazardous temperature condition.

The temperature status may be output directly on a GPIO pin by setting the respective GPIO fields as described in [Section 4.14.1](#). A GPIO pin can be used to indicate either an Overheat Warning Temperature event or an Overheat Shutdown Temperature event.

The CS47L35 provides short-circuit protection on the Class D speaker outputs, and on each of the headphone output paths.

The status of the Class D speaker short-circuit detection circuits may be output directly on a GPIO pin by setting the respective GPIO fields as described in [Section 4.14.1](#).

If the Overheat Shutdown Temperature is exceeded, or if a short circuit is detected on the Class D speaker outputs, the Class D speaker outputs are automatically disabled in order to protect the device. The general-purpose timers can be used as a watchdog function to trigger a shutdown of the Class D speaker drivers. Further details of the Speaker Shutdown functions are described in [Section 4.21](#). When the speaker driver shutdown is complete, the Speaker Shutdown signal is asserted. The speaker driver shutdown status can also be output directly on a GPIO pin.

The Overtemperature, short-circuit protection, and Speaker Shutdown status flags are inputs to the interrupt control circuit. An interrupt event may be triggered on the applicable edges of these signals. The associated interrupt bit is latched once set; it can be polled at any time or used to control the IRQ signal. See [Section 4.15](#) for details of the interrupt event handling.

#### 4.14.14 General-Purpose Timer Status Output—GPn\_FN = 0x140–0x143

The general-purpose timers can count up or down, and support continuous or single count modes. Status outputs indicating the progress of these timers are provided. See [Section 4.5.3](#) for details of the general-purpose timers.

A logic signal from the general-purpose timers may be output directly on a GPIO pin by setting the respective GPIO fields as described in [Section 4.14.1](#). This logic signal is pulsed high whenever the respective timer reaches its final count value.

The general-purpose timers also provide inputs to the interrupt control circuit. An interrupt event is triggered whenever the respective timer reaches its final count value. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See [Section 4.15](#) for details of the interrupt event handling.

#### 4.14.15 Event Logger FIFO Buffer Status Output—GPn\_FN = 0x150–0x153

The event loggers are each provided with a 16-stage FIFO buffer, in which any detected events (signal transitions) are recorded. Status outputs for each FIFO buffer are provided. See [Section 4.5.2](#) for details of the event loggers.

A logic signal from the event loggers may be output directly on a GPIO pin by setting the respective GPIO fields as described in [Section 4.14.1](#). This logic signal is set high whenever the FIFO not-empty condition is true.

The event loggers also provide inputs to the interrupt control circuit. An interrupt event is triggered whenever the respective FIFO condition occurs. The associated interrupt bits are latched once set; they can be polled at any time or used to control the IRQ signal. See [Section 4.15](#) for details of the interrupt event handling.

#### 4.14.16 General-Purpose Switch

The CS47L35 provides a general-purpose switch, which can be used as a controllable analog switch for external functions. The switch is implemented between the GPSWP and GPSWN pins. Note that this feature is entirely independent of the GPIO pins.

The general-purpose switch is configured using SW1\_MODE. This field allows the switch to be disabled, enabled, or synchronized to the MICDET clamp status, as described in [Table 4-88](#).

The switch is a bidirectional analog switch, offering flexibility in the potential circuit applications. Refer to [Table 3-2](#) and [Table 3-10](#) for further details.

The switch can be used in conjunction with the MICDET clamp function to suppress pops and clicks associated with jack insertion and removal. An example circuit is shown in [Fig. 4-58](#) within the [External Accessory Detection](#) section. Note that the MICDET clamp function must also be configured appropriately when using this method of pop suppression.

**Table 4-88. General-Purpose Switch Control**

| Register Address             | Bit | Label         | Default | Description                                                                                                                                                                 |
|------------------------------|-----|---------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R712 (0x02C8)<br>GP_Switch_1 | 1:0 | SW1_MODE[1:0] | 00      | General-purpose Switch control<br>00 = Disabled (open)<br>01 = Enabled (closed)<br>10 = Enabled when MICDET clamp is active<br>11 = Enabled when MICDET clamp is not active |

## 4.15 Interrupts

The interrupt controller has multiple inputs. These include the jack detect and GPIO input pins, DSP\_IRQn flags, headphone/accessory detection, FLL lock detection, and status flags from DSP peripheral functions. See [Table 4-89](#) and [Table 4-90](#) for a full definition of the interrupt controller inputs. Any combination of these inputs can be used to trigger an interrupt request event.

The interrupt controller supports two sets of interrupt registers. This allows two separate interrupt request (IRQ) outputs to be generated, and for each IRQ to report a different set of input or status conditions.

For each interrupt request (IRQ1 and IRQ2) output, there is an interrupt register field associated with each of the interrupt inputs. These fields are asserted whenever a logic edge is detected on the respective input. Some inputs are triggered on rising edges only; some are triggered on both edges. Separate rising and falling interrupt bits are provided for the JD1 and JD2 signals. The interrupt register fields for IRQ1 are described in [Table 4-89](#). The interrupt register fields for IRQ2 are described in [Table 4-90](#). The interrupt flags can be polled at any time or in response to the interrupt request output being signaled via the IRQ pin or a GPIO pin.

All interrupts are edge triggered, as noted above. Many are triggered on both the rising and falling edges and, therefore, the interrupt bits cannot indicate which edge has been detected. The raw status fields described in [Table 4-89](#) and [Table 4-90](#) indicate the current value of the corresponding inputs to the interrupt controller. Note that the raw status bits associated with IRQ1 and IRQ2 provide the same information. The status of any GPIO (or DSP GPIO) inputs can also be read using the GPIO (or DSP GPIO) control fields, as described in [Table 4-83](#) and [Table 4-34](#).

Individual mask bits can enable or disable different functions from the interrupt controller. The mask bits are described in [Table 4-89](#) (for IRQ1) and [Table 4-90](#) (for IRQ2). Note that a masked interrupt input does not assert the corresponding interrupt register field and does not cause the associated interrupt request output to be asserted.

The interrupt request outputs represent the logical OR of the associated interrupt registers. IRQ1 is derived from the x\_EINT1 registers; IRQ2 is derived from the x\_EINT2 registers. The interrupt register fields are latching fields and, once they are set, they are not reset until a 1 is written to the respective bits. The interrupt request outputs are not reset until each of the associated interrupts has been reset.

A debounce circuit can be enabled on any GPIO input, to avoid false event triggers. This is enabled on each pin using the fields described in [Table 4-83](#). The GPIO debounce circuit uses the 32-kHz clock, which must be enabled whenever the GPIO debounce function is required.

A debounce circuit is always enabled on the FLL status inputs; to trigger an interrupt from the FLL status inputs, the 32-kHz clock or the SYSCLK signal must be enabled. Note that the raw status fields (described in [Table 4-89](#) and [Table 4-90](#)) are valid without clocking, and can be used to provide FLL status indication when system clocks are not available.

The IRQ outputs can be globally masked using the IM\_IRQ1 and IM\_IRQ2 bits. When not masked, the IRQ status can be read from IRQ1\_STS and IRQ2\_STS for the respective IRQ outputs.

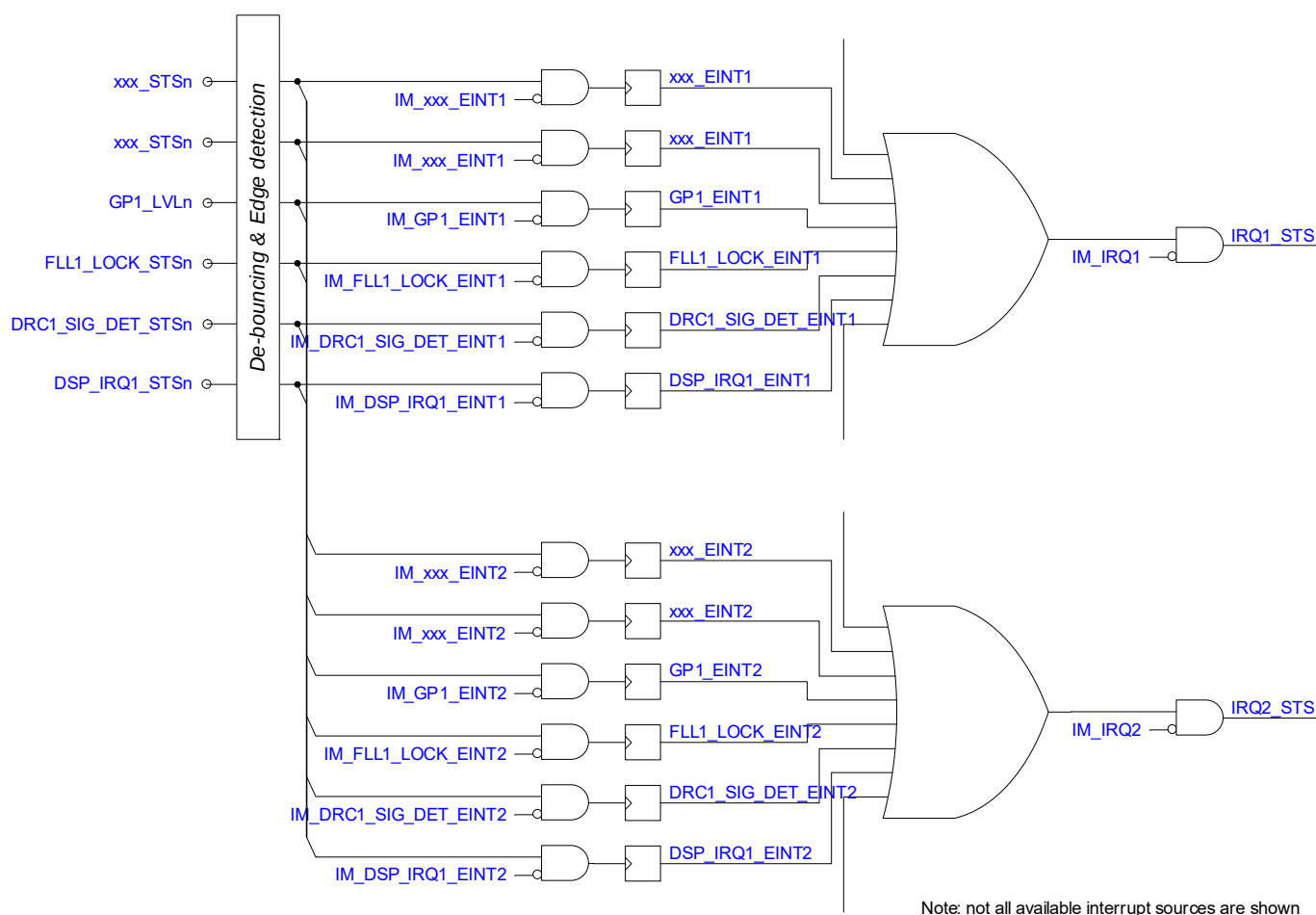
The IRQ1 output is provided externally on the  $\overline{\text{IRQ}}$  pin. Under default conditions, this output is active low. The polarity can be inverted using  $\text{IRQ\_POL}$ . The  $\overline{\text{IRQ}}$  output can be either CMOS driven or open drain; this is selected using the  $\text{IRQ\_OP\_CFG}$  bit. The  $\overline{\text{IRQ}}$  output is referenced to the DBVDD1 power domain.

The IRQ2 status can be used to trigger DSP firmware execution; see [Section 4.4](#). This allows the DSP firmware execution to be linked to external events (e.g., jack detection, or GPIO input), or to any of the status conditions flagged by the interrupt registers.

The IRQ1 and IRQ2 signals may be output on a GPIO pin; see [Section 4.14](#).

The CS47L35 interrupt controller circuit is shown in [Fig. 4-62](#). (Note that not all interrupt inputs are shown.) The control fields associated with IRQ1 and IRQ2 are described in [Table 4-89](#) and [Table 4-90](#) respectively. The global interrupt mask bits, status bits, and output configuration fields are described [Table 4-91](#).

Note that, under default register conditions, the boot done status is the only unmasked interrupt source; a falling edge on the  $\overline{\text{IRQ}}$  pin indicates completion of the boot sequence.



**Figure 4-62. Interrupt Controller**

The IRQ1 interrupt, mask, and status control registers are described in [Table 4-89](#).

**Table 4-89. Interrupt 1 Control Registers**

| Register Address                | Bit | Label                    | Default | Description                                                                                             |
|---------------------------------|-----|--------------------------|---------|---------------------------------------------------------------------------------------------------------|
| R6144 (0x1800)<br>IRQ1_Status_1 | 15  | DSP_SHARED_WR_COLL_EINT1 | 0       | DSP Shared Memory Collision Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.     |
|                                 | 12  | CTRLIF_ERR_EINT1         | 0       | Control Interface Error Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.         |
|                                 | 9   | SYSCLK_FAIL_EINT1        | 0       | SYSCLK Fail Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                     |
|                                 | 7   | BOOT_DONE_EINT1          | 0       | Boot Done Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                       |
| R6145 (0x1801)<br>IRQ1_Status_2 | 8   | FLL1_LOCK_EINT1          | 0       | FLL1 Lock Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
| R6149 (0x1805)<br>IRQ1_Status_6 | 8   | MICDET_EINT1             | 0       | Microphone/Accessory Detect Interrupt (Detection event triggered)<br>Note: Cleared when a 1 is written. |
|                                 | 0   | HPDET_EINT1              | 0       | Headphone Detect Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                |
| R6150 (0x1806)<br>IRQ1_Status_7 | 5   | MICD_CLAMP_FALL_EINT1    | 0       | MICDET Clamp Interrupt (Falling edge triggered)<br>Note: Cleared when a 1 is written.                   |
|                                 | 4   | MICD_CLAMP_RISE_EINT1    | 0       | MICDET Clamp Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                    |
|                                 | 3   | JD2_FALL_EINT1           | 0       | JD2 Interrupt (Falling edge triggered)<br>Note: Cleared when a 1 is written.                            |
|                                 | 2   | JD2_RISE_EINT1           | 0       | JD2 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                             |
|                                 | 1   | JD1_FALL_EINT1           | 0       | JD1 Interrupt (Falling edge triggered)<br>Note: Cleared when a 1 is written.                            |
|                                 | 0   | JD1_RISE_EINT1           | 0       | JD1 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                             |
| R6152 (0x1808)<br>IRQ1_Status_9 | 1   | DRC2_SIG_DET_EINT1       | 0       | DRC2 Signal-Detect Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.  |
|                                 | 0   | DRC1_SIG_DET_EINT1       | 0       | DRC1 Signal-Detect Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.  |

**Table 4-89. Interrupt 1 Control Registers (Cont.)**

| Register Address                 | Bit | Label                      | Default | Description                                                                                              |
|----------------------------------|-----|----------------------------|---------|----------------------------------------------------------------------------------------------------------|
| R6154 (0x180A)<br>IRQ1_Status_11 | 15  | DSP_IRQ16_EINT1            | 0       | DSP IRQ16 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                        |
|                                  | 14  | DSP_IRQ15_EINT1            | 0       | DSP IRQ15 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                        |
|                                  | 13  | DSP_IRQ14_EINT1            | 0       | DSP IRQ14 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                        |
|                                  | 12  | DSP_IRQ13_EINT1            | 0       | DSP IRQ13 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                        |
|                                  | 11  | DSP_IRQ12_EINT1            | 0       | DSP IRQ12 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                        |
|                                  | 10  | DSP_IRQ11_EINT1            | 0       | DSP IRQ11 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                        |
|                                  | 9   | DSP_IRQ10_EINT1            | 0       | DSP IRQ10 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                        |
|                                  | 8   | DSP_IRQ9_EINT1             | 0       | DSP IRQ9 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 7   | DSP_IRQ8_EINT1             | 0       | DSP IRQ8 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 6   | DSP_IRQ7_EINT1             | 0       | DSP IRQ7 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 5   | DSP_IRQ6_EINT1             | 0       | DSP IRQ6 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 4   | DSP_IRQ5_EINT1             | 0       | DSP IRQ5 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 3   | DSP_IRQ4_EINT1             | 0       | DSP IRQ4 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 2   | DSP_IRQ3_EINT1             | 0       | DSP IRQ3 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 1   | DSP_IRQ2_EINT1             | 0       | DSP IRQ2 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 0   | DSP_IRQ1_EINT1             | 0       | DSP IRQ1 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
| R6155 (0x180B)<br>IRQ1_Status_12 | 6   | SPKOUTL_SC_EINT1           | 0       | SPKOUT Short Circuit Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written. |
|                                  | 3   | HP2R_SC_EINT1              | 0       | EPOUTN Short Circuit Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.             |
|                                  | 2   | HP2L_SC_EINT1              | 0       | EPOUTP Short Circuit Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.             |
|                                  | 1   | HP1R_SC_EINT1              | 0       | HPOUTR Short Circuit Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.             |
|                                  | 0   | HP1L_SC_EINT1              | 0       | HPOUTL Short Circuit Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.             |
| R6156 (0x180C)<br>IRQ1_Status_13 | 6   | SPKOUTL_ENABLE_DONE_EINT1  | 0       | SPKOUT Enable Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                    |
|                                  | 1   | HP1R_ENABLE_DONE_EINT1     | 0       | HPOUTR/EPOUTN Enable Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.             |
|                                  | 0   | HP1L_ENABLE_DONE_EINT1     | 0       | HPOUTL/EPOUTP Enable Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.             |
| R6157 (0x180D)<br>IRQ1_Status_14 | 6   | SPKOUTL_DISABLE_DONE_EINT1 | 0       | SPKOUTL Disable Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                  |
|                                  | 1   | HP1R_DISABLE_DONE_EINT1    | 0       | HPOUTR/EPOUTN Disable Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 0   | HP1L_DISABLE_DONE_EINT1    | 0       | HPOUTL/EPOUTP Disable Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.            |

**Table 4-89. Interrupt 1 Control Registers (Cont.)**

| Register Address                 | Bit | Label                   | Default | Description                                                                                          |
|----------------------------------|-----|-------------------------|---------|------------------------------------------------------------------------------------------------------|
| R6158 (0x180E)<br>IRQ1_Status_15 | 2   | SPK_OVERHEAT_WARN_EINT1 | 0       | Speaker Overheat Warning Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.     |
|                                  | 1   | SPK_OVERHEAT_EINT1      | 0       | Speaker Overheat Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.             |
|                                  | 0   | SPK_SHUTDOWN_EINT1      | 0       | Speaker Shutdown Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written. |
| R6160 (0x1810)<br>IRQ1_Status_17 | 15  | GP16_EINT1              | 0       | GPIO16 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
|                                  | 14  | GP15_EINT1              | 0       | GPIO15 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
|                                  | 13  | GP14_EINT1              | 0       | GPIO14 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
|                                  | 12  | GP13_EINT1              | 0       | GPIO13 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
|                                  | 11  | GP12_EINT1              | 0       | GPIO12 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
|                                  | 10  | GP11_EINT1              | 0       | GPIO11 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
|                                  | 9   | GP10_EINT1              | 0       | GPIO10 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
|                                  | 8   | GP9_EINT1               | 0       | GPIO9 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 7   | GP8_EINT1               | 0       | GPIO8 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 6   | GP7_EINT1               | 0       | GPIO7 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 5   | GP6_EINT1               | 0       | GPIO6 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 4   | GP5_EINT1               | 0       | GPIO5 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 3   | GP4_EINT1               | 0       | GPIO4 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 2   | GP3_EINT1               | 0       | GPIO3 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 1   | GP2_EINT1               | 0       | GPIO2 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 0   | GP1_EINT1               | 0       | GPIO1 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
| R6164 (0x1814)<br>IRQ1_Status_21 | 3   | TIMER4_EINT1            | 0       | Timer 4 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                      |
|                                  | 2   | TIMER3_EINT1            | 0       | Timer 3 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                      |
|                                  | 1   | TIMER2_EINT1            | 0       | Timer 2 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                      |
|                                  | 0   | TIMER1_EINT1            | 0       | Timer 1 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                      |
| R6165 (0x1815)<br>IRQ1_Status_22 | 3   | EVENT4_NOT_EMPTY_EINT1  | 0       | Event Log 4 FIFO Not Empty Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.   |
|                                  | 2   | EVENT3_NOT_EMPTY_EINT1  | 0       | Event Log 3 FIFO Not Empty Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.   |
|                                  | 1   | EVENT2_NOT_EMPTY_EINT1  | 0       | Event Log 2 FIFO Not Empty Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.   |
|                                  | 0   | EVENT1_NOT_EMPTY_EINT1  | 0       | Event Log 1 FIFO Not Empty Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.   |

**Table 4-89. Interrupt 1 Control Registers (Cont.)**

| Register Address                       | Bit | Label              | Default        | Description                                                                                                                                                                                             |
|----------------------------------------|-----|--------------------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R6166 (0x1816)<br>IRQ1_Status_23       | 3   | EVENT4_FULL_EINT1  | 0              | Event Log 4 FIFO Full Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                           |
|                                        | 2   | EVENT3_FULL_EINT1  | 0              | Event Log 3 FIFO Full Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                           |
|                                        | 1   | EVENT2_FULL_EINT1  | 0              | Event Log 2 FIFO Full Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                           |
|                                        | 0   | EVENT1_FULL_EINT1  | 0              | Event Log 1 FIFO Full Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                           |
| R6167 (0x1817)<br>IRQ1_Status_24       | 3   | EVENT4_WMARK_EINT1 | 0              | Event Log 4 FIFO Watermark Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                      |
|                                        | 2   | EVENT3_WMARK_EINT1 | 0              | Event Log 3 FIFO Watermark Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                      |
|                                        | 1   | EVENT2_WMARK_EINT1 | 0              | Event Log 2 FIFO Watermark Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                      |
|                                        | 0   | EVENT1_WMARK_EINT1 | 0              | Event Log 1 FIFO Watermark Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                      |
| R6168 (0x1818)<br>IRQ1_Status_25       | 2   | DSP3_DMA_EINT1     | 00             | DSP3 DMA Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                        |
|                                        | 1   | DSP2_DMA_EINT1     | 00             | DSP2 DMA Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                        |
|                                        | 0   | DSP1_DMA_EINT1     | 00             | DSP1 DMA Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                        |
| R6170 (0x181A)<br>IRQ1_Status_27       | 2   | DSP3_START1_EINT1  | 0              | DSP3 Start 1 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                    |
|                                        | 1   | DSP2_START1_EINT1  | 0              | DSP2 Start 1 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                    |
|                                        | 0   | DSP1_START1_EINT1  | 0              | DSP1 Start 1 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                    |
| R6171 (0x181B)<br>IRQ1_Status_28       | 2   | DSP3_START2_EINT1  | 0              | DSP3 Start 2 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                    |
|                                        | 1   | DSP2_START2_EINT1  | 0              | DSP2 Start 2 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                    |
|                                        | 0   | DSP1_START2_EINT1  | 0              | DSP1 Start 2 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                    |
| R6173 (0x181D)<br>IRQ1_Status_30       | 2   | DSP3_BUSY_EINT1    | 0              | DSP3 Busy Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                       |
|                                        | 1   | DSP2_BUSY_EINT1    | 0              | DSP2 Busy Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                       |
|                                        | 0   | DSP1_BUSY_EINT1    | 0              | DSP1 Busy Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                       |
| R6174 (0x181E)<br>IRQ1_Status_31       | 0   | MIF1_DONE_EINT1    | 0              | MIF1 Done Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                       |
| R6175 (0x181F)<br>IRQ1_Status_32       | 0   | MIF1_BLOCK_EINT1   | 0              | MIF1 Block Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                      |
| R6208 (0x1840)<br>to<br>R6239 (0x185F) |     | IM_*               | See Footnote 1 | For each x_EINT1 interrupt bit in R6144 to R6175, a corresponding mask bit (IM_*) is provided in R6208 to R6239. The mask bits are coded as follows:<br>0 = Do not mask interrupt<br>1 = Mask interrupt |
| R6272 (0x1880)<br>IRQ1_Raw_Status_1    | 12  | CTRLIF_ERR_STS1    | 0              | Control Interface Error Status<br>0 = Normal<br>1 = Control Interface Error                                                                                                                             |
|                                        | 7   | BOOT_DONE_STS1     | 0              | Boot Status<br>0 = Busy (boot sequence in progress)<br>1 = Idle (boot sequence completed)<br>Control register writes should not be attempted until Boot Sequence has completed.                         |

**Table 4-89. Interrupt 1 Control Registers (Cont.)**

| Register Address                         | Bit | Label                     | Default | Description                                                                                                                           |
|------------------------------------------|-----|---------------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------|
| R6273 (0x1881)<br>IRQ1_Raw_<br>Status_2  | 8   | FLL1_LOCK_STS1            | 0       | FLL1 Lock Status<br>0 = Not locked<br>1 = Locked                                                                                      |
| R6278 (0x1886)<br>IRQ1_Raw_<br>Status_7  | 4   | MICD_CLAMP_STS1           | 0       | MICDET Clamp status<br>0 = Clamp not active<br>1 = Clamp active                                                                       |
|                                          | 2   | JD2_STS1                  | 0       | JACKDET2 input status<br>0 = Jack not detected<br>1 = Jack is detected<br>(Assumes the JACKDET2 pin is pulled low on jack insertion.) |
|                                          | 0   | JD1_STS1                  | 0       | JACKDET1 input status<br>0 = Jack not detected<br>1 = Jack is detected<br>(Assumes the JACKDET1 pin is pulled low on jack insertion.) |
| R6280 (0x1888)<br>IRQ1_Raw_<br>Status_9  | 1   | DRC2_SIG_DET_STS1         | 0       | DRC2 Signal-Detect Status<br>0 = Normal<br>1 = Signal detected                                                                        |
|                                          | 0   | DRC1_SIG_DET_STS1         | 0       | DRC1 Signal-Detect Status<br>0 = Normal<br>1 = Signal detected                                                                        |
| R6283 (0x188B)<br>IRQ1_Raw_<br>Status_12 | 6   | SPKOUTL_SC_STS1           | 0       | SPKOUT Short Circuit Status<br>0 = Normal<br>1 = Short Circuit detected                                                               |
|                                          | 3   | HP2R_SC_STS1              | 0       | EPOUTN Short Circuit Status<br>0 = Normal<br>1 = Short Circuit detected                                                               |
|                                          | 2   | HP2L_SC_STS1              | 0       | EPOUTP Short Circuit Status<br>0 = Normal<br>1 = Short Circuit detected                                                               |
|                                          | 1   | HP1R_SC_STS1              | 0       | HPOUTR Short Circuit Status<br>0 = Normal<br>1 = Short Circuit detected                                                               |
|                                          | 0   | HP1L_SC_STS1              | 0       | HPOUTL Short Circuit Status<br>0 = Normal<br>1 = Short Circuit detected                                                               |
| R6284 (0x188C)<br>IRQ1_Raw_<br>Status_13 | 6   | SPKOUTL_ENABLE_DONE_STS1  | 0       | SPKOUT Enable Status<br>0 = Busy (sequence in progress)<br>1 = Idle (sequence completed)                                              |
|                                          | 1   | HP1R_ENABLE_DONE_STS1     | 0       | HPOUTR/EPOUTN Enable Status<br>0 = Busy (sequence in progress)<br>1 = Idle (sequence completed)                                       |
|                                          | 0   | HP1L_ENABLE_DONE_STS1     | 0       | HPOUTL/EPOUTP Enable Status<br>0 = Busy (sequence in progress)<br>1 = Idle (sequence completed)                                       |
| R6285 (0x188D)<br>IRQ1_Raw_<br>Status_14 | 6   | SPKOUTL_DISABLE_DONE_STS1 | 0       | SPKOUT Disable Status<br>0 = Busy (sequence in progress)<br>1 = Idle (sequence completed)                                             |
|                                          | 1   | HP1R_DISABLE_DONE_STS1    | 0       | HPOUTR/EPOUTN Disable Status<br>0 = Busy (sequence in progress)<br>1 = Idle (sequence completed)                                      |
|                                          | 0   | HP1L_DISABLE_DONE_STS1    | 0       | HPOUTL/EPOUTP Disable Status<br>0 = Busy (sequence in progress)<br>1 = Idle (sequence completed)                                      |

**Table 4-89. Interrupt 1 Control Registers (Cont.)**

| Register Address                         | Bit | Label                  | Default | Description                                                                                                                                                          |
|------------------------------------------|-----|------------------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R6286 (0x188E)<br>IRQ1_Raw_<br>Status_15 | 2   | SPK_OVERHEAT_WARN_STS1 | 0       | Speaker Overheat Warning Status<br>0 = Normal<br>1 = Warning temperature exceeded                                                                                    |
|                                          | 1   | SPK_OVERHEAT_STS1      | 0       | Speaker Overheat Status<br>0 = Normal<br>1 = Shutdown temperature exceeded                                                                                           |
|                                          | 0   | SPK_SHUTDOWN_STS1      | 0       | Speaker Shutdown Status<br>0 = Normal<br>1 = Speaker Shutdown completed (due to Overheat Temperature or Short Circuit condition)                                     |
| R6288 (0x1890)<br>IRQ1_Raw_<br>Status_17 | 15  | GP16_STS1              | 0       | GPIO <sub>n</sub> Input status. Reads back the logic level of GPIO <sub>n</sub> .<br>Only valid for pins configured as GPIO input (does not include DSPGPIO inputs). |
|                                          | 14  | GP15_STS1              | 0       |                                                                                                                                                                      |
|                                          | 13  | GP14_STS1              | 0       |                                                                                                                                                                      |
|                                          | 12  | GP13_STS1              | 0       |                                                                                                                                                                      |
|                                          | 11  | GP12_STS1              | 0       |                                                                                                                                                                      |
|                                          | 10  | GP11_STS1              | 0       |                                                                                                                                                                      |
|                                          | 9   | GP10_STS1              | 0       |                                                                                                                                                                      |
|                                          | 8   | GP9_STS1               | 0       |                                                                                                                                                                      |
|                                          | 7   | GP8_STS1               | 0       |                                                                                                                                                                      |
|                                          | 6   | GP7_STS1               | 0       |                                                                                                                                                                      |
|                                          | 5   | GP6_STS1               | 0       |                                                                                                                                                                      |
|                                          | 4   | GP5_STS1               | 0       |                                                                                                                                                                      |
|                                          | 3   | GP4_STS1               | 0       |                                                                                                                                                                      |
|                                          | 2   | GP3_STS1               | 0       |                                                                                                                                                                      |
|                                          | 1   | GP2_STS1               | 0       |                                                                                                                                                                      |
|                                          | 0   | GP1_STS1               | 0       |                                                                                                                                                                      |
| R6293 (0x1895)<br>IRQ1_Raw_<br>Status_22 | 3   | EVENT4_NOT_EMPTY_STS1  | 0       | Event Log <i>n</i> FIFO Not Empty status<br>0 = FIFO Empty<br>1 = FIFO Not Empty                                                                                     |
|                                          | 2   | EVENT3_NOT_EMPTY_STS1  | 0       |                                                                                                                                                                      |
|                                          | 1   | EVENT2_NOT_EMPTY_STS1  | 0       |                                                                                                                                                                      |
|                                          | 0   | EVENT1_NOT_EMPTY_STS1  | 0       |                                                                                                                                                                      |
| R6294 (0x1896)<br>IRQ1_Raw_<br>Status_23 | 3   | EVENT4_FULL_STS1       | 0       | Event Log <i>n</i> FIFO Full status<br>0 = FIFO Not Full<br>1 = FIFO Full                                                                                            |
|                                          | 2   | EVENT3_FULL_STS1       | 0       |                                                                                                                                                                      |
|                                          | 1   | EVENT2_FULL_STS1       | 0       |                                                                                                                                                                      |
|                                          | 0   | EVENT1_FULL_STS1       | 0       |                                                                                                                                                                      |
| R6295 (0x1897)<br>IRQ1_Raw_<br>Status_24 | 3   | EVENT4_WMARK_STS1      | 0       | Event Log <i>n</i> FIFO Watermark status<br>0 = FIFO Watermark not reached<br>1 = FIFO Watermark reached                                                             |
|                                          | 2   | EVENT3_WMARK_STS1      | 0       |                                                                                                                                                                      |
|                                          | 1   | EVENT2_WMARK_STS1      | 0       |                                                                                                                                                                      |
|                                          | 0   | EVENT1_WMARK_STS1      | 0       |                                                                                                                                                                      |
| R6296 (0x1898)<br>IRQ1_Raw_<br>Status_25 | 2   | DSP3_DMA_STS1          | 00      | DSP <sub>n</sub> DMA status<br>0 = Normal<br>1 = All enabled WDMA buffers filled, and all enabled RDMA buffers emptied                                               |
|                                          | 1   | DSP2_DMA_STS1          | 00      |                                                                                                                                                                      |
|                                          | 0   | DSP1_DMA_STS1          | 00      |                                                                                                                                                                      |
| R6301 (0x189D)<br>IRQ1_Raw_<br>Status_30 | 2   | DSP3_BUSY_STS1         | 0       | DSP <sub>n</sub> Busy status<br>0 = DSP Idle<br>1 = DSP Busy                                                                                                         |
|                                          | 1   | DSP2_BUSY_STS1         | 0       |                                                                                                                                                                      |
|                                          | 0   | DSP1_BUSY_STS1         | 0       |                                                                                                                                                                      |

1. The BOOT\_DONE\_EINT1 interrupt is 0 (unmasked) by default; all other interrupts are 1 (masked) by default.

The IRQ2 interrupt, mask, and status control registers are described in [Table 4-90](#).

**Table 4-90. Interrupt 2 Control Registers**

| Register Address                | Bit | Label                    | Default | Description                                                                                             |
|---------------------------------|-----|--------------------------|---------|---------------------------------------------------------------------------------------------------------|
| R6400 (0x1900)<br>IRQ2_Status_1 | 15  | DSP_SHARED_WR_COLL_EINT2 | 0       | DSP Shared Memory Collision Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.     |
|                                 | 12  | CTRLIF_ERR_EINT2         | 0       | Control Interface Error Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.         |
|                                 | 9   | SYSCLK_FAIL_EINT2        | 0       | SYSCLK Fail Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                     |
|                                 | 7   | BOOT_DONE_EINT2          | 0       | Boot Done Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                       |
| R6401 (0x1901)<br>IRQ2_Status_2 | 8   | FLL1_LOCK_EINT2          | 0       | FLL1 Lock Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
| R6405 (0x1905)<br>IRQ2_Status_6 | 8   | MICDET_EINT2             | 0       | Microphone/Accessory Detect Interrupt (Detection event triggered)<br>Note: Cleared when a 1 is written. |
|                                 | 0   | HPDET_EINT2              | 0       | Headphone Detect Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                |
| R6406 (0x1906)<br>IRQ2_Status_7 | 5   | MICD_CLAMP_FALL_EINT2    | 0       | MICDET Clamp Interrupt (Falling edge triggered)<br>Note: Cleared when a 1 is written.                   |
|                                 | 4   | MICD_CLAMP_RISE_EINT2    | 0       | MICDET Clamp Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                    |
|                                 | 3   | JD2_FALL_EINT2           | 0       | JD2 Interrupt (Falling edge triggered)<br>Note: Cleared when a 1 is written.                            |
|                                 | 2   | JD2_RISE_EINT2           | 0       | JD2 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                             |
|                                 | 1   | JD1_FALL_EINT2           | 0       | JD1 Interrupt (Falling edge triggered)<br>Note: Cleared when a 1 is written.                            |
|                                 | 0   | JD1_RISE_EINT2           | 0       | JD1 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                             |
| R6408 (0x1908)<br>IRQ2_Status_9 | 1   | DRC2_SIG_DET_EINT2       | 0       | DRC2 Signal-Detect Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.  |
|                                 | 0   | DRC1_SIG_DET_EINT2       | 0       | DRC1 Signal-Detect Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.  |

**Table 4-90. Interrupt 2 Control Registers (Cont.)**

| Register Address                 | Bit | Label                      | Default | Description                                                                                              |
|----------------------------------|-----|----------------------------|---------|----------------------------------------------------------------------------------------------------------|
| R6410 (0x190A)<br>IRQ2_Status_11 | 15  | DSP_IRQ16_EINT2            | 0       | DSP IRQ16 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                        |
|                                  | 14  | DSP_IRQ15_EINT2            | 0       | DSP IRQ15 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                        |
|                                  | 13  | DSP_IRQ14_EINT2            | 0       | DSP IRQ14 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                        |
|                                  | 12  | DSP_IRQ13_EINT2            | 0       | DSP IRQ13 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                        |
|                                  | 11  | DSP_IRQ12_EINT2            | 0       | DSP IRQ12 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                        |
|                                  | 10  | DSP_IRQ11_EINT2            | 0       | DSP IRQ11 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                        |
|                                  | 9   | DSP_IRQ10_EINT2            | 0       | DSP IRQ10 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                        |
|                                  | 8   | DSP_IRQ9_EINT2             | 0       | DSP IRQ9 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 7   | DSP_IRQ8_EINT2             | 0       | DSP IRQ8 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 6   | DSP_IRQ7_EINT2             | 0       | DSP IRQ7 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 5   | DSP_IRQ6_EINT2             | 0       | DSP IRQ6 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 4   | DSP_IRQ5_EINT2             | 0       | DSP IRQ5 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 3   | DSP_IRQ4_EINT2             | 0       | DSP IRQ4 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 2   | DSP_IRQ3_EINT2             | 0       | DSP IRQ3 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 1   | DSP_IRQ2_EINT2             | 0       | DSP IRQ2 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
|                                  | 0   | DSP_IRQ1_EINT2             | 0       | DSP IRQ1 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                         |
| R6411 (0x190B)<br>IRQ2_Status_12 | 6   | SPKOUTL_SC_EINT2           | 0       | SPKOUT Short Circuit Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written. |
|                                  | 3   | HP2R_SC_EINT2              | 0       | EPOUTN Short Circuit Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.             |
|                                  | 2   | HP2L_SC_EINT2              | 0       | EPOUTP Short Circuit Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.             |
|                                  | 1   | HP1R_SC_EINT2              | 0       | HPOUTR Short Circuit Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.             |
|                                  | 0   | HP1L_SC_EINT2              | 0       | HPOUTL Short Circuit Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.             |
| R6412 (0x190C)<br>IRQ2_Status_13 | 6   | SPKOUTL_ENABLE_DONE_EINT2  | 0       | SPKOUT Enable Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                    |
|                                  | 1   | HP1R_ENABLE_DONE_EINT2     | 0       | HPOUTR/EPOUTN Enable Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.             |
|                                  | 0   | HP1L_ENABLE_DONE_EINT2     | 0       | HPOUTL/EPOUTP Enable Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.             |
| R6413 (0x190D)<br>IRQ2_Status_14 | 6   | SPKOUTL_DISABLE_DONE_EINT2 | 0       | SPKOUT Disable Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                   |
|                                  | 1   | HP1R_DISABLE_DONE_EINT2    | 0       | HPOUTR/EPOUTN Disable Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 0   | HP1L_DISABLE_DONE_EINT2    | 0       | HPOUTL/EPOUTP Disable Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.            |

**Table 4-90. Interrupt 2 Control Registers (Cont.)**

| Register Address                 | Bit | Label                   | Default | Description                                                                                          |
|----------------------------------|-----|-------------------------|---------|------------------------------------------------------------------------------------------------------|
| R6414 (0x190E)<br>IRQ2_Status_15 | 2   | SPK_OVERHEAT_WARN_EINT2 | 0       | Speaker Overheat Warning Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.     |
|                                  | 1   | SPK_OVERHEAT_EINT2      | 0       | Speaker Overheat Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.             |
|                                  | 0   | SPK_SHUTDOWN_EINT2      | 0       | Speaker Shutdown Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written. |
| R6416 (0x1910)<br>IRQ2_Status_17 | 15  | GP16_EINT2              | 0       | GPIO16 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
|                                  | 14  | GP15_EINT2              | 0       | GPIO15 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
|                                  | 13  | GP14_EINT2              | 0       | GPIO14 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
|                                  | 12  | GP13_EINT2              | 0       | GPIO13 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
|                                  | 11  | GP12_EINT2              | 0       | GPIO12 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
|                                  | 10  | GP11_EINT2              | 0       | GPIO11 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
|                                  | 9   | GP10_EINT2              | 0       | GPIO10 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.           |
|                                  | 8   | GP9_EINT2               | 0       | GPIO9 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 7   | GP8_EINT2               | 0       | GPIO8 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 6   | GP7_EINT2               | 0       | GPIO7 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 5   | GP6_EINT2               | 0       | GPIO6 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 4   | GP5_EINT2               | 0       | GPIO5 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 3   | GP4_EINT2               | 0       | GPIO4 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 2   | GP3_EINT2               | 0       | GPIO3 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 1   | GP2_EINT2               | 0       | GPIO2 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
|                                  | 0   | GP1_EINT2               | 0       | GPIO1 Interrupt (Rising and falling edge triggered)<br>Note: Cleared when a 1 is written.            |
| R6420 (0x1914)<br>IRQ2_Status_21 | 3   | TIMER4_EINT2            | 0       | Timer 4 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                      |
|                                  | 2   | TIMER3_EINT2            | 0       | Timer 3 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                      |
|                                  | 1   | TIMER2_EINT2            | 0       | Timer 2 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                      |
|                                  | 0   | TIMER1_EINT2            | 0       | Timer 1 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                      |
| R6421 (0x1915)<br>IRQ2_Status_22 | 3   | EVENT4_NOT_EMPTY_EINT2  | 0       | Event Log 4 FIFO Not Empty Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.   |
|                                  | 2   | EVENT3_NOT_EMPTY_EINT2  | 0       | Event Log 3 FIFO Not Empty Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.   |
|                                  | 1   | EVENT2_NOT_EMPTY_EINT2  | 0       | Event Log 2 FIFO Not Empty Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.   |
|                                  | 0   | EVENT1_NOT_EMPTY_EINT2  | 0       | Event Log 1 FIFO Not Empty Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.   |

**Table 4-90. Interrupt 2 Control Registers (Cont.)**

| Register Address                        | Bit | Label              | Default | Description                                                                                                                                                                                             |
|-----------------------------------------|-----|--------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R6422 (0x1916)<br>IRQ2_Status_23        | 3   | EVENT4_FULL_EINT2  | 0       | Event Log 4 FIFO Full Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                           |
|                                         | 2   | EVENT3_FULL_EINT2  | 0       | Event Log 3 FIFO Full Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                           |
|                                         | 1   | EVENT2_FULL_EINT2  | 0       | Event Log 2 FIFO Full Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                           |
|                                         | 0   | EVENT1_FULL_EINT2  | 0       | Event Log 1 FIFO Full Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                           |
| R6423 (0x1917)<br>IRQ2_Status_24        | 3   | EVENT4_WMARK_EINT2 | 0       | Event Log 4 FIFO Watermark Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                      |
|                                         | 2   | EVENT3_WMARK_EINT2 | 0       | Event Log 3 FIFO Watermark Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                      |
|                                         | 1   | EVENT2_WMARK_EINT2 | 0       | Event Log 2 FIFO Watermark Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                      |
|                                         | 0   | EVENT1_WMARK_EINT2 | 0       | Event Log 1 FIFO Watermark Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                      |
| R6424 (0x1918)<br>IRQ2_Status_25        | 2   | DSP3_DMA_EINT2     | 00      | DSP3 DMA Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                        |
|                                         | 1   | DSP2_DMA_EINT2     | 00      | DSP2 DMA Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                        |
|                                         | 0   | DSP1_DMA_EINT2     | 00      | DSP1 DMA Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                        |
| R6426 (0x191A)<br>IRQ2_Status_27        | 2   | DSP3_START1_EINT2  | 0       | DSP3 Start 1 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                    |
|                                         | 1   | DSP2_START1_EINT2  | 0       | DSP2 Start 1 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                    |
|                                         | 0   | DSP1_START1_EINT2  | 0       | DSP1 Start 1 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                    |
| R6427 (0x191B)<br>IRQ2_Status_28        | 2   | DSP3_START2_EINT2  | 0       | DSP3 Start 2 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                    |
|                                         | 1   | DSP2_START2_EINT2  | 0       | DSP2 Start 2 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                    |
|                                         | 0   | DSP1_START2_EINT2  | 0       | DSP1 Start 2 Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                    |
| R6429 (0x191D)<br>IRQ2_Status_30        | 2   | DSP3_BUSY_EINT2    | 0       | DSP3 Busy Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                       |
|                                         | 1   | DSP2_BUSY_EINT2    | 0       | DSP2 Busy Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                       |
|                                         | 0   | DSP1_BUSY_EINT2    | 0       | DSP1 Busy Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                       |
| R6430 (0x191E)<br>IRQ2_Status_31        | 0   | MIF1_DONE_EINT2    | 0       | MIF1 Done Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                       |
| R6431 (0x191F)<br>IRQ2_Status_32        | 0   | MIF1_BLOCK_EINT2   | 0       | MIF1 Block Interrupt (Rising edge triggered)<br>Note: Cleared when a 1 is written.                                                                                                                      |
| R6464 (0x1940)<br>to<br>R6495 (0x195F)  |     | IM_*               | 1       | For each x_EINT2 interrupt bit in R6400 to R6431, a corresponding mask bit (IM_*) is provided in R6464 to R6495. The mask bits are coded as follows:<br>0 = Do not mask interrupt<br>1 = Mask interrupt |
| R6528 (0x1980)<br>IRQ2_Raw_<br>Status_1 | 12  | CTRLIF_ERR_STS2    | 0       | Control Interface Error Status<br>0 = Normal<br>1 = Control Interface Error                                                                                                                             |
|                                         | 7   | BOOT_DONE_STS2     | 0       | Boot Status<br>0 = Busy (boot sequence in progress)<br>1 = Idle (boot sequence completed)<br>Control register writes should not be attempted until Boot Sequence has completed.                         |

**Table 4-90. Interrupt 2 Control Registers (Cont.)**

| Register Address                         | Bit | Label                     | Default | Description                                                                                                                           |
|------------------------------------------|-----|---------------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------|
| R6529 (0x1981)<br>IRQ2_Raw_<br>Status_2  | 8   | FLL1_LOCK_STS2            | 0       | FLL1 Lock Status<br>0 = Not locked<br>1 = Locked                                                                                      |
| R6534 (0x1986)<br>IRQ2_Raw_<br>Status_7  | 4   | MICD_CLAMP_STS2           | 0       | MICDET Clamp status<br>0 = Clamp not active<br>1 = Clamp active                                                                       |
|                                          | 2   | JD2_STS2                  | 0       | JACKDET2 input status<br>0 = Jack not detected<br>1 = Jack is detected<br>(Assumes the JACKDET2 pin is pulled low on jack insertion.) |
|                                          | 0   | JD1_STS2                  | 0       | JACKDET1 input status<br>0 = Jack not detected<br>1 = Jack is detected<br>(Assumes the JACKDET1 pin is pulled low on jack insertion.) |
| R6536 (0x1988)<br>IRQ2_Raw_<br>Status_9  | 1   | DRC2_SIG_DET_STS2         | 0       | DRC2 Signal-Detect Status<br>0 = Normal<br>1 = Signal detected                                                                        |
|                                          | 0   | DRC1_SIG_DET_STS2         | 0       | DRC1 Signal-Detect Status<br>0 = Normal<br>1 = Signal detected                                                                        |
| R6539 (0x198B)<br>IRQ2_Raw_<br>Status_12 | 6   | SPKOUTL_SC_STS2           | 0       | SPKOUT Short Circuit Status<br>0 = Normal<br>1 = Short Circuit detected                                                               |
|                                          | 3   | HP2R_SC_STS2              | 0       | EPOUTN Short Circuit Status<br>0 = Normal<br>1 = Short Circuit detected                                                               |
|                                          | 2   | HP2L_SC_STS2              | 0       | EPOUTP Short Circuit Status<br>0 = Normal<br>1 = Short Circuit detected                                                               |
|                                          | 1   | HP1R_SC_STS2              | 0       | HPOUTR Short Circuit Status<br>0 = Normal<br>1 = Short Circuit detected                                                               |
|                                          | 0   | HP1L_SC_STS2              | 0       | HPOUTL Short Circuit Status<br>0 = Normal<br>1 = Short Circuit detected                                                               |
| R6540 (0x198C)<br>IRQ2_Raw_<br>Status_13 | 6   | SPKOUTL_ENABLE_DONE_STS2  | 0       | SPKOUT Enable Status<br>0 = Busy (sequence in progress)<br>1 = Idle (sequence completed)                                              |
|                                          | 1   | HP1R_ENABLE_DONE_STS2     | 0       | HPOUTR/EPOUTN Enable Status<br>0 = Busy (sequence in progress)<br>1 = Idle (sequence completed)                                       |
|                                          | 0   | HP1L_ENABLE_DONE_STS2     | 0       | HPOUTL/EPOUTP Enable Status<br>0 = Busy (sequence in progress)<br>1 = Idle (sequence completed)                                       |
| R6541 (0x198D)<br>IRQ2_Raw_<br>Status_14 | 6   | SPKOUTL_DISABLE_DONE_STS2 | 0       | SPKOUT Disable Status<br>0 = Busy (sequence in progress)<br>1 = Idle (sequence completed)                                             |
|                                          | 1   | HP1R_DISABLE_DONE_STS2    | 0       | HPOUTR/EPOUTN Disable Status<br>0 = Busy (sequence in progress)<br>1 = Idle (sequence completed)                                      |
|                                          | 0   | HP1L_DISABLE_DONE_STS2    | 0       | HPOUTL/EPOUTP Disable Status<br>0 = Busy (sequence in progress)<br>1 = Idle (sequence completed)                                      |

**Table 4-90. Interrupt 2 Control Registers (Cont.)**

| Register Address                         | Bit | Label                  | Default | Description                                                                                                                                   |
|------------------------------------------|-----|------------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| R6542 (0x198E)<br>IRQ2_Raw_<br>Status_15 | 2   | SPK_OVERHEAT_WARN_STS2 | 0       | Speaker Overheat Warning Status<br>0 = Normal<br>1 = Warning temperature exceeded                                                             |
|                                          | 1   | SPK_OVERHEAT_STS2      | 0       | Speaker Overheat Status<br>0 = Normal<br>1 = Shutdown temperature exceeded                                                                    |
|                                          | 0   | SPK_SHUTDOWN_STS2      | 0       | Speaker Shutdown Status<br>0 = Normal<br>1 = Speaker Shutdown completed (due to Overheat Temperature or Short Circuit condition)              |
| R6544 (0x1990)<br>IRQ2_Raw_<br>Status_17 | 15  | GP16_STS2              | 0       | GPIOn Input status<br>Reads back the logic level of GPIOn.<br>Only valid for pins configured as GPIO input (does not include DSPGPIO inputs). |
|                                          | 14  | GP15_STS2              | 0       |                                                                                                                                               |
|                                          | 13  | GP14_STS2              | 0       |                                                                                                                                               |
|                                          | 12  | GP13_STS2              | 0       |                                                                                                                                               |
|                                          | 11  | GP12_STS2              | 0       |                                                                                                                                               |
|                                          | 10  | GP11_STS2              | 0       |                                                                                                                                               |
|                                          | 9   | GP10_STS2              | 0       |                                                                                                                                               |
|                                          | 8   | GP9_STS2               | 0       |                                                                                                                                               |
|                                          | 7   | GP8_STS2               | 0       |                                                                                                                                               |
|                                          | 6   | GP7_STS2               | 0       |                                                                                                                                               |
|                                          | 5   | GP6_STS2               | 0       |                                                                                                                                               |
|                                          | 4   | GP5_STS2               | 0       |                                                                                                                                               |
|                                          | 3   | GP4_STS2               | 0       |                                                                                                                                               |
|                                          | 2   | GP3_STS2               | 0       |                                                                                                                                               |
|                                          | 1   | GP2_STS2               | 0       |                                                                                                                                               |
|                                          | 0   | GP1_STS2               | 0       |                                                                                                                                               |
| R6549 (0x1995)<br>IRQ2_Raw_<br>Status_22 | 3   | EVENT4_NOT_EMPTY_STS2  | 0       | Event Log <i>n</i> FIFO Not Empty status<br>0 = FIFO Empty<br>1 = FIFO Not Empty                                                              |
|                                          | 2   | EVENT3_NOT_EMPTY_STS2  | 0       |                                                                                                                                               |
|                                          | 1   | EVENT2_NOT_EMPTY_STS2  | 0       |                                                                                                                                               |
|                                          | 0   | EVENT1_NOT_EMPTY_STS2  | 0       |                                                                                                                                               |
| R6550 (0x1996)<br>IRQ2_Raw_<br>Status_23 | 3   | EVENT4_FULL_STS2       | 0       | Event Log <i>n</i> FIFO Full status<br>0 = FIFO Not Full<br>1 = FIFO Full                                                                     |
|                                          | 2   | EVENT3_FULL_STS2       | 0       |                                                                                                                                               |
|                                          | 1   | EVENT2_FULL_STS2       | 0       |                                                                                                                                               |
|                                          | 0   | EVENT1_FULL_STS2       | 0       |                                                                                                                                               |
| R6551 (0x1997)<br>IRQ2_Raw_<br>Status_24 | 3   | EVENT4_WMARK_STS2      | 0       | Event Log <i>n</i> FIFO Watermark status<br>0 = FIFO Watermark not reached<br>1 = FIFO Watermark reached                                      |
|                                          | 2   | EVENT3_WMARK_STS2      | 0       |                                                                                                                                               |
|                                          | 1   | EVENT2_WMARK_STS2      | 0       |                                                                                                                                               |
|                                          | 0   | EVENT1_WMARK_STS2      | 0       |                                                                                                                                               |
| R6552 (0x1998)<br>IRQ2_Raw_<br>Status_25 | 2   | DSP3_DMA_STS2          | 00      | DSP <i>n</i> DMA status<br>0 = Normal<br>1 = All enabled WDMA buffers filled, and all enabled RDMA buffers emptied                            |
|                                          | 1   | DSP2_DMA_STS2          | 00      |                                                                                                                                               |
|                                          | 0   | DSP1_DMA_STS2          | 00      |                                                                                                                                               |
| R6557 (0x199D)<br>IRQ2_Raw_<br>Status_30 | 2   | DSP3_BUSY_STS2         | 0       | DSP <i>n</i> Busy status<br>0 = DSP Idle<br>1 = DSP Busy                                                                                      |
|                                          | 1   | DSP2_BUSY_STS2         | 0       |                                                                                                                                               |
|                                          | 0   | DSP1_BUSY_STS2         | 0       |                                                                                                                                               |

The IRQ output and polarity control registers are described in [Table 4-91](#).

**Table 4-91. Interrupt Control Registers**

| Register Address                             | Bit | Label      | Default | Description                                                                                                     |
|----------------------------------------------|-----|------------|---------|-----------------------------------------------------------------------------------------------------------------|
| R6784 (0x1A80)<br>IRQ1_CTRL                  | 11  | IM_IRQ1    | 0       | IRQ1 Output Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.                                |
|                                              | 10  | IRQ_POL    | 1       | IRQ Output Polarity Select<br>0 = Noninverted (Active High)<br>1 = Inverted (Active Low)                        |
|                                              | 9   | IRQ_OP_CFG | 0       | IRQ Output Configuration<br>0 = CMOS<br>1 = Open drain                                                          |
| R6786 (0x1A82)<br>IRQ2_CTRL                  | 11  | IM_IRQ2    | 0       | IRQ2 Output Interrupt mask.<br>0 = Do not mask interrupt.<br>1 = Mask interrupt.                                |
| R6816 (0x1AA0)<br>Interrupt_Raw_<br>Status_1 | 1   | IRQ2_STS   | 0       | IRQ2 Status. IRQ2_STS is the logical OR of all unmasked x_EINT2 interrupts.<br>0 = Not asserted<br>1 = Asserted |
|                                              | 0   | IRQ1_STS   | 0       | IRQ1 Status. IRQ1_STS is the logical OR of all unmasked x_EINT1 interrupts.<br>0 = Not asserted<br>1 = Asserted |

## 4.16 Clocking and Sample Rates

The CS47L35 requires a clock reference for its internal functions and also for the input (ADC) paths, output (DAC) paths, and digital audio interfaces. Under typical clocking configurations, all commonly used audio sample rates can be derived directly from the external reference; for additional flexibility, the CS47L35 incorporates an FLL circuit to perform frequency conversion and filtering.

External clock signals may be connected via MCLK1 and MCLK2. These inputs are referenced to the DBVDD1 and DBVDD2 power domains respectively. In AIF Slave Modes, the BCLK signals may be used as a reference for the system clocks. The SLIMbus interface can provide the clock reference, when used as the input to the FLL. To avoid audible glitches, all clock configurations must be set up before enabling playback.

### 4.16.1 System Clocking Overview

The CS47L35 supports two primary clock domains—SYSCLK and DSPCLK.

The SYSCLK clock domain is the reference clock for all the audio signal paths on the CS47L35. Up to three different sample rates may be independently selected for specific audio interfaces and other input/output signal paths.

The DSPCLK clock domain is the reference clock for the programmable DSP cores on the CS47L35. A wide range of DSPCLK frequencies can be supported, and a programmable clock divider is provided for each DSP core, allowing the DSP clocking (and power consumption) to be optimized according to the applicable processing requirements of each DSP core. See [Section 4.4](#) for further details.

Note that there is no requirement for DSPCLK to be synchronized to SYSCLK. The DSPCLK controls the software execution in the DSP cores; audio outputs from the DSP cores are synchronized to SYSCLK, regardless of the applicable DSPCLK rate.

Excluding the DSP cores, each subsystem within the CS47L35 digital core is clocked at a dynamically controlled rate, limited by the SYSCLK frequency. For maximum signal mixing and processing capacity, it is recommended that the highest possible SYSCLK frequency is configured.

The DSP cores are clocked at the DSPCLK rate (or supported divisions of the DSPCLK frequency). The DSPCLK configuration must ensure that sufficient clock cycles are available for the processing requirements of each DSP core. The requirements vary, according to the particular software that is in use.

### 4.16.2 Sample-Rate Control

The CS47L35 audio signal paths are synchronized to the SYSCLK system clock.

Different sample rates may be selected for each of the audio interfaces (AIF1, AIF2, AIF3, SLIMbus), and for the input (ADC) and output (DAC) paths, but each enabled interface must still be synchronized to SYSCLK.

The CS47L35 can support a maximum of three different sample rates at any time. The supported sample rates range from 8kHz to 192kHz.

The applicable sample rates are selected using SAMPLE\_RATE\_1, SAMPLE\_RATE\_2 and SAMPLE\_RATE\_3. These must each be numerically related to each other and to the SYSCLK frequency (further details of these requirements are provided in [Table 4-92](#) and the accompanying text).

Each of the audio interfaces, input paths, and output paths is associated with one of the sample rates selected by the SAMPLE\_RATE\_n fields.

Note that, when any of the SAMPLE\_RATE\_n fields is written to, the activation of the new setting is automatically synchronized by the CS47L35 to ensure continuity of all active signal paths. The SAMPLE\_RATE\_n\_STS bits provide indication of the sample rate selections that have been implemented.

The following restrictions must be observed regarding the sample-rate control configuration:

- All external clock references (MCLK input or Slave Mode AIF input) must be within 1% of the applicable register field settings.
- The input (ADC/DMIC) sample rate is valid from 8–192 kHz. If 384- or 768-kHz DMIC clock rate is selected on any of the input paths, the supported sample rate is valid only up to 48 or 96 kHz respectively.
- The S/PDIF sample rate is valid from 32–192 kHz.
- The isochronous sample-rate converters (ISRCs) support sample rates 8–192 kHz. For each ISRC, the higher sample rate must be an integer multiple of the lower rate.

### 4.16.3 Automatic Sample-Rate Detection

The CS47L35 supports automatic sample-rate detection on the digital audio interfaces (AIF1–AIF3). Note that this is only possible when the respective interface is operating in Slave Mode (i.e., when LRCLK and BCLK are inputs to the CS47L35).

Automatic sample-rate detection is enabled by setting RATE\_EST\_ENA. The LRCLK input pin selected for sample-rate detection is set using LRCLK\_SRC.

As many as four audio sample rates can be configured for automatic detection; these sample rates are selected using the SAMPLE\_RATE\_DETECT\_n fields. Note that the function only detects sample rates that match one of the SAMPLE\_RATE\_DETECT\_n fields.

If one of the selected audio sample rates is detected on the selected LRCLK input, the control-write sequencer is triggered. A unique sequence of actions may be programmed for each of the detected sample rates. Note that the applicable control sequences must be programmed by the user for each detection outcome; see [Section 4.18](#).

The TRIG\_ON\_STARTUP bit controls whether the sample-rate detection circuit responds to the initial detection of the applicable interface (i.e., when the AIFn interface starts up).

- If TRIG\_ON\_STARTUP = 0, the detection circuit only responds (i.e., trigger the control-write sequencer) to a change in the detected sample rate—the initial sample-rate detection is ignored. (Note that the initial sample-rate detection is the first detection of a sample rate that matches one of the SAMPLE\_RATE\_DETECT\_n fields.)
- If TRIG\_ON\_STARTUP = 1, the detection circuit triggers the control-write sequencer whenever a selected sample rate is detected, including when the AIF interface starts up, or when the sample-rate detection is first enabled.

As described above, setting TRIG\_ON\_STARTUP = 0 is designed to inhibit any response to the initial detection of a sample rate that matches one of the SAMPLE\_RATE\_DETECT\_n fields. Note that, if the LRCLK\_SRC setting is changed, or if the detection function is disabled and reenabled, a subsequent detection of a matching sample rate may trigger the control-write sequencer, regardless of the TRIG\_ON\_STARTUP setting.

There are some restrictions to be observed regarding the automatic sample-rate detection configuration, as noted in the following:

- The same sample rate must not be selected on more than one of the SAMPLE\_RATE\_DETECT<sub>n</sub> fields.
- Sample rates 192 kHz and 176.4 kHz must not be selected concurrently.
- Sample rates 96 kHz and 88.2 kHz must not be selected concurrently.

The control registers associated with the automatic sample-rate detection function are described in [Table 4-93](#).

#### 4.16.4 SYSCLK Control

The SYSCLK clock may be provided directly from external inputs (MCLK, or Slave Mode BCLK inputs). Alternatively, SYSCLK can be derived using the integrated FLL, with MCLK, BCLK, LRCLK or SLIMCLK as a reference. The SYSCLK must be configured and enabled before any audio path is enabled.

The SYSCLK frequency must be valid for all of the SAMPLE\_RATE<sub>n</sub> fields. It follows that all of the SAMPLE\_RATE<sub>n</sub> fields must select numerically-related values, that is, all from the same group of sample rates as represented in [Table 4-92](#).

**Table 4-92. SYSCLK Frequency Selection**

| SYSCLK Frequency (MHz) | SYSCLK_FREQ | SYSCLK_FRAC | Sample Rate (kHz) | SAMPLE_RATE <sub>n</sub> |
|------------------------|-------------|-------------|-------------------|--------------------------|
| 6.144                  | 000         | 0           | 12                | 0x01                     |
| 12.288                 | 001         |             | 24                | 0x02                     |
| 24.576                 | 010         |             | 48                | 0x03                     |
| 49.152                 | 011         |             | 96                | 0x04                     |
| 98.304                 | 100         |             | 192               | 0x05                     |
|                        |             |             | 8                 | 0x11                     |
|                        |             |             | 16                | 0x12                     |
|                        |             |             | 32                | 0x13                     |
| 5.6448                 | 000         | 1           | 11.025            | 0x09                     |
| 11.2896                | 001         |             | 22.05             | 0x0A                     |
| 22.5792                | 010         |             | 44.1              | 0x0B                     |
| 45.1584                | 011         |             | 88.2              | 0x0C                     |
| 90.3168                | 100         |             | 176.4             | 0x0D                     |

**Note:** The SAMPLE\_RATE<sub>n</sub> fields must each be set to a value from the same group of sample rates, and from the same group as the SYSCLK frequency.

SYSCLK\_SRC is used to select the SYSCLK source, as described in [Table 4-93](#). The source may be MCLK<sub>n</sub>, AIF<sub>n</sub>BCLK, or FLL. If the FLL circuit is selected as the source, the FLL must be enabled and configured, as described in [Section 4.16.9](#).

**Note:** If FLL1 is selected as SYSCLK source, the SYSCLK frequency is  $F_{VCO} / 3$ . This enables SYSCLK frequencies of 98.304 MHz or 90.3168 MHz. See [Section 4.16.9](#).

SYSCLK\_FREQ and SYSCLK\_FRAC must be set according to the frequency of the selected SYSCLK source.

The SYSCLK-referenced circuits within the digital core are clocked at a dynamically controlled rate that is limited by the SYSCLK frequency. For maximum signal mixing and processing capacity, the highest possible SYSCLK frequency should be used.

The SAMPLE\_RATE<sub>n</sub> fields are set according to the sample rates that are required by one or more of the CS47L35 audio interfaces. The CS47L35 supports sample rates ranging from 8–192 kHz.

The SYSCLK signal is enabled by setting SYSCLK\_ENA. The applicable clock source (MCLK<sub>n</sub>, AIF<sub>n</sub>BCLK, or FLL) must be enabled before setting SYSCLK\_ENA. This bit must be cleared when reconfiguring the SYSCLK source or frequency. The SYSCLK\_ENA bit should also be cleared before stopping or removing the applicable clock source.

The SYSCLK signal is the reference clock for many different subsystems on the CS47L35. All of the SYSCLK-dependent subsystems should be disabled if SYSCLK is not enabled. The SYSCLK\_ENA bit must be set before enabling any SYSCLK-dependent function, and all the dependent functions should be disabled before clearing the SYSCLK\_ENA bit.

The SYSCLK-dependent subsystems are referenced below; if one or more of the following conditions is met, then the SYSCLK signal is required, and should not be interrupted or reconfigured.

- Input signal path enabled (INnx\_ENA = 1)
- OPCLK enabled for GPIO output (OPCLK\_ENA = 1)
- Output signal path enabled (OUT5x\_ENA = 1, SPKOUTL\_ENA = 1, HP1x\_ENA = 1)
- Digital audio interface path enabled (AIFnTXm\_ENA = 1, AIFnRXm\_ENA = 1)
- Digital audio interface clocks enabled (AIFn\_BCLK\_FRC = 1, AIFn\_LRCLK\_FRC = 1)
- SPDIF output enabled (SPD1\_ENA = 1)
- Digital Core Mixer enabled (x\_SRCn > 0x00)
- Haptic generator enabled (HAP\_CTRL > 00)
- Tone generator enabled (TONEn\_ENA = 1)
- PWM generator enabled (PWMn\_ENA = 1)
- EQ, DRC, or LHPF processor enabled (EQn\_ENA = 1, DRCnx\_ENA = 1, LHPFn\_ENA = 1)
- ISRC channel enabled (ISRCn\_INTm\_ENA = 1, ISRCn\_DECM\_ENA = 1)
- SLIMbus data channel enabled (SLIMTXn\_ENA = 1, SLIMRXn\_ENA = 1)
- Noise generator enabled (NOISE\_GEN\_ENA = 1)
- Timer enabled, with SYSCLK as clock source (TIMERn\_RUNNING\_STS = 1 and TIMERn\_REFCLK\_SRC = 0x8)
- DSP Core firmware requires access to registers below 0x40000

If reconfiguration of the SYSCLK source or frequency is required, and it is not possible to disable all of the SYSCLK-dependent subsystems, then the control-write sequencer must be used for the reconfiguration of SYSCLK. The control sequence should apply the following actions:

- Clear SYSCLK\_ENA to 0
- Write updates to SYSCLK\_SRC, SYSCLK\_FREQ, and SYSCLK\_FRAC
- Set SYSCLK\_ENA to 1

The CS47L35 performs automatic checks to confirm that the SYSCLK frequency is high enough to support the commanded signal paths and processing functions. If the frequency is too low, an attempt to enable a signal path or processing function fails. Note that active signal paths are not affected under such circumstances.

### 4.16.5 DSPCLK Control

The DSPCLK clock may be provided directly from external inputs (MCLK, or Slave Mode BCLK inputs). Alternatively, DSPCLK can be derived using the integrated FLL, with MCLK, BCLK, LRCLK, or SLIMCLK as a reference. The DSPCLK must be configured and enabled, if running firmware applications on any of the DSP cores.

The required DSPCLK frequency depends on the requirements of firmware loaded on the DSP cores. The DSP cores are clocked at the DSPCLK rate or at supported divisions of the DSPCLK frequency. The DSPCLK configuration must ensure that sufficient clock cycles are available for the processing requirements of each DSP core. The requirements vary, according to the particular software that is in use.

A configurable clock divider is provided for each DSP core, allowing the DSP clocking (and power consumption) to be optimized according to the applicable processing requirements of each DSP core; see [Section 4.4](#) for details.

DSP\_CLK\_FREQ\_RANGE must be configured for the applicable DSPCLK frequency. Note that, if the DSPCLK frequency is equal to one of the threshold frequencies quoted, the higher range setting should be selected. For example, if the DSPCLK frequency is 37.5 MHz, DSP\_CLK\_FREQ\_RANGE should be set to 011.

DSP\_CLK\_SRC is used to select the DSPCLK source, as described in [Table 4-93](#). The source may be MCLKn, AIFnBCLK, or FLL. If the FLL circuit is selected as the source, the FLL must be enabled and configured, as described in [Section 4.16.9](#).

**Note:** If the FLL is selected as DSPCLK source, two different clock frequencies are available. For most use cases, the FLL output frequency is divided by two, when used as the DSPCLK source; this enables DSPCLK frequencies in the range 135–150 MHz. A divide-by-six option is also available, supporting low-power DSP operation with DSPCLK frequencies in the range 45–50 MHz.

The DSPCLK signal is enabled by setting DSP\_CLK\_ENA. The applicable clock source (MCLK<sub>n</sub>, AIF<sub>n</sub>BCLK, or FLL) must be enabled before setting DSP\_CLK\_ENA. This bit must be cleared when reconfiguring the clock sources.

In a typical application, DSPCLK and SYSCLK are derived from a single FLL source. In this case, one of the nominal DSPCLK frequencies is likely to be applicable (see [Table 4-93](#)). Note that there is no requirement for DSPCLK to be synchronized to SYSCLK. The DSPCLK controls the software execution in the DSP cores; audio outputs from the DSP cores are synchronized to SYSCLK, regardless of the applicable DSPCLK rate.

The DSPCLK signal is the reference clock for the DSP cores and DSP peripherals on the CS47L35. All of the DSPCLK-dependent functions should be disabled if DSPCLK is not enabled. The DSPCLK\_ENA bit must be set before enabling any DSPCLK-dependent function, and all the dependent functions should be disabled before clearing the DSPCLK\_ENA bit.

The DSPCLK-dependent subsystems are referenced below; if one or more of the following conditions is met, then the DSPCLK signal is required, and should not be interrupted or reconfigured.

- DSP core enabled (DSP<sub>n</sub>\_CORE\_ENA = 1)
- DSP DMA function enabled (DSP<sub>n</sub>\_[WDMA/RDMA]\_CHANNEL\_ENABLE > 0x00)
- DSP core in JTAG mode
- Master Interface active (MIF1\_BUSY\_STS = 1)
- Timer enabled (TIMER<sub>n</sub>\_RUNNING\_STS = 1)

If reconfiguration of the DSPCLK source or frequency is required, and it is not possible to disable all of the DSPCLK-dependent functions, then the following control requirements must be applied to reconfigure DSPCLK:

- Clear DSP\_CLK\_ENA to 0
- Wait 34  $\mu$ s (only required if a Timer is enabled)
- Update DSP\_CLK\_SRC and DSP\_CLK\_FREQ\_RANGE, and set DSP\_CLK\_ENA = 1. (These must be applied in a single register write operation)
- Note that, if a DSP core is enabled, DMA function is enabled, DSP core is in JTAG mode, or a Master Interface is active, then no other register read/write actions (either by Control Interface or by DSP firmware access) can be permitted during this sequence.
- If a Timer is enabled, but no DSP core, DMA, JTAG, or MIF is active, then DSPCLK can be stopped at any time. The minimum wait time of 34  $\mu$ s is required before changing DSP\_CLK\_SRC or DSP\_CLK\_FREQ\_RANGE, but there are no other constraints on configuring DSPCLK in these circumstances.

If DSPCLK is the Timer clock source, the Timer pauses when DSPCLK stops, and resumes operation when DSPCLK restarts. If DSPCLK is not the clock source, the Timer operation continues when DSPCLK stops, but the Timer no longer synchronizes to DSPCLK.

#### 4.16.6 Miscellaneous Clock Controls

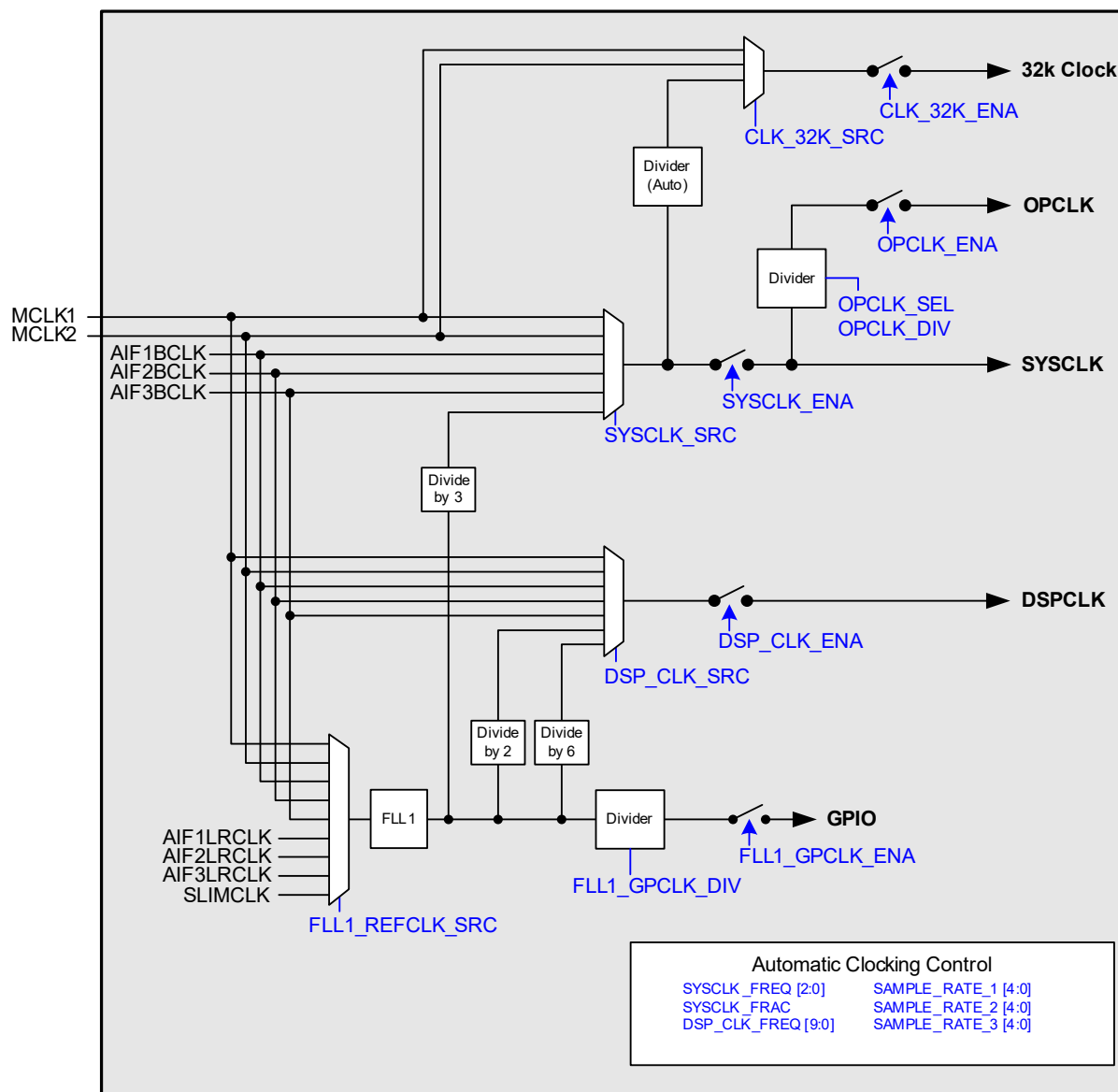
The CS47L35 incorporates a 32-kHz clock circuit, which is required for input signal debounce, microphone/accessory detect, and for the Charge Pump 2 (CP2) circuits. The 32-kHz clock must be configured and enabled whenever any of these features are in use.

The 32-kHz clock can be generated automatically from SYSCLK, or may be input directly as MCLK1 or MCLK2. The 32-kHz clock source is selected using CLK\_32K\_SRC. The 32-kHz clock is enabled by setting CLK\_32K\_ENA.

A clock output (OPCLK) derived from SYSCLK can be output on a GPIO pin. See [Section 4.14](#) for details on configuring a GPIO pin for this function.

The CS47L35 provides integrated pull-down resistors on the MCLK1 and MCLK2 pins. This provides a flexible capability for interfacing with other devices.

The clocking scheme for the CS47L35 is shown in [Fig. 4-63](#).



**Figure 4-63. System Clocking**

The CS47L35 clocking control registers are described in [Table 4-93](#).

**Table 4-93. Clocking Control**

| Register Address             | Bit | Label            | Default | Description                                                                                                              |
|------------------------------|-----|------------------|---------|--------------------------------------------------------------------------------------------------------------------------|
| R256 (0x0100)<br>Clock_32k_1 | 6   | CLK_32K_ENA      | 0       | 32kHz Clock Enable<br>0 = Disabled<br>1 = Enabled                                                                        |
|                              | 1:0 | CLK_32K_SRC[1:0] | 10      | 32kHz Clock Source<br>00 = MCLK1 (direct)<br>01 = MCLK2 (direct)<br>10 = SYSCLK (automatically divided)<br>11 = Reserved |

**Table 4-93. Clocking Control (Cont.)**

| Register Address                      | Bit  | Label                  | Default | Description                                                                                                                                                                                                                                                                                                                         |
|---------------------------------------|------|------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R257 (0x0101)<br>System_Clock_1       | 15   | SYSClk_FRAC            | 0       | SYSClk Frequency<br>0 = SYSClk is a multiple of 6.144MHz<br>1 = SYSClk is a multiple of 5.6448MHz                                                                                                                                                                                                                                   |
|                                       | 10:8 | SYSClk_FREQ[2:0]       | 100     | SYSClk Frequency<br>000 = 6.144 MHz (5.6448 MHz)<br>001 = 12.288 MHz (11.2896 MHz)<br>010 = 24.576 MHz (22.5792 MHz)<br>011 = 49.152 MHz (45.1584 MHz)<br>100 = 98.304 MHz (90.3168 MHz)<br>All other codes are reserved<br>The frequencies in brackets apply for 44.1 kHz–related sample rates only (i.e., SAMPLE_RATE_n = 01XXX). |
|                                       | 6    | SYSClk_ENA             | 0       | SYSClk Control<br>0 = Disabled<br>1 = Enabled<br>SYSClk should only be enabled after the applicable clock source has been configured and enabled. Set this bit to 0 when reconfiguring the clock sources.<br>All digital core (audio mixer) x_SRC fields must be cleared before clearing SYSClk_ENA = 0.                            |
|                                       | 3:0  | SYSClk_SRC[3:0]        | 0100    | SYSClk Source<br>0000 = MCLK1<br>0001 = MCLK2<br>0100 = FLL1<br>1000 = AIF1BCLK<br>1001 = AIF2BCLK<br>1010 = AIF3BCLK<br>All other codes are reserved                                                                                                                                                                               |
| R258 (0x0102)<br>Sample_rate_1        | 4:0  | SAMPLE_RATE_1[4:0]     | 0x11    | Sample Rate 1 Select<br>0x00 = None<br>0x01 = 12 kHz<br>0x02 = 24 kHz<br>0x03 = 48 kHz<br>0x04 = 96 kHz<br>0x05 = 192 kHz<br>0x09 = 11.025 kHz<br>0x0A = 22.05 kHz<br>0x0B = 44.1 kHz<br>0x0C = 88.2 kHz<br>0x0D = 176.4 kHz<br>0x11 = 8 kHz<br>0x12 = 16 kHz<br>0x13 = 32 kHz<br>All other codes are reserved                      |
| R259 (0x0103)<br>Sample_rate_2        | 4:0  | SAMPLE_RATE_2[4:0]     | 0x11    | Sample Rate 2 Select<br>Field coding is same as SAMPLE_RATE_1.                                                                                                                                                                                                                                                                      |
| R260 (0x0104)<br>Sample_rate_3        | 4:0  | SAMPLE_RATE_3[4:0]     | 0x11    | Sample Rate 3 Select<br>Field coding is same as SAMPLE_RATE_1.                                                                                                                                                                                                                                                                      |
| R266 (0x010A)<br>Sample_rate_1_status | 4:0  | SAMPLE_RATE_1_STS[4:0] | 0x00    | Sample Rate 1 Status<br>(Read only)<br>Field coding is same as SAMPLE_RATE_1.                                                                                                                                                                                                                                                       |
| R267 (0x010B)<br>Sample_rate_2_status | 4:0  | SAMPLE_RATE_2_STS[4:0] | 0x00    | Sample Rate 2 Status<br>(Read only)<br>Field coding is same as SAMPLE_RATE_1.                                                                                                                                                                                                                                                       |
| R268 (0x010C)<br>Sample_rate_3_status | 4:0  | SAMPLE_RATE_3_STS[4:0] | 0x00    | Sample Rate 3 Status<br>(Read only)<br>Field coding is same as SAMPLE_RATE_1.                                                                                                                                                                                                                                                       |

**Table 4-93. Clocking Control (Cont.)**

| Register Address                     | Bit  | Label                   | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|--------------------------------------|------|-------------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R288 (0x0120)<br>DSP_Clock_1         | 10:8 | DSP_CLK_FREQ_RANGE[2:0] | 011     | DSPCLK Frequency<br>000=5.5 MHz to 9.375 MHz (9.216 MHz)<br>001=9.375 MHz to 18.75 MHz (18.432 MHz)<br>010=18.75 MHz to 37.5 MHz (36.864 MHz)<br>011=37.5 MHz to 75 MHz (73.728 MHz)<br>100=75 MHz to 150 MHz (147.456 MHz)<br>All other codes are reserved<br>The frequencies in brackets are the nominal (or typical) frequencies for each setting.<br>If the DSPCLK frequency is equal to one of the threshold frequencies quoted (e.g., 37.5 MHz), the higher range setting (e.g., 011) should be selected. |
|                                      | 6    | DSP_CLK_ENA             | 0       | DSPCLK Control<br>0 = Disabled<br>1 = Enabled<br>DSPCLK should only be enabled after the applicable clock source has been configured and enabled.<br>Set this bit to 0 when reconfiguring the clock sources.                                                                                                                                                                                                                                                                                                    |
|                                      | 3:0  | DSP_CLK_SRC[3:0]        | 0101    | DSPCLK Source<br>0000 = MCLK1<br>0001 = MCLK2<br>0100 = FLL1<br>0111 = FLL1 DIV6<br>1000 = AIF1BCLK<br>1001 = AIF2BCLK<br>1010 = AIF3BCLK<br>All other codes are reserved                                                                                                                                                                                                                                                                                                                                       |
| R329 (0x0149)<br>Output_system_clock | 15   | OPCLK_ENA               | 0       | OPCLK Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|                                      | 7:3  | OPCLK_DIV[4:0]          | 0x00    | OPCLK Divider<br>0x02 = Divide by 2<br>0x04 = Divide by 4<br>0x06 = Divide by 6<br>... (even numbers only)<br>0x1E = Divide by 30<br>Note that only even numbered divisions (2, 4, 6, etc.) are valid selections.<br>All other codes are reserved when the OPCLK signal is enabled.                                                                                                                                                                                                                             |
|                                      | 2:0  | OPCLK_SEL[2:0]          | 000     | OPCLK Source Frequency<br>000 = 6.144 MHz (5.6448 MHz)<br>001 = 12.288 MHz (11.2896 MHz)<br>010 = 24.576 MHz (22.5792 MHz)<br>011 = 49.152 MHz (45.1584 MHz)<br>All other codes are reserved<br>The frequencies in brackets apply for 44.1 kHz-related SYSCLK rates only (i.e., SAMPLE_RATE_n = 01XXX).<br>The OPCLK Source Frequency must be less than or equal to the SYSCLK frequency.                                                                                                                       |
| R334 (0x014E)<br>Clock_Gen_Pad_Ctrl  | 8    | MCLK2_PD                | 0       | MCLK2 Pull-Down Control<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|                                      | 7    | MCLK1_PD                | 0       | MCLK1 Pull-Down Control<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

**Table 4-93. Clocking Control (Cont.)**

| Register Address                  | Bit | Label                     | Default | Description                                                                                                                                                                   |
|-----------------------------------|-----|---------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R338 (0x0152)<br>Rate_Estimator_1 | 4   | TRIG_ON_STARTUP           | 0       | Automatic Sample-Rate Detection Start-Up select<br>0 = Do not trigger Write Sequencer on initial detection<br>1 = Always trigger the Write Sequencer on sample-rate detection |
|                                   | 3:1 | LRCLK_SRC[2:0]            | 000     | Automatic Sample-Rate Detection source<br>000 = AIF1LRCLK<br>010 = AIF2LRCLK<br>100 = AIF3LRCLK<br>All other codes are reserved                                               |
|                                   | 0   | RATE_EST_ENA              | 0       | Automatic Sample-Rate Detection control<br>0 = Disabled<br>1 = Enabled                                                                                                        |
| R339 (0x0153)<br>Rate_Estimator_2 | 4:0 | SAMPLE_RATE_DETECT_A[4:0] | 0x00    | Automatic Detection Sample Rate A<br>(Up to four different sample rates can be configured for automatic detection.)<br>Field coding is same as SAMPLE_RATE_n.                 |
| R340 (0x0154)<br>Rate_Estimator_3 | 4:0 | SAMPLE_RATE_DETECT_B[4:0] | 0x00    | Automatic Detection Sample Rate B<br>(Up to four different sample rates can be configured for automatic detection.)<br>Field coding is same as SAMPLE_RATE_n.                 |
| R341 (0x0155)<br>Rate_Estimator_4 | 4:0 | SAMPLE_RATE_DETECT_C[4:0] | 0x00    | Automatic Detection Sample Rate C<br>(Up to four different sample rates can be configured for automatic detection.)<br>Field coding is same as SAMPLE_RATE_n.                 |
| R342 (0x0156)<br>Rate_Estimator_5 | 4:0 | SAMPLE_RATE_DETECT_D[4:0] | 0x00    | Automatic Detection Sample Rate D<br>(Up to four different sample rates can be configured for automatic detection.)<br>Field coding is same as SAMPLE_RATE_n.                 |

In AIF Slave Modes, it is important to ensure that SYSCLK is synchronized with the associated external LRCLK. This can be achieved by selecting an MCLK input that is derived from the same reference as the LRCLK, or can be achieved by selecting the external BCLK or LRCLK signal as a reference input to the FLL, as a source for SYSCLK.

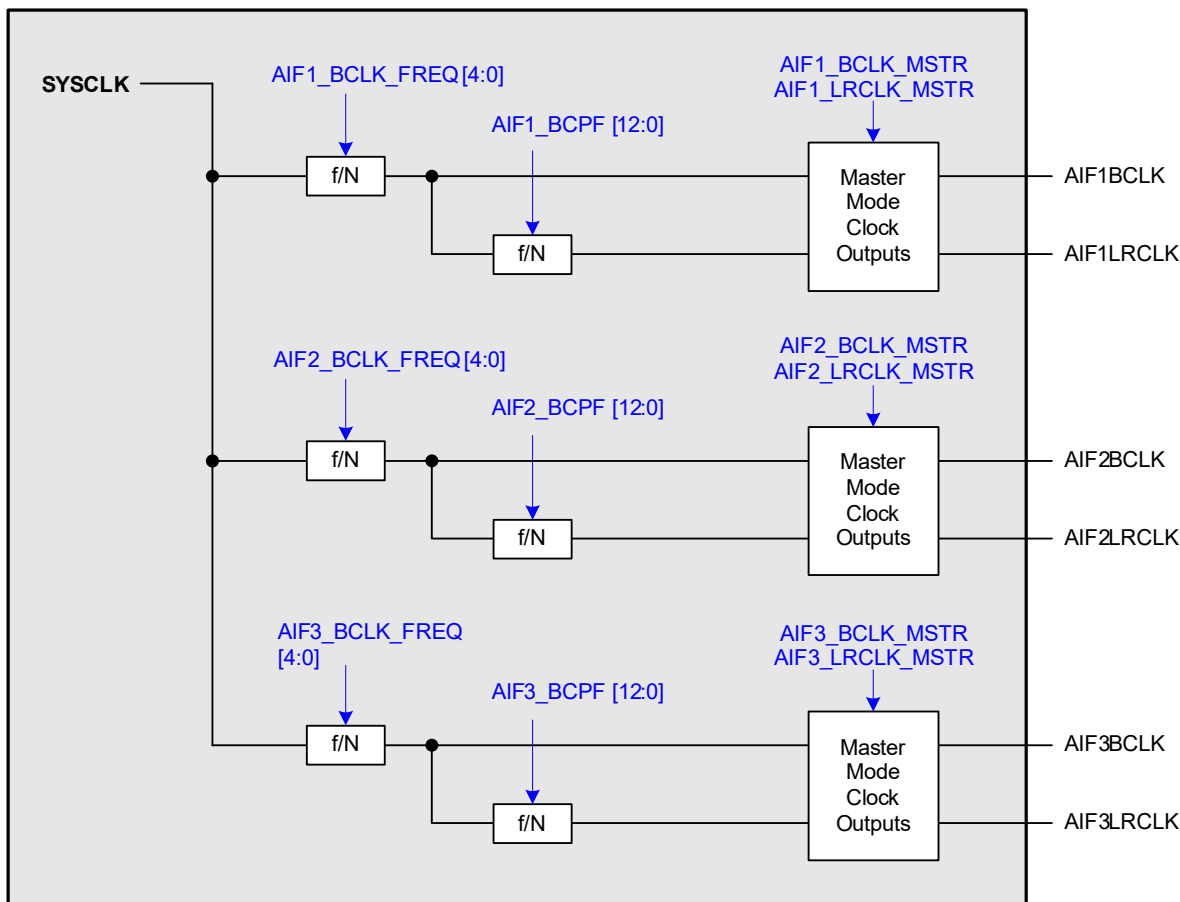
If the AIF clock domain is not synchronized with the LRCLK, clicks arising from dropped or repeated audio samples occur, due to the inherent tolerances of multiple, asynchronous, system clocks. See [Section 5.4](#) for further details on valid clocking configurations.

#### 4.16.7 BCLK and LRCLK Control

The digital audio interfaces (AIF1–AIF3) use BCLK and LRCLK signals for synchronization. In Master Mode, these are output signals, generated by the CS47L35. In Slave Mode, these are input signals to the CS47L35. It is also possible to support mixed master/slave operation.

The BCLK and LRCLK signals are controlled as shown in [Fig. 4-64](#). See [Section 4.7](#) for details of the associated control fields.

Note that the BCLK and LRCLK signals are synchronized to SYSCLK. See [Section 4.3.13](#) for further details.



**Figure 4-64. BCLK and LRCLK Control**

### 4.16.8 Control Interface Clocking

Register map access is possible with or without a system clock—there is no requirement for SYSCLK, or any other system clock, to be enabled when accessing the register map.

See [Section 4.17](#) for details of control register access.

### 4.16.9 Frequency-Locked Loop (FLL)

An integrated FLL is provided to support the clocking requirements of the CS47L35. This can be configured according to the available reference clocks and the application requirements. The reference clock may use a high frequency (e.g., 12.288 MHz) or low frequency (e.g., 32.768 kHz). The FLL is tolerant of jitter and may be used to generate a stable output clock from a less stable input reference.

#### 4.16.9.1 Overview

The FLL characteristics are summarized in [Table 3-11](#). In normal operation, the FLL output is frequency locked to an input clock reference. The FLL can be used to generate a free-running clock in the absence of any external reference, as described in [Section 4.16.9.7](#). Configurable spread-spectrum modulation can be applied to the FLL outputs, to control electro-magnetic interference (EMI) effects.

The FLL comprises two subsystems—the main loop and the synchronizer loop; these can be used together to maintain best frequency accuracy and noise (jitter) performance across multiple use cases. The two-loop design enables the FLL to synchronize effectively to an input clock that may be intermittent or noisy, while also achieving the performance benefits of a stable clock reference that may be asynchronous to the audio data.

The main loop takes a constant and stable clock reference as its input. For best performance, a high-frequency (e.g., 12.288 MHz) reference is recommended. The main FLL loop is free running without any clock reference if the input signal is removed; it can also be configured to initiate an output in the absence of any reference signal.

The synchronizer loop takes a separate clock reference as its input. The synchronizer input may be intermittent (e.g., during voice calls only). The FLL uses the synchronizer input, when available, as the frequency reference. To achieve the designed performance advantage, the synchronizer input must be synchronous with the audio data.

Note that, if only a single clock input reference is used, this must be configured as the main FLL input reference. The synchronizer should be disabled in this case.

The synchronizer loop should only be used when the main loop clock reference is present. If the input reference to the main FLL is intermittent, or may be interrupted unexpectedly, the synchronizer should be disabled.

#### 4.16.9.2 FLL Enable

The FLL is enabled by setting FLL1\_ENA. The FLL synchronizer is enabled by setting FLL1\_SYNC\_ENA. The FLL should be fully configured before setting the FLL1\_ENA bit—this should be set as the final step of the FLL-enable sequence.

The FLL1\_SYNC\_ENA bit should not be changed if FLL1\_ENA is set—the FLL1\_ENA bit should be cleared before setting or clearing FLL1\_SYNC\_ENA.

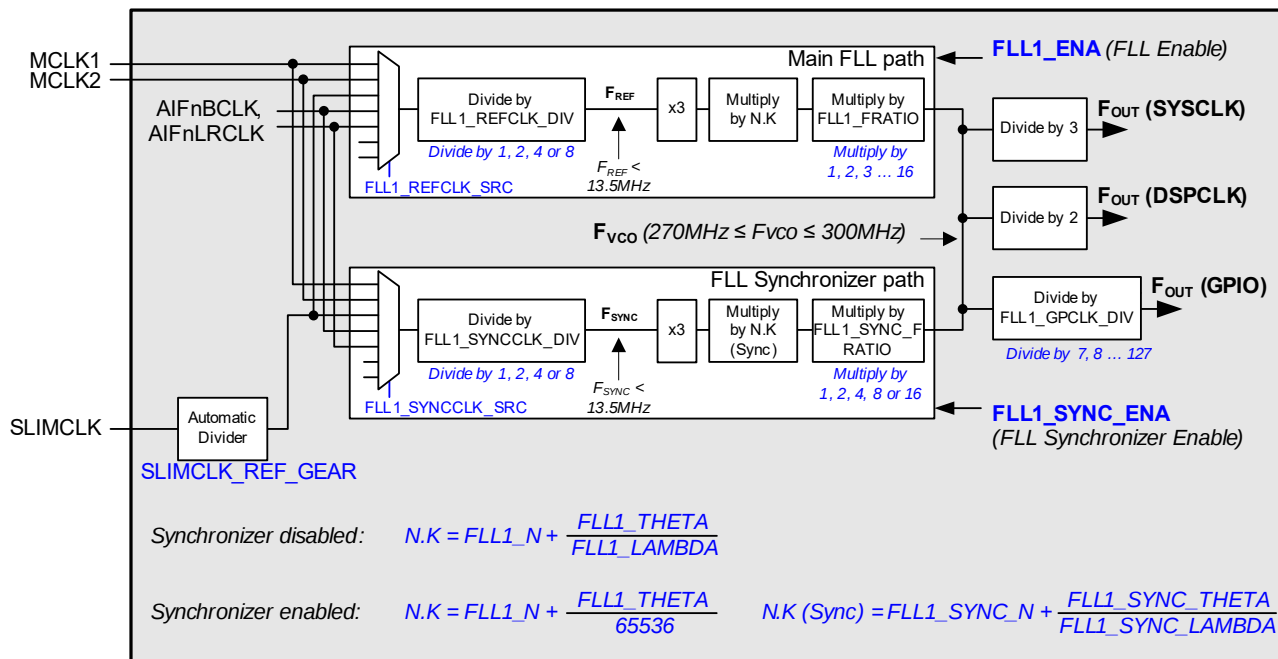
The FLL supports configurable free-running operation, using the FLL1\_FREERUN bit described in [Section 4.16.9.7](#). Note that, once the FLL output has been established, the FLL is always free running if the input reference clock is stopped, regardless of the FLL1\_FREERUN bit.

To disable the FLL while the input reference clock has stopped, FLL1\_FREERUN must be set before clearing the FLL1\_ENA bit.

When changing any of the FLL-configuration fields, it is recommended to disable the FLL by clearing the FLL1\_ENA bit before updating the other register fields; the FLL1\_ENA bit should remain cleared until after the FLL has been reconfigured. If the FLL configuration is changed while the FLL is enabled, the FLL1\_FREERUN bit should be set before updating any other FLL fields. A minimum delay of 32  $\mu$ s should be allowed between setting FLL1\_FREERUN and writing to the required FLL register fields. The FLL1\_FREERUN bit should remain set until after the FLL has been reconfigured.

Note that, if the FLL1\_N or FLL1\_THETA fields are changed while the FLL is enabled, the FLL1\_CTRL\_UPD bit must also be written, as described in [Section 4.16.9.4](#). As a general rule, however, it is recommended to configure the FLL (and FLL synchronizer, if applicable), before setting the FLL1\_ENA bit.

The FLL configuration is shown in [Fig. 4-65](#).



**Figure 4-65. FLL Configuration**

The procedure for configuring the FLL is described in the following subsections. Note that the configuration of the main FLL path and the FLL synchronizer path are very similar. One or both paths must be configured, depending on the application requirements:

- If a single clock input reference is used, only the main FLL path should be used.
- If the input reference to the main FLL is intermittent, or may be interrupted unexpectedly, only the main FLL path should be used.
- If two clock input references are used, the constant or low-noise clock is configured on the main FLL path and the high-accuracy clock is configured on the FLL synchronizer path. Note that the synchronizer input must be synchronous with the audio data.

#### 4.16.9.3 Input Frequency Control

The main input reference is selected using FLL1\_REFCLK\_SRC. The synchronizer input reference is selected using FLL1\_SYNCCLK\_SRC. The available options in each case are MCLK1, MCLK2, SLIMCLK, AIFnBCLK, or AIFnLRCLK.

The SLIMCLK reference is controlled by an adaptive divider on the external SLIMCLK input. The divider automatically adapts to the SLIMbus clock gear, to provide a constant reference frequency for the FLL—see [Section 4.10.7](#).

The FLL1\_REFCLK\_DIV field controls a programmable divider on the main input reference. The FLL1\_SYNCCLK\_DIV field controls a programmable divider on the synchronizer input reference. Each input can be divided by 1, 2, 4 or 8. The divider should be set to bring each reference down to 13.5 MHz or below. For best performance, it is recommended that the highest possible frequency—within the 13.5 MHz limit—should be selected.

#### 4.16.9.4 Output Frequency Control—Main Loop

The FLL output frequency, relative to the main input reference  $F_{REF}$ , is a function of the following:

- The FLL oscillator frequency,  $F_{VCO}$
- The frequency ratio set by FLL1\_FRATIO
- The real number represented by N.K. (N = integer; K = fractional portion)

The  $F_{VCO}$  frequency must be in the range 270–300 MHz.

If the FLL is selected as SYSCLK source, a fixed divider sets the output frequency equal to  $F_{VCO} / 3$ . Therefore,  $F_{VCO}$  must be exactly 294.912 MHz (for 48 kHz–related sample rates) or 270.9504 MHz (for 44.1 kHz–related sample rates).

If the FLL is selected as DSPCLK source, a fixed divider sets the output frequency equal to  $F_{VCO} / 2$ . This enables DSPCLK frequencies in the range 135–150 MHz. A divide-by-six option is also available, supporting low-power DSP operation with DSPCLK frequencies in the range 45–50 MHz. Note that the DSPCLK can be divided to lower clocking rates for each individual DSP.

The FLL clock can be configured as a GPIO output; a programmable divider supports division ratios in the range 7 through 127, enabling a wide range of GPIO clock output frequencies.

**Note:** The chosen  $F_{VCO}$  frequency can be used to support multiple outputs simultaneously (e.g., SYSCLK, DSPCLK, and GPIO), as shown in [Fig. 4-65](#).

The FLL oscillator frequency,  $F_{VCO}$  is set according to the following equation:

$$F_{VCO} = (F_{REF} \times 3 \times N.K \times FLL1\_FRATIO)$$

The value of N.K can thus be determined as follows:

$$N.K = F_{VCO} / (FLL1\_FRATIO \times 3 \times F_{REF})$$

It is recommended to calculate N.K using an initial assumption of  $FLL1\_FRATIO = 1$ . If  $N > 1023$ ,  $FLL1\_FRATIO$  should be incremented until  $N < 1024$ .

Note that, in the above equations, the following interpretations are assumed:

- $F_{REF}$  is the input frequency, after division by  $FLL1\_REFCLK\_DIV$ , where applicable
- $FLL1\_FRATIO$  is the  $F_{VCO}$  clock ratio (1, 2, 3, ... 16)

The value of N is held in  $FLL1\_N$ .

The value of K is determined by the  $FLL1\_THETA$  and  $FLL1\_LAMBDA$  fields:

- In Integer Mode ( $K = 0$ ),  $FLL1\_THETA$  must be set to 0. The  $FLL1\_LAMBDA$  field is not used in Integer Mode.
- In Fractional Mode ( $K > 0$ ), the  $FLL1\_THETA$  and  $FLL1\_LAMBDA$  fields can be derived as described in [Section 4.16.9.6](#).

The  $FLL1\_N$ ,  $FLL1\_THETA$ , and  $FLL1\_LAMBDA$  fields are all coded as integers (LSB = 1).

The  $FLL1\_CTRL\_UPD$  bit controls the updating of the  $FLL1\_N$  or  $FLL1\_THETA$  fields:

- If the  $FLL1\_N$  or  $FLL1\_THETA$  fields are updated while the FLL is enabled ( $FLL1\_ENA = 1$ ), the new values are only effective when a 1 is written to  $FLL1\_CTRL\_UPD$ . This makes it possible to update the two fields simultaneously, without disabling the FLL.

Note that, if the FLL is disabled ( $FLL1\_ENA = 0$ ), the  $FLL1\_N$  and  $FLL1\_THETA$  fields can be updated without writing to  $FLL1\_CTRL\_UPD$ .

The  $FLL1\_GAIN$  and  $FLL1\_PHASE\_ENA$  fields should be set as shown in [Table 4-94](#), depending on  $F_{REF}$ ,  $FLL1\_THETA$ , and whether the FLL synchronizer is enabled.

**Table 4-94. Selection of  $FLL1\_GAIN$  and  $FLL1\_PHASE\_ENA$**

| Condition                                                                                   |                                    | $FLL1\_GAIN$ | $FLL1\_PHASE\_ENA$ |
|---------------------------------------------------------------------------------------------|------------------------------------|--------------|--------------------|
| Synchronizer disabled ( $FLL1\_SYNC\_ENA = 0$ ) and FLL Integer Mode ( $FLL1\_THETA = 0$ )  | $F_{REF} < 768$ kHz                | 0x2          | 1                  |
|                                                                                             | $F_{REF} \geq 768$ kHz             | 0x3          |                    |
| Synchronizer enabled ( $FLL1\_SYNC\_ENA = 1$ ) or FLL Fractional Mode ( $FLL1\_THETA > 0$ ) | $F_{REF} < 100$ kHz                | 0x0          | 0                  |
|                                                                                             | $100$ kHz $\leq F_{REF} < 375$ kHz | 0x2          |                    |
|                                                                                             | $375$ kHz $\leq F_{REF} < 1.5$ MHz | 0x3          |                    |
|                                                                                             | $1.5$ MHz $\leq F_{REF} < 6.0$ MHz | 0x4          |                    |
|                                                                                             | $F_{REF} \geq 6.0$ MHz             | 0x5          |                    |

**Note:**  $F_{REF}$  is the input frequency, after division by  $FLL1\_REFCLK\_DIV$ , where applicable.

Other FLL fields are configured as follows:

- FLL1\_PHASE\_GAIN must be set to 0x2 in all cases.
- FLL1\_CTRL\_RATE must be set to 0x1 in all cases.

#### 4.16.9.5 Output Frequency Control—Synchronizer Loop

A similar procedure applies for the derivation of the FLL synchronizer parameters—assuming that this function is used.

The FLL1\_SYNC\_FRATIO field selects the frequency division ratio of the FLL synchronizer input. The FLL1\_GAIN and FLL1\_SYNC\_DFSAT fields are used to optimize the FLL, according to the input frequency. These fields should be set as described in [Table 4-95](#).

**Note:** The FLL1\_SYNC\_FRATIO coding differs from that of FLL1\_FRATIO.

**Table 4-95. Selection of FLL1\_SYNC\_FRATIO, FLL1\_SYNC\_GAIN, FLL1\_SYNC\_DFSAT**

| Condition                                                | FLL1_SYNC_FRATIO   | FLL1_SYNC_GAIN | FLL1_SYNC_DFSAT      |
|----------------------------------------------------------|--------------------|----------------|----------------------|
| $1 \text{ MHz} \leq F_{\text{SYNC}} < 13.5 \text{ MHz}$  | 0x0 (divide by 1)  | 0x4 (16x gain) | 0 (wide bandwidth)   |
| $256 \text{ kHz} \leq F_{\text{SYNC}} < 1 \text{ MHz}$   | 0x1 (divide by 2)  | 0x2 (4x gain)  | 0 (wide bandwidth)   |
| $128 \text{ kHz} \leq F_{\text{SYNC}} < 256 \text{ kHz}$ | 0x2 (divide by 4)  | 0x0 (1x gain)  | 0 (wide bandwidth)   |
| $64 \text{ kHz} \leq F_{\text{SYNC}} < 128 \text{ kHz}$  | 0x3 (divide by 8)  | 0x0 (1x gain)  | 1 (narrow bandwidth) |
| $F_{\text{SYNC}} < 64 \text{ kHz}$                       | 0x4 (divide by 16) | 0x0 (1x gain)  | 1 (narrow bandwidth) |

**Note:**  $F_{\text{SYNC}}$  is the synchronizer input frequency, after division by FLL1\_SYNCCLK\_DIV, where applicable.

The FLL oscillator frequency,  $F_{\text{VCO}}$ , is the same frequency calculated as described in [Section 4.16.9.4](#).

The value of  $N \cdot K_{\text{SYNC}}$  can then be determined as follows:

$$N \cdot K_{\text{SYNC}} = F_{\text{VCO}} / (\text{FLL1\_SYNC\_FRATIO} \times 3 \times F_{\text{SYNC}})$$

Note that, in the above equation, the following interpretations are assumed:

- $F_{\text{SYNC}}$  is the synchronizer input frequency, after division by FLL1\_SYNCCLK\_DIV, where applicable
- FLL1\_SYNC\_FRATIO is the  $F_{\text{VCO}}$  clock ratio (1, 2, 4, 8, or 16)

The value of  $N_{\text{SYNC}}$  is held in FLL1\_SYNC\_N.

The value of  $K_{\text{SYNC}}$  is determined by the FLL1\_SYNC\_THETA and FLL1\_SYNC\_LAMBDA fields:

- In Integer Mode ( $K_{\text{SYNC}} = 0$ ), FLL1\_SYNC\_THETA must be set to 0. The FLL1\_SYNC\_THETA field is not used in Integer Mode.
- In Fractional Mode ( $K_{\text{SYNC}} > 0$ ), the FLL1\_SYNC\_THETA and FLL1\_SYNC\_LAMBDA fields can be derived as described in [Section 4.16.9.6](#).

The FLL1\_SYNC\_N, FLL1\_SYNC\_THETA, and FLL1\_SYNC\_LAMBDA fields are all coded as integers (LSB = 1).

#### 4.16.9.6 Calculation of Theta and Lambda

In Fractional Mode, with the synchronizer disabled ( $K > 0$ , and FLL1\_SYNC\_ENA = 0), FLL1\_THETA and FLL1\_LAMBDA are calculated with the following steps:

1. Calculate GCD(FLL) using the Greatest Common Denominator function:  
 $\text{GCD}(\text{FLL}) = \text{GCD}(\text{FLL1\_FRATIO} \times F_{\text{REF}}, F_{\text{VCO}} / 3)$ ,  
 where  $\text{GCD}(x, y)$  is the greatest common denominator of  $x$  and  $y$ .  
 $F_{\text{REF}}$  is the input frequency, after division by FLL1\_REFCLK\_DIV, where applicable.
2. Calculate FLL1\_THETA and FLL1\_LAMBDA using the following equations:  
 $\text{FLL1\_THETA} = ((F_{\text{VCO}} / 3) - (\text{FLL1\_N} \times \text{FLL1\_FRATIO} \times F_{\text{REF}})) / \text{GCD}(\text{FLL})$   
 $\text{FLL1\_LAMBDA} = (\text{FLL1\_FRATIO} \times F_{\text{REF}}) / \text{GCD}(\text{FLL})$

Note also that the values of FLL1\_THETA and FLL1\_LAMBDA must be coprime (i.e., not divisible by any common integer). The value of K must be less than 1 (i.e., FLL1\_THETA must be less than FLL1\_LAMBDA).

If the synchronizer is enabled, the FLL1\_SYNC\_THETA and FLL1\_SYNC\_LAMBDA fields are calculated in the same manner described above, using the corresponding synchronizer parameters.

In Fractional Mode, with the synchronizer enabled ( $K > 0$ , and FLL1\_SYNC\_ENA = 1), FLL1\_THETA is calculated as  $FLL1\_THETA = K \times 65536$ . The FLL1\_LAMBDA field is ignored in this case, and the coprime requirement for FLL1\_LAMBDA and FLL1\_THETA is not applicable.

#### 4.16.9.7 Free-Running FLL Mode

The FLL can generate a clock signal even if no external reference is available. This may be because the normal input reference has been interrupted, or may be during a standby or start-up period when no initial reference clock is available.

Free-Running FLL Mode is enabled by setting FLL1\_FREERUN. Note that FLL1\_ENA must also be enabled in Free-Running FLL Mode.

In Free-Running FLL Mode, the normal feedback mechanism of the FLL is halted and the FLL oscillates independently of the external input references.

If the FLL was previously operating normally (with an input reference clock), the FLL output frequency remains unchanged when Free-Running FLL Mode is enabled. The FLL output is independent of the input reference while operating with FLL1\_FREERUN = 1.

The main FLL loop always runs freely if the input reference clock is stopped (regardless of the FLL1\_FREERUN setting). If FLL1\_FREERUN = 0, the FLL relocks to the input reference whenever it is available.

In Free-Running FLL Mode, (with FLL1\_FREERUN = 1), the FLL integrator value (part of the feedback mechanism) can be commanded directly using FLL1\_FRC\_INTEG\_VAL. The integrator value in this field is applied to the FLL when a 1 is written to FLL1\_FRC\_INTEG\_UPD.

If the FLL is started up in Free-Running FLL Mode, (i.e., it was not previously running), the default value of FLL1\_FRC\_INTEG\_VAL is applied.

The FLL integrator value (part of the feedback mechanism) can be read from the FLL1\_INTEG field; the value of this field may be stored for later use. Note that the value of FLL1\_INTEG is only valid if FLL1\_FREERUN = 1 and the FLL1\_INTEG\_VALID = 1.

The FLL integrator setting does not ensure a specific output frequency for the FLL across all devices and operating conditions; some level of variation applies.

The free-running FLL clock may be selected as the SYSCCLK or DSPCLK source, as shown in [Fig. 4-63](#).

#### 4.16.9.8 Spread-Spectrum FLL Control

The CS47L35 can apply modulation to the FLL output, using spread-spectrum techniques. This can be used to control the EMI characteristics of the circuits that are clocked via the FLL.

The FLL can be configured for triangle modulation, zero mean frequency modulation (ZMFM), or dither. The amplitude and frequency parameters of the spread spectrum functions is also programmable, using the fields described in [Section 4.16.9.9](#).

#### 4.16.9.9 FLL Control Registers

The FLL control registers are described in [Table 4-96](#).

Example settings for a variety of reference frequencies and output frequencies are shown in [Section 4.16.9.12](#).

**Table 4-96. FLL1 Register Map**

| Register Address                         | Bit  | Label                    | Default | Description                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------------------------------------------|------|--------------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R369 (0x0171)<br>FLL1_Control_1          | 1    | FLL1_FREERUN             | 1       | FLL1 Free-Running Mode Enable<br>0 = Disabled<br>1 = Enabled<br>The FLL feedback mechanism is halted in Free-Running FLL Mode, and the latest integrator setting is maintained                                                                                                                                                                                                                                                       |
|                                          | 0    | FLL1_ENA                 | 0       | FLL1 Enable<br>0 = Disabled<br>1 = Enabled<br>This should be set as the final step of the FLL1 enable sequence, i.e., after the other FLL fields have been configured.                                                                                                                                                                                                                                                               |
| R370 (0x0172)<br>FLL1_Control_2          | 15   | FLL1_CTRL_UPD            | 0       | FLL1 Control Update<br>Write 1 to apply the FLL1_N and FLL1_THETA field settings.<br>(Only valid if FLL1_ENA = 1)                                                                                                                                                                                                                                                                                                                    |
|                                          | 9:0  | FLL1_N[9:0]              | 0x008   | FLL1 Integer multiply for $F_{REF}$<br>(LSB = 1)<br>If updated while the FLL is enabled, the new value is only effective when a 1 is written to FLL1_CTRL_UPD.                                                                                                                                                                                                                                                                       |
| R371 (0x0173)<br>FLL1_Control_3          | 15:0 | FLL1_THETA[15:0]         | 0x0018  | FLL1 Fractional multiply for $F_{REF}$ . Sets the numerator (multiply) part of the FLL1_THETA / FLL1_LAMBDA ratio.<br>Coded as LSB = 1.<br>If updated while the FLL is enabled, the new value is only effective when a 1 is written to FLL1_CTRL_UPD.                                                                                                                                                                                |
| R372 (0x0174)<br>FLL1_Control_4          | 15:0 | FLL1_LAMBDA[15:0]        | 0x007D  | FLL1 Fractional multiply for $F_{REF}$<br>This field sets the denominator (dividing) part of the FLL1_THETA / FLL1_LAMBDA ratio.<br>Coded as LSB = 1.                                                                                                                                                                                                                                                                                |
| R373 (0x0175)<br>FLL1_Control_5          | 11:8 | FLL1_FRATIO[3:0]         | 0x0     | FLL1 $F_{VCO}$ clock divider<br>0x0 = 1                                      0x2 = 3                                      ...<br>0x1 = 2                                      0x3 = 4                                      0xF = 16                                                                                                                                                                                                  |
| R374 (0x0176)<br>FLL1_Control_6          | 7:6  | FLL1_REFCLK_DIV[1:0]     | 00      | FLL1 Clock Reference Divider<br>00 = 1                                      10 = 4<br>01 = 2                                      11 = 8<br>MCLK (or other input reference) must be divided down to $\leq 13.5$ MHz.                                                                                                                                                                                                                 |
|                                          | 3:0  | FLL1_REFCLK_SRC[3:0]     | 0000    | FLL1 Clock source<br>0000 = MCLK1                                      1001 = AIF2BCLK                                      1110 = AIF3LRCLK<br>0001 = MCLK2                                      1010 = AIF3BCLK                                      All other codes are reserved<br>0011 = SLIMCLK                                      1100 = AIF1LRCLK<br>1000 = AIF1BCLK                                      1101 = AIF2LRCLK |
| R375 (0x0177)<br>FLL1_Loop_Filter_Test_1 | 15   | FLL1_FRC_INTEG_UPD       | 0       | Write 1 to apply the FLL1_FRC_INTEG_VAL setting.<br>(Only valid if FLL1_FREERUN = 1)                                                                                                                                                                                                                                                                                                                                                 |
|                                          | 11:0 | FLL1_FRC_INTEG_VAL[11:0] | 0x281   | FLL1 Forced Integrator Value                                                                                                                                                                                                                                                                                                                                                                                                         |
| R376 (0x0178)<br>FLL1_NCO_Test_0         | 15   | FLL1_INTEG_VALID         | 0       | FLL1 Integrator Valid. Indicates whether FLL1_INTEG is valid<br>0 = Not valid<br>1 = Valid                                                                                                                                                                                                                                                                                                                                           |
|                                          | 11:0 | FLL1_INTEG[11:0]         | 0x000   | FLL1 Integrator Value (Read-only). Indicates the current FLL1 integrator setting. Only valid if FLL1_INTEG_VALID = 1.                                                                                                                                                                                                                                                                                                                |
| R377 (0x0179)<br>FLL1_Control_7          | 5:2  | FLL1_GAIN[3:0]           | 0000    | FLL1 Gain<br>0000 = 1                                      0011 = 8                                      0110 = 64<br>0001 = 2                                      0100 = 16                                      0111 = 128<br>0010 = 4                                      0101 = 32                                      1000–1111 = 256                                                                                        |

**Table 4-96. FLL1 Register Map (Cont.)**

| Register Address                      | Bit   | Label                  | Default | Description                                                                                                                                                                                                                                                                    |
|---------------------------------------|-------|------------------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R378 (0x017A)<br>FLL1_Control_8       | 15:12 | FLL1_PHASE_GAIN[3:0]   | 0010    | FLL1 Phase Gain<br>0000 = Reserved      0011 = 8      0110 = 64<br>0001 = Reserved      0100 = 16      0111 = 128<br>0010 = 4      0101 = 32      1000–1111 = 256                                                                                                              |
|                                       | 11    | FLL1_PHASE_ENA         | 1       | FLL1 Phase Integrator Control<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                   |
|                                       | 10:8  | FLL1_CTRL_RATE[2:0]    | 001     | FLL1 Control Ratio<br>000 = 1      011 = 8      110 = 64<br>001 = 2      100 = 16      111 = 128<br>010 = 4      101 = 32                                                                                                                                                      |
| R383 (0x017F)<br>FLL1_Synchroniser_1  | 0     | FLL1_SYNC_ENA          | 0       | FLL1 Synchronizer Enable<br>0 = Disabled<br>1 = Enabled<br>This should be set as the final step of the FLL1 synchronizer enable sequence, i.e., after the other synchronizer fields have been configured.                                                                      |
| R384 (0x0180)<br>FLL1_Synchroniser_2  | 9:0   | FLL1_SYNC_N[9:0]       | 0x000   | FLL1 Integer multiply for F <sub>SYNC</sub><br>(LSB = 1)                                                                                                                                                                                                                       |
| R385 (0x0181)<br>FLL1_Synchroniser_3  | 15:0  | FLL1_SYNC_THETA[15:0]  | 0x0000  | FLL1 Fractional multiply for F <sub>SYNC</sub><br>This field sets the numerator (multiply) part of the FLL1_SYNC_THETA / FLL1_SYNC_LAMBDA ratio.<br>Coded as LSB = 1.                                                                                                          |
| R386 (0x0182)<br>FLL1_Synchroniser_4  | 15:0  | FLL1_SYNC_LAMBDA[15:0] | 0x0000  | FLL1 Fractional multiply for F <sub>SYNC</sub><br>This field sets the denominator (dividing) part of the FLL1_SYNC_THETA / FLL1_SYNC_LAMBDA ratio.<br>Coded as LSB = 1.                                                                                                        |
| R387 (0x0183)<br>FLL1_Synchroniser_5  | 10:8  | FLL1_SYNC_FRATIO[2:0]  | 000     | FLL1 Synchronizer F <sub>VCO</sub> clock divider<br>000 = 1      010 = 4      1XX = 16<br>001 = 2      011 = 8                                                                                                                                                                 |
| R388 (0x0184)<br>FLL1_Synchroniser_6  | 7:6   | FLL1_SYNCCLK_DIV[1:0]  | 00      | FLL1 Synchronizer Clock Reference Divider<br>00 = 1      10 = 4<br>01 = 2      11 = 8<br>MCLK (or other input reference) must be divided down to ≤13.5 MHz.                                                                                                                    |
|                                       | 3:0   | FLL1_SYNCCLK_SRC       | 0000    | FLL1 Synchronizer Clock source<br>0000 = MCLK1      1001 = AIF2BCLK      1101 = AIF2LRCLK<br>0001 = MCLK2      1010 = AIF3BCLK      1110 = AIF3LRCLK<br>0011 = SLIMCLK      1100 = AIF1LRCLK      All other codes are reserved<br>1000 = AIF1BCLK                              |
| R389 (0x0185)<br>FLL1_Synchroniser_7  | 5:2   | FLL1_SYNC_GAIN[3:0]    | 0000    | FLL1 Synchronizer Gain<br>0000 = 1      0011 = 8      0110 = 64<br>0001 = 2      0100 = 16      0111 = 128<br>0010 = 4      0101 = 32      1000–1111 = 256                                                                                                                     |
|                                       | 0     | FLL1_SYNC_DFSAT        | 1       | FLL1 Synchronizer Bandwidth<br>0 = Wide bandwidth<br>1 = Narrow bandwidth                                                                                                                                                                                                      |
| R391 (0x0187)<br>FLL1_Spread_Spectrum | 5:4   | FLL1_SS_AMPL[1:0]      | 00      | FLL1 Spread Spectrum Amplitude. Controls the extent of the spread-spectrum modulation.<br>00 = 0.7% (triangle), 0.7% (ZMFM, dither)      10 = 2.3% (triangle), 2.6% (ZMFM, dither)<br>01 = 1.1% (triangle), 1.3% (ZMFM, dither)      11 = 4.6% (triangle), 5.2% (ZMFM, dither) |
|                                       | 3:2   | FLL1_SS_FREQ[1:0]      | 00      | FLL1 Spread Spectrum Frequency. Controls the spread spectrum modulation frequency in Triangle Mode.<br>00 = 439 kHz      10 = 1.17 MHz<br>01 = 878 kHz      11 = 1.76 MHz                                                                                                      |
|                                       | 1:0   | FLL1_SS_SEL[1:0]       | 00      | FLL1 Spread Spectrum Select.<br>00 = Disabled      10 = Triangle<br>01 = Zero Mean Frequency (ZMFM)      11 = Dither                                                                                                                                                           |

#### 4.16.9.10 FLL Interrupts and GPIO Output

The CS47L35 provides an FLL lock signal, which indicates whether FLL lock has been achieved (i.e., the FLL is locked to the input reference signal).

The FLL lock signal is an input to the interrupt control circuit and can be used to trigger an interrupt event; see [Section 4.15](#). Note that the interrupt signal is debounced, and requires clocking to be present in order to assert the respective interrupt; either the 32-kHz clock, or the SYSCLK signal, must be enabled to trigger an interrupt from the FLL lock signal.

The FLL lock signal can be output directly on a GPIO pin as an external indication of the FLL status. See [Section 4.14](#) to configure a GPIO pin for these functions. (This GPIO output is not debounced, and does not require clocking to be present.)

Clock output signals derived from the FLL can be output on a GPIO pin. See [Section 4.14](#) to configure a GPIO pin for this function.

The FLL clocking configuration is shown in [Fig. 4-65](#).

#### 4.16.9.11 Example FLL Calculation

The following example illustrates how to derive the FLL1 register fields to generate an oscillator frequency ( $F_{VCO}$ ) of 294.912 MHz from a 12.000-MHz reference clock ( $F_{REF}$ ). This is suitable for generating SYSCLK at 98.304 MHz and/or DSPCLK at 147.456 MHz.

Note that, for the purposes of this calculation, it is assumed that the synchronizer is disabled.

1. Set FLL1\_REFCLK\_DIV to generate  $F_{REF} \leq 13.5$  MHz:  
FLL1\_REFCLK\_DIV = 00 (divide by 1)
2. Calculate N.K as given by  $N.K = F_{VCO} / (FLL1\_FRATIO \times 3 \times F_{REF})$ . Assume FLL1\_FRATIO = 0x0 (divide by 1).  
 $N.K = 294912000 / (1 \times 3 \times 12000000) = 8.192$
3. Confirm that the calculated value of N is less than 1024.
4. Determine FLL1\_N from the integer portion of N.K:  
FLL1\_N = 8 (0x008)
5. Determine GCD(FLL), as given by  $GCD(FLL) = GCD(FLL1\_FRATIO \times F_{REF}, F_{VCO} / 3)$ :  
 $GCD(FLL) = GCD(1 \times 12000000, 294912000 / 3) = 96000$
6. Determine FLL1\_THETA, as given by  $FLL1\_THETA = (F_{VCO} / 3 - (FLL1\_N \times FLL1\_FRATIO \times F_{REF})) / GCD(FLL)$ :  
 $FLL1\_THETA = ((294912000 / 3) - (8 \times 1 \times 12000000)) / 96000$   
FLL1\_THETA = 24 (0x0018)
7. Determine FLL1\_LAMBDA, as given by  $FLL1\_LAMBDA = (FLL1\_FRATIO \times F_{REF}) / GCD(FLL)$ :  
 $FLL1\_LAMBDA = (1 \times 12000000) / 96000$   
FLL1\_LAMBDA = 125 (0x007D)
8. Determine FLL1\_GAIN, FLL1\_PHASE\_GAIN, FLL1\_PHASE\_ENA, and FLL1\_CTRL\_RATE as specified in [Section 4.16.9.4](#):  
FLL1\_GAIN = 0x5  
FLL1\_PHASE\_GAIN = 0x2  
FLL1\_PHASE\_ENA = 1  
FLL1\_CTRL\_RATE = 0x1

### 4.16.9.12 Example FLL Settings

Table 4-97 shows FLL settings for generating an oscillator frequency ( $F_{VCO}$ ) of 294.912 MHz from a variety of low- and high-frequency reference inputs. This is suitable for generating SYSCLK at 98.304 MHz and/or DSPCLK at 147.456 MHz.

The recommended values of FLL1\_PHASE\_GAIN (0x2) and FLL1\_CTRL\_RATE (0x1) are also applicable in each case.

Note that the FLL settings in Table 4-97 assume that the synchronizer is disabled.

**Table 4-97. Example FLL Settings—Synchronizer Disabled**

| FLL (Main Loop) Settings |                                     |                                       |                     |                  |        |            |             |           |                |
|--------------------------|-------------------------------------|---------------------------------------|---------------------|------------------|--------|------------|-------------|-----------|----------------|
| F <sub>SOURCE</sub>      | F <sub>VCO</sub> (MHz) <sup>1</sup> | F <sub>REF</sub> Divider <sup>2</sup> | FRATIO <sup>2</sup> | N.K <sup>3</sup> | FLL1_N | FLL1_THETA | FLL1_LAMBDA | FLL1_GAIN | FLL1_PHASE_ENA |
| 32.000 kHz               | 294.912                             | 1                                     | 4                   | 768              | 0x300  | 0x0000     | 0x0001      | 0x2       | 1              |
| 32.768 kHz               | 294.912                             | 1                                     | 3                   | 1000             | 0x3E8  | 0x0000     | 0x0001      | 0x2       | 1              |
| 48 kHz                   | 294.912                             | 1                                     | 3                   | 682.6667         | 0x2AA  | 0x0002     | 0x0003      | 0x0       | 0              |
| 128 kHz                  | 294.912                             | 1                                     | 1                   | 768              | 0x300  | 0x0000     | 0x0001      | 0x2       | 1              |
| 512 kHz                  | 294.912                             | 1                                     | 1                   | 192              | 0x0C0  | 0x0000     | 0x0001      | 0x2       | 1              |
| 1.536 MHz                | 294.912                             | 1                                     | 1                   | 64               | 0x040  | 0x0000     | 0x0001      | 0x3       | 1              |
| 3.072 MHz                | 294.912                             | 1                                     | 1                   | 32               | 0x020  | 0x0000     | 0x0001      | 0x3       | 1              |
| 11.2896 MHz              | 294.912                             | 1                                     | 1                   | 8.7075           | 0x008  | 0x0068     | 0x0093      | 0x5       | 0              |
| 12.000 MHz               | 294.912                             | 1                                     | 1                   | 8.192            | 0x008  | 0x0018     | 0x007D      | 0x5       | 0              |
| 12.288 MHz               | 294.912                             | 1                                     | 1                   | 8                | 0x008  | 0x0000     | 0x0001      | 0x3       | 1              |
| 13.000 MHz               | 294.912                             | 1                                     | 1                   | 7.5618           | 0x007  | 0x0391     | 0x0659      | 0x5       | 0              |
| 19.200 MHz               | 294.912                             | 2                                     | 1                   | 10.24            | 0x00A  | 0x0006     | 0x0019      | 0x5       | 0              |
| 24 MHz                   | 294.912                             | 2                                     | 1                   | 8.192            | 0x008  | 0x0018     | 0x007D      | 0x5       | 0              |
| 26 MHz                   | 294.912                             | 2                                     | 1                   | 7.5618           | 0x007  | 0x0391     | 0x0659      | 0x5       | 0              |
| 27 MHz                   | 294.912                             | 2                                     | 1                   | 7.2818           | 0x007  | 0x013D     | 0x0465      | 0x5       | 0              |

1.  $F_{VCO} = (F_{SOURCE}/F_{REF} \text{ Divider}) \times 3 \times N.K \times FRATIO$

2. See Table 4-96 for the coding of the FLL1\_REFCLK\_DIV and FLL1\_FRATIO fields.

3. N.K values are represented in the FLL1\_N, FLL1\_THETA, and FLL1\_LAMBDA fields.

Table 4-98 shows example FLL settings for generating an oscillator frequency ( $F_{VCO}$ ) of 294.912 MHz from a variety of low- and high-frequency reference inputs, with the synchronizer enabled. The main loop and the synchronizer loop must each be configured according to the respective input source.

Note that, if the FLL synchronizer is enabled, the recommended settings for the main loop are not the same as those described in Table 4-97.

**Table 4-98. Example FLL Settings—Synchronizer Enabled**

| FLL (Main Loop) Settings         |                              |                                    |                     |                  |             |                 |                  |                |                 |
|----------------------------------|------------------------------|------------------------------------|---------------------|------------------|-------------|-----------------|------------------|----------------|-----------------|
| $F_{SOURCE}$                     | $F_{VCO}$ (MHz) <sup>1</sup> | $F_{REF}$<br>Divider <sup>2</sup>  | FRATIO <sup>2</sup> | N.K <sup>3</sup> | FLL1_N      | FLL1_THETA      | FLL1_LAMBDA      | FLL1_GAIN      | FLL1_PHASE_ENA  |
| 32.000 kHz                       | 294.912                      | 1                                  | 4                   | 768              | 0x300       | 0x0000          | 0x0000           | 0x0            | 0               |
| 32.768 kHz                       | 294.912                      | 1                                  | 3                   | 1000             | 0x3E8       | 0x0000          | 0x0000           | 0x0            | 0               |
| 48 kHz                           | 294.912                      | 1                                  | 3                   | 682.6667         | 0x2AA       | 0xAAAA          | 0x0000           | 0x0            | 0               |
| 128 kHz                          | 294.912                      | 1                                  | 1                   | 768              | 0x300       | 0x0000          | 0x0000           | 0x2            | 0               |
| 512 kHz                          | 294.912                      | 1                                  | 1                   | 192              | 0x0C0       | 0x0000          | 0x0000           | 0x3            | 0               |
| 1.536 MHz                        | 294.912                      | 1                                  | 1                   | 64               | 0x040       | 0x0000          | 0x0000           | 0x4            | 0               |
| 3.072 MHz                        | 294.912                      | 1                                  | 1                   | 32               | 0x020       | 0x0000          | 0x0000           | 0x4            | 0               |
| 11.2896 MHz                      | 294.912                      | 1                                  | 1                   | 8.7075           | 0x008       | 0xB51D          | 0x0000           | 0x5            | 0               |
| 12.000 MHz                       | 294.912                      | 1                                  | 1                   | 8.192            | 0x008       | 0x3126          | 0x0000           | 0x5            | 0               |
| 12.288 MHz                       | 294.912                      | 1                                  | 1                   | 8                | 0x008       | 0x0000          | 0x0000           | 0x5            | 0               |
| 13.000 MHz                       | 294.912                      | 1                                  | 1                   | 7.5618           | 0x007       | 0x8FD5          | 0x0000           | 0x5            | 0               |
| 19.200 MHz                       | 294.912                      | 2                                  | 1                   | 10.24            | 0x00A       | 0x3D70          | 0x0000           | 0x5            | 0               |
| 24 MHz                           | 294.912                      | 2                                  | 1                   | 8.192            | 0x008       | 0x3126          | 0x0000           | 0x5            | 0               |
| 26 MHz                           | 294.912                      | 2                                  | 1                   | 7.5618           | 0x007       | 0x8FD5          | 0x0000           | 0x5            | 0               |
| 27 MHz                           | 294.912                      | 2                                  | 1                   | 7.2818           | 0x007       | 0x4822          | 0x0000           | 0x5            | 0               |
| FLL (Synchronizer Loop) Settings |                              |                                    |                     |                  |             |                 |                  |                |                 |
| $F_{SOURCE}$                     | $F_{VCO}$ (MHz) <sup>4</sup> | $F_{SYNC}$<br>Divider <sup>5</sup> | FRATIO <sup>5</sup> | N.K <sup>6</sup> | FLL1_SYNC_N | FLL1_SYNC_THETA | FLL1_SYNC_LAMBDA | FLL1_SYNC_GAIN | FLL1_SYNC_DFSAT |
| 32.000 kHz                       | 294.912                      | 1                                  | 16                  | 192              | 0x0C0       | 0x0000          | 0x0001           | 0x0            | 1               |
| 32.768 kHz                       | 294.912                      | 1                                  | 16                  | 187.5            | 0x0BB       | 0x0001          | 0x0002           | 0x0            | 1               |
| 48 kHz                           | 294.912                      | 1                                  | 16                  | 128              | 0x080       | 0x0000          | 0x0001           | 0x0            | 1               |
| 128 kHz                          | 294.912                      | 1                                  | 4                   | 192              | 0x0C0       | 0x0000          | 0x0001           | 0x0            | 0               |
| 512 kHz                          | 294.912                      | 1                                  | 2                   | 96               | 0x060       | 0x0000          | 0x0001           | 0x2            | 0               |
| 1.536 MHz                        | 294.912                      | 1                                  | 1                   | 64               | 0x040       | 0x0000          | 0x0001           | 0x4            | 0               |
| 3.072 MHz                        | 294.912                      | 1                                  | 1                   | 32               | 0x020       | 0x0000          | 0x0001           | 0x4            | 0               |
| 11.2896 MHz                      | 294.912                      | 1                                  | 1                   | 8.7075           | 0x008       | 0x0068          | 0x0093           | 0x4            | 0               |
| 12.000 MHz                       | 294.912                      | 1                                  | 1                   | 8.192            | 0x008       | 0x0018          | 0x007D           | 0x4            | 0               |
| 12.288 MHz                       | 294.912                      | 1                                  | 1                   | 8                | 0x008       | 0x0000          | 0x0001           | 0x4            | 0               |
| 13.000 MHz                       | 294.912                      | 1                                  | 1                   | 7.5618           | 0x007       | 0x0391          | 0x0659           | 0x4            | 0               |
| 19.200 MHz                       | 294.912                      | 2                                  | 1                   | 10.24            | 0x00A       | 0x0006          | 0x0019           | 0x4            | 0               |
| 24 MHz                           | 294.912                      | 2                                  | 1                   | 8.192            | 0x008       | 0x0018          | 0x007D           | 0x4            | 0               |
| 26 MHz                           | 294.912                      | 2                                  | 1                   | 7.5618           | 0x007       | 0x0391          | 0x0659           | 0x4            | 0               |
| 27 MHz                           | 294.912                      | 2                                  | 1                   | 7.2818           | 0x007       | 0x013D          | 0x0465           | 0x4            | 0               |

1.  $F_{VCO} = (F_{SOURCE}/F_{REF} \text{ Divider}) \times 3 \times N.K \times FRATIO$

2. See Table 4-96 for the coding of the FLL1\_REFCLK\_DIV and FLL1\_FRATIO fields.

3. N.K values are represented in the FLL1\_N, FLL1\_THETA, and FLL1\_LAMBDA fields.

4.  $F_{VCO} = (F_{SOURCE}/F_{SYNC} \text{ Divider}) \times 3 \times N.K \times FRATIO$

5. See Table 4-96 for the coding of the FLL1\_SYNCCLK\_DIV and FLL1\_SYNC\_FRATIO fields.

6. N.K values are represented in the FLL1\_SYNC\_N, FLL1\_SYNC\_THETA, and FLL1\_SYNC\_LAMBDA fields.

## 4.17 Control Interface

The CS47L35 is controlled by read/write access to its control registers. Two independent control interfaces are provided, giving flexible capability as described below. Note that the SLIMbus interface also supports read/write access to the CS47L35 control registers; see [Section 4.10](#).

Register access is possible on all of the control interfaces (including SLIMbus) simultaneously. Note that the control interface function can be supported with or without system clocking—there is no requirement for SYSCLK, or any other system clock, to be enabled when accessing the register map.

The CS47L35 executes a boot sequence following power-on reset, hardware reset, software reset, or wake-up from Sleep Mode. Note that control register writes should not be attempted until the boot sequence has completed. See [Section 4.22](#) for further details.

A summary of the CS47L35 control interfaces is described in [Table 4-99](#).

**Table 4-99. CS47L35 Control Interface Summary**

| Control Interface | Description                           | Pin Functions                                                                                              | Power Domain |
|-------------------|---------------------------------------|------------------------------------------------------------------------------------------------------------|--------------|
| CIF1              | Four-wire (SPI) interface             | CIF1MISO—Data output<br>CIF1MOSI—Data input<br>CIF1SCLK—Interface clock input<br>CIF1SS—Slave select input | DBVDD1       |
| CIF2              | Two-wire (I <sup>2</sup> C) interface | CIF2SCLK—Interface clock input<br>CIF2SDA—Data input/output                                                | DBVDD1       |

The CS47L35 provides an integrated pull-down resistor on the CIF1MISO pin. This provides a flexible capability for interfacing with other devices. The pull-down is enabled by setting CIF1MISO\_PD, as described in [Table 4-100](#).

**Table 4-100. Control Interface Pull-Down**

| Register Address             | Bit | Label       | Default | Description                                               |
|------------------------------|-----|-------------|---------|-----------------------------------------------------------|
| R8 (0x0008)<br>Ctrl_IF_CFG_1 | 7   | CIF1MISO_PD | 0       | CIF1MISO Pull-Down Control<br>0 = Disabled<br>1 = Enabled |

A detailed description of the I<sup>2</sup>C and SPI interface modes is provided in the following sections.

### 4.17.1 Four-Wire (SPI) Control Mode

The SPI control interface mode is supported on CIF1 only and uses the respective  $\overline{SS}$ , SCLK, MOSI, and MISO pins.

In write operations ( $R/\overline{W} = 0$ ), the MOSI pin input is driven by the controlling device.

In read operations ( $R/\overline{W} = 1$ ), the MOSI pin is ignored following receipt of the valid register address.

If  $\overline{SS}$  is asserted (Logic 0), the MISO output is actively driven when outputting data and is high impedance at other times. If  $\overline{SS}$  is not asserted, the MISO output is high impedance.

The high-impedance state of the MISO output allows the pin to be shared with other slaves. An internal pull-down resistor can be enabled on the CIF1MISO pin, as described in [Table 4-100](#).

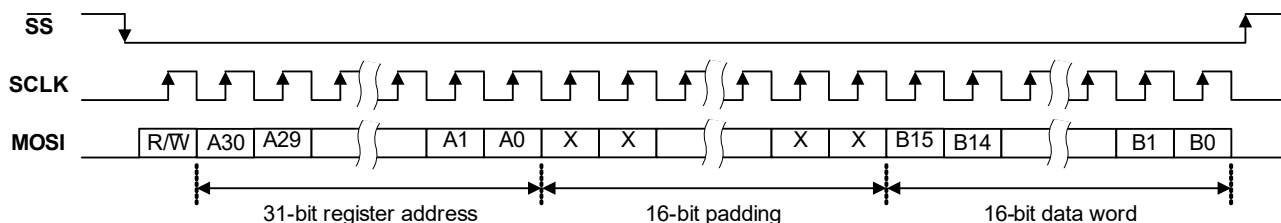
Data transfers on CIF1 must use the applicable SPI message format, according to the register address space that is being accessed:

- When accessing register addresses below R12288 (0x3000), the applicable SPI protocol comprises a 31-bit register address and 16-bit data words.
- When accessing register addresses from R12888 (0x3000) upwards, the applicable SPI protocol comprises a 31-bit register address and 32-bit data words.
- Note that, in all cases, the complete SPI message protocol also includes a read/write bit and a 16-bit padding phase (see [Fig. 4-66](#) and [Fig. 4-67](#) below).

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS47L35 automatically increments the register address at the end of each data word, for as long as  $\overline{SS}$  is held low and SCLK is toggled. Successive data words can be input/output every 16 (or 32) clock cycles (depending on the applicable register address space).

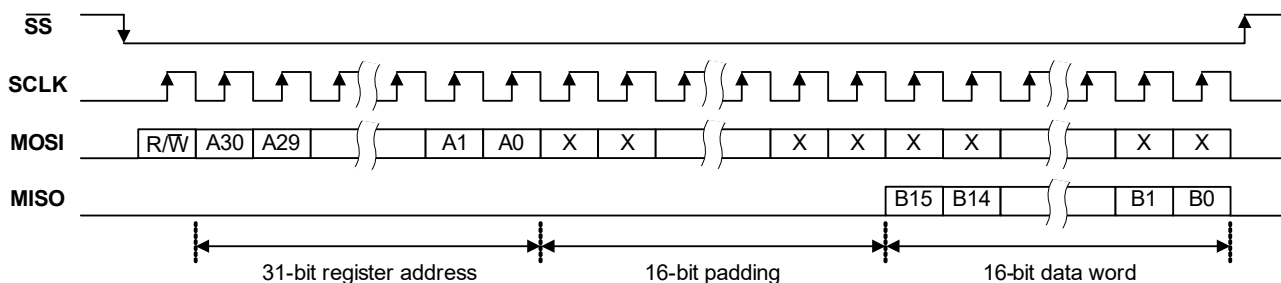
The SPI protocol is shown in Fig. 4-66 and Fig. 4-67. Note that 16-bit data words are shown, but the equivalent protocol also applies to 32-bit data words.

Fig. 4-66 shows a single register write to a specified address.



**Figure 4-66. Control Interface SPI Register Write (16-Bit Data Words)**

Fig. 4-67 shows a single register read from a specified address.



**Figure 4-67. Control Interface SPI Register Read (16-Bit Data Words)**

### 4.17.2 Two-Wire (I<sup>2</sup>C) Control Mode

The I<sup>2</sup>C control interface mode is supported on CIF2 only and uses the respective SCLK and SDA pins.

In I<sup>2</sup>C Mode, the CS47L35 is a slave device on the control interface; SCLK is a clock input, while SDA is a bidirectional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the CS47L35 transmits Logic 1 by tristating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the Logic 1 can be recognized by the master.

In order to allow many devices to share a single two-wire control bus, every device on the bus has a unique 8-bit device ID (this is not the same as the address of each register in the CS47L35).

The CS47L35 device ID is 0011\_0100 (0x34). Note that the LSB of the device ID is the read/write bit; this bit is set to Logic 1 for read and Logic 0 for write.

The CS47L35 operates as a slave device only. The controller indicates the start of data transfer with a high-to-low transition on SDA while SCLK remains high. This indicates that a device ID and subsequent address/data bytes follow. The CS47L35 responds to the start condition and shifts in the next 8 bits on SDA (8-bit device ID, including read/write bit, MSB first). If the device ID received matches the device ID of the CS47L35, the CS47L35 responds by pulling SDA low on the next clock pulse (ACK). If the device ID is not recognized or the R/W bit is set incorrectly, the CS47L35 returns to the idle condition and waits for a new start condition.

If the device ID matches the device ID of the CS47L35, the data transfer continues. The controller indicates the end of data transfer with a low-to-high transition on SDA while SCLK remains high. After receiving a complete address and data sequence the CS47L35 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e., SDA changes while SCLK is high), the device returns to the idle condition.

Data transfers on CIF2 must use the applicable I<sup>2</sup>C message format, according to the register address space that is being accessed:

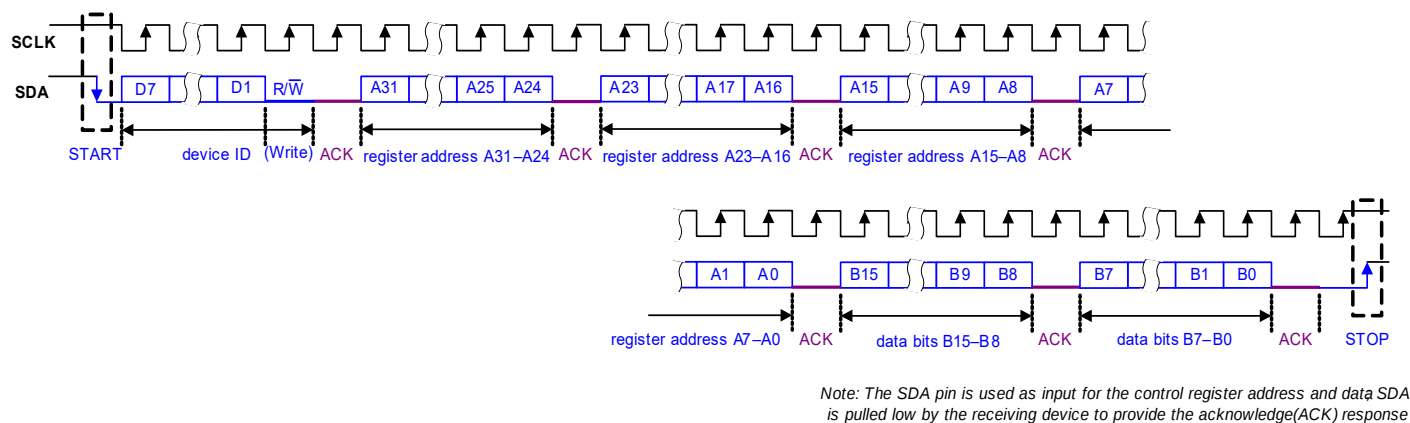
- When accessing register addresses below R12288 (0x3000), the applicable I<sup>2</sup>C protocol comprises a 32-bit register address and 16-bit data words.
- When accessing register addresses from R12888 (0x3000) upwards, the applicable I<sup>2</sup>C protocol comprises a 32-bit register address and 32-bit data words.
- Note that, in all cases, the complete I<sup>2</sup>C message protocol also includes a device ID, a read/write bit, and other signaling bits (see Fig. 4-68 and Fig. 4-69).

The CS47L35 supports the following read and write operations:

- Single write
- Single read
- Multiple write
- Multiple read

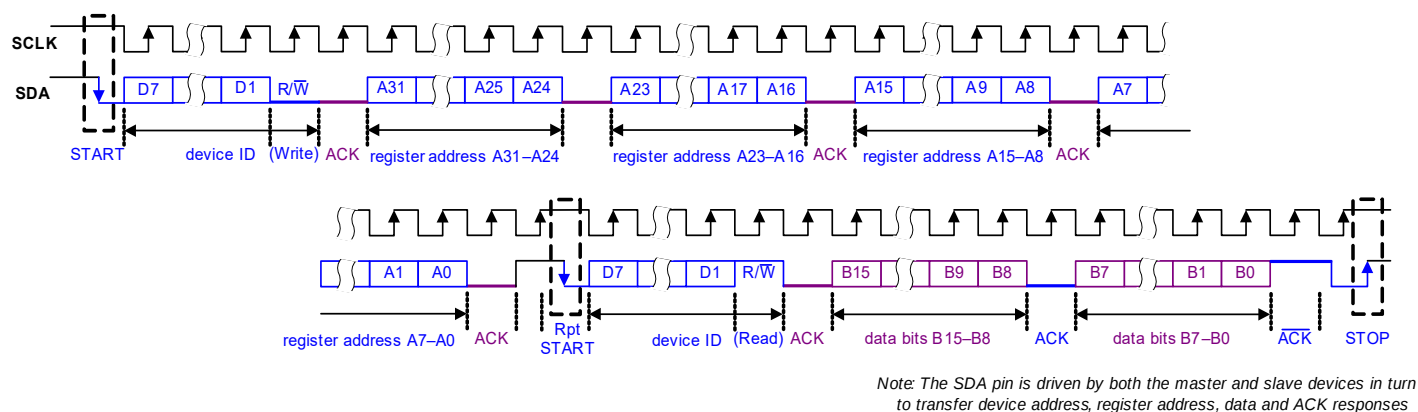
Continuous (multiple) read and write modes allow register operations to be scheduled faster than is possible with single register operations. In these modes, the CS47L35 automatically increments the register address after each data word. Successive data words can be input/output every 2 (or 4) data bytes, depending on the applicable register address space.

The I<sup>2</sup>C protocol for a single, 16-bit register write operation is shown in Fig. 4-68.



**Figure 4-68. Control Interface I<sup>2</sup>C Register Write (16-Bit Data Words)**

The I<sup>2</sup>C protocol for a single, 16-bit register read operation is shown in Fig. 4-69.



**Figure 4-69. Control Interface I<sup>2</sup>C Register Read (16-Bit Data Words)**

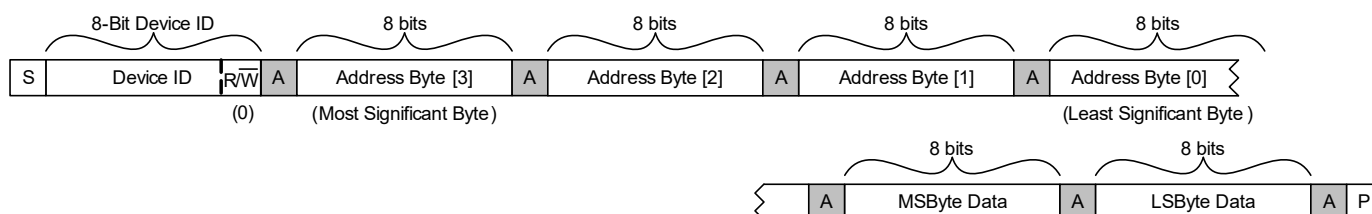
The control interface also supports other register operations; the interface protocol for these operations is shown in Fig. 4-70 through Fig. 4-73. The terminology used in the following figures is detailed in Table 4-101.

Note that 16-bit data words are shown in these illustrations. The equivalent protocol is also applicable to 32-bit words, with 4 data bytes transmitted (or received) instead of 2.

**Table 4-101. Control Interface (I<sup>2</sup>C) Terminology**

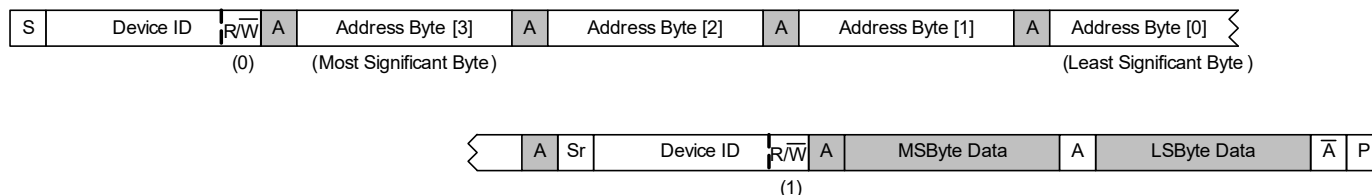
| Terminology   | Description                           |
|---------------|---------------------------------------|
| S             | Start condition                       |
| Sr            | Repeated start                        |
| A             | Acknowledge (SDA low)                 |
| $\bar{A}$     | Not acknowledge (SDA high)            |
| P             | Stop condition                        |
| R/ $\bar{W}$  | Read/not write<br>0 = Write; 1 = Read |
| [White field] | Data flow from bus master to CS47L35  |
| [Gray field]  | Data flow from CS47L35 to bus master  |

Fig. 4-70 shows a single register write to a specified address.



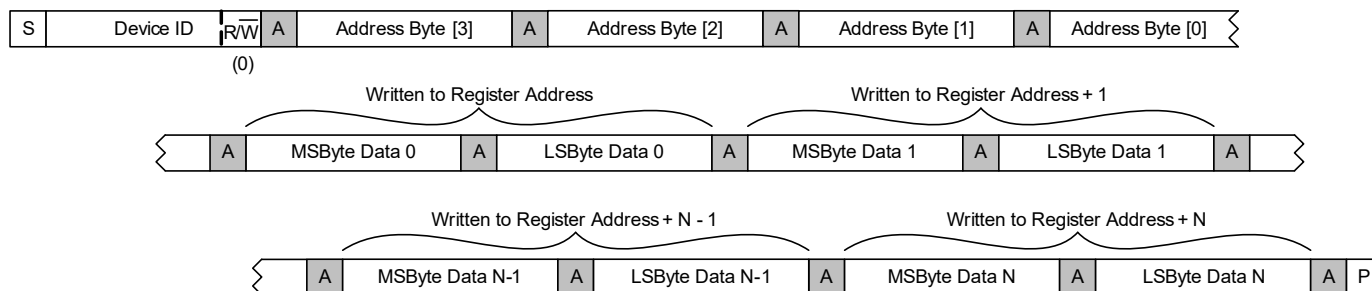
**Figure 4-70. Single-Register Write to Specified Address**

Fig. 4-71 shows a single register read from a specified address.



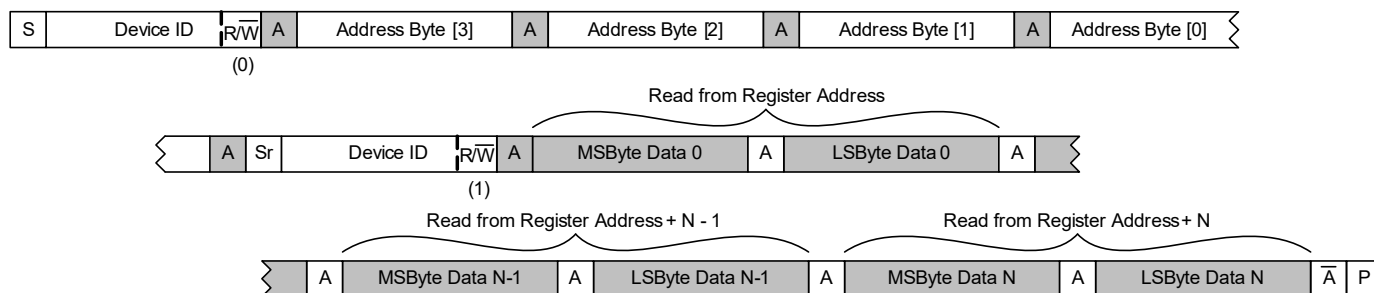
**Figure 4-71. Single-Register Read from Specified Address**

Fig. 4-72 shows a multiple register write to a specified address.



**Figure 4-72. Multiple-Register Write to Specified Address**

Fig. 4-73 shows a multiple register read from a specified address.



**Figure 4-73. Multiple-Register Read from Specified Address**

## 4.18 Control-Write Sequencer

The control-write sequencer is a programmable unit that forms part of the CS47L35 control interface logic. It provides the ability to perform a sequence of register-write operations with the minimum of demands on the host processor—the sequence may be initiated by a single operation from the host processor and then left to execute independently.

Default sequences for pop-suppressed start-up and shutdown of each headphone/earpiece output driver are provided (these are scheduled automatically when the respective output paths are enabled or disabled). Other control sequences can be programmed, and may be associated with sample-rate detection, DRC, MICDET clamp, or event-logger status; these sequences are automatically scheduled whenever a corresponding event is detected.

When a sequence is initiated, the sequencer performs a series of predefined register writes. The start index of a control sequence within the sequencer's memory may be commanded directly by the host processor. The applicable start index for each of the sequences associated with sample-rate detection, DRC, or MICDET clamp, or event logger status is held in a user-programmed control register.

The control-write sequencer may be triggered by a number of different events. Multiple sequences are queued if necessary, and each is scheduled in turn.

The control-write sequencer can be supported with or without system clocking—there is no requirement for SYSCLK or for any other system clock to be enabled when using the control-write sequencer. The timing accuracy of the sequencer operation is improved when SYSCLK is present, but the general functionality is supported with or without SYSCLK.

### 4.18.1 Initiating a Sequence

The fields associated with running the control-write sequencer are described in [Table 4-102](#).

The CS47L35 provides 16 general-purpose trigger bits for the write sequencer to allow easy triggering of the associated control sequences. Writing 1 to the trigger bit initiates a control sequence, starting at the respective index position within the control-write sequencer memory.

The WSEQ\_TRG1\_INDEX field defines the sequencer start index corresponding to the WSEQ\_TRG1 trigger control bit. Equivalent start index fields are provided for each of the trigger control bits, as described in [Table 4-102](#). Note that a sequencer start index of 0x1FF causes the respective sequence to be aborted.

The general-purpose control sequences are undefined following power-on reset, a hardware reset, or a Sleep Mode transition. The general-purpose control sequences must be reconfigured by the host processor following any of these events. Note that all control sequences are maintained in the sequencer memory through software reset.

The write sequencer can also be commanded using control bits in register R22 (0x16). In this case, the write sequencer is enabled using the WSEQ\_ENA bit and the index location of the first command in the sequence is held in the WSEQ\_START\_INDEX field. Writing 1 to the WSEQ\_START bit commands the sequencer to execute a control sequence, starting at the specified index position. Note that, if the sequencer is already running, the WSEQ\_START command is queued and executed when the sequencer becomes available.

**Note:** The mechanism for queuing multiple sequence requests has limitations when the WSEQ\_START bit is used to trigger the write sequencer. If a sequence is initiated using the WSEQ\_START bit, no other control sequences should be triggered until the sequence completes. The WSEQ\_BUSY bit (described in [Table 4-108](#)) provides an indication of the sequencer status and can be used to confirm the sequence has completed.

Multiple control sequences triggered by any other method are queued if necessary, and scheduled in turn.

The write sequencer can be interrupted by writing 1 to the WSEQ\_ABORT bit. Note that this command only aborts a sequence that is currently running; if other sequence commands are pending and not yet started, these sequences are not aborted by writing to the WSEQ\_ABORT bit.

The write sequencer stores up to 252 register-write commands. These are defined in registers R12288 (0x3000) through R12790 (0x31F6). See [Table 4-109](#) for a description of these registers.

**Table 4-102. Write Sequencer Control—Initiating a Sequence**

| Register Address                       | Bit | Label                 | Default | Description                                                                                                                                                                                                               |
|----------------------------------------|-----|-----------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R22 (0x0016)<br>Write_Sequencer_Ctrl_0 | 11  | WSEQ_ABORT            | 0       | Writing 1 to this bit aborts the current sequence.                                                                                                                                                                        |
|                                        | 10  | WSEQ_START            | 0       | Writing 1 to this bit starts the write sequencer at the index location selected by WSEQ_START_INDEX. At the end of the sequence, this bit is reset by the write sequencer.                                                |
|                                        | 9   | WSEQ_ENA              | 0       | Write Sequencer Enable<br>0 = Disabled<br>1 = Enabled<br>Only applies to sequences triggered using the WSEQ_START bit.                                                                                                    |
|                                        | 8:0 | WSEQ_START_INDEX[8:0] | 0x000   | Sequence Start Index. Contains the index location in the sequencer memory of the first command in the selected sequence.<br>Only applies to sequences triggered using the WSEQ_START bit.<br>Valid from 0 to 251 (0x0FB). |
| R66 (0x0042)<br>Spare_Triggers         | 15  | WSEQ_TRG16            | 0       | Write Sequence Trigger 16<br>Write 1 to trigger                                                                                                                                                                           |
|                                        | 14  | WSEQ_TRG15            | 0       | Write Sequence Trigger 15<br>Write 1 to trigger                                                                                                                                                                           |
|                                        | 13  | WSEQ_TRG14            | 0       | Write Sequence Trigger 14<br>Write 1 to trigger                                                                                                                                                                           |
|                                        | 12  | WSEQ_TRG13            | 0       | Write Sequence Trigger 13<br>Write 1 to trigger                                                                                                                                                                           |
|                                        | 11  | WSEQ_TRG12            | 0       | Write Sequence Trigger 12<br>Write 1 to trigger                                                                                                                                                                           |
|                                        | 10  | WSEQ_TRG11            | 0       | Write Sequence Trigger 11<br>Write 1 to trigger                                                                                                                                                                           |
|                                        | 9   | WSEQ_TRG10            | 0       | Write Sequence Trigger 10<br>Write 1 to trigger                                                                                                                                                                           |
|                                        | 8   | WSEQ_TRG9             | 0       | Write Sequence Trigger 9<br>Write 1 to trigger                                                                                                                                                                            |
|                                        | 7   | WSEQ_TRG8             | 0       | Write Sequence Trigger 8<br>Write 1 to trigger                                                                                                                                                                            |
|                                        | 6   | WSEQ_TRG7             | 0       | Write Sequence Trigger 7<br>Write 1 to trigger                                                                                                                                                                            |
|                                        | 5   | WSEQ_TRG6             | 0       | Write Sequence Trigger 6<br>Write 1 to trigger                                                                                                                                                                            |
|                                        | 4   | WSEQ_TRG5             | 0       | Write Sequence Trigger 5<br>Write 1 to trigger                                                                                                                                                                            |
|                                        | 3   | WSEQ_TRG4             | 0       | Write Sequence Trigger 4<br>Write 1 to trigger                                                                                                                                                                            |
|                                        | 2   | WSEQ_TRG3             | 0       | Write Sequence Trigger 3<br>Write 1 to trigger                                                                                                                                                                            |
|                                        | 1   | WSEQ_TRG2             | 0       | Write Sequence Trigger 2<br>Write 1 to trigger                                                                                                                                                                            |
|                                        | 0   | WSEQ_TRG1             | 0       | Write Sequence Trigger 1<br>Write 1 to trigger                                                                                                                                                                            |

**Table 4-102. Write Sequencer Control—Initiating a Sequence (Cont.)**

| Register Address                          | Bit | Label                 | Default | Description                                                                                                                                                                                         |
|-------------------------------------------|-----|-----------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R75 (0x004B)<br>Spare_Sequence_Select_1   | 8:0 | WSEQ_TRG1_INDEX[8:0]  | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG1 trigger. Valid from 0 to 251 (0x0FB).  |
| R76 (0x004C)<br>Spare_Sequence_Select_2   | 8:0 | WSEQ_TRG2_INDEX[8:0]  | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG2 trigger. Valid from 0 to 251 (0x0FB).  |
| R77 (0x004D)<br>Spare_Sequence_Select_3   | 8:0 | WSEQ_TRG3_INDEX[8:0]  | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG3 trigger. Valid from 0 to 251 (0x0FB).  |
| R78 (0x004E)<br>Spare_Sequence_Select_4   | 8:0 | WSEQ_TRG4_INDEX[8:0]  | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG4 trigger. Valid from 0 to 251 (0x0FB).  |
| R79 (0x004F)<br>Spare_Sequence_Select_5   | 8:0 | WSEQ_TRG5_INDEX[8:0]  | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG5 trigger. Valid from 0 to 251 (0x0FB).  |
| R80 (0x0050)<br>Spare_Sequence_Select_6   | 8:0 | WSEQ_TRG6_INDEX[8:0]  | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG6 trigger. Valid from 0 to 251 (0x0FB).  |
| R89 (0x0059)<br>Spare_Sequence_Select_7   | 8:0 | WSEQ_TRG7_INDEX[8:0]  | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG7 trigger. Valid from 0 to 251 (0x0FB).  |
| R90 (0x005A)<br>Spare_Sequence_Select_8   | 8:0 | WSEQ_TRG8_INDEX[8:0]  | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG8 trigger. Valid from 0 to 251 (0x0FB).  |
| R91 (0x005B)<br>Spare_Sequence_Select_9   | 8:0 | WSEQ_TRG9_INDEX[8:0]  | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG9 trigger. Valid from 0 to 251 (0x0FB).  |
| R92 (0x005C)<br>Spare_Sequence_Select_10  | 8:0 | WSEQ_TRG10_INDEX[8:0] | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG10 trigger. Valid from 0 to 251 (0x0FB). |
| R93 (0x005D)<br>Spare_Sequence_Select_11  | 8:0 | WSEQ_TRG11_INDEX[8:0] | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG11 trigger. Valid from 0 to 251 (0x0FB). |
| R94 (0x005E)<br>Spare_Sequence_Select_12  | 8:0 | WSEQ_TRG12_INDEX[8:0] | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG12 trigger. Valid from 0 to 251 (0x0FB). |
| R104 (0x0068)<br>Spare_Sequence_Select_13 | 8:0 | WSEQ_TRG13_INDEX[8:0] | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG13 trigger. Valid from 0 to 251 (0x0FB). |
| R105 (0x0069)<br>Spare_Sequence_Select_14 | 8:0 | WSEQ_TRG14_INDEX[8:0] | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG14 trigger. Valid from 0 to 251 (0x0FB). |
| R106 (0x006A)<br>Spare_Sequence_Select_15 | 8:0 | WSEQ_TRG15_INDEX[8:0] | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG15 trigger. Valid from 0 to 251 (0x0FB). |
| R107 (0x006B)<br>Spare_Sequence_Select_16 | 8:0 | WSEQ_TRG16_INDEX[8:0] | 0x1FF   | Write Sequence trigger 1 start index. Contains the index location in the sequencer memory of the first command in the sequence associated with the WSEQ_TRG16 trigger. Valid from 0 to 251 (0x0FB). |

### 4.18.2 Automatic Sample-Rate Detection Sequences

The CS47L35 supports automatic sample-rate detection on the digital audio interfaces (AIF1–AIF3) when operating in AIF Slave Mode. Automatic sample-rate detection is enabled by setting RATE\_EST\_ENA—see [Table 4-93](#).

As many as four audio sample rates can be configured for automatic detection; these sample rates are selected using the `SAMPLE_RATE_DETECT_n` fields. If a selected audio sample rate is detected, the control-write sequencer is triggered. The applicable start index location within the sequencer memory is separately configurable for each detected sample rate.

The `WSEQ_SAMPLE_RATE_DETECT_A_INDEX` field defines the sequencer start index corresponding to the `SAMPLE_RATE_DETECT_A` sample rate. Equivalent start index fields are defined for the other sample rates, as described in [Table 4-103](#).

Note that a sequencer start index of `0x1FF` causes the respective sequence to be aborted.

The automatic sample-rate detection control sequences are undefined following power-on reset, a hardware reset, or a Sleep Mode transition. The automatic sample-rate detection control sequences must be reconfigured by the host processor following any of these events. Note that all control sequences are maintained in the sequencer memory through software reset.

See [Section 4.16](#) for further details of the automatic sample-rate detection function.

**Table 4-103. Write Sequence Control—Automatic Sample-Rate Detection**

| Register Address                               | Bit | Label                                | Default | Description                                                                                                                                                                                                 |
|------------------------------------------------|-----|--------------------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R97 (0x0061)<br>Sample_Rate_Sequence_Select_1  | 8:0 | WSEQ_SAMPLE_RATE_DETECT_A_INDEX[8:0] | 0x1FF   | Sample Rate A Write Sequence start index. Contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate A detection.<br>Valid from 0 to 251 (0x0FB). |
| R98 (0x0062)<br>Sample_Rate_Sequence_Select_2  | 8:0 | WSEQ_SAMPLE_RATE_DETECT_B_INDEX[8:0] | 0x1FF   | Sample Rate B Write Sequence start index. Contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate B detection.<br>Valid from 0 to 251 (0x0FB). |
| R99 (0x0063)<br>Sample_Rate_Sequence_Select_3  | 8:0 | WSEQ_SAMPLE_RATE_DETECT_C_INDEX[8:0] | 0x1FF   | Sample Rate C Write Sequence start index. Contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate C detection.<br>Valid from 0 to 251 (0x0FB). |
| R100 (0x0064)<br>Sample_Rate_Sequence_Select_4 | 8:0 | WSEQ_SAMPLE_RATE_DETECT_D_INDEX[8:0] | 0x1FF   | Sample Rate D Write Sequence start index. Contains the index location in the sequencer memory of the first command in the sequence associated with Sample Rate D detection.<br>Valid from 0 to 251 (0x0FB). |

### 4.18.3 DRC Signal-Detect Sequences

The DRC function within the CS47L35 digital core provides a configurable signal-detect function. This allows the signal level at the DRC input to be monitored and used to trigger other events.

The DRC signal-detect functions are enabled and configured using the fields described in [Table 4-13](#) and [Table 4-14](#) for DRC1 and DRC2 respectively.

A control-write sequence can be associated with a rising edge and/or a falling edge of the DRC1 signal-detect output. This is enabled by setting `DRC1_WSEQ_SIG_DET_ENA`, as described in [Table 4-13](#).

Note that signal detection is supported on DRC1 and DRC2, but the triggering of the control-write sequencer is available on DRC1 only.

When the DRC signal-detect sequence is enabled, the control-write sequencer is triggered whenever the DRC1 signal-detect output transitions (high or low). The applicable start index location within the sequencer memory is separately configurable for each logic condition.

The `WSEQ_DRC1_SIG_DET_RISE_SEQ_INDEX` field defines the sequencer start index corresponding to a DRC1 signal-detect rising edge event, as described in [Table 4-104](#). The `WSEQ_DRC1_SIG_DET_FALL_SEQ_INDEX` field defines the sequencer start index corresponding to a DRC1 signal-detect falling edge event.

Note that a sequencer start index of `0x1FF` causes the respective sequence to be aborted.

The DRC signal-detect sequences cannot be independently enabled for rising and falling edges. Instead, a start index of `0x1FF` can be used to disable the sequence for either edge, if required.

The DRC signal-detect control sequences are undefined following power-on reset, a hardware reset, or a Sleep Mode transition. The DRC signal-detect control sequences must be reconfigured by the host processor following any of these events. Note that all control sequences are maintained in the sequencer memory through software reset.

See [Section 4.3.5](#) for further details of the DRC function.

**Table 4-104. Write Sequencer Control—DRC Signal-Detect**

| Register Address                            | Bit | Label                             | Default | Description                                                                                                                                                                                                                               |
|---------------------------------------------|-----|-----------------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R110 (0x006E)<br>Trigger_Sequence_Select_32 | 8:0 | WSEQ_DRC1_SIG_DET_RISE_INDEX[8:0] | 0x1FF   | DRC1 Signal-Detect (Rising) Write Sequence start index. Contains the index location in the sequencer memory of the first command in the sequence associated with DRC1 Signal-Detect (Rising) detection.<br>Valid from 0 to 251 (0x0FB).   |
| R111 (0x006F)<br>Trigger_Sequence_Select_33 | 8:0 | WSEQ_DRC1_SIG_DET_FALL_INDEX[8:0] | 0x1FF   | DRC1 Signal-Detect (Falling) Write Sequence start index. Contains the index location in the sequencer memory of the first command in the sequence associated with DRC1 Signal-Detect (Falling) detection.<br>Valid from 0 to 251 (0x0FB). |

#### 4.18.4 MICDET Clamp Sequences

The CS47L35 supports external accessory detection functions, including the MICDET clamp circuit. The MICDET clamp status can be used to trigger the control-write sequencer. The MICDET clamp is controlled by the JD1 and/or JD2 signals, as described in [Table 4-75](#).

A control-write sequence can be associated with a rising edge and/or a falling edge of the MICDET clamp status. This is configured using the fields described in [Table 4-75](#).

If one of the selected logic conditions is detected, the control-write sequencer is triggered. The applicable start index location within the sequencer memory is separately configurable for the rising and falling edge conditions.

The WSEQ\_MICD\_CLAMP\_RISE\_INDEX field defines the sequencer start index corresponding to a MICDET clamp rising edge (clamp active) event, as described in [Table 4-105](#). The WSEQ\_MICD\_CLAMP\_FALL\_INDEX field defines the sequencer start index corresponding to a MICDET clamp falling edge event.

Note that a sequencer start index of 0x1FF causes the respective sequence to be aborted.

The MICDET clamp control sequences are undefined following power-on reset, a hardware reset, or a Sleep Mode transition. The MICDET clamp control sequences must be reconfigured by the host processor following any of these events. Note that all control sequences are maintained in the sequencer memory through software reset.

See [Section 4.12](#) for further details of the MICDET clamp status signals.

**Table 4-105. Write Sequencer Control—MICDET Clamp**

| Register Address                                      | Bit | Label                           | Default | Description                                                                                                                                                                                                                   |
|-------------------------------------------------------|-----|---------------------------------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R102 (0x0066)<br>Always_On_Triggers_Sequence_Select_1 | 8:0 | WSEQ_MICD_CLAMP_RISE_INDEX[8:0] | 0x1FF   | MICDET Clamp (Rising) Write Sequence start index. Contains the index location in the sequencer memory of the first command in the sequence associated with MICDET clamp (Rising) detection.<br>Valid from 0 to 251 (0x0FB).   |
| R103 (0x0067)<br>Always_On_Triggers_Sequence_Select_2 | 8:0 | WSEQ_MICD_CLAMP_FALL_INDEX[8:0] | 0x1FF   | MICDET Clamp (Falling) Write Sequence start index. Contains the index location in the sequencer memory of the first command in the sequence associated with MICDET clamp (Falling) detection.<br>Valid from 0 to 251 (0x0FB). |

#### 4.18.5 Event Logger Sequences

The CS47L35 provides four event log functions, for monitoring and recording internal or external signals. The logged events are held in a FIFO buffer, from which the application software can read details of the detected logic transitions.

The control-write sequencer is automatically triggered whenever the NOT\_EMPTY status of the event log buffer is asserted. A different control sequence may be configured for each of the event loggers.

The WSEQ\_EVENTLOG<sub>n</sub>\_INDEX field defines the sequencer start index corresponding to respective event logger (where *n* is 1 to 4), as described in [Table 4-106](#).

Note that a sequencer start index of 0x1FF causes the respective sequence to be aborted.

The event logger control sequences are undefined following power-on reset, a hardware reset, or a Sleep Mode transition. The event logger control sequences must be reconfigured by the host processor following any of these events. Note that all control sequences are maintained in the sequencer memory through software reset.

See [Section 4.5.2](#) for further details of the event loggers.

**Table 4-106. Write Sequencer Control—Event Loggers**

| Register Address                                    | Bit | Label                             | Default | Description                                                                                                                                                                                                            |
|-----------------------------------------------------|-----|-----------------------------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R120 (0x0078)<br>Eventlog_<br>Sequence_<br>Select_1 | 8:0 | WSEQ_<br>EVENTLOG1_<br>INDEX[8:0] | 0x1FF   | Event Log 1 Write Sequence start index. Contains the index location in the sequencer memory of the first command in the sequence associated with Event Log 1 FIFO Not-Empty detection.<br>Valid from 0 to 251 (0x0FB). |
| R121 (0x0079)<br>Eventlog_<br>Sequence_<br>Select_2 | 8:0 | WSEQ_<br>EVENTLOG2_<br>INDEX[8:0] | 0x1FF   | Event Log 2 Write Sequence start index. Contains the index location in the sequencer memory of the first command in the sequence associated with Event Log 2 FIFO Not-Empty detection.<br>Valid from 0 to 251 (0x0FB). |
| R122 (0x007A)<br>Eventlog_<br>Sequence_<br>Select_3 | 8:0 | WSEQ_<br>EVENTLOG3_<br>INDEX[8:0] | 0x1FF   | Event Log 3 Write Sequence start index. Contains the index location in the sequencer memory of the first command in the sequence associated with Event Log 3 FIFO Not-Empty detection.<br>Valid from 0 to 251 (0x0FB). |
| R123 (0x007B)<br>Eventlog_<br>Sequence_<br>Select_4 | 8:0 | WSEQ_<br>EVENTLOG4_<br>INDEX[8:0] | 0x1FF   | Event Log 4 Write Sequence start index. Contains the index location in the sequencer memory of the first command in the sequence associated with Event Log 4 FIFO Not-Empty detection.<br>Valid from 0 to 251 (0x0FB). |

### 4.18.6 Boot Sequence

The CS47L35 executes a boot sequence following power-on reset, hardware reset, software reset, or wake-up from Sleep Mode. The boot sequence configures the CS47L35 with factory-set trim (calibration) data. See [Section 4.22](#) and [Section 4.23](#) for further details.

The start index location of the boot sequence is 224 (0x0E0). See [Table 4-111](#) for details of the write sequencer memory allocation.

The boot sequence can be commanded at any time by writing 1 to the WSEQ\_BOOT\_START bit.

**Table 4-107. Write Sequencer Control—Boot Sequence**

| Register Address                           | Bit | Label               | Default | Description                                                                                                                                               |
|--------------------------------------------|-----|---------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| R24 (0x0018)<br>Write_Sequencer_<br>Ctrl_2 | 1   | WSEQ_BOOT_<br>START | 0       | Writing 1 to this bit starts the write sequencer at the index location configured for the Boot Sequence.<br>The Boot Sequence start index is 224 (0x0E0). |

### 4.18.7 Sequencer Status Indication

The status of the write sequencer can be read using WSEQ\_BUSY and WSEQ\_CURRENT\_INDEX, as described in [Table 4-108](#). When the WSEQ\_BUSY bit is asserted, this indicates that the write sequencer is busy.

The index address of the most recent write sequencer command can be read from the WSEQ\_CURRENT\_INDEX field. This can be used to provide a precise indication of the write sequencer progress.

**Table 4-108. Write Sequencer Control—Status Indication**

| Register Address                           | Bit | Label                                      | Default | Description                                                                                                                                                                |
|--------------------------------------------|-----|--------------------------------------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R23 (0x0017)<br>Write_Sequencer_<br>Ctrl_1 | 9   | WSEQ_BUSY<br>(read only)                   | 0       | Sequencer Busy flag (Read Only).<br>0 = Sequencer idle<br>1 = Sequencer busy                                                                                               |
|                                            | 8:0 | WSEQ_CURRENT_<br>INDEX[8:0]<br>(read only) | 0x000   | Sequence Current Index. This indicates the memory location of the most recently accessed command in the write sequencer memory.<br>Coding is the same as WSEQ_START_INDEX. |

## 4.18.8 Programming a Sequence

A control-write sequence comprises a series of write operations to data bits within the control register map. Standard write operations are defined by 5 fields, contained within a single 32-bit register. An extended instruction set is also defined; the associated actions makes use of alternate definitions of the 32-bit registers.

The sequencer instruction fields are replicated 252 times, defining each of the sequencer's 252 possible index addresses. Many sequences can be stored in the sequencer memory at the same time, with each assigned a unique range of index addresses. The WSEQ\_DELAY $n$  field is used to identify the end-of-sequence position, as described below.

The general definition of the sequencer instruction fields is described as follows, where  $n$  denotes the sequencer index address (valid from 0 to 251):

- WSEQ\_DATA\_WIDTH $n$  is a 3-bit field that identifies the width of the data block to be written. Note that the maximum value of this field selects a width of 8 bits; writes to fields that are larger than 8 bits wide must be performed using two separate operations of the write sequencer.
- WSEQ\_ADDR $n$  is a 12-bit field containing the register address in which the data should be written. The applicable register address is referenced to the base address currently configured for the sequencer—it is calculated as: (base address \* 512) + WSEQ\_ADDR $n$ . Note that the base address is configured using the sequencer's extended instruction set.
- WSEQ\_DELAY $n$  is a 4-bit field that controls the waiting time between the current step and the next step in the sequence (i.e., the delay occurs after the write in which it was called). The total delay time per step (including execution) is defined below, giving a useful range of execution/delay times from 3.3  $\mu$ s up to 1 s per step.
  - If WSEQ\_DELAY $n$  = 0x0 or 0xF, the step execution time is 3.3  $\mu$ s
  - For all other values, the step execution time is 61.44  $\mu$ s x ((2 WSEQ\_DELAY) – 1)
  - Setting this field to 0xF identifies the step as the last in the sequence
- WSEQ\_DATA\_START $n$  is a 4-bit field that identifies the LSB position within the selected control register to which the data should be written. For example, setting WSEQ\_DATA\_START $n$  = 0100 selects bit [4] as the LSB position of the data to be written.
- WSEQ\_DATA $n$  is an 8-bit field that contains the data to be written to the selected control register. The WSEQ\_DATA\_WIDTH $n$  field determines how many of these bits are written to the selected control register; the most significant bits (above the number indicated by WSEQ\_DATA\_WIDTH $n$ ) are ignored.

The extended instruction set for the write sequencer is accessed by setting WSEQ\_MODE $n$  (bit [28]) in the respective sequencer definition register. The extended instruction set comprises the following functions:

- If bits [31:24] = 0x11, the register base address is set equal to the value contained in bits [23:0].
- If bits [31:16] = 0x12FF, the sequencer performs an unconditional jump to the index location defined in bits [15:0]. The index location is valid in the range 0 to 251 (0x0FB).
- All other settings within the extended instruction set are reserved.

The control field definitions for Step 0 are described in [Table 4-109](#). The equivalent definitions also apply to Step 1 through Step 251, in the subsequent register address locations.

**Table 4-109. Write Sequencer Control—Programming a Sequence**

| Register Address                       | Bit   | Label                     | Default | Description                                                                                                                                                                                                                                                                     |
|----------------------------------------|-------|---------------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R12288 (0x3000)<br>WSEQ_<br>Sequence_1 | 31:29 | WSEQ_DATA_<br>WIDTH0[2:0] | 000     | Width of the data block written in this sequence step.<br>000 = 1 bit                      011 = 4 bits                      110 = 7 bits<br>001 = 2 bits                      100 = 5 bits                      111 = 8 bits<br>010 = 3 bits                      101 = 6 bits |
|                                        | 28    | WSEQ_MODE0                | 0       | Extended Sequencer Instruction select<br>0 = Basic instruction set<br>1 = Extended instruction set                                                                                                                                                                              |
|                                        | 27:16 | WSEQ_ADDR0[11:0]          | 0x000   | Control Register Address to be written to in this sequence step.<br>The register address is calculated as: (Base Address * 512) + WSEQ_ADDRn.<br>Base Address is 0x00_0000 by default, and is configured using the sequencer's extended instruction set.                        |
|                                        | 15:12 | WSEQ_DELAY0[3:0]          | 0000    | Time delay after executing this step.<br>0x0 = 3.3 $\mu$ s<br>0x1 to 0xE = 61.44 $\mu$ s x ((2 <sup>WSEQ_DELAY</sup> )–1)<br>0xF = End of sequence marker                                                                                                                       |
|                                        | 11:8  | WSEQ_DATA_<br>START0[3:0] | 0000    | Bit position of the LSB of the data block written in this sequence step.<br>0000 = Bit 0<br>...<br>1111 = Bit 15                                                                                                                                                                |
|                                        | 7:0   | WSEQ_DATA0[7:0]           | 0x00    | Data to be written in this sequence step. When the data width is less than 8 bits, one or more of the MSBs of WSEQ_DATA <sub>n</sub> are ignored. It is recommended that unused bits be cleared.                                                                                |

### 4.18.9 Sequencer Memory Definition

The write sequencer memory defines up to 252 write operations; these are indexed as 0 to 251 in the sequencer memory map.

The write sequencer memory reverts to its default contents following power-on reset, a hardware reset, or a Sleep Mode transition. In these cases, the sequence memory contains the boot sequence and the OUT1–OUT4 signal path enable/disable sequences; the remainder of the sequence memory is undefined.

User-defined sequences can be programmed after power-up. The user-defined control sequences must be reconfigured by the host processor following power-on reset, a hardware reset, or a Sleep Mode transition. Note that all control sequences are maintained in the sequencer memory through software reset. See [Section 5.2](#) for a summary of the CS47L35 memory reset conditions.

The default control sequences can be overwritten in the sequencer memory, if required. Note that the headphone and earpiece output path enable bits (HP<sub>n</sub>x\_ENA, SPKOUT<sub>x</sub>\_ENA) always trigger the write sequencer (at the predetermined start index addresses).

Writing 1 to the WSEQ\_LOAD\_MEM bit clears the sequencer memory to the power-on reset state.

**Table 4-110. Write Sequencer Control—Load Memory Control**

| Register Address                       | Bit | Label             | Default | Description                                                                    |
|----------------------------------------|-----|-------------------|---------|--------------------------------------------------------------------------------|
| R24 (0x0018)<br>Write_Sequencer_Ctrl_2 | 0   | WSEQ_LOAD_<br>MEM | 0       | Writing 1 to this bit resets the sequencer memory to the power-on reset state. |

The sequencer memory is summarized in [Table 4-111](#). User-defined sequences should be assigned space within the allocated portion (user space) of the write sequencer memory.

The start index for the user-defined sequences is configured using the fields described in [Table 4-102](#) through [Table 4-106](#).

**Table 4-111. Write Sequencer Memory Allocation**

| Description       | Sequence Index Range |
|-------------------|----------------------|
| Default Sequences | 0 to 114             |
| User Space        | 115 to 223           |
| Boot Sequence     | 224 to 251           |

## 4.19 Charge Pumps, Regulators, and Voltage Reference

The CS47L35 incorporates two charge-pump circuits and an LDO-regulator circuit to generate supply rails for internal functions and to support external microphone requirements. The CS47L35 also provides two MICBIAS generators (with four switchable outputs), which provide low noise reference voltages suitable for biasing ECM-type microphones or powering digital microphones.

Refer to [Section 5.1](#) for recommended external components.

The CPVDD1 domain (1.8 V) powers the Charge Pump 1 and Charge Pump 2 circuits. The CPVDD2 power domain (1.2 V) is an additional supply used by Charge Pump 1 only.

### 4.19.1 Charge Pump 1

Charge Pump 1 (CP1) is used to generate the positive and negative supply rails for the analog output drivers. CP1 is enabled automatically by the CS47L35 when required by the output drivers.

The Charge Pump 1 circuit is shown in [Fig. 4-74](#).

### 4.19.2 Charge Pump 2 and LDO2 Regulator

Charge Pump 2 (CP2) powers LDO2, which provides the supply rail for analog input circuits and for the MICBIAS generators. CP2 and LDO2 are enabled by setting CP2\_ENA.

The 32-kHz clock must be configured and enabled when using CP2. See [Section 4.16](#) for details of the system clocks.

When CP2 and LDO2 are enabled, the MICVDD voltage is selected using the LDO2\_VSEL field. Note that, when one or more of the MICBIAS generators is operating in normal (regulator) mode, the MICVDD voltage must be at least 200 mV greater than the highest selected MICBIASn output voltages.

When CP2 and LDO2 are enabled, an internal bypass path may be selected, connecting the MICVDD pin directly to the CPVDD1 supply. This path is controlled using the CP2\_BYPASS bit. Note that the bypass path is only supported when CP2 is enabled.

When CP2 is disabled, the CP2VOUT pin can be configured to be floating or to be actively discharged. This is selected using the CP2\_DISCH bit.

When LDO2 is disabled, the MICVDD pin can be configured to be floating or to be actively discharged. This is selected using the LDO2\_DISCH bit.

The MICVDD pin is connected to the output of LDO2. Note that the MICVDD does not support direct connection to an external supply; MICVDD is always powered internally to the CS47L35.

The Charge Pump 2 and LDO2 Regulator circuits are shown in [Fig. 4-74](#). The associated control bits are described in [Table 4-112](#).

Note that decoupling capacitors and flyback capacitors are required for these circuits. Refer to [Section 5.1](#) for recommended external components.

### 4.19.3 Microphone Bias (MICBIAS) Control

There are two MICBIAS generators, which provide low-noise reference voltages suitable for biasing ECM-type microphones or powering digital microphones. Refer to [Section 5.1.3](#) for recommended external components.

The MICBIAS generators are powered from MICVDD, which is generated by an internal charge pump and LDO, as shown in [Fig. 4-74](#).

Switchable outputs from the MICBIAS generators allow four separate reference/supply outputs to be independently controlled. The MICBIAS regulators are enabled using the MICB1\_ENA and MICB2\_ENA bits. The MICBIAS output switches are enabled using MICB1A\_ENA, MICB1B\_ENA, MICB2A\_ENA, and MICB2B\_ENA.

Note that, to enable any of the MICBIAS<sub>n</sub>x outputs, both the output switch and the respective regulator must be enabled.

When a MICBIAS output is disabled, it can be configured to be floating or to be actively discharged. This is configured using the MICB<sub>n</sub>\_DISCH bits (for the MICBIAS regulators), and the MICB<sub>n</sub>x\_DISCH bits (for the switched outputs). Each discharge path is only effective when the respective regulator, or switched output, is disabled.

The MICBIAS generators can each operate in Regulator Mode or in Bypass Mode. The applicable mode is selected using the MICB<sub>n</sub>\_BYPASS bits.

In Regulator Mode (MICB<sub>n</sub>\_BYPASS = 0), the output voltage is selected using the MICB<sub>n</sub>\_LVL fields. In this mode, MICVDD must be at least 200mV greater than the required MICBIAS output voltages. The MICBIAS outputs are powered from the MICVDD pin and use the internal band-gap circuit as a reference.

In Regulator Mode, the MICBIAS regulators are designed to operate without external decoupling capacitors. The regulators can be configured to support a capacitive load if required, using the MICB<sub>n</sub>\_EXT\_CAP bits. (This may be appropriate for a DMIC supply.) It is important that the external capacitance is compatible with the applicable MICB<sub>n</sub>\_EXT\_CAP setting. The compatible load conditions are detailed in [Table 3-11](#).

In Bypass Mode (MICB<sub>n</sub>\_BYPASS = 1), the respective outputs (MICBIAS<sub>n</sub>x), when enabled, are connected directly to MICVDD. This enables a low power operating state. Note that the MICB<sub>n</sub>\_EXT\_CAP settings are not applicable in Bypass Mode—there are no restrictions on the external MICBIAS capacitance in Bypass Mode.

The MICBIAS generators incorporate a pop-free control circuit to ensure smooth transitions when the MICBIAS outputs are enabled or disabled in Bypass Mode; this feature is enabled using the MICB<sub>n</sub>\_RATE bits.

The MICBIAS generators are shown in [Fig. 4-74](#). The MICBIAS control fields are described in [Table 4-112](#).

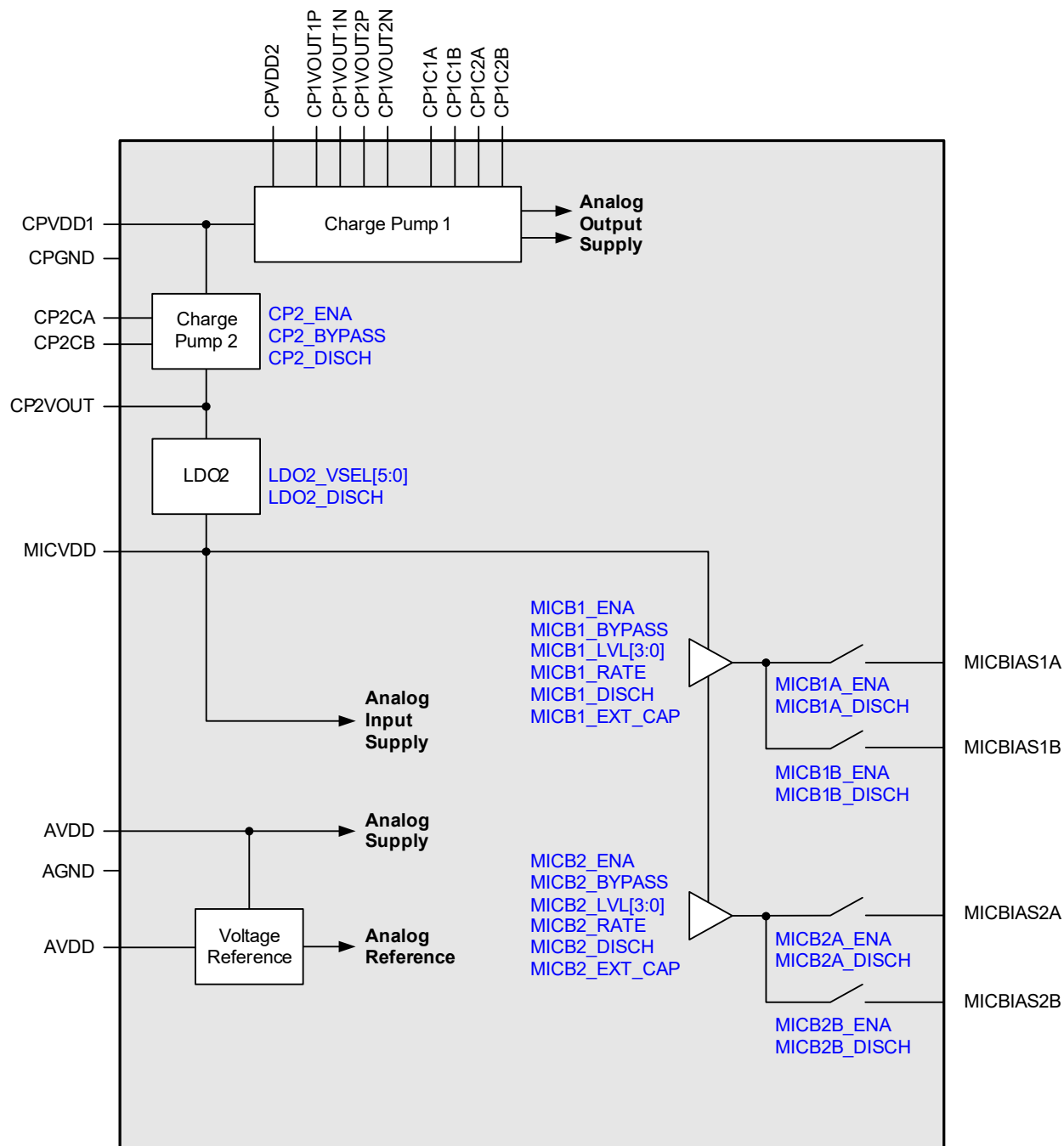
The maximum output current for each MICBIAS regulator is noted in [Table 3-11](#). This limit must be observed for each pair of MICBIAS<sub>n</sub>x outputs, especially if more than one microphone is connected to a single regulator. Note that the maximum output current differs between Regulator Mode and Bypass Mode.

#### 4.19.4 Voltage-Reference Circuit

The CS47L35 incorporates a voltage-reference circuit, powered by AVDD. This circuit ensures the accuracy of the LDO-regulator and MICBIAS voltage settings.

#### 4.19.5 Block Diagram and Control Registers

The charge-pump and regulator circuits are shown in [Fig. 4-74](#). Note that decoupling capacitors and flyback capacitors are required for these circuits. Refer to [Section 5.1](#) for recommended external components.



**Figure 4-74. Charge Pumps and Regulators**

The charge-pump and regulator control registers are described in [Table 4-112](#).

**Table 4-112. Charge-Pump and LDO Control Registers**

| Register Address                   | Bit  | Label          | Default | Description                                                                                                                                                                                                                                                                                                                                                                                |
|------------------------------------|------|----------------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R512 (0x0200)<br>Mic_Charge_Pump_1 | 2    | CP2_DISCH      | 1       | Charge Pump 2 Discharge<br>0 = CP2VOUT floating when disabled<br>1 = CP2VOUT discharged when disabled                                                                                                                                                                                                                                                                                      |
|                                    | 1    | CP2_BYPASS     | 1       | Charge Pump 2 and LDO2 Bypass Mode<br>0 = Normal<br>1 = Bypass Mode<br>In Bypass Mode, CPVDD1 is connected directly to MICVDD.<br>Note that CP2_ENA must also be set.                                                                                                                                                                                                                      |
|                                    | 0    | CP2_ENA        | 0       | Charge Pump 2 and LDO2 Control<br>(Provides analog input and MICVDD supplies)<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                               |
| R531 (0x0213)<br>LDO2_Control_1    | 10:5 | LDO2_VSEL[5:0] | 0x1F    | LDO2 Output Voltage Select <sup>1</sup><br>0x00 = 0.900 V                      0x13 = 1.375 V                      ... (100-mV steps)<br>0x01 = 0.925 V                      0x14 = 1.400 V                      0x26 = 3.200 V<br>0x02 = 0.950 V                      0x15 = 1.500 V                      0x27 to 0x3F = 3.300 V<br>... (25-mV steps)                      0x16 = 1.600 V |
|                                    | 2    | LDO2_DISCH     | 1       | LDO2 Discharge<br>0 = MICVDD floating when disabled<br>1 = MICVDD discharged when disabled                                                                                                                                                                                                                                                                                                 |
| R536 (0x0218)<br>Mic_Bias_Ctrl_1   | 15   | MICB1_EXT_CAP  | 0       | Microphone Bias 1 External Capacitor (when MICB1_BYPASS = 0).<br>Configures the MICBIAS1 regulator according to the specified capacitance connected to the MICBIAS1x outputs.<br>0 = No external capacitor<br>1 = External capacitor connected                                                                                                                                             |
|                                    | 8:5  | MICB1_LVL[3:0] | 0x7     | Microphone Bias 1 Voltage Control (when MICB1_BYPASS = 0)<br>0x0 = 1.5 V                      ... (0.1-V steps)                      0xD to 0xF = 2.8 V<br>0x1 = 1.6 V                      0xC = 2.7 V                                                                                                                                                                                    |
|                                    | 3    | MICB1_RATE     | 0       | Microphone Bias 1 Rate (Bypass Mode)<br>0 = Fast start-up/shutdown<br>1 = Pop-free start-up/shutdown                                                                                                                                                                                                                                                                                       |
|                                    | 2    | MICB1_DISCH    | 1       | Microphone Bias 1 Discharge<br>0 = MICBIAS1 floating when disabled<br>1 = MICBIAS1 discharged when disabled                                                                                                                                                                                                                                                                                |
|                                    | 1    | MICB1_BYPASS   | 1       | Microphone Bias 1 Mode<br>0 = Regulator Mode<br>1 = Bypass Mode                                                                                                                                                                                                                                                                                                                            |
|                                    | 0    | MICB1_ENA      | 0       | Microphone Bias 1 Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                                                                                                                                                                    |

**Table 4-112. Charge-Pump and LDO Control Registers (Cont.)**

| Register Address                 | Bit | Label          | Default | Description                                                                                                                                                                                                                                 |
|----------------------------------|-----|----------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R537 (0x0219)<br>Mic_Bias_Ctrl_2 | 15  | MICB2_EXT_CAP  | 0       | Microphone Bias 2 External Capacitor (when MICB2_BYPASS = 0). Configures the MICBIAS2 regulator according to the specified capacitance connected to the MICBIAS2x outputs.<br>0 = No external capacitor<br>1 = External capacitor connected |
|                                  | 8:5 | MICB2_LVL[3:0] | 0x7     | Microphone Bias 2 Voltage Control (when MICB2_BYPASS = 0)<br>0x0 = 1.5 V ... (0.1-V steps) 0xD to 0xF = 2.8 V<br>0x1 = 1.6 V 0xC = 2.7 V                                                                                                    |
|                                  | 3   | MICB2_RATE     | 0       | Microphone Bias 2 Rate (Bypass Mode)<br>0 = Fast start-up/shutdown<br>1 = Pop-free start-up/shutdown                                                                                                                                        |
|                                  | 2   | MICB2_DISCH    | 1       | Microphone Bias 2 Discharge<br>0 = MICBIAS2 floating when disabled<br>1 = MICBIAS2 discharged when disabled                                                                                                                                 |
|                                  | 1   | MICB2_BYPASS   | 1       | Microphone Bias 2 Mode<br>0 = Regulator Mode<br>1 = Bypass Mode                                                                                                                                                                             |
|                                  | 0   | MICB2_ENA      | 0       | Microphone Bias 2 Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                     |
| R540 (0x021C)<br>Mic_Bias_Ctrl_5 | 5   | MICB1B_DISCH   | 0       | Microphone Bias 1B Discharge<br>0 = MICBIAS1B floating when disabled<br>1 = MICBIAS1B discharged when disabled                                                                                                                              |
|                                  | 4   | MICB1B_ENA     | 0       | Microphone Bias 1B Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                    |
|                                  | 1   | MICB1A_DISCH   | 0       | Microphone Bias 1A Discharge<br>0 = MICBIAS1A floating when disabled<br>1 = MICBIAS1A discharged when disabled                                                                                                                              |
|                                  | 0   | MICB1A_ENA     | 0       | Microphone Bias 1A Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                    |
| R542 (0x021E)<br>Mic_Bias_Ctrl_6 | 5   | MICB2B_DISCH   | 0       | Microphone Bias 2B Discharge<br>0 = MICBIAS2B floating when disabled<br>1 = MICBIAS2B discharged when disabled                                                                                                                              |
|                                  | 4   | MICB2B_ENA     | 0       | Microphone Bias 2B Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                    |
|                                  | 1   | MICB2A_DISCH   | 0       | Microphone Bias 2A Discharge<br>0 = MICBIAS2A floating when disabled<br>1 = MICBIAS2A discharged when disabled                                                                                                                              |
|                                  | 0   | MICB2A_ENA     | 0       | Microphone Bias 2A Enable<br>0 = Disabled<br>1 = Enabled                                                                                                                                                                                    |

1. See Table 4-113 for LDO2 output voltage definition.

Table 4-113 lists the LDO2 voltage control settings.

**Table 4-113. LDO2 Voltage Control**

| LDO2_VSEL[5:0] | LDO Output | LDO2_VSEL[5:0] | LDO Output | LDO2_VSEL[5:0] | LDO Output |
|----------------|------------|----------------|------------|----------------|------------|
| 0x00           | 0.900 V    | 0x10           | 1.300 V    | 0x20           | 2.600 V    |
| 0x01           | 0.925 V    | 0x11           | 1.325 V    | 0x21           | 2.700 V    |
| 0x02           | 0.950 V    | 0x12           | 1.350 V    | 0x22           | 2.800 V    |
| 0x03           | 0.975 V    | 0x13           | 1.375 V    | 0x23           | 2.900 V    |
| 0x04           | 1.000 V    | 0x14           | 1.400 V    | 0x24           | 3.000 V    |
| 0x05           | 1.025 V    | 0x0E           | 1.250 V    | 0x1C           | 2.200 V    |

**Table 4-113. LDO2 Voltage Control (Cont.)**

| LDO2_VSEL[5:0] | LDO Output | LDO2_VSEL[5:0] | LDO Output | LDO2_VSEL[5:0] | LDO Output |
|----------------|------------|----------------|------------|----------------|------------|
| 0x06           | 1.050 V    | 0x0F           | 1.275 V    | 0x1D           | 2.300 V    |
| 0x07           | 1.075 V    | 0x15           | 1.500 V    | 0x1E           | 2.400V     |
| 0x08           | 1.100 V    | 0x16           | 1.600 V    | 0x1F           | 2.500 V    |
| 0x09           | 1.125 V    | 0x17           | 1.700 V    | 0x25           | 3.100 V    |
| 0x0A           | 1.150 V    | 0x18           | 1.800 V    | 0x26           | 3.200 V    |
| 0x0B           | 1.175 V    | 0x19           | 1.900 V    | 0x27           | 3.300 V    |
| 0x0C           | 1.200 V    | 0x1A           | 2.000 V    | 0x28 to 0x3F   | 3.300 V    |
| 0x0D           | 1.225 V    | 0x1B           | 2.100 V    |                |            |

## 4.20 JTAG Interface

The JTAG interface provides test and debug access to the CS47L35 DSP core. The interface comprises five pins, as detailed below.

- TCK: clock input
- TDI: data input
- TDO: data output
- TMS: mode select input
- TRST: test access port reset input (active low)

For normal operation (test and debug access disabled), the JTAG interface should be held in reset (i.e., TRST should be at Logic 0). An internal pull-down resistor holds the TRST pin low when not actively driven. External connection to DGND is recommended, if the JTAG interface function is not required.

The other JTAG input pins (TCK, TDI, TMS) should also be held at Logic 0 for normal operation. An internal pull-down resistor holds these pins low when not actively driven.

If the JTAG interface is enabled (TRST deasserted and TCK active) at the time of any reset, a software reset must be scheduled, with the TCK input stopped or TRST asserted (Logic 0), before using the JTAG interface.

It is recommended to always schedule a software reset before starting the JTAG clock or deasserting the JTAG reset. In this event, the JTAG interface should be held in its reset state until the software reset has completed, and the BOOT\_DONE\_STSx bits have been set.

See [Section 4.23](#) for further details of the CS47L35 software reset.

## 4.21 Thermal, Short-Circuit, and Timer-Controlled Protection

The CS47L35 incorporates thermal protection, short-circuit detection, and timer-controlled speaker disable functions; these are described in the following subsections.

### 4.21.1 Thermal Shutdown

The temperature sensor detects when the device temperature is within normal limits or if the device is approaching a hazardous temperature condition.

The temperature sensor is an input to the interrupt control circuit and can be used to trigger an interrupt event; see [Section 4.15](#). A two-stage indication is provided, via the SPK\_OVERHEAT\_WARN\_EINTn and SPK\_OVERHEAT\_EINTn interrupts.

If the upper temperature threshold (SPK\_OVERHEAT\_EINTn) is exceeded, the Class D speaker outputs are automatically disabled in order to protect the device. When the speaker driver shutdown is complete, a further interrupt, SPK\_SHUTDOWN\_EINTn, is asserted.

## 4.21.2 Short Circuit Protection

The short-circuit detection function for the Class D speaker outputs is triggered when the respective output drivers are enabled (see [Table 4-64](#)). If a short circuit is detected at this time, the enable does not succeed, and the respective output driver is not enabled.

The Class D speaker short-circuit detection provides inputs to the interrupt control circuit and can be used to trigger an interrupt event; see [Section 4.15](#). If the Class D speaker short-circuit condition is detected, the respective drivers are automatically disabled in order to protect the device. When the speaker driver shutdown is complete, a further interrupt, `SPK_SHUTDOWN_EINTn`, is asserted.

To enable the Class D speaker outputs following a short-circuit detection, the host processor must disable and reen able the output drivers. Note that the short-circuit status bits are always cleared when the drivers are disabled.

The short-circuit detection function for the headphone and earpiece output paths operates continuously if the respective output driver is enabled. If a short circuit is detected on the headphone or earpiece output, current limiting is applied to protect the respective output driver. Note that the driver continues to operate, but the output is current-limited.

The headphone and earpiece short-circuit detection functions provide input to the interrupt control circuit and can be used to trigger an interrupt event when a short-circuit condition is detected; see [Section 4.15](#).

## 4.21.3 Timer-Controlled Speaker Shutdown

The general-purpose timers (see [Section 4.5.3](#)) can also be used to trigger a shutdown of the Class D speaker drivers. This is configured using the `SPK_SHUTDOWN_TIMER_SEL` field, as described in [Table 4-114](#).

If one of the general-purpose timers is selected for the speaker shutdown function, and the respective timer reaches its final count value, the Class D speaker drivers are automatically disabled. When the driver shutdown is complete, an interrupt event (`SPK_SHUTDOWN_EINTn`) is signaled.

To enable the Class D speaker outputs following a timeout condition, the host processor must disable and reen able the output drivers.

**Table 4-114. Speaker Shutdown—Timer Control**

| Register Address                             | Bit | Label                                    | Default | Description                                                                                                                                                                      |
|----------------------------------------------|-----|------------------------------------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R620 (0x026D)<br><code>SPK_Watchdog_1</code> | 3:0 | <code>SPK_SHUTDOWN_TIMER_SEL[3:0]</code> | 0x0     | Speaker Shutdown Timer select. Unlisted codes are reserved<br>0x0 = Disabled<br>0x1 = Timer 1<br>0x2 = Timer 2<br>0x3 = Timer 3<br>0x4 = Timer 4<br>All other codes are reserved |

## 4.21.4 GPIO Output

The thermal status, Class D speaker short-circuit protection, and Class D speaker shutdown flags can be output directly on a GPIO pin as an external indication of the associated events. See [Section 4.14](#) to configure a GPIO pin for this function.

## 4.22 Power-On Reset (POR)

The CS47L35 remains in the reset state until `AVDD`, `DBVDD1`, and `DCVDD` are above their respective reset thresholds. Note that specified device performance is not assured outside the voltage ranges defined in [Table 3-3](#).

After the initial power-up, the POR is rescheduled following an interruption to the `DBVDD1` or `AVDD` supplies.

If the CS47L35 SLIMbus component is in its operational state, it must be reset before scheduling a POR. See [Section 4.10](#) for details of the SLIMbus reset control messages.

## 4.22.1 Boot Sequence

Following power-on reset, a boot sequence is executed. The BOOT\_DONE\_STSx bits are asserted on completion of the boot sequence, as described in [Table 4-115](#). Control-register writes should not be attempted until BOOT\_DONE\_STSx has been asserted. Note that the BOOT\_DONE\_STS1 and BOOT\_DONE\_STS2 bits provide the same information.

The BOOT\_DONE\_STSx signal is an input to the interrupt control circuit and can be used to trigger an interrupt event on completion of the boot sequence; see [Section 4.15](#). Under default register conditions, a falling edge on the  $\overline{\text{IRQ}}$  pin indicates completion of the boot sequence.

For details of the boot sequence, see [Section 4.18](#).

**Table 4-115. Device Boot-Up Status**

| Register Address                        | Bit | Label              | Default | Description                                                                                                                                                                     |
|-----------------------------------------|-----|--------------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R6272 (0x1880)<br>IRQ1_Raw_<br>Status_1 | 7   | BOOT_DONE_<br>STS1 | 0       | Boot Status<br>0 = Busy (boot sequence in progress)<br>1 = Idle (boot sequence completed)<br>Control register writes should not be attempted until Boot Sequence has completed. |
| R6528 (0x1980)<br>IRQ2_Raw_<br>Status_1 | 7   | BOOT_DONE_<br>STS2 | 0       | Boot Status<br>0 = Busy (boot sequence in progress)<br>1 = Idle (boot sequence completed)<br>Control register writes should not be attempted until Boot Sequence has completed. |

## 4.22.2 Digital I/O Status in Reset

[Table 4-116](#) describes the default status of the CS47L35 digital I/O pins on completion of power-on reset and before any register writes. The same default conditions are also applicable on completion of a hardware reset or software reset (see [Section 4.23](#)).

The same default conditions are applicable following a wake-up transition, except for the  $\overline{\text{IRQ}}$  and  $\overline{\text{RESET}}$  pins. These are always-on pins whose configuration is unchanged in Sleep Mode and during a wake-up transition.

Note that the default conditions described in [Table 4-116](#) are not valid if modified by the boot sequence or by a wake-up control sequence. See [Section 4.18](#) for details of these functions.

**Table 4-116. CS47L35 Digital I/O Status in Reset**

| Power Domain        | Pin No | Name             | Type                        | Reset Status                                          |
|---------------------|--------|------------------|-----------------------------|-------------------------------------------------------|
| MICVDD <sup>1</sup> | E3     | IN1ALN/DMICCLK1  | Analog input/Digital output | Analog input                                          |
|                     | C1     | IN1ARN/DMICDAT1  | Analog input/Digital input  | Analog input                                          |
|                     | H4     | IN2LN/DMICCLK2   | Analog input/Digital output | Analog input                                          |
|                     | E1     | IN2RN/DMICDAT2   | Analog input/Digital input  | Analog input                                          |
| DBVDD1              | T12    | AIF1BCLK/GPIO9   | Digital I/O                 | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|                     | R11    | AIF1LRCLK/GPIO11 | Digital I/O                 | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|                     | P10    | AIF1RXDAT/GPIO8  | Digital I/O                 | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|                     | T10    | AIF1TXDAT/GPIO10 | Digital I/O                 | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|                     | M10    | CIF1MISO         | Digital output              | Digital output                                        |
|                     | L9     | CIF1MOSI         | Digital input               | Digital input                                         |
|                     | L11    | CIF1SCLK         | Digital input               | Digital input                                         |
|                     | K10    | CIF1SS           | Digital input               | Digital input                                         |
|                     | P12    | CIF2SCLK         | Digital input               | Digital input                                         |
|                     | N11    | CIF2SDA          | Digital I/O                 | Digital input                                         |
|                     | J9     | IRQ              | Digital output              | Digital output                                        |
|                     | M12    | MCLK1            | Digital input               | Digital input                                         |
|                     | T8     | MIF1SCLK/GPIO16  | Digital I/O                 | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|                     | P8     | MIF1SDA/GPIO7    | Digital I/O                 | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|                     | H8     | RESET            | Digital input               | Digital input, Pull-up to DBVDD1                      |
|                     | R9     | SLIMCLK          | Digital I/O                 | Digital input                                         |
|                     | N9     | SLIMDAT          | Digital I/O                 | Digital input                                         |

**Table 4-116. CS47L35 Digital I/O Status in Reset (Cont.)**

| Power Domain | Pin No | Name             | Type           | Reset Status                                          |
|--------------|--------|------------------|----------------|-------------------------------------------------------|
| DBVDD2       | P6     | AIF2BCLK/GPIO13  | Digital I/O    | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|              | M6     | AIF2LRCLK/GPIO15 | Digital I/O    | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|              | K6     | AIF2RXDAT/GPIO14 | Digital I/O    | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|              | L5     | AIF2TXDAT/GPIO12 | Digital I/O    | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|              | R5     | AIF3BCLK/GPIO2   | Digital I/O    | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|              | N5     | AIF3LRCLK/GPIO4  | Digital I/O    | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|              | P4     | AIF3RXDAT/GPIO3  | Digital I/O    | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|              | M4     | AIF3TXDAT/GPIO1  | Digital I/O    | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|              | T6     | MCLK2            | Digital input  | Digital input                                         |
|              | M2     | SPKCLK/GPIO6     | Digital I/O    | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|              | N3     | SPKDAT/GPIO5     | Digital I/O    | Digital input (GPIO), bus-keeper enabled <sup>2</sup> |
|              | R7     | TCK              | Digital input  | Digital input, Pull-down to DGND                      |
|              | N7     | TDI              | Digital input  | Digital input, Pull-down to DGND                      |
|              | L7     | TDO              | Digital output | Digital output                                        |
|              | K8     | TMS              | Digital input  | Digital input, Pull-down to DGND                      |
|              | M8     | TRST             | Digital input  | Digital input, Pull-down to DGND                      |

1. The dual-function INnLN/DMICCLKn and INnRN/DMICDATn pins default to their respective analog input functions after power-on reset is completed. The analog input functions are referenced to the MICVDD power domain.
2. The power-up condition of the GPIO pins depends upon whether the pin is actively driven by another device when the CS47L35 starts up. If the pin is actively driven, the bus keeper maintains this logic level. If the pin is not actively driven, the bus keeper may establish either a Logic 1 or Logic 0 as the default input level.

## 4.23 Hardware Reset, Software Reset, Wake-Up, and Device ID

The CS47L35 supports hardware- and software-controlled reset functions. The reset functions, and the Sleep/Wake-Up state transitions, provide similar (but not identical) functionality. Each of these is described in the following subsections.

The CS47L35 device ID can be read from the Software\_Reset (R0) control register, as described in [Section 4.23.7](#).

### 4.23.1 Hardware Reset

The CS47L35 provides a hardware reset function, which is executed whenever the  $\overline{\text{RESET}}$  input is asserted (Logic 0). The  $\overline{\text{RESET}}$  input is active low and is referenced to the DBVDD1 power domain. A hardware reset causes all of the CS47L35 control registers to be reset to their default states.

An internal pull-up resistor is enabled by default on the  $\overline{\text{RESET}}$  pin; this can be configured using the RESET\_PU bit. A pull-down resistor is also available, as described in [Table 4-117](#). When the pull-up and pull-down resistors are both enabled, the CS47L35 provides a bus keeper function on the  $\overline{\text{RESET}}$  pin. The bus keeper function holds the input logic level unchanged whenever the external circuit removes the drive (e.g., if the signal is tristated).

If the CS47L35 SLIMbus component is in its operational state, it must be reset prior to scheduling a hardware reset. See [Section 4.10](#) for details of the SLIMbus reset control messages.

**Table 4-117. Reset Pull-Up/Pull-Down Configuration**

| Register Address               | Bit | Label    | Default | Description                                                                                                                                                                                             |
|--------------------------------|-----|----------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R6864 (0x1AD0)<br>AOD_Pad_Ctrl | 1   | RESET_PU | 1       | $\overline{\text{RESET}}$ Pull-up enable<br>0 = Disabled<br>1 = Enabled<br><b>Note:</b> If RESET_PD and RESET_PU are both set, a bus keeper function is enabled on the $\overline{\text{RESET}}$ pin.   |
|                                | 0   | RESET_PD | 0       | $\overline{\text{RESET}}$ Pull-down enable<br>0 = Disabled<br>1 = Enabled<br><b>Note:</b> If RESET_PD and RESET_PU are both set, a bus keeper function is enabled on the $\overline{\text{RESET}}$ pin. |

### 4.23.2 Software Reset

A software reset is executed by writing any value to register R0. A software reset causes most of the CS47L35 control registers to be reset to their default states. Note that the control-write sequencer memory is retained during software reset.

Note that the first register read/write operation following a software reset may be unsuccessful, if the register access is attempted via a different control interface to the one that commanded the software reset. Note that only the first register read/write is affected, and only when using more than one control interface.

### 4.23.3 Wake-Up

The CS47L35 is in Sleep Mode when AVDD and DBVDD1 are present, and DCVDD is below its reset threshold. (Note that specific control requirements are also applicable for entering Sleep Mode, as described in [Section 4.13](#).)

In Sleep Mode, most of the digital core (and control registers) are held in reset; selected functions and control registers are maintained via an always-on internal supply domain. See [Section 4.13](#) for details of the always-on functions.

A wake-up transition (from Sleep Mode) is similar to a software reset, but selected functions and control registers are maintained via an always-on internal supply domain—the always-on registers are not reset during wake-up. See [Section 4.13](#) for details of the always-on functions.

### 4.23.4 Write Sequencer and DSP Firmware Memory Control in Reset and Wake-Up

The control-write sequencer memory contents reverts to its default contents following power-on reset, a hardware reset, or a Sleep Mode transition. The control sequences (including any user-defined sequences) are maintained in the sequencer memory through software reset.

The DSP firmware memory contents are cleared following power-on reset, a hardware reset, or a Sleep Mode transition. The firmware memory contents are not affected by software reset, provided DCVDD is held above its reset threshold.

See [Section 5.2](#) for a summary of the CS47L35 memory reset conditions.

### 4.23.5 Boot Sequence

Following hardware reset, software reset, or wake-up from Sleep Mode, a boot sequence is executed. The BOOT\_DONE\_STSx bits (see [Table 4-115](#)) are deasserted during hardware reset and software reset, and also in Sleep Mode. The BOOT\_DONE\_STSx bits are asserted on completion of the boot sequence. Control register writes should not be attempted until BOOT\_DONE\_STSx has been asserted.

The BOOT\_DONE\_STSx status is an input to the interrupt control circuit and can be used to trigger an interrupt event; see [Section 4.15](#). Note that the BOOT\_DONE\_STS1 and BOOT\_DONE\_STS2 bits provide the same information.

For details of the boot sequence, see [Section 4.18](#).

### 4.23.6 Digital I/O Status in Reset

The status of the CS47L35 digital I/O pins following hardware reset, software reset, or wake-up is described in [Section 4.22.2](#).

### 4.23.7 Device ID

The device ID can be read from Register R0. The hardware revision can be read from Register R1.

The software revision can be read from Register R2. The software revision code is incremented if software driver compatibility or software feature support is changed.

**Table 4-118. Device Reset and ID**

| Register Address                 | Bit  | Label               | Default | Description                                                                                                                  |
|----------------------------------|------|---------------------|---------|------------------------------------------------------------------------------------------------------------------------------|
| R0 (0x0000)<br>Software_Reset    | 15:0 | SW_RST_DEV_ID[15:0] | 0x6360  | Writing to this register resets all registers to their default state. Reading from this register indicates Device ID 0x6360. |
| R1 (0x0001)<br>Hardware_Revision | 7:0  | HW_REVISION[7:0]    | —       | Hardware Device revision. This field is incremented for every new revision of the device.                                    |
| R2 (0x0002)<br>Software_Revision | 7:0  | SW_REVISION[7:0]    | —       | Software Device revision. This field is incremented if software driver compatibility or software feature support is changed. |

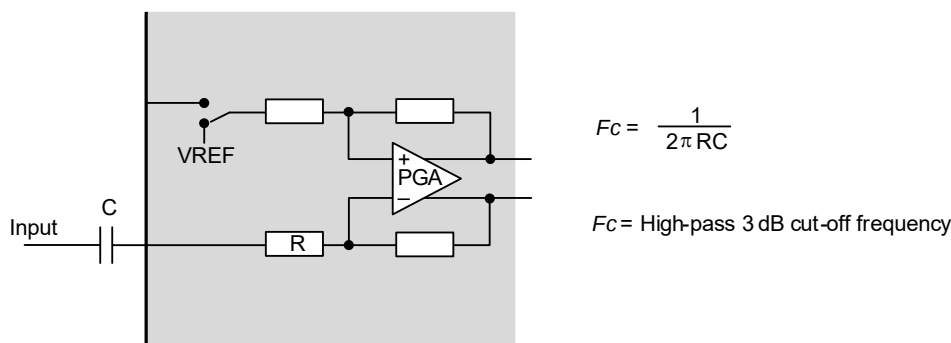
## 5 Applications

### 5.1 Recommended External Components

This section provides information on the recommended external components for use with the CS47L35.

#### 5.1.1 Analog Input Paths

The CS47L35 supports up to six analog audio input connections. Each of these inputs is biased to the internal DC reference, VREF. (Note that this reference voltage is present on the VREFC pin.) A DC-blocking capacitor is required for each analog input pin used in the target application. The choice of capacitor is determined by the filter that is formed between that capacitor and the impedance of the input pin. The circuit is shown in [Fig. 5-1](#).


**Figure 5-1. Audio Input Path DC-Blocking Capacitor**

In accordance with the CS47L35 input pin resistance (see [Table 3-5](#)), a 1-μF capacitance for all input connections gives good results in most cases, with a 3-dB cut-off frequency around 13 Hz.

Ceramic capacitors are suitable, but take care to ensure the desired capacitance is maintained at the AVDD operating voltage. Also, ceramic capacitors may show microphonic effects, where vibrations and mechanical conditions give rise to electrical signals. This is particularly problematic for microphone input paths where a large signal gain is required.

A single capacitor is required for a single-ended line or microphone input connection. For a differential input connection, a DC-blocking capacitor is required on both input pins.

The external connections for single-ended and differential microphones, incorporating the CS47L35 microphone bias circuit, are shown in [Section 5.1.3](#); see [Fig. 5-2](#).

#### 5.1.2 DMIC Input Paths

The CS47L35 supports up to four channels of DMIC input; two channels of audio data can be multiplexed on each DMICDAT<sub>n</sub> pin. Each of these stereo pairs is clocked using the respective DMICCLK<sub>n</sub> pin.

The external connections for digital microphones, incorporating the CS47L35 microphone bias circuit, are shown in [Fig. 5-4](#). Ceramic decoupling capacitors for the digital microphones may be required—refer to the specific recommendations for the application microphones.

If two microphones are connected to a single DMICDAT pin, the microphones must be configured to ensure that the Left mic transmits a data bit when DMICCLK is high, and the Right mic transmits a data bit when DMICCLK is low. The CS47L35 samples the DMIC data at the end of each DMICCLK phase. Each microphone must tristate its data output when the other microphone is transmitting. Integrated pull-down resistors can be enabled on the DMICDAT pins if required.

The voltage reference for each DMIC interface is selectable. It is important that the selected reference for the CS47L35 interface is compatible with the applicable configuration of the external microphone.

### 5.1.3 Microphone Bias Circuit

The CS47L35 is designed to interface easily with analog or digital microphones.

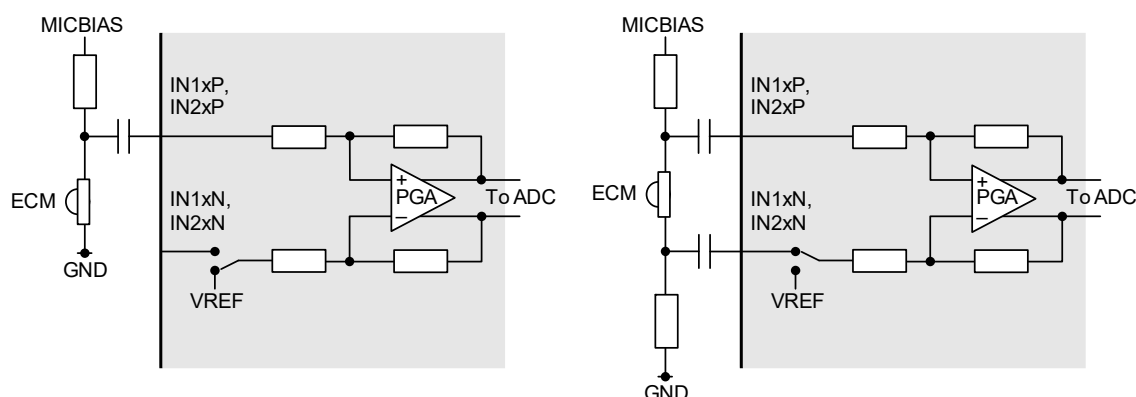
Each microphone requires a bias current (electret condenser microphones) or voltage supply (silicon microphones); these can be provided by the MICBIAS regulators on the CS47L35. Two MICBIAS generators are available; switchable outputs allow four separate reference/supply outputs to be independently controlled.

Note that the MICVDD pin can also be used (instead of MICBIAS<sub>nx</sub>) as a reference or power supply for external microphones. The MICBIAS outputs are recommended, as these offer better noise performance and independent enable/disable control.

Analog microphones may be connected in single-ended or differential configurations, as shown in [Fig. 5-2](#). The differential configuration provides better performance due to its rejection of common-mode noise; the single-ended method provides a reduction in external component count.

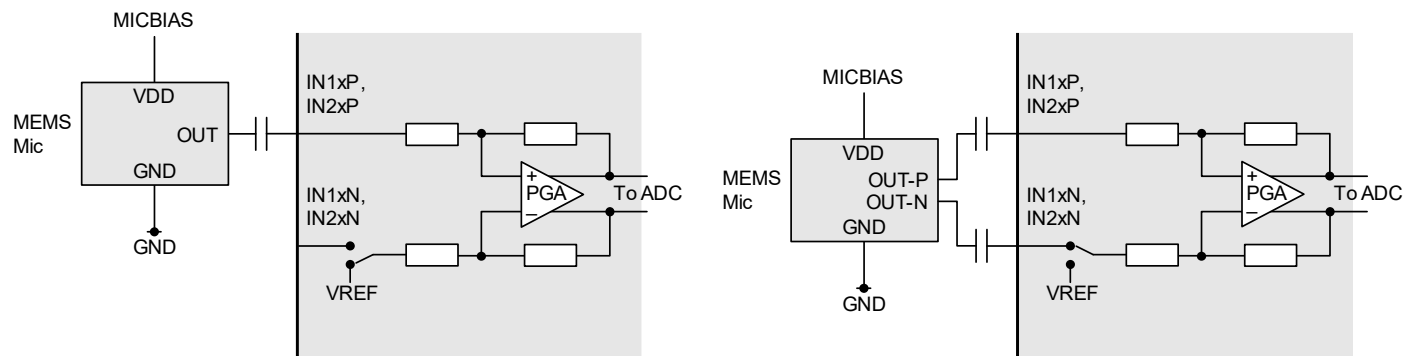
A bias resistor is required when using an ECM. The bias resistor should be chosen according to the minimum operating impedance of the microphone and MICBIAS voltage so that the maximum bias current of the CS47L35 is not exceeded.

A 2.2-k $\Omega$  bias resistor is recommended; this provides compatibility with a wide range of microphone components.



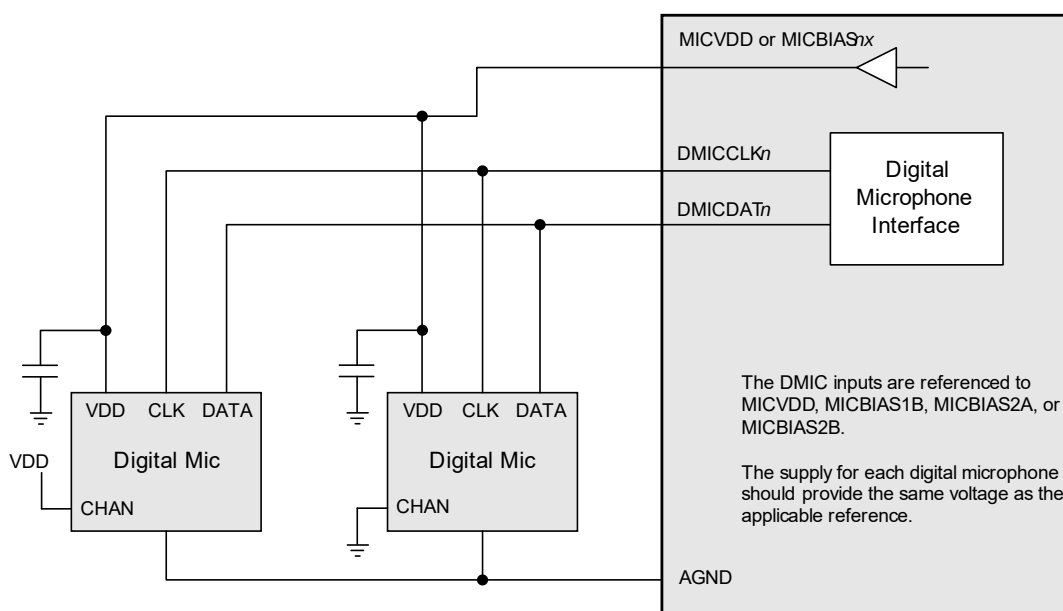
**Figure 5-2. Single-Ended and Differential ECM Microphone Connections**

Analog MEMS microphones can be connected to the CS47L35 as shown in [Fig. 5-3](#). In this configuration, the MICBIAS generators provide a low-noise supply for the microphones; a bias resistor is not required.



**Figure 5-3. Single-Ended and Differential Analog MEMS Microphone Connections**

DMIC connection to the CS47L35 is shown in [Fig. 5-4](#). Note that ceramic decoupling capacitors at the DMIC power supply pins may be required—refer to the specific recommendations for the application microphones.



**Figure 5-4. DMIC Connection**

Each MICBIAS generator can operate in Regulator Mode or in Bypass Mode. See [Section 4.19](#) for details of the MICBIAS generators.

In Regulator Mode, the MICBIAS regulators are designed to operate without external decoupling capacitors. The regulators can be configured to support a capacitive load if required (e.g., for DMIC supply decoupling). The compatible load conditions are detailed in [Table 3-11](#).

If the capacitive load on MICBIAS1 or MICBIAS2 exceeds the specified conditions for Regulator Mode (e.g., due to a decoupling capacitor or long PCB trace), the respective generator must be configured in Bypass Mode.

The maximum output current for each MICBIAS regulator is noted in [Table 3-11](#). This limit must be observed for each pair of MICBIAS<sub>n</sub>x outputs, especially if more than one microphone is connected to a single regulator. Note that the maximum output current differs between Regulator Mode and Bypass Mode. The MICBIAS output voltage can be adjusted using register control in Regulator Mode.

### 5.1.4 Headphone/Earpiece Driver Output Path

The CS47L35 provides a stereo headphone output driver and a mono (differential) earpiece output driver. Note that the respective output signal path is common to both drivers; only one of these drivers may be enabled at any time. These outputs are all ground referenced, allowing direct connection to the external loads. There is no requirement for DC-blocking capacitors.

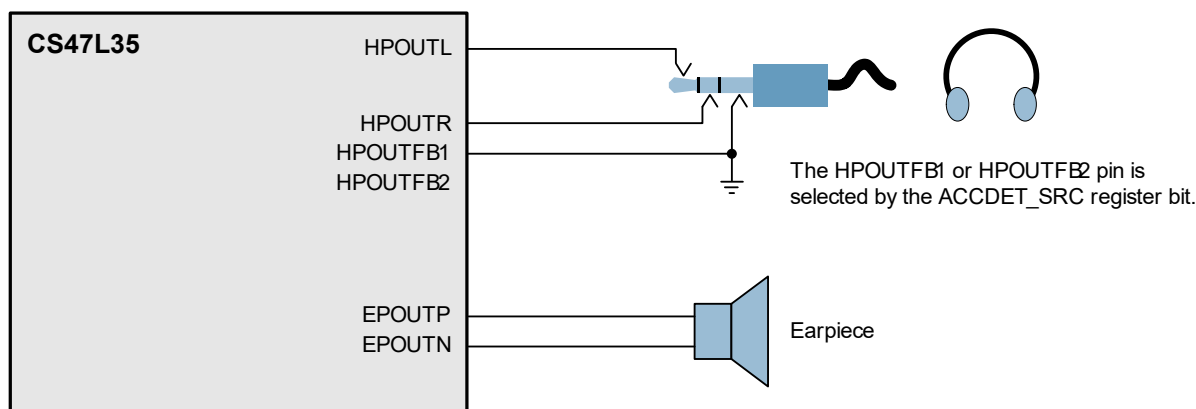
Under default register conditions, the headphone/earpiece output path is configured for stereo output on HPOUTL and HPOUTR; this is ideal for stereo headphone loads. In Mono Mode, with the earpiece output driver selected, the output path is configured for mono (differential) output on EOUTP and EOUTN; this is suitable for an earpiece or hearing coil load.

The headphone output incorporates a common mode, or ground loop, feedback path that provides rejection of system-related ground noise. The feedback pin must be connected to ground for normal operation of the headphone outputs. The HPOUT feedback is supported on two pins—the applicable pin is selected using ACCDET\_SRC.

The selected feedback pin should be connected to GND as close as possible to the respective headphone jack ground pin, as shown in Fig. 5-5. In mono (differential) mode, the feedback pins should be connected to the ground plane that is closest to the earpiece output PCB tracks.

It is recommended to ensure that the electrical characteristics of the PCB traces for each output pair are closely matched. This is particularly important to matching the two traces of a differential (BTL) output.

Typical headphone and earpiece connections are shown in Fig. 5-5.



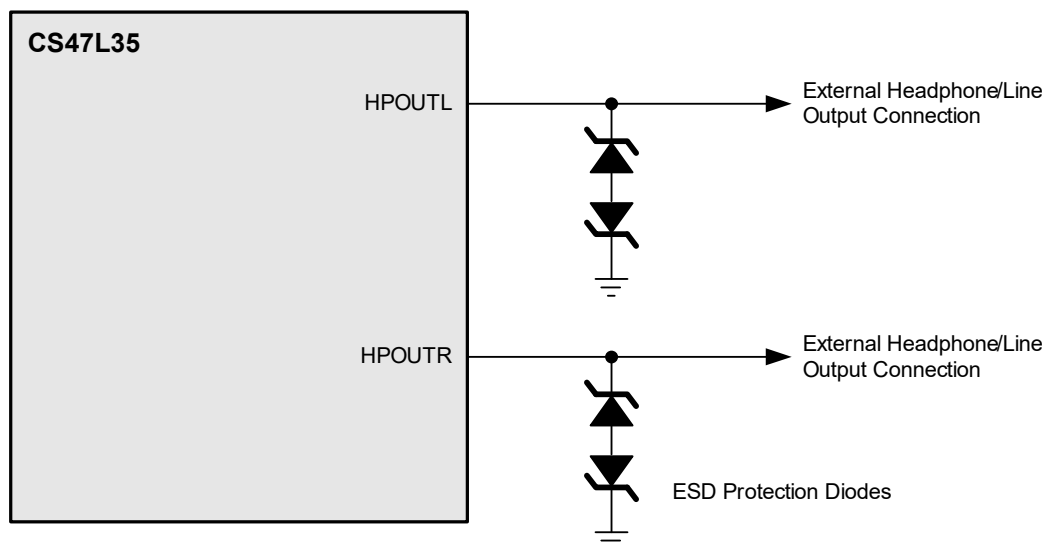
**Figure 5-5. Headphone and Earpiece Connection**

It is common for ESD diodes to be wired to pins that link to external connectors. This provides protection from potentially harmful ESD effects. In a typical application, ESD diodes are recommended if the headphone path is used for external headphone or line output.

The HPOUT outputs are ground-referenced, and the respective voltages may swing between +1.8V and –1.8V. The ESD diode configuration must be carefully chosen.

The recommended ESD diode configuration for these ground-referenced outputs is shown in Fig. 5-6. The back-to-back arrangement prevents clipping and distortion of the output signal.

Note that similar care is required when connecting the CS47L35 outputs to external circuits that provide input path ESD protection; the configuration on those input circuits must be correctly designed to accommodate ground-referenced signals.

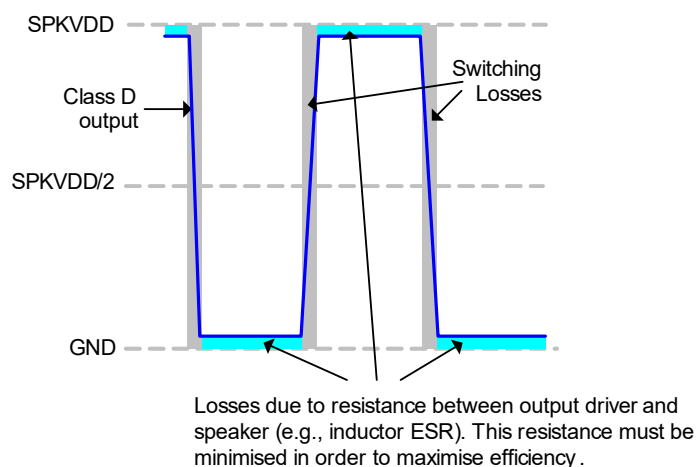


**Figure 5-6. ESD Diode Configuration for External Output Connections**

### 5.1.5 Speaker-Driver Output Path

The CS47L35 incorporates a Class D speaker driver, offering high amplifier efficiency at large signal levels. As the Class D output is a pulse-width modulated signal, the choice of speakers and tracking of signals is critical for ensuring good performance and reducing EMI in this mode.

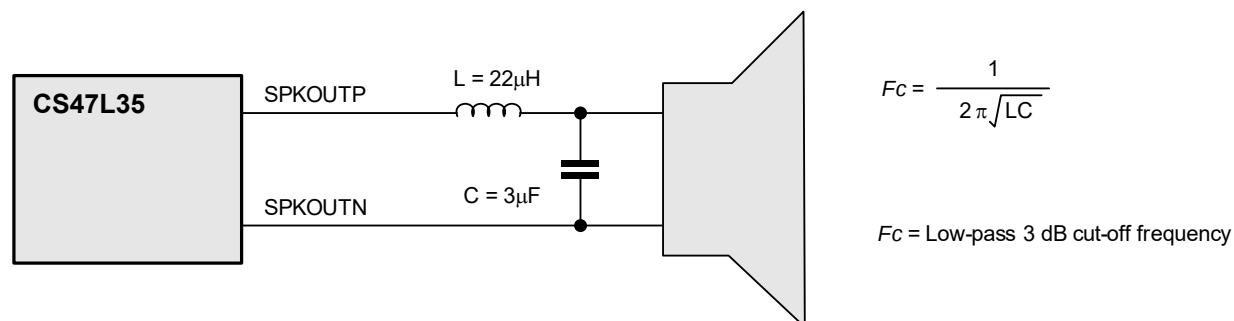
The efficiency of the speaker driver is affected by the series resistance between the CS47L35 and the speaker (e.g., PCB track loss and inductor ESR) as shown in [Fig. 5-7](#). This resistance should be as low as possible to maximize efficiency.



**Figure 5-7. Speaker Connection Losses**

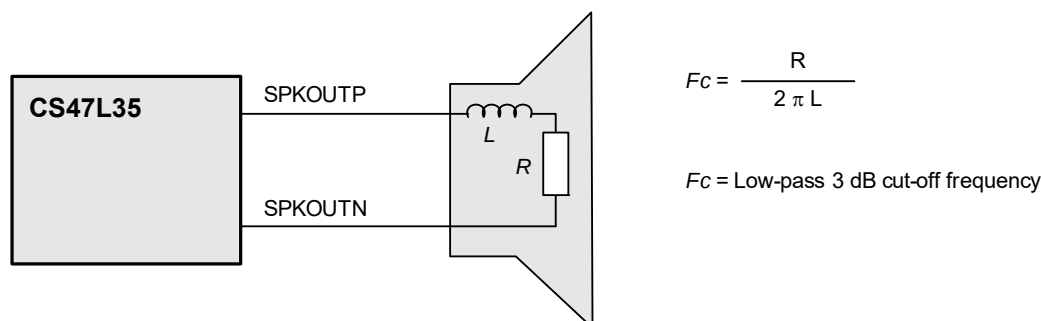
The Class D output requires external filtering to recreate the audio signal. This may be implemented using a 2<sup>nd</sup> order LC or 1<sup>st</sup> order RC filter, or else may be achieved by using a loudspeaker whose internal inductance provides the required filter response. An LC or RC filter should be used if the loudspeaker characteristics are unknown or unsuitable, or if the length of the loudspeaker connection is likely to lead to EMI problems.

In applications where it is necessary to provide Class D filter components, a second-order LC filter is the recommended solution as it provides more attenuation at higher frequencies and minimizes power dissipated in the filter when compared to a first order RC filter (lower ESR). This maximizes both rejection of unwanted switching frequencies and overall speaker efficiency. A suitable implementation is shown in [Fig. 5-8](#).



**Figure 5-8. Class D Output Filter Components**

A simple equivalent circuit of a loudspeaker consists of a serially-connected resistor and inductor, as shown in [Fig. 5-9](#). This circuit provides a low-pass filter for the speaker output. If the loudspeaker characteristics are suitable, the loudspeaker itself can be used in place of the filter components described earlier. This is known as filterless operation.



**Figure 5-9. Speaker Equivalent Circuit for Filterless Operation**

For filterless Class D operation, it is important to ensure that a speaker with suitable inductance is chosen. For example, if we know the speaker impedance is 8 Ω and the desired cut-off frequency is 20 kHz, the optimum speaker inductance may be calculated as shown in [Eq. 5-1](#).

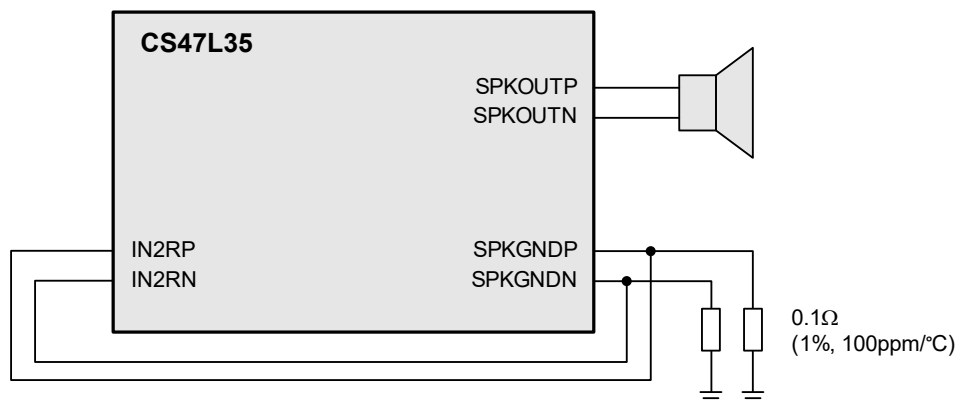
$$L = \frac{R}{2\pi F_c} = \frac{8\Omega}{2\pi \times 20\text{kHz}} = 64\mu\text{H}$$

**Equation 5-1. Speaker Inductance Calculation**

An 8-Ω loudspeaker typically has an inductance in the range 20–100 µH; however, it should be noted that a loudspeaker inductance is not constant across the relevant frequencies for Class D operation (up to and beyond the Class D switching frequency). Care should be taken to ensure that the cut-off frequency of the loudspeaker's filtering is low enough to suppress the high-frequency energy of the Class D switching and, in so doing, to prevent speaker damage. The Class D outputs of the CS47L35 operate at much higher frequencies than is recommended for most speakers, and it must be ensured that the cut-off frequency is low enough to protect the speaker.

The Class D speaker outputs are designed to support monitoring of external loudspeakers, giving real-time feedback for algorithms such as Cirrus Logic's speaker protection software. This enables maximum audio output to be achieved, while ensuring the loudspeakers are also fully protected from damage.

The external speaker connections, incorporating the output current monitoring requirements, are shown in [Fig. 5-10](#). Note that, if output current monitoring is not required on one or more speaker channels, the respective ground connections should be tied directly to ground on the PCB.



**Figure 5-10. Speaker Output Current Monitoring Connections (Speaker Protection)**

### 5.1.6 Power Supply/Reference Decoupling

Electrical coupling exists particularly in digital logic systems where switching in one subsystem causes fluctuations on the power supply. This effect occurs because the inductance of the power supply acts in opposition to the changes in current flow that are caused by the logic switching. The resultant variations (spikes) in the power-supply voltage can cause malfunctions and unintentional behavior in other components. A decoupling (bypass) capacitor can be used as an energy storage component that provides power to the decoupled circuit for the duration of these power-supply variations, protecting it from malfunctions that could otherwise arise.

Coupling also occurs in a lower frequency form when ripple is present on the power supply rail caused by changes in the load current or by limitations of the power-supply regulation method. In audio components such as the CS47L35, these variations can alter the performance of the signal path, leading to degradation in signal quality. A decoupling capacitor can be used to filter these effects by presenting the ripple voltage with a low-impedance path that does not affect the circuit to be decoupled.

These coupling effects are addressed by placing a capacitor between the supply rail and the corresponding ground reference. In the case of systems comprising multiple power supply rails, decoupling should be provided on each rail.

PCB layout is also a contributory factor for coupling effects. If multiple power supply rails are connected to a single supply source, it is recommended to provide separate PCB tracks connecting each rail to the supply. See [Section 5.5](#) for PCB-layout recommendations.

The recommended power-supply decoupling capacitors for CS47L35 are detailed in [Table 5-1](#).

**Table 5-1. Power Supply Decoupling Capacitors**

| Power Supply   | Decoupling Capacitor                                                   |
|----------------|------------------------------------------------------------------------|
| AVDD1, AVDD2   | 2 x 1.0 $\mu$ F ceramic—one capacitor on each AVDDn pin                |
| CPVDD1         | 4.7 $\mu$ F ceramic                                                    |
| CPVDD2         | 4.7 $\mu$ F ceramic                                                    |
| DBVDD1, DBVDD2 | 2 x 0.1 $\mu$ F ceramic <sup>1</sup> —one capacitor on each DBVDDn pin |
| DCVDD          | 4.7 $\mu$ F ceramic                                                    |
| FLLVDD         | 1.0 $\mu$ F ceramic                                                    |
| MICVDD         | 4.7 $\mu$ F ceramic                                                    |
| SPKVDD         | 4.7 $\mu$ F ceramic                                                    |
| VREFC          | 2.2 $\mu$ F ceramic                                                    |

1. Total capacitance of 4.7  $\mu$ F is required for each DBVDDn domain. This can be provided by dedicated DBVDDn decoupling or by other capacitors on the same power rail.

All decoupling capacitors should be placed as close as possible to the CS47L35 device. The connection between AGND, the AVDD decoupling capacitor, and the main system ground should be made at a single point as close as possible to the AGND balls of the CS47L35.

Due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. For most application the use of ceramic capacitors with capacitor dielectric X5R is recommended.

### 5.1.7 Charge-Pump Components

The CS47L35 incorporates two charge-pump circuits (CP1 and CP2).

CP1 generates the CP1VOUT<sub>nx</sub> supply rails for the ground-referenced headphone drivers; CP2 generates the CP2VOUT supply rail for the microphone bias (MICBIAS) regulators.

Decoupling capacitors are required on each of the charge-pump outputs. Two fly-back capacitors are required for CP1; a single fly-back capacitor is required for CP2.

The recommended charge-pump capacitors for CS47L35 are detailed in [Table 5-2](#).

**Table 5-2. Charge-Pump External Capacitors**

| Description                                           | Capacitor                                                                                  |
|-------------------------------------------------------|--------------------------------------------------------------------------------------------|
| CP1VOUT1P decoupling                                  | Required capacitance is 2.0 $\mu$ F at 2 V.<br>Suitable component typically 4.7 $\mu$ F.   |
| CP1VOUT1N decoupling                                  | Required capacitance is 2.0 $\mu$ F at 2 V.<br>Suitable component typically 4.7 $\mu$ F.   |
| CP1 fly-back 1<br>(connect between CP1C1A and CP1C1B) | Required capacitance is 1.0 $\mu$ F at 2 V.<br>Suitable component typically 2.2 $\mu$ F.   |
| CP1VOUT2P decoupling                                  | Required capacitance is 2.0 $\mu$ F at 2 V.<br>Suitable component typically 4.7 $\mu$ F.   |
| CP1VOUT2N decoupling                                  | Required capacitance is 2.0 $\mu$ F at 2 V.<br>Suitable component typically 4.7 $\mu$ F.   |
| CP1 fly-back 2<br>(connect between CP1C2A and CP1C2B) | Required capacitance is 1.0 $\mu$ F at 2 V.<br>Suitable component typically 2.2 $\mu$ F.   |
| CP2VOUT decoupling                                    | Required capacitance is 1.0 $\mu$ F at 3.6 V.<br>Suitable component typically 4.7 $\mu$ F. |
| CP2 fly-back<br>(connect between CP2CA and CP2CB)     | Required capacitance is 220 nF at 2 V.<br>Suitable component typically 470 nF.             |

Ceramic capacitors are recommended for these charge-pump requirements. Note that, due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. Ceramic capacitors with X5R dielectric are recommended.

The positioning of the charge-pump capacitors is important. These capacitors (particularly the fly-back capacitors) must be placed as close as possible to the CS47L35. The component choice and positioning of the CP1 components are more critical than those of CP2, due to the higher output power requirements of CP1.

### 5.1.8 External Accessory Detection Components

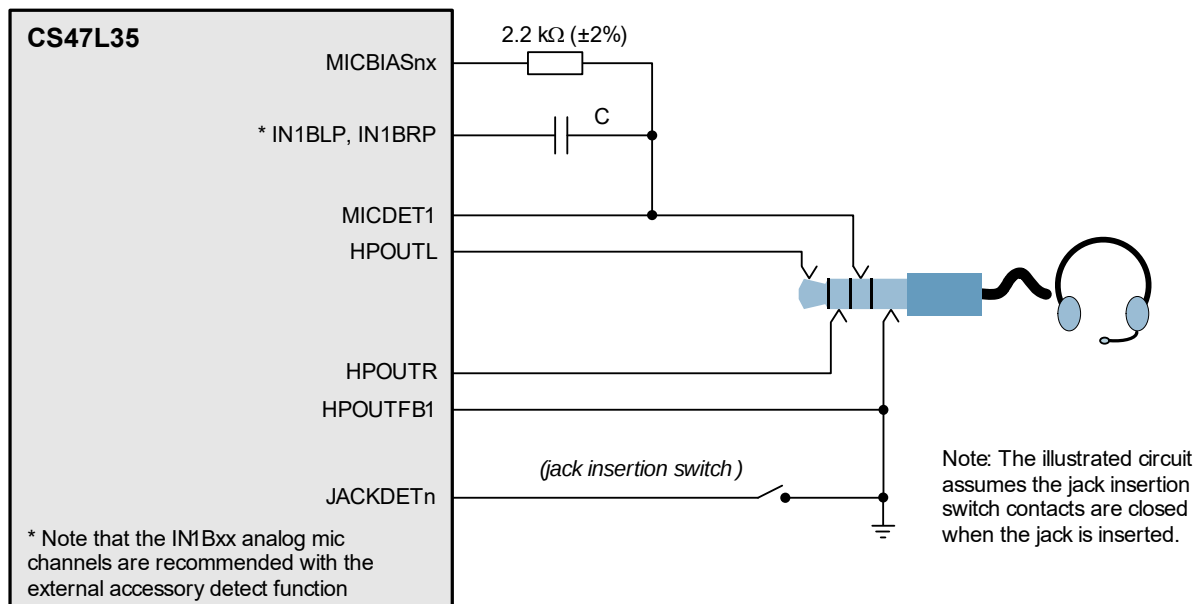
The external accessory detection circuit measures jack insertion using the JACKDET1 and JACKDET2 pins. The insertion switch status is detected using an internal pull-up resistor circuit on the respective pin. Note that the logic thresholds associated with the two JACKDET differ from each other, as described in [Table 3-11](#)—this provides support for different jack switch configurations.

Microphone detection and key-button press detection is supported using the MICDET<sub>n</sub> pins. The applicable pin should be connected to one of the MICBIAS<sub>nx</sub> outputs, via a 2.2-k $\Omega$  bias resistor, as described in [Section 5.1.3](#). Note that, when using the external accessory detection function, the MICBIAS<sub>nx</sub> resistor must be 2.2 k $\Omega$   $\pm$ 2%.

A recommended circuit configuration, including headphone output on HPOUT and microphone connections, is shown in [Fig. 5-11](#). See [Section 5.1.1](#) for details of the DC-blocking microphone input capacitor selection.

The recommended external components and connections for microphone/push-button detection are shown in [Fig. 5-11](#).

Note that, when using the microphone detect circuit, it is recommended to use the IN1BLP or IN1BRP analog microphone input paths to ensure best immunity to electrical transients arising from the external accessory.



**Figure 5-11. External Accessory Detection**

The accessory detection circuit measures the impedance of an external load connected to one of the MICDET pins.

The microphone-detection circuit uses MICVDD, MICBIAS1A, MICBIAS1B, or MICBIAS2A as a reference. The applicable source is configured using MICD\_BIAS\_SRC.

The CS47L35 can detect the presence of a typical microphone and up to six push buttons, using the components shown in Fig. 5-12. When the microphone detection circuit is enabled, each of the push buttons shown causes a different bit in the MICD\_LVL field to be set.

The choice of external resistor values must take into account the impedance of the microphone—the detected impedance corresponds to the combined parallel resistance of the microphone and any asserted push button. The components shown in Fig. 5-12 are examples only, assuming default impedance measurement ranges and a microphone impedance of  $1\text{ k}\Omega$  or higher.

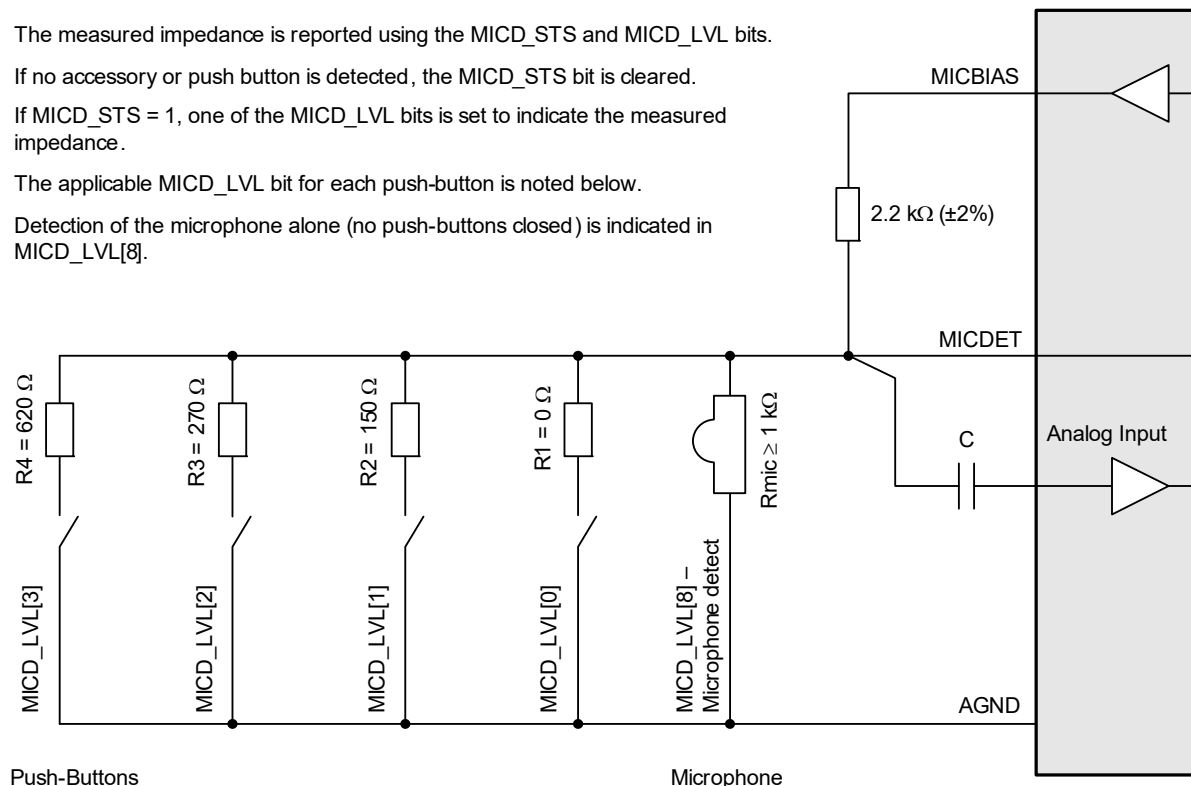
The measured impedance is reported using the MICD\_STS and MICD\_LVL bits.

If no accessory or push button is detected, the MICD\_STS bit is cleared.

If MICD\_STS = 1, one of the MICD\_LVL bits is set to indicate the measured impedance.

The applicable MICD\_LVL bit for each push-button is noted below.

Detection of the microphone alone (no push-buttons closed) is indicated in MICD\_LVL[8].



**Figure 5-12. External Accessory Detect Components**

## 5.2 Resets Summary

**Table 5-3** summarizes of the CS47L35 registers and other programmable memory under different reset conditions. The associated events and conditions are listed as follows:

- A power-on reset occurs when AVDD or DBVDD1 is below its respective reset threshold. Note that DCVDD is also required for initial start-up; subsequent interruption to DCVDD should only be permitted as part of a control sequence for entering Sleep Mode.
- A hardware reset occurs when the  $\overline{\text{RESET}}$  input is asserted (Logic 0).
- A software reset occurs when register R0 is written to.
- Sleep Mode is selected when DCVDD is removed. Note that the AVDD and DBVDD1 supplies must be present throughout the Sleep Mode duration.

**Table 5-3. Memory Reset Summary**

| Reset Type     | Always-On Registers <sup>1</sup> | Other Registers | Control-Write Sequencer Memory | DSP Firmware Memory   |
|----------------|----------------------------------|-----------------|--------------------------------|-----------------------|
| Power-on reset | Reset                            | Reset           | Reset                          | Reset                 |
| Hardware reset | Reset                            | Reset           | Reset                          | Reset                 |
| Software reset | Reset                            | Reset           | Retained                       | Retained <sup>2</sup> |
| Sleep Mode     | Retained                         | Reset           | Reset                          | Reset                 |

1. See [Section 4.13](#) for details of Sleep Mode and the always-on registers.

2. To retain the DSP firmware memory contents during software reset, it must be ensured that DCVDD is held above its reset threshold.

## 5.3 Output-Signal Drive-Strength Control

The CS47L35 supports configurable drive-strength control for the digital output pins. This can be used to assist system-level integration and design considerations.

The drive-strength control bits are described in [Table 5-4](#). Note that, in the case of bidirectional pins (e.g., GPIO<sub>n</sub>), the drive-strength control bits are only applicable if the pin is configured as an output.

**Table 5-4. Output Drive-Strength and Slew-Rate Control**

| Register Address                   | Bit | Label            | Default | Description                                                    |
|------------------------------------|-----|------------------|---------|----------------------------------------------------------------|
| R8 (0x0008)<br>Ctrl_IF_CFG_1       | 8   | CIF1MISO_DRV_STR | 1       | CIF1MISO output drive strength<br>0 = 4 mA<br>1 = 8 mA         |
| R9 (0x0009)<br>Ctrl_IF_CFG_2       | 9   | CIF2SDA_DRV_STR  | 1       | CIF2SDA output drive strength<br>0 = 4 mA<br>1 = 8 mA          |
| R1520 (0x05F0)<br>Slimbus_Pad_Ctrl | 1   | SLIMDAT_DRV_STR  | 0       | SLIMDAT output drive strength<br>0 = 8 mA<br>1 = 12 mA         |
| R5889 (0x1701)<br>GPIO1_CTRL2      | 12  | GP1_DRV_STR      | 1       | AIF3TXDAT/GPIO1 output drive strength<br>0 = 4 mA<br>1 = 8 mA  |
| R5891 (0x1703)<br>GPIO2_CTRL2      | 12  | GP2_DRV_STR      | 1       | AIF3BCLK/GPIO2 output drive strength<br>0 = 4 mA<br>1 = 8 mA   |
| R5893 (0x1705)<br>GPIO3_CTRL2      | 12  | GP3_DRV_STR      | 1       | AIF3RXDAT/GPIO3 output drive strength<br>0 = 4 mA<br>1 = 8 mA  |
| R5895 (0x1707)<br>GPIO4_CTRL2      | 12  | GP4_DRV_STR      | 1       | AIF3LRCLK/GPIO4 output drive strength<br>0 = 4 mA<br>1 = 8 mA  |
| R5897 (0x1709)<br>GPIO5_CTRL2      | 12  | GP5_DRV_STR      | 1       | SPKDAT/GPIO5 output drive strength<br>0 = 4 mA<br>1 = 8 mA     |
| R5899 (0x170B)<br>GPIO6_CTRL2      | 12  | GP6_DRV_STR      | 1       | SPKCLK/GPIO6 output drive strength<br>0 = 4 mA<br>1 = 8 mA     |
| R5901 (0x170D)<br>GPIO7_CTRL2      | 12  | GP7_DRV_STR      | 1       | MIF1SDA/GPIO7 output drive strength<br>0 = 4 mA<br>1 = 8 mA    |
| R5903 (0x170F)<br>GPIO8_CTRL2      | 12  | GP8_DRV_STR      | 1       | AIF1RXDAT/GPIO8 output drive strength<br>0 = 4 mA<br>1 = 8 mA  |
| R5905 (0x1711)<br>GPIO9_CTRL2      | 12  | GP9_DRV_STR      | 1       | AIF1BCLK/GPIO9 output drive strength<br>0 = 4 mA<br>1 = 8 mA   |
| R5907 (0x1713)<br>GPIO10_CTRL2     | 12  | GP10_DRV_STR     | 1       | AIF1TXDAT/GPIO10 output drive strength<br>0 = 4 mA<br>1 = 8 mA |
| R5909 (0x1715)<br>GPIO11_CTRL2     | 12  | GP11_DRV_STR     | 1       | AIF1LRCLK/GPIO11 output drive strength<br>0 = 4 mA<br>1 = 8 mA |
| R5911 (0x1717)<br>GPIO12_CTRL2     | 12  | GP12_DRV_STR     | 1       | AIF2TXDAT/GPIO12 output drive strength<br>0 = 4 mA<br>1 = 8 mA |
| R5913 (0x1719)<br>GPIO13_CTRL2     | 12  | GP13_DRV_STR     | 1       | AIF2BCLK/GPIO13 output drive strength<br>0 = 4 mA<br>1 = 8 mA  |

**Table 5-4. Output Drive-Strength and Slew-Rate Control (Cont.)**

| Register Address               | Bit | Label        | Default | Description                                                    |
|--------------------------------|-----|--------------|---------|----------------------------------------------------------------|
| R5915 (0x171B)<br>GPIO14_CTRL2 | 12  | GP14_DRV_STR | 1       | AIF2RXDAT/GPIO14 output drive strength<br>0 = 4 mA<br>1 = 8 mA |
| R5917 (0x171D)<br>GPIO15_CTRL2 | 12  | GP15_DRV_STR | 1       | AIF2LRCLK/GPIO15 output drive strength<br>0 = 4 mA<br>1 = 8 mA |
| R5919 (0x171F)<br>GPIO16_CTRL2 | 12  | GP16_DRV_STR | 1       | MIF1SCLK/GPIO16 output drive strength<br>0 = 4 mA<br>1 = 8 mA  |

## 5.4 Digital Audio Interface Clocking Configurations

The digital audio interfaces (AIF1–AIF3) can be configured in master or slave modes. In all applications, it is important that the system clocking configuration is correctly designed. Incorrect clock configurations lead to audible clicks arising from dropped or repeated audio samples; this is caused by the inherent tolerances of multiple asynchronous system clocks.

To ensure reliable clocking of the audio interface functions, the external interface clocks (e.g., BCLK, LRCLK) must be derived from the same clock source as SYSCLK.

In AIF Master Mode, the external BCLK and LRCLK signals are generated by the CS47L35 and synchronization of these signals with SYSCLK is ensured. In this case, clocking of the AIF is typically derived from the MCLK1 or MCLK2 inputs, either directly or via the FLL circuit. Alternatively, an AIF<sub>n</sub> or SLIMbus interface can be used to provide the reference clock to which the AIF master can be synchronized.

In AIF Slave Mode, the external BCLK and LRCLK signals are generated by another device, as inputs to the CS47L35. In this case, the system clock (SYSCLK) must be generated from a source that is synchronized to the external BCLK and LRCLK inputs.

In a typical Slave Mode application, the BCLK input is selected as the clock reference, using the FLL to perform frequency shifting. The MCLK1 or MCLK2 inputs can also be used, but only if the selected clock is synchronized externally to the BCLK and LRCLK inputs. The SLIMbus interface can also provide the clock reference, via the FLL, provided that the BCLK and LRCLK signals are externally synchronized with the SLIMCLK input.

The valid AIF clocking configurations are listed in [Table 5-5](#) for AIF Master and AIF Slave Modes.

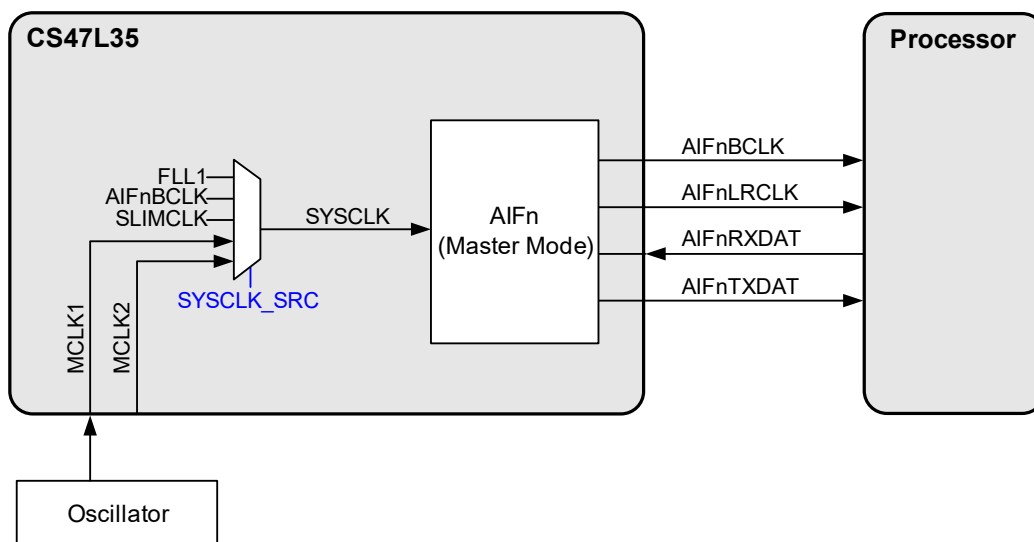
**Table 5-5. AIF Clocking Configurations**

| AIF Mode        | Clocking Configuration                                                                                                                                                                                |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AIF Master Mode | SYSCLK_SRC selects MCLK1 or MCLK2 as SYSCLK source.                                                                                                                                                   |
|                 | SYSCLK_SRC selects FLL1 as SYSCLK source;<br>FLL1_REFCLK_SRC selects MCLK1 or MCLK2 as FLL1 source.                                                                                                   |
|                 | SYSCLK_SRC selects FLL1 as SYSCLK source;<br>FLL1_REFCLK_SRC selects a different interface (BCLK, LRCLK, SLIMCLK) as FLL1 source.                                                                     |
| AIF Slave Mode  | SYSCLK_SRC selects FLL1 as SYSCLK source;<br>FLL1_REFCLK_SRC selects BCLK as FLL1 source.                                                                                                             |
|                 | SYSCLK_SRC selects MCLK1 or MCLK2 as SYSCLK source, provided MCLK is externally synchronized to the BCLK input.                                                                                       |
|                 | SYSCLK_SRC selects FLL1 as SYSCLK source;<br>FLL1_REFCLK_SRC selects MCLK1 or MCLK2 as FLL1 source, provided MCLK is externally synchronized to the BCLK input.                                       |
|                 | SYSCLK_SRC selects FLL1 as SYSCLK source;<br>FLL1_REFCLK_SRC selects a different interface (e.g., SLIMCLK) as FLL1 source, provided the other interface is externally synchronized to the BCLK input. |

In each case, the SYSCLK frequency must be a valid ratio to the LRCLK frequency; the supported clocking rates are defined by the SYSCLK\_FREQ and SAMPLE\_RATE<sub>n</sub> fields.

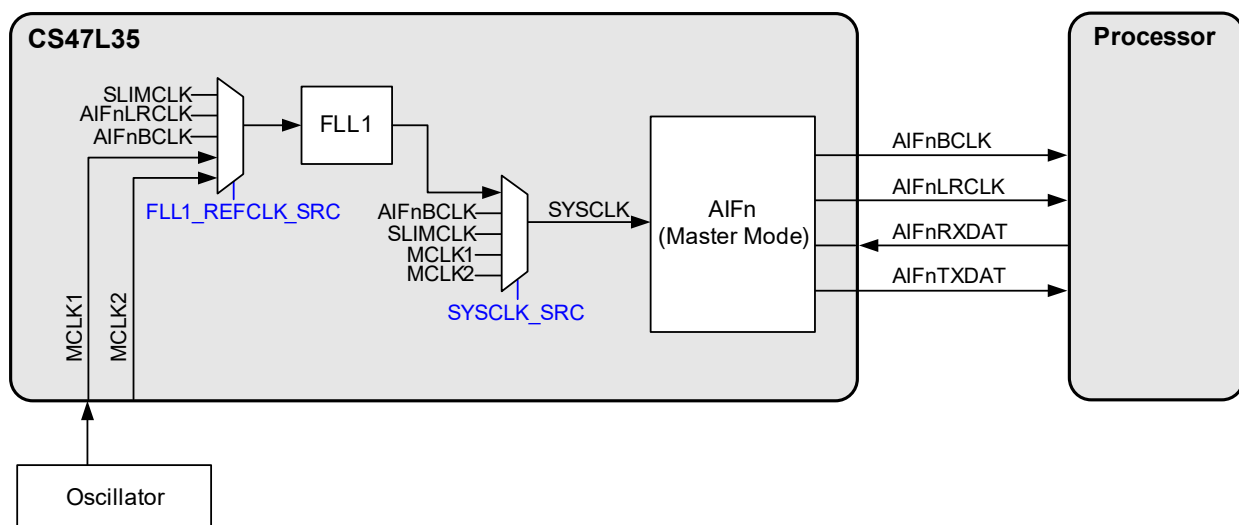
The valid AIF clocking configurations are shown in [Fig. 5-13](#) to [Fig. 5-19](#). Note that, where MCLK1 is shown as the clock source, it is equally possible to select MCLK2 as the clock source.

Fig. 5-13 shows AIF Master Mode operation, using MCLK as the clock reference.



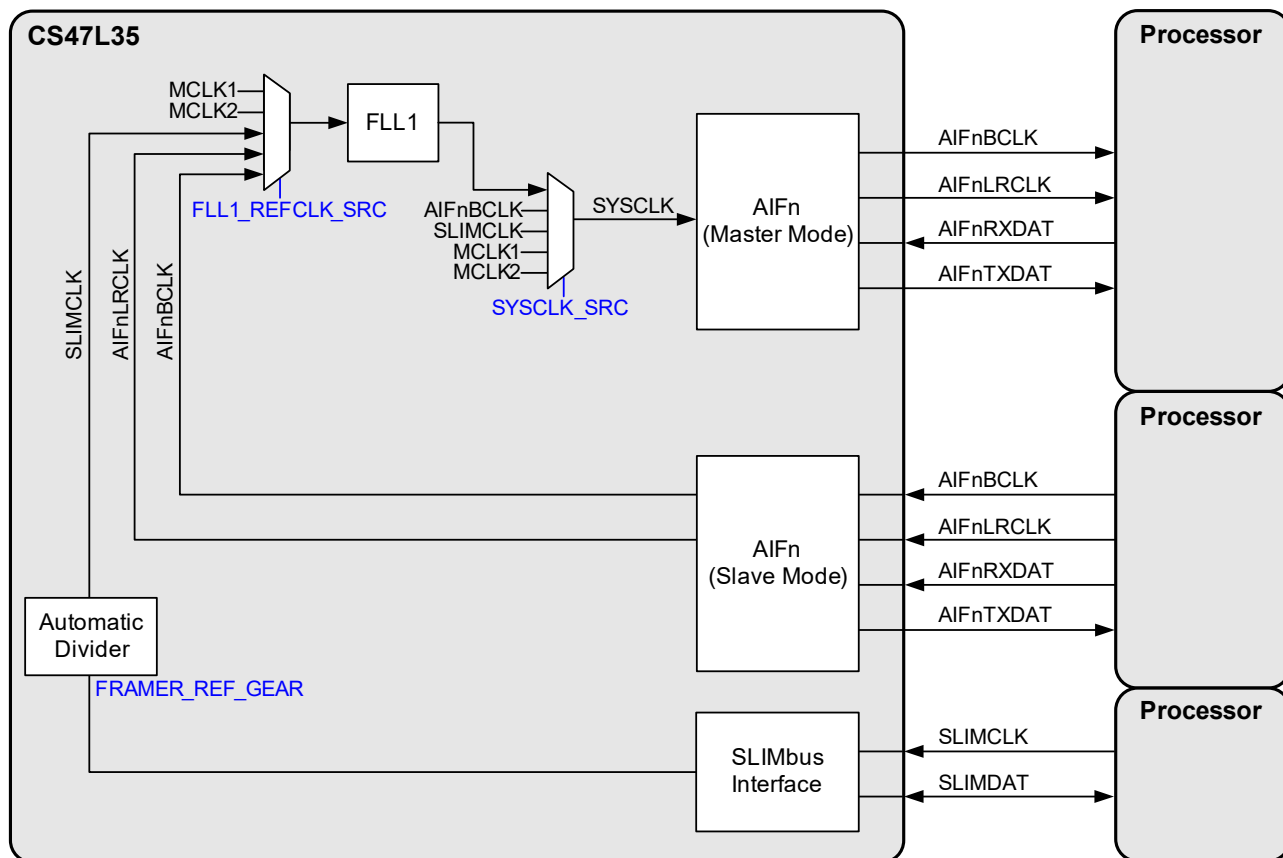
**Figure 5-13. AIF Master Mode, Using MCLK as Reference**

Fig. 5-14 shows AIF Master Mode operation, using MCLK as the clock reference. In this example, the FLL is used to generate the system clock, with MCLK as the reference.



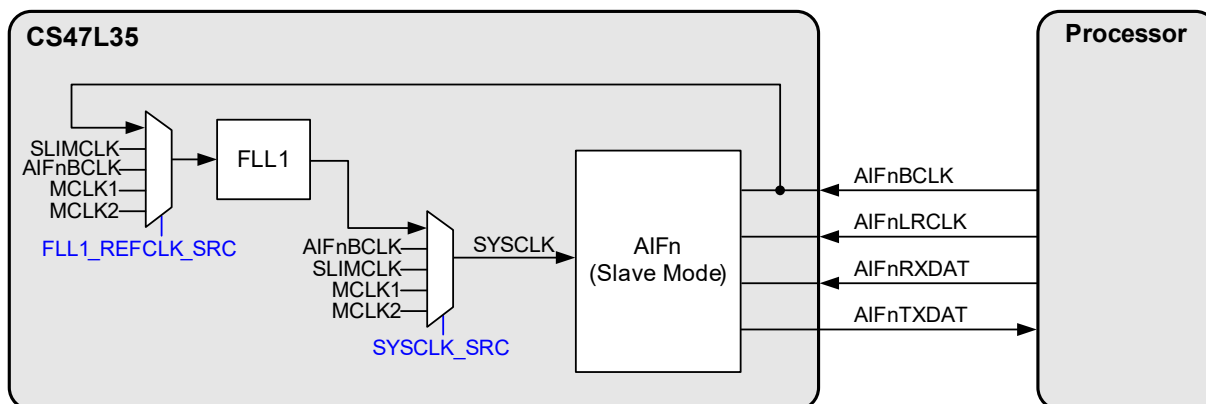
**Figure 5-14. AIF Master Mode, Using MCLK and FLL as Reference**

Fig. 5-15 shows AIF Master Mode operation, using a separate interface as the clock reference. In this example, the FLL is used to generate the system clock, with SLIMCLK as the reference.



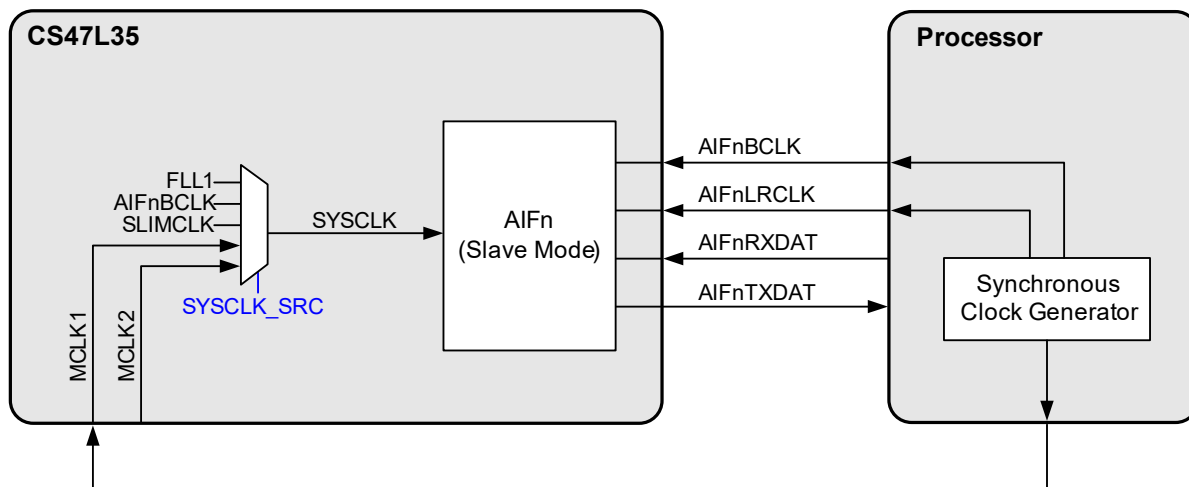
**Figure 5-15. AIF Master Mode, Using Another Interface as Reference**

Fig. 5-16 shows AIF Slave Mode operation, using BCLK as the clock reference. In this example, the FLL is used to generate the system clock, with BCLK as the reference.



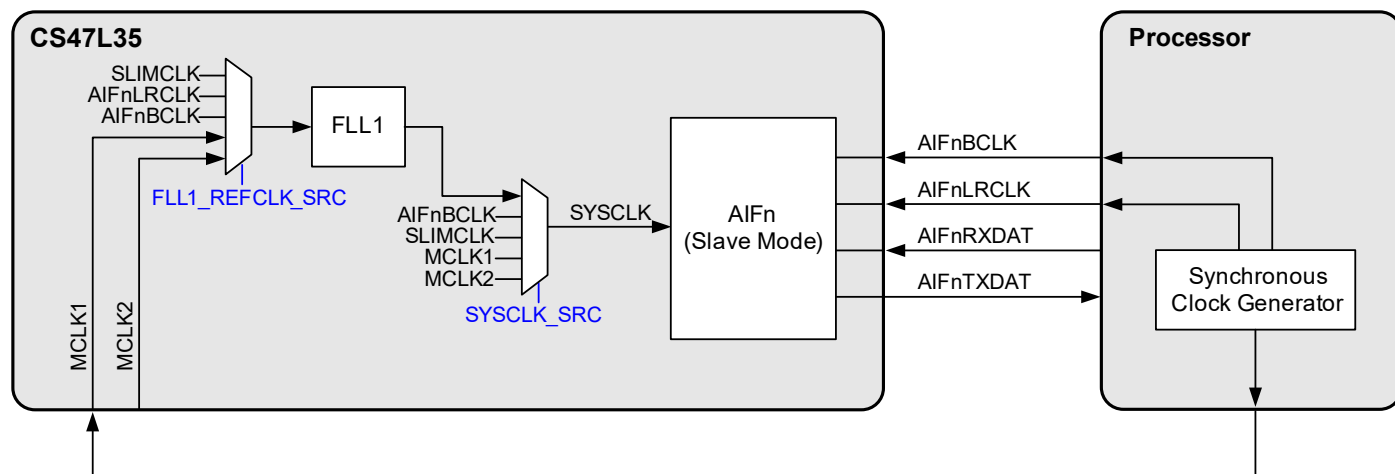
**Figure 5-16. AIF Slave Mode, Using BCLK and FLL as Reference**

Fig. 5-17 shows AIF Slave Mode operation, using MCLK as the clock reference. For correct operation, the MCLK input must be fully synchronized to the audio interface.



**Figure 5-17. AIF Slave Mode, Using MCLK as Reference**

Fig. 5-18 shows AIF Slave Mode operation, using MCLK as the clock reference. For correct operation, the MCLK input must be fully synchronized to the audio interface. In this example, the FLL is used to generate the system clock, with MCLK as the reference.



**Figure 5-18. AIF Slave Mode, Using MCLK and FLL as Reference**

Fig. 5-19 shows AIF Slave Mode operation, using a separate interface as the clock reference. In this example, the FLL is used to generate the system clock, with SLIMCLK as the reference. For correct operation, the SLIMCLK input must be fully synchronized to the other audio interfaces.

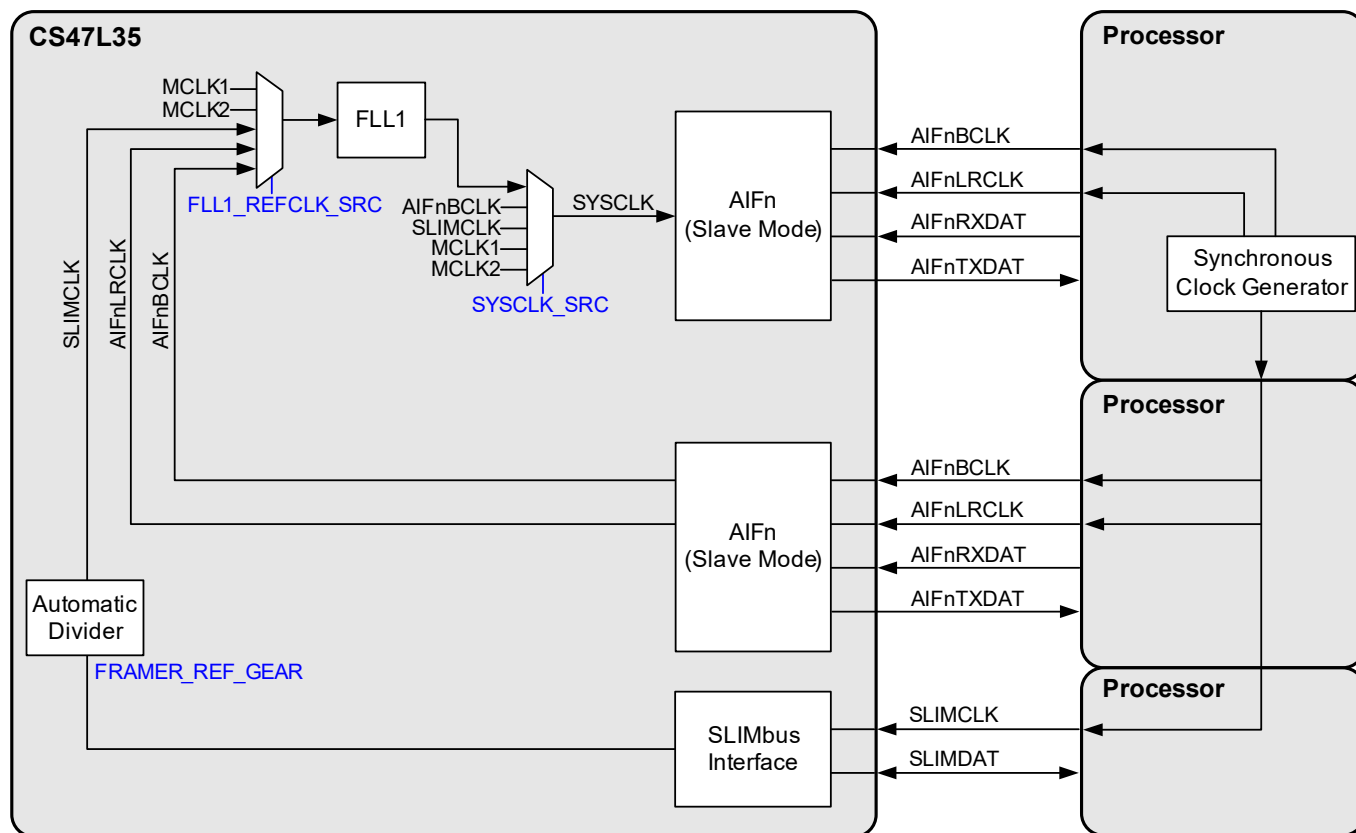


Figure 5-19. AIF Slave Mode, Using Another Interface as Reference

## 5.5 PCB Layout Considerations

Poor PCB layout degrades the performance and is a contributory factor in EMI, ground bounce, and resistive voltage losses. All external components should be placed as close to the CS47L35 device as possible, with current loop areas kept as small as possible.

## 6 Register Map

The CS47L35 control registers are listed in the following tables. Note that only the register addresses described here should be accessed; writing to other addresses may result in undefined behavior. Register bits that are not documented should not be changed from the default values.

The CS47L35 register map is defined in two regions:

- The codec register space (below 0x3000) is defined in 16-bit word format
- The DSP register space (from 0x3000 upwards) is defined in 32-bit word format

It is important to ensure that all control interface register operations use the applicable data word format, in accordance with the applicable register addresses.

The 16-bit codec register space is described in [Table 6-1](#).

**Table 6-1. Register Map Definition—16-bit region**

| Register      | Name                                 | 15                   | 14              | 13         | 12         | 11         | 10                | 9                 | 8                                     | 7                        | 6                        | 5         | 4         | 3         | 2         | 1               | 0             | Default |
|---------------|--------------------------------------|----------------------|-----------------|------------|------------|------------|-------------------|-------------------|---------------------------------------|--------------------------|--------------------------|-----------|-----------|-----------|-----------|-----------------|---------------|---------|
| R0<br>(0h)    | Software_Reset                       | SW_RST_DEV_ID [15:0] |                 |            |            |            |                   |                   |                                       |                          |                          |           |           |           |           |                 |               | 6360h   |
| R1<br>(1h)    | Hardware_Revision                    | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | 0                                     | HW_REVISION [7:0]        |                          |           |           |           |           |                 |               | 0000h   |
| R2<br>(2h)    | Software_Revision                    | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | 0                                     | SW_REVISION [7:0]        |                          |           |           |           |           |                 |               | 0000h   |
| R8<br>(8h)    | Ctrl_IF_CFG_1                        | 0                    | 0               | 0          | 0          | 0          | 0                 | 1                 | CIF1MISO_DRV_STR                      | CIF1MISO_PD              | 0                        | 0         | 0         | 1         | 0         | 0               | 0             | 0308h   |
| R9<br>(9h)    | Ctrl_IF_CFG_2                        | 0                    | 0               | 0          | 0          | 0          | 0                 | CIF2SDA_DRV_STR   | 0                                     | 0                        | 0                        | 0         | 0         | 0         | 0         | 0               | 0             | 0200h   |
| R22<br>(16h)  | Write_Sequencer_Ctrl_0               | 0                    | 0               | 0          | 0          | WSEQ_ABORT | WSEQ_START        | WSEQ_ENA          | WSEQ_START_INDEX [8:0]                |                          |                          |           |           |           |           |                 | 0000h         |         |
| R23<br>(17h)  | Write_Sequencer_Ctrl_1               | 0                    | 0               | 0          | 0          | 0          | 0                 | WSEQ_BUSY         | WSEQ_CURRENT_INDEX [8:0]              |                          |                          |           |           |           |           |                 | 0000h         |         |
| R24<br>(18h)  | Write_Sequencer_Ctrl_2               | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | 0                                     | 0                        | 0                        | 0         | 0         | 0         | 0         | WSEQ_BOOT_START | WSEQ_LOAD_MEM | 0000h   |
| R32<br>(20h)  | Tone_Generator_1                     | 0                    | TONE_RATE [3:0] |            |            |            | 0                 | TONE_OFFSET [1:0] |                                       | 0                        | 0                        | TONE2_OVD | TONE1_OVD | 0         | 0         | TONE2_ENA       | TONE1_ENA     | 0000h   |
| R33<br>(21h)  | Tone_Generator_2                     | TONE1_LVL [23:8]     |                 |            |            |            |                   |                   |                                       |                          |                          |           |           |           |           |                 |               | 1000h   |
| R34<br>(22h)  | Tone_Generator_3                     | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | 0                                     | TONE1_LVL [7:0]          |                          |           |           |           |           |                 |               | 0000h   |
| R35<br>(23h)  | Tone_Generator_4                     | TONE2_LVL [23:8]     |                 |            |            |            |                   |                   |                                       |                          |                          |           |           |           |           |                 |               | 1000h   |
| R36<br>(24h)  | Tone_Generator_5                     | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | 0                                     | TONE2_LVL [7:0]          |                          |           |           |           |           |                 |               | 0000h   |
| R48<br>(30h)  | PWM_Drive_1                          | 0                    | PWM_RATE [3:0]  |            |            |            | PWM_CLK_SEL [2:0] |                   |                                       | 0                        | 0                        | PWM2_OVD  | PWM1_OVD  | 0         | 0         | PWM2_ENA        | PWM1_ENA      | 0000h   |
| R49<br>(31h)  | PWM_Drive_2                          | 0                    | 0               | 0          | 0          | 0          | 0                 | PWM1_LVL [9:0]    |                                       |                          |                          |           |           |           |           |                 |               | 0100h   |
| R50<br>(32h)  | PWM_Drive_3                          | 0                    | 0               | 0          | 0          | 0          | 0                 | PWM2_LVL [9:0]    |                                       |                          |                          |           |           |           |           |                 |               | 0100h   |
| R65<br>(41h)  | Sequence_Control                     | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | 0                                     | WSEQ_ENA_MICD_CLAMP_FALL | WSEQ_ENA_MICD_CLAMP_RISE | 0         | 0         | 0         | 0         | 0               | 0             | 0000h   |
| R66<br>(42h)  | Spare_Triggers                       | WSEQ_TRG16           | WSEQ_TRG15      | WSEQ_TRG14 | WSEQ_TRG13 | WSEQ_TRG12 | WSEQ_TRG11        | WSEQ_TRG10        | WSEQ_TRG9                             | WSEQ_TRG8                | WSEQ_TRG7                | WSEQ_TRG6 | WSEQ_TRG5 | WSEQ_TRG4 | WSEQ_TRG3 | WSEQ_TRG2       | WSEQ_TRG1     | 0000h   |
| R75<br>(4Bh)  | Spare_Sequence_Select_1              | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_TRG1_INDEX [8:0]                 |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R76<br>(4Ch)  | Spare_Sequence_Select_2              | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_TRG2_INDEX [8:0]                 |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R77<br>(4Dh)  | Spare_Sequence_Select_3              | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_TRG3_INDEX [8:0]                 |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R78<br>(4Eh)  | Spare_Sequence_Select_4              | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_TRG4_INDEX [8:0]                 |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R79<br>(4Fh)  | Spare_Sequence_Select_5              | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_TRG5_INDEX [8:0]                 |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R80<br>(50h)  | Spare_Sequence_Select_6              | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_TRG6_INDEX [8:0]                 |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R89<br>(59h)  | Spare_Sequence_Select_7              | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_TRG7_INDEX [8:0]                 |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R90<br>(5Ah)  | Spare_Sequence_Select_8              | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_TRG8_INDEX [8:0]                 |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R91<br>(5Bh)  | Spare_Sequence_Select_9              | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_TRG9_INDEX [8:0]                 |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R92<br>(5Ch)  | Spare_Sequence_Select_10             | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_TRG10_INDEX [8:0]                |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R93<br>(5Dh)  | Spare_Sequence_Select_11             | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_TRG11_INDEX [8:0]                |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R94<br>(5Eh)  | Spare_Sequence_Select_12             | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_TRG12_INDEX [8:0]                |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R97<br>(61h)  | Sample_Rate_Sequence_Select_1        | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_SAMPLE_RATE_DETECT_A_INDEX [8:0] |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R98<br>(62h)  | Sample_Rate_Sequence_Select_2        | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_SAMPLE_RATE_DETECT_B_INDEX [8:0] |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R99<br>(63h)  | Sample_Rate_Sequence_Select_3        | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_SAMPLE_RATE_DETECT_C_INDEX [8:0] |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R100<br>(64h) | Sample_Rate_Sequence_Select_4        | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_SAMPLE_RATE_DETECT_D_INDEX [8:0] |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R102<br>(66h) | Always_On Triggers_Sequence_Select_1 | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_MICD_CLAMP_RISE_INDEX [8:0]      |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R103<br>(67h) | Always_On Triggers_Sequence_Select_2 | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_MICD_CLAMP_FALL_INDEX [8:0]      |                          |                          |           |           |           |           |                 | 01FFh         |         |
| R104<br>(68h) | Spare_Sequence_Select_13             | 0                    | 0               | 0          | 0          | 0          | 0                 | 0                 | WSEQ_TRG13_INDEX [8:0]                |                          |                          |           |           |           |           |                 | 01FFh         |         |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register    | Name                       | 15                | 14                   | 13 | 12 | 11 | 10                       | 9            | 8                                  | 7                      | 6           | 5 | 4                          | 3                    | 2               | 1                 | 0            | Default |       |
|-------------|----------------------------|-------------------|----------------------|----|----|----|--------------------------|--------------|------------------------------------|------------------------|-------------|---|----------------------------|----------------------|-----------------|-------------------|--------------|---------|-------|
| R105 (69h)  | Spare_Sequence_Select_14   | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | WSEQ_TRG14_INDEX [8:0]             |                        |             |   |                            |                      |                 |                   |              | 01FFh   |       |
| R106 (6Ah)  | Spare_Sequence_Select_15   | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | WSEQ_TRG15_INDEX [8:0]             |                        |             |   |                            |                      |                 |                   |              | 01FFh   |       |
| R107 (6Bh)  | Spare_Sequence_Select_16   | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | WSEQ_TRG16_INDEX [8:0]             |                        |             |   |                            |                      |                 |                   |              | 01FFh   |       |
| R110 (6Eh)  | Trigger_Sequence_Select_32 | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | WSEQ_DRC1_SIG_DET_RISE_INDEX [8:0] |                        |             |   |                            |                      |                 |                   |              | 01FFh   |       |
| R111 (6Fh)  | Trigger_Sequence_Select_33 | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | WSEQ_DRC1_SIG_DET_FALL_INDEX [8:0] |                        |             |   |                            |                      |                 |                   |              | 01FFh   |       |
| R120 (78h)  | Eventlog_Sequence_Select_1 | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | WSEQ_EVENTLOG1_INDEX [8:0]         |                        |             |   |                            |                      |                 |                   |              | 01FFh   |       |
| R121 (79h)  | Eventlog_Sequence_Select_2 | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | WSEQ_EVENTLOG2_INDEX [8:0]         |                        |             |   |                            |                      |                 |                   |              | 01FFh   |       |
| R122 (7Ah)  | Eventlog_Sequence_Select_3 | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | WSEQ_EVENTLOG3_INDEX [8:0]         |                        |             |   |                            |                      |                 |                   |              | 01FFh   |       |
| R123 (7Bh)  | Eventlog_Sequence_Select_4 | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | WSEQ_EVENTLOG4_INDEX [8:0]         |                        |             |   |                            |                      |                 |                   |              | 01FFh   |       |
| R144 (90h)  | Haptics_Control_1          | 0                 | HAP_RATE [3:0]       |    |    |    | 0                        | 0            | 0                                  | 0                      | 0           | 0 | ONESHOT_TRIG               | HAP_CTRL [1:0]       |                 | HAP_ACT           | 0            | 0000h   |       |
| R145 (91h)  | Haptics_Control_2          | 0                 | LRA_FREQ [14:0]      |    |    |    |                          |              |                                    |                        |             |   |                            |                      |                 |                   |              | 7FFFh   |       |
| R146 (92h)  | Haptics_phase_1_intensity  | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | PHASE1_INTENSITY [7:0] |             |   |                            |                      |                 |                   |              | 0000h   |       |
| R147 (93h)  | Haptics_phase_1_duration   | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | PHASE1_DURATION [8:0]              |                        |             |   |                            |                      |                 |                   | 0000h        |         |       |
| R148 (94h)  | Haptics_phase_2_intensity  | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | PHASE2_INTENSITY [7:0] |             |   |                            |                      |                 |                   |              | 0000h   |       |
| R149 (95h)  | Haptics_phase_2_duration   | 0                 | 0                    | 0  | 0  | 0  | PHASE2_DURATION [10:0]   |              |                                    |                        |             |   |                            |                      | 0000h           |                   |              |         |       |
| R150 (96h)  | Haptics_phase_3_intensity  | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | PHASE3_INTENSITY [7:0] |             |   |                            |                      |                 |                   |              | 0000h   |       |
| R151 (97h)  | Haptics_phase_3_duration   | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | PHASE3_DURATION [8:0]              |                        |             |   |                            |                      |                 |                   | 0000h        |         |       |
| R152 (98h)  | Haptics_Status             | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | 0                      | 0           | 0 | 0                          | 0                    | 0               | 0                 | ONESHOT_STS  | 0000h   |       |
| R160 (A0h)  | Comfort_Noise_Generator    | 0                 | NOISE_GEN_RATE [3:0] |    |    |    | 0                        | 0            | 0                                  | 0                      | 0           | 0 | NOISE_GEN_ENA              | NOISE_GEN_GAIN [4:0] |                 |                   |              |         | 0000h |
| R256 (100h) | Clock_32k_1                | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | 0                      | CLK_32K_ENA | 0 | 0                          | 0                    | 0               | CLK_32K_SRC [1:0] |              | 0002h   |       |
| R257 (101h) | System_Clock_1             | SYSCLK_FRAC       | 0                    | 0  | 0  | 0  | SYSCLK_FREQ [2:0]        |              |                                    | 0                      | SYSCLK_ENA  | 0 | 0                          | SYSCLK_SRC [3:0]     |                 |                   |              | 0404h   |       |
| R258 (102h) | Sample_rate_1              | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | 0                      | 0           | 0 | SAMPLE_RATE_1 [4:0]        |                      |                 |                   |              | 0011h   |       |
| R259 (103h) | Sample_rate_2              | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | 0                      | 0           | 0 | SAMPLE_RATE_2 [4:0]        |                      |                 |                   |              | 0011h   |       |
| R260 (104h) | Sample_rate_3              | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | 0                      | 0           | 0 | SAMPLE_RATE_3 [4:0]        |                      |                 |                   |              | 0011h   |       |
| R266 (10Ah) | Sample_rate_1_status       | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | 0                      | 0           | 0 | SAMPLE_RATE_1_STS [4:0]    |                      |                 |                   |              | 0000h   |       |
| R267 (10Bh) | Sample_rate_2_status       | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | 0                      | 0           | 0 | SAMPLE_RATE_2_STS [4:0]    |                      |                 |                   |              | 0000h   |       |
| R268 (10Ch) | Sample_rate_3_status       | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | 0                      | 0           | 0 | SAMPLE_RATE_3_STS [4:0]    |                      |                 |                   |              | 0000h   |       |
| R288 (120h) | DSP_Clock_1                | 0                 | 0                    | 0  | 0  | 0  | DSP_CLK_FREQ_RANGE [2:0] |              |                                    | 0                      | DSP_CLK_ENA | 0 | 0                          | DSP_CLK_SRC [3:0]    |                 |                   |              | 0305h   |       |
| R329 (149h) | Output_system_clock        | OPCLK_ENA         | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | OPCLK_DIV [4:0]        |             |   |                            |                      | OPCLK_SEL [2:0] |                   |              |         | 0000h |
| R334 (14Eh) | Clock_Gen_Pad_Ctrl         | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | MCLK2_PD                           | MCLK1_PD               | 0           | 0 | 0                          | 0                    | 0               | 0                 | 0            | 0000h   |       |
| R338 (152h) | Rate_Estimator_1           | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | 0                      | 0           | 0 | TRIG_ON_STARTUP            | LRCLK_SRC [2:0]      |                 |                   | RATE_EST_ENA | 0000h   |       |
| R339 (153h) | Rate_Estimator_2           | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | 0                      | 0           | 0 | SAMPLE_RATE_DETECT_A [4:0] |                      |                 |                   |              | 0000h   |       |
| R340 (154h) | Rate_Estimator_3           | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | 0                      | 0           | 0 | SAMPLE_RATE_DETECT_B [4:0] |                      |                 |                   |              | 0000h   |       |
| R341 (155h) | Rate_Estimator_4           | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | 0                      | 0           | 0 | SAMPLE_RATE_DETECT_C [4:0] |                      |                 |                   |              | 0000h   |       |
| R342 (156h) | Rate_Estimator_5           | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | 0                      | 0           | 0 | SAMPLE_RATE_DETECT_D [4:0] |                      |                 |                   |              | 0000h   |       |
| R369 (171h) | FLL1_Control_1             | 0                 | 0                    | 0  | 0  | 0  | 0                        | 0            | 0                                  | 0                      | 0           | 0 | 0                          | 0                    | 0               | FLL1_FREERUN      | FLL1_ENA     | 0002h   |       |
| R370 (172h) | FLL1_Control_2             | FLL1_CTRL_UPD     | 0                    | 0  | 0  | 0  | 0                        | FLL1_N [9:0] |                                    |                        |             |   |                            |                      |                 |                   |              | 0008h   |       |
| R371 (173h) | FLL1_Control_3             | FLL1_THETA [15:0] |                      |    |    |    |                          |              |                                    |                        |             |   |                            |                      |                 |                   |              | 0018h   |       |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register    | Name                    | 15                        | 14            | 13          | 12 | 11                        | 10                       | 9                    | 8               | 7                      | 6                   | 5                    | 4                            | 3                      | 2             | 1                 | 0              | Default |
|-------------|-------------------------|---------------------------|---------------|-------------|----|---------------------------|--------------------------|----------------------|-----------------|------------------------|---------------------|----------------------|------------------------------|------------------------|---------------|-------------------|----------------|---------|
| R372 (174h) | FLL1_Control_4          | FLL1_LAMBDA [15:0]        |               |             |    |                           |                          |                      |                 |                        |                     |                      |                              |                        |               |                   |                | 007Dh   |
| R373 (175h) | FLL1_Control_5          | 0                         | 0             | 0           | 0  | FLL1_FRATIO [3:0]         |                          |                      |                 | 0                      | 0                   | 0                    | 0                            | 0                      | 0             | 0                 | 0              | 0000h   |
| R374 (176h) | FLL1_Control_6          | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | FLL1_REFCLK_DIV [1:0]  |                     | 0                    | 0                            | FLL1_REFCLK_SRC [3:0]  |               |                   |                | 0000h   |
| R375 (177h) | FLL1_Loop_Filter_Test_1 | FLL1_FRC_INTEG_UPD        | 0             | 0           | 0  | FLL1_FRC_INTEG_VAL [11:0] |                          |                      |                 |                        |                     |                      |                              |                        |               |                   |                | 0281h   |
| R376 (178h) | FLL1_NCO_Test_0         | FLL1_INTEG_VALID          | 0             | 0           | 0  | FLL1_INTEG [11:0]         |                          |                      |                 |                        |                     |                      |                              |                        |               |                   |                | 0000h   |
| R377 (179h) | FLL1_Control_7          | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | 0                      | 0                   | FLL1_GAIN [3:0]      |                              |                        |               | 0                 | 0              | 0000h   |
| R378 (17Ah) | FLL1_Control_8          | FLL1_PHASE_GAIN[3:0]      |               |             |    | FLL1_PHASE_ENA            | FLL1_CTRL_RATE[2:0]      |                      |                 | 0                      | 0                   | 0                    | 0                            | 0                      | 1             | 1                 | 0              | 2906h   |
| R383 (17Fh) | FLL1_Synchroniser_1     | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | 0                      | 0                   | 0                    | 0                            | 0                      | 0             | 0                 | FLL1_SYNC_ENA  | 0000h   |
| R384 (180h) | FLL1_Synchroniser_2     | 0                         | 0             | 0           | 0  | 0                         | 0                        | FLL1_SYNC_N [9:0]    |                 |                        |                     |                      |                              |                        |               |                   |                | 0000h   |
| R385 (181h) | FLL1_Synchroniser_3     | FLL1_SYNC_THETA [15:0]    |               |             |    |                           |                          |                      |                 |                        |                     |                      |                              |                        |               |                   |                | 0000h   |
| R386 (182h) | FLL1_Synchroniser_4     | FLL1_SYNC_LAMBDA [15:0]   |               |             |    |                           |                          |                      |                 |                        |                     |                      |                              |                        |               |                   |                | 0000h   |
| R387 (183h) | FLL1_Synchroniser_5     | 0                         | 0             | 0           | 0  | 0                         | FLL1_SYNC_FRATIO [2:0]   |                      |                 | 0                      | 0                   | 0                    | 0                            | 0                      | 0             | 0                 | 0              | 0000h   |
| R388 (184h) | FLL1_Synchroniser_6     | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | FLL1_SYNCCLK_DIV [1:0] |                     | 0                    | 0                            | FLL1_SYNCCLK_SRC [3:0] |               |                   |                | 0000h   |
| R389 (185h) | FLL1_Synchroniser_7     | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | 0                      | 0                   | FLL1_SYNC_GAIN [3:0] |                              |                        | 0             | FLL1_SYNC_DFSAT   | 0001h          |         |
| R391 (187h) | FLL1_Spread_Spectrum    | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | 0                      | 0                   | FLL1_SS_AMPL [1:0]   |                              | FLL1_SS_FREQ [1:0]     |               | FLL1_SS_SEL [1:0] |                | 0000h   |
| R392 (188h) | FLL1_GPIO_Clock         | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | FLL1_GPCLK_DIV [6:0]   |                     |                      |                              |                        |               |                   | FLL1_GPCLK_ENA | 000Ch   |
| R512 (200h) | Mic_Charge_Pump_1       | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | 0                      | 0                   | 0                    | 0                            | 0                      | CP2_DISCH     | CP2_BYPASS        | CP2_ENA        | 0006h   |
| R531 (213h) | LDO2_Control_1          | 0                         | 0             | 0           | 0  | 0                         | LDO2_VSEL [5:0]          |                      |                 |                        |                     | 0                    | 0                            | LDO2_DISCH             | 0             | 0                 | 03E4h          |         |
| R536 (218h) | Mic_Bias_Ctrl_1         | MICB1_EXT_CAP             | 0             | 0           | 0  | 0                         | 0                        | 0                    | MICB1_LVL [3:0] |                        |                     |                      | 0                            | MICB1_RATE             | MICB1_DISCH   | MICB1_BYPASS      | MICB1_ENA      | 00E6h   |
| R537 (219h) | Mic_Bias_Ctrl_2         | MICB2_EXT_CAP             | 0             | 0           | 0  | 0                         | 0                        | 0                    | MICB2_LVL [3:0] |                        |                     |                      | 0                            | MICB2_RATE             | MICB2_DISCH   | MICB2_BYPASS      | MICB2_ENA      | 00E6h   |
| R540 (21Ch) | Mic_Bias_Ctrl_5         | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | 0                      | 0                   | MICB1B_DISCH         | MICB1B_ENA                   | 0                      | 0             | MICB1A_DISCH      | MICB1A_ENA     | 0022h   |
| R542 (21Eh) | Mic_Bias_Ctrl_6         | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | 0                      | 0                   | MICB2B_DISCH         | MICB2B_ENA                   | 0                      | 0             | MICB2A_DISCH      | MICB2A_ENA     | 0022h   |
| R620 (26Ch) | SPK_Watchdog_1          | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | 0                      | 0                   | 0                    | SPK_SHUTDOWN_TIMER_SEL [3:0] |                        |               |                   | 0000h          |         |
| R659 (293h) | Accessory_Detect_Mode_1 | 0                         | 0             | ACCDDET_SRC | 0  | 0                         | 0                        | 0                    | 0               | 1                      | 0                   | 0                    | 0                            | ACCDDET_MODE [2:0]     |               |                   | 0080h          |         |
| R667 (29Bh) | Headphone_Detect_1      | 0                         | 0             | 0           | 0  | 0                         | HP_IMPEDANCE_RANGE [1:0] |                      | 0               | 0                      | 0                   | 0                    | HP_CLK_DIV [1:0]             |                        | HP_RATE [1:0] |                   | HP_POLL (M)    | 0000h   |
| R668 (29Ch) | Headphone_Detect_2      | HP_DONE                   | HP_LVL [14:0] |             |    |                           |                          |                      |                 |                        |                     |                      |                              |                        |               |                   |                | 0000h   |
| R669 (29Dh) | Headphone_Detect_3      | 0                         | 0             | 0           | 0  | 0                         | 0                        | HP_DACVAL [9:0]      |                 |                        |                     |                      |                              |                        |               |                   |                | 0000h   |
| R671 (29Fh) | Headphone_Detect_5      | 0                         | 0             | 0           | 0  | 0                         | 0                        | HP_DACVAL_DOWN [9:0] |                 |                        |                     |                      |                              |                        |               |                   |                | 0000h   |
| R675 (2A3h) | Mic_Detect_1            | MICD_BIAS_STARTTIME [3:0] |               |             |    | MICD_RATE [3:0]           |                          |                      |                 | 0                      | MICD_BIAS_SRC [2:0] |                      |                              | 0                      | 0             | MICD_DBTIME       | MICD_ENA       | 1102h   |
| R676 (2A4h) | Mic_Detect_2            | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | MICD_LVL_SEL [7:0]     |                     |                      |                              |                        |               |                   |                | 009Fh   |
| R677 (2A5h) | Mic_Detect_3            | 0                         | 0             | 0           | 0  | 0                         | MICD_LVL [8:0]           |                      |                 |                        |                     |                      |                              |                        | MICD_VALID    |                   | MICD_STS       | 0000h   |
| R683 (2ABh) | Mic_Detect_4            | MICDET_ADCVAL_DIFF [7:0]  |               |             |    |                           |                          |                      |                 | 0                      | MICDET_ADCVAL [6:0] |                      |                              |                        |               |                   |                | 0000h   |
| R710 (2C6h) | Micd_Clamp_control      | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | 0                      | 0                   | 0                    | MICD_CLAMP_OVD               | MICD_CLAMP_MODE [3:0]  |               |                   |                | 0010h   |
| R712 (2C8h) | GP_Switch_1             | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | 0                      | 0                   | 0                    | 0                            | 0                      | 0             | SW1_MODE [1:0]    |                | 0000h   |
| R723 (2D3h) | Jack_detect_analogue    | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | 0                      | 0                   | 0                    | 0                            | 0                      | 0             | JD2_ENA           | JD1_ENA        | 0000h   |
| R768 (300h) | Input_Enables           | 0                         | 0             | 0           | 0  | 0                         | 0                        | 0                    | 0               | 0                      | 0                   | 0                    | 0                            | IN2L_ENA               | IN2R_ENA      | IN1L_ENA          | IN1R_ENA       | 0000h   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register        | Name                  | 15       | 14             | 13         | 12                 | 11                     | 10            | 9             | 8                | 7                   | 6                 | 5                       | 4 | 3               | 2                 | 1                 | 0             | Default |  |
|-----------------|-----------------------|----------|----------------|------------|--------------------|------------------------|---------------|---------------|------------------|---------------------|-------------------|-------------------------|---|-----------------|-------------------|-------------------|---------------|---------|--|
| R769<br>(301h)  | Input_Enables_Status  | 0        | 0              | 0          | 0                  | 0                      | 0             | 0             | 0                | 0                   | 0                 | 0                       | 0 | IN2L_ENA_STS    | IN2R_ENA_STS      | IN1L_ENA_STS      | IN1R_ENA_STS  | 0000h   |  |
| R776<br>(308h)  | Input_Rate            | 0        | IN_RATE [3:0]  |            |                    |                        | 0             | 0             | 0                | 0                   | 0                 | 0                       | 0 | 0               | 0                 | 0                 | 0             | 0000h   |  |
| R777<br>(309h)  | Input_Volume_Ramp     | 0        | 0              | 0          | 0                  | 0                      | 0             | 0             | 0                | 0                   | IN_VD_RAMP [2:0]  |                         |   | 0               | IN_VI_RAMP [2:0]  |                   |               | 0022h   |  |
| R780<br>(30Ch)  | HPF_Control           | 0        | 0              | 0          | 0                  | 0                      | 0             | 0             | 0                | 0                   | 0                 | 0                       | 0 | 0               | IN_HPF_CUT [2:0]  |                   |               | 0002h   |  |
| R784<br>(310h)  | IN1L_Control          | IN1L_HPF | 0              | 0          | IN1_DMIC_SUP [1:0] |                        | IN1_MODE      | 0             | 0                | IN1L_PGA_VOL [6:0]  |                   |                         |   |                 |                   | 0                 |               | 0080h   |  |
| R785<br>(311h)  | ADC_Digital_Volume_1L | 0        | IN1L_SRC [1:0] |            | 0                  | 0                      | 0             | IN_VU         | IN1L_MUTE        | IN1L_VOL [7:0]      |                   |                         |   |                 |                   |                   |               | 0180h   |  |
| R786<br>(312h)  | DMIC1L_Control        | 0        | 0              | 0          | 0                  | 0                      | IN1_OSR [2:0] |               |                  | 0                   | 0                 | IN1L_DMIC_DLY [5:0]     |   |                 |                   |                   |               | 0500h   |  |
| R788<br>(314h)  | IN1R_Control          | IN1R_HPF | 0              | 0          | 0                  | 0                      | 0             | 0             | 0                | IN1R_PGA_VOL [6:0]  |                   |                         |   |                 |                   | 0                 |               | 0080h   |  |
| R789<br>(315h)  | ADC_Digital_Volume_1R | 0        | IN1R_SRC [1:0] |            | 0                  | 0                      | 0             | IN_VU         | IN1R_MUTE        | IN1R_VOL [7:0]      |                   |                         |   |                 |                   |                   |               | 0180h   |  |
| R790<br>(316h)  | DMIC1R_Control        | 0        | 0              | 0          | 0                  | 0                      | 0             | 0             | 0                | 0                   | 0                 | IN1R_DMIC_DLY [5:0]     |   |                 |                   |                   |               | 0000h   |  |
| R792<br>(318h)  | IN2L_Control          | IN2L_HPF | 0              | 0          | IN2_DMIC_SUP [1:0] |                        | IN2_MODE      | 0             | 0                | IN2L_PGA_VOL [6:0]  |                   |                         |   |                 |                   | 0                 |               | 0080h   |  |
| R793<br>(319h)  | ADC_Digital_Volume_2L | 0        | IN2L_SRC [1:0] |            | 0                  | 0                      | 0             | IN_VU         | IN2L_MUTE        | IN2L_VOL [7:0]      |                   |                         |   |                 |                   |                   |               | 0180h   |  |
| R794<br>(31Ah)  | DMIC2L_Control        | 0        | 0              | 0          | 0                  | 0                      | IN2_OSR [2:0] |               |                  | 0                   | 0                 | IN2L_DMIC_DLY [5:0]     |   |                 |                   |                   |               | 0500h   |  |
| R796<br>(31Ch)  | IN2R_Control          | IN2R_HPF | 0              | 0          | 0                  | 0                      | 0             | 0             | 0                | IN2R_PGA_VOL [6:0]  |                   |                         |   |                 |                   | 0                 |               | 0080h   |  |
| R797<br>(31Dh)  | ADC_Digital_Volume_2R | 0        | IN2R_SRC [1:0] |            | 0                  | 0                      | 0             | IN_VU         | IN2R_MUTE        | IN2R_VOL [7:0]      |                   |                         |   |                 |                   |                   |               | 0180h   |  |
| R798<br>(31Eh)  | DMIC2R_Control        | 0        | 0              | 0          | 0                  | 0                      | 0             | 0             | 0                | 0                   | 0                 | IN2R_DMIC_DLY [5:0]     |   |                 |                   |                   |               | 0000h   |  |
| R840<br>(348h)  | Dig_Mic_Pad_Ctrl      | 0        | 0              | 0          | 0                  | 0                      | 0             | 0             | 0                | 0                   | 0                 | 0                       | 0 | 0               | 0                 | DMICDAT2_PD       | DMICDAT1_PD   | 0000h   |  |
| R1024<br>(400h) | Output_Enables_1      | EP_SEL   | 0              | 0          | 0                  | 0                      | 0             | OUT5L_ENA     | OUT5R_ENA        | SPKOUTL_ENA         | 0                 | 0                       | 0 | 0               | 0                 | HP1L_ENA          | HP1R_ENA      | 0000h   |  |
| R1025<br>(401h) | Output_Status_1       | 0        | 0              | 0          | 0                  | 0                      | 0             | OUT5L_ENA_STS | OUT5R_ENA_STS    | OUT4L_ENA_STS       | 0                 | 0                       | 0 | 0               | 0                 | 0                 | 0             | 0000h   |  |
| R1030<br>(406h) | Raw_Output_Status_1   | 0        | 0              | 0          | 0                  | 0                      | 0             | 0             | 0                | 0                   | 0                 | 0                       | 0 | 0               | 0                 | OUT1L_ENA_STS     | OUT1R_ENA_STS | 0000h   |  |
| R1032<br>(408h) | Output_Rate_1         | 0        | OUT_RATE [3:0] |            |                    |                        | 0             | 0             | 0                | 0                   | 0                 | 0                       | 0 | 0               | 0                 | 0                 | 0             | 0000h   |  |
| R1033<br>(409h) | Output_Volume_Ramp    | 0        | 0              | 0          | 0                  | 0                      | 0             | 0             | 0                | 0                   | OUT_VD_RAMP [2:0] |                         |   | 0               | OUT_VI_RAMP [2:0] |                   |               | 0022h   |  |
| R1040<br>(410h) | Output_Path_Config_1L | 0        | 0              | 0          | OUT1_MONO          | 0                      | 0             | 0             | 0                | 1                   | 0                 | 0                       | 0 | 0               | 0                 | 0                 | 0             | 0080h   |  |
| R1041<br>(411h) | DAC_Digital_Volume_1L | 0        | 0              | 0          | 0                  | 0                      | 0             | OUT_VU        | OUT1L_MUTE       | OUT1L_VOL [7:0]     |                   |                         |   |                 |                   |                   |               | 0180h   |  |
| R1043<br>(413h) | Noise_Gate_Select_1L  | 0        | 0              | 0          | 0                  | OUT1L_NGATE_SRC [11:0] |               |               |                  |                     |                   |                         |   |                 |                   |                   |               | 0001h   |  |
| R1045<br>(415h) | DAC_Digital_Volume_1R | 0        | 0              | 0          | 0                  | 0                      | 0             | OUT_VU        | OUT1R_MUTE       | OUT1R_VOL [7:0]     |                   |                         |   |                 |                   |                   |               | 0180h   |  |
| R1047<br>(417h) | Noise_Gate_Select_1R  | 0        | 0              | 0          | 0                  | OUT1R_NGATE_SRC [11:0] |               |               |                  |                     |                   |                         |   |                 |                   |                   |               | 0002h   |  |
| R1065<br>(429h) | DAC_Digital_Volume_4L | 0        | 0              | 0          | 0                  | 0                      | 0             | OUT_VU        | OUT4L_MUTE       | OUT4L_VOL [7:0]     |                   |                         |   |                 |                   |                   |               | 0180h   |  |
| R1067<br>(42Bh) | Noise_Gate_Select_4L  | 0        | 0              | 0          | 0                  | OUT4L_NGATE_SRC [11:0] |               |               |                  |                     |                   |                         |   |                 |                   |                   |               | 0040h   |  |
| R1072<br>(430h) | Output_Path_Config_5L | 0        | 0              | OUT5_OSR   | 0                  | 0                      | 0             | 0             | 0                | 0                   | 0                 | 0                       | 0 | 0               | 0                 | 0                 | 0             | 0000h   |  |
| R1073<br>(431h) | DAC_Digital_Volume_5L | 0        | 0              | 0          | 0                  | 0                      | 0             | OUT_VU        | OUT5L_MUTE       | OUT5L_VOL [7:0]     |                   |                         |   |                 |                   |                   |               | 0180h   |  |
| R1075<br>(433h) | Noise_Gate_Select_5L  | 0        | 0              | 0          | 0                  | OUT5L_NGATE_SRC [11:0] |               |               |                  |                     |                   |                         |   |                 |                   |                   |               | 0100h   |  |
| R1077<br>(435h) | DAC_Digital_Volume_5R | 0        | 0              | 0          | 0                  | 0                      | 0             | OUT_VU        | OUT5R_MUTE       | OUT5R_VOL [7:0]     |                   |                         |   |                 |                   |                   |               | 0180h   |  |
| R1079<br>(437h) | Noise_Gate_Select_5R  | 0        | 0              | 0          | 0                  | OUT5R_NGATE_SRC [11:0] |               |               |                  |                     |                   |                         |   |                 |                   |                   |               | 0200h   |  |
| R1104<br>(450h) | DAC_AEC_Control_1     | 0        | 0              | 0          | 0                  | 0                      | 0             | 0             | 0                | 0                   | 0                 | AEC1_LOOPBACK_SRC [3:0] |   |                 | AEC1_ENA_STS      | AEC1_LOOPBACK_ENA | 0000h         |         |  |
| R1105<br>(451h) | DAC_AEC_Control_2     | 0        | 0              | 0          | 0                  | 0                      | 0             | 0             | 0                | 0                   | 0                 | AEC2_LOOPBACK_SRC [3:0] |   |                 | AEC2_ENA_STS      | AEC2_LOOPBACK_ENA | 0000h         |         |  |
| R1112<br>(458h) | Noise_Gate_Control    | 0        | 0              | 0          | 0                  | 0                      | 0             | 0             | 0                | 0                   | 0                 | NGATE_HOLD [1:0]        |   | NGATE_THR [2:0] |                   | NGATE_ENA         |               | 0000h   |  |
| R1168<br>(490h) | PDM_SPK1_CTRL_1       | 0        | 0              | SPK1R_MUTE | SPK1L_MUTE         | 0                      | 0             | 0             | SPK1_MUTE_ENDIAN | SPK1_MUTE_SEQ [7:0] |                   |                         |   |                 |                   |                   |               | 0069h   |  |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register        | Name               | 15 | 14              | 13              | 12               | 11 | 10 | 9 | 8 | 7                     | 6             | 5                  | 4                    | 3              | 2              | 1              | 0               | Default |       |
|-----------------|--------------------|----|-----------------|-----------------|------------------|----|----|---|---|-----------------------|---------------|--------------------|----------------------|----------------|----------------|----------------|-----------------|---------|-------|
| R1169<br>(491h) | PDM_SPK1_CTRL_2    | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | 0                  | 0                    | 0              | 0              | 0              | SPK1_FMT        | 0000h   |       |
| R1280<br>(500h) | AIF1_BCLK_Ctrl     | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | AIF1_BCLK_INV         | AIF1_BCLK_FRC | AIF1_BCLK_MSTR     | AIF1_BCLK_FREQ [4:0] |                |                |                |                 | 000Ch   |       |
| R1281<br>(501h) | AIF1_Tx_Pin_Ctrl   | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1TX_DAT_TRI     | 0                    | 0              | 0              | 0              | 0               | 0000h   |       |
| R1282<br>(502h) | AIF1_Rx_Pin_Ctrl   | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | 0                  | 0                    | AIF1_LRCLK_ADV | AIF1_LRCLK_INV | AIF1_LRCLK_FRC | AIF1_LRCLK_MSTR | 0000h   |       |
| R1283<br>(503h) | AIF1_Rate_Ctrl     | 0  | AIF1_RATE [3:0] |                 |                  |    | 0  | 0 | 0 | 0                     | AIF1_TRI      | 0                  | 0                    | 0              | 0              | 0              | 0               | 0000h   |       |
| R1284<br>(504h) | AIF1_Format        | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | 0                  | 0                    | 0              | AIF1_FMT [2:0] |                |                 | 0000h   |       |
| R1286<br>(506h) | AIF1_Rx_BCLK_Rate  | 0  | 0               | 0               | AIF1_BCPF [12:0] |    |    |   |   |                       |               |                    |                      |                |                |                |                 |         | 0040h |
| R1287<br>(507h) | AIF1_Frame_Ctrl_1  | 0  | 0               | AIF1TX_WL [5:0] |                  |    |    |   |   | AIF1TX_SLOT_LEN [7:0] |               |                    |                      |                |                |                |                 | 1818h   |       |
| R1288<br>(508h) | AIF1_Frame_Ctrl_2  | 0  | 0               | AIF1RX_WL [5:0] |                  |    |    |   |   | AIF1RX_SLOT_LEN [7:0] |               |                    |                      |                |                |                |                 | 1818h   |       |
| R1289<br>(509h) | AIF1_Frame_Ctrl_3  | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1TX1_SLOT [5:0] |                      |                |                |                | 0000h           |         |       |
| R1290<br>(50Ah) | AIF1_Frame_Ctrl_4  | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1TX2_SLOT [5:0] |                      |                |                |                | 0001h           |         |       |
| R1291<br>(50Bh) | AIF1_Frame_Ctrl_5  | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1TX3_SLOT [5:0] |                      |                |                |                | 0002h           |         |       |
| R1292<br>(50Ch) | AIF1_Frame_Ctrl_6  | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1TX4_SLOT [5:0] |                      |                |                |                | 0003h           |         |       |
| R1293<br>(50Dh) | AIF1_Frame_Ctrl_7  | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1TX5_SLOT [5:0] |                      |                |                |                | 0004h           |         |       |
| R1294<br>(50Eh) | AIF1_Frame_Ctrl_8  | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1TX6_SLOT [5:0] |                      |                |                |                | 0005h           |         |       |
| R1297<br>(511h) | AIF1_Frame_Ctrl_11 | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1RX1_SLOT [5:0] |                      |                |                |                | 0000h           |         |       |
| R1298<br>(512h) | AIF1_Frame_Ctrl_12 | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1RX2_SLOT [5:0] |                      |                |                |                | 0001h           |         |       |
| R1299<br>(513h) | AIF1_Frame_Ctrl_13 | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1RX3_SLOT [5:0] |                      |                |                |                | 0002h           |         |       |
| R1300<br>(514h) | AIF1_Frame_Ctrl_14 | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1RX4_SLOT [5:0] |                      |                |                |                | 0003h           |         |       |
| R1301<br>(515h) | AIF1_Frame_Ctrl_15 | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1RX5_SLOT [5:0] |                      |                |                |                | 0004h           |         |       |
| R1302<br>(516h) | AIF1_Frame_Ctrl_16 | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1RX6_SLOT [5:0] |                      |                |                |                | 0005h           |         |       |
| R1305<br>(519h) | AIF1_Tx_Enables    | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1TX6_ENA        | AIF1TX5_ENA          | AIF1TX4_ENA    | AIF1TX3_ENA    | AIF1TX2_ENA    | AIF1TX1_ENA     | 0000h   |       |
| R1306<br>(51Ah) | AIF1_Rx_Enables    | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF1RX6_ENA        | AIF1RX5_ENA          | AIF1RX4_ENA    | AIF1RX3_ENA    | AIF1RX2_ENA    | AIF1RX1_ENA     | 0000h   |       |
| R1344<br>(540h) | AIF2_BCLK_Ctrl     | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | AIF2_BCLK_INV         | AIF2_BCLK_FRC | AIF2_BCLK_MSTR     | AIF2_BCLK_FREQ [4:0] |                |                |                |                 | 000Ch   |       |
| R1345<br>(541h) | AIF2_Tx_Pin_Ctrl   | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF2TX_DAT_TRI     | 0                    | 0              | 0              | 0              | 0               | 0000h   |       |
| R1346<br>(542h) | AIF2_Rx_Pin_Ctrl   | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | 0                  | 0                    | AIF2_LRCLK_ADV | AIF2_LRCLK_INV | AIF2_LRCLK_FRC | AIF2_LRCLK_MSTR | 0000h   |       |
| R1347<br>(543h) | AIF2_Rate_Ctrl     | 0  | AIF2_RATE [3:0] |                 |                  |    | 0  | 0 | 0 | 0                     | AIF2_TRI      | 0                  | 0                    | 0              | 0              | 0              | 0               | 0       | 0000h |
| R1348<br>(544h) | AIF2_Format        | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | 0                  | 0                    | 0              | AIF2_FMT [2:0] |                |                 | 0000h   |       |
| R1350<br>(546h) | AIF2_Rx_BCLK_Rate  | 0  | 0               | 0               | AIF2_BCPF [12:0] |    |    |   |   |                       |               |                    |                      |                |                |                |                 |         | 0040h |
| R1351<br>(547h) | AIF2_Frame_Ctrl_1  | 0  | 0               | AIF2TX_WL [5:0] |                  |    |    |   |   | AIF2TX_SLOT_LEN [7:0] |               |                    |                      |                |                |                |                 | 1818h   |       |
| R1352<br>(548h) | AIF2_Frame_Ctrl_2  | 0  | 0               | AIF2RX_WL [5:0] |                  |    |    |   |   | AIF2RX_SLOT_LEN [7:0] |               |                    |                      |                |                |                |                 | 1818h   |       |
| R1353<br>(549h) | AIF2_Frame_Ctrl_3  | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF2TX1_SLOT [5:0] |                      |                |                |                | 0000h           |         |       |
| R1354<br>(54Ah) | AIF2_Frame_Ctrl_4  | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF2TX2_SLOT [5:0] |                      |                |                |                | 0001h           |         |       |
| R1361<br>(551h) | AIF2_Frame_Ctrl_11 | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF2RX1_SLOT [5:0] |                      |                |                |                | 0000h           |         |       |
| R1362<br>(552h) | AIF2_Frame_Ctrl_12 | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | AIF2RX2_SLOT [5:0] |                      |                |                |                | 0001h           |         |       |
| R1369<br>(559h) | AIF2_Tx_Enables    | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | 0                  | 0                    | 0              | 0              | AIF2TX2_ENA    | AIF2TX1_ENA     | 0000h   |       |
| R1370<br>(55Ah) | AIF2_Rx_Enables    | 0  | 0               | 0               | 0                | 0  | 0  | 0 | 0 | 0                     | 0             | 0                  | 0                    | 0              | 0              | AIF2RX2_ENA    | AIF2RX1_ENA     | 0000h   |       |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register        | Name                      | 15                 | 14                 | 13                      | 12               | 11                 | 10 | 9 | 8 | 7                     | 6                  | 5                       | 4                    | 3                      | 2                 | 1                | 0                | Default |
|-----------------|---------------------------|--------------------|--------------------|-------------------------|------------------|--------------------|----|---|---|-----------------------|--------------------|-------------------------|----------------------|------------------------|-------------------|------------------|------------------|---------|
| R1408<br>(580h) | AIF3_BCLK_Ctrl            | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | AIF3_BCLK_INV         | AIF3_BCLK_FRC      | AIF3_BCLK_MSTR          | AIF3_BCLK_FREQ [4:0] |                        |                   |                  |                  | 000Ch   |
| R1409<br>(581h) | AIF3_Tx_Pin_Ctrl          | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | AIF3TX_DAT_TRI          | 0                    | 0                      | 0                 | 0                | 0                | 0000h   |
| R1410<br>(582h) | AIF3_Rx_Pin_Ctrl          | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | 0                       | 0                    | AIF3_LRCLK_ADV         | AIF3_LRCLK_INV    | AIF3_LRCLK_FRC   | AIF3_LRCLK_MSTR  | 0000h   |
| R1411<br>(583h) | AIF3_Rate_Ctrl            | 0                  | AIF3_RATE [3:0]    |                         |                  |                    | 0  | 0 | 0 | 0                     | AIF3_TRI           | 0                       | 0                    | 0                      | 0                 | 0                | 0                | 0000h   |
| R1412<br>(584h) | AIF3_Format               | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | 0                       | 0                    | 0                      | AIF3_FMT [2:0]    |                  |                  | 0000h   |
| R1414<br>(586h) | AIF3_Rx_BCLK_Rate         | 0                  | 0                  | 0                       | AIF3_BCPF [12:0] |                    |    |   |   |                       |                    |                         |                      |                        |                   |                  |                  | 0040h   |
| R1415<br>(587h) | AIF3_Frame_Ctrl_1         | 0                  | 0                  | AIF3TX_WL [5:0]         |                  |                    |    |   |   | AIF3TX_SLOT_LEN [7:0] |                    |                         |                      |                        |                   | 1818h            |                  |         |
| R1416<br>(588h) | AIF3_Frame_Ctrl_2         | 0                  | 0                  | AIF3RX_WL [5:0]         |                  |                    |    |   |   | AIF3RX_SLOT_LEN [7:0] |                    |                         |                      |                        |                   | 1818h            |                  |         |
| R1417<br>(589h) | AIF3_Frame_Ctrl_3         | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | AIF3TX1_SLOT [5:0]      |                      |                        |                   |                  | 0000h            |         |
| R1418<br>(58Ah) | AIF3_Frame_Ctrl_4         | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | AIF3TX2_SLOT [5:0]      |                      |                        |                   |                  | 0001h            |         |
| R1425<br>(591h) | AIF3_Frame_Ctrl_11        | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | AIF3RX1_SLOT [5:0]      |                      |                        |                   |                  | 0000h            |         |
| R1426<br>(592h) | AIF3_Frame_Ctrl_12        | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | AIF3RX2_SLOT [5:0]      |                      |                        |                   |                  | 0001h            |         |
| R1433<br>(599h) | AIF3_Tx_Enables           | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | 0                       | 0                    | 0                      | 0                 | AIF3TX2_ENA      | AIF3TX1_ENA      | 0000h   |
| R1434<br>(59Ah) | AIF3_Rx_Enables           | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | 0                       | 0                    | 0                      | 0                 | AIF3RX2_ENA      | AIF3RX1_ENA      | 0000h   |
| R1474<br>(5C2h) | SPD1_TX_Control           | 0                  | 0                  | SPD1_VAL2               | SPD1_VAL1        | 0                  | 0  | 0 | 0 | SPD1_RATE [3:0]       |                    |                         |                      | 0                      | 0                 | 0                | SPD1_ENA         | 0000h   |
| R1475<br>(5C3h) | SPD1_TX_Channel_Status_1  | SPD1_CATCODE [7:0] |                    |                         |                  |                    |    |   |   | SPD1_CHSTMODE [1:0]   | SPD1_PREEMPH [2:0] |                         |                      | SPD1_NOCOPY            | SPD1_NOAUDIO      | SPD1_PRO         | 0000h            |         |
| R1476<br>(5C4h) | SPD1_TX_Channel_Status_2  | SPD1_FREQ [3:0]    |                    |                         |                  | SPD1_CHNUM2 [3:0]  |    |   |   | SPD1_CHNUM1 [3:0]     |                    |                         |                      | SPD1_SRCNUM [3:0]      |                   |                  |                  | 0001h   |
| R1477<br>(5C5h) | SPD1_TX_Channel_Status_3  | 0                  | 0                  | 0                       | 0                | SPD1_ORGSAMP [3:0] |    |   |   | SPD1_TXWL [2:0]       |                    | SPD1_MAXWL              | SPD1_CS31_30 [1:0]   |                        | SPD1_CLKACU [1:0] |                  | 0000h            |         |
| R1490<br>(5D2h) | SLIMbus_RX_Ports0         | 0                  | 0                  | SLIMRX2_PORT_ADDR [5:0] |                  |                    |    |   |   | 0                     | 0                  | SLIMRX1_PORT_ADDR [5:0] |                      |                        |                   |                  | 0100h            |         |
| R1491<br>(5D3h) | SLIMbus_RX_Ports1         | 0                  | 0                  | SLIMRX4_PORT_ADDR [5:0] |                  |                    |    |   |   | 0                     | 0                  | SLIMRX3_PORT_ADDR [5:0] |                      |                        |                   |                  | 0302h            |         |
| R1492<br>(5D4h) | SLIMbus_RX_Ports2         | 0                  | 0                  | SLIMRX6_PORT_ADDR [5:0] |                  |                    |    |   |   | 0                     | 0                  | SLIMRX5_PORT_ADDR [5:0] |                      |                        |                   |                  | 0504h            |         |
| R1494<br>(5D6h) | SLIMbus_TX_Ports0         | 0                  | 0                  | SLIMTX2_PORT_ADDR [5:0] |                  |                    |    |   |   | 0                     | 0                  | SLIMTX1_PORT_ADDR [5:0] |                      |                        |                   |                  | 0908h            |         |
| R1495<br>(5D7h) | SLIMbus_TX_Ports1         | 0                  | 0                  | SLIMTX4_PORT_ADDR [5:0] |                  |                    |    |   |   | 0                     | 0                  | SLIMTX3_PORT_ADDR [5:0] |                      |                        |                   |                  | 0B0Ah            |         |
| R1496<br>(5D8h) | SLIMbus_TX_Ports2         | 0                  | 0                  | SLIMTX6_PORT_ADDR [5:0] |                  |                    |    |   |   | 0                     | 0                  | SLIMTX5_PORT_ADDR [5:0] |                      |                        |                   |                  | 0D0Ch            |         |
| R1507<br>(5E3h) | SLIMbus_Framer_Ref_Gear   | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | 0                       | 0                    | SLIMCLK_REF_GEAR [3:0] |                   |                  |                  | 0000h   |
| R1509<br>(5E5h) | SLIMbus_Rates_1           | 0                  | SLIMRX2_RATE [3:0] |                         |                  |                    | 0  | 0 | 0 | 0                     | SLIMRX1_RATE [3:0] |                         |                      |                        | 0                 | 0                | 0                | 0000h   |
| R1510<br>(5E6h) | SLIMbus_Rates_2           | 0                  | SLIMRX4_RATE [3:0] |                         |                  |                    | 0  | 0 | 0 | 0                     | SLIMRX3_RATE [3:0] |                         |                      |                        | 0                 | 0                | 0                | 0000h   |
| R1511<br>(5E7h) | SLIMbus_Rates_3           | 0                  | SLIMRX6_RATE [3:0] |                         |                  |                    | 0  | 0 | 0 | 0                     | SLIMRX5_RATE [3:0] |                         |                      |                        | 0                 | 0                | 0                | 0000h   |
| R1513<br>(5E9h) | SLIMbus_Rates_5           | 0                  | SLIMTX2_RATE [3:0] |                         |                  |                    | 0  | 0 | 0 | 0                     | SLIMTX1_RATE [3:0] |                         |                      |                        | 0                 | 0                | 0                | 0000h   |
| R1514<br>(5EAh) | SLIMbus_Rates_6           | 0                  | SLIMTX4_RATE [3:0] |                         |                  |                    | 0  | 0 | 0 | 0                     | SLIMTX3_RATE [3:0] |                         |                      |                        | 0                 | 0                | 0                | 0000h   |
| R1515<br>(5EBh) | SLIMbus_Rates_7           | 0                  | SLIMTX6_RATE [3:0] |                         |                  |                    | 0  | 0 | 0 | 0                     | SLIMTX5_RATE [3:0] |                         |                      |                        | 0                 | 0                | 0                | 0000h   |
| R1520<br>(5F0h) | Slimbus_Pad_Ctrl          | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | 0                       | 0                    | 0                      | 0                 | SLIMDAT_DRV_STR  | SLIMCLK_DRV_STR  | 0003h   |
| R1525<br>(5F5h) | SLIMbus_RX_Channel_Enable | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | SLIMRX6_ENA             | SLIMRX5_ENA          | SLIMRX4_ENA            | SLIMRX3_ENA       | SLIMRX2_ENA      | SLIMRX1_ENA      | 0000h   |
| R1526<br>(5F6h) | SLIMbus_TX_Channel_Enable | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | SLIMTX6_ENA             | SLIMTX5_ENA          | SLIMTX4_ENA            | SLIMTX3_ENA       | SLIMTX2_ENA      | SLIMTX1_ENA      | 0000h   |
| R1527<br>(5F7h) | SLIMbus_RX_Port_Status    | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | SLIMRX6_PORT_STS        | SLIMRX5_PORT_STS     | SLIMRX4_PORT_STS       | SLIMRX3_PORT_STS  | SLIMRX2_PORT_STS | SLIMRX1_PORT_STS | 0000h   |
| R1528<br>(5F8h) | SLIMbus_TX_Port_Status    | 0                  | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | 0                     | 0                  | SLIMTX6_PORT_STS        | SLIMTX5_PORT_STS     | SLIMTX4_PORT_STS       | SLIMTX3_PORT_STS  | SLIMTX2_PORT_STS | SLIMTX1_PORT_STS | 0000h   |
| R1600<br>(640h) | PWM1MIX_Input_1_Source    | PWM1MIX_STS1       | 0                  | 0                       | 0                | 0                  | 0  | 0 | 0 | PWM1MIX_SRC1 [7:0]    |                    |                         |                      |                        |                   |                  |                  | 0000h   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register        | Name                    | 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |
|-----------------|-------------------------|---------------|----|----|----|----|----|---|---|---------------------|---|---|---|---|---|---|---|---------|
| R1601<br>(641h) | PWM1MIX_Input_1_Volume  | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM1MIX_VOL1 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R1602<br>(642h) | PWM1MIX_Input_2_Source  | PWM1MIX_STS2  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM1MIX_SRC2 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R1603<br>(643h) | PWM1MIX_Input_2_Volume  | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM1MIX_VOL2 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R1604<br>(644h) | PWM1MIX_Input_3_Source  | PWM1MIX_STS3  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM1MIX_SRC3 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R1605<br>(645h) | PWM1MIX_Input_3_Volume  | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM1MIX_VOL3 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R1606<br>(646h) | PWM1MIX_Input_4_Source  | PWM1MIX_STS4  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM1MIX_SRC4 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R1607<br>(647h) | PWM1MIX_Input_4_Volume  | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM1MIX_VOL4 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R1608<br>(648h) | PWM2MIX_Input_1_Source  | PWM2MIX_STS1  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM2MIX_SRC1 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R1609<br>(649h) | PWM2MIX_Input_1_Volume  | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM2MIX_VOL1 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R1610<br>(64Ah) | PWM2MIX_Input_2_Source  | PWM2MIX_STS2  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM2MIX_SRC2 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R1611<br>(64Bh) | PWM2MIX_Input_2_Volume  | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM2MIX_VOL2 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R1612<br>(64Ch) | PWM2MIX_Input_3_Source  | PWM2MIX_STS3  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM2MIX_SRC3 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R1613<br>(64Dh) | PWM2MIX_Input_3_Volume  | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM2MIX_VOL3 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R1614<br>(64Eh) | PWM2MIX_Input_4_Source  | PWM2MIX_STS4  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM2MIX_SRC4 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R1615<br>(64Fh) | PWM2MIX_Input_4_Volume  | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | PWM2MIX_VOL4 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R1664<br>(680h) | OUT1LMIX_Input_1_Source | OUT1LMIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1LMIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1665<br>(681h) | OUT1LMIX_Input_1_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1LMIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1666<br>(682h) | OUT1LMIX_Input_2_Source | OUT1LMIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1LMIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1667<br>(683h) | OUT1LMIX_Input_2_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1LMIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1668<br>(684h) | OUT1LMIX_Input_3_Source | OUT1LMIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1LMIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1669<br>(685h) | OUT1LMIX_Input_3_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1LMIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1670<br>(686h) | OUT1LMIX_Input_4_Source | OUT1LMIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1LMIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1671<br>(687h) | OUT1LMIX_Input_4_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1LMIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1672<br>(688h) | OUT1RMIX_Input_1_Source | OUT1RMIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1RMIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1673<br>(689h) | OUT1RMIX_Input_1_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1RMIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1674<br>(68Ah) | OUT1RMIX_Input_2_Source | OUT1RMIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1RMIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1675<br>(68Bh) | OUT1RMIX_Input_2_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1RMIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1676<br>(68Ch) | OUT1RMIX_Input_3_Source | OUT1RMIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1RMIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1677<br>(68Dh) | OUT1RMIX_Input_3_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1RMIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1678<br>(68Eh) | OUT1RMIX_Input_4_Source | OUT1RMIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1RMIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1679<br>(68Fh) | OUT1RMIX_Input_4_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT1RMIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1712<br>(6B0h) | OUT4LMIX_Input_1_Source | OUT4LMIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT4LMIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1713<br>(6B1h) | OUT4LMIX_Input_1_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT4LMIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1714<br>(6B2h) | OUT4LMIX_Input_2_Source | OUT4LMIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT4LMIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1715<br>(6B3h) | OUT4LMIX_Input_2_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT4LMIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1716<br>(6B4h) | OUT4LMIX_Input_3_Source | OUT4LMIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT4LMIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1717<br>(6B5h) | OUT4LMIX_Input_3_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT4LMIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1718<br>(6B6h) | OUT4LMIX_Input_4_Source | OUT4LMIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT4LMIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register        | Name                      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                     | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |
|-----------------|---------------------------|-----------------|----|----|----|----|----|---|---|-----------------------|---|---|---|---|---|---|---|---------|
| R1719<br>(6B7h) | OUT4LMIX_Input_4_Volume   | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT4LMIX_VOL4 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R1728<br>(6C0h) | OUT5LMIX_Input_1_Source   | OUT5LMIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5LMIX_SRC1 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R1729<br>(6C1h) | OUT5LMIX_Input_1_Volume   | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5LMIX_VOL1 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R1730<br>(6C2h) | OUT5LMIX_Input_2_Source   | OUT5LMIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5LMIX_SRC2 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R1731<br>(6C3h) | OUT5LMIX_Input_2_Volume   | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5LMIX_VOL2 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R1732<br>(6C4h) | OUT5LMIX_Input_3_Source   | OUT5LMIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5LMIX_SRC3 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R1733<br>(6C5h) | OUT5LMIX_Input_3_Volume   | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5LMIX_VOL3 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R1734<br>(6C6h) | OUT5LMIX_Input_4_Source   | OUT5LMIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5LMIX_SRC4 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R1735<br>(6C7h) | OUT5LMIX_Input_4_Volume   | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5LMIX_VOL4 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R1736<br>(6C8h) | OUT5RMIX_Input_1_Source   | OUT5RMIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5RMIX_SRC1 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R1737<br>(6C9h) | OUT5RMIX_Input_1_Volume   | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5RMIX_VOL1 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R1738<br>(6CAh) | OUT5RMIX_Input_2_Source   | OUT5RMIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5RMIX_SRC2 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R1739<br>(6CBh) | OUT5RMIX_Input_2_Volume   | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5RMIX_VOL2 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R1740<br>(6CCh) | OUT5RMIX_Input_3_Source   | OUT5RMIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5RMIX_SRC3 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R1741<br>(6CDh) | OUT5RMIX_Input_3_Volume   | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5RMIX_VOL3 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R1742<br>(6CEh) | OUT5RMIX_Input_4_Source   | OUT5RMIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5RMIX_SRC4 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R1743<br>(6CFh) | OUT5RMIX_Input_4_Volume   | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | OUT5RMIX_VOL4 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R1792<br>(700h) | AIF1TX1MIX_Input_1_Source | AIF1TX1MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX1MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1793<br>(701h) | AIF1TX1MIX_Input_1_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX1MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1794<br>(702h) | AIF1TX1MIX_Input_2_Source | AIF1TX1MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX1MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1795<br>(703h) | AIF1TX1MIX_Input_2_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX1MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1796<br>(704h) | AIF1TX1MIX_Input_3_Source | AIF1TX1MIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX1MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1797<br>(705h) | AIF1TX1MIX_Input_3_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX1MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1798<br>(706h) | AIF1TX1MIX_Input_4_Source | AIF1TX1MIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX1MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1799<br>(707h) | AIF1TX1MIX_Input_4_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX1MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1800<br>(708h) | AIF1TX2MIX_Input_1_Source | AIF1TX2MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX2MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1801<br>(709h) | AIF1TX2MIX_Input_1_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX2MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1802<br>(70Ah) | AIF1TX2MIX_Input_2_Source | AIF1TX2MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX2MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1803<br>(70Bh) | AIF1TX2MIX_Input_2_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX2MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1804<br>(70Ch) | AIF1TX2MIX_Input_3_Source | AIF1TX2MIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX2MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1805<br>(70Dh) | AIF1TX2MIX_Input_3_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX2MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1806<br>(70Eh) | AIF1TX2MIX_Input_4_Source | AIF1TX2MIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX2MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1807<br>(70Fh) | AIF1TX2MIX_Input_4_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX2MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1808<br>(710h) | AIF1TX3MIX_Input_1_Source | AIF1TX3MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX3MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1809<br>(711h) | AIF1TX3MIX_Input_1_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX3MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1810<br>(712h) | AIF1TX3MIX_Input_2_Source | AIF1TX3MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX3MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1811<br>(713h) | AIF1TX3MIX_Input_2_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX3MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1812<br>(714h) | AIF1TX3MIX_Input_3_Source | AIF1TX3MIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX3MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register        | Name                      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                     | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |
|-----------------|---------------------------|-----------------|----|----|----|----|----|---|---|-----------------------|---|---|---|---|---|---|---|---------|
| R1813<br>(715h) | AIF1TX3MIX_Input_3_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX3MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1814<br>(716h) | AIF1TX3MIX_Input_4_Source | AIF1TX3MIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX3MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1815<br>(717h) | AIF1TX3MIX_Input_4_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX3MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1816<br>(718h) | AIF1TX4MIX_Input_1_Source | AIF1TX4MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX4MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1817<br>(719h) | AIF1TX4MIX_Input_1_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX4MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1818<br>(71Ah) | AIF1TX4MIX_Input_2_Source | AIF1TX4MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX4MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1819<br>(71Bh) | AIF1TX4MIX_Input_2_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX4MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1820<br>(71Ch) | AIF1TX4MIX_Input_3_Source | AIF1TX4MIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX4MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1821<br>(71Dh) | AIF1TX4MIX_Input_3_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX4MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1822<br>(71Eh) | AIF1TX4MIX_Input_4_Source | AIF1TX4MIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX4MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1823<br>(71Fh) | AIF1TX4MIX_Input_4_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX4MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1824<br>(720h) | AIF1TX5MIX_Input_1_Source | AIF1TX5MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX5MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1825<br>(721h) | AIF1TX5MIX_Input_1_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX5MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1826<br>(722h) | AIF1TX5MIX_Input_2_Source | AIF1TX5MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX5MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1827<br>(723h) | AIF1TX5MIX_Input_2_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX5MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1828<br>(724h) | AIF1TX5MIX_Input_3_Source | AIF1TX5MIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX5MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1829<br>(725h) | AIF1TX5MIX_Input_3_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX5MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1830<br>(726h) | AIF1TX5MIX_Input_4_Source | AIF1TX5MIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX5MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1831<br>(727h) | AIF1TX5MIX_Input_4_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX5MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1832<br>(728h) | AIF1TX6MIX_Input_1_Source | AIF1TX6MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX6MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1833<br>(729h) | AIF1TX6MIX_Input_1_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX6MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1834<br>(72Ah) | AIF1TX6MIX_Input_2_Source | AIF1TX6MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX6MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1835<br>(72Bh) | AIF1TX6MIX_Input_2_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX6MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1836<br>(72Ch) | AIF1TX6MIX_Input_3_Source | AIF1TX6MIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX6MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1837<br>(72Dh) | AIF1TX6MIX_Input_3_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX6MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1838<br>(72Eh) | AIF1TX6MIX_Input_4_Source | AIF1TX6MIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX6MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1839<br>(72Fh) | AIF1TX6MIX_Input_4_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF1TX6MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1856<br>(740h) | AIF2TX1MIX_Input_1_Source | AIF2TX1MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX1MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1857<br>(741h) | AIF2TX1MIX_Input_1_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX1MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1858<br>(742h) | AIF2TX1MIX_Input_2_Source | AIF2TX1MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX1MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1859<br>(743h) | AIF2TX1MIX_Input_2_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX1MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1860<br>(744h) | AIF2TX1MIX_Input_3_Source | AIF2TX1MIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX1MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1861<br>(745h) | AIF2TX1MIX_Input_3_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX1MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1862<br>(746h) | AIF2TX1MIX_Input_4_Source | AIF2TX1MIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX1MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1863<br>(747h) | AIF2TX1MIX_Input_4_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX1MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1864<br>(748h) | AIF2TX2MIX_Input_1_Source | AIF2TX2MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX2MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1865<br>(749h) | AIF2TX2MIX_Input_1_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX2MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1866<br>(74Ah) | AIF2TX2MIX_Input_2_Source | AIF2TX2MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX2MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register        | Name                      | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                     | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |
|-----------------|---------------------------|-----------------|----|----|----|----|----|---|---|-----------------------|---|---|---|---|---|---|---|---------|
| R1867<br>(74Bh) | AIF2TX2MIX_Input_2_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX2MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1868<br>(74Ch) | AIF2TX2MIX_Input_3_Source | AIF2TX2MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX2MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1869<br>(74Dh) | AIF2TX2MIX_Input_3_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX2MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1870<br>(74Eh) | AIF2TX2MIX_Input_4_Source | AIF2TX2MIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX2MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1871<br>(74Fh) | AIF2TX2MIX_Input_4_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF2TX2MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1920<br>(780h) | AIF3TX1MIX_Input_1_Source | AIF3TX1MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX1MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1921<br>(781h) | AIF3TX1MIX_Input_1_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX1MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1922<br>(782h) | AIF3TX1MIX_Input_2_Source | AIF3TX1MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX1MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1923<br>(783h) | AIF3TX1MIX_Input_2_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX1MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1924<br>(784h) | AIF3TX1MIX_Input_3_Source | AIF3TX1MIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX1MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1925<br>(785h) | AIF3TX1MIX_Input_3_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX1MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1926<br>(786h) | AIF3TX1MIX_Input_4_Source | AIF3TX1MIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX1MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1927<br>(787h) | AIF3TX1MIX_Input_4_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX1MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1928<br>(788h) | AIF3TX2MIX_Input_1_Source | AIF3TX2MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX2MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1929<br>(789h) | AIF3TX2MIX_Input_1_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX2MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1930<br>(78Ah) | AIF3TX2MIX_Input_2_Source | AIF3TX2MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX2MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1931<br>(78Bh) | AIF3TX2MIX_Input_2_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX2MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1932<br>(78Ch) | AIF3TX2MIX_Input_3_Source | AIF3TX2MIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX2MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1933<br>(78Dh) | AIF3TX2MIX_Input_3_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX2MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1934<br>(78Eh) | AIF3TX2MIX_Input_4_Source | AIF3TX2MIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX2MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1935<br>(78Fh) | AIF3TX2MIX_Input_4_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | AIF3TX2MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1984<br>(7C0h) | SLIMTX1MIX_Input_1_Source | SLIMTX1MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX1MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1985<br>(7C1h) | SLIMTX1MIX_Input_1_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX1MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1986<br>(7C2h) | SLIMTX1MIX_Input_2_Source | SLIMTX1MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX1MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1987<br>(7C3h) | SLIMTX1MIX_Input_2_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX1MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1988<br>(7C4h) | SLIMTX1MIX_Input_3_Source | SLIMTX1MIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX1MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1989<br>(7C5h) | SLIMTX1MIX_Input_3_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX1MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1990<br>(7C6h) | SLIMTX1MIX_Input_4_Source | SLIMTX1MIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX1MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1991<br>(7C7h) | SLIMTX1MIX_Input_4_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX1MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1992<br>(7C8h) | SLIMTX2MIX_Input_1_Source | SLIMTX2MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX2MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1993<br>(7C9h) | SLIMTX2MIX_Input_1_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX2MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1994<br>(7CAh) | SLIMTX2MIX_Input_2_Source | SLIMTX2MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX2MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1995<br>(7CBh) | SLIMTX2MIX_Input_2_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX2MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1996<br>(7CCh) | SLIMTX2MIX_Input_3_Source | SLIMTX2MIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX2MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1997<br>(7CDh) | SLIMTX2MIX_Input_3_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX2MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R1998<br>(7CEh) | SLIMTX2MIX_Input_4_Source | SLIMTX2MIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX2MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R1999<br>(7CFh) | SLIMTX2MIX_Input_4_Volume | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX2MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2000<br>(7D0h) | SLIMTX3MIX_Input_1_Source | SLIMTX3MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX3MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register        | Name                        | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                      | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |
|-----------------|-----------------------------|-------------------|----|----|----|----|----|---|---|------------------------|---|---|---|---|---|---|---|---------|
| R2001<br>(7D1h) | SLIMTX3MIX_Input_1_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX3MIX_VOL1 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2002<br>(7D2h) | SLIMTX3MIX_Input_2_Source   | SLIMTX3MIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX3MIX_SRC2 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2003<br>(7D3h) | SLIMTX3MIX_Input_2_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX3MIX_VOL2 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2004<br>(7D4h) | SLIMTX3MIX_Input_3_Source   | SLIMTX3MIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX3MIX_SRC3 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2005<br>(7D5h) | SLIMTX3MIX_Input_3_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX3MIX_VOL3 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2006<br>(7D6h) | SLIMTX3MIX_Input_4_Source   | SLIMTX3MIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX3MIX_SRC4 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2007<br>(7D7h) | SLIMTX3MIX_Input_4_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX3MIX_VOL4 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2008<br>(7D8h) | SLIMTX4MIX_Input_1_Source   | SLIMTX4MIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX4MIX_SRC1 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2009<br>(7D9h) | SLIMTX4MIX_Input_1_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX4MIX_VOL1 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2010<br>(7DAh) | SLIMTX4MIX_Input_2_Source   | SLIMTX4MIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX4MIX_SRC2 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2011<br>(7DBh) | SLIMTX4MIX_Input_2_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX4MIX_VOL2 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2012<br>(7DCh) | SLIMTX4MIX_Input_3_Source   | SLIMTX4MIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX4MIX_SRC3 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2013<br>(7DDh) | SLIMTX4MIX_Input_3_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX4MIX_VOL3 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2014<br>(7DEh) | SLIMTX4MIX_Input_4_Source   | SLIMTX4MIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX4MIX_SRC4 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2015<br>(7DFh) | SLIMTX4MIX_Input_4_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX4MIX_VOL4 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2016<br>(7E0h) | SLIMTX5MIX_Input_1_Source   | SLIMTX5MIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX5MIX_SRC1 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2017<br>(7E1h) | SLIMTX5MIX_Input_1_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX5MIX_VOL1 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2018<br>(7E2h) | SLIMTX5MIX_Input_2_Source   | SLIMTX5MIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX5MIX_SRC2 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2019<br>(7E3h) | SLIMTX5MIX_Input_2_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX5MIX_VOL2 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2020<br>(7E4h) | SLIMTX5MIX_Input_3_Source   | SLIMTX5MIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX5MIX_SRC3 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2021<br>(7E5h) | SLIMTX5MIX_Input_3_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX5MIX_VOL3 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2022<br>(7E6h) | SLIMTX5MIX_Input_4_Source   | SLIMTX5MIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX5MIX_SRC4 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2023<br>(7E7h) | SLIMTX5MIX_Input_4_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX5MIX_VOL4 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2024<br>(7E8h) | SLIMTX6MIX_Input_1_Source   | SLIMTX6MIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX6MIX_SRC1 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2025<br>(7E9h) | SLIMTX6MIX_Input_1_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX6MIX_VOL1 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2026<br>(7EAh) | SLIMTX6MIX_Input_2_Source   | SLIMTX6MIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX6MIX_SRC2 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2027<br>(7EBh) | SLIMTX6MIX_Input_2_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX6MIX_VOL2 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2028<br>(7ECh) | SLIMTX6MIX_Input_3_Source   | SLIMTX6MIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX6MIX_SRC3 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2029<br>(7EDh) | SLIMTX6MIX_Input_3_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX6MIX_VOL3 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2030<br>(7EEh) | SLIMTX6MIX_Input_4_Source   | SLIMTX6MIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX6MIX_SRC4 [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2031<br>(7EFh) | SLIMTX6MIX_Input_4_Volume   | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SLIMTX6MIX_VOL4 [6:0]  |   |   |   |   |   |   | 0 | 0080h   |
| R2048<br>(800h) | SPDIF1TX1MIX_Input_1_Source | SPDIF1TX1MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SPDIF1TX1MIX_SRC [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2049<br>(801h) | SPDIF1TX1MIX_Input_1_Volume | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SPDIF1TX1MIX_VOL [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2056<br>(808h) | SPDIF1TX2MIX_Input_1_Source | SPDIF1TX2MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SPDIF1TX2MIX_SRC [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2057<br>(809h) | SPDIF1TX2MIX_Input_1_Volume | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | SPDIF1TX2MIX_VOL [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2176<br>(880h) | EQ1MIX_Input_1_Source       | EQ1MIX_STS1       | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ1MIX_SRC1 [7:0]      |   |   |   |   |   |   |   | 0000h   |
| R2177<br>(881h) | EQ1MIX_Input_1_Volume       | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ1MIX_VOL1 [6:0]      |   |   |   |   |   |   | 0 | 0080h   |
| R2178<br>(882h) | EQ1MIX_Input_2_Source       | EQ1MIX_STS2       | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ1MIX_SRC2 [7:0]      |   |   |   |   |   |   |   | 0000h   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register        | Name                    | 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |
|-----------------|-------------------------|---------------|----|----|----|----|----|---|---|---------------------|---|---|---|---|---|---|---|---------|
| R2179<br>(883h) | EQ1MIX_Input_2_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ1MIX_VOL2 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2180<br>(884h) | EQ1MIX_Input_3_Source   | EQ1MIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ1MIX_SRC3 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R2181<br>(885h) | EQ1MIX_Input_3_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ1MIX_VOL3 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2182<br>(886h) | EQ1MIX_Input_4_Source   | EQ1MIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ1MIX_SRC4 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R2183<br>(887h) | EQ1MIX_Input_4_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ1MIX_VOL4 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2184<br>(888h) | EQ2MIX_Input_1_Source   | EQ2MIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ2MIX_SRC1 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R2185<br>(889h) | EQ2MIX_Input_1_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ2MIX_VOL1 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2186<br>(88Ah) | EQ2MIX_Input_2_Source   | EQ2MIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ2MIX_SRC2 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R2187<br>(88Bh) | EQ2MIX_Input_2_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ2MIX_VOL2 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2188<br>(88Ch) | EQ2MIX_Input_3_Source   | EQ2MIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ2MIX_SRC3 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R2189<br>(88Dh) | EQ2MIX_Input_3_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ2MIX_VOL3 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2190<br>(88Eh) | EQ2MIX_Input_4_Source   | EQ2MIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ2MIX_SRC4 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R2191<br>(88Fh) | EQ2MIX_Input_4_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ2MIX_VOL4 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2192<br>(890h) | EQ3MIX_Input_1_Source   | EQ3MIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ3MIX_SRC1 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R2193<br>(891h) | EQ3MIX_Input_1_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ3MIX_VOL1 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2194<br>(892h) | EQ3MIX_Input_2_Source   | EQ3MIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ3MIX_SRC2 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R2195<br>(893h) | EQ3MIX_Input_2_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ3MIX_VOL2 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2196<br>(894h) | EQ3MIX_Input_3_Source   | EQ3MIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ3MIX_SRC3 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R2197<br>(895h) | EQ3MIX_Input_3_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ3MIX_VOL3 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2198<br>(896h) | EQ3MIX_Input_4_Source   | EQ3MIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ3MIX_SRC4 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R2199<br>(897h) | EQ3MIX_Input_4_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ3MIX_VOL4 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2200<br>(898h) | EQ4MIX_Input_1_Source   | EQ4MIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ4MIX_SRC1 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R2201<br>(899h) | EQ4MIX_Input_1_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ4MIX_VOL1 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2202<br>(89Ah) | EQ4MIX_Input_2_Source   | EQ4MIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ4MIX_SRC2 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R2203<br>(89Bh) | EQ4MIX_Input_2_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ4MIX_VOL2 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2204<br>(89Ch) | EQ4MIX_Input_3_Source   | EQ4MIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ4MIX_SRC3 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R2205<br>(89Dh) | EQ4MIX_Input_3_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ4MIX_VOL3 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2206<br>(89Eh) | EQ4MIX_Input_4_Source   | EQ4MIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ4MIX_SRC4 [7:0]   |   |   |   |   |   |   |   | 0000h   |
| R2207<br>(89Fh) | EQ4MIX_Input_4_Volume   | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | EQ4MIX_VOL4 [6:0]   |   |   |   |   |   |   | 0 | 0080h   |
| R2240<br>(8C0h) | DRC1LMIX_Input_1_Source | DRC1LMIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1LMIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2241<br>(8C1h) | DRC1LMIX_Input_1_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1LMIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2242<br>(8C2h) | DRC1LMIX_Input_2_Source | DRC1LMIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1LMIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2243<br>(8C3h) | DRC1LMIX_Input_2_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1LMIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2244<br>(8C4h) | DRC1LMIX_Input_3_Source | DRC1LMIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1LMIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2245<br>(8C5h) | DRC1LMIX_Input_3_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1LMIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2246<br>(8C6h) | DRC1LMIX_Input_4_Source | DRC1LMIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1LMIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2247<br>(8C7h) | DRC1LMIX_Input_4_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1LMIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2248<br>(8C8h) | DRC1RMIX_Input_1_Source | DRC1RMIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1RMIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register        | Name                    | 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |
|-----------------|-------------------------|---------------|----|----|----|----|----|---|---|---------------------|---|---|---|---|---|---|---|---------|
| R2249<br>(8C9h) | DRC1RMIX_Input_1_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1RMIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2250<br>(8CAh) | DRC1RMIX_Input_2_Source | DRC1RMIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1RMIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2251<br>(8CBh) | DRC1RMIX_Input_2_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1RMIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2252<br>(8CCh) | DRC1RMIX_Input_3_Source | DRC1RMIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1RMIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2253<br>(8CDh) | DRC1RMIX_Input_3_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1RMIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2254<br>(8CEh) | DRC1RMIX_Input_4_Source | DRC1RMIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1RMIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2255<br>(8CFh) | DRC1RMIX_Input_4_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC1RMIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2256<br>(8D0h) | DRC2LMIX_Input_1_Source | DRC2LMIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2LMIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2257<br>(8D1h) | DRC2LMIX_Input_1_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2LMIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2258<br>(8D2h) | DRC2LMIX_Input_2_Source | DRC2LMIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2LMIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2259<br>(8D3h) | DRC2LMIX_Input_2_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2LMIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2260<br>(8D4h) | DRC2LMIX_Input_3_Source | DRC2LMIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2LMIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2261<br>(8D5h) | DRC2LMIX_Input_3_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2LMIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2262<br>(8D6h) | DRC2LMIX_Input_4_Source | DRC2LMIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2LMIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2263<br>(8D7h) | DRC2LMIX_Input_4_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2LMIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2264<br>(8D8h) | DRC2RMIX_Input_1_Source | DRC2RMIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2RMIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2265<br>(8D9h) | DRC2RMIX_Input_1_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2RMIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2266<br>(8DAh) | DRC2RMIX_Input_2_Source | DRC2RMIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2RMIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2267<br>(8DBh) | DRC2RMIX_Input_2_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2RMIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2268<br>(8DCh) | DRC2RMIX_Input_3_Source | DRC2RMIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2RMIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2269<br>(8DDh) | DRC2RMIX_Input_3_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2RMIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2270<br>(8DEh) | DRC2RMIX_Input_4_Source | DRC2RMIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2RMIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2271<br>(8DFh) | DRC2RMIX_Input_4_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DRC2RMIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2304<br>(900h) | HPLP1MIX_Input_1_Source | LHPF1MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF1MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2305<br>(901h) | HPLP1MIX_Input_1_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF1MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2306<br>(902h) | HPLP1MIX_Input_2_Source | LHPF1MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF1MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2307<br>(903h) | HPLP1MIX_Input_2_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF1MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2308<br>(904h) | HPLP1MIX_Input_3_Source | LHPF1MIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF1MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2309<br>(905h) | HPLP1MIX_Input_3_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF1MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2310<br>(906h) | HPLP1MIX_Input_4_Source | LHPF1MIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF1MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2311<br>(907h) | HPLP1MIX_Input_4_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF1MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2312<br>(908h) | HPLP2MIX_Input_1_Source | LHPF2MIX_STS1 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF2MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2313<br>(909h) | HPLP2MIX_Input_1_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF2MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2314<br>(90Ah) | HPLP2MIX_Input_2_Source | LHPF2MIX_STS2 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF2MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2315<br>(90Bh) | HPLP2MIX_Input_2_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF2MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2316<br>(90Ch) | HPLP2MIX_Input_3_Source | LHPF2MIX_STS3 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF2MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2317<br>(90Dh) | HPLP2MIX_Input_3_Volume | 0             | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF2MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2318<br>(90Eh) | HPLP2MIX_Input_4_Source | LHPF2MIX_STS4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF2MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register        | Name                       | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |
|-----------------|----------------------------|-----------------|----|----|----|----|----|---|---|---------------------|---|---|---|---|---|---|---|---------|
| R2319<br>(90Fh) | HPLP2MIX_Input_4_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF2MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2320<br>(910h) | HPLP3MIX_Input_1_Source    | LHPF3MIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF3MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2321<br>(911h) | HPLP3MIX_Input_1_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF3MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2322<br>(912h) | HPLP3MIX_Input_2_Source    | LHPF3MIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF3MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2323<br>(913h) | HPLP3MIX_Input_2_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF3MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2324<br>(914h) | HPLP3MIX_Input_3_Source    | LHPF3MIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF3MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2325<br>(915h) | HPLP3MIX_Input_3_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF3MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2326<br>(916h) | HPLP3MIX_Input_4_Source    | LHPF3MIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF3MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2327<br>(917h) | HPLP3MIX_Input_4_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF3MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2328<br>(918h) | HPLP4MIX_Input_1_Source    | LHPF4MIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF4MIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2329<br>(919h) | HPLP4MIX_Input_1_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF4MIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2330<br>(91Ah) | HPLP4MIX_Input_2_Source    | LHPF4MIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF4MIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2331<br>(91Bh) | HPLP4MIX_Input_2_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF4MIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2332<br>(91Ch) | HPLP4MIX_Input_3_Source    | LHPF4MIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF4MIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2333<br>(91Dh) | HPLP4MIX_Input_3_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF4MIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2334<br>(91Eh) | HPLP4MIX_Input_4_Source    | LHPF4MIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF4MIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2335<br>(91Fh) | HPLP4MIX_Input_4_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | LHPF4MIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2368<br>(940h) | DSP1LMIX_Input_1_Source    | DSP1LMIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1LMIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2369<br>(941h) | DSP1LMIX_Input_1_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1LMIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2370<br>(942h) | DSP1LMIX_Input_2_Source    | DSP1LMIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1LMIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2371<br>(943h) | DSP1LMIX_Input_2_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1LMIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2372<br>(944h) | DSP1LMIX_Input_3_Source    | DSP1LMIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1LMIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2373<br>(945h) | DSP1LMIX_Input_3_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1LMIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2374<br>(946h) | DSP1LMIX_Input_4_Source    | DSP1LMIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1LMIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2375<br>(947h) | DSP1LMIX_Input_4_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1LMIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2376<br>(948h) | DSP1RMIX_Input_1_Source    | DSP1RMIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1RMIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2377<br>(949h) | DSP1RMIX_Input_1_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1RMIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2378<br>(94Ah) | DSP1RMIX_Input_2_Source    | DSP1RMIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1RMIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2379<br>(94Bh) | DSP1RMIX_Input_2_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1RMIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2380<br>(94Ch) | DSP1RMIX_Input_3_Source    | DSP1RMIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1RMIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2381<br>(94Dh) | DSP1RMIX_Input_3_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1RMIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2382<br>(94Eh) | DSP1RMIX_Input_4_Source    | DSP1RMIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1RMIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2383<br>(94Fh) | DSP1RMIX_Input_4_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1RMIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2384<br>(950h) | DSP1AUX1MIX_Input_1_Source | DSP1AUX1MIX_STS | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1AUX1_SRC [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2392<br>(958h) | DSP1AUX2MIX_Input_1_Source | DSP1AUX2MIX_STS | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1AUX2_SRC [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2400<br>(960h) | DSP1AUX3MIX_Input_1_Source | DSP1AUX3MIX_STS | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1AUX3_SRC [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2408<br>(968h) | DSP1AUX4MIX_Input_1_Source | DSP1AUX4MIX_STS | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1AUX4_SRC [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2416<br>(970h) | DSP1AUX5MIX_Input_1_Source | DSP1AUX5MIX_STS | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1AUX5_SRC [7:0]  |   |   |   |   |   |   |   | 0000h   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register        | Name                       | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                   | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |
|-----------------|----------------------------|-----------------|----|----|----|----|----|---|---|---------------------|---|---|---|---|---|---|---|---------|
| R2424<br>(978h) | DSP1AUX6MIX_Input_1_Source | DSP1AUX6MIX_STS | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP1AUX6_SRC [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2432<br>(980h) | DSP2LMIX_Input_1_Source    | DSP2LMIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2LMIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2433<br>(981h) | DSP2LMIX_Input_1_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2LMIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2434<br>(982h) | DSP2LMIX_Input_2_Source    | DSP2LMIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2LMIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2435<br>(983h) | DSP2LMIX_Input_2_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2LMIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2436<br>(984h) | DSP2LMIX_Input_3_Source    | DSP2LMIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2LMIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2437<br>(985h) | DSP2LMIX_Input_3_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2LMIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2438<br>(986h) | DSP2LMIX_Input_4_Source    | DSP2LMIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2LMIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2439<br>(987h) | DSP2LMIX_Input_4_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2LMIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2440<br>(988h) | DSP2RMIX_Input_1_Source    | DSP2RMIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2RMIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2441<br>(989h) | DSP2RMIX_Input_1_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2RMIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2442<br>(98Ah) | DSP2RMIX_Input_2_Source    | DSP2RMIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2RMIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2443<br>(98Bh) | DSP2RMIX_Input_2_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2RMIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2444<br>(98Ch) | DSP2RMIX_Input_3_Source    | DSP2RMIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2RMIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2445<br>(98Dh) | DSP2RMIX_Input_3_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2RMIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2446<br>(98Eh) | DSP2RMIX_Input_4_Source    | DSP2RMIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2RMIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2447<br>(98Fh) | DSP2RMIX_Input_4_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2RMIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2448<br>(990h) | DSP2AUX1MIX_Input_1_Source | DSP2AUX1MIX_STS | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2AUX1_SRC [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2456<br>(998h) | DSP2AUX2MIX_Input_1_Source | DSP2AUX2MIX_STS | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2AUX2_SRC [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2464<br>(9A0h) | DSP2AUX3MIX_Input_1_Source | DSP2AUX3MIX_STS | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2AUX3_SRC [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2472<br>(9A8h) | DSP2AUX4MIX_Input_1_Source | DSP2AUX4MIX_STS | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2AUX4_SRC [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2480<br>(9B0h) | DSP2AUX5MIX_Input_1_Source | DSP2AUX5MIX_STS | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2AUX5_SRC [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2488<br>(9B8h) | DSP2AUX6MIX_Input_1_Source | DSP2AUX6MIX_STS | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP2AUX6_SRC [7:0]  |   |   |   |   |   |   |   | 0000h   |
| R2496<br>(9C0h) | DSP3LMIX_Input_1_Source    | DSP3LMIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3LMIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2497<br>(9C1h) | DSP3LMIX_Input_1_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3LMIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2498<br>(9C2h) | DSP3LMIX_Input_2_Source    | DSP3LMIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3LMIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2499<br>(9C3h) | DSP3LMIX_Input_2_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3LMIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2500<br>(9C4h) | DSP3LMIX_Input_3_Source    | DSP3LMIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3LMIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2501<br>(9C5h) | DSP3LMIX_Input_3_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3LMIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2502<br>(9C6h) | DSP3LMIX_Input_4_Source    | DSP3LMIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3LMIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2503<br>(9C7h) | DSP3LMIX_Input_4_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3LMIX_VOL4 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2504<br>(9C8h) | DSP3RMIX_Input_1_Source    | DSP3RMIX_STS1   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3RMIX_SRC1 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2505<br>(9C9h) | DSP3RMIX_Input_1_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3RMIX_VOL1 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2506<br>(9CAh) | DSP3RMIX_Input_2_Source    | DSP3RMIX_STS2   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3RMIX_SRC2 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2507<br>(9CBh) | DSP3RMIX_Input_2_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3RMIX_VOL2 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2508<br>(9CCh) | DSP3RMIX_Input_3_Source    | DSP3RMIX_STS3   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3RMIX_SRC3 [7:0] |   |   |   |   |   |   |   | 0000h   |
| R2509<br>(9CDh) | DSP3RMIX_Input_3_Volume    | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3RMIX_VOL3 [6:0] |   |   |   |   |   |   | 0 | 0080h   |
| R2510<br>(9CEh) | DSP3RMIX_Input_4_Source    | DSP3RMIX_STS4   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | DSP3RMIX_SRC4 [7:0] |   |   |   |   |   |   |   | 0000h   |



**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register        | Name   | 15                | 14 | 13 | 12 | 11                | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3       | 2           | 1     | 0     | Default |
|-----------------|--------|-------------------|----|----|----|-------------------|----|---|---|-------------------|---|---|---|---------|-------------|-------|-------|---------|
| R3613<br>(E1Dh) | EQ1_14 | EQ1_B4_A [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 16F8h   |
| R3614<br>(E1Eh) | EQ1_15 | EQ1_B4_B [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | F7D9h   |
| R3615<br>(E1Fh) | EQ1_16 | EQ1_B4_C [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 040Ah   |
| R3616<br>(E20h) | EQ1_17 | EQ1_B4_PG [15:0]  |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 1F14h   |
| R3617<br>(E21h) | EQ1_18 | EQ1_B5_A [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 058Ch   |
| R3618<br>(E22h) | EQ1_19 | EQ1_B5_B [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 0563h   |
| R3619<br>(E23h) | EQ1_20 | EQ1_B5_PG [15:0]  |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 4000h   |
| R3620<br>(E24h) | EQ1_21 | EQ1_B1_C [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 0B75h   |
| R3622<br>(E26h) | EQ2_1  | EQ2_B1_GAIN [4:0] |    |    |    | EQ2_B2_GAIN [4:0] |    |   |   | EQ2_B3_GAIN [4:0] |   |   |   | EQ2_ENA |             |       | 6318h |         |
| R3623<br>(E27h) | EQ2_2  | EQ2_B4_GAIN [4:0] |    |    |    | EQ2_B5_GAIN [4:0] |    |   |   | 0                 | 0 | 0 | 0 | 0       | EQ2_B1_MODE | 6300h |       |         |
| R3624<br>(E28h) | EQ2_3  | EQ2_B1_A [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 0FC8h   |
| R3625<br>(E29h) | EQ2_4  | EQ2_B1_B [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 03FEh   |
| R3626<br>(E2Ah) | EQ2_5  | EQ2_B1_PG [15:0]  |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 00E0h   |
| R3627<br>(E2Bh) | EQ2_6  | EQ2_B2_A [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 1EC4h   |
| R3628<br>(E2Ch) | EQ2_7  | EQ2_B2_B [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | F136h   |
| R3629<br>(E2Dh) | EQ2_8  | EQ2_B2_C [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 0409h   |
| R3630<br>(E2Eh) | EQ2_9  | EQ2_B2_PG [15:0]  |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 04CCh   |
| R3631<br>(E2Fh) | EQ2_10 | EQ2_B3_A [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 1C9Bh   |
| R3632<br>(E30h) | EQ2_11 | EQ2_B3_B [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | F337h   |
| R3633<br>(E31h) | EQ2_12 | EQ2_B3_C [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 040Bh   |
| R3634<br>(E32h) | EQ2_13 | EQ2_B3_PG [15:0]  |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 0CBBh   |
| R3635<br>(E33h) | EQ2_14 | EQ2_B4_A [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 16F8h   |
| R3636<br>(E34h) | EQ2_15 | EQ2_B4_B [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | F7D9h   |
| R3637<br>(E35h) | EQ2_16 | EQ2_B4_C [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 040Ah   |
| R3638<br>(E36h) | EQ2_17 | EQ2_B4_PG [15:0]  |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 1F14h   |
| R3639<br>(E37h) | EQ2_18 | EQ2_B5_A [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 058Ch   |
| R3640<br>(E38h) | EQ2_19 | EQ2_B5_B [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 0563h   |
| R3641<br>(E39h) | EQ2_20 | EQ2_B5_PG [15:0]  |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 4000h   |
| R3642<br>(E3Ah) | EQ2_21 | EQ2_B1_C [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 0B75h   |
| R3644<br>(E3Ch) | EQ3_1  | EQ3_B1_GAIN [4:0] |    |    |    | EQ3_B2_GAIN [4:0] |    |   |   | EQ3_B3_GAIN [4:0] |   |   |   | EQ3_ENA |             |       | 6318h |         |
| R3645<br>(E3Dh) | EQ3_2  | EQ3_B4_GAIN [4:0] |    |    |    | EQ3_B5_GAIN [4:0] |    |   |   | 0                 | 0 | 0 | 0 | 0       | EQ3_B1_MODE | 6300h |       |         |
| R3646<br>(E3Eh) | EQ3_3  | EQ3_B1_A [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 0FC8h   |
| R3647<br>(E3Fh) | EQ3_4  | EQ3_B1_B [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 03FEh   |
| R3648<br>(E40h) | EQ3_5  | EQ3_B1_PG [15:0]  |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 00E0h   |
| R3649<br>(E41h) | EQ3_6  | EQ3_B2_A [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 1EC4h   |
| R3650<br>(E42h) | EQ3_7  | EQ3_B2_B [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | F136h   |
| R3651<br>(E43h) | EQ3_8  | EQ3_B2_C [15:0]   |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 0409h   |
| R3652<br>(E44h) | EQ3_9  | EQ3_B2_PG [15:0]  |    |    |    |                   |    |   |   |                   |   |   |   |         |             |       |       | 04CCh   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register      | Name                      | 15                     | 14              | 13             | 12             | 11                | 10                    | 9                   | 8                 | 7                 | 6                  | 5                 | 4                   | 3             | 2                  | 1                  | 0             | Default |
|---------------|---------------------------|------------------------|-----------------|----------------|----------------|-------------------|-----------------------|---------------------|-------------------|-------------------|--------------------|-------------------|---------------------|---------------|--------------------|--------------------|---------------|---------|
| R3720 (E8h)   | DRC2_ctrl1                | DRC2_SIG_DET_RMS [4:0] |                 |                |                |                   | DRC2_SIG_DET_PK [1:0] |                     | DRC2_NG_ENA       | DRC2_SIG_DET_MODE | DRC2_SIG_DET       | DRC2_KNEE2_OP_ENA | DRC2_QR             | DRC2_ANTICLIP | 0                  | DRC2L_ENA          | DRC2R_ENA     | 0018h   |
| R3721 (E89h)  | DRC2_ctrl2                | 0                      | 0               | 0              | DRC2_ATK [3:0] |                   |                       |                     | DRC2_DCY [3:0]    |                   |                    |                   | DRC2_MINGAIN [2:0]  |               |                    | DRC2_MAXGAIN [1:0] |               | 0933h   |
| R3722 (E8Ah)  | DRC2_ctrl3                | DRC2_NG_MINGAIN [3:0]  |                 |                |                | DRC2_NG_EXP [1:0] |                       | DRC2_QR_THR [1:0]   | DRC2_QR_DCY [1:0] |                   | DRC2_HI_COMP [2:0] |                   |                     |               | DRC2_LO_COMP [2:0] |                    |               | 0018h   |
| R3723 (E8Bh)  | DRC2_ctrl4                | 0                      | 0               | 0              | 0              | 0                 | DRC2_KNEE_IP [5:0]    |                     |                   |                   |                    |                   | DRC2_KNEE_OP [4:0]  |               |                    |                    |               | 0000h   |
| R3724 (E8Ch)  | DRC2_ctrl5                | 0                      | 0               | 0              | 0              | 0                 | 0                     | DRC2_KNEE2_IP [4:0] |                   |                   |                    |                   | DRC2_KNEE2_OP [4:0] |               |                    |                    |               | 0000h   |
| R3776 (EC0h)  | HPLPF1_1                  | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | LHPF1_MODE         | LHPF1_ENA     | 0000h   |
| R3777 (EC1h)  | HPLPF1_2                  | LHPF1_COEFF [15:0]     |                 |                |                |                   |                       |                     |                   |                   |                    |                   |                     |               |                    |                    |               | 0000h   |
| R3780 (EC4h)  | HPLPF2_1                  | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | LHPF2_MODE         | LHPF2_ENA     | 0000h   |
| R3781 (EC5h)  | HPLPF2_2                  | LHPF2_COEFF [15:0]     |                 |                |                |                   |                       |                     |                   |                   |                    |                   |                     |               |                    |                    |               | 0000h   |
| R3784 (EC8h)  | HPLPF3_1                  | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | LHPF3_MODE         | LHPF3_ENA     | 0000h   |
| R3785 (EC9h)  | HPLPF3_2                  | LHPF3_COEFF [15:0]     |                 |                |                |                   |                       |                     |                   |                   |                    |                   |                     |               |                    |                    |               | 0000h   |
| R3788 (ECCh)  | HPLPF4_1                  | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | LHPF4_MODE         | LHPF4_ENA     | 0000h   |
| R3789 (EC Dh) | HPLPF4_2                  | LHPF4_COEFF [15:0]     |                 |                |                |                   |                       |                     |                   |                   |                    |                   |                     |               |                    |                    |               | 0000h   |
| R3824 (EF0h)  | ISRC1_CTRL_1              | 0                      | ISRC1_FSH [3:0] |                |                |                   | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | 0                  | 0             | 0000h   |
| R3825 (EF1h)  | ISRC1_CTRL_2              | 0                      | ISRC1_FSL [3:0] |                |                |                   | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | 0                  | 1             | 0001h   |
| R3826 (EF2h)  | ISRC1_CTRL_3              | ISRC1_INT1_ENA         | ISRC1_INT2_ENA  | ISRC1_INT3_ENA | ISRC1_INT4_ENA | 0                 | 0                     | ISRC1_DEC1_ENA      | ISRC1_DEC2_ENA    | ISRC1_DEC3_ENA    | ISRC1_DEC4_ENA     | 0                 | 0                   | 0             | 0                  | 0                  | 0             | 0000h   |
| R3827 (EF3h)  | ISRC2_CTRL_1              | 0                      | ISRC2_FSH [3:0] |                |                |                   | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | 0                  | 0             | 0000h   |
| R3828 (EF4h)  | ISRC2_CTRL_2              | 0                      | ISRC2_FSL [3:0] |                |                |                   | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | 0                  | 1             | 0001h   |
| R3829 (EF5h)  | ISRC2_CTRL_3              | ISRC2_INT1_ENA         | ISRC2_INT2_ENA  | ISRC2_INT3_ENA | ISRC2_INT4_ENA | 0                 | 0                     | ISRC2_DEC1_ENA      | ISRC2_DEC2_ENA    | ISRC2_DEC3_ENA    | ISRC2_DEC4_ENA     | 0                 | 0                   | 0             | 0                  | 0                  | 0             | 0000h   |
| R4608 (1200h) | Clock_enable_overrides_1  | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA1          | DSP_CLK_ENA1  | 0000h   |
| R4610 (1202h) | Clock_enable_overrides_2  | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA2          | DSP_CLK_ENA2  | 0000h   |
| R4612 (1204h) | Clock_enable_overrides_3  | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA3          | DSP_CLK_ENA3  | 0000h   |
| R4614 (1206h) | Clock_enable_overrides_4  | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA4          | DSP_CLK_ENA4  | 0000h   |
| R4616 (1208h) | Clock_enable_overrides_5  | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA5          | DSP_CLK_ENA5  | 0000h   |
| R4618 (120Ah) | Clock_enable_overrides_6  | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA6          | DSP_CLK_ENA6  | 0000h   |
| R4620 (120Ch) | Clock_enable_overrides_7  | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA7          | DSP_CLK_ENA7  | 0000h   |
| R4622 (120Eh) | Clock_enable_overrides_8  | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA8          | DSP_CLK_ENA8  | 0000h   |
| R4624 (1210h) | Clock_enable_overrides_9  | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA9          | DSP_CLK_ENA9  | 0000h   |
| R4626 (1212h) | Clock_enable_overrides_10 | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA10         | DSP_CLK_ENA10 | 0000h   |
| R4628 (1214h) | Clock_enable_overrides_11 | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA11         | DSP_CLK_ENA11 | 0000h   |
| R4630 (1216h) | Clock_enable_overrides_12 | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA12         | DSP_CLK_ENA12 | 0000h   |
| R4632 (1218h) | Clock_enable_overrides_13 | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA13         | DSP_CLK_ENA13 | 0000h   |
| R4634 (121Ah) | Clock_enable_overrides_14 | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA14         | DSP_CLK_ENA14 | 0000h   |
| R4636 (121Ch) | Clock_enable_overrides_15 | 0                      | 0               | 0              | 0              | 0                 | 0                     | 0                   | 0                 | 0                 | 0                  | 0                 | 0                   | 0             | 0                  | FLL1_ENA15         | DSP_CLK_ENA15 | 0000h   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register         | Name                       | 15       | 14          | 13      | 12           | 11 | 10 | 9 | 8             | 7 | 6 | 5 | 4 | 3 | 2 | 1             | 0              | Default |
|------------------|----------------------------|----------|-------------|---------|--------------|----|----|---|---------------|---|---|---|---|---|---|---------------|----------------|---------|
| R4638<br>(121Eh) | Clock_enable_ overrides_16 | 0        | 0           | 0       | 0            | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | FLL1<br>ENA16 | DSP_CLK_ ENA16 | 0000h   |
| R5632<br>(1600h) | ADSP2_IRQ0                 | 0        | 0           | 0       | 0            | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | DSP_IRQ2      | DSP_IRQ1       | 0000h   |
| R5633<br>(1601h) | ADSP2_IRQ1                 | 0        | 0           | 0       | 0            | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | DSP_IRQ4      | DSP_IRQ3       | 0000h   |
| R5634<br>(1602h) | ADSP2_IRQ2                 | 0        | 0           | 0       | 0            | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | DSP_IRQ6      | DSP_IRQ5       | 0000h   |
| R5635<br>(1603h) | ADSP2_IRQ3                 | 0        | 0           | 0       | 0            | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | DSP_IRQ8      | DSP_IRQ7       | 0000h   |
| R5636<br>(1604h) | ADSP2_IRQ4                 | 0        | 0           | 0       | 0            | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | DSP_IRQ10     | DSP_IRQ9       | 0000h   |
| R5637<br>(1605h) | ADSP2_IRQ5                 | 0        | 0           | 0       | 0            | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | DSP_IRQ12     | DSP_IRQ11      | 0000h   |
| R5638<br>(1606h) | ADSP2_IRQ6                 | 0        | 0           | 0       | 0            | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | DSP_IRQ14     | DSP_IRQ13      | 0000h   |
| R5639<br>(1607h) | ADSP2_IRQ7                 | 0        | 0           | 0       | 0            | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | DSP_IRQ16     | DSP_IRQ15      | 0000h   |
| R5888<br>(1700h) | GPIO1_CTRL_1               | GP1_LVL  | GP1_OP_CFG  | GP1_DB  | GP1_POL      | 0  | 0  | 0 | GP1_FN [8:0]  |   |   |   |   |   |   |               | 2001h          |         |
| R5889<br>(1701h) | GPIO1_CTRL_2               | GP1_DIR  | GP1_PU      | GP1_PD  | GP1_DRV_STR  | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0              | F000h   |
| R5890<br>(1702h) | GPIO2_CTRL_1               | GP2_LVL  | GP2_OP_CFG  | GP2_DB  | GP2_POL      | 0  | 0  | 0 | GP2_FN [8:0]  |   |   |   |   |   |   |               | 2001h          |         |
| R5891<br>(1703h) | GPIO2_CTRL_2               | GP2_DIR  | GP2_PU      | GP2_PD  | GP2_DRV_STR  | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0              | F000h   |
| R5892<br>(1704h) | GPIO3_CTRL_1               | GP3_LVL  | GP3_OP_CFG  | GP3_DB  | GP3_POL      | 0  | 0  | 0 | GP3_FN [8:0]  |   |   |   |   |   |   |               | 2001h          |         |
| R5893<br>(1705h) | GPIO3_CTRL_2               | GP3_DIR  | GP3_PU      | GP3_PD  | GP3_DRV_STR  | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0              | F000h   |
| R5894<br>(1706h) | GPIO4_CTRL_1               | GP4_LVL  | GP4_OP_CFG  | GP4_DB  | GP4_POL      | 0  | 0  | 0 | GP4_FN [8:0]  |   |   |   |   |   |   |               | 2001h          |         |
| R5895<br>(1707h) | GPIO4_CTRL_2               | GP4_DIR  | GP4_PU      | GP4_PD  | GP4_DRV_STR  | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0              | F000h   |
| R5896<br>(1708h) | GPIO5_CTRL_1               | GP5_LVL  | GP5_OP_CFG  | GP5_DB  | GP5_POL      | 0  | 0  | 0 | GP5_FN [8:0]  |   |   |   |   |   |   |               | 2001h          |         |
| R5897<br>(1709h) | GPIO5_CTRL_2               | GP5_DIR  | GP5_PU      | GP5_PD  | GP5_DRV_STR  | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0              | F000h   |
| R5898<br>(170Ah) | GPIO6_CTRL_1               | GP6_LVL  | GP6_OP_CFG  | GP6_DB  | GP6_POL      | 0  | 0  | 0 | GP6_FN [8:0]  |   |   |   |   |   |   |               | 2001h          |         |
| R5899<br>(170Bh) | GPIO6_CTRL_2               | GP6_DIR  | GP6_PU      | GP6_PD  | GP6_DRV_STR  | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0              | F000h   |
| R5900<br>(170Ch) | GPIO7_CTRL_1               | GP7_LVL  | GP7_OP_CFG  | GP7_DB  | GP7_POL      | 0  | 0  | 0 | GP7_FN [8:0]  |   |   |   |   |   |   |               | 2001h          |         |
| R5901<br>(170Dh) | GPIO7_CTRL_2               | GP7_DIR  | GP7_PU      | GP7_PD  | GP7_DRV_STR  | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0              | F000h   |
| R5902<br>(170Eh) | GPIO8_CTRL_1               | GP8_LVL  | GP8_OP_CFG  | GP8_DB  | GP8_POL      | 0  | 0  | 0 | GP8_FN [8:0]  |   |   |   |   |   |   |               | 2001h          |         |
| R5903<br>(170Fh) | GPIO8_CTRL_2               | GP8_DIR  | GP8_PU      | GP8_PD  | GP8_DRV_STR  | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0              | F000h   |
| R5904<br>(1710h) | GPIO9_CTRL_1               | GP9_LVL  | GP9_OP_CFG  | GP9_DB  | GP9_POL      | 0  | 0  | 0 | GP9_FN [8:0]  |   |   |   |   |   |   |               | 2001h          |         |
| R5905<br>(1711h) | GPIO9_CTRL_2               | GP9_DIR  | GP9_PU      | GP9_PD  | GP9_DRV_STR  | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0              | F000h   |
| R5906<br>(1712h) | GPIO10_CTRL_1              | GP10_LVL | GP10_OP_CFG | GP10_DB | GP10_POL     | 0  | 0  | 0 | GP10_FN [8:0] |   |   |   |   |   |   |               | 2001h          |         |
| R5907<br>(1713h) | GPIO10_CTRL_2              | GP10_DIR | GP10_PU     | GP10_PD | GP10_DRV_STR | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0              | F000h   |
| R5908<br>(1714h) | GPIO11_CTRL_1              | GP11_LVL | GP11_OP_CFG | GP11_DB | GP11_POL     | 0  | 0  | 0 | GP11_FN [8:0] |   |   |   |   |   |   |               | 2001h          |         |
| R5909<br>(1715h) | GPIO11_CTRL_2              | GP11_DIR | GP11_PU     | GP11_PD | GP11_DRV_STR | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0              | F000h   |
| R5910<br>(1716h) | GPIO12_CTRL_1              | GP12_LVL | GP12_OP_CFG | GP12_DB | GP12_POL     | 0  | 0  | 0 | GP12_FN [8:0] |   |   |   |   |   |   |               | 2001h          |         |
| R5911<br>(1717h) | GPIO12_CTRL_2              | GP12_DIR | GP12_PU     | GP12_PD | GP12_DRV_STR | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0              | F000h   |
| R5912<br>(1718h) | GPIO13_CTRL_1              | GP13_LVL | GP13_OP_CFG | GP13_DB | GP13_POL     | 0  | 0  | 0 | GP13_FN [8:0] |   |   |   |   |   |   |               | 2001h          |         |
| R5913<br>(1719h) | GPIO13_CTRL_2              | GP13_DIR | GP13_PU     | GP13_PD | GP13_DRV_STR | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0              | F000h   |
| R5914<br>(171Ah) | GPIO14_CTRL_1              | GP14_LVL | GP14_OP_CFG | GP14_DB | GP14_POL     | 0  | 0  | 0 | GP14_FN [8:0] |   |   |   |   |   |   |               | 2001h          |         |
| R5915<br>(171Bh) | GPIO14_CTRL_2              | GP14_DIR | GP14_PU     | GP14_PD | GP14_DRV_STR | 0  | 0  | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0              | F000h   |
| R5916<br>(171Ch) | GPIO15_CTRL_1              | GP15_LVL | GP15_OP_CFG | GP15_DB | GP15_POL     | 0  | 0  | 0 | GP15_FN [8:0] |   |   |   |   |   |   |               | 2001h          |         |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register         | Name           | 15                          | 14              | 13              | 12                  | 11              | 10              | 9                    | 8                  | 7                  | 6                          | 5                        | 4                        | 3                      | 2                       | 1                       | 0                       | Default |
|------------------|----------------|-----------------------------|-----------------|-----------------|---------------------|-----------------|-----------------|----------------------|--------------------|--------------------|----------------------------|--------------------------|--------------------------|------------------------|-------------------------|-------------------------|-------------------------|---------|
| R5917<br>(171Dh) | GPIO15_CTRL_2  | GP15_DIR                    | GP15_PU         | GP15_PD         | GP15_DRV_STR        | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | 0                      | 0                       | 0                       | 0                       | F000h   |
| R5918<br>(171Eh) | GPIO16_CTRL_1  | GP16_LVL                    | GP16_OP_CFG     | GP16_DB         | GP16_POL            | 0               | 0               | 0                    | GP16_FN [8:0]      |                    |                            |                          |                          |                        |                         |                         |                         | 2001h   |
| R5919<br>(171Fh) | GPIO16_CTRL_2  | GP16_DIR                    | GP16_PU         | GP16_PD         | GP16_DRV_STR        | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | 0                      | 0                       | 0                       | 0                       | F000h   |
| R6144<br>(1800h) | IRQ1_Status_1  | DSP_SHARED_WR_COLL_EINT1    | 0               | 0               | CTRLIF_ERR_EINT1    | 0               | 0               | SYSCLK_FAIL_EINT1    | 0                  | BOOT_DONE_EINT1    | 0                          | 0                        | 0                        | 0                      | 0                       | 0                       | 0                       | 0000h   |
| R6145<br>(1801h) | IRQ1_Status_2  | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | FLL1_LOCK_EINT1    | 0                  | 0                          | 0                        | 0                        | 0                      | 0                       | 0                       | 0                       | 0000h   |
| R6149<br>(1805h) | IRQ1_Status_6  | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | MICDET_EINT1       | 0                  | 0                          | 0                        | 0                        | 0                      | 0                       | 0                       | HPDET_EINT1             | 0000h   |
| R6150<br>(1806h) | IRQ1_Status_7  | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | MICD_CLAMP_FALL_EINT1    | MICD_CLAMP_RISE_EINT1    | JD2_FALL_EINT1         | JD2_RISE_EINT1          | JD1_FALL_EINT1          | JD1_RISE_EINT1          | 0000h   |
| R6152<br>(1808h) | IRQ1_Status_9  | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | 0                      | 0                       | DRC2_SIG_DET_EINT1      | DRC1_SIG_DET_EINT1      | 0000h   |
| R6154<br>(180Ah) | IRQ1_Status_11 | DSP_IRQ16_EINT1             | DSP_IRQ15_EINT1 | DSP_IRQ14_EINT1 | DSP_IRQ13_EINT1     | DSP_IRQ12_EINT1 | DSP_IRQ11_EINT1 | DSP_IRQ10_EINT1      | DSP_IRQ9_EINT1     | DSP_IRQ8_EINT1     | DSP_IRQ7_EINT1             | DSP_IRQ6_EINT1           | DSP_IRQ5_EINT1           | DSP_IRQ4_EINT1         | DSP_IRQ3_EINT1          | DSP_IRQ2_EINT1          | DSP_IRQ1_EINT1          | 0000h   |
| R6155<br>(180Bh) | IRQ1_Status_12 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | SPKOUTL_SC_EINT1           | 0                        | 0                        | HP2R_SC_EINT1          | HP2L_SC_EINT1           | HP1R_SC_EINT1           | HP1L_SC_EINT1           | 0000h   |
| R6156<br>(180Ch) | IRQ1_Status_13 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | SPKOUTL_ENABLE_DONE_EINT1  | 0                        | 0                        | 0                      | 0                       | HP1R_ENABLE_DONE_EINT1  | HP1L_ENABLE_DONE_EINT1  | 0000h   |
| R6157<br>(180Dh) | IRQ1_Status_14 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | SPKOUTL_DISABLE_DONE_EINT1 | 0                        | 0                        | 0                      | 0                       | HP1R_DISABLE_DONE_EINT1 | HP1L_DISABLE_DONE_EINT1 | 0000h   |
| R6158<br>(180Eh) | IRQ1_Status_15 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | 0                      | SPK_OVERHEAT_WARN_EINT1 | SPK_OVERHEAT_EINT1      | SPK_SHUTDOWN_EINT1      | 0000h   |
| R6160<br>(1810h) | IRQ1_Status_17 | GPIO16_EINT1                | GPIO15_EINT1    | GPIO14_EINT1    | GPIO13_EINT1        | GPIO12_EINT1    | GPIO11_EINT1    | GPIO10_EINT1         | GPIO9_EINT1        | GPIO8_EINT1        | GPIO7_EINT1                | GPIO6_EINT1              | GPIO5_EINT1              | GPIO4_EINT1            | GPIO3_EINT1             | GPIO2_EINT1             | GPIO1_EINT1             | 0000h   |
| R6164<br>(1814h) | IRQ1_Status_21 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | TIMER4_EINT1           | TIMER3_EINT1            | TIMER2_EINT1            | TIMER1_EINT1            | 0000h   |
| R6165<br>(1815h) | IRQ1_Status_22 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | EVENT4_NOT_EMPTY_EINT1 | EVENT3_NOT_EMPTY_EINT1  | EVENT2_NOT_EMPTY_EINT1  | EVENT1_NOT_EMPTY_EINT1  | 0000h   |
| R6166<br>(1816h) | IRQ1_Status_23 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | EVENT4_FULL_EINT1      | EVENT3_FULL_EINT1       | EVENT2_FULL_EINT1       | EVENT1_FULL_EINT1       | 0000h   |
| R6167<br>(1817h) | IRQ1_Status_24 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | EVENT4_WMARK_EINT1     | EVENT3_WMARK_EINT1      | EVENT2_WMARK_EINT1      | EVENT1_WMARK_EINT1      | 0000h   |
| R6168<br>(1818h) | IRQ1_Status_25 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | 0                      | DSP3_DMA_EINT1          | DSP2_DMA_EINT1          | DSP1_DMA_EINT1          | 0000h   |
| R6170<br>(181Ah) | IRQ1_Status_27 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | 0                      | DSP3_START1_EINT1       | DSP2_START1_EINT1       | DSP1_START1_EINT1       | 0000h   |
| R6171<br>(181Bh) | IRQ1_Status_28 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | 0                      | DSP3_START2_EINT1       | DSP2_START2_EINT1       | DSP1_START2_EINT1       | 0000h   |
| R6173<br>(181Dh) | IRQ1_Status_30 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | 0                      | DSP3_BUSY_EINT1         | DSP2_BUSY_EINT1         | DSP1_BUSY_EINT1         | 0000h   |
| R6174<br>(181Eh) | IRQ1_Status_31 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | 0                      | 0                       | 0                       | MIF1_DONE_EINT1         | 0000h   |
| R6175<br>(181Fh) | IRQ1_Status_32 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | 0                      | 0                       | 0                       | MIF1_BLOCK_EINT1        | 0000h   |
| R6208<br>(1840h) | IRQ1_Mask_1    | IM_DSP_SHARED_WR_COLL_EINT1 | 0               | 0               | IM_CTRLIF_ERR_EINT1 | 0               | 0               | IM_SYSCLK_FAIL_EINT1 | 1                  | IM_BOOT_DONE_EINT1 | 0                          | 0                        | 0                        | 0                      | 0                       | 0                       | 0                       | 9300h   |
| R6209<br>(1841h) | IRQ1_Mask_2    | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | IM_FLL1_LOCK_EINT1 | 0                  | 0                          | 0                        | 0                        | 0                      | 0                       | 0                       | 0                       | 0100h   |
| R6213<br>(1845h) | IRQ1_Mask_6    | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | IM_MICDET_EINT1    | 0                  | 0                          | 0                        | 0                        | 0                      | 0                       | 0                       | IM_HPDET_EINT1          | 0101h   |
| R6214<br>(1846h) | IRQ1_Mask_7    | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | IM_MICD_CLAMP_FALL_EINT1 | IM_MICD_CLAMP_RISE_EINT1 | IM_JD2_FALL_EINT1      | IM_JD2_RISE_EINT1       | IM_JD1_FALL_EINT1       | IM_JD1_RISE_EINT1       | 003Fh   |
| R6216<br>(1848h) | IRQ1_Mask_9    | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0                          | 0                        | 0                        | 0                      | 0                       | IM_DRC2_SIG_DET_EINT1   | IM_DRC1_SIG_DET_EINT1   | 0003h   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register         | Name              | 15                 | 14                 | 13                 | 12                 | 11                 | 10                 | 9                  | 8                 | 7                 | 6                             | 5                 | 4                 | 3                         | 2                          | 1                          | 0                          | Default |
|------------------|-------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|-------------------|-------------------|-------------------------------|-------------------|-------------------|---------------------------|----------------------------|----------------------------|----------------------------|---------|
| R6218<br>(184Ah) | RQ1_Mask_11       | IM_DSP_IRO16_EINT1 | IM_DSP_IRO15_EINT1 | IM_DSP_IRO14_EINT1 | IM_DSP_IRO13_EINT1 | IM_DSP_IRO12_EINT1 | IM_DSP_IRO11_EINT1 | IM_DSP_IRO10_EINT1 | IM_DSP_IRO9_EINT1 | IM_DSP_IRO8_EINT1 | IM_DSP_IRO7_EINT1             | IM_DSP_IRO6_EINT1 | IM_DSP_IRO5_EINT1 | IM_DSP_IRO4_EINT1         | IM_DSP_IRO3_EINT1          | IM_DSP_IRO2_EINT1          | IM_DSP_IRO1_EINT1          | FFFFh   |
| R6219<br>(184Bh) | RQ1_Mask_12       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | IM_SPKOUTL_SC_EINT1           | 0                 | 0                 | IM_HP2R_SC_EINT1          | IM_HP2L_SC_EINT1           | IM_HP1R_SC_EINT1           | IM_HP1L_SC_EINT1           | 004Fh   |
| R6220<br>(184Ch) | RQ1_Mask_13       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | IM_SPKOUTL_ENABLE_DONE_EINT1  | 0                 | 0                 | 0                         | 0                          | IM_HP1R_ENABLE_DONE_EINT1  | IM_HP1L_ENABLE_DONE_EINT1  | 0043h   |
| R6221<br>(184Dh) | RQ1_Mask_14       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | IM_SPKOUTL_DISABLE_DONE_EINT1 | 0                 | 0                 | 0                         | 0                          | IM_HP1R_DISABLE_DONE_EINT1 | IM_HP1L_DISABLE_DONE_EINT1 | 0043h   |
| R6222<br>(184Eh) | RQ1_Mask_15       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | IM_SPK_OVERHEAT_WARN_EINT1 | IM_SPK_OVERHEAT_EINT1      | IM_SPK_SHUTDOWN_EINT1      | 0007h   |
| R6224<br>(1850h) | RQ1_Mask_17       | IM_GPIO16_EINT1    | IM_GPIO15_EINT1    | IM_GPIO14_EINT1    | IM_GPIO13_EINT1    | IM_GPIO12_EINT1    | IM_GPIO11_EINT1    | IM_GPIO10_EINT1    | IM_GPIO9_EINT1    | IM_GPIO8_EINT1    | IM_GPIO7_EINT1                | IM_GPIO6_EINT1    | IM_GPIO5_EINT1    | IM_GPIO4_EINT1            | IM_GPIO3_EINT1             | IM_GPIO2_EINT1             | IM_GPIO1_EINT1             | FFFFh   |
| R6228<br>(1854h) | RQ1_Mask_21       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | IM_TIMER4_EINT1           | IM_TIMER3_EINT1            | IM_TIMER2_EINT1            | IM_TIMER1_EINT1            | 000Fh   |
| R6229<br>(1855h) | RQ1_Mask_22       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | IM_EVENT4_NOT_EMPTY_EINT1 | IM_EVENT3_NOT_EMPTY_EINT1  | IM_EVENT2_NOT_EMPTY_EINT1  | IM_EVENT1_NOT_EMPTY_EINT1  | 000Fh   |
| R6230<br>(1856h) | RQ1_Mask_23       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | IM_EVENT4_FULL_EINT1      | IM_EVENT3_FULL_EINT1       | IM_EVENT2_FULL_EINT1       | IM_EVENT1_FULL_EINT1       | 000Fh   |
| R6231<br>(1857h) | RQ1_Mask_24       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | IM_EVENT4_WMARK_EINT1     | IM_EVENT3_WMARK_EINT1      | IM_EVENT2_WMARK_EINT1      | IM_EVENT1_WMARK_EINT1      | 000Fh   |
| R6232<br>(1858h) | RQ1_Mask_25       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | IM_DSP3_DMA_EINT1          | IM_DSP2_DMA_EINT1          | IM_DSP1_DMA_EINT1          | 0007h   |
| R6234<br>(185Ah) | RQ1_Mask_27       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | IM_DSP3_START1_EINT1       | IM_DSP2_START1_EINT1       | IM_DSP1_START1_EINT1       | 0007h   |
| R6235<br>(185Bh) | RQ1_Mask_28       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | IM_DSP3_START2_EINT1       | IM_DSP2_START2_EINT1       | IM_DSP1_START2_EINT1       | 0007h   |
| R6237<br>(185Dh) | RQ1_Mask_30       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | IM_DSP3_BUSY_EINT1         | IM_DSP2_BUSY_EINT1         | IM_DSP1_BUSY_EINT1         | 0007h   |
| R6238<br>(185Eh) | RQ1_Mask_31       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | IM_MIF1_DONE_EINT1         | 0001h   |
| R6239<br>(185Fh) | RQ1_Mask_32       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | IM_MIF1_BLOCK_EINT1        | 0001h   |
| R6272<br>(1880h) | RQ1_Raw_Status_1  | 0                  | 0                  | 0                  | CTRLIF_ERR_STS1    | 0                  | 0                  | 0                  | 0                 | BOOT_DONE_STS1    | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | 0                          | 0000h   |
| R6273<br>(1881h) | RQ1_Raw_Status_2  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | FLL1_LOCK_STS1    | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | 0                          | 0000h   |
| R6278<br>(1886h) | RQ1_Raw_Status_7  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | MICD_CLAMP_STS1   | 0                         | JD2_STS1                   | 0                          | JD1_STS1                   | 0000h   |
| R6280<br>(1888h) | RQ1_Raw_Status_9  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | 0                          | DRC2_SIG_DET_STS1          | DRC1_SIG_DET_STS1          | 0000h   |
| R6283<br>(188Bh) | RQ1_Raw_Status_12 | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | SPKOUTL_SC_STS1               | 0                 | 0                 | HP2R_SC_STS1              | HP2L_SC_STS1               | HP1R_SC_STS1               | HP1L_SC_STS1               | 0000h   |
| R6284<br>(188Ch) | RQ1_Raw_Status_13 | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | SPKOUTL_ENABLE_DONE_STS1      | 0                 | 0                 | 0                         | 0                          | HP1R_ENABLE_DONE_STS1      | HP1L_ENABLE_DONE_STS1      | 0000h   |
| R6285<br>(188Dh) | RQ1_Raw_Status_14 | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | SPKOUTL_DISABLE_DONE_STS1     | 0                 | 0                 | 0                         | 0                          | HP1R_DISABLE_DONE_STS1     | HP1L_DISABLE_DONE_STS1     | 0000h   |
| R6286<br>(188Eh) | RQ1_Raw_Status_15 | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | SPK_OVERHEAT_WARN_STS1     | SPK_OVERHEAT_STS1          | SPK_SHUTDOWN_STS1          | 0000h   |
| R6288<br>(1890h) | RQ1_Raw_Status_17 | GPIO16_STS1        | GPIO15_STS1        | GPIO14_STS1        | GPIO13_STS1        | GPIO12_STS1        | GPIO11_STS1        | GPIO10_STS1        | GPIO9_STS1        | GPIO8_STS1        | GPIO7_STS1                    | GPIO6_STS1        | GPIO5_STS1        | GPIO4_STS1                | GPIO3_STS1                 | GPIO2_STS1                 | GPIO1_STS1                 | 0000h   |
| R6293<br>(1895h) | RQ1_Raw_Status_22 | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | EVENT4_NOT_EMPTY_STS1     | EVENT3_NOT_EMPTY_STS1      | EVENT2_NOT_EMPTY_STS1      | EVENT1_NOT_EMPTY_STS1      | 0000h   |
| R6294<br>(1896h) | RQ1_Raw_Status_23 | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | EVENT4_FULL_STS1          | EVENT3_FULL_STS1           | EVENT2_FULL_STS1           | EVENT1_FULL_STS1           | 0000h   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register         | Name              | 15                          | 14              | 13              | 12                  | 11              | 10              | 9                    | 8                  | 7                  | 6              | 5                        | 4                        | 3                      | 2                      | 1                       | 0                       | Default |
|------------------|-------------------|-----------------------------|-----------------|-----------------|---------------------|-----------------|-----------------|----------------------|--------------------|--------------------|----------------|--------------------------|--------------------------|------------------------|------------------------|-------------------------|-------------------------|---------|
| R6295<br>(1897h) | RQ1_Raw_Status_24 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | EVENT4_WMARK_STS1      | EVENT3_WMARK_STS1      | EVENT2_WMARK_STS1       | EVENT1_WMARK_STS1       | 0000h   |
| R6296<br>(1898h) | RQ1_Raw_Status_25 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | 0                      | DSP3_DMA_STS1          | DSP2_DMA_STS1           | DSP1_DMA_STS1           | 0000h   |
| R6301<br>(189Dh) | RQ1_Raw_Status_30 | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | 0                      | DSP3_BUSY_STS1         | DSP2_BUSY_STS1          | DSP1_BUSY_STS1          | 0000h   |
| R6400<br>(1900h) | RQ2_Status_1      | DSP_SHARED_WR_COLL_EINT2    | 0               | 0               | CTRLIF_ERR_EINT2    | 0               | 0               | SYSCLK_FAIL_EINT2    | 0                  | BOOT_DONE_EINT2    | 0              | 0                        | 0                        | 0                      | 0                      | 0                       | 0                       | 0000h   |
| R6401<br>(1901h) | RQ2_Status_2      | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | FLL1_LOCK_EINT2    | 0                  | 0              | 0                        | 0                        | 0                      | 0                      | 0                       | 0                       | 0000h   |
| R6405<br>(1905h) | RQ2_Status_6      | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | MICDET_EINT2       | 0                  | 0              | 0                        | 0                        | 0                      | 0                      | 0                       | HPDET_EINT2             | 0000h   |
| R6406<br>(1906h) | RQ2_Status_7      | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | MICD_CLAMP_FALL_EINT2    | MICD_CLAMP_RISE_EINT2    | JD2_FALL_EINT2         | JD2_RISE_EINT2         | JD1_FALL_EINT2          | JD1_RISE_EINT2          | 0000h   |
| R6408<br>(1908h) | RQ2_Status_9      | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | 0                      | 0                      | DRG2_SIG_DET_EINT2      | DRG1_SIG_DET_EINT2      | 0000h   |
| R6410<br>(190Ah) | RQ2_Status_11     | DSP_IRQ16_EINT2             | DSP_IRQ15_EINT2 | DSP_IRQ14_EINT2 | DSP_IRQ13_EINT2     | DSP_IRQ12_EINT2 | DSP_IRQ11_EINT2 | DSP_IRQ10_EINT2      | DSP_IRQ9_EINT2     | DSP_IRQ8_EINT2     | DSP_IRQ7_EINT2 | DSP_IRQ6_EINT2           | DSP_IRQ5_EINT2           | DSP_IRQ4_EINT2         | DSP_IRQ3_EINT2         | DSP_IRQ2_EINT2          | DSP_IRQ1_EINT2          | 0000h   |
| R6411<br>(190Bh) | RQ2_Status_12     | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | HP2R_SC_EINT2          | HP2L_SC_EINT2          | HP1R_SC_EINT2           | HP1L_SC_EINT2           | 0000h   |
| R6412<br>(190Ch) | RQ2_Status_13     | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | 0                      | 0                      | HP1R_ENABLE_DONE_EINT2  | HP1L_ENABLE_DONE_EINT2  | 0000h   |
| R6413<br>(190Dh) | RQ2_Status_14     | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | 0                      | 0                      | HP1R_DISABLE_DONE_EINT2 | HP1L_DISABLE_DONE_EINT2 | 0000h   |
| R6414<br>(190Eh) | RQ2_Status_15     | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | 0                      | 0                      | SPK_OVERHEAT_WARN_EINT2 | SPK_SHUTDOWN_EINT2      | 0000h   |
| R6416<br>(1910h) | RQ2_Status_17     | GPIO16_EINT2                | GPIO15_EINT2    | GPIO14_EINT2    | GPIO13_EINT2        | GPIO12_EINT2    | GPIO11_EINT2    | GPIO10_EINT2         | GPIO9_EINT2        | GPIO8_EINT2        | GPIO7_EINT2    | GPIO6_EINT2              | GPIO5_EINT2              | GPIO4_EINT2            | GPIO3_EINT2            | GPIO2_EINT2             | GPIO1_EINT2             | 0000h   |
| R6420<br>(1914h) | RQ2_Status_21     | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | TIMER4_EINT2           | TIMER3_EINT2           | TIMER2_EINT2            | TIMER1_EINT2            | 0000h   |
| R6421<br>(1915h) | RQ2_Status_22     | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | EVENT4_NOT_EMPTY_EINT2 | EVENT3_NOT_EMPTY_EINT2 | EVENT2_NOT_EMPTY_EINT2  | EVENT1_NOT_EMPTY_EINT2  | 0000h   |
| R6422<br>(1916h) | RQ2_Status_23     | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | EVENT4_FULL_EINT2      | EVENT3_FULL_EINT2      | EVENT2_FULL_EINT2       | EVENT1_FULL_EINT2       | 0000h   |
| R6423<br>(1917h) | RQ2_Status_24     | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | EVENT4_WMARK_EINT2     | EVENT3_WMARK_EINT2     | EVENT2_WMARK_EINT2      | EVENT1_WMARK_EINT2      | 0000h   |
| R6424<br>(1918h) | RQ2_Status_25     | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | 0                      | DSP3_DMA_EINT2         | DSP2_DMA_EINT2          | DSP1_DMA_EINT2          | 0000h   |
| R6426<br>(191Ah) | RQ2_Status_27     | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | 0                      | DSP3_START1_EINT2      | DSP2_START1_EINT2       | DSP1_START1_EINT2       | 0000h   |
| R6427<br>(191Bh) | RQ2_Status_28     | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | 0                      | DSP3_START2_EINT2      | DSP2_START2_EINT2       | DSP1_START2_EINT2       | 0000h   |
| R6429<br>(191Dh) | RQ2_Status_30     | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | 0                      | DSP3_BUSY_EINT2        | DSP2_BUSY_EINT2         | DSP1_BUSY_EINT2         | 0000h   |
| R6430<br>(191Eh) | RQ2_Status_31     | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | 0                      | 0                      | 0                       | MIF1_DONE_EINT2         | 0000h   |
| R6431<br>(191Fh) | RQ2_Status_32     | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | 0                        | 0                        | 0                      | 0                      | 0                       | MIF1_BLOCK_EINT2        | 0000h   |
| R6464<br>(1940h) | RQ2_Mask_1        | IM_DSP_SHARED_WR_COLL_EINT2 | 0               | 0               | IM_CTRLIF_ERR_EINT2 | 0               | 0               | IM_SYSCLK_FAIL_EINT2 | 1                  | IM_BOOT_DONE_EINT2 | 0              | 0                        | 0                        | 0                      | 0                      | 0                       | 0                       | 9380h   |
| R6465<br>(1941h) | RQ2_Mask_2        | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | IM_FLL1_LOCK_EINT2 | 0                  | 0              | 0                        | 0                        | 0                      | 0                      | 0                       | 0                       | 0100h   |
| R6469<br>(1945h) | RQ2_Mask_6        | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | IM_MICDET_EINT2    | 0                  | 0              | 0                        | 0                        | 0                      | 0                      | 0                       | IM_HPDET_EINT2          | 0101h   |
| R6470<br>(1946h) | RQ2_Mask_7        | 0                           | 0               | 0               | 0                   | 0               | 0               | 0                    | 0                  | 0                  | 0              | IM_MICD_CLAMP_FALL_EINT2 | IM_MICD_CLAMP_RISE_EINT2 | IM_JD2_FALL_EINT2      | IM_JD2_RISE_EINT2      | IM_JD1_FALL_EINT2       | IM_JD1_RISE_EINT2       | 003Fh   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register         | Name              | 15                 | 14                 | 13                 | 12                 | 11                 | 10                 | 9                  | 8                 | 7                 | 6                             | 5                 | 4                 | 3                         | 2                          | 1                          | 0                          | Default |
|------------------|-------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|-------------------|-------------------|-------------------------------|-------------------|-------------------|---------------------------|----------------------------|----------------------------|----------------------------|---------|
| R6472<br>(1948h) | RQ2_Mask_9        | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | 0                          | IM_DRC2_SIG_DET_EINT2      | IM_DRC1_SIG_DET_EINT2      | 0003h   |
| R6474<br>(194Ah) | RQ2_Mask_11       | IM_DSP_IRQ16_EINT2 | IM_DSP_IRQ15_EINT2 | IM_DSP_IRQ14_EINT2 | IM_DSP_IRQ13_EINT2 | IM_DSP_IRQ12_EINT2 | IM_DSP_IRQ11_EINT2 | IM_DSP_IRQ10_EINT2 | IM_DSP_IRQ9_EINT2 | IM_DSP_IRQ8_EINT2 | IM_DSP_IRQ7_EINT2             | IM_DSP_IRQ6_EINT2 | IM_DSP_IRQ5_EINT2 | IM_DSP_IRQ4_EINT2         | IM_DSP_IRQ3_EINT2          | IM_DSP_IRQ2_EINT2          | IM_DSP_IRQ1_EINT2          | FFFFh   |
| R6475<br>(194Bh) | RQ2_Mask_12       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | IM_SPKOUTL_SC_EINT2           | 0                 | 0                 | IM_HP2R_SC_EINT2          | IM_HP2L_SC_EINT2           | IM_HP1R_SC_EINT2           | IM_HP1L_SC_EINT2           | 004Fh   |
| R6476<br>(194Ch) | RQ2_Mask_13       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | IM_SPKOUTL_ENABLE_DONE_EINT2  | 0                 | 0                 | 0                         | 0                          | IM_HP1R_ENABLE_DONE_EINT2  | IM_HP1L_ENABLE_DONE_EINT2  | 0043h   |
| R6477<br>(194Dh) | RQ2_Mask_14       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | IM_SPKOUTL_DISABLE_DONE_EINT2 | 0                 | 0                 | 0                         | 0                          | IM_HP1R_DISABLE_DONE_EINT2 | IM_HP1L_DISABLE_DONE_EINT2 | 0043h   |
| R6478<br>(194Eh) | RQ2_Mask_15       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | IM_SPK_OVERHEAT_WARN_EINT2 | IM_SPK_OVERHEAT_EINT2      | IM_SPK_SHUTDOWN_EINT2      | 0007h   |
| R6480<br>(1950h) | RQ2_Mask_17       | IM_GPIO16_EINT2    | IM_GPIO15_EINT2    | IM_GPIO14_EINT2    | IM_GPIO13_EINT2    | IM_GPIO12_EINT2    | IM_GPIO11_EINT2    | IM_GPIO10_EINT2    | IM_GPIO9_EINT2    | IM_GPIO8_EINT2    | IM_GPIO7_EINT2                | IM_GPIO6_EINT2    | IM_GPIO5_EINT2    | IM_GPIO4_EINT2            | IM_GPIO3_EINT2             | IM_GPIO2_EINT2             | IM_GPIO1_EINT2             | FFFFh   |
| R6484<br>(1954h) | RQ2_Mask_21       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | IM_TIMER4_EINT2           | IM_TIMER3_EINT2            | IM_TIMER2_EINT2            | IM_TIMER1_EINT2            | 000Fh   |
| R6485<br>(1955h) | RQ2_Mask_22       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | IM_EVENT4_NOT_EMPTY_EINT2 | IM_EVENT3_NOT_EMPTY_EINT2  | IM_EVENT2_NOT_EMPTY_EINT2  | IM_EVENT1_NOT_EMPTY_EINT2  | 000Fh   |
| R6486<br>(1956h) | RQ2_Mask_23       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | IM_EVENT4_FULL_EINT2      | IM_EVENT3_FULL_EINT2       | IM_EVENT2_FULL_EINT2       | IM_EVENT1_FULL_EINT2       | 000Fh   |
| R6487<br>(1957h) | RQ2_Mask_24       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | IM_EVENT4_WMARK_EINT2     | IM_EVENT3_WMARK_EINT2      | IM_EVENT2_WMARK_EINT2      | IM_EVENT1_WMARK_EINT2      | 000Fh   |
| R6488<br>(1958h) | RQ2_Mask_25       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | IM_DSP3_DMA_EINT2          | IM_DSP2_DMA_EINT2          | IM_DSP1_DMA_EINT2          | 0007h   |
| R6490<br>(195Ah) | RQ2_Mask_27       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | IM_DSP3_START1_EINT2       | IM_DSP2_START1_EINT2       | IM_DSP1_START1_EINT2       | 0007h   |
| R6491<br>(195Bh) | RQ2_Mask_28       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | IM_DSP3_START2_EINT2       | IM_DSP2_START2_EINT2       | IM_DSP1_START2_EINT2       | 0007h   |
| R6493<br>(195Dh) | RQ2_Mask_30       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | IM_DSP3_BUSY_EINT2         | IM_DSP2_BUSY_EINT2         | IM_DSP1_BUSY_EINT2         | 0007h   |
| R6494<br>(195Eh) | RQ2_Mask_31       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | IM_MIF1_DONE_EINT2         | 0001h   |
| R6495<br>(195Fh) | RQ2_Mask_32       | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | IM_MIF1_BLOCK_EINT2        | 0001h   |
| R6528<br>(1980h) | RQ2_Raw_Status_1  | 0                  | 0                  | 0                  | CTRLIF_ERR_STS2    | 0                  | 0                  | 0                  | 0                 | BOOT_DONE_STS2    | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | 0                          | 0000h   |
| R6529<br>(1981h) | RQ2_Raw_Status_2  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | 0                          | 0000h   |
| R6534<br>(1986h) | RQ2_Raw_Status_7  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | 0                          | 0000h   |
| R6536<br>(1988h) | RQ2_Raw_Status_9  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | 0                          | 0000h   |
| R6539<br>(198Bh) | RQ2_Raw_Status_12 | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | 0                          | 0000h   |
| R6540<br>(198Ch) | RQ2_Raw_Status_13 | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | 0                          | 0000h   |
| R6541<br>(198Dh) | RQ2_Raw_Status_14 | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | 0                          | 0000h   |
| R6542<br>(198Eh) | RQ2_Raw_Status_15 | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | 0                          | 0000h   |
| R6544<br>(1990h) | RQ2_Raw_Status_17 | GPIO16_STS2        | GPIO15_STS2        | GPIO14_STS2        | GPIO13_STS2        | GPIO12_STS2        | GPIO11_STS2        | GPIO10_STS2        | GPIO9_STS2        | GPIO8_STS2        | GPIO7_STS2                    | GPIO6_STS2        | GPIO5_STS2        | GPIO4_STS2                | GPIO3_STS2                 | GPIO2_STS2                 | GPIO1_STS2                 | 0000h   |
| R6549<br>(1995h) | RQ2_Raw_Status_22 | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                 | 0                 | 0                             | 0                 | 0                 | 0                         | 0                          | 0                          | 0                          | 0000h   |

**Table 6-1. Register Map Definition—16-bit region (Cont.)**

| Register      | Name                   | 15 | 14 | 13 | 12 | 11      | 10      | 9          | 8 | 7 | 6 | 5 | 4 | 3                 | 2                 | 1                 | 0                 | Default |
|---------------|------------------------|----|----|----|----|---------|---------|------------|---|---|---|---|---|-------------------|-------------------|-------------------|-------------------|---------|
| R6550 (1996h) | RQ2_Raw_Status_23      | 0  | 0  | 0  | 0  | 0       | 0       | 0          | 0 | 0 | 0 | 0 | 0 | EVENT4_FULL_STS2  | EVENT3_FULL_STS2  | EVENT2_FULL_STS2  | EVENT1_FULL_STS2  | 0000h   |
| R6551 (1997h) | RQ2_Raw_Status_24      | 0  | 0  | 0  | 0  | 0       | 0       | 0          | 0 | 0 | 0 | 0 | 0 | EVENT4_WMARK_STS2 | EVENT3_WMARK_STS2 | EVENT2_WMARK_STS2 | EVENT1_WMARK_STS2 | 0000h   |
| R6552 (1998h) | RQ2_Raw_Status_25      | 0  | 0  | 0  | 0  | 0       | 0       | 0          | 0 | 0 | 0 | 0 | 0 | 0                 | DSP3_DMA_STS2     | DSP2_DMA_STS2     | DSP1_DMA_STS2     | 0000h   |
| R6557 (199Dh) | RQ2_Raw_Status_30      | 0  | 0  | 0  | 0  | 0       | 0       | 0          | 0 | 0 | 0 | 0 | 0 | 0                 | DSP3_BUSY_STS2    | DSP2_BUSY_STS2    | DSP1_BUSY_STS2    | 0000h   |
| R6662 (1A06h) | Interrupt_Debounce_7   | 0  | 0  | 0  | 0  | 0       | 0       | 0          | 0 | 0 | 0 | 0 | 0 | MICD_CLAMP_DB     | JD2_DB            | 0                 | JD1_DB            | 0000h   |
| R6784 (1A80h) | RQ1_CTRL               | 0  | 1  | 0  | 0  | IM_IRQ1 | IRQ_POL | IRQ_OP_CFG | 0 | 0 | 0 | 0 | 0 | 0                 | 0                 | 0                 | 0                 | 4400h   |
| R6786 (1A82h) | RQ2_CTRL               | 0  | 0  | 0  | 0  | IM_IRQ2 | 0       | 0          | 0 | 0 | 0 | 0 | 0 | 0                 | 0                 | 0                 | 0                 | 0000h   |
| R6816 (1AA0h) | Interrupt_Raw_Status_1 | 0  | 0  | 0  | 0  | 0       | 0       | 0          | 0 | 0 | 0 | 0 | 0 | 0                 | 0                 | IRQ2_STS          | IRQ1_STS          | 0000h   |
| R6848 (1AC0h) | GPIO_Debounce_Config   | 0  | 0  | 0  | 0  | 0       | 0       | 0          | 0 | 0 | 0 | 0 | 0 | GP_DBTIME [3:0]   |                   |                   |                   | 0000h   |
| R6864 (1AD0h) | AOD_Pad_Ctrl           | 0  | 0  | 0  | 0  | 0       | 0       | 0          | 0 | 0 | 0 | 0 | 0 | 0                 | 0                 | RESET_PU          | RESET_PD          | 0002h   |

The 32-bit DSP register space is described in [Table 6-2](#).

**Table 6-2. Register Map Definition—32-bit region**

| Register       | Name             | 31<br>15                | 30<br>14 | 29<br>13 | 28<br>12 | 27<br>11           | 26<br>10 | 25<br>9 | 24<br>8 | 23<br>7 | 22<br>6 | 21<br>5 | 20<br>4 | 19<br>3           | 18<br>2 | 17<br>1 | 16<br>0 | Default   |
|----------------|------------------|-------------------------|----------|----------|----------|--------------------|----------|---------|---------|---------|---------|---------|---------|-------------------|---------|---------|---------|-----------|
| R12288 (3000h) | WSEQ_Sequence_1  | WSEQ_DATA_WIDTH0 [2:0]  |          |          |          | WSEQ_ADDR0 [12:0]  |          |         |         |         |         |         |         | WSEQ_DATA0 [7:0]  |         |         |         | 82253719h |
| R12290 (3002h) | WSEQ_Sequence_2  | WSEQ_DATA_WIDTH1 [2:0]  |          |          |          | WSEQ_ADDR1 [12:0]  |          |         |         |         |         |         |         | WSEQ_DATA1 [7:0]  |         |         |         | C2300001h |
| R12292 (3004h) | WSEQ_Sequence_3  | WSEQ_DATA_WIDTH2 [2:0]  |          |          |          | WSEQ_ADDR2 [12:0]  |          |         |         |         |         |         |         | WSEQ_DATA2 [7:0]  |         |         |         | 02251301h |
| R12294 (3006h) | WSEQ_Sequence_4  | WSEQ_DATA_WIDTH3 [2:0]  |          |          |          | WSEQ_ADDR3 [12:0]  |          |         |         |         |         |         |         | WSEQ_DATA3 [7:0]  |         |         |         | 8225191Fh |
| R12296 (3008h) | WSEQ_Sequence_5  | WSEQ_DATA_WIDTH4 [2:0]  |          |          |          | WSEQ_ADDR4 [12:0]  |          |         |         |         |         |         |         | WSEQ_DATA4 [7:0]  |         |         |         | 82310B00h |
| R12298 (300Ah) | WSEQ_Sequence_6  | WSEQ_DATA_WIDTH5 [2:0]  |          |          |          | WSEQ_ADDR5 [12:0]  |          |         |         |         |         |         |         | WSEQ_DATA5 [7:0]  |         |         |         | E231023Bh |
| R12300 (300Ch) | WSEQ_Sequence_7  | WSEQ_DATA_WIDTH6 [2:0]  |          |          |          | WSEQ_ADDR6 [12:0]  |          |         |         |         |         |         |         | WSEQ_DATA6 [7:0]  |         |         |         | 02313B01h |
| R12302 (300Eh) | WSEQ_Sequence_8  | WSEQ_DATA_WIDTH7 [2:0]  |          |          |          | WSEQ_ADDR7 [12:0]  |          |         |         |         |         |         |         | WSEQ_DATA7 [7:0]  |         |         |         | 62300000h |
| R12304 (3010h) | WSEQ_Sequence_9  | WSEQ_DATA_WIDTH8 [2:0]  |          |          |          | WSEQ_ADDR8 [12:0]  |          |         |         |         |         |         |         | WSEQ_DATA8 [7:0]  |         |         |         | E2314288h |
| R12306 (3012h) | WSEQ_Sequence_10 | WSEQ_DATA_WIDTH9 [2:0]  |          |          |          | WSEQ_ADDR9 [12:0]  |          |         |         |         |         |         |         | WSEQ_DATA9 [7:0]  |         |         |         | 02310B00h |
| R12308 (3014h) | WSEQ_Sequence_11 | WSEQ_DATA_WIDTH10 [2:0] |          |          |          | WSEQ_ADDR10 [12:0] |          |         |         |         |         |         |         | WSEQ_DATA10 [7:0] |         |         |         | 02310B00h |
| R12310 (3016h) | WSEQ_Sequence_12 | WSEQ_DATA_WIDTH11 [2:0] |          |          |          | WSEQ_ADDR11 [12:0] |          |         |         |         |         |         |         | WSEQ_DATA11 [7:0] |         |         |         | 02250E01h |
| R12312 (3018h) | WSEQ_Sequence_13 | WSEQ_DATA_WIDTH12 [2:0] |          |          |          | WSEQ_ADDR12 [12:0] |          |         |         |         |         |         |         | WSEQ_DATA12 [7:0] |         |         |         | 42310C02h |
| R12314 (301Ah) | WSEQ_Sequence_14 | WSEQ_DATA_WIDTH13 [2:0] |          |          |          | WSEQ_ADDR13 [12:0] |          |         |         |         |         |         |         | WSEQ_DATA13 [7:0] |         |         |         | E2310227h |
| R12316 (301Ch) | WSEQ_Sequence_15 | WSEQ_DATA_WIDTH14 [2:0] |          |          |          | WSEQ_ADDR14 [12:0] |          |         |         |         |         |         |         | WSEQ_DATA14 [7:0] |         |         |         | 02313B01h |
| R12318 (301Eh) | WSEQ_Sequence_16 | WSEQ_DATA_WIDTH15 [2:0] |          |          |          | WSEQ_ADDR15 [12:0] |          |         |         |         |         |         |         | WSEQ_DATA15 [7:0] |         |         |         | E2314266h |
| R12320 (3020h) | WSEQ_Sequence_17 | WSEQ_DATA_WIDTH16 [2:0] |          |          |          | WSEQ_ADDR16 [12:0] |          |         |         |         |         |         |         | WSEQ_DATA16 [7:0] |         |         |         | E2315294h |
| R12322 (3022h) | WSEQ_Sequence_18 | WSEQ_DATA_WIDTH17 [2:0] |          |          |          | WSEQ_ADDR17 [12:0] |          |         |         |         |         |         |         | WSEQ_DATA17 [7:0] |         |         |         | 02310B00h |
| R12324 (3024h) | WSEQ_Sequence_19 | WSEQ_DATA_WIDTH18 [2:0] |          |          |          | WSEQ_ADDR18 [12:0] |          |         |         |         |         |         |         | WSEQ_DATA18 [7:0] |         |         |         | 02310B00h |
| R12326 (3026h) | WSEQ_Sequence_20 | WSEQ_DATA_WIDTH19 [2:0] |          |          |          | WSEQ_ADDR19 [12:0] |          |         |         |         |         |         |         | WSEQ_DATA19 [7:0] |         |         |         | E2251734h |
| R12328 (3028h) | WSEQ_Sequence_21 | WSEQ_DATA_WIDTH20 [2:0] |          |          |          | WSEQ_ADDR20 [12:0] |          |         |         |         |         |         |         | WSEQ_DATA20 [7:0] |         |         |         | 0225F501h |
| R12330 (302Ah) | WSEQ_Sequence_22 | WSEQ_DATA_WIDTH21 [2:0] |          |          |          | WSEQ_ADDR21 [12:0] |          |         |         |         |         |         |         | WSEQ_DATA21 [7:0] |         |         |         | 0000F000h |









**Table 6-2. Register Map Definition—32-bit region (Cont.)**

| Register          | Name              | 31<br>15                 | 30<br>14 | 29<br>13 | 28<br>12                 | 27<br>11 | 26<br>10 | 25<br>9            | 24<br>8 | 23<br>7 | 22<br>6 | 21<br>5 | 20<br>4 | 19<br>3 | 18<br>2 | 17<br>1 | 16<br>0 | Default |           |
|-------------------|-------------------|--------------------------|----------|----------|--------------------------|----------|----------|--------------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|-----------|
| R12620<br>(314Ch) | WSEQ_Sequence_167 | WSEQ_DATA_WIDTH166 [2:0] |          |          | WSEQ_ADDR166 [12:0]      |          |          | WSEQ_DATA166 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY166 [3:0]      |          |          | WSEQ_DATA_START166 [3:0] |          |          | WSEQ_DATA166 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12622<br>(314Eh) | WSEQ_Sequence_168 | WSEQ_DATA_WIDTH167 [2:0] |          |          | WSEQ_ADDR167 [12:0]      |          |          | WSEQ_DATA167 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY167 [3:0]      |          |          | WSEQ_DATA_START167 [3:0] |          |          | WSEQ_DATA167 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12624<br>(3150h) | WSEQ_Sequence_169 | WSEQ_DATA_WIDTH168 [2:0] |          |          | WSEQ_ADDR168 [12:0]      |          |          | WSEQ_DATA168 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY168 [3:0]      |          |          | WSEQ_DATA_START168 [3:0] |          |          | WSEQ_DATA168 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12626<br>(3152h) | WSEQ_Sequence_170 | WSEQ_DATA_WIDTH169 [2:0] |          |          | WSEQ_ADDR169 [12:0]      |          |          | WSEQ_DATA169 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY169 [3:0]      |          |          | WSEQ_DATA_START169 [3:0] |          |          | WSEQ_DATA169 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12628<br>(3154h) | WSEQ_Sequence_171 | WSEQ_DATA_WIDTH170 [2:0] |          |          | WSEQ_ADDR170 [12:0]      |          |          | WSEQ_DATA170 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY170 [3:0]      |          |          | WSEQ_DATA_START170 [3:0] |          |          | WSEQ_DATA170 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12630<br>(3156h) | WSEQ_Sequence_172 | WSEQ_DATA_WIDTH171 [2:0] |          |          | WSEQ_ADDR171 [12:0]      |          |          | WSEQ_DATA171 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY171 [3:0]      |          |          | WSEQ_DATA_START171 [3:0] |          |          | WSEQ_DATA171 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12632<br>(3158h) | WSEQ_Sequence_173 | WSEQ_DATA_WIDTH172 [2:0] |          |          | WSEQ_ADDR172 [12:0]      |          |          | WSEQ_DATA172 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY172 [3:0]      |          |          | WSEQ_DATA_START172 [3:0] |          |          | WSEQ_DATA172 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12634<br>(315Ah) | WSEQ_Sequence_174 | WSEQ_DATA_WIDTH173 [2:0] |          |          | WSEQ_ADDR173 [12:0]      |          |          | WSEQ_DATA173 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY173 [3:0]      |          |          | WSEQ_DATA_START173 [3:0] |          |          | WSEQ_DATA173 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12636<br>(315Ch) | WSEQ_Sequence_175 | WSEQ_DATA_WIDTH174 [2:0] |          |          | WSEQ_ADDR174 [12:0]      |          |          | WSEQ_DATA174 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY174 [3:0]      |          |          | WSEQ_DATA_START174 [3:0] |          |          | WSEQ_DATA174 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12638<br>(315Eh) | WSEQ_Sequence_176 | WSEQ_DATA_WIDTH175 [2:0] |          |          | WSEQ_ADDR175 [12:0]      |          |          | WSEQ_DATA175 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY175 [3:0]      |          |          | WSEQ_DATA_START175 [3:0] |          |          | WSEQ_DATA175 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12640<br>(3160h) | WSEQ_Sequence_177 | WSEQ_DATA_WIDTH176 [2:0] |          |          | WSEQ_ADDR176 [12:0]      |          |          | WSEQ_DATA176 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY176 [3:0]      |          |          | WSEQ_DATA_START176 [3:0] |          |          | WSEQ_DATA176 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12642<br>(3162h) | WSEQ_Sequence_178 | WSEQ_DATA_WIDTH177 [2:0] |          |          | WSEQ_ADDR177 [12:0]      |          |          | WSEQ_DATA177 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY177 [3:0]      |          |          | WSEQ_DATA_START177 [3:0] |          |          | WSEQ_DATA177 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12644<br>(3164h) | WSEQ_Sequence_179 | WSEQ_DATA_WIDTH178 [2:0] |          |          | WSEQ_ADDR178 [12:0]      |          |          | WSEQ_DATA178 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY178 [3:0]      |          |          | WSEQ_DATA_START178 [3:0] |          |          | WSEQ_DATA178 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12646<br>(3166h) | WSEQ_Sequence_180 | WSEQ_DATA_WIDTH179 [2:0] |          |          | WSEQ_ADDR179 [12:0]      |          |          | WSEQ_DATA179 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY179 [3:0]      |          |          | WSEQ_DATA_START179 [3:0] |          |          | WSEQ_DATA179 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12648<br>(3168h) | WSEQ_Sequence_181 | WSEQ_DATA_WIDTH180 [2:0] |          |          | WSEQ_ADDR180 [12:0]      |          |          | WSEQ_DATA180 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY180 [3:0]      |          |          | WSEQ_DATA_START180 [3:0] |          |          | WSEQ_DATA180 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12650<br>(316Ah) | WSEQ_Sequence_182 | WSEQ_DATA_WIDTH181 [2:0] |          |          | WSEQ_ADDR181 [12:0]      |          |          | WSEQ_DATA181 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY181 [3:0]      |          |          | WSEQ_DATA_START181 [3:0] |          |          | WSEQ_DATA181 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12652<br>(316Ch) | WSEQ_Sequence_183 | WSEQ_DATA_WIDTH182 [2:0] |          |          | WSEQ_ADDR182 [12:0]      |          |          | WSEQ_DATA182 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY182 [3:0]      |          |          | WSEQ_DATA_START182 [3:0] |          |          | WSEQ_DATA182 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12654<br>(316Eh) | WSEQ_Sequence_184 | WSEQ_DATA_WIDTH183 [2:0] |          |          | WSEQ_ADDR183 [12:0]      |          |          | WSEQ_DATA183 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY183 [3:0]      |          |          | WSEQ_DATA_START183 [3:0] |          |          | WSEQ_DATA183 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12656<br>(3170h) | WSEQ_Sequence_185 | WSEQ_DATA_WIDTH184 [2:0] |          |          | WSEQ_ADDR184 [12:0]      |          |          | WSEQ_DATA184 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY184 [3:0]      |          |          | WSEQ_DATA_START184 [3:0] |          |          | WSEQ_DATA184 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12658<br>(3172h) | WSEQ_Sequence_186 | WSEQ_DATA_WIDTH185 [2:0] |          |          | WSEQ_ADDR185 [12:0]      |          |          | WSEQ_DATA185 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY185 [3:0]      |          |          | WSEQ_DATA_START185 [3:0] |          |          | WSEQ_DATA185 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12660<br>(3174h) | WSEQ_Sequence_187 | WSEQ_DATA_WIDTH186 [2:0] |          |          | WSEQ_ADDR186 [12:0]      |          |          | WSEQ_DATA186 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY186 [3:0]      |          |          | WSEQ_DATA_START186 [3:0] |          |          | WSEQ_DATA186 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12662<br>(3176h) | WSEQ_Sequence_188 | WSEQ_DATA_WIDTH187 [2:0] |          |          | WSEQ_ADDR187 [12:0]      |          |          | WSEQ_DATA187 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY187 [3:0]      |          |          | WSEQ_DATA_START187 [3:0] |          |          | WSEQ_DATA187 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12664<br>(3178h) | WSEQ_Sequence_189 | WSEQ_DATA_WIDTH188 [2:0] |          |          | WSEQ_ADDR188 [12:0]      |          |          | WSEQ_DATA188 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY188 [3:0]      |          |          | WSEQ_DATA_START188 [3:0] |          |          | WSEQ_DATA188 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12666<br>(317Ah) | WSEQ_Sequence_190 | WSEQ_DATA_WIDTH189 [2:0] |          |          | WSEQ_ADDR189 [12:0]      |          |          | WSEQ_DATA189 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY189 [3:0]      |          |          | WSEQ_DATA_START189 [3:0] |          |          | WSEQ_DATA189 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12668<br>(317Ch) | WSEQ_Sequence_191 | WSEQ_DATA_WIDTH190 [2:0] |          |          | WSEQ_ADDR190 [12:0]      |          |          | WSEQ_DATA190 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY190 [3:0]      |          |          | WSEQ_DATA_START190 [3:0] |          |          | WSEQ_DATA190 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12670<br>(317Eh) | WSEQ_Sequence_192 | WSEQ_DATA_WIDTH191 [2:0] |          |          | WSEQ_ADDR191 [12:0]      |          |          | WSEQ_DATA191 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY191 [3:0]      |          |          | WSEQ_DATA_START191 [3:0] |          |          | WSEQ_DATA191 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12672<br>(3180h) | WSEQ_Sequence_193 | WSEQ_DATA_WIDTH192 [2:0] |          |          | WSEQ_ADDR192 [12:0]      |          |          | WSEQ_DATA192 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY192 [3:0]      |          |          | WSEQ_DATA_START192 [3:0] |          |          | WSEQ_DATA192 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12674<br>(3182h) | WSEQ_Sequence_194 | WSEQ_DATA_WIDTH193 [2:0] |          |          | WSEQ_ADDR193 [12:0]      |          |          | WSEQ_DATA193 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY193 [3:0]      |          |          | WSEQ_DATA_START193 [3:0] |          |          | WSEQ_DATA193 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12676<br>(3184h) | WSEQ_Sequence_195 | WSEQ_DATA_WIDTH194 [2:0] |          |          | WSEQ_ADDR194 [12:0]      |          |          | WSEQ_DATA194 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY194 [3:0]      |          |          | WSEQ_DATA_START194 [3:0] |          |          | WSEQ_DATA194 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12678<br>(3186h) | WSEQ_Sequence_196 | WSEQ_DATA_WIDTH195 [2:0] |          |          | WSEQ_ADDR195 [12:0]      |          |          | WSEQ_DATA195 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY195 [3:0]      |          |          | WSEQ_DATA_START195 [3:0] |          |          | WSEQ_DATA195 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12680<br>(3188h) | WSEQ_Sequence_197 | WSEQ_DATA_WIDTH196 [2:0] |          |          | WSEQ_ADDR196 [12:0]      |          |          | WSEQ_DATA196 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY196 [3:0]      |          |          | WSEQ_DATA_START196 [3:0] |          |          | WSEQ_DATA196 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12682<br>(318Ah) | WSEQ_Sequence_198 | WSEQ_DATA_WIDTH197 [2:0] |          |          | WSEQ_ADDR197 [12:0]      |          |          | WSEQ_DATA197 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY197 [3:0]      |          |          | WSEQ_DATA_START197 [3:0] |          |          | WSEQ_DATA197 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12684<br>(318Ch) | WSEQ_Sequence_199 | WSEQ_DATA_WIDTH198 [2:0] |          |          | WSEQ_ADDR198 [12:0]      |          |          | WSEQ_DATA198 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY198 [3:0]      |          |          | WSEQ_DATA_START198 [3:0] |          |          | WSEQ_DATA198 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12686<br>(318Eh) | WSEQ_Sequence_200 | WSEQ_DATA_WIDTH199 [2:0] |          |          | WSEQ_ADDR199 [12:0]      |          |          | WSEQ_DATA199 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY199 [3:0]      |          |          | WSEQ_DATA_START199 [3:0] |          |          | WSEQ_DATA199 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12688<br>(3190h) | WSEQ_Sequence_201 | WSEQ_DATA_WIDTH200 [2:0] |          |          | WSEQ_ADDR200 [12:0]      |          |          | WSEQ_DATA200 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY200 [3:0]      |          |          | WSEQ_DATA_START200 [3:0] |          |          | WSEQ_DATA200 [7:0] |         |         |         |         |         |         |         |         |         |         |           |
| R12690<br>(3192h) | WSEQ_Sequence_202 | WSEQ_DATA_WIDTH201 [2:0] |          |          | WSEQ_ADDR201 [12:0]      |          |          | WSEQ_DATA201 [7:0] |         |         |         |         |         |         |         |         |         |         | 00000000h |
|                   |                   | WSEQ_DELAY201 [3:0]      |          |          | WSEQ_DATA_START201 [3:0] |          |          | WSEQ_DATA201 [7:0] |         |         |         |         |         |         |         |         |         |         |           |



**Table 6-2. Register Map Definition—32-bit region (Cont.)**

| Register            | Name              | 31<br>15                 | 30<br>14 | 29<br>13 | 28<br>12 | 27<br>11                 | 26<br>10                | 25<br>9 | 24<br>8 | 23<br>7             | 22<br>6 | 21<br>5                | 20<br>4                | 19<br>3 | 18<br>2            | 17<br>1              | 16<br>0        | Default                    |           |           |  |          |  |  |  |          |
|---------------------|-------------------|--------------------------|----------|----------|----------|--------------------------|-------------------------|---------|---------|---------------------|---------|------------------------|------------------------|---------|--------------------|----------------------|----------------|----------------------------|-----------|-----------|--|----------|--|--|--|----------|
| R12764<br>(31DCh)   | WSEQ_Sequence_239 | WSEQ_DATA_WIDTH238 [2:0] |          |          |          | WSEQ_DATA_START238 [3:0] |                         |         |         | WSEQ_ADDR238 [12:0] |         |                        |                        |         |                    |                      |                | WSEQ_DATA238 [7:0]         |           |           |  | FFFFFFFh |  |  |  |          |
| R12766<br>(31DEh)   | WSEQ_Sequence_240 | WSEQ_DATA_WIDTH239 [2:0] |          |          |          | WSEQ_DATA_START239 [3:0] |                         |         |         | WSEQ_ADDR239 [12:0] |         |                        |                        |         |                    |                      |                | WSEQ_DATA239 [7:0]         |           |           |  | FFFFFFFh |  |  |  |          |
| R12768<br>(31E0h)   | WSEQ_Sequence_241 | WSEQ_DATA_WIDTH240 [2:0] |          |          |          | WSEQ_DATA_START240 [3:0] |                         |         |         | WSEQ_ADDR240 [12:0] |         |                        |                        |         |                    |                      |                | WSEQ_DATA240 [7:0]         |           |           |  | FFFFFFFh |  |  |  |          |
| R12770<br>(31E2h)   | WSEQ_Sequence_242 | WSEQ_DATA_WIDTH241 [2:0] |          |          |          | WSEQ_DATA_START241 [3:0] |                         |         |         | WSEQ_ADDR241 [12:0] |         |                        |                        |         |                    |                      |                | WSEQ_DATA241 [7:0]         |           |           |  | FFFFFFFh |  |  |  |          |
| R12772<br>(31E4h)   | WSEQ_Sequence_243 | WSEQ_DATA_WIDTH242 [2:0] |          |          |          | WSEQ_DATA_START242 [3:0] |                         |         |         | WSEQ_ADDR242 [12:0] |         |                        |                        |         |                    |                      |                | WSEQ_DATA242 [7:0]         |           |           |  | FFFFFFFh |  |  |  |          |
| R12774<br>(31E6h)   | WSEQ_Sequence_244 | WSEQ_DATA_WIDTH243 [2:0] |          |          |          | WSEQ_DATA_START243 [3:0] |                         |         |         | WSEQ_ADDR243 [12:0] |         |                        |                        |         |                    |                      |                | WSEQ_DATA243 [7:0]         |           |           |  | FFFFFFFh |  |  |  |          |
| R12776<br>(31E8h)   | WSEQ_Sequence_245 | WSEQ_DATA_WIDTH244 [2:0] |          |          |          | WSEQ_DATA_START244 [3:0] |                         |         |         | WSEQ_ADDR244 [12:0] |         |                        |                        |         |                    |                      |                | WSEQ_DATA244 [7:0]         |           |           |  | FFFFFFFh |  |  |  |          |
| R12778<br>(31EAh)   | WSEQ_Sequence_246 | WSEQ_DATA_WIDTH245 [2:0] |          |          |          | WSEQ_DATA_START245 [3:0] |                         |         |         | WSEQ_ADDR245 [12:0] |         |                        |                        |         |                    |                      |                | WSEQ_DATA245 [7:0]         |           |           |  | FFFFFFFh |  |  |  |          |
| R12780<br>(31ECh)   | WSEQ_Sequence_247 | WSEQ_DATA_WIDTH246 [2:0] |          |          |          | WSEQ_DATA_START246 [3:0] |                         |         |         | WSEQ_ADDR246 [12:0] |         |                        |                        |         |                    |                      |                | WSEQ_DATA246 [7:0]         |           |           |  | FFFFFFFh |  |  |  |          |
| R12782<br>(31EEh)   | WSEQ_Sequence_248 | WSEQ_DATA_WIDTH247 [2:0] |          |          |          | WSEQ_DATA_START247 [3:0] |                         |         |         | WSEQ_ADDR247 [12:0] |         |                        |                        |         |                    |                      |                | WSEQ_DATA247 [7:0]         |           |           |  | FFFFFFFh |  |  |  |          |
| R12784<br>(31F0h)   | WSEQ_Sequence_249 | WSEQ_DATA_WIDTH248 [2:0] |          |          |          | WSEQ_DATA_START248 [3:0] |                         |         |         | WSEQ_ADDR248 [12:0] |         |                        |                        |         |                    |                      |                | WSEQ_DATA248 [7:0]         |           |           |  | FFFFFFFh |  |  |  |          |
| R12786<br>(31F2h)   | WSEQ_Sequence_250 | WSEQ_DATA_WIDTH249 [2:0] |          |          |          | WSEQ_DATA_START249 [3:0] |                         |         |         | WSEQ_ADDR249 [12:0] |         |                        |                        |         |                    |                      |                | WSEQ_DATA249 [7:0]         |           |           |  | FFFFFFFh |  |  |  |          |
| R12788<br>(31F4h)   | WSEQ_Sequence_251 | WSEQ_DATA_WIDTH250 [2:0] |          |          |          | WSEQ_DATA_START250 [3:0] |                         |         |         | WSEQ_ADDR250 [12:0] |         |                        |                        |         |                    |                      |                | WSEQ_DATA250 [7:0]         |           |           |  | FFFFFFFh |  |  |  |          |
| R12790<br>(31F6h)   | WSEQ_Sequence_252 | WSEQ_DATA_WIDTH251 [2:0] |          |          |          | WSEQ_DATA_START251 [3:0] |                         |         |         | WSEQ_ADDR251 [12:0] |         |                        |                        |         |                    |                      |                | WSEQ_DATA251 [7:0]         |           |           |  | FFFFFFFh |  |  |  |          |
| R12792<br>(31F8h)   | OTP_HPDET_Cal_1   | HP_OFFSET_11 [7:0]       |          |          |          |                          |                         |         |         | HP_OFFSET_10 [7:0]  |         |                        |                        |         |                    |                      |                | HP_OFFSET_00 [7:0]         |           |           |  |          |  |  |  | 0000000h |
| R12794<br>(31FAh)   | OTP_HPDET_Cal_2   | SPARE2 [7:0]             |          |          |          |                          |                         |         |         | SPARE1 [7:0]        |         |                        |                        |         |                    |                      |                | HP_GRADIENT_0X [7:0]       |           |           |  |          |  |  |  | 0000000h |
| R12796<br>(31FCh)   | OTP_Security_1    | SECURITY_VALUE [63:48]   |          |          |          |                          |                         |         |         |                     |         |                        |                        |         |                    |                      |                | 0000000h                   |           |           |  |          |  |  |  |          |
| R12798<br>(31FEh)   | OTP_Security_2    | SECURITY_VALUE [31:16]   |          |          |          |                          |                         |         |         |                     |         |                        |                        |         |                    |                      |                | 0000000h                   |           |           |  |          |  |  |  |          |
| R262146<br>(40002h) | MIF1_I2C_CONFIG_2 | 0                        | 0        | 0        | 0        | 0                        | 0                       | 0       | 0       | 0                   | 0       | 0                      | 0                      | 0       | 0                  | 0                    | 0              | MIF1_ADDR_MODE             |           |           |  |          |  |  |  |          |
| R262148<br>(40004h) | MIF1_I2C_CONFIG_3 | 0                        | 0        | 0        | 0        | 0                        | MIF1_HS_MASTER_ID [2:0] |         |         | 0                   | 0       | 0                      | 0                      | 0       | MIF1_NACK_RESPONSE | MIF1_SCL_MON_ENA     | MIF1_RPT_START | MIF1_START_BYTE_ENA        |           |           |  |          |  |  |  |          |
| R262152<br>(40008h) | MIF1_I2C_CONFIG_5 | 0                        | 0        | 0        | 0        | 0                        | 0                       | 0       | 0       | 0                   | 0       | 0                      | 0                      | 0       | 0                  | 0                    | 0              | MIF1_WDT_ENA               |           |           |  |          |  |  |  |          |
| R262272<br>(40080h) | MIF1_I2C_STATUS_1 | 0                        | 0        | 0        | 0        | 0                        | 0                       | 0       | 0       | 0                   | 0       | 0                      | 0                      | 0       | 0                  | 0                    | 0              | MIF1_WDT_TIMEOUT_STS       |           |           |  |          |  |  |  |          |
| R262400<br>(40100h) | MIF1_CONFIG_1     | 0                        | 0        | 0        | 0        | 0                        | 0                       | 0       | 0       | 0                   | 0       | 0                      | 0                      | 0       | 0                  | 0                    | 0              | MIF1_START                 |           |           |  |          |  |  |  |          |
| R262404<br>(40104h) | MIF1_CONFIG_3     | 0                        | 0        | 0        | 0        | 0                        | 0                       | 0       | 0       | 0                   | 0       | 0                      | 0                      | 0       | 0                  | MIF1_WORD_SIZE [1:0] |                | MIF1_READ_WRITE_SEL        |           |           |  |          |  |  |  |          |
| R262406<br>(40106h) | MIF1_CONFIG_4     | 0                        | 0        | 0        | 0        | 0                        | 0                       | 0       | 0       | 0                   | 0       | 0                      | MIF1_TX_LENGTH [20:16] |         |                    |                      |                |                            | 00000000h |           |  |          |  |  |  |          |
| R262416<br>(40110h) | MIF1_CONFIG_5     | MIF1_TX_LENGTH [15:0]    |          |          |          |                          |                         |         |         |                     |         | MIF1_RX_LENGTH [20:16] |                        |         |                    |                      |                |                            |           | 00000000h |  |          |  |  |  |          |
| R262418<br>(40112h) | MIF1_CONFIG_6     | 0                        | 0        | 0        | 0        | 0                        | 0                       | 0       | 0       | 0                   | 0       | 0                      | 0                      | 0       | 0                  | 0                    | 0              | MIF1_TX_BLOCK_LENGTH [7:0] |           |           |  |          |  |  |  |          |
| R262420<br>(40114h) | MIF1_CONFIG_7     | 0                        | 0        | 0        | 0        | 0                        | 0                       | 0       | 0       | 0                   | 0       | 0                      | 0                      | 0       | 0                  | 0                    | 0              | MIF1_RX_BLOCK_LENGTH [7:0] |           |           |  |          |  |  |  |          |
| R262422<br>(40116h) | MIF1_CONFIG_8     | 0                        | 0        | 0        | 0        | 0                        | 0                       | 0       | 0       | 0                   | 0       | 0                      | 0                      | 0       | 0                  | 0                    | 0              | MIF1_TX_DONE               |           |           |  |          |  |  |  |          |
| R262528<br>(40180h) | MIF1_STATUS_1     | 0                        | 0        | 0        | 0        | 0                        | 0                       | 0       | 0       | 0                   | 0       | 0                      | 0                      | 0       | 0                  | 0                    | 0              | MIF1_TX_REQUEST            |           |           |  |          |  |  |  |          |











**Table 6-2. Register Map Definition—32-bit region (Cont.)**

| Register            | Name                        | 31<br>15                     | 30<br>14           | 29<br>13           | 28<br>12           | 27<br>11                  | 26<br>10           | 25<br>9            | 24<br>8                  | 23<br>7                  | 22<br>6           | 21<br>5           | 20<br>4           | 19<br>3           | 18<br>2                    | 17<br>1           | 16<br>0             | Default             |           |
|---------------------|-----------------------------|------------------------------|--------------------|--------------------|--------------------|---------------------------|--------------------|--------------------|--------------------------|--------------------------|-------------------|-------------------|-------------------|-------------------|----------------------------|-------------------|---------------------|---------------------|-----------|
| R295948<br>(4840Ch) | EVENTLOG3_FIFO_<br>CONTROL1 | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 00000001h           |           |
|                     |                             | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | EVENTLOG3_FIFO_WMARK [3:0] |                   |                     |                     |           |
| R295950<br>(4840Eh) | EVENTLOG3_FIFO_<br>POINTER1 | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | EVENTLOG3_FULL    | EVENTLOG3_WMARK_STS | EVENTLOG3_NOT_EMPTY | 00000000h |
|                     |                             | 0                            | 0                  | 0                  | 0                  | EVENTLOG3_FIFO_WPTR [3:0] |                    |                    |                          |                          | 0                 | 0                 | 0                 | 0                 | EVENTLOG3_FIFO_RPTR [3:0]  |                   |                     |                     |           |
| R295968<br>(48420h) | EVENTLOG3_CH_<br>ENABLE1    | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
| R296000<br>(48440h) | EVENTLOG3_CH1_<br>DEFINE    | EVENTLOG3_CH16_ENA           | EVENTLOG3_CH15_ENA | EVENTLOG3_CH14_ENA | EVENTLOG3_CH13_ENA | EVENTLOG3_CH12_ENA        | EVENTLOG3_CH11_ENA | EVENTLOG3_CH10_ENA | EVENTLOG3_CH9_ENA        | EVENTLOG3_CH8_ENA        | EVENTLOG3_CH7_ENA | EVENTLOG3_CH6_ENA | EVENTLOG3_CH5_ENA | EVENTLOG3_CH4_ENA | EVENTLOG3_CH3_ENA          | EVENTLOG3_CH2_ENA | EVENTLOG3_CH1_ENA   | 00000000h           |           |
|                     |                             | EVENTLOG3_CH1_DB             | EVENTLOG3_CH1_POL  | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH1_SEL [8:0]  |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296002<br>(48442h) | EVENTLOG3_CH2_<br>DEFINE    | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH2_DB             | EVENTLOG3_CH2_POL  | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH2_SEL [8:0]  |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296004<br>(48444h) | EVENTLOG3_CH3_<br>DEFINE    | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH3_DB             | EVENTLOG3_CH3_POL  | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH3_SEL [8:0]  |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296006<br>(48446h) | EVENTLOG3_CH4_<br>DEFINE    | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH4_DB             | EVENTLOG3_CH4_POL  | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH4_SEL [8:0]  |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296008<br>(48448h) | EVENTLOG3_CH5_<br>DEFINE    | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH5_DB             | EVENTLOG3_CH5_POL  | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH5_SEL [8:0]  |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296010<br>(4844Ah) | EVENTLOG3_CH6_<br>DEFINE    | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH6_DB             | EVENTLOG3_CH6_POL  | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH6_SEL [8:0]  |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296012<br>(4844Ch) | EVENTLOG3_CH7_<br>DEFINE    | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH7_DB             | EVENTLOG3_CH7_POL  | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH7_SEL [8:0]  |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296014<br>(4844Eh) | EVENTLOG3_CH8_<br>DEFINE    | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH8_DB             | EVENTLOG3_CH8_POL  | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH8_SEL [8:0]  |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296016<br>(48450h) | EVENTLOG3_CH9_<br>DEFINE    | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH9_DB             | EVENTLOG3_CH9_POL  | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH9_SEL [8:0]  |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296018<br>(48452h) | EVENTLOG3_CH10_<br>DEFINE   | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH10_DB            | EVENTLOG3_CH10_POL | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH10_SEL [8:0] |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296020<br>(48454h) | EVENTLOG3_CH11_<br>DEFINE   | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH11_DB            | EVENTLOG3_CH11_POL | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH11_SEL [8:0] |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296022<br>(48456h) | EVENTLOG3_CH12_<br>DEFINE   | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH12_DB            | EVENTLOG3_CH12_POL | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH12_SEL [8:0] |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296024<br>(48458h) | EVENTLOG3_CH13_<br>DEFINE   | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH13_DB            | EVENTLOG3_CH13_POL | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH13_SEL [8:0] |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296026<br>(4845Ah) | EVENTLOG3_CH14_<br>DEFINE   | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH14_DB            | EVENTLOG3_CH14_POL | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH14_SEL [8:0] |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296028<br>(4845Ch) | EVENTLOG3_CH15_<br>DEFINE   | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH15_DB            | EVENTLOG3_CH15_POL | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH15_SEL [8:0] |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296030<br>(4845Eh) | EVENTLOG3_CH16_<br>DEFINE   | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | EVENTLOG3_CH16_DB            | EVENTLOG3_CH16_POL | 0                  | 0                  | 0                         | 0                  | 0                  | EVENTLOG3_CH16_SEL [8:0] |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296064<br>(48480h) | EVENTLOG3_FIFO0_<br>READ    | 0                            | 0                  | 0                  | 0                  | 0                         | 0                  | 0                  | 0                        | 0                        | 0                 | 0                 | 0                 | 0                 | 0                          | 0                 | 0                   | 0                   | 00000000h |
|                     |                             | 0                            | 0                  | 0                  | 0                  | EVENTLOG3_FIFO0_POL       | 0                  | 0                  | 0                        | EVENTLOG3_FIFO0_ID [8:0] |                   |                   |                   |                   |                            |                   |                     |                     |           |
| R296066<br>(48482h) | EVENTLOG3_FIFO0_<br>TIME    | EVENTLOG3_FIFO0_TIME [31:16] |                    |                    |                    |                           |                    |                    |                          |                          |                   |                   |                   |                   |                            |                   |                     | 00000000h           |           |
|                     |                             | EVENTLOG3_FIFO0_TIME [15:0]  |                    |                    |                    |                           |                    |                    |                          |                          |                   |                   |                   |                   |                            |                   |                     |                     |           |















**Table 6-2. Register Map Definition—32-bit region (Cont.)**

| Register            | Name                                  | 31<br>15                                                              | 30<br>14            | 29<br>13 | 28<br>12 | 27<br>11 | 26<br>10 | 25<br>9 | 24<br>8 | 23<br>7 | 22<br>6 | 21<br>5 | 20<br>4                   | 19<br>3 | 18<br>2 | 17<br>1 | 16<br>0 | Default  |
|---------------------|---------------------------------------|-----------------------------------------------------------------------|---------------------|----------|----------|----------|----------|---------|---------|---------|---------|---------|---------------------------|---------|---------|---------|---------|----------|
| R330788<br>(50C24h) | RA_DSPGP_SET2_<br>Thread_Ctrl_3       | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
| R330792<br>(50C28h) | RA_DSPGP_SET2_<br>Thread_Ctrl_Debug_1 | RA_DSPGP_SET2_IN_USE_DBG0 [31:16]<br>RA_DSPGP_SET2_IN_USE_DBG0 [15:0] |                     |          |          |          |          |         |         |         |         |         |                           |         |         |         |         | 0000000h |
| R330800<br>(50C30h) | RA_DSPGP_SET3_<br>Thread_Ctrl_1       | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
|                     | RA_DSPGP_SET3_IN_USE_STS              | RA_DSPGP_SET3_IN_USE_STS                                              | RA_DSPGP_SET3_SHARE |          |          |          |          |         |         |         |         |         | RA_DSPGP_SET3_OWNER [4:0] |         |         |         |         |          |
| R330802<br>(50C32h) | RA_DSPGP_SET3_<br>Thread_Ctrl_2       | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
| R330804<br>(50C34h) | RA_DSPGP_SET3_<br>Thread_Ctrl_3       | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
| R330808<br>(50C38h) | RA_DSPGP_SET3_<br>Thread_Ctrl_Debug_1 | RA_DSPGP_SET3_IN_USE_DBG0 [31:16]<br>RA_DSPGP_SET3_IN_USE_DBG0 [15:0] |                     |          |          |          |          |         |         |         |         |         |                           |         |         |         |         | 0000000h |
| R330816<br>(50C40h) | RA_DSPGP_SET4_<br>Thread_Ctrl_1       | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
|                     | RA_DSPGP_SET4_IN_USE_STS              | RA_DSPGP_SET4_IN_USE_STS                                              | RA_DSPGP_SET4_SHARE |          |          |          |          |         |         |         |         |         | RA_DSPGP_SET4_OWNER [4:0] |         |         |         |         |          |
| R330818<br>(50C42h) | RA_DSPGP_SET4_<br>Thread_Ctrl_2       | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
| R330820<br>(50C44h) | RA_DSPGP_SET4_<br>Thread_Ctrl_3       | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
| R330824<br>(50C48h) | RA_DSPGP_SET4_<br>Thread_Ctrl_Debug_1 | RA_DSPGP_SET4_IN_USE_DBG0 [31:16]<br>RA_DSPGP_SET4_IN_USE_DBG0 [15:0] |                     |          |          |          |          |         |         |         |         |         |                           |         |         |         |         | 0000000h |
| R331776<br>(51000h) | RA_SPARE_A_Thread_<br>Ctrl_1          | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
| R331780<br>(51004h) | RA_SPARE_A_Thread_<br>Ctrl_2          | RA_SPARE_A_STS [15:0]<br>RA_SPARE_A_SHARE_STS [15:0]                  |                     |          |          |          |          |         |         |         |         |         |                           |         |         |         |         | 0000000h |
| R331784<br>(51008h) | RA_SPARE_A_Thread_<br>Ctrl_3          | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000010h |
| R331792<br>(51010h) | RA_SPARE_A1_<br>Thread_Ctrl_1         | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
|                     | RA_SPARE_A1_IN_USE_STS                | RA_SPARE_A1_IN_USE_STS                                                | RA_SPARE_A1_SHARE   |          |          |          |          |         |         |         |         |         | RA_SPARE_A1_OWNER [4:0]   |         |         |         |         |          |
| R331794<br>(51012h) | RA_SPARE_A1_<br>Thread_Ctrl_2         | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
| R331796<br>(51014h) | RA_SPARE_A1_<br>Thread_Ctrl_3         | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
| R331800<br>(51018h) | RA_SPARE_A1_<br>Thread_Ctrl_Debug_1   | RA_SPARE_A1_IN_USE_DBG0 [31:16]<br>RA_SPARE_A1_IN_USE_DBG0 [15:0]     |                     |          |          |          |          |         |         |         |         |         |                           |         |         |         |         | 0000000h |
| R331808<br>(51020h) | RA_SPARE_A2_<br>Thread_Ctrl_1         | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
|                     | RA_SPARE_A2_IN_USE_STS                | RA_SPARE_A2_IN_USE_STS                                                | RA_SPARE_A2_SHARE   |          |          |          |          |         |         |         |         |         | RA_SPARE_A2_OWNER [4:0]   |         |         |         |         |          |
| R331810<br>(51022h) | RA_SPARE_A2_<br>Thread_Ctrl_2         | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
| R331812<br>(51024h) | RA_SPARE_A2_<br>Thread_Ctrl_3         | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
| R331816<br>(51028h) | RA_SPARE_A2_<br>Thread_Ctrl_Debug_1   | RA_SPARE_A2_IN_USE_DBG0 [31:16]<br>RA_SPARE_A2_IN_USE_DBG0 [15:0]     |                     |          |          |          |          |         |         |         |         |         |                           |         |         |         |         | 0000000h |
| R331824<br>(51030h) | RA_SPARE_A3_<br>Thread_Ctrl_1         | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
|                     | RA_SPARE_A3_IN_USE_STS                | RA_SPARE_A3_IN_USE_STS                                                | RA_SPARE_A3_SHARE   |          |          |          |          |         |         |         |         |         | RA_SPARE_A3_OWNER [4:0]   |         |         |         |         |          |
| R331826<br>(51032h) | RA_SPARE_A3_<br>Thread_Ctrl_2         | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
| R331828<br>(51034h) | RA_SPARE_A3_<br>Thread_Ctrl_3         | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
| R331832<br>(51038h) | RA_SPARE_A3_<br>Thread_Ctrl_Debug_1   | RA_SPARE_A3_IN_USE_DBG0 [31:16]<br>RA_SPARE_A3_IN_USE_DBG0 [15:0]     |                     |          |          |          |          |         |         |         |         |         |                           |         |         |         |         | 0000000h |
| R331840<br>(51040h) | RA_SPARE_A4_<br>Thread_Ctrl_1         | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
|                     | RA_SPARE_A4_IN_USE_STS                | RA_SPARE_A4_IN_USE_STS                                                | RA_SPARE_A4_SHARE   |          |          |          |          |         |         |         |         |         | RA_SPARE_A4_OWNER [4:0]   |         |         |         |         |          |
| R331842<br>(51042h) | RA_SPARE_A4_<br>Thread_Ctrl_2         | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
| R331844<br>(51044h) | RA_SPARE_A4_<br>Thread_Ctrl_3         | 0                                                                     | 0                   | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                         | 0       | 0       | 0       | 0       | 0000000h |
| R331848<br>(51048h) | RA_SPARE_A4_<br>Thread_Ctrl_Debug_1   | RA_SPARE_A4_IN_USE_DBG0 [31:16]<br>RA_SPARE_A4_IN_USE_DBG0 [15:0]     |                     |          |          |          |          |         |         |         |         |         |                           |         |         |         |         | 0000000h |















**Table 6-2. Register Map Definition—32-bit region (Cont.)**

| Register              | Name              | 31<br>15                   | 30<br>14 | 29<br>13 | 28<br>12 | 27<br>11 | 26<br>10 | 25<br>9 | 24<br>8 | 23<br>7 | 22<br>6 | 21<br>5 | 20<br>4                | 19<br>3 | 18<br>2 | 17<br>1 | 16<br>0 | Default   |
|-----------------------|-------------------|----------------------------|----------|----------|----------|----------|----------|---------|---------|---------|---------|---------|------------------------|---------|---------|---------|---------|-----------|
| R2096730<br>(1FFE5Ah) | DSP3_Ext_window_D | DSP3<br>EXT_D<br>PSIZE[16] | 0        | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                      | 0       | 0       | 0       | 0       | 00000000h |
|                       |                   | DSP3_EXT_D_PAGE [15:0]     |          |          |          |          |          |         |         |         |         |         |                        |         |         |         |         |           |
| R2096736<br>(1FFE60h) | DSP3_Identity     | 0                          | 0        | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | 0                      | 0       | 0       | 0       | 0       | 00000000h |
|                       |                   | 0                          | 0        | 0        | 0        | 0        | 0        | 0       | 0       | 0       | 0       | 0       | DSP3_CORE_NUMBER [4:0] |         |         |         |         |           |

## 7 Thermal Characteristics

**Table 7-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics**

| Parameter                                                  | Symbol        | WLCSP | Units |
|------------------------------------------------------------|---------------|-------|-------|
| Junction-to-ambient thermal resistance                     | $\theta_{JA}$ | 34.5  | °C/W  |
| Junction-to-board thermal resistance                       | $\theta_{JB}$ | 7.6   | °C/W  |
| Junction-to-case thermal resistance                        | $\theta_{JC}$ | 0.895 | °C/W  |
| Junction-to-board thermal-characterization parameter       | $\Psi_{JB}$   | 7.6   | °C/W  |
| Junction-to-package-top thermal-characterization parameter | $\Psi_{JT}$   | 0.075 | °C/W  |

**Notes:**

- Natural convection at the maximum recommended operating temperature  $T_A$  (see [Table 3-3](#))
- Four-layer, 2s2p PCB as specified by JESD51-9 and JESD51-11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51-12

## 8 Package Dimensions

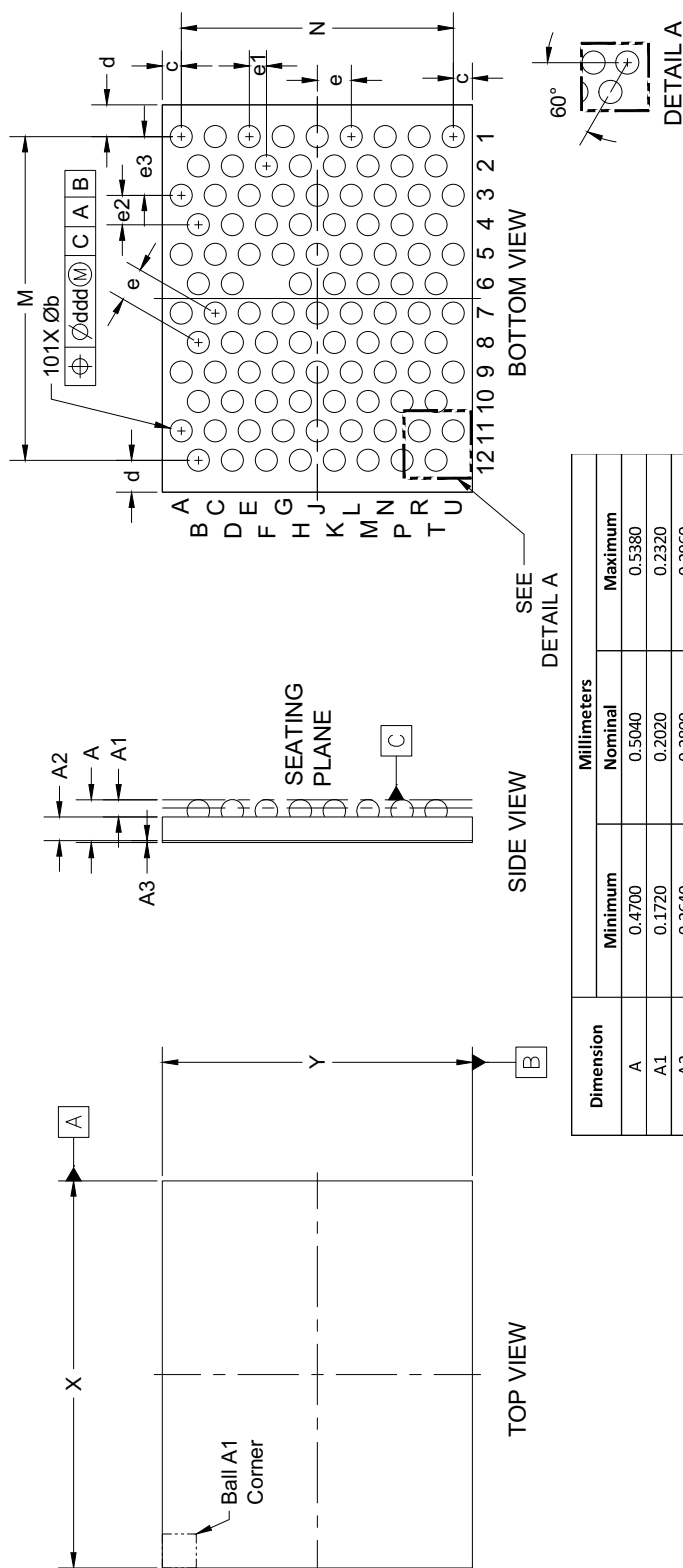


Figure 8-1. Package Drawing POD00152 Rev A

**Notes:** Controlling dimension is millimeters.  
 Dimensioning and tolerances per ASME Y 14.5-2009. The Ball A1 position indicator is for illustration purposes only. Dimension "b" applies to the solder sphere diameter and is measured at the maximum solder sphere diameter, parallel to primary Datum C.  
 X/Y Tolerances can apply to an individual edge increasing or decreasing by 30um.

## 9 Ordering Information

**Table 9-1. Ordering Information**

| Product | Description                          | Package        | Halogen Free | Pb Free | Grade      | Temperature Range | Container                  | Order #      |
|---------|--------------------------------------|----------------|--------------|---------|------------|-------------------|----------------------------|--------------|
| CS47L35 | Smart Codec with Low-Power Audio DSP | 101-ball WLCSP | Yes          | Yes     | Commercial | –40 to +85°C      | Tape and Reel <sup>1</sup> | CS47L35-CWZR |

1. Reel quantity = 7000

## 10 References

- MIPI Alliance, *MIPI Alliance Specification for Serial Low-Power Inter-Chip Media Bus (SLIMbus)*. <http://www.mipi.org>
- Google Inc, *Android Wired Headset Specification, Version 1.1*. <https://source.android.com/accessories/headset-spec.html>
- International Electrotechnical Commission, *IEC60958-3 Digital Audio Interface—Consumer*. <http://www.ansi.org/>

## 11 Revision History

**Table 11-1. Revision History**

| Revision      | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F1<br>JUN '16 | <ul style="list-style-type: none"> <li>• Series resistor recommended on FLLVDD connection (<a href="#">Section 2</a>, <a href="#">Table 3-3</a>).</li> <li>• THD+N test limits updated (<a href="#">Table 3-9</a>).</li> <li>• Typical power consumption updated (<a href="#">Table 3-23</a>).</li> <li>• DMA data word format (DSPn_DMA_WORD_SEL) control field added (<a href="#">Section 4.4.3</a>).</li> <li>• GPn_OP_CFG and GPn_DIR field descriptions updated (<a href="#">Section 4.14.1</a>, <a href="#">Section 4.14.3</a>).</li> <li>• Deleted I2C support for multiple register read from previous register address (<a href="#">Section 4.17.2</a>).</li> <li>• PCB layout guidelines updated (<a href="#">Section 5.1.6</a>).</li> </ul> |
| F2<br>JAN '17 | <ul style="list-style-type: none"> <li>• Clarification of PDM input/output digital signal levels (<a href="#">Section 4.2.7</a>, <a href="#">Section 4.11.4</a>).</li> <li>• Clarification of DSPn_DUALMEM_COLLISION_ADDR field (<a href="#">Section 4.4.1</a>, <a href="#">Table 4-25</a>).</li> <li>• FLL configuration and example settings updated (<a href="#">Section 4.16.9</a>).</li> <li>• Correction to FLL synchronizer example settings (<a href="#">Table 4-98</a>).</li> <li>• Thermal characteristics updated (<a href="#">Section 7</a>).</li> </ul>                                                                                                                                                                                   |
| F3<br>SEP '18 | <ul style="list-style-type: none"> <li>• Correction to HPD_DACVAL limit (<a href="#">Section 4.12.4.2</a>).</li> <li>• Fixed incorrect labeling describing FLL configuration (<a href="#">Fig. 4-65</a>).</li> <li>• Default value of CP2_ENA corrected (<a href="#">Table 4-112</a>).</li> <li>• Package outline drawing updated for clarity (<a href="#">Section 8</a>).</li> </ul>                                                                                                                                                                                                                                                                                                                                                                  |

---

## Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.

To find the one nearest you, go to [www.cirrus.com](http://www.cirrus.com).

---

### IMPORTANT NOTICE

The products and services of Cirrus Logic International (UK) Limited; Cirrus Logic, Inc.; and other companies in the Cirrus Logic group (collectively either "Cirrus Logic" or "Cirrus") are sold subject to Cirrus Logic's terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. Software is provided pursuant to applicable license terms. Cirrus Logic reserves the right to make changes to its products and specifications or to discontinue any product or service without notice. Customers should therefore obtain the latest version of relevant information from Cirrus Logic to verify that the information is current and complete. Testing and other quality control techniques are utilized to the extent Cirrus Logic deems necessary. Specific testing of all parameters of each device is not necessarily performed. In order to minimize risks associated with customer applications, the customer must use adequate design and operating safeguards to minimize inherent or procedural hazards. Cirrus Logic is not liable for applications assistance or customer product design. The customer is solely responsible for its product design, including the specific manner in which it uses Cirrus Logic components, and certain uses or product designs may require an intellectual property license from a third party. Features and operations described herein are for illustrative purposes only and do not constitute a suggestion or instruction to adopt a particular product design or a particular mode of operation for a Cirrus Logic component.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS LOGIC PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, NUCLEAR SYSTEMS, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS LOGIC PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS LOGIC DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS LOGIC PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS LOGIC PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS LOGIC, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

This document is the property of Cirrus Logic, and you may not use this document in connection with any legal analysis concerning Cirrus Logic products described herein. No license to any technology or intellectual property right of Cirrus Logic or any third party is granted herein, including but not limited to any patent right, copyright, mask work right, or other intellectual property rights. Any provision or publication of any third party's products or services does not constitute Cirrus Logic's approval, license, warranty or endorsement thereof. Cirrus Logic gives consent for copies to be made of the information contained herein only for use within your organization with respect to Cirrus Logic integrated circuits or other products of Cirrus Logic, and only if the reproduction is without alteration and is accompanied by all associated copyright, proprietary and other notices and conditions (including this notice). This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale. This document and its information is provided "AS IS" without warranty of any kind (express or implied). All statutory warranties and conditions are excluded to the fullest extent possible. No responsibility is assumed by Cirrus Logic for the use of information herein, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. Cirrus Logic, Cirrus, the Cirrus Logic logo design, and SoundClear are among the trademarks of Cirrus Logic. Other brand and product names may be trademarks or service marks of their respective owners.

Copyright © 2015–2018 Cirrus Logic, Inc. All rights reserved.

MIPI and SLIMbus are trademarks or registered trademarks of MIPI Alliance, Inc.

USB-C is a trademark of USB Implementers Forum.

Android is a trademark of Google, Inc.

SPI is a trademark of Motorola.