# DC5304P-ADC User Guide

## Introduction

The DC5304P-ADC is a daughter card for the Cirrus Logic Dunglass (CDB-PROAUDIO) system for high performance ADC, DAC and codec devices. This user guide details how to connect the DC5304P-ADC to a Dunglass (CDB-PROAUDIO) system platform and how to get started.

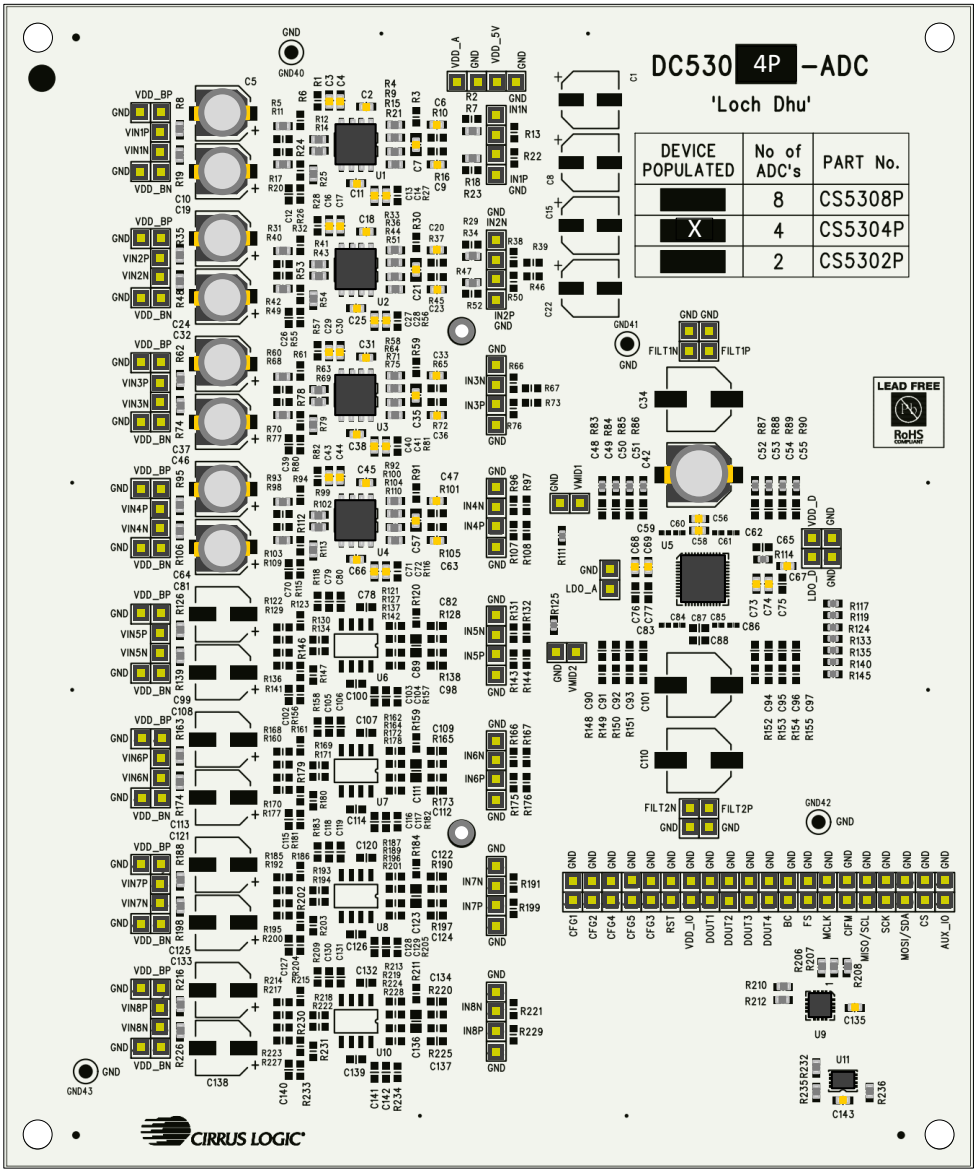


**Figure 1: DC5304P-ADC Daughter Card**

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# 1 Hardware Connections

The Dunglass system supports interchangeable daughter cards for a variety of ADC, DAC and codec devices.

**Caution:**

Daughter cards should not be inserted or removed while the Dunglass system is powered. Fully disconnect or power down external power supply before changing daughter cards.

For more information on the Dunglass (CDB-PROAUDIO) platform, refer to the CDB-PROAUDIO User Guide.

## 1.1 How to Connect DC5304P-ADC onto the Dunglass System

The DC5304P is a 4-header daughter card and should be plugged onto DCJ1, DCJ2, DCJ3 & DCJ4. The daughter card connectors are keyed and will only plug in one way. There is also an alignment dot on each board to help with placement.

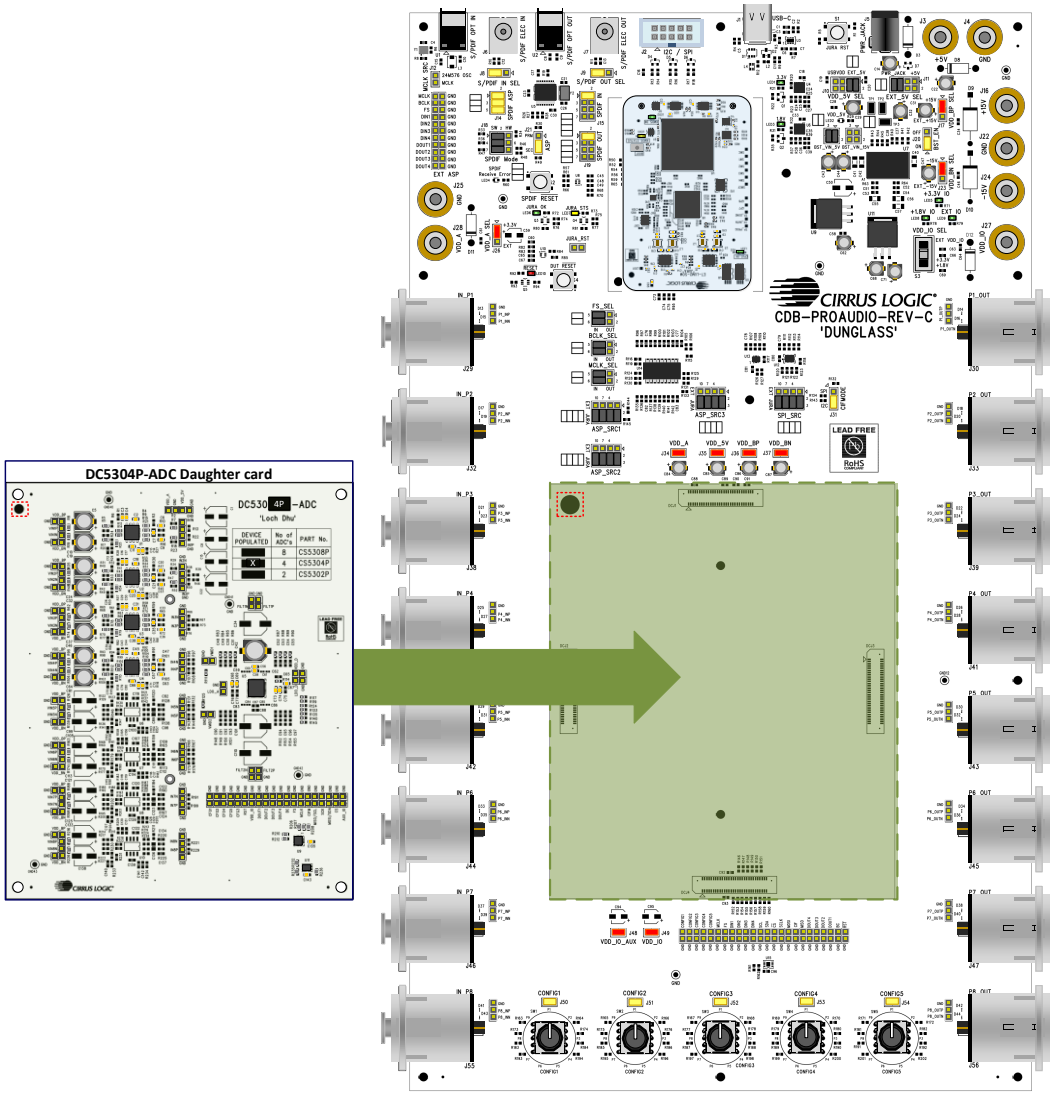



**Figure 2: How to Connect DC5304P-ADC onto the Dunglass System**

## 1.2 USB & Power Connection

Dunglass is powered using a 5V external power supply and is controlled via a single USB connection. The Jura module supports the following functions via the USB connection:

- I2C/SPI communications to control device and board.
- Multichannel USB streaming audio (USB class 2).

The board is provided with a USB-A to USB-C cable and a 5V wall supply.

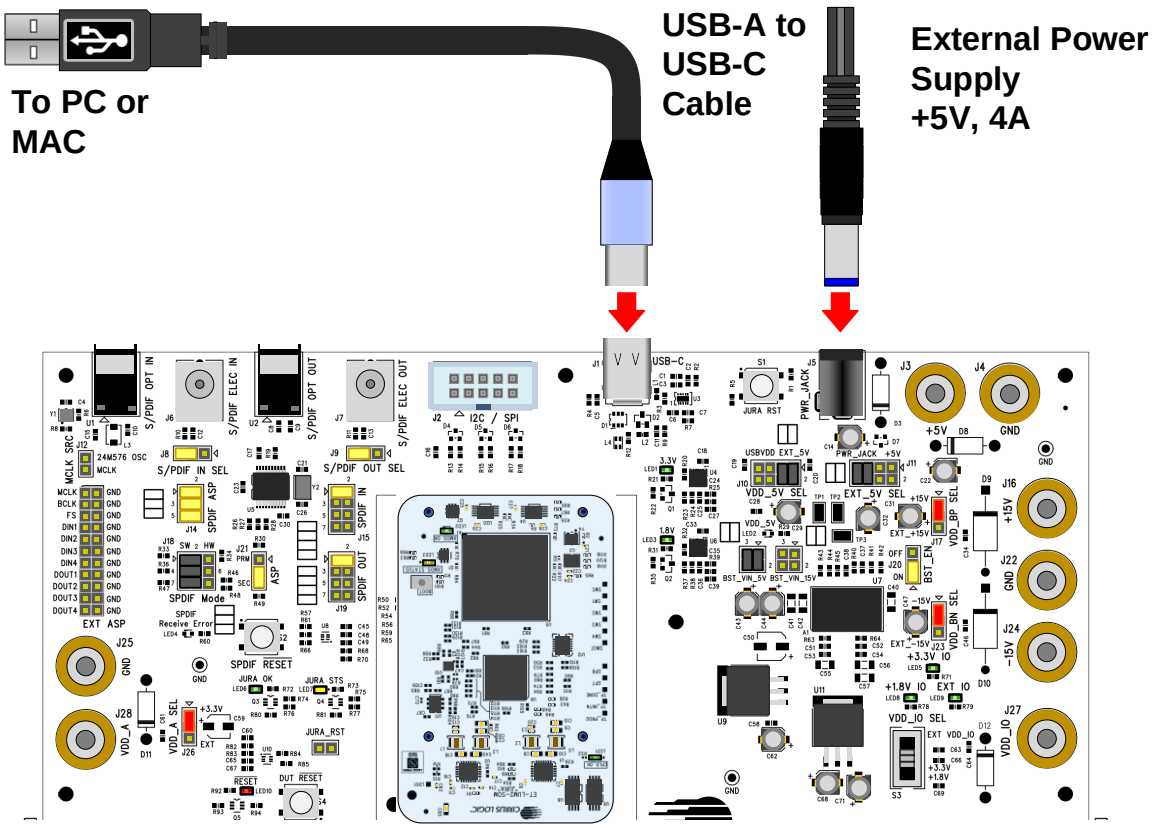



**Figure 3: Dunglass (CDB-PROAUDIO) USB & Power Connection**

A Total Phase Aardvark connector can be used for I2C/SPI communication. Refer to the CDB-PROAUDIO User Guide for more details.

### 1.2.1 JURA Module

The Jura module supports I2C/SPI communication to control the Dunglass system and daughter card; it also enables multichannel USB streaming audio (USB audio Class 2).

The Jura module is connected to the Dunglass board as shown below:

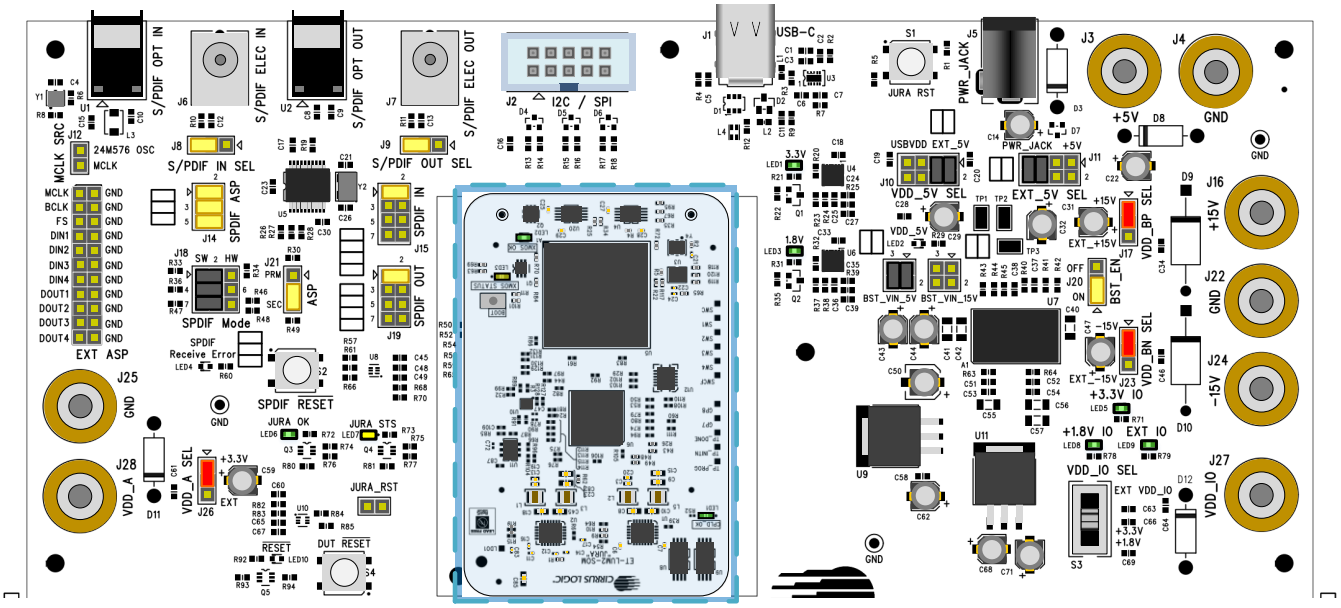



**Figure 4: How to Connect JURA Module to Dunglass System**

### 1.2.2 Dunglass Boot Procedure with Jura Module

The USB-C cable must be connected between the Dunglass system and the PC/Mac prior to powering up the board.

The boot time of the Dunglass system varies depending on the version of firmware on the Jura module but is typically in the range of 2 to 5 seconds after applying power to the board.

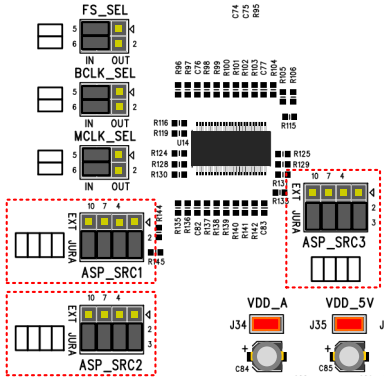
## 1.3 Routing the Digital Audio Signals

The digital audio paths to/from the daughter card can be routed to the Jura module, or else to the EXT ASP header and S/PDIF transceiver. The routing is configured using the ASP_SRC1, ASP_SRC2 & ASP_SRC3 headers.

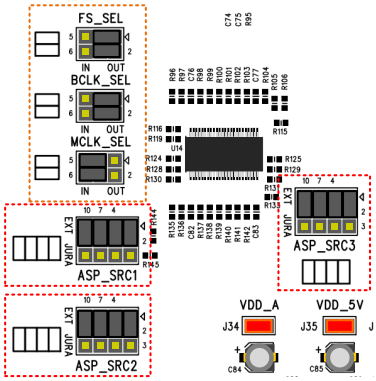
- JURA = Digital audio signals routed to Jura module.
- EXT = Digital audio signals routed to EXT ASP header/SPDIF.

The ASP_SRC1, ASP_SRC2 & ASP_SRC3 headers are configured as shown in Table 1.

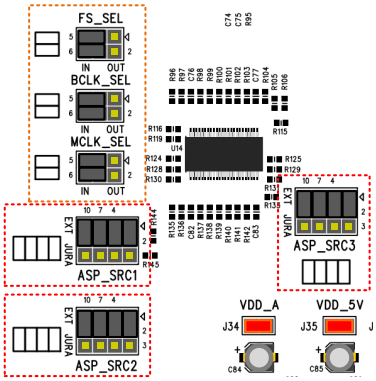
**Table 1 Digital Signal Routing**




**Jura Module Primary Mode**




**EXT ASP / SPDIF Primary Mode**




**EXT ASP / SPDIF Secondary Mode**

The Jura module always operates in Primary Mode – the MCLK, BCLK and FSYNC are generated by the Jura module, as inputs to the daughter card.

If the digital audio is routed to the EXT ASP header and S/PDIF transceiver, the direction of the MCLK, BCLK, and FSYNC signals must be configured using the MCLK_SEL, BCLK_SEL & FS_SEL headers:

- The MCLK_SEL sets the direction of the MCLK signal to/from the daughter card; IN configures the EXT_ASP header/SPDIF as the MCLK input to the daughter card; OUT configures the daughter card as the MCLK source.
- The BCLK_SEL and FS_SEL links select the direction of the BCLK and FSYNC signals to/from the daughter card.

Note that the EXT ASP header and S/PDIF transceiver use 3.3V logic levels; a level shifter is incorporated to interface with the configured VDD_IO domain.

# 2 Driver Installation and SoundClear Studio Support

## 2.1 SoundClear Studio

SoundClear Studio (SCS) is a PC/Mac-based tool used to configure Cirrus Logic devices. The tools suite provides support for evaluation and development and can be used with Dunglass system and associated daughter cards.

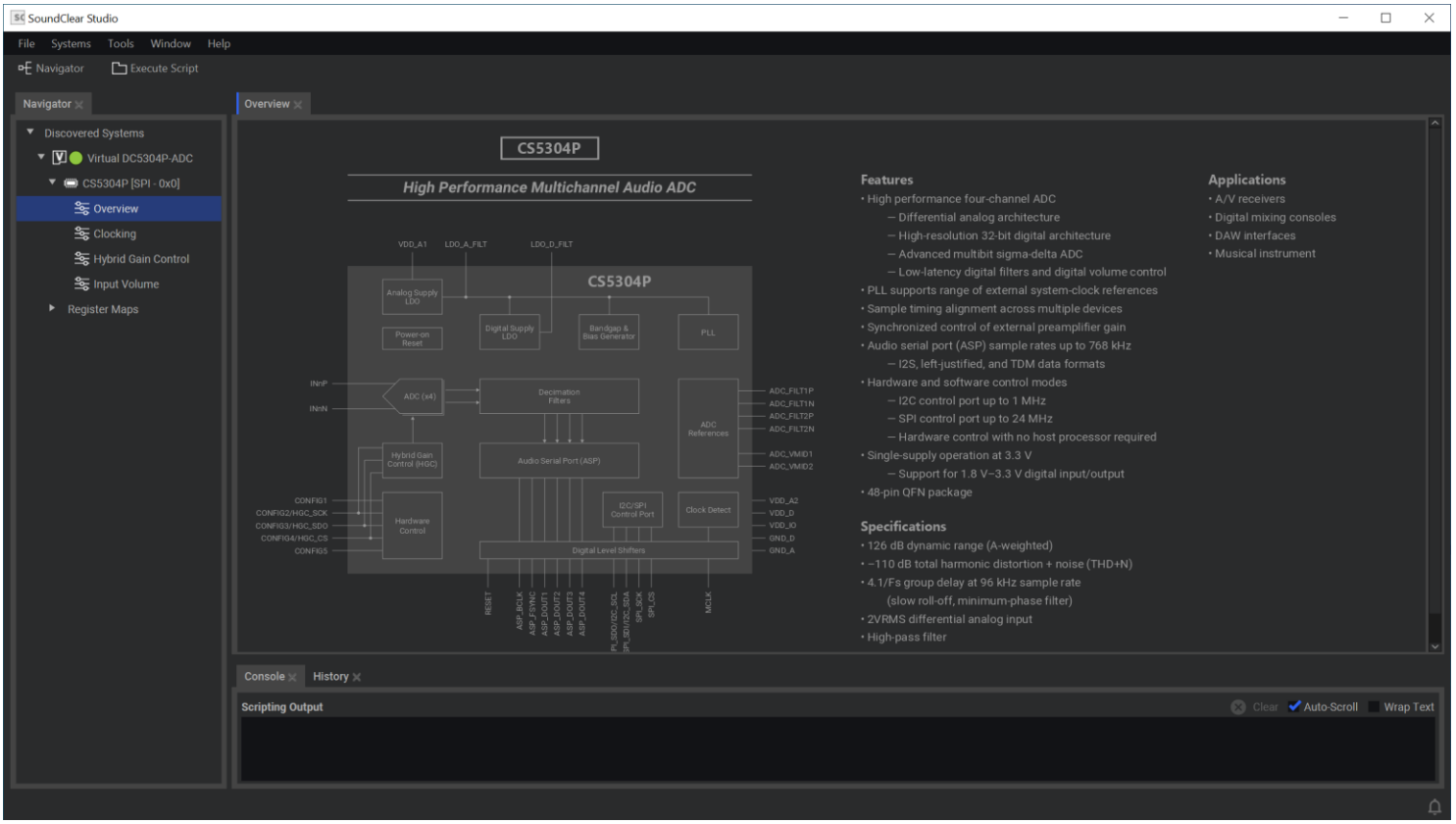



**Figure 5: SoundClear Studio**

### 2.1.1 Download SoundClear Studio Software & Drivers

SoundClear Studio and associated software collateral required for the Dunglass system can be downloaded from the CS5304P product page: https://cirrus.com/products/cs5304p/

The required components are as follows:

- **SoundClear Studio 2.1**. Run the appropriate installer on your Windows or macOS computer to install SoundClear Studio.
- **CS5304P SCS Package**. Install this in SoundClear Studio to incorporate the CS5304P-specific software components in SoundClear Studio. See Section 2.2.1 for details on how to install an SCS package.
- **Jura Windows Setup**. On Windows computers, run the Cirrus Logic USB Audio Setup to install the driver that enables SoundClear Studio to communicate with the Jura board. (There is no additional setup required on macOS.)

## 2.2 SoundClear Studio Quick Start Guide

### 2.2.1 Installing Packages

Each daughter card has its own individual SoundClear Studio package that must be installed separately from the main SoundClear Studio Software. These are installed from the main menu using **"File → Install Package..."**. Multiple packages can be installed together by selecting more than one using the file dialog.

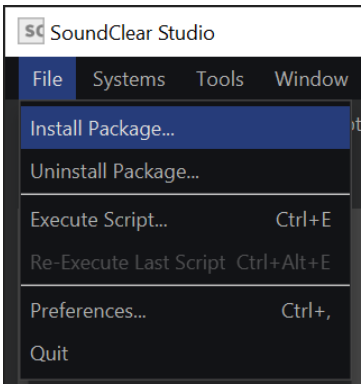



**Figure 6: SoundClear Studio – Installing Board Packages**

### 2.2.2 SoundClear Studio User Guide

The SoundClear Studio User Guide can be accessed from the main menu using **"Help → Open Help Contents..."**

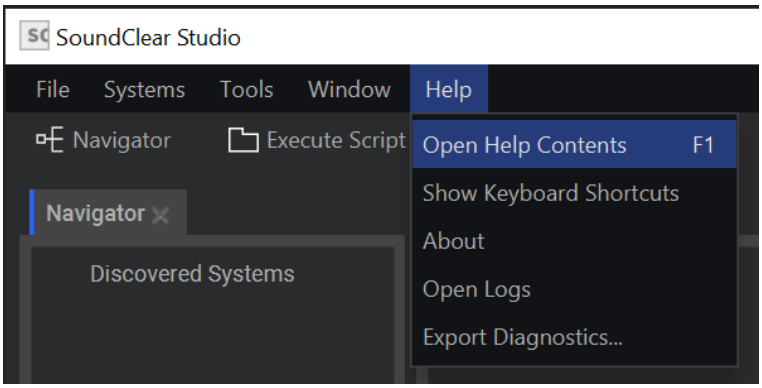



**Figure 7: SoundClear Studio – User Guide**

### 2.2.3 Creating a Virtual System

A virtual (non-hardware) version of the system can be created using **"Systems → Add Virtual System..."**

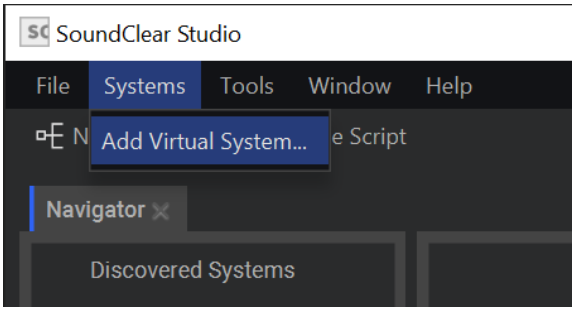



**Figure 8: SoundClear Studio – Creating a Virtual System**

This opens a dialog to select an installed system (shown here is the DC5304P-ADC):

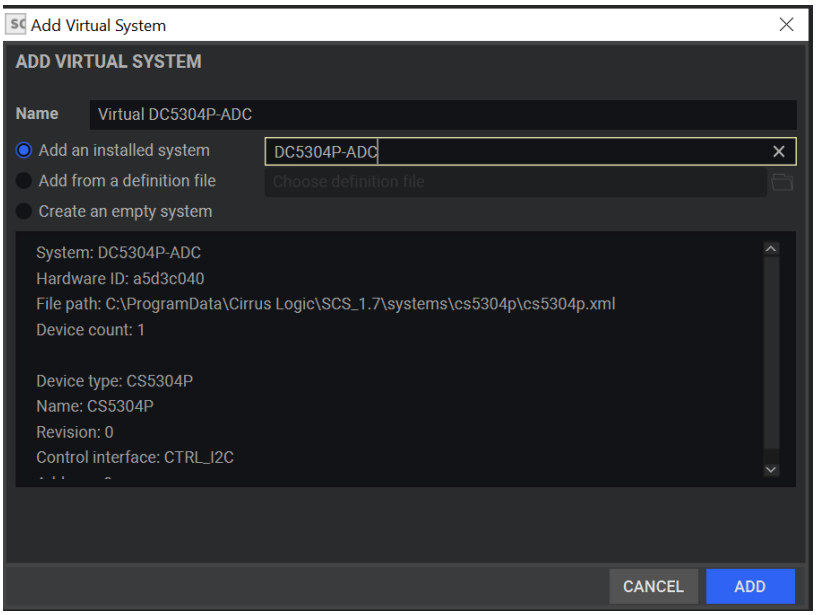



**Figure 9: SoundClear Studio – Adding a Virtual System**

Once created, a virtual system enables the user to interact with virtual versions of the device register map and helper panels.

### 2.2.4 Adding an Existing System

SoundClear Studio automatically detects board hardware such as the Jura module and Cirrus Logic devices. In the event of devices not being detected automatically, a device can be added manually. Right click on the system and select **"Add Device…"**

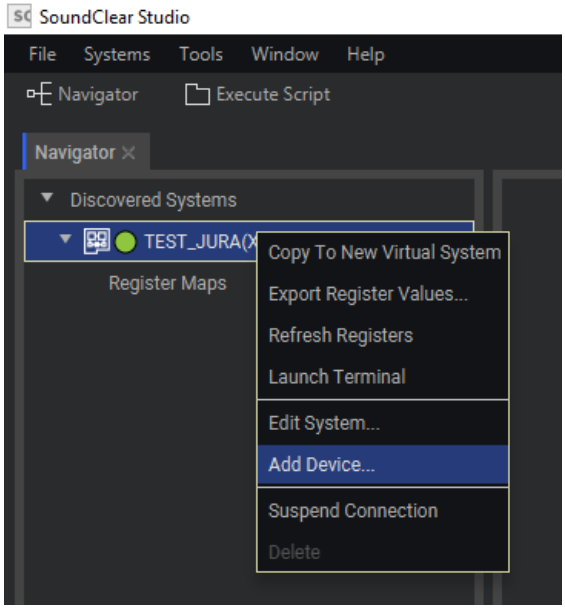



**Figure 10: SoundClear Studio – Adding an Existing System**

Then select the device from those installed, along with the protocol and address of the part (this can be edited again by right clicking on the device and selected **"Edit Device..."**):

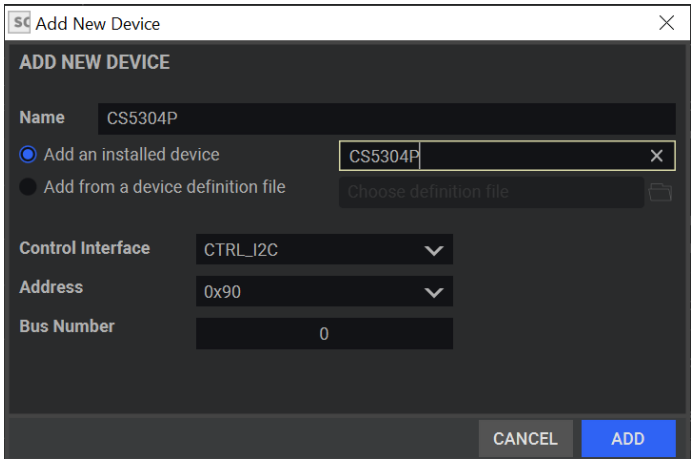



**Figure 11: SoundClear Studio – Adding an Existing System**

### 2.2.5 Executing SoundClear Studio Scripts

SoundClear Studio provides the ability to interact with the device register map using Python scripts. These scripts can sequence register operations to configure the desire into desired states, which can then be executed from SoundClear Studio using **"File→Execute Script…"**

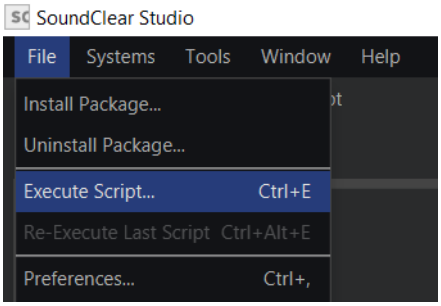



**Figure 12: SoundClear Studio – Executing Script**

The daughter card SoundClear Studio package installs a set of scripts to configure the device for common use cases. These are available at:

- Windows: C:\ProgramData\Cirrus Logic\SCS_1.7\scripts
- Mac: /Users/Shared/Cirrus Logic/SCS_1.7/scripts

## 3 DC5304P-ADC Software Mode Quick Start

After installing the SoundClear Studio software and DC5304P-ADC board package, follow the steps below to get up and running quickly:

- Connect the hardware as shown in Figure 2
- Connect USB cable to PC
- Power up the system and ensure JURA OK, 1.8V, 3.3V, VDD_5V LEDs are illuminated.
- Configure signal routing as shown in Table 1
  - For SPDIF output see Section 5
- Start SoundClear Studio
  - SoundClear Studio should auto-detect the DC5304P-ADC daughter card. If not, follow the procedure specified in Section 2.2.4
- Run one of the scripts from the following location.
  - Windows script location: C:\ProgramData\Cirrus Logic\SCS_1.7\scripts
  - Mac script location: /Users/Shared/Cirrus Logic/SCS_1.7/scripts

# 4 Hardware Mode Control

The Dunglass system supports the hardware control modes for Cirrus Logic high performance ADC, DAC and Codec devices. These are supported via the rotary switches on the Dunglass system.

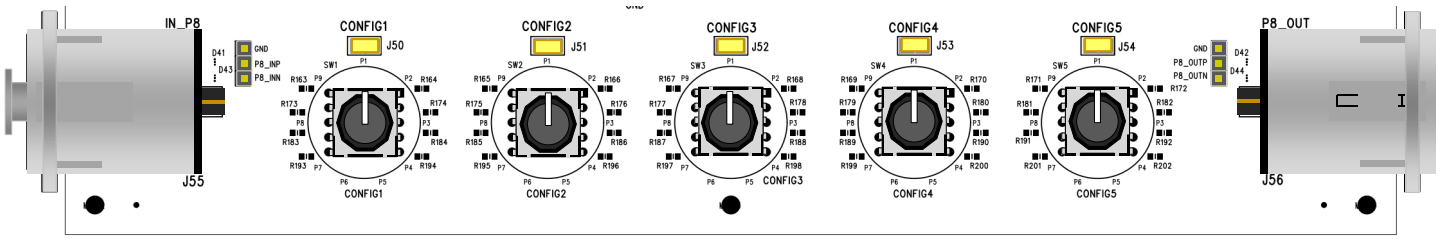



**Figure 13: Dunglass Rotary Switches for Hardware Control Mode**

Each switch has silkscreen on the board to indicate the position of the switch. Each switch position enables a pull resistor on the respective CONFIG pin to VDD_A or ground.

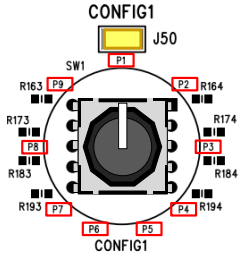



**Figure 14: Rotary Switch**

## 4.1 Hardware Mode Rotary Switch Settings

The rotary switch functions are described in the following tables. Refer to the CS5304P datasheet for further details of the hardware-mode control options.

The CONFIG1 pin selects the ASP operating configuration.

**Table 2: CONFIG1 Hardware Control – ASP Configuration**

| Switch Position | Config Pin Configuration | | Description |
|---|---|---|---|
| P1 | Pull-up to VDD_A | 0 Ω | Software control mode (I2C/SPI) |
| P2 | | 4.7 kΩ | ASP Primary Mode, 44.1 kHz, 48 kHz sample rate |
| P3 | | 22 kΩ | ASP Primary Mode, 88.2 kHz, 96 kHz sample rate |
| P4 | | 100 kΩ | ASP Primary Mode, 176.4 kHz, 192 kHz sample rate |
| P5 | Pull-Down to GND | 100 kΩ | ASP Secondary Mode, 176.4 kHz, 192 kHz sample rate |
| P6 | | 22 kΩ | ASP Secondary Mode, 88.2 kHz, 96 kHz sample rate |
| P7 | | 4.7 kΩ | ASP Secondary Mode, 44.1 kHz, 48 kHz sample rate |
| P8 | | 0 Ω | ASP Secondary Mode, autodetect sample rate |
| P9 | No Connection | | |

1. Autodetect sample rate is only supported in MCLK 256 fsb or MCLK 512 fsb clocking configurations.

The CONFIG2 pin selects the ASP format and TDM timeslots option.

**Table 3: CONFIG2 Hardware Control – ASP Configuration**

| Switch Position | Config Pin Configuration | | Description |
|---|---|---|---|
| P1 | Pull-up to VDD_A | 0 Ω | ASP TDM Mode—minimum time slots |
| P2 | | 4.7 kΩ | ASP TDM Mode—maximum time slots,<br>data output on BCLK falling edge (half-cycle mode) |
| P3 | | 22 kΩ | ASP TDM Mode—maximum time slots,<br>data output on BCLK rising edge (full-cycle mode) |
| P4 | | 100 kΩ | |
| P5 | Pull-Down to GND | 100 kΩ | |
| P6 | | 22 kΩ | |
| P7 | | 4.7 kΩ | ASP Left-Justified Mode |
| P8 | | 0 Ω | ASP $I^2S$ Mode |
| P9 | No Connection | | |

The CONFIG3 pin selects the TDM slot selection in TDM Mode.

**Table 4: CONFIG3 Hardware Control – TDM Slot Selection**

| Switch Position | Config Pin Configuration | | Description |
|---|---|---|---|
| P1 | Pull-up to VDD_A | 0 Ω | Slots 12–15 |
| P2 | | 4.7 kΩ | |
| P3 | | 22 kΩ | Slots 8-11 |
| P4 | | 100 kΩ | |
| P5 | Pull-Down to GND | 100 kΩ | Slots 4–7 |
| P6 | | 22 kΩ | |
| P7 | | 4.7 kΩ | Slots 0-3 |
| P8 | | 0 Ω | |
| P9 | No Connection | | |

The CONFIG4 pin selects the clock reference and ASP channel ordering.

**Table 5: CONFIG4 Hardware Control – Clocking Configuration**

| Switch Position | Config Pin Configuration | | Clock Reference | PLL | Channel Order |
|---|---|---|---|---|---|
| P1 | Pull-up to VDD_A | 0 Ω | BCLK = 64 fs | Enabled | Default |
| P2 | | 4.7 kΩ | MCLK = 512 fsb | Bypass | Default |
| P3 | | 22 kΩ | MCLK = 256 fsb | Enabled | Default |
| P4 | | 100 kΩ | MCLK = 512 fsb | Enabled | Default |
| P5 | Pull-Down to GND | 100 kΩ | MCLK = 512 fsb | Enabled | Reversed |
| P6 | | 22 kΩ | MCLK = 256 fsb | Enabled | Reversed |
| P7 | | 4.7 kΩ | MCLK = 512 fsb | Enabled | Reversed |
| P8 | | 0 Ω | BCLK = 64 fs | Bypass | Reversed |
| P9 | No Connection | | | | |

1. fsb is the base sample rate. fsb = 48 kHz for 48 kHz-related sample rates; fsb = 44.1 kHz for 44.1 kHz-related sample rates.
2. BCLK 64 fs configuration is only supported in ASP Secondary Mode.

The CONFIG5 pin selects the digital filter.

**Table 6: CONFIG5 Hardware Control – Digital Filter Selection**

| Switch Position | Config Pin Configuration | | Description |
|---|---|---|---|
| P1 | Pull-up to VDD_A | 0 Ω | Minimum phase, slow roll-off, HPF bypass |
| P2 | | 4.7 kΩ | Minimum phase, fast roll-off, HPF bypass |
| P3 | | 22 kΩ | Linear phase, slow roll-off, HPF bypass |
| P4 | | 100 kΩ | Linear phase, fast roll-off, HPF bypass |
| P5 | Pull-Down to GND | 100 kΩ | Linear phase, fast roll-off, HPF enabled |
| P6 | | 22 kΩ | Linear phase, slow roll-off, HPF enabled |
| P7 | | 4.7 kΩ | Minimum phase, fast roll-off, HPF enabled |
| P8 | | 0 Ω | Minimum phase, slow roll-off, HPF enabled |
| P9 | No Connection | | |

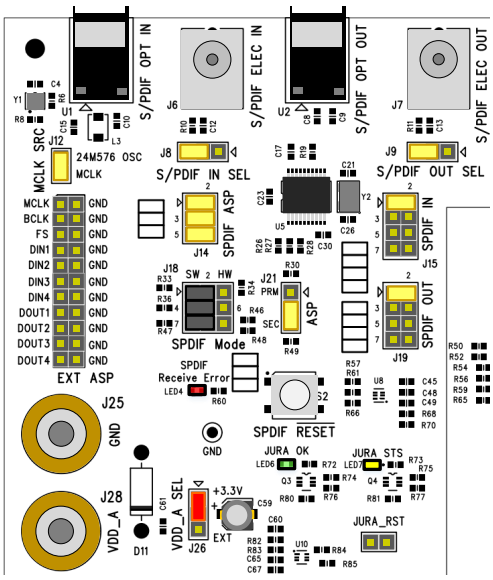
# 5 SPDIF Out

The DC5304P-ADC daughtercard supports S/PDIF output via optical and electrical connectors in software mode for sample rates up to 96 kHz (optical) or up to 192 kHz (electrical). The Dunglass system supports S/PDIF output at 48 kHz, 96 kHz, and 192 kHz sample rates.

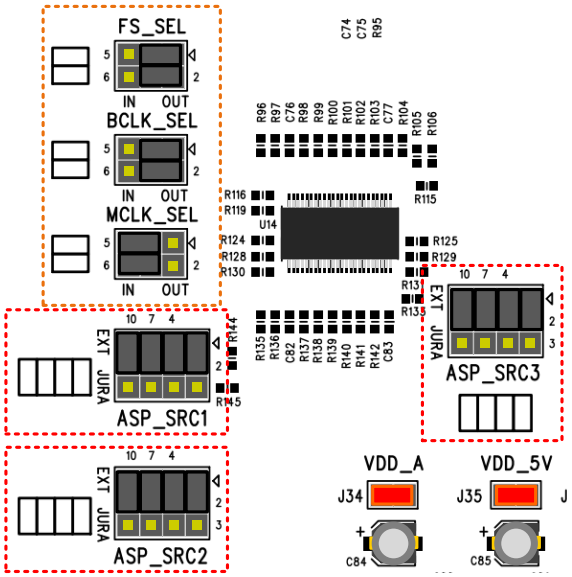
## 5.1 Dunglass Jumper Config for DC5304P-ADC

When using the S/PDIF transceiver on the Dunglass system, the jumper links must be configured as in Table 7. The WM8804 S/PDIF transceiver operates in software mode. Configuration scripts are provided as part of the DC5304P-ADC daughter card SoundClear Studio package.

**Table 7 SPDIF Jumper Link Configuration for DC5304P-ADC**




**S/PDIF Jumper Link Configuration**




**S/PDIF Digital Audio Signal Routing**

The SPDIF Receive Error (LED4) is lit when there is no S/PDIF input source present.

## 5.2 Digital Audio Signal Routing to S/PDIF Transceiver

The signal source for the S/PDIF output transmitter is configured using the SPDIF OUT header; the source can be selected from any of the ASP_DOUTn pins from the ADC device.

Note that the S/PDIF output is compatible with ASP I2S and Left-Justified Modes only. The ASP_DOUTn pins support Channels 1–2 and 3–4 respectively.

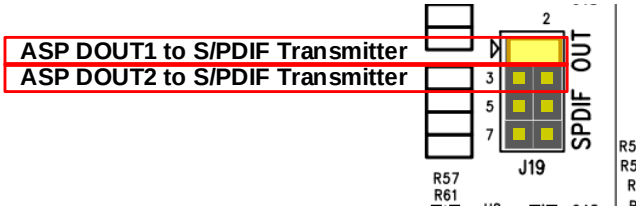


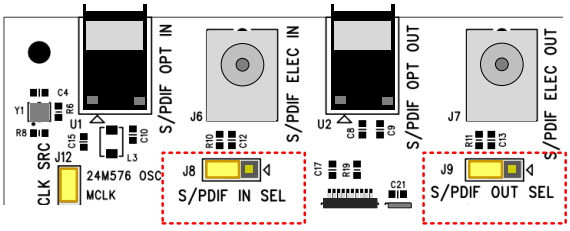

**Figure 15: SPDIF IN and SPDIF out Jumper Link Configuration**

## 5.3 Selecting Optical or Electrical S/PDIF

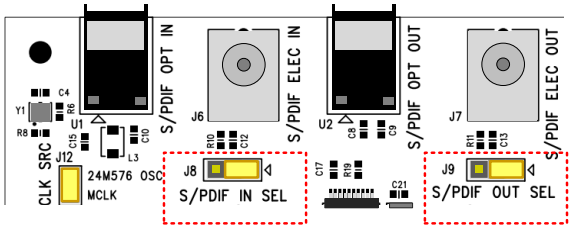
The S/PDIF IN SEL and S/PDIF OUT SEL headers configure the S/PDIF input and output paths in optical or electrical modes. The headers are configured as shown in Table 8.

The Dunglass system supports S/PDIF input/output at sample rates up to 96 kHz (optical) or up to 192 kHz (electrical).

**Table 8 SPDIF I/O Configuration**




**Optical Input & Output**




**Electrical Input & Output**

# 6 Notices

Jura firmware development utilizes components under the following licenses:

1. XMOS PUBLIC LICENCE: Version 1, available at www.xmos.ai/license-agreements/
2. The MIT License, available at www.github.com/microsoft/uf2/blob/master/LICENSE.txt. Copyright © Microsoft Corporation

Unmodified USB Audio 2.0 Device Software source code is available from www.xmos.ai under XMOS PUBLIC LICENCE: Version 1.

# 7 Revision History

**Revision History**

| Revision | Changes |
|---|---|
| R1<br>Sept 2023 | • Initial version. |

**Contacting Cirrus Logic Support**

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.