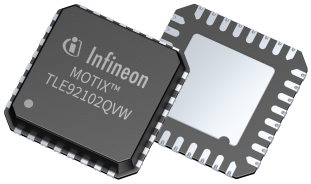
Technical documents

MOTIX™ TLE92102 multi MOSFET gate driver IC for BDC motors with current sense amplifier

Features



AEC Qualified

RoHS

ISO 26262 compliant

- H-bridge driver for switching four N-channel FETs with a Q_{Gtot} of 85 nC at a 20 kHz PWM
- 8 V to 29 V functional supply voltage range for 12 V battery supply systems
- Extended functional supply voltage down to 4.5 V with four N-channel FETs with a QGtot of 55 nC at a 20 kHz PWM
- Programmable current controlled output stages
- 0…100% duty cycle supported without restrictions
- High robustness of motor connection pins of -6 V to 40 V
- Current sense amplifier for low side shunt current measurement with high accuracy of 0.8% and fast settle time 1 µs
- Serial peripheral interface (SPI) providing extended monitoring and diagnostic functions
- SPI configurable failure reaction
- SPI window watchdog for microcontroller supervision
- Passive clamping of external FETs
- Low quiescent current mode
- Small VQFN 32 pin 5x5 mm supporting automated optical inspection capability (AOI)
- Green product (RoHS-compliant)
- AEC-Q100, Grade 0 qualified
- Developed according to ISO 26262 ed. 2018 ASIL-B

Potential applications

- 12 V seat control and extended functions (steering column adjustment, gas pedal adjustment)
- 12 V power lift gate
- 12 V central door lock
- 12 V body control module (cargo cover, washer pump, window lift, rear wiper ...)

Product validation

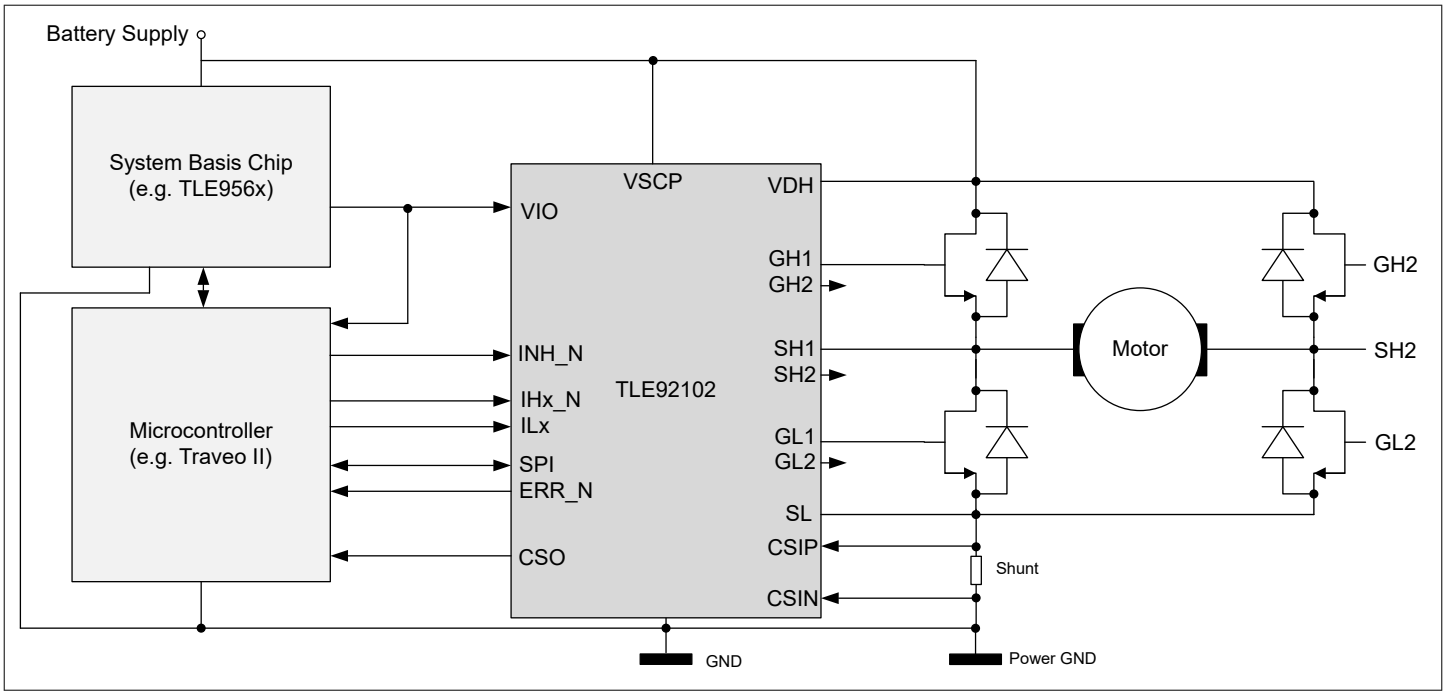
Product validation according to AEC-Q100, Grade 0. Qualified for automotive applications

Description

The TLE92102 is an advanced gate driver IC dedicated to control up to four N-channel MOSFETs. It includes two half-bridges for DC motor control applications such as automotive power seat control or other applications.

An integrated SPI interface is used to configure the TLE92102 for the application after power-up. After successful power-up, parameters can be adjusted by SPI, monitoring data, configuration and error registers can be read out. Cyclic redundancy check over data and address bits ensures safe communication and data integrity. GND related inverter bridge current can be measured with an integrated current sense amplifier.

The TLE92102 offers a wide range of diagnostic features, like monitoring of power supply voltages as well as system parameter monitoring. Failure behavior, threshold voltages and filter times of the supervisions of the device are adjustable via SPI. The TLE92102 is especially designed for safety relevant motor drive applications and was developed according to ISO 26262 ed. 2018 ASIL-B. Safety documentation, such as safety manual is provided. An optimized monitoring and diagnostic concept, including self-test functions ensures high flexibility on fault reactions and low FIT rates for the relevant failure modes. The VQFN32 package with an exposed pad for an optimized thermal performance and provides special leads allowing an automated optical inspection.



Product type	Package	Marking
TLE92102	VQFN-32	TLE92102QVW

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1 Functional block diagram

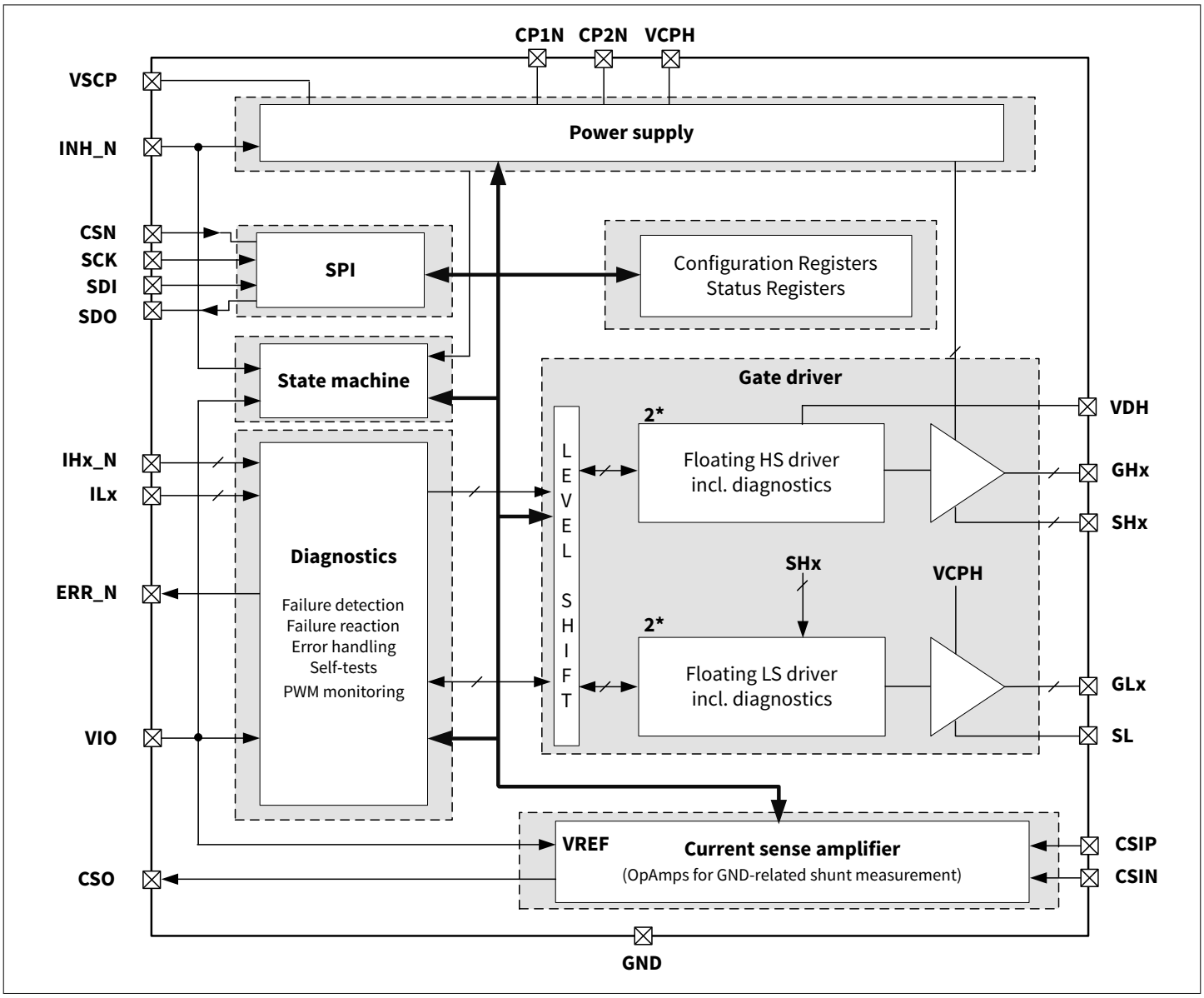

Figure 1 Block diagram

2 Pin configuration

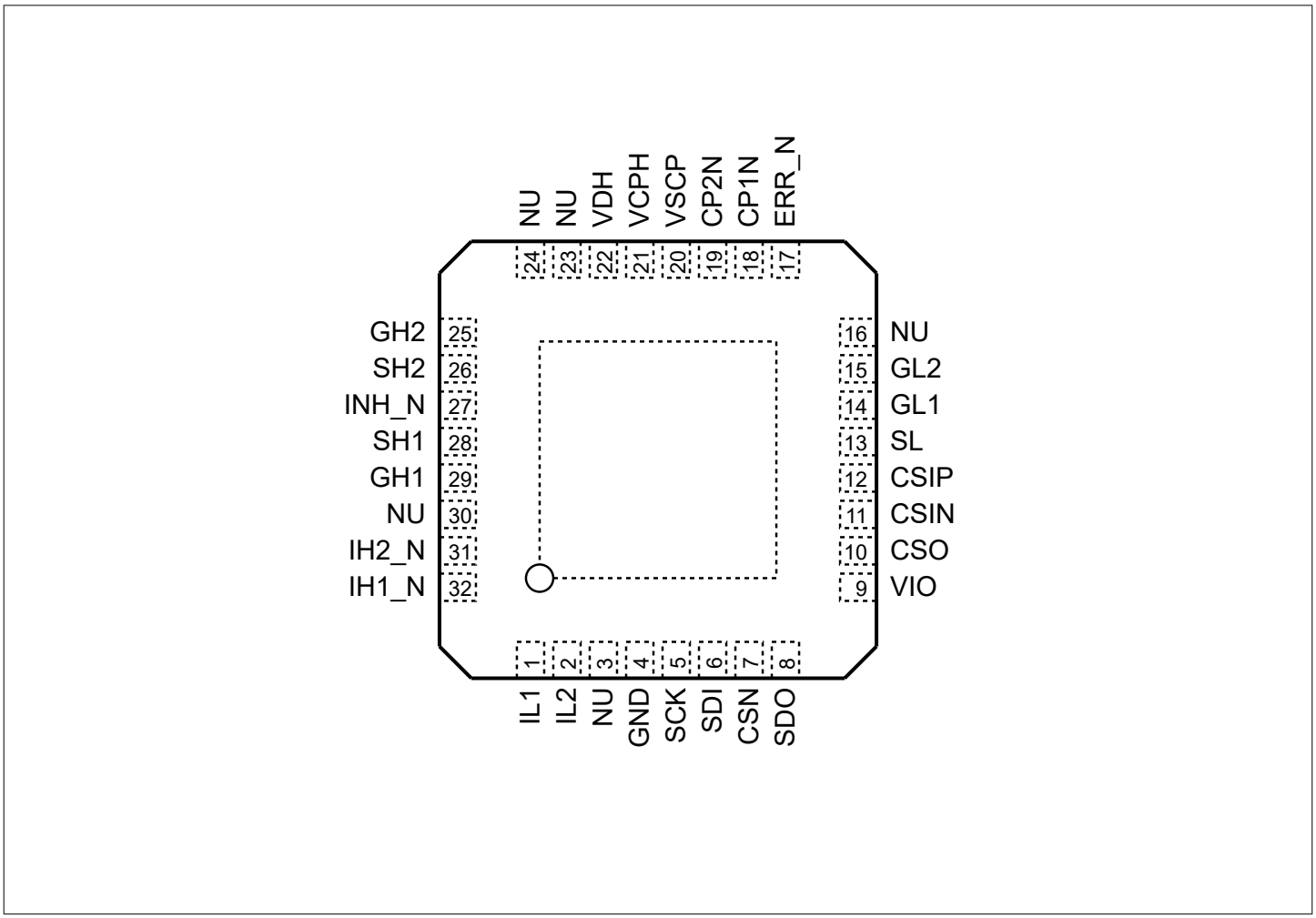

Figure 2 Pin assignment VQFN-32

Table 1 Pin definitions and function

Pin number	Symbol	Function	I/O
1	IL1	**Input low-side 1** Digital active-high input pin to turn on/off low-side FET 1 referred to VIO supply voltage	Digital input
2	IL2	**Input low-side 2** Digital active-high input pin to turn on/off low-side FET 2 referred to VIO supply voltage	Digital input
3	NU	**Not used** Leave open all NU pins - do not connect to any potential	No function
4	GND	**Ground pin** Connect this pin directly (low ohmic and low inductive) to GND	Ground

(table continues...)

Table 1 (continued) Pin definitions and function

Pin number	Symbol	Function	I/O
5	SCK	**Serial clock peripheral interface** Digital SPI signaling input port referred to VIO supply voltage. Connect to SPI port “clock” of microcontroller	Digital input
6	SDI	**Serial data in** Digital SPI signaling input port referred to VIO supply voltage. Connect to SPI port “data output” of microcontroller	Digital input
7	CSN	**Chip select not** Digital active-low SPI signaling input port referred to VIO supply voltage. Connect to SPI port “chip select” of microcontroller	Digital input
8	SDO	**Serial data out** Digital SPI signaling output port referred to VIO supply voltage. Connect to SPI port “data input” of microcontroller	Digital output
9	VIO	**Supply for digital core, digital I/O pins and current sense amplifier** Connect the input capacitor as close as possible to pin	Local supply
10	CSO	**Current sense output** Analog output of current sense amplifier for shunt signal amplification referred to VIO	Analog output
11	CSIN	**Current sense input negative** Input for motor current measurement	Analog input
12	CSIP	**Current sense input positive** Input for motor current measurement	Analog input
13	SL	**Source low-side** Analog I/O pin to turn on/off low-side FET 1 and 2. Connect to the source of low-side FETs 1 and 2. If transients violate maximum rating or functional range external protection circuit is required	Power I/O
14	GL1	**Gate low-side 1** Analog I/O pin to turn on/off low-side FET 1. Connect to the gate of low-side FET 1	Analog output
15	GL2	**Gate low-side 2** Analog I/O pin to turn on/off low-side FET 2. Connect to the gate of low-side FET 2.	Analog output
16	NU	**Not used** Leave open all NU pins - do not connect to any potential	No function
17	ERR_N	**Digital active-low open drain error output pin** Indication for detected errors. If not used keep pin open	Digital output
18	CP1N	**Charge pump stage 1 driver output** Connect the pump capacitor as close as possible to pin	Supply

(table continues...)

Table 1 (continued) Pin definitions and function

Pin number	Symbol	Function	I/O
19	CP2N	**Charge pump stage 2 driver output** Connect the pump capacitor as close as possible to pin	Supply
20	VSCP	**Voltage supply** Supply input for high voltage charge pump. Connect low ohmic and low inductive to recommended common star point of the high-side FETs drains and buffer capacitors	Local supply
21	VCPH	**Charge pump output voltage** Buffer capacitor connection for charge pump output. Connect the capacitor as close as possible to pin	Supply
22	VDH	**Voltage drain high-side** Sense input for short circuit detection (SCD) of all high-side FETs. Connect this pin to recommended common star point of the drains of the high-side FETs and buffer capacitor. External filter recommended	Analog input
23	NU	**Not used** Leave open all NU pins - do not connect to any potential	No function
24	NU	**Not used** Leave open all NU pins - do not connect to any potential	No function
25	GH2	**Gate high-side 2** Analog I/O pin to turn on/off high-side FET 2. Connect to the gate of high-side FET 2	Analog output
26	SH2	**Source high-side 2** Analog output pin to turn on/off high-side FET 2. If transients violate maximum rating or functional range, external protection circuit is required	Power I/O
27	INH_N	**Inhibit not** Analog active-low inhibit pin. Sets device into sleep mode for low quiescent current consumption. External FETs are turned off actively before the charge pumps are turned off. Reset via inhibit requires a new configuration via SPI	Digital input
28	SH1	**Source high-side 1** Analog I/O pin to turn on/off high-side FET 1. If transients violate maximum rating or functional range, external protection circuit is required	Power I/O
29	GH1	**Gate high-side 1** Analog output pin to turn on/off high-side FET 1. Connect to the gate of high-side FET 1	Analog output
30	NU	**Not used** Leave open all NU pins - do not connect to any potential	No function
31	IH2_N	**Input high-side 2 NOT** Digital active-low input pin to turn on/off high-side FET 2 referred to VIO supply voltage	Digital input

(table continues...)

Table 1 (continued) Pin definitions and function

Pin number	Symbol	Function	I/O
32	IH1_N	**Input high-side 1 NOT** Digital active-low input pin to turn on/off high-side FET 1 referred to VIO supply voltage	Digital input
Exposed pad	E-pad	**Cooling tab** Connect to GND	Floating

3 General product characteristics

3.1 Absolute maximum ratings

T_J = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Table 2 Electrical characteristics - absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply							
Voltage range VSCP	V_{VSCP_MR}	-0.3	–	40	V	Load dump condition maximum 400 ms at 40 V	P_GEN_01_01
Negative current capability range VSCP	$I_{VSCP\_OL\_MR}$	-700	–	–	mA	t < 8 ms	P_GEN_01_02
Voltage range VSCP transients	$V_{VSCP\_SP\_MR}$	-0.3	–	48	V	t < 500 ns	P_GEN_01_03
Slew rate VSCP	SR_{VSCP}	-10	–	10	V/µs	Applied before R_{VSCP}	P_GEN_01_04
Voltage range VIO	V_{VIO_MR}	-0.3	–	5.75	V	–	P_GEN_01_05
Voltage range CPxN	V_{CPxN_MR}	-0.3	–	V_{VSCP} + 0.3	V	–	P_GEN_01_06
Voltage range VCPH	V_{VCPH_MR}	VSCP - 0.3	–	51	V	–	P_GEN_01_07
Voltage range VCPH	V_{VCPH_MR}	VSCP - 0.3	–	40	V	VSCP pin open	P_GEN_01_08
Digital input and output pins							
Voltage range digital input pins	V_{DI_MR}	-0.3	–	5.75	V	Digital input pins: IHx_N, ILx, SDI, SCK, CSN	P_GEN_02_01
Voltage range ERR_N pin	V_{ERR_MR}	-0.3	–	40	V	Digital output pins: ERR_N	P_GEN_02_03
Voltage range INH_N pin	V_{INH_MR}	-6.5	–	40	V	–	P_GEN_02_04
Voltage range digital output pin: SDO	V_{SDO_MR}	-0.3	–	5.75	V	Digital output pin SDO	P_GEN_02_05
Current sense amplifier							
Voltage range CSIN	V_{CSIN_MR}	-6.5	–	6.5	V	–	P_GEN_03_01
Voltage range CSIP	V_{CSIP_MR}	-6.5	–	6.5	V	–	P_GEN_03_02
Voltage range CSIP - CSIN	$V_{CSIP\_CSIN\_MR\_diff}$	-6.5	–	6.5	V	–	P_GEN_03_03

(table continues...)

Table 2 (continued) Electrical characteristics - absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Voltage range CSO	V_{CSO_MR}	-0.3	–	5.75	V	–	P_GEN_03_04
Inverter stage							
Voltage range SHx	V_{SHx_MR}	-6.5	–	40	V	–	P_GEN_04_01
Voltage range GHx	V_{GHx_MR}	V_{SHx} - 0.3	–	MIN(48, V_{SHx} + 14)	V	–	P_GEN_04_02
Voltage range GHx	V_{GHx_MR}	V_{SHx} - 0.3	–	MIN(40; V_{SHx} + 14)	V	VSCP pin open OR device in sleep mode or safe state	P_GEN_04_12
Voltage range SL	V_{SL_MR}	-6.5	–	40	V	–	P_GEN_04_05
Voltage range GLx	V_{GLx_MR}	V_{SL} - 0.3	–	MIN(40, V_{SL} + 14)	V	–	P_GEN_04_06
Slew rate Sxx	SR_{Sxx_MR}	-1	–	1	V/ns	Amplitude 18 V	P_GEN_04_09
Voltage range VDH	V_{VDH_MR}	-0.3	–	51	V	100 Ω > R_{VDH} > 35 Ω t < 400ms for V_{VDH} > 40V	P_GEN_04_10
Voltage range VDH	V_{VDH_MR}	-0.3	–	40	V	VSCP pin open	P_GEN_04_13
Negative current capability range VDH	$I_{VDH\_OL\_MR}$	-100	–	–	mA	t < 8 ms	P_GEN_04_14
Temperatures							
Storage temperature	T_{stg}	-55	–	175	°C	–	P_GEN_05_01
Junction temperature	T_{J_MR}	-40	–	175	°C	–	P_GEN_05_02
ESD susceptibility							
ESD resistivity HBM all pins	V_{ESD_HBM}	-2	–	2	kV	1)	P_GEN_06_01
ESD resistivity CDM all pins	V_{ESD_CDM}	-500	–	500	V	2)	P_GEN_06_02
ESD resistivity CDM corner pins	$V_{ESD\_CDM\_CR}$	-750	–	750	V	2)	P_GEN_06_03

1) *Human body model (HBM) robustness according to AEC - Q100-002*
2) *Charged device model (CDM) robustness according to AEC - Q100-011; voltage level refers to test condition (TC) mentioned in the standard*

***Note**: Latchup robustness: class II according to AEC-Q100-04*

***Notes**:*

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

The following functional range shall not be exceeded in order to ensure correct operation of the device. All parameters specified in the following sections refer to these operating conditions unless otherwise indicated.

T_J = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Table 3 Electrical characteristics - functional range

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply							
Functional voltage range VSCP	$V_{VSCP\_FR\_DC}$	8.0	–	29	V	–	P_GEN_07_01
Extended voltage range VSCP	V_{VSCP_EXT}	29	–	35	V	Allowed for t_{max} < 400 ms Parameter deviations may apply	P_GEN_07_02
Extended voltage range VSCP	V_{VSCP_EXT}	7	–	8	V	Two-Stage Charge Pump configuration. Parameter deviations may apply	P_GEN_07_03
Extended voltage range VSCP	V_{VSCP_EXT}	4.5	–	8	V	Three-Stage Charge Pump configuration. Parameter deviations may apply	P_GEN_07_04
Voltage range VIO	V_{VIO_FR}	3.0	–	5.5	V	–	P_GEN_07_05
Digital input and output pins							
Voltage range input pins	V_{DI_FR}	-0.3	–	5.5	V	Pins SDI, CSN, SCK, INH_N, ILx, IHx_N	P_GEN_08_01
Voltage range output pins	V_{DO_FR}	-0.3	–	5.5	V	Pins ERR_N, SDO	P_GEN_08_02
Temperatures							
Nominal operating junction temperature range	$T_{J\_FR\_nom}$	-40	–	175	°C	Specified temperature range	P_GEN_10_01
Limited extended operating junction temperature range	$T_{J\_FR\_lim}$	175	–	195	°C	1)	P_GEN_10_02

1) t < 1 h over life time. Overtemperature detection works as specified; all other blocks might violate the specified electrical characteristics parameter, the functionality of all other blocks is still available until overtemperature detection.

***Note**: Within the functional or operating range, the IC operates as described in the circuit description, all blocks are functional without a fault detection (for example, PWM pattern is applied at FETs). The electrical characteristics are specified within the conditions given in Chapter 3.1.*

3.3 Thermal resistance

Table 4 Electrical characteristics - thermal resistance

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VQFN-32 package							
Junction to case	R_{THJC1}	–	5	10	K/W	–	P_GEN_11_01
Junction to top	Ψ_{thJT}	–	5	10	K/W	–	P_GEN_11_02
Junction to ambient	R_{THJA1}	–	25	35	K/W	1)	P_GEN_11_03

1) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer

3.4 Current consumption

T_J = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Table 5 Electrical characteristics - current consumption

The electrical characteristics are specified within the conditions given in Chapter 3.4.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Quiescent current VSCP	I_{qVSCP}	–	–	2	µA	$T_J \le 85°C$; $V_{VSCP} \le 14.0$ V; Device in sleep mode; V_{INH_N} = GND	P_GEN_12_01
Quiescent current VSCP	I_{qVSCP}	–	–	8	µA	$T_J \le 150°C$; $V_{VSCP} \le 14.0$ V; Device in sleep mode; V_{INH_N} = GND	P_GEN_12_02
Quiescent current VDH	I_{qVDH}	–	–	1	µA	Device in sleep mode	P_GEN_12_03

(table continues...)

Table 5 (continued) Electrical characteristics - current consumption

The electrical characteristics are specified within the conditions given in Chapter 3.4.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Quiescent current VIO	I_{qVIO}	–	–	4	µA	Device in sleep mode V_{VIO} < 5.5 V T_J < 85°C	P_GEN_12_04
CSA current	I_{CSA}	–	4	7	mA	Static condition; I_{CSA} current consumption applicable to VIO pin	P_GEN_12_05
Mean supply current VIO	I_{VIO_NOM}	–	8	14	mA	V_{IO} within V_{IO_FR}; INH_N = "high"; Normal operation mode, power-up mode; Static condition	P_GEN_12_06
Mean supply current VDH	I_{VDH_NOM}	–	120	180	µA	Current applicable on VDH pin per enabled half-bridge	P_GEN_12_07
Mean supply current VSCP - no FET operation	$I_{VSCP\_NOM\_DIS}$	–	3	5	mA	INH_N = "high"; Normal operation mode, power-up mode; CSA disabled, charge pump enabled, all half-bridges disabled	P_GEN_12_08
Mean supply current VSCP - no FET operation, active half-bridges	$I_{VSCP\_NOM\_EN}$	–	30	40	mA	7 V < V_{VSCP} < 16 V; INH_N = "high"; Normal operation mode, power-up mode; CSA disabled, charge pump enabled, all half-bridges enabled	P_GEN_12_09
Mean supply current VSCP - FET operation	$I_{VSCP(ON)}$	–	–	60	mA	Bridge driver fully operating I_{VCPH} = - 9 mA V_{VSCP} = 13.5 V	P_GEN_12_10
Mean supply current VSCP - FET operation	$I_{VSCP(ON)}$	–	–	80	mA	Bridge driver fully operating I_{VCPH} = - 4.8 mA V_{VSCP} = 4.5 V	P_GEN_12_11

4 State machine

4.1 Functional description (state machine)

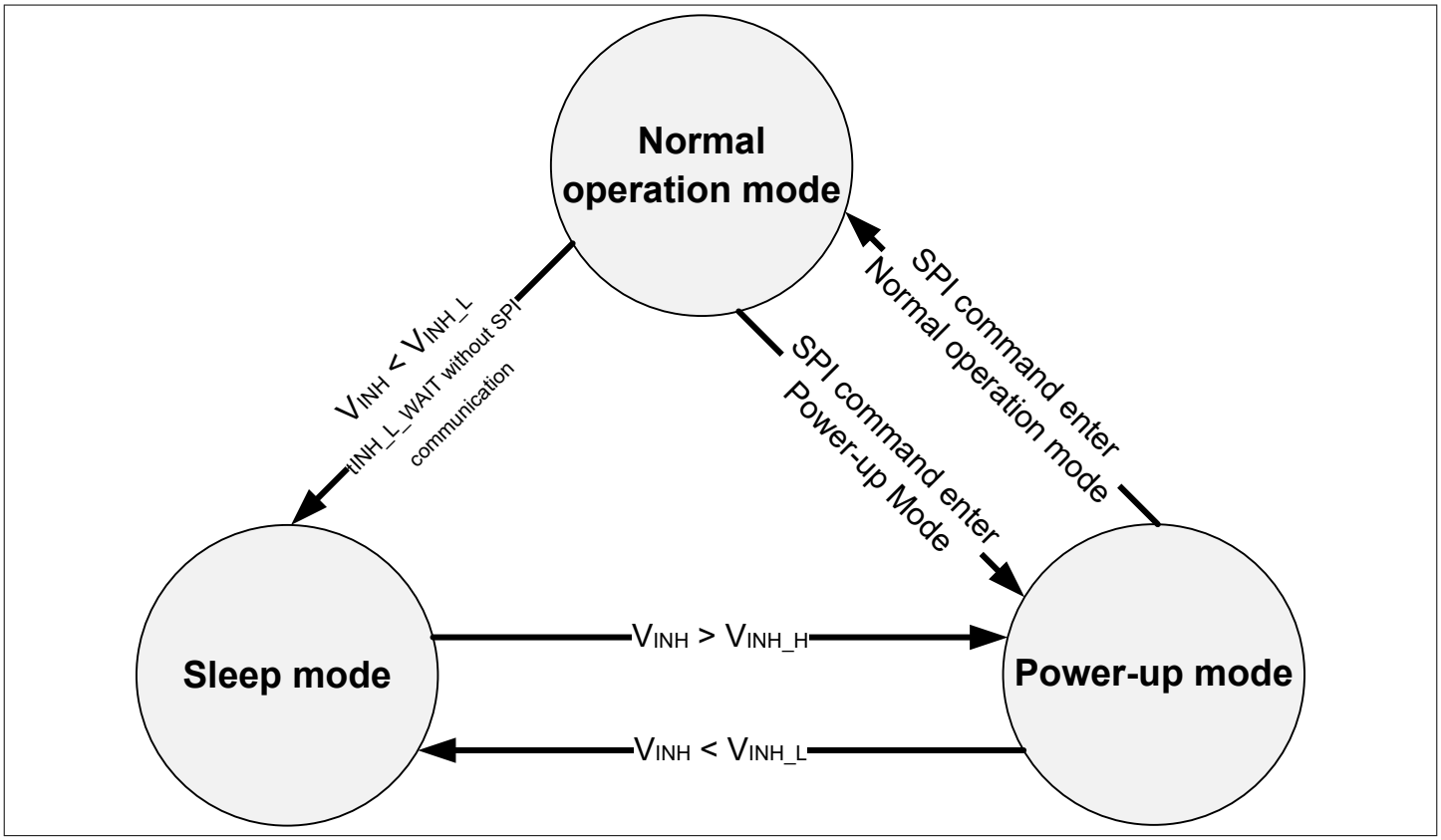

Figure 3 State diagram

Figure 3 is valid for V_{VSCP} and V_{VIO} within functional range.

- In case V_{VIO} drops below $V_{VIO} < V_{VIO\_FR}$ the digital input and output pins are deactivated and power-on reset is triggered
- The digital logic of the device is supplied by V_{VIO}
- The output stages Gxx are supplied by pin VSCP. If $V_{VSCP} < V_{VSCP\_UV\_SD}$, then the output stages are deactivated. ERR_N pin is set to "low"

4.1.1 Sleep mode

In Sleep mode the device has following characteristics:

- All internal functions are deactivated
- Safe state entered: floating FET driver OFF (passive clamping active, Gxx-GND passive discharge enabled)
- ERR_N pin not actively driven

A mode change from normal-operation mode OR power-up mode to sleep mode is triggered by a INH_N low level detection $V_{INH} < V_{INH\_L}$ for $t > t_{INH\_filter}$ AND without SPI communication during $t_{INH\_L\_WAIT}$. After $t_{INH\_L\_WAIT}$ expiration, sleep mode is entered after t_{SMA}.

In case INH_N pin is set low for $t > t_{INH\_filter}$ as long as $t_{INH\_L\_WAIT}$ has not expired:

- SPI communication is available
- ERR_N pin actively pulled "low"
- Gxx output stages are kept OFF

4.1.1.1 INH_N pin function

The INH_N pin function is supplied by VIO supply pin and is functional in case $V_{VIO} > V_{VIO\_POR}$. The INH_N pin function sets the device into safe state from any operation mode.

In case INH_N is set to "low" for t > t_{INH_filter}, then after t_{SOFF_APD} has expired, the driver output stages are turned off and kept off with Gxx-Sxx passive clamping and Gxx-GND passive discharge enabled.

When the device is in normal-operation mode or power-up mode and INH_N pin is set to "low" for t > t_{INH_filter} then the power down sequence is initiated after $t_{INH\_L\_WAIT}$ expiration in case:

- no SPI command has been received during $t_{INH\_L\_WAIT}$
- AND no INH_N high level detected during $t_{INH\_L\_WAIT}$

In case INH_N pin is detected "high" during $t_{INH\_L\_WAIT}$, the power down sequence is canceled. After the canceled power down sequence the device stays in currently selected mode of operation.

In case a valid SPI communication is detected by the device during $t_{INH\_L\_WAIT}$, then two behavioral options are available and configurable by protected SPI control bit:

- Setting 1 (Default): the device remains in current mode of operation and safe state
- Setting 2: the device remains in current mode of operation and safe state while $t_{INH\_L\_WAIT}$ is restarted. If during $t_{INH\_L\_WAIT}$ no SPI communication is detected, the device will go to sleep mode

Any INH_N pin "low" detection of t > t_{INH_filter} is indicated towards the microcontroller via a SPI status bit and latched error 1 failure reaction is executed.

4.1.2 Power-up mode

The default device configuration at power-up is (after internal power on reset is released):
- Internal digital core active
- Watchdog function disabled
- Charge pump disabled
- Current sense amplifier disabled
- Monitoring and diagnostics functions active
- Gate drivers OFF (Gxx-Sxx passive clamping active and Gxx-GND passive discharge enabled)
- ERR_N active low

The device changes mode of operation from normal mode to power-up mode if one of the below actions is executed:

- SPI write command for mode change is sent
- SPI write command to trigger clear configuration (reset to default setting of non-protected registers)

The device changes mode of operation from sleep mode to power-up mode in case INH_N high level $V_{INH} > V_{INH\_H}$ is detected for $t > t_{INH\_filter}$.

During power-up mode:
- During start-up of the device once the digital core is supplied the ERR_N pin is actively pulled low
- SPI communication is accepted by the device after t_{core_up} has elapsed and VIO is within the functional range

4.1.3 Normal operation mode

In normal operation mode the following functions are available:
- Internal digital core active
- Charge pump active
- Gate drivers active
- Current sense amplifier active
- Watchdog function active
- Monitoring and diagnostics functions active

The device is set from power-up mode to normal operation mode in case a the mode change write SPI command is sent, provided that:

- $t_{core\text{-}up}$ elapsed
- At least one correct SPI SDI frame command was received by the device.
- VIO within the functional range

***Note**: It is recommended to configure properly the protected registers prior to normal-operation mode entry. It is required to configure VIO supply level before mode change request to normal operation mode.*

4.1.4 Power-up and power-down sequence

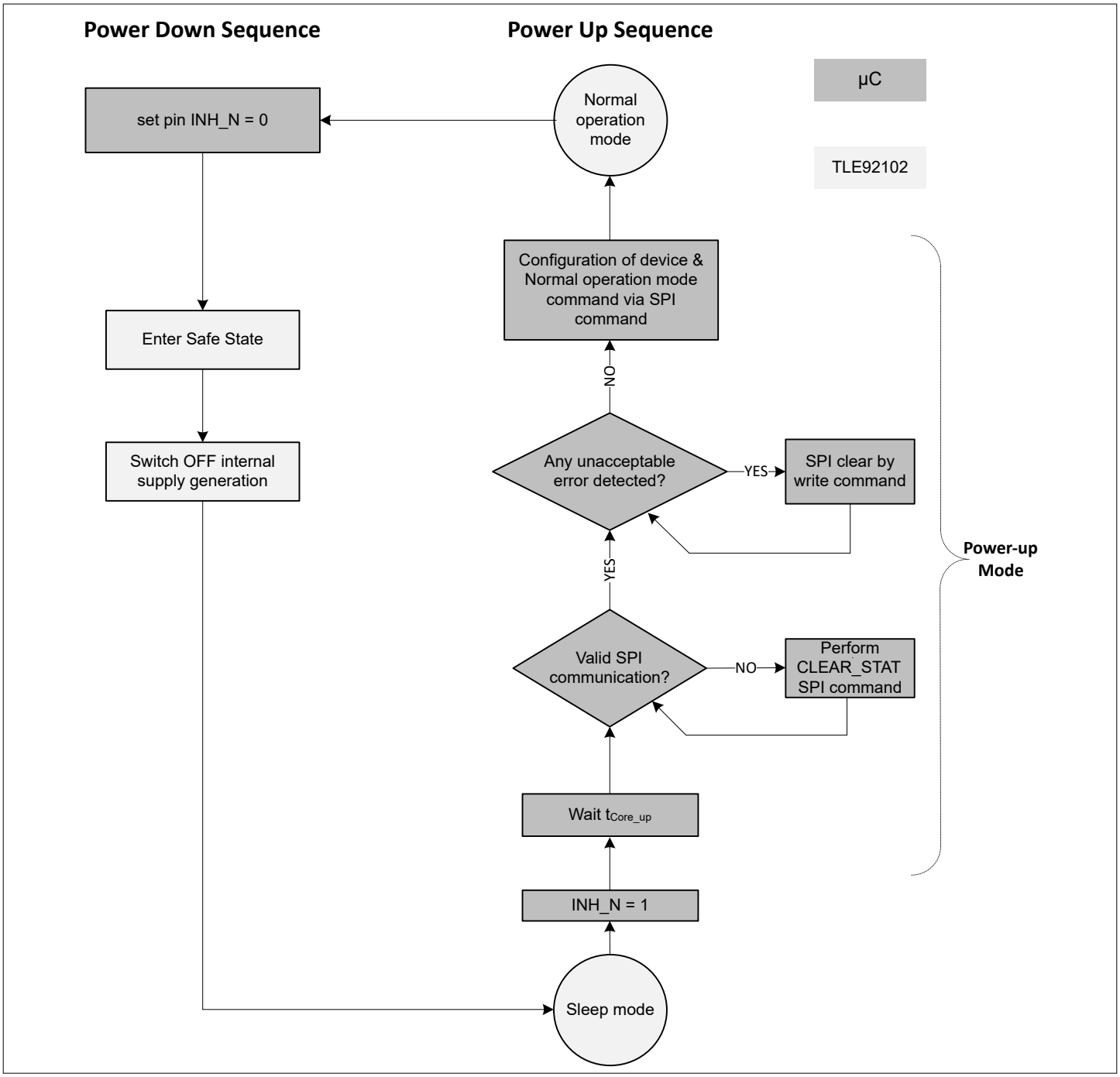

Figure 4 Simplified power-up & power-down diagram

4.2 Electrical characteristics (state machine)

Table 6 Electrical characteristics - state machine

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C; normal operating mode, power-up mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Digital core ready	t_{core_up}	–	0.5	1.0	ms	INH_N high level till SPI communication ready	P_STM_01_01
Sleep mode activation time	t_{SMA}	1	–	12	µs	After $t_{INH\_L\_WAIT}$ expired and no SPI communication	P_STM_01_02
INH_N filter time	t_{INH_filter}	1.0	–	4.0	µs	–	P_STM_01_03
INH_N "low" wait time	$t_{INH\_L\_WAIT}$	100	–	500	µs	–	P_STM_01_04
Low input voltage of INH_N	V_{INH_L}	–	–	0.3 x V_{VIO}	V	–	P_STM_01_05
High input voltage of INH_N	V_{INH_H}	0.7 x V_{VIO}	–	–	V	–	P_STM_01_06
Hysteresis of INH_N	V_{INHN_HY}	100	–	–	mV	–	P_STM_01_07
INH_N pull-down resistor	R_{PD_INHN}	20	40	60	kΩ	–	P_STM_01_08
INH_N pin input capacitance	C_{INHN}	–	–	20	pF	–	P_STM_01_09
Analog passive discharge filter time	t_{SOFF_APD}	2	10	14	µs	–	P_STM_01_10
VIO POR threshold	V_{VIO_POR}	2.3	2.5	2.9	V	–	P_STM_01_11

5 Supply

5.1 Functional description (power supply)

5.1.1 Charge pump supply

The device offers two different charge pump supply configurations, which can be selected by a control bit:

- Two-stage charge pump configuration
- Three-stage charge pump configuration

Depending on the configuration selected different charge pump modes are available see Chapter 5.1.1.1.

The charge pump's external required components depend on the selected configuration:

- Two-stage charge pump configuration: 3 external diodes and 3 external capacitors
- Three-stage charge pump configuration: 4 external diodes and 4 external capacitors.

For both use cases at VSCP pin a series resistor and buffer capacitor is needed.

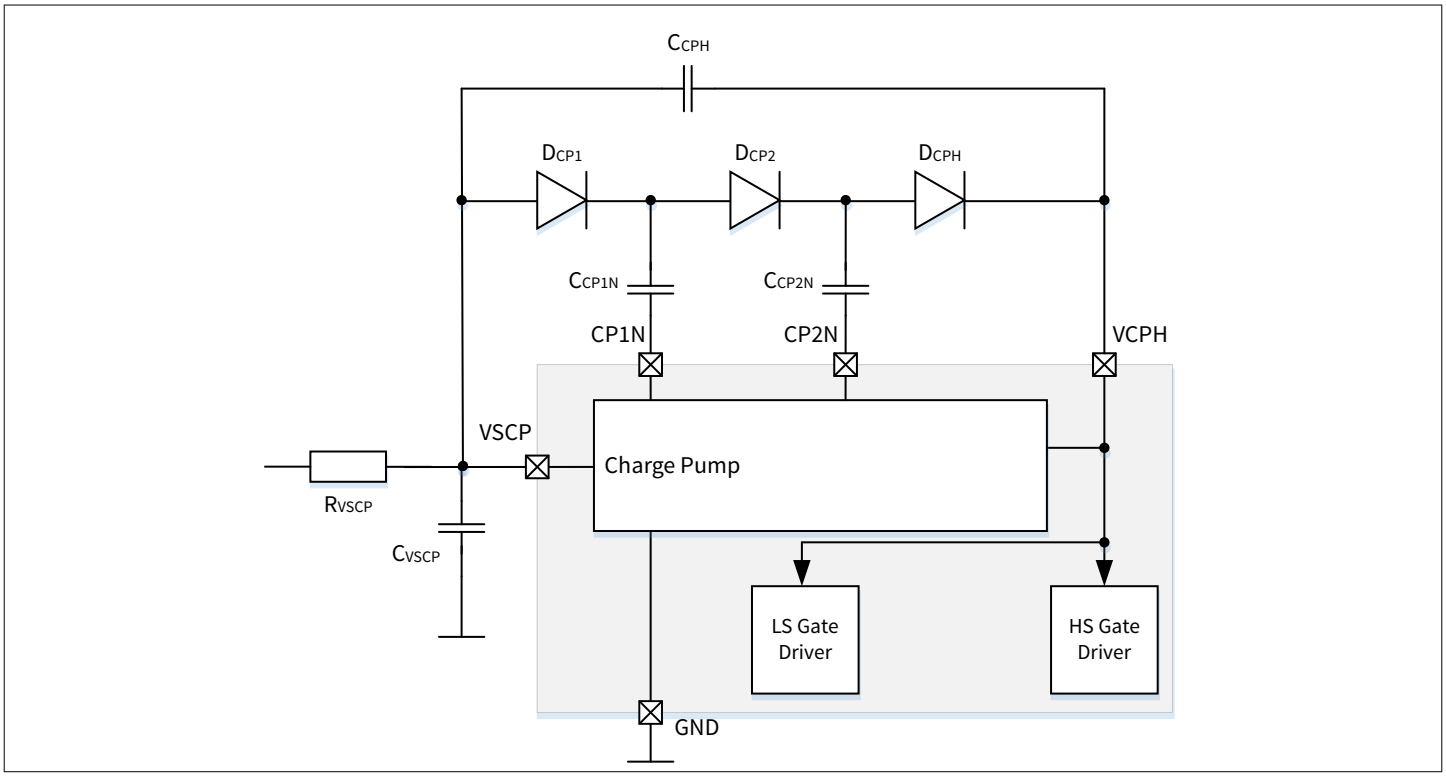

Figure 5 Simplified block diagram: Two-stage charge pump configuration

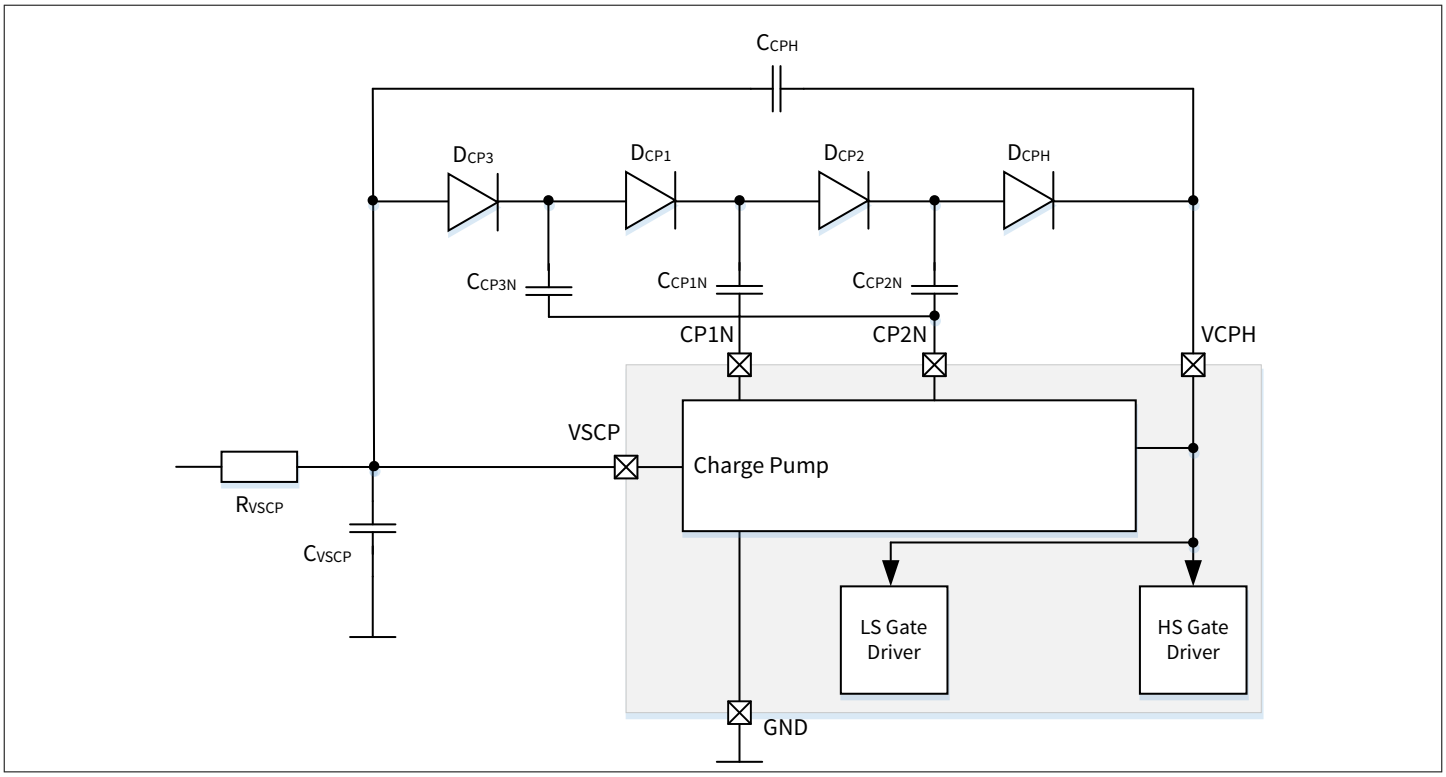

Figure 6 Simplified block diagram: Three-stage charge pump configuration

In case the driver has to work in low supply voltages, an additional diode and switching capacitor have to be added. In this option, the output current capability of the charge pump is reduced.

5.1.1.1 Charge pump modes

The charge pump is automatically selecting single-stage mode if $V_{VSCP} > V_{VSCP\_HV}$ in order to minimize the internal power dissipation.

In case three-stage charge pump configuration is enabled by a dedicated control bit, then for $V_{VSCP} < V_{VSCP\_LV}$ the charge pump operates in the triple-stage mode.

Table 7 Charge pump mode (Two-stage charge pump configuration)

Charge pump mode	VSCP range
Double-stage mode	$V_{VSCP} < V_{VSCP\_HV}$
Single stage mode	$V_{VSCP} > V_{VSCP\_HV}$

Table 8 Charge pump mode (Three-stage charge pump configuration)

Charge pump mode	VSCP range
Triple-stage mode	$V_{VSCP} < V_{VSCP\_LV}$
Double-stage mode	$V_{VSCP\_HV} > V_{VSCP} > V_{VSCP\_LV}$
Single-stage mode	$V_{VSCP} > V_{VSCP\_HV}$

5.1.1.2 Charge pump frequency configuration

The charge pump frequency is configurable:

- Setting 1 (default): 250kHz
- Setting 2: 220kHz

- Setting 3: 200kHz
- Setting 4: 175kHz

5.1.2 Microcontroller interface supply: VIO

The internal logic power supply is supplied from VIO supply pin. VIO pin is the input supply for the digital input, output pins (SDI, SDO, CSN, SCK, ILx, IHx_N) and the current sense amplifier of the device (see Chapter 7.1.1). Digital input and output pins and SPI communication is available if V_{VIO} is within the functional range. Digital input pin "low" and "high" thresholds are reference to VIO supply.

The device is capable to operate with 3.3 V and 5 V microcontroller supply. Undervoltage and overvoltage detection thresholds are configurable see Chapter 9.4.6.2.

Once the device has powered-up the device keeps its register values (configuration) for $V_{VIO} > V_{VIO\_PORf}$.

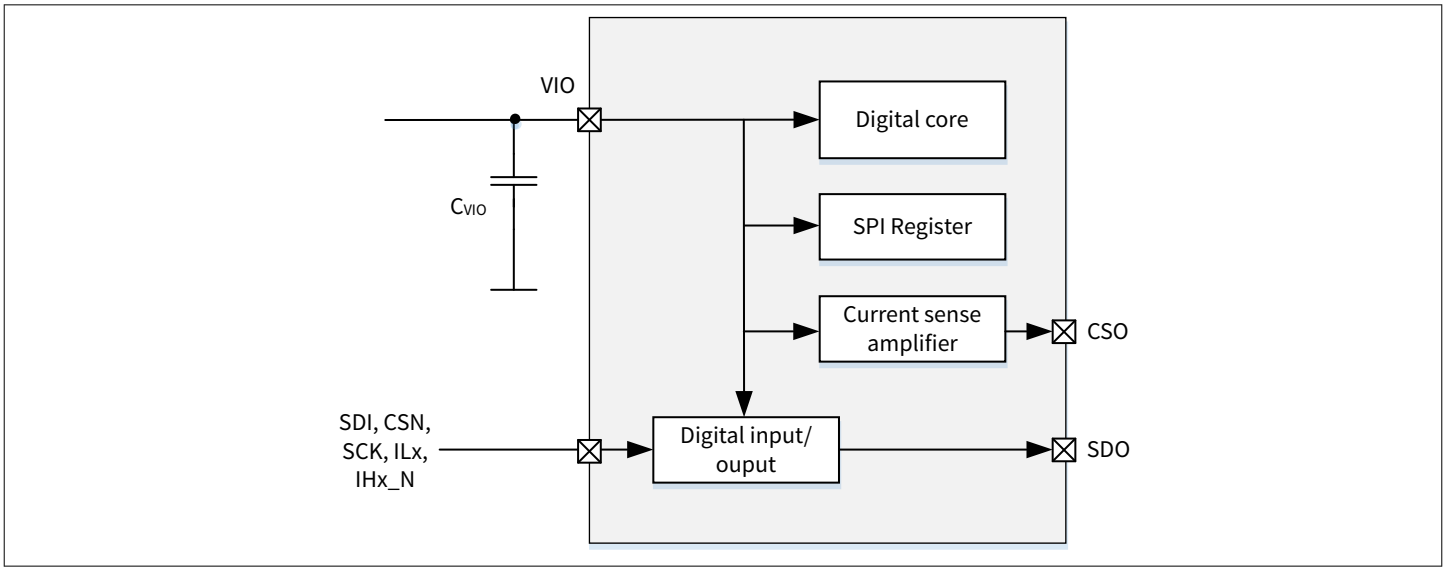

Figure 7 Simplified VIO power supply block

5.2 Electrical characteristics (power supply)

Table 9 Electrical characteristics - power supply

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C; normal operating mode, power-up mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Charge pump frequency accuracy	f_{CP_ACC}	-12	–	12	%	nominal charge pump frequency is defined in Chapter 5.1.1.2	P_SUP_01_01
Regulated charge pump output voltage VCPH vs. VSCP	V_{VCPH}	11	–	15.5	V	1)	P_SUP_01_02

(table continues...)

Table 9 (continued) Electrical characteristics - power supply

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C; normal operating mode, power-up mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Regulated charge pump output voltage VCPH vs. VSCP	V_{VCPH}	9	–	15.5	V	1) Two-stage charge pump configuration 7V < V_{VSCP} < 8V	P_SUP_01_10
Regulated charge pump output voltage VCPH vs. VSCP	V_{VCPH}	8.5	–	15.5	V	2) Three-stage charge pump configuration 4.5V < V_{VSCP} < 8V	P_SUP_01_11
Maximum charge pump load current	I_{VCPH}	-9	–	–	mA	1)	P_SUP_01_04
Maximum charge pump load current	I_{VCPH}	-4.8	–	–	mA	2) Three-stage charge pump configuration 4.5V < VSCP < 8V	P_SUP_01_05
Charge pump high-voltage mode select threshold	V_{VSCP_HV}	17	17.75	18.5	V	Rising edge; Two-Stage Charge Pump configuration	P_SUP_01_06
Charge pump high-voltage mode select threshold	V_{VSCP_HV}	19.0		21	V	Rising edge; Three-Stage Charge Pump configuration	P_SUP_01_07
Charge pump low-voltage mode select threshold	V_{VSCP_LV}	8.5	–	9.5	V	Falling edge Three-stage charge pump configuration	P_SUP_01_08
Turn-on time of charge pumps	t_{ON_VCPH}	20	250	600	µs	I_{VCPH} = 0 mA; 3) 4)	P_SUP_01_09
Blank time of charge pumps	t_{BLANK_CP}	410	600	940	µs	Applicable after charge pump enabling after SPI activation or automatic reactivation	P_SUP_01_10
Charge pump mode threshold hysteresis	$V_{VSCP\_HV\_hys}$	0.3	0.5	0.7	V	–	P_SUP_01_11

1) The current is calculated by I_{VCPH} = number of switching MOSFETs × f_{PWM} × Q_{gtot} = 7.2 mA + additional external circuity supplied by charge pump (1 mA).
2) The current is calculated by I_{VCPH} = number of switching MOSFETs × f_{PWM} × Q_{gtot} = 4.8 mA
3) C_{CP1N} = C_{CP2N} = 220 nF, C_{CPH} = 470 nF
4) Parameter dependent on the capacitance selected charge pump capacitors C_{CP1N}, C_{CP2N} and C_{CPH}

6 Gate driver

The gate driver unit integrates four floating gate drivers capable of controlling a wide range of n-channel MOSFETs which are configured half-bridges to drive DC brushed motors.

A floating high-side or low-side driver is connected between gate and source of an external MOSFET in order to

- Charge and discharge the MOSFET gate by a programmable current-controlled output stage, or
- Keep the MOSFET gate discharged in any condition where no active switching is intended

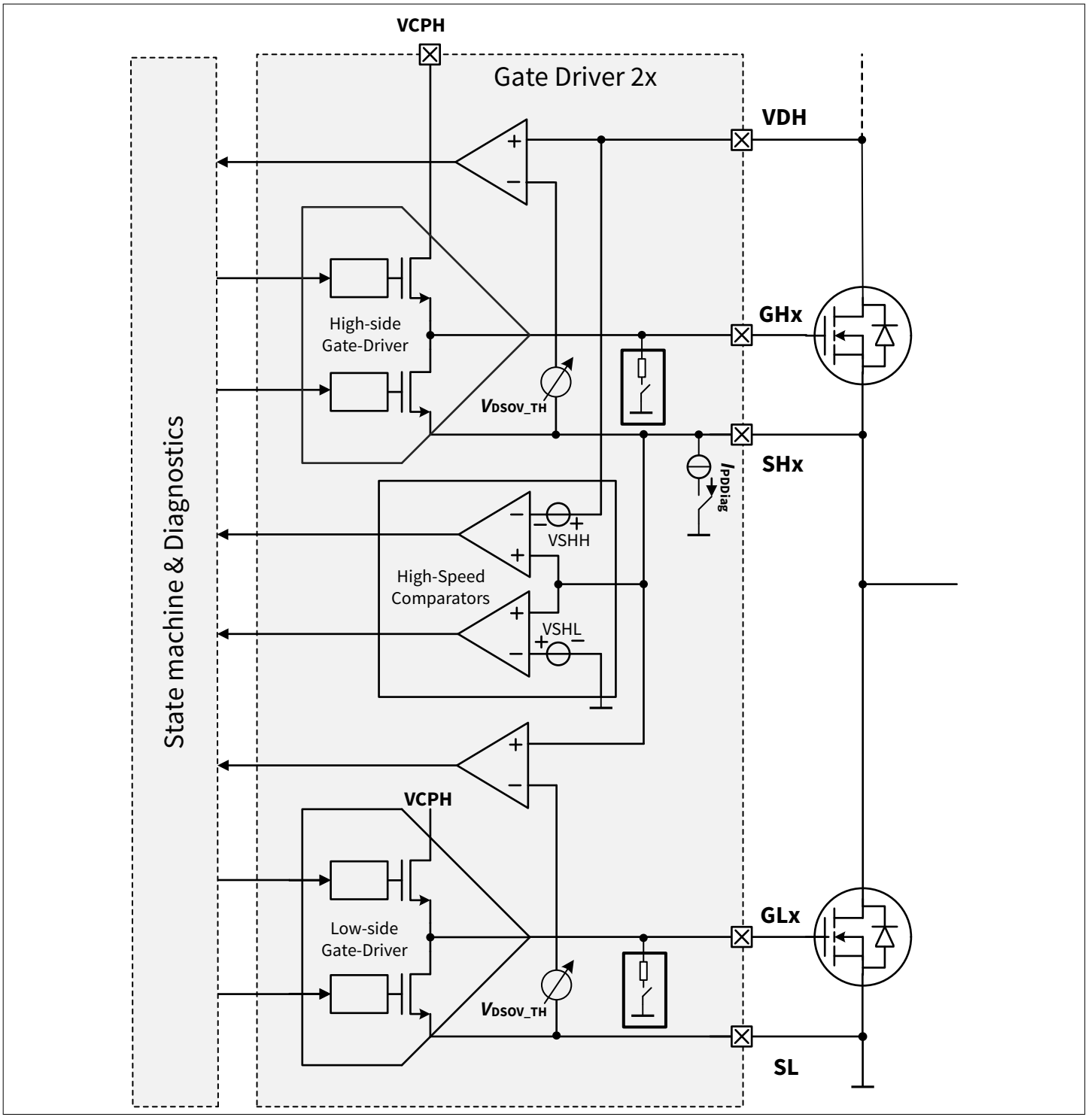

Figure 8 Simplified block diagram: gate driver

6.1 PWM Operation

The pins IHx_N and ILx provide the PWM signal for GHx and GLx output stage. For typical configuration of the input signals to gate driver output stages see Figure 8.

The “active driver” is the gate driver in a half-bridge which controls the slew rate of the motor phase of the “active MOSFET”. It generates the current and voltage slopes during PWM operation of an inductive load. Depending on the direction of the load current this is either the low-side or the high-side gate driver.

The active output stage can be automatically determined by observing the output signals of the phase voltage comparators (see Chapter 6.3).

The automatic detection of the "active driver" and "freewheeling driver" is always enabled. Depending on the phase voltage VSHx the "active driver and "freewheeling driver" can be determined. The active free-wheeling reduces the power dissipation of the free-wheeling MOSFET. If an active MOSFET is OFF, the opposite MOSFET of the same half-bridge is actively turned on. Please see Chapter 6.2.2 for further details.

The device includes a function to map each ILx PWM input pin to control the assigned low-side and high-side output stage of the half-bridge. The function is disabled by default. In case the function is enabled and the device is in normal operation mode, charge pump enabled and half-bridges are enabled, then if:

- ILx = "low": Low-side GLx is kept OFF and high-side GHx is turn ON
- ILx = "high": Low-side GLx is turn ON and high-side GHx is kept OFF

During transition of ILx pin from "high" to "low" or vice versa the cross-current protection time is generated internally by the device.

6.2 Gate current control

6.2.1 Global control

The gate current control unit can be programmed to select the control input signals for each half bridge separately from different sources which are then validated against shoot-through conditions and a programmable cross-conduction protection time.

Table 10 Cross-current protection time configuration

Parameter	Symbol	Unit	Range min	Range max	Step width	Default
Cross-current protection time active MOSFET	t_{CCP}	ns	240	3840	240	2160
Cross-current protection time free-wheeling MOSFET	t_{CCP_FW}	ns	240	3840	240	2160

6.2.2 Active MOSFET detection

The MOSFET of a half bridge, which controls the slew rate at the motor phase, is called the active MOSFET while the other MOSFET of the same half bridge is called the free-wheeling (FW) MOSFET.

The gate current control unit decides at every switch-on event if the respective MOSFET is an active MOSFET or a free-wheeling MOSFET. The gate driver unit switches each MOSFET as an active MOSFET unless it detects one of the following conditions:

- If the high-side MOSFET *x* is intended to be switched on and $V_{SHx} > V_{SHH}$, this high-side MOSFET is determined as free-wheeling MOSFET
- If the low-side MOSFET *x* is intended to be switched on and $V_{SHx} < V_{SHL}$, this low-side MOSFET is determined as free-wheeling MOSFET

6.2.3 Gate current sequencer

The device includes two current control gate sequencer functions:

- Time programable referenced gate sequencer function (default) see Chapter 6.2.3.1.1
- Fast comparator referenced gate sequencer function see Chapter 6.2.3.1.2

The microcontroller can select the current control gate sequencer function by valid SPI write command on a protected control bit only in power-up mode.

For active MOSFETs the gate current sequencer provides a sequence of four consecutive gate current settings with programmable gate current values and programmable durations separately for switch-on and switch-off events and separately for high-side and low-side MOSFETs.

For active MOSFETs the gate current sequencer includes for charge phase (I2ON) and discharge phase (I2OFF) independent current settings for each output stage.

For active MOSFETs only in case the fast comparator reference gate current sequencer feature is enabled, then the gate current sequencer includes an additional current setting I_{ON} and I_{OFF} used for every output stages.

By default for free-wheeling MOSFETs the gate current sequencer provides a sequence of one gate current setting with a programmable gate current value and a programmable duration, which is used for switch-on and switch-off events and for high-side MOSFETs and low-side MOSFETs.

Additionally the device offers the configurability to start the free-wheeling sequencer with the configured pre-charge/ pre-discharge phase of the active MOSFET.

Whenever the gate current sequencer switches on one MOSFET of a half bridge it discharges the gate of the other MOSFET of the same half bridge with the maximum gate current setting for the duration of the switch-on sequence.

Diagnostic switch off behavior:

In case the switch-off is triggered by a diagnosis event (latched error 1 or safe state entry) the gate current sequencer can be programmed to use either the regular switch-off sequence of an active MOSFET or the following special diagnosis switch-off sequence:

1. Use only the first phase of the regular switch-off sequence of an active MOSFET, then
2. Use a programmable static discharge current until the end of the cross-current protection phase

After finishing any switch-on or switch-off sequence the gate current sequencer keeps on charging the gates of switched on MOSFETs or discharging the gates of switched off MOSFETs with a programmable hold current.

Table 11 Gate current sequencer configuration

Parameter	Range min	Range max	Unit	Number of steps
Gate current values for active MOSFETs	0.5	100	mA	64 (Active MOSFET current setting 1)
	1	150	mA	64 (Active MOSFET current setting 2)
Gate current values for free-wheeling MOSFETs	3.3	100	mA	8
Static discharge current	3.3	100	mA	8
Hold current	10	30	mA	4
Duration (t_{1ON}, t_{2ON}, t_{1OFF}, t_{2OFF}, t_{3OFF})	25	1600	ns	64
Freewheeling time (t_{FW})	25	3200	ns	64

6.2.3.1 Description and example diagrams

6.2.3.1.1 Time programable referenced gate sequencer function

Active turn ON of an output stage

The turn-on of the active high-side MOSFET is done in four steps:

1. Cross-current protection phase: the cross-current protection time t_{CCP_FW} starts when the low-side control signal turns "OFF". During t_{FW}, the low-side MOSFET is turned off with the current I_{FW} while the high-side is kept off with holding current I_{HOLD}. After t_{FW} expires the low-side MOSFET is kept switched off by the current I_{HOLD}. During the following 3 phases the low-side MOSFET is kept off with current I_{DCHG_MAX} .

2. Pre-charge phase: Only after t_{CCP_FW} is expired, the high-side control signal is acknowledged to be set to "ON". As soon as the high-side control "ON" signal is acknowledged, the gate of the high-side MOSFET is charged with the current I_{1ON_HS} for a duration of t_{1ON_HS}. When t_{1ON_HS} expires the charge phase is entered.

3. Charge phase (dI/dt phase and dV/dt phase): In charge phase the charge current is set to the current I_{2ON_HSx}. The gate of the high-side MOSFET will be charged with I_{2ON_HSx} until t_{2ON_HS} expires. After that the post-charge phase is entered.

4. Post-charge phase: In the post charge phase the charge current is set to I_{3ON_HS} until the end of t_{VDS_BLK} + t_{VDS_FILT}. After t_{VDS_BLK} + t_{VDS_FILT} expires, the current will be switched to the holding current I_{HOLD}.

The turn-on of the active low-side MOSFET is done in four steps:

1. Cross-current protection phase: the cross-current protection time t_{CCP_FW} starts when the high-side control signal turns "OFF". During t_{FW}, the high-side MOSFET is turned off with the current I_{FW} while the low-side is kept off with holding current I_{HOLD}. After t_{FW} expires the high-side MOSFET is kept switched off by the current I_{HOLD}. During the following 3 phases the high-side MOSFET is kept off with current I_{DCHG_MAX} .

2. Pre-charge phase: Only after t_{CCP_FW} is expired, the low-side control signal is acknowledged to be set to "ON". As soon as the low-side control "ON" signal is acknowledged the gate of the low-side MOSFET is charged with the current I_{1ON_LS} for a duration of t_{1ON_LS}. When t_{1ON_LS} expires the charge phase is entered.

3. Charge phase (dI/dt phase and dV/dt phase): In charge phase the charge current is set to the current I_{2ON_LSx}. The gate of the low-side MOSFET will be charged with I_{2ON_LSx} until t_{2ON_LS} expires. After that the post-charge phase is entered.

4. Post-charge phase: In the post charge phase the charge current is set to I_{3ON_LS} until the end of t_{VDS_BLK} + t_{VDS_FILT}. After t_{VDS_BLK} + t_{VDS_FILT} expires, the current will be switched to the holding current I_{HOLD}.

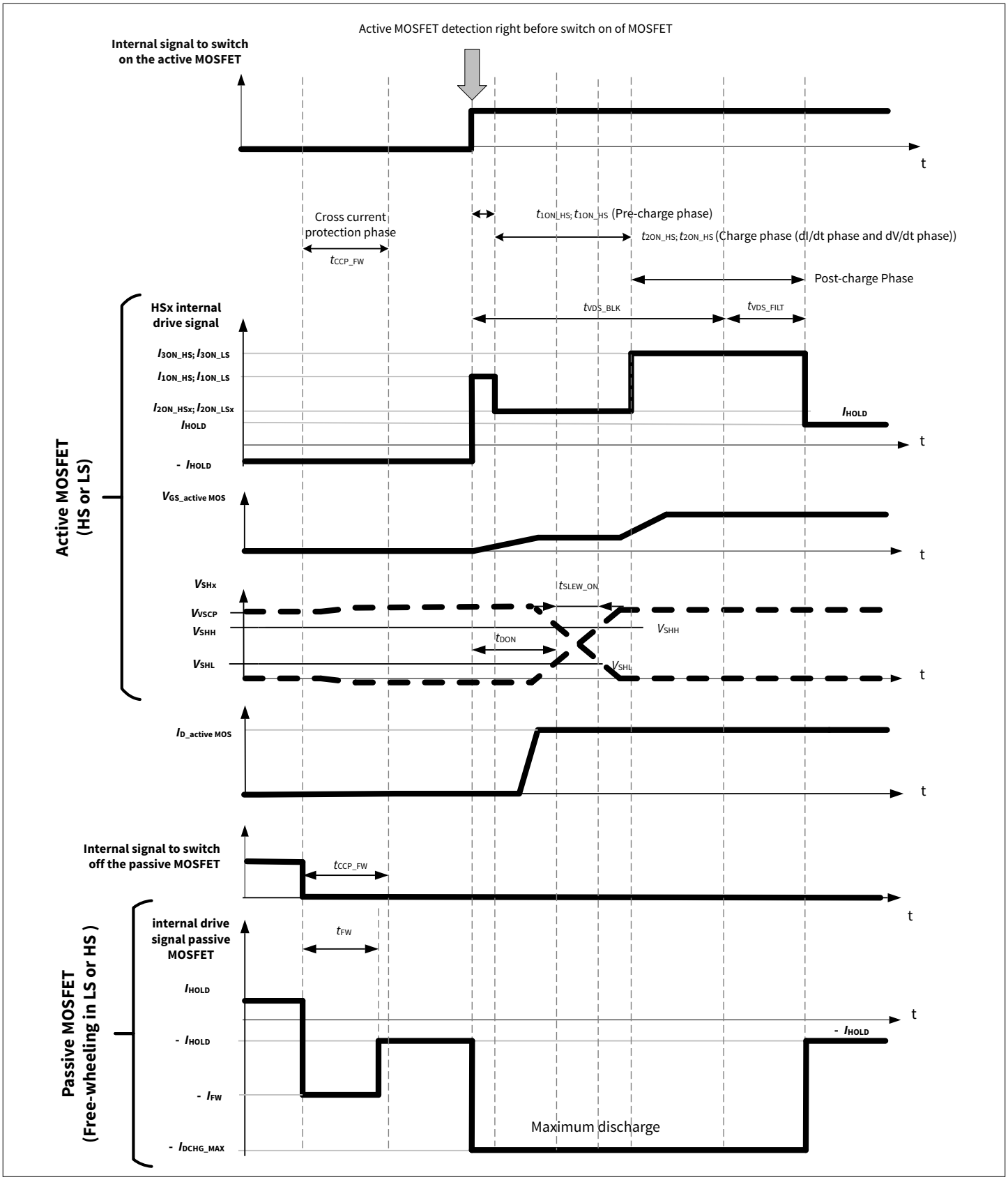

Figure 9 Turn-on of active MOSFET and turn-off of FW MOSFET

Active turn OFF of an output stage

The turn-off of the active high-side MOSFET is done in four steps:

1. Pre-discharge phase: in case the high-side control signal is set to "OFF", the gate of the high-side MOSFET is discharged with the current I_{1OFF_HS} for a duration of t_{1OFF_HS}. After t_{1OFF_HS} expires the discharge phase is entered.

2. Discharge phase (dV/dt phase and dI/dt phase): the gate of the high-side MOSFET is discharged with the current I_{2OFF_HSx} for a duration of t_{2OFF_HS}. After t_{2OFF_HS} expires the post discharge phase is entered.

3. Post discharge phase: the gate of the high-side MOSFET is discharged with the current I_{DCHG_MAX} for a duration of t_{3OFF_HS}. After t_{3OFF_HS} expires the holding phase is entered.

4. Holding phase: In the holding phase the high-side MOSFET will be kept off with the holding current I_{HOLD}. Only after t_{CCP} the low-side control signal is acknowledged to be set to "ON". As soon as the low-side control "ON" signal is acknowledged the low-side MOSFET is switched on with the current I_{FW} for the time t_{FW}. During the time t_{FW} the holding current for the high-side MOSFET is increased to I_{DCHG_MAX}. After t_{FW} is expired, both MOSFETs are kept in their current state by I_{HOLD}.

The turn-off of the active low-side MOSFET is done in four steps:

1. Pre-discharge phase: in case the low-side control signal is set to "OFF", the gate of the low-side MOSFET is discharged with the current I_{1OFF_LS} for a duration of t_{1OFF_LS}. After t_{1OFF_LS} expires the discharge phase is entered.

2. Discharge phase (dV/dt phase and dI/dt phase): the gate of the low-side MOSFET is discharged with the current I_{2OFF_LSx} for a duration of t_{2OFF_LS}. After t_{2OFF_LS} expires the post discharge phase is entered.

3. Post discharge phase: the gate of the low-side MOSFET is discharged with the current I_{DCHG_MAX} for a duration of t_{3OFF_LS}. After t_{3OFF_LS} expires the holding phase is entered.

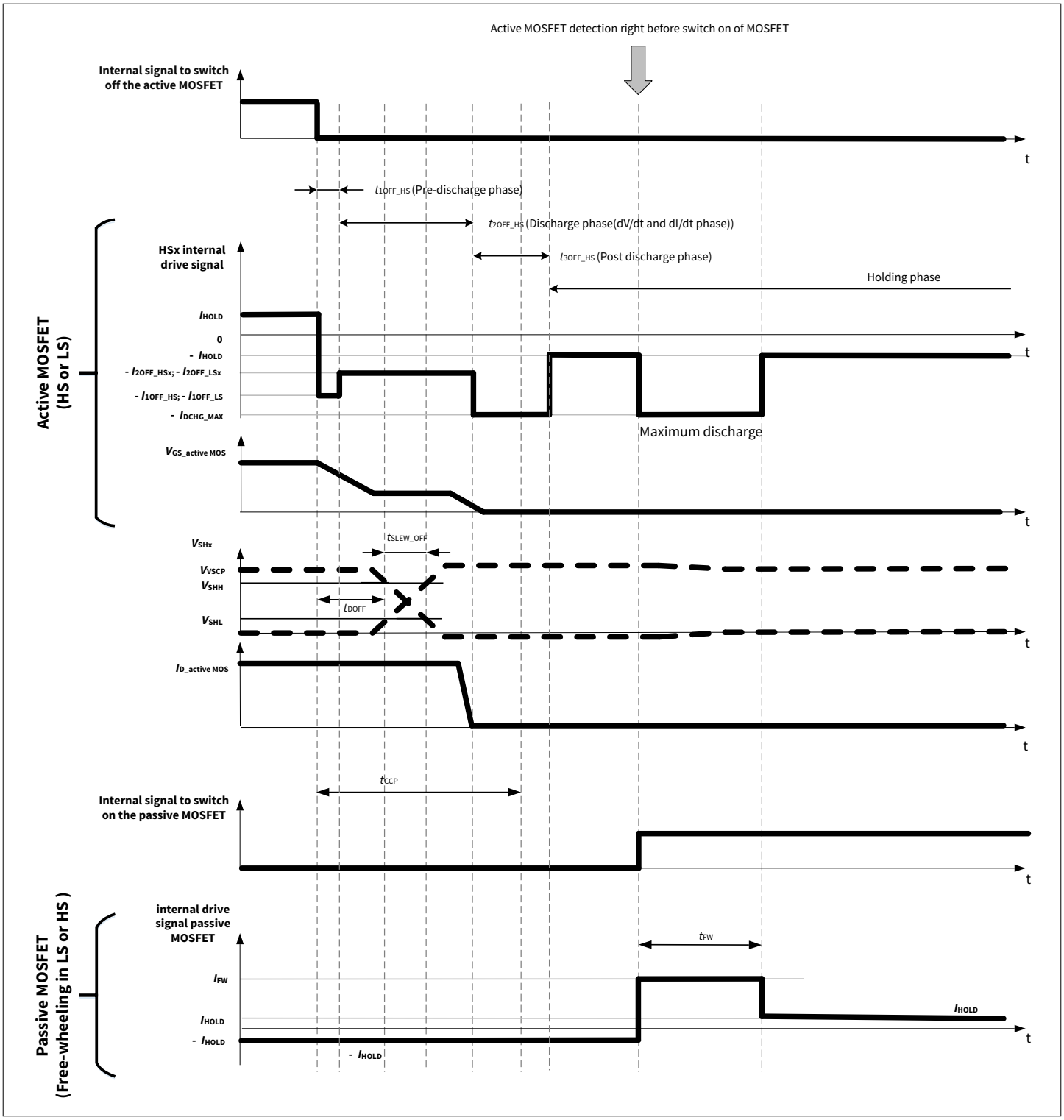

Figure 10 Turn-off of active MOSFET and turn-on of FW MOSFET

6.2.3.1.2 Fast comparator referenced gate sequencer function

Active turn ON of an output stage

The turn-on of the active high-side MOSFET is done in four steps:

1. Cross-current protection phase: the cross-current protection time t_{CCP_FW} starts when the low-side control signal turns "OFF. During t_{CCP_FW}, the low-side MOSFET is turned off with pre-discharge current I_{1OFF_LS} for t_{1OFF_LS}. When t_{1OFF_LS} expires the freewheeling MOSFET is discharged with I_{FW} until $t_{OFF\_timeout}$ has elapsed. After $t_{OFF\_timeout}$ the freewheeling MOSFET is kept in its current state by I_{HOLD}. The low-side is kept off with current I_{DCHG_MAX} until $t_{VDS\_BLK} + t_{VDS\_FILT}$ has elapsed.

2. Pre-charge phase: Only after t_{CCP_FW} is expired, the high-side control signal is acknowledged to be set to "ON". As soon as the high-side control "ON" signal is acknowledged, the gate of the high-side MOSFET is charged with the current I_{1ON_HS} for a duration of t_{1ON_HS}. When t_{1ON_HS} expires it enters the miller-charge phase. In case during pre-charge phase the phase voltage V_{SHx} reaches V_{SHL} before t_{1ON_HS}, then the current is changed from I_{1ON_HS} directly to I_{2ON_HSx}.

3. Charge phase (dI/dt phase): The charge current is decreased from I_{1ON_HS} down to the charge current I_{ON}. The gate of the high-side MOSFET will be charged with I_{ON} until the phase voltage V_{SHx} reaches V_{SHL}.

4. Miller-charge phase (dV/dt phase): The charge current is changed from I_{ON} to the miller-charge current I_{2ON_HSx}. The gate of the high-side MOSFET will be charged with I_{2ON_HSx} until the phase voltage V_{SHx} reaches V_{SHH}.

4. Post-charge phase: After the charge phase, the charge current is set to post-charge current I_{3ON_HS} until the end of $t_{VDS\_BLK} + t_{VDS\_FILT}$. If the device is still in the ramping phase of the post-charge current when $t_{VDS\_BLK} + t_{VDS\_FILT}$ has expired, the ramp phase will be extended until it reaches I_{3ON_HS}. After $t_{VDS\_BLK} + t_{VDS\_FILT}$ expires and I_{3ON_HS} is reached, the current will be switched to the holding current I_{HOLD}.

The turn-on of the active low-side MOSFET is done in four steps:

1. Cross-current protection phase: the cross-current protection time t_{CCP_FW} starts when the high-side control signal turns "OFF". During t_{CCP_FW}, the high-side MOSFET is turned off with pre-discharge current I_{1OFF_HS} for t_{1OFF_HS}. When t_{1OFF_HS} expires the freewheeling MOSFET is discharged with I_{FW} until $t_{OFF\_timeout}$ has elapsed. After $t_{OFF\_timeout}$ the freewheeling MOSFET is kept in its current state by I_{HOLD}. The high-side is kept off with current I_{DCHG_MAX} until $t_{VDS\_BLK} + t_{VDS\_FILT}$ has elapsed.

2. Pre-charge phase: Only after t_{CCP_FW} is expired, the low-side control signal is acknowledged to be set to "ON". As soon as the low-side control "ON" signal is acknowledged, the gate of the low-side MOSFET is charged with the current I_{1ON_LS} for a duration of t_{1ON_LS}. When t_{1ON_LS} expires it enters the miller-charge phase. In case during pre-charge phase the phase voltage V_{SHx} reaches V_{SHH} before t_{1ON_LS}, then the current is changed from I_{1ON_LS} directly to I_{2ON_LSx}.

3. Charge phase (dI/dt phase): The charge current is decreased from I_{1ON_LS} down to the charge current I_{ON}. The gate of the low-side MOSFET will be charged with I_{ON} until the phase voltage V_{SHx} reaches V_{SHH}.

4. Miller-charge phase (dV/dt phase): The charge current is changed from I_{ON} to the miller-charge current I_{2ON_LSx}. The gate of the low-side MOSFET will be charged with I_{2ON_LSx} until the phase voltage V_{SHx} reaches V_{SHL}.

4. Post-charge phase: After the charge phase, the charge current is set to post-charge current I_{3ON_LS} until the end of $t_{VDS\_BLK} + t_{VDS\_FILT}$. If the device is still in the ramping phase of the post-charge current when $t_{VDS\_BLK} + t_{VDS\_FILT}$ has expired, the ramp phase will be extended until it reaches I_{3ON_LS}. After $t_{VDS\_BLK} + t_{VDS\_FILT}$ expires and I_{3ON_LS}. is reached, the current will be switched to the holding current I_{HOLD}.

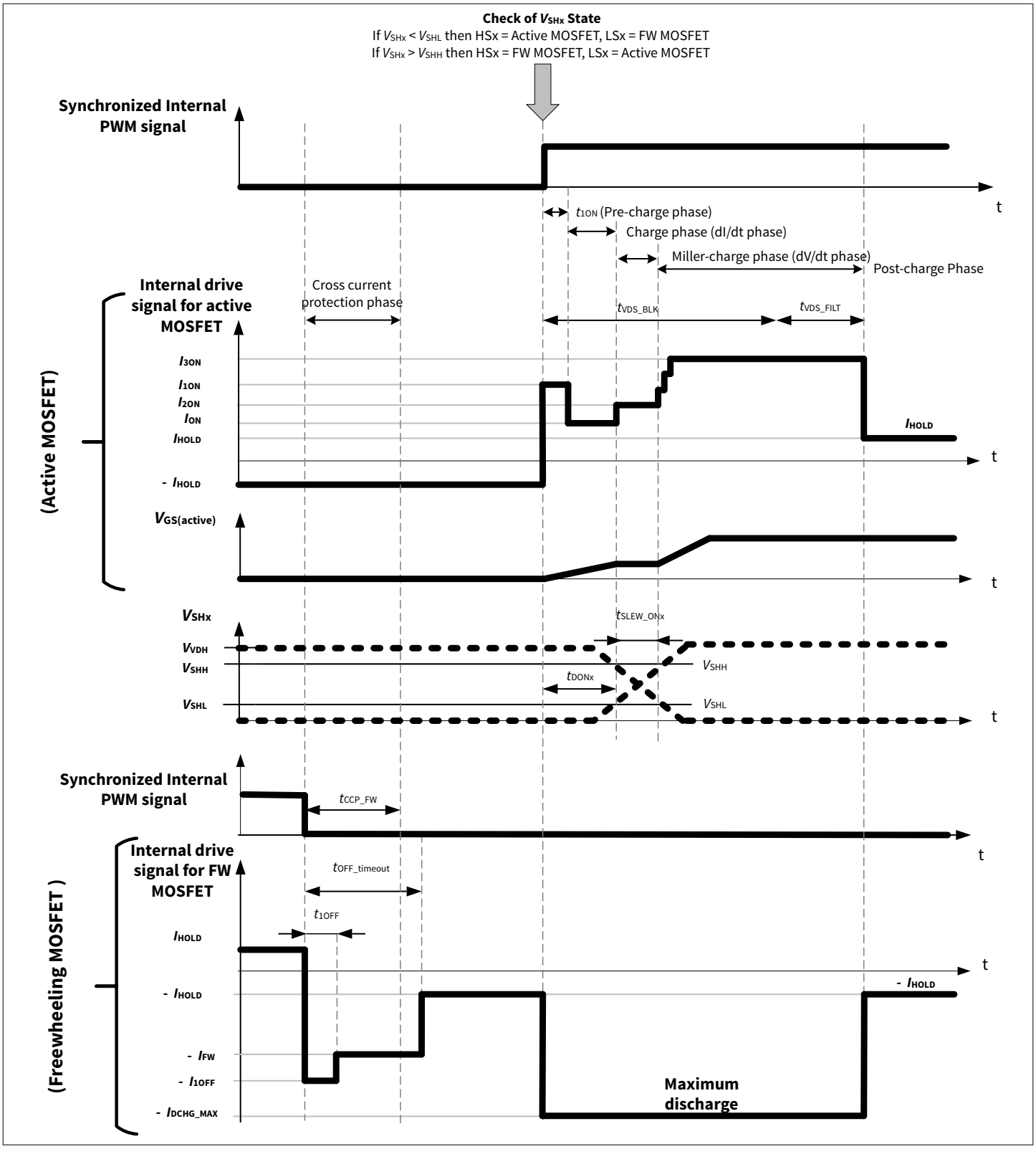

Figure 11 Simplified diagram: Turn on behavior of active MOSFET

Active turn OFF of an output stage

Cross-current protection time t_{CCP} represents the time after which the complementary MOSFET in the same half-bridge can be activated. Therefore t_{CCP} is the minimum discharge time for the MOSFET. $t_{OFF\_timeout}$ is the maximum time for discharge with discharge current I_{DCHG_MAX}. In case the uC applies an external cross current protection time which is longer than the configured internal cross current protection time at the PWM input pins of the driver, the external cross current protection time is used.

The turn-off of the active high-side MOSFET is done in four steps:

1. Pre-discharge phase: in case synchronized IHx is set to low, the gate of the high-side MOSFET is pre-discharged with the current I_{1OFF_HS} for a duration of t_{1OFF_HS}. After t_{1OFF_HS} time expires the discharge current is changed to I_{2OFF_HSx}. In case during pre-discharge phase the phase voltage V_{SHx} reaches V_{SHH} before t_{1OFF_HS}, then the current is changed from I_{1OFF_HS} directly to I_{2OFF_HSx}.

2. Miller-discharge phase (dV/dt phase): the gate of the high-side MOSFET is discharged with current I_{2OFF_HSx} until V_{SHx} reaches V_{SHL}. When V_{SHx} reaches V_{SHL} the post discharge phase is entered.

3. Discharge phase (dI/dt phase): The discharge phase is part of the post discharge phase.
When V_{SHx} reaches V_{SHL} the high-side MOSFET is discharged with I_{OFF} for the configured extension time t_{3OFF_HS}.

4. Post discharge phase: Once t_{3OFF_HS} expires the gate of the high-side MOSFET is discharged with the maximum discharge current I_{DCHG_MAX} until $t_{OFF\_timeout}$ expires. After $t_{OFF\_timeout}$ expires the holding phase is entered.

5. Holding phase: After the $t_{OFF\_timeout}$ expires the high-side MOSFET will be kept off with holding current I_{HOLD}.

The turn-off of the active low-side MOSFET is done in four steps:

1. Pre-discharge phase: in case synchronized ILx is set to low, the gate of the high-side MOSFET is pre-discharged with the current I_{1OFF_LS} for a duration of t_{1OFF_LS}. After t_{1OFF_LS} time expires the discharge current is changed to I_{2OFF_LSx}. In case during pre-discharge phase the phase voltage V_{SHx} reaches V_{SHL} before t_{1OFF_LS}, then the current is changed from I_{1OFF_LS} directly to I_{2OFF_LSx}.

2. Miller-discharge phase (dV/dt phase): the gate of the high-side MOSFET is discharged with current I_{2OFF_LSx} until V_{SHx} reaches V_{SHH}. When V_{SHx} reaches V_{SHH} the post discharge phase is entered.

3. Discharge phase (dI/dt phase): The discharge phase is part of the post discharge phase.
When V_{SHx} reaches V_{SHH} the low-side MOSFET is discharged with I_{OFF} for the configured extension time t_{3OFF_LS}.

4. Post discharge phase: Once t_{3OFF_LS} expires the gate of the low-side MOSFET is discharged with the maximum discharge current I_{DCHG_MAX} until $t_{OFF\_timeout}$ expires. After $t_{OFF\_timeout}$ expires the holding phase is entered.

5. Holding phase: After the $t_{OFF\_timeout}$ expires the low-side MOSFET will be kept off with holding current I_{HOLD}.

In the holding phase the active MOSFET will be kept off with the holding current I_{HOLD}. Only after t_{CCP} the control signal for the freewheeling MOSFET is acknowledged to be set to "ON". As soon as the freewheeling MOSFET control "ON" signal is acknowledged the freewheeling MOSFET is switched on with the corresponding pre-charge current I_{1ON_HS} / I_{1ON_LS} for a duration of t_{1ON_HS} / t_{1ON_LS}. When t_{1ON_HS} / t_{1ON_LS} expires the freewheeling MOSFET is charged with I_{FW} until $t_{VDS\_BLK\_FW} + t_{VDS\_FILT}$ has elapsed. After $t_{VDS\_BLK\_FW} + t_{VDS\_FILT}$ the freewheeling MOSFET is kept in its current state by I_{HOLD}.

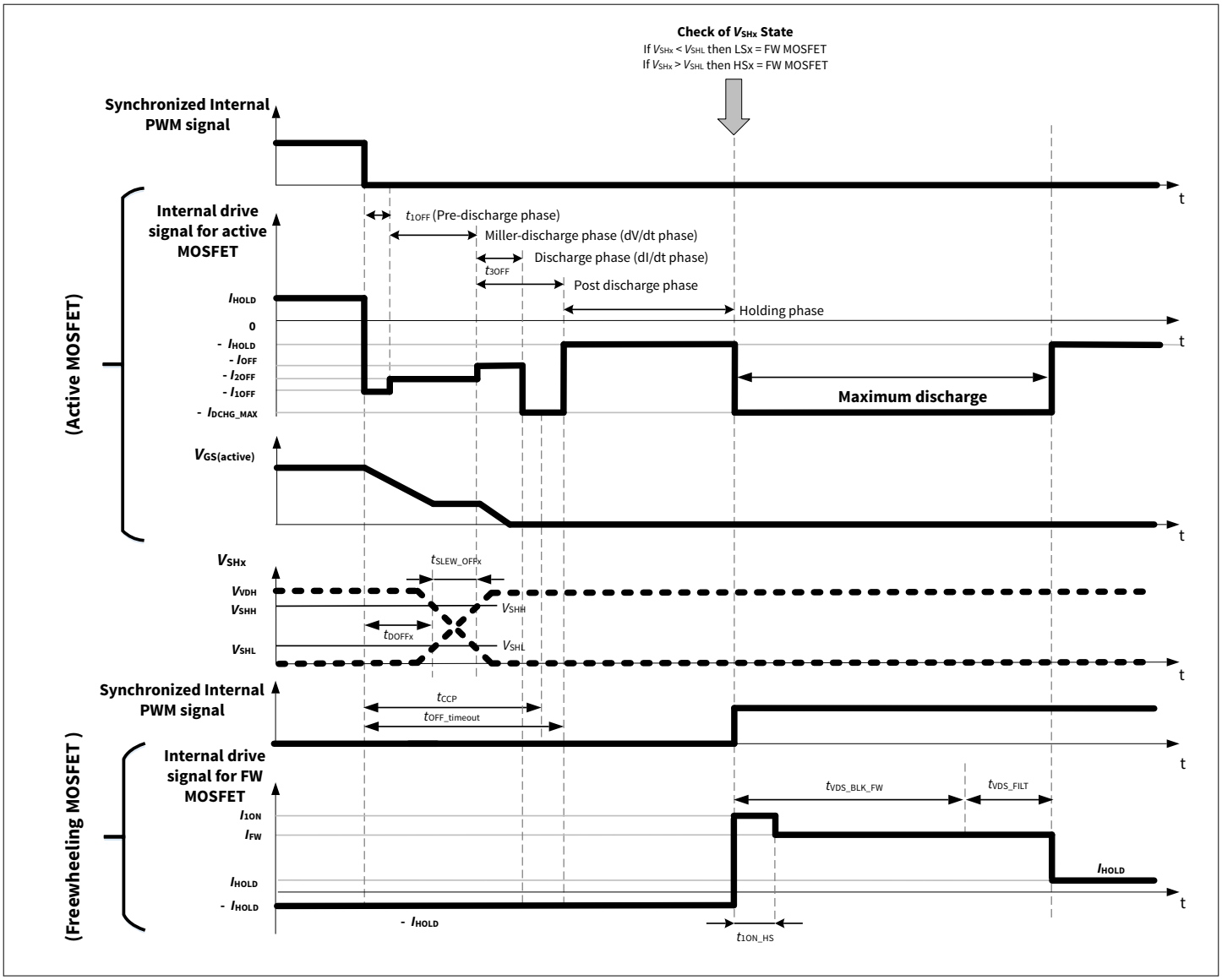

Figure 12 Simplified diagram: Turn off behavior of active MOSFET

6.2.3.2 Configurable current settings overview

6.2.3.2.1 Configurable time settings overview

Time settings for t_{1ON}, t_{2ON}, t_{1OFF}, t_{2OFF}, t_{3OFF} are configurable for high-side and low-side output stages with the nominal values shown in below table.

Table 12 Time settings for t_{1ON}, t_{2ON}, t_{1OFF}, t_{2OFF}, t_{3OFF}

Setting options for t_{1ON}, t_{2ON}, t_{1OFF}, t_{2OFF}, t_{3OFF}	Nominal time [ns]	Setting options for t_{1ON}, t_{2ON}, t_{1OFF}, t_{2OFF}, t_{3OFF}	Nominal time [ns]
Setting 1	27	Setting 33	880
Setting 2	53	Setting 34	907
Setting 3	80	Setting 35	933

(table continues...)

Table 12 (continued) Time settings for t_{1ON}, t_{2ON}, t_{1OFF}, t_{2OFF}, t_{3OFF}

Setting options for t_{1ON}, t_{2ON}, t_{1OFF}, t_{2OFF}, t_{3OFF}	Nominal time [ns]	Setting options for t_{1ON}, t_{2ON}, t_{1OFF}, t_{2OFF}, t_{3OFF}	Nominal time [ns]
Setting 4	107	Setting 36	960
Setting 5	133	Setting 37	987
Setting 6	160	Setting 38	1013
Setting 7	187	Setting 39	1040
Setting 8	213	Setting 40	1067
Setting 9	240	Setting 41	1093
Setting 10	267	Setting 42	1120
Setting 11	293	Setting 43	1147
Setting 12	320	Setting 44	1173
Setting 13	347	Setting 45	1200
Setting 14	373	Setting 46	1227
Setting 15	400	Setting 47	1253
Setting 16	427	Setting 48	1280
Setting 17	453	Setting 49	1307
Setting 18	480	Setting 50	1333
Setting 19	507	Setting 51	1360
Setting 20	533	Setting 52	1387
Setting 21	560	Setting 53	1413
Setting 22	587	Setting 54	1440
Setting 23	613	Setting 55	1467
Setting 24	640	Setting 56	1493
Setting 25	667	Setting 57	1520
Setting 26	693	Setting 58	1547
Setting 27	720	Setting 59	1573
Setting 28	747	Setting 60	1600
Setting 29	773	Setting 61	1627
Setting 30	800	Setting 62	1653
Setting 31	827	Setting 63	1680
Setting 32	853	Setting 64	1707

6.2.3.2.2 Configurable current settings overview

The current settings for I_{I1ON} / I_{I2ON} / I_{I3ON} are configurable with the nominal values shown in below table.
The device has two configurable current control ranges for I1ON, I2ON, I3ON, I1OFF, I2OFF:

- Setting 1 (range 1): 0.5 mA - 100 mA
- Setting 2 (range 2): mA - 150 mA

Table 13 Settings options (range 1) for gate current values for active MOSFET: I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF}

Setting option for I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF}	Nominal current [mA]	Setting option for I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF}	Nominal current [mA]
Setting 1	0.5	Setting 33	31.8
Setting 2	0.7	Setting 34	33.7
Setting 3	0.8	Setting 35	35.5
Setting 4	1.1	Setting 36	37.4
Setting 5	1.3	Setting 37	39.4
Setting 6	1.6	Setting 38	41.4
Setting 7	2.0	Setting 39	43.4
Setting 8	2.4	Setting 40	45.4
Setting 9	2.8	Setting 41	47.4
Setting 10	3.4	Setting 42	49.6
Setting 11	3.9	Setting 43	51.7
Setting 12	4.5	Setting 44	53.9
Setting 13	5.3	Setting 45	56.0
Setting 14	6.1	Setting 46	58.2
Setting 15	6.9	Setting 47	60.4
Setting 16	7.8	Setting 48	62.6
Setting 17	8.8	Setting 49	65.0
Setting 18	9.8	Setting 50	67.3
Setting 19	10.9	Setting 51	69.6
Setting 20	12.0	Setting 52	72.0
Setting 21	13.3	Setting 53	74.3
Setting 22	14.4	Setting 54	76.7
Setting 23	15.9	Setting 55	79.1
Setting 24	17.3	Setting 56	81.5
Setting 25	18.7	Setting 57	83.9
Setting 26	20.2	Setting 58	86.4
Setting 27	21.7	Setting 59	88.9
Setting 28	23.3	Setting 60	91.4
Setting 29	24.9	Setting 61	93.9
Setting 30	26.6	Setting 62	96.4

(table continues...)

Table 13 (continued) Settings options (range 1) for gate current values for active MOSFET: I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF}

Setting option for I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF}	Nominal current [mA]	Setting option for I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF}	Nominal current [mA]
Setting 31	28.2	Setting 63	99.0
Setting 32	30.0	Setting 64	101.5

Table 14 Settings options (range 2) for gate current values for active MOSFET: I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF}

Setting option for I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF}	Nominal current [mA]	Setting option for I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF}	Nominal current [mA]
Setting 1	1.0	Setting 33	54.5
Setting 2	1.4	Setting 34	57.2
Setting 3	1.8	Setting 35	60.0
Setting 4	2.3	Setting 36	63.0
Setting 5	2.9	Setting 37	66.0
Setting 6	3.5	Setting 38	69.0
Setting 7	4.3	Setting 39	71.7
Setting 8	5.2	Setting 40	74.5
Setting 9	6.2	Setting 41	77.8
Setting 10	7.3	Setting 42	80.9
Setting 11	8.5	Setting 43	84.0
Setting 12	9.8	Setting 44	87.1
Setting 13	11.1	Setting 45	90.2
Setting 14	12.5	Setting 46	93.3
Setting 15	14.2	Setting 47	96.5
Setting 16	15.9	Setting 48	99.7
Setting 17	17.7	Setting 49	102.9
Setting 18	19.5	Setting 50	106.0
Setting 19	21.4	Setting 51	109.5
Setting 20	23.4	Setting 52	112.6
Setting 21	25.4	Setting 53	115.7
Setting 22	27.5	Setting 54	119.0
Setting 23	29.6	Setting 55	122.4
Setting 24	31.9	Setting 56	125.8
Setting 25	34.2	Setting 57	129.1
Setting 26	36.5	Setting 58	132.4

(table continues...)

Table 14 (continued) Settings options (range 2) for gate current values for active MOSFET: I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF}

Setting option for I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF}	Nominal current [mA]	Setting option for I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF}	Nominal current [mA]
Setting 27	39.0	Setting 59	135.7
Setting 28	41.5	Setting 60	139.0
Setting 29	43.9	Setting 61	142.4
Setting 30	47.0	Setting 62	145.8
Setting 31	49.1	Setting 63	149.2
Setting 32	51.8	Setting 64	152.6

Current settings for I_{FW}, I_{DCHG_ST} follow the selected current control range and is configurable with the nominal values shown in below table.

Table 15 Setting options for gate current values for free-wheeling MOSFETs and static discharge current

Setting for I_{FW}, I_{DCHG_ST}	Range 1: Nominal current [mA]	Range 2: Nominal current [mA]	Setting for I_{FW}, I_{DCHG_ST}	Range 1: Nominal current [mA]	Range 2: Nominal current [mA]
Setting 1	3.4	7.3	Setting 5	45.4	74.5
Setting 2	7.8	15.9	Setting 6	62.6	99.7
Setting 3	17.3	31.9	Setting 7	81.5	125.8
Setting 4	30	51.8	Setting 8	101.5	152.6

I_{HOLD} is the hold current used to keep the gate of the external MOSFETs in the desired state.

- An output stage Gxx is kept ON with the current I_{HOLD}
- An output stage Gxx is kept OFF with the current - I_{HOLD}

Current settings for I_{HOLD} is configurable with the nominal values shown in below table.

Setting options for I_{HOLD}	Nominal current [mA]
Setting 1	10
Setting 2	15 (default)
Setting 3	20
Setting 4	30

6.3 SHx timing measurement

The SHx timing measurement unit provides two high-speed voltage comparators at the SHx pin of each half bridge with thresholds V_{SHH} and V_{SHL} to measure the time from a switch-on or switch-off command until the beginning and the end of the resulting SHx voltage slope during the switch-on and switch-off event of an external MOSFET.

SHx comparator voltage thresholds (V_{SHH} and V_{SHL}) are fixed:

- SHx high level threshold nominal V_{SHH}: V_{VDH} - 2 V
- SHx low level threshold nominal V_{SHL}: GND + 2 V

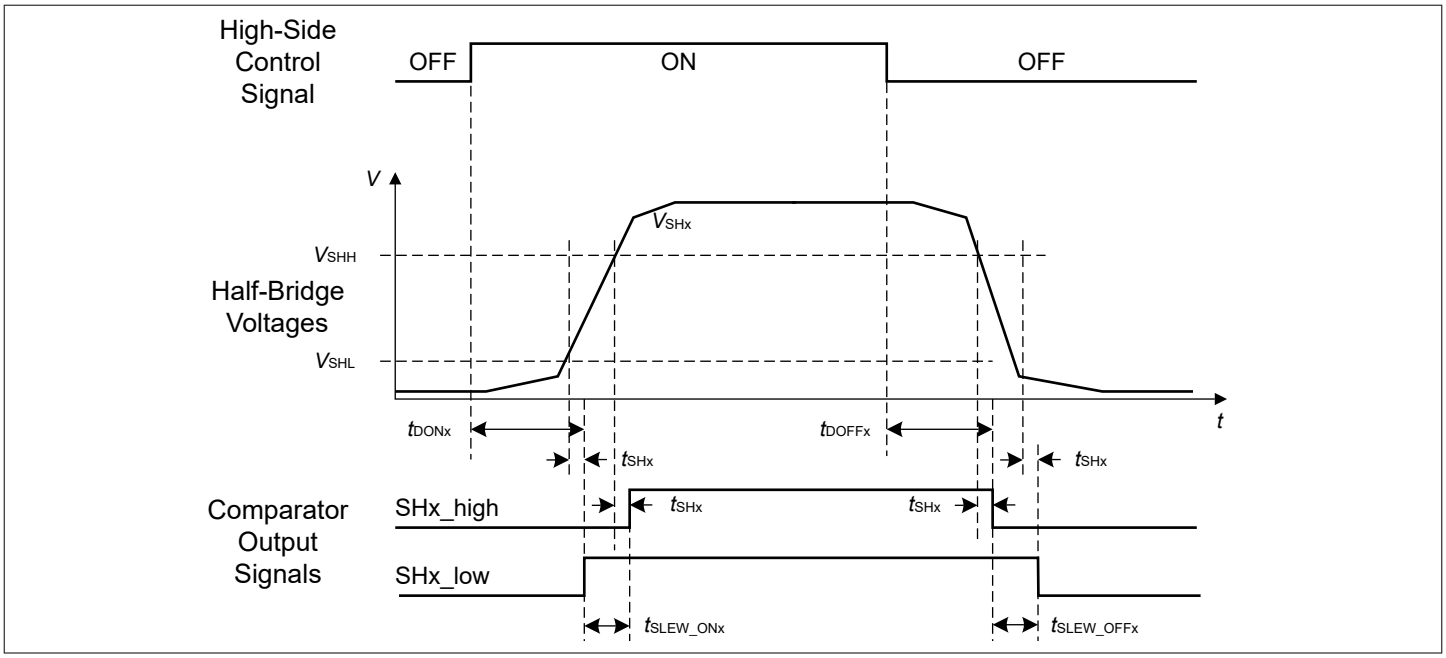

Figure 13 High side SHx comparator timings measurements

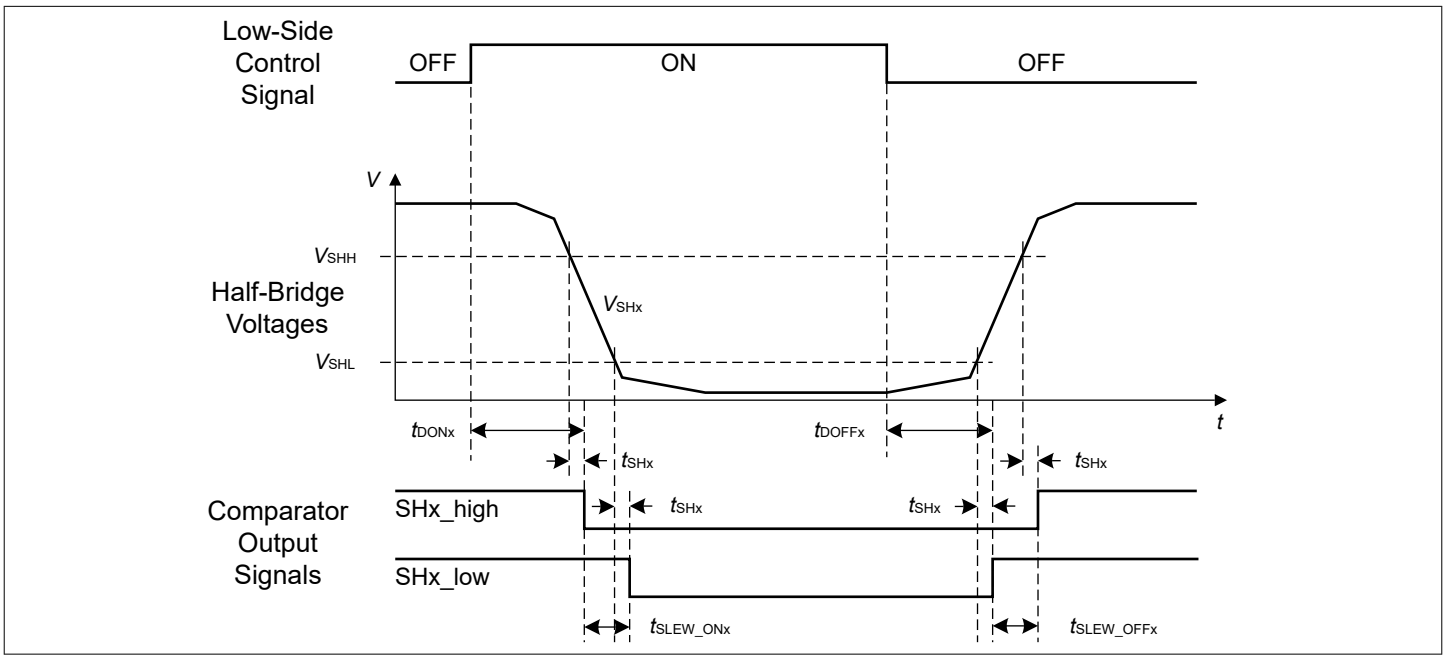

Figure 14 Low side SHx comparator timings measurements

6.4 Passive discharge

Passive discharge is a resistor (R_{GGND}) between the gate of GHx and GND, and between GLx and GND. Passive discharge is active in following condition:

- Device in safe state OR
- Device in sleep mode (VSCP in functional range) OR
- Half-bridge disabled by half bride control bit OR
- Charge pump disabled

6.5 Passive clamping

Passive clamping is only active in following condition:

- Device in safe state OR
- Device in sleep mode OR
- Device unsupplied (VIO below power-on reset threshold) OR
- Half-bridge disabled by half bride control bit OR
- Charge pump disabled

The passive clamping structure is implemented between Gxx and Sxx pin. In case of leakage current on the PCB at the Gxx pins, the passive clamping structure avoids turning on the external MOSFET by sinking the current via R_{GSxP}.

6.6 Electrical characteristics (gate driver)

Table 16 Electrical characteristics - gate driver

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
PWM input pins							
High level input voltage threshold ILx, IHx_N	V_{IH_IN}	0.7 x V_{VIO}	–	–	V	–	P_GDRV_01_01
Low level input voltage threshold ILx, IHx	V_{IL_IN}	–	–	0.3 x V_{VIO}	V	–	P_GDRV_01_02
Hysteresis ILx, IHx_N	V_{IHY_IN}	100	–	–	mV	–	P_GDRV_01_03
Pull down resistor at input pin ILx	R_{PD_ILx}	52	80	108	kΩ	–	P_GDRV_01_04
Pull up resistor at input pin IHx	R_{PU_IHx}	13	20	27	kΩ	–	P_GDRV_01_05
PWM synchronization time	t_{SYNC}	–	13	15	ns	Internal clock frequency: 75 MHz	P_GDRV_01_06
Gate driver							
ON-state output voltage Gxx vs. Sxx	$V_{GS(ON)}$	10	–	12.5	V	V_{VSCP} ≥ 8 V, [1]	P_GDRV_02_01
ON-state output voltage Gxx vs. Sxx	$V_{GS(ON)}$	7.0	–	12.5	V	V_{VSCP} ≥ 7 V, [1]	P_GDRV_02_02
ON-state output voltage Gxx vs. Sxx	$V_{GS(ON)}$	7.0	–	12.5	V	V_{VSCP} ≥ 4.5 V, [2] Three-stage charge pump configuration	P_GDRV_02_03

(table continues...)

Table 16 (continued) Electrical characteristics - gate driver

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
OFF-state output voltage Gxx vs. Sxx	$V_{GS(OFF)}$	–	–	100	mV	I_{HOLD} Setting 1, 1mA injected into Gxx pin	P_GDRV_02_04
RDSON Gxx vs. Sxx	R_{Gxx_OFF}	–	14	20	Ω	$V_{VCPH} > V_{VSCP}$ + 13 V, Programmable gate current setting 64, 50mA forced in the Gxx pin	P_GDRV_02_05
Gate current settling time	t_{GATE_SET}	–	–	100	ns	–	P_GDRV_02_08
Gate driver current turn-on rise time	$t_{GDRV\_RISE(ON)}$	4	25	50	ns	From 20% of I_{GATEx} to 80% of I_{GATEx}, C_{Load} = 6 nF 3)	P_GDRV_02_09
Gate driver current turn-off rise time	$t_{GDRV\_RISE(OFF)}$	4	25	50	ns	From 20% of I_{GATEx} to 80% of I_{GATEx}, C_{Load} = 6 nF 3)	P_GDRV_02_10
Delay on time high frequency	t_{DGDRV_ONx}	–	100	300	ns	From PWM reaching turn on threshold to 20% of I_{Gatex}; t_{SYNC} is included 3)	P_GDRV_02_11
Delay on time low frequency	t_{DGDRV_ONx}	300	350	390	ns	From PWM reaching turn on threshold to 20% of I_{Gatex}, t_{SYNC} is included 3)	P_GDRV_02_12
Delay off time high frequency	t_{DGDRV_OFFx}	–	100	300	ns	From PWM reaching turn off threshold to 20% of I_{Gatex} t_{SYNC} is included 3)	P_GDRV_02_13
Delay off time low frequency	t_{DGDRV_OFFx}	300	340	390	ns	From PWM reaching turn off threshold to 20% of I_{Gatex}, t_{SYNC} is included 3)	P_GDRV_02_14

(table continues...)

Table 16 (continued) Electrical characteristics - gate driver

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Charge/discharge current setting 1 accuracy	I_{CHG1_ACC}	-60	–	+60	%	Valid for Setting 1 of I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF} C_{load} = 4.7 nF, 3) VSCP, Temperature and aging dependencies included Nominal value setting listed in Table 13	P_GDRV_02_15
Charge/discharge current setting 16 accuracy	I_{CHG16_ACC}	-45	–	+45	%	Valid for Setting 16 of I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF} C_{load} = 4.7 nF, 3) VSCP, Temperature and aging dependencies included Nominal value setting listed in Table 13	P_GDRV_02_16
Charge/discharge current setting 32 accuracy	I_{CHG32_ACC}	-30	–	+30	%	Valid for Setting 32 of I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF} C_{load} = 4.7 nF, 3) VSCP, Temperature and aging dependencies included Nominal value setting listed in Table 13	P_GDRV_02_17
Charge/discharge current setting 48 accuracy	I_{CHG48_ACC}	-25	–	+25	%	Valid for Setting 48 of I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF} C_{load} = 4.7 nF, 3) VSCP, Temperature and aging dependencies included Nominal value setting listed in Table 13	P_GDRV_02_18

(table continues...)

Table 16 (continued) Electrical characteristics - gate driver

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Charge/discharge current setting 64 accuracy	I_{CHG64_ACC}	-18	–	+18	%	Valid for Setting 64 of I_{1ON}, I_{2ON}, I_{3ON}, I_{1OFF}, I_{2OFF} C_{load} = 4.7 nF, 3) VSCP, Temperature and aging dependencies included Nominal value setting listed in Table 13	P_GDRV_02_19
Freewheeling charge/discharge current setting 1 accuracy	I_{FW1_ACC}	-50	–	+50	%	Valid for Setting 1 of I_{FW} , I_{DCHG_ST} C_{load} = 4.7nF, Nominal value setting listed in Table 15	P_GDRV_02_21
Freewheeling charge/discharge current setting 4 accuracy	I_{FW4_ACC}	-30	–	+30	%	Valid for Setting 4 of I_{FW} , I_{DCHG_ST} C_{load} = 4.7nF, Nominal value setting listed in Table 15	P_GDRV_02_22
Freewheeling charge/discharge current setting 8 accuracy	I_{FW8_ACC}	-15	–	+15	%	Valid for Setting 8 of I_{FW} , I_{DCHG_ST} C_{load} = 4.7nF, Nominal value setting listed in Table 15	P_GDRV_02_23
Turn off timeout	$t_{OFF\_timeout}$	3.8	4.7	5.6	µs	–	P_GDRV_02_24
SHx fast comparator							
SHx comparator threshold accuracy	V_{SHx_ACC}	-12	–	+12	%	Refer to Chapter 6.3 for nominal V_{SHH} and V_{SHL}	P_GDRV_03_01
SHx comparator delay	t_{SHx}	–	15	30	ns	–	P_GDRV_03_02

(table continues...)

Table 16 (continued) Electrical characteristics - gate driver

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Passive discharge							
Passive clamping between Gxx to Sxx	R_{GSxP}	2.5	4	5.5	kΩ	Device unsupplied OR sleep mode OR safe state V_{Gxx} - V_{Sxx} > 1.8 V @ T_J = -40°C V_{Gxx} - V_{Sxx} > 1.6 V @ T_J = 25°C V_{Gxx} - V_{Sxx} > 1.4 V @ T_J = 150°C	P_GDRV_04_01
Passive discharge resistance between GHx/GLx and GND	R_{GGND}	35	45	55	kΩ	–	P_GDRV_04_02
Resistor between SHx and GND	R_{SHGND}	35	45	55	kΩ	4)	P_GDRV_04_03

1) The current is calculated by I_{VCPH} = number of switching MOSFETs × f_{PWM} × Q_{gtot} = 7.2 mA + additional external circuity supplied by charge pump (1 mA).
2) The current is calculated by I_{VCPH} = number of switching MOSFETs × f_{PWM} × Q_{gtot} = 4.8 mA
3) Valid for V_{VSCP} = 8 … 19 V, V_{VSCP} reference = 13.5 V
4) This resistance is the resistance between GHx and GND connected through a diode to SHx. As a consequence, the voltage at SHx can rise up to 0.6 V typ. before it is discharged through the resistor

7 Current sense amplifier

7.1 Functional description (current sense amplifier)

The current sense amplifier (CSA) allows current measurement with one external shunt resistor in low-side configuration. The CSA function is internally supplied by the charge pump (VCPH). Therefore, if the charge pump is off, then the CSA is deactivated.

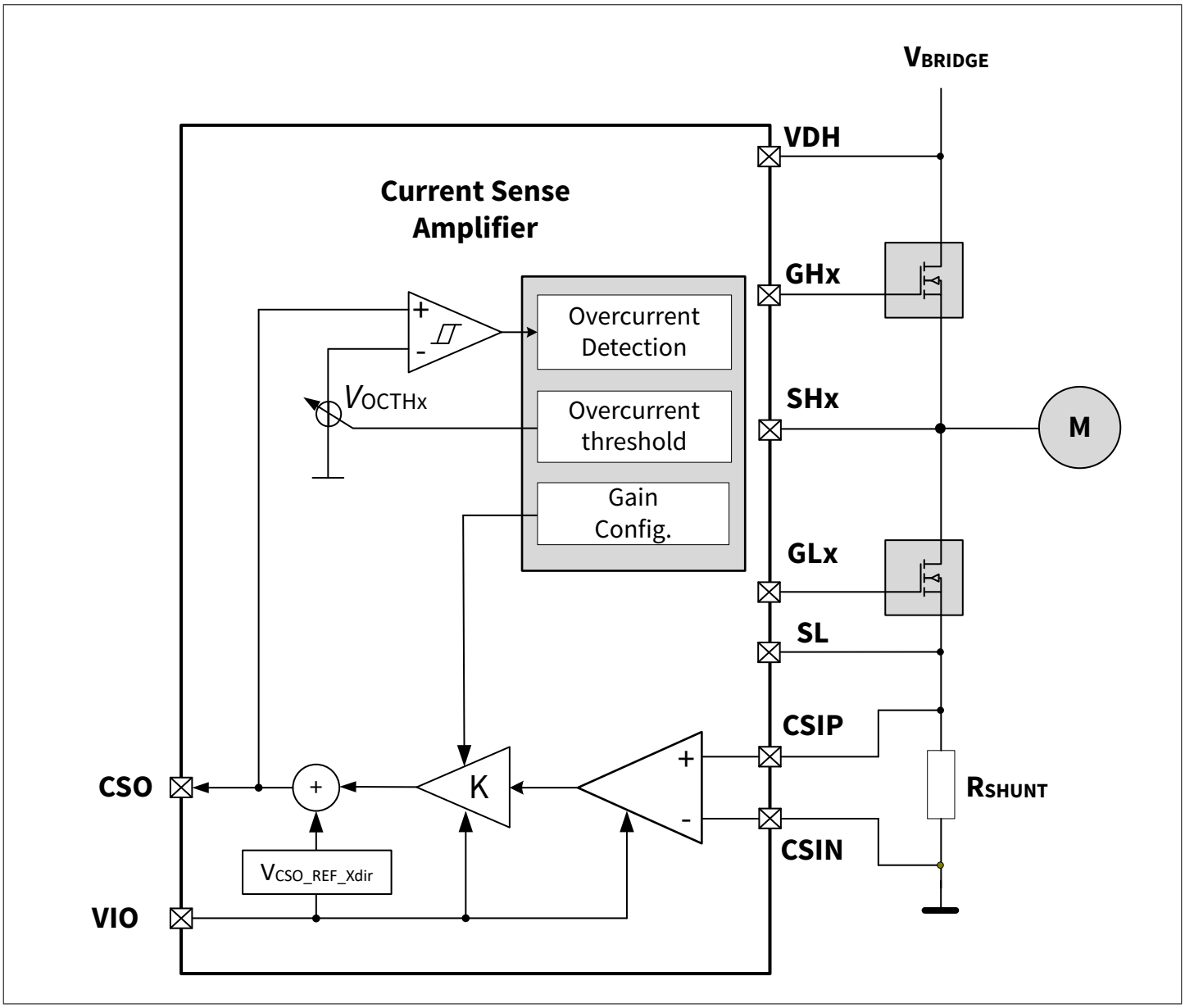

Figure 15 Simplified block diagram: CSA Module

In unidirectional operation, the current sense amplifier is optimized to measure the current flowing through the external shunt resistor when $V_{CSIP} \geq V_{CSIN}$. The resulting output voltage at pin CSO is: $V_{CSO} = V_{CSO\_REF\_Unidir} + (V_{CSIP} - V_{CSIN}) \times G_{DIFF}$ provided that V_{CSO} is in the linear range. Common mode offset and input related offset is neglected.

In bidirectional operation, the CSA measures the current flowing through the external shunt resistor in both directions: $V_{CSIP} \geq V_{CSIN}$ or $V_{CSIP} \leq V_{CSIN}$. The resulting output voltage at pin CSO is symmetrically centered on $V_{CSO\_REF\_Bidir}$: $V_{CSO} = V_{CSO\_REF\_Bidir} + (V_{CSIP} - V_{CSIN}) \times G_{DIFF}$, provided that CSO is in the linear range. Common mode offset and input related offset is neglected.

The gain of the current sense amplifier is configurable:

Gain setting option	Gain setting parameter symbol
Setting 1	G_{DIFF6}
Setting 2	G_{DIFF8}
Setting 3	G_{DIFF10}
Setting 4	G_{DIFF15}
Setting 5	G_{DIFF24}
Setting 6	G_{DIFF40}

The device offers configuration possibility for the output capacitance range. Two capacitance ranges are available. The CSO output capacitance is configurable via SPI configuration.

7.1.1 CSA reference voltage: VIO

The function of VIO pin is fixed as input reference voltage to be supplied externally.

The voltage at VIO is the reference voltage for the CSA output voltage at CSO pin. The configured $V_{CSO\_REF\_Unidir}$ / $V_{CSO\_REF\_Bidir}$ is internally supplied by pin VIO. Therefore, if the VIO is unsupplied, then CSO pin is unsupplied.

7.2 Electrical characteristics (current sense amplifier)

Table 17 Electrical characteristics - current sense amplifier

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C; normal operating mode, power-up mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Operating common mode input voltage range referred to GND (CSIP - GND) or (CSIN- GND)	V_{CM_CSA}	-2.0	–	2.0	V	–	P_CSA_01_01
Common mode rejection ratio	CMRR	58 64 70 76	–	–	dB	Gain setting 1; Gain setting 2; Gain setting 3; Gain setting 4; DC to 50 kHz; V_{CM}= -2 ... 2 V; V_{CSIP} = V_{CSIN}	P_CSA_01_02
CSA settling time to 98%	t_{CSA_SET}	–	1.0	1.5	µs	measured after output filter C_{CSO} = 2.2 nF and R_{CSO} = 50 Ω [1)]	P_CSA_01_03

(table continues...)

Table 17 (continued) Electrical characteristics - current sense amplifier

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C; normal operating mode, power-up mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
CSA settling time to 98% after gain change	$t_{CSA\_SET\_GAIN}$	–	–	4	µs	After gain change via SPI command from CSN rising edge including SPI command interpretation by IC measured after output filter C_{CSO} = 2.2 nF and R_{CSO} = 50 Ω [1)]	P_CSA_01_04
Input offset voltage	V_{CSA_OS}	-1	0	1	mV	–	P_CSA_01_06
Current sense amplifier DC gain	G_{DIFF6}	5.94	5.99	6.04	V/V	Setting 1; $T_J \leq 150°C$	P_CSA_01_07
Current sense amplifier DC gain	G_{DIFF8}	7.92	7.98	8.04	V/V	Setting 2; $T_J \leq 150°C$	P_CSA_01_08
Current sense amplifier DC gain	G_{DIFF10}	9.90	9.98	10.06	V/V	Setting 3; $T_J \leq 150°C$	P_CSA_01_09
Current sense amplifier DC gain	G_{DIFF8}	14.84	14.96	15.08	V/V	Setting 4; $T_J \leq 150°C$	P_CSA_01_10
Current sense amplifier DC gain	G_{DIFF24}	23.74	23.93	24.12	V/V	Setting 5; $T_J \leq 150°C$	P_CSA_01_11
Current sense amplifier DC gain	G_{DIFF40}	39.55	39.87	40.19	V/V	Setting 6; $T_J \leq 150°C$	P_CSA_01_12
CSA gain drift	G_{DRIFT}	-0.1	–	0.1	%	Gain drift after calibration	P_CSA_01_13
Gain accuracy temperature drift	dG_{CSA_TD}	-50	–	50	ppm /K	All gain settings	P_CSA_01_14
CSO single ended output voltage range (linear range)	V_{CSO_linear}	0.4	–	0.9 x V_{VIO}	V	Gain accuracy +/-1%	P_CSA_01_15
CSO single ended output voltage range (extended linear range)	V_{CSO_linear}	0.25	–	V_{VIO} - 0.25	V	Gain accuracy +/-1.5%	P_CSA_01_16
CSO reference voltage unidirectional	$V_{CSO\_REF\_Unidir}$	-1%	0.15 * V_{VIO}	+1%	V	–	P_CSA_01_17

(table continues...)

Table 17 (continued) Electrical characteristics - current sense amplifier

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C; normal operating mode, power-up mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
CSO reference voltage bidirectional	$V_{CSO\_REF\_Bidir}$	-1%	0.5 * V_{VIO}	+1%	V	–	P_CSA_01_18
Power supply rejection ratio	PSRR	60	–	–	dB	f = 1 kHz … 100 kHz	P_CSA_01_21

1) Settling time valid for both available CSA output capacitive load ranges

8 Serial peripherial interface (SPI)

8.1 Functional description (SPI)

8.1.1 SPI description

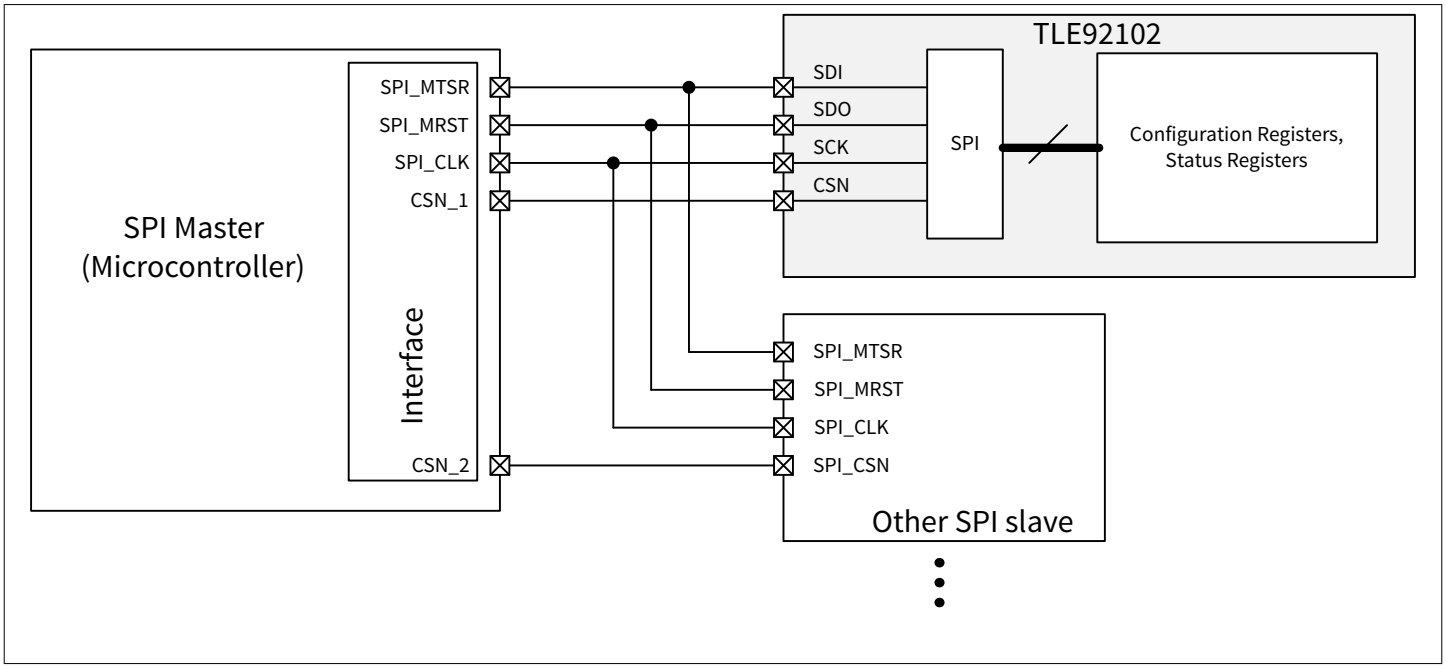

Figure 16 Simplified block diagram: SPI

The control input frame is read via the data input SDI, which is synchronized with the clock input SCK provided by the microcontroller. The output frame of the actual command appears synchronously at the data output SDO see Figure 17.

The transmission cycle begins when the chip is selected by the input CSN (chip select not), LOW active. After the CSN input returns from LOW to HIGH, the received word is interpreted according to the content. The SDO output switches to tristate status (high impedance) at this point, thereby releasing the SDO bus for other use. The state of SDI is shifted into the input register with every falling edge on SCK. The state of SDO is shifted out of the output register after every rising edge on SCK. The SPI of the device is not daisy chain capable.

The SPI has have following two general characteristics:

- Clock polarity is 0 (first edge = rising edge, second edge = falling edge)
- Clock phase is 1 (shifting data on first edge, sampling data on second edge)

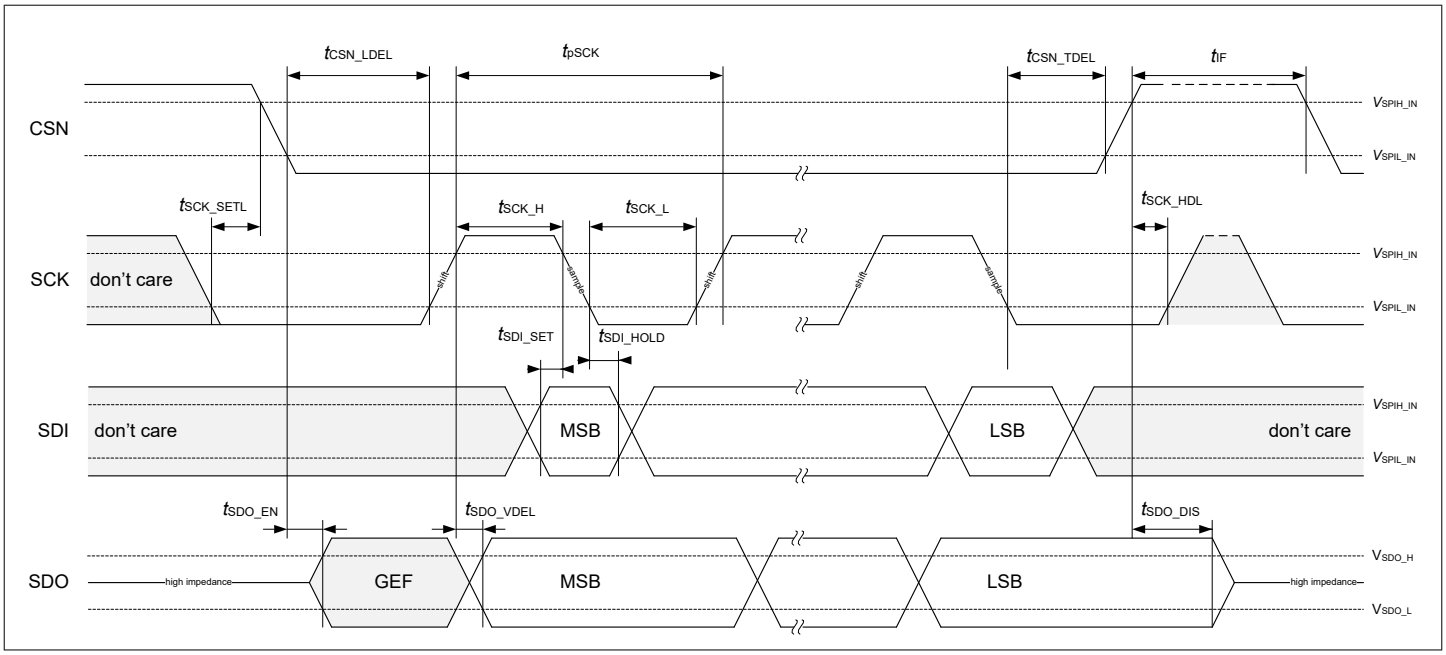

Figure 17 SPI data transfer timing

8.1.1.1 SPI Protocol

A SPI communication consists of 32-bit frames.

SPI response type is configurable only in power-up mode. It is configurable by a protected control bit:

- Setting 1 (default): SDO in-frame response format (IFR)
- Setting 2: SDO next-frame response format (NFR)

8.1.1.1.1 SDI frame format

The SDI frame consists of 7 bit address, 1 command bit "C" and 16 bit write data followed by 8 bit CRC. The 8 bit address bits consist of first 7 bits defining the SPI register address and 1 bit "C" (command) defining if a read command or write command is sent.

- "C" = 1: SPI write command
- "C" = 0: SPI read command

The address byte specifies:

- The type of operation:
  - For configuration and control registers:
    - Read only: C bit = '0'
    - Read and write: C bit = '1'
  - For status registers:
    - Read only: C bit = '0'
    - Read and clear: C bit = '1'
- The target register (A[6:0])

8.1.1.1.2 SDO frame format (in-frame response)

SDO transmits 8 bit global status register + 16 bit read data followed by 8 bit CRC8 (including received SPI register address).

During CSN is set to "low", before a rising edge is sent via SCK, the SDO transmits the global error flag (see Chapter 8.1.2)

Figure 18 SPI protocol for in-frame response (IFR)

8.1.1.1.3 SDO frame format (next frame response)

The SDO transmits 8 bit global status register + 16 bit read data followed by 8 bit CRC8 (including received SPI register address).

During CSN is set to "low", before a rising edge is sent via SCK, the SDO transmits the global error flag (see Chapter 8.1.2)

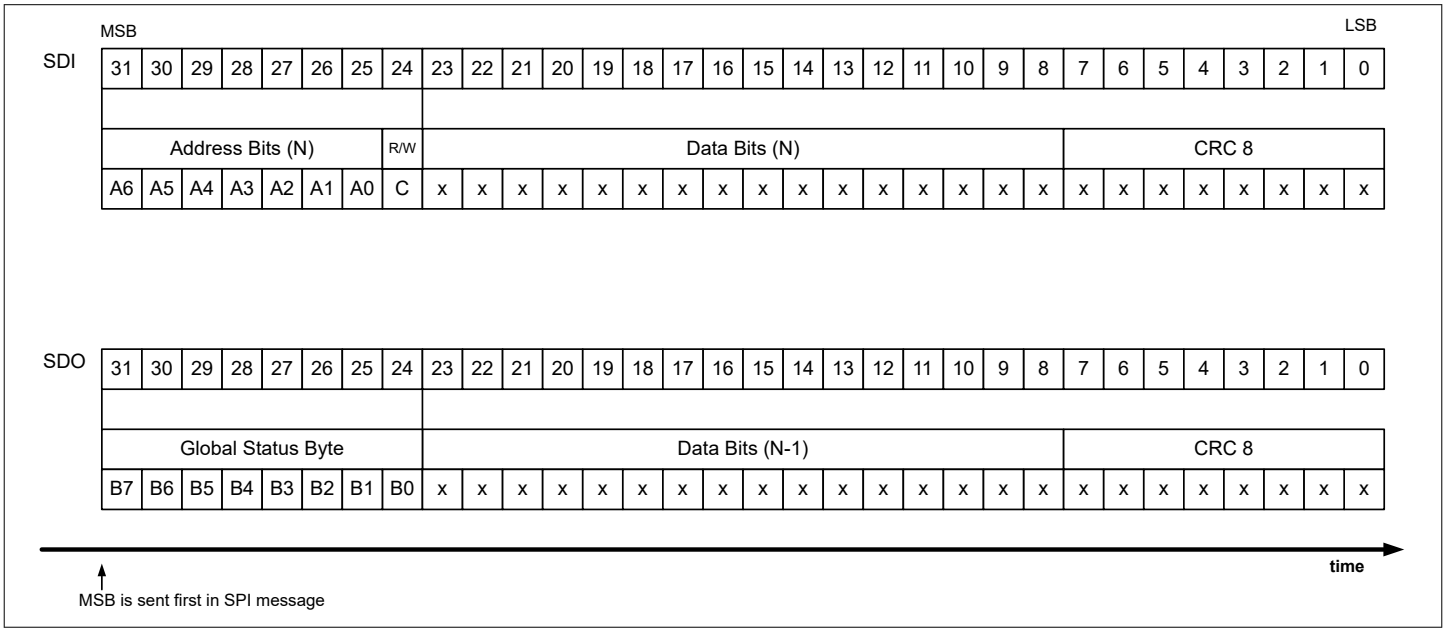

Figure 19 SPI protocol for next-frame response (NFR)

8.1.1.2 CRC8 SPI frame calculation

The CRC8 is added to any data transmitted via SDO and SDI pin at the end of the frame.

- For SDI Frame the CRC8 is calculated for the SDI 24 payload bits consisting of received 7 bit address + 1 bit C and 16 bit write data, CRC8 bits excluded.

- For SDO in-frame response the CRC8 is calculated for a 32 bit payload consisting of: dummy "0" bit + received 7 bit address (current frame) + SDO 8bit Global Status Flags + SDO 16bit read data, CRC8 bits excluded (see Figure 20).
- For SDO next-frame response the CRC8 is calculated for a 32 bit payload consisting of: dummy "0" bit + received 7 bit address (previous frame) + SDO 8bit Global Status Flags + SDO 16bit read data, CRC8 bits excluded (see Figure 21).

In case of an CRC8 error detection on the SDO line by the microcontroller, the message should be discarded and the register access should be repeated.

The 8-bit CRC calculation is performed with AutoSAR SAE J1850 polynomial calculation from AUTOSAR CRC specification shown in table below.

Table 18 CRC 8 AutoSAR SAE J1850 polynomial calculation

CRC result width	8 bits
Polynomial	$0x1D_H$
Initial value	$0xFF_H$
XOR value	$0xFF_H$
Check	$0x4B_H$
Magic check	$0xC4_H$

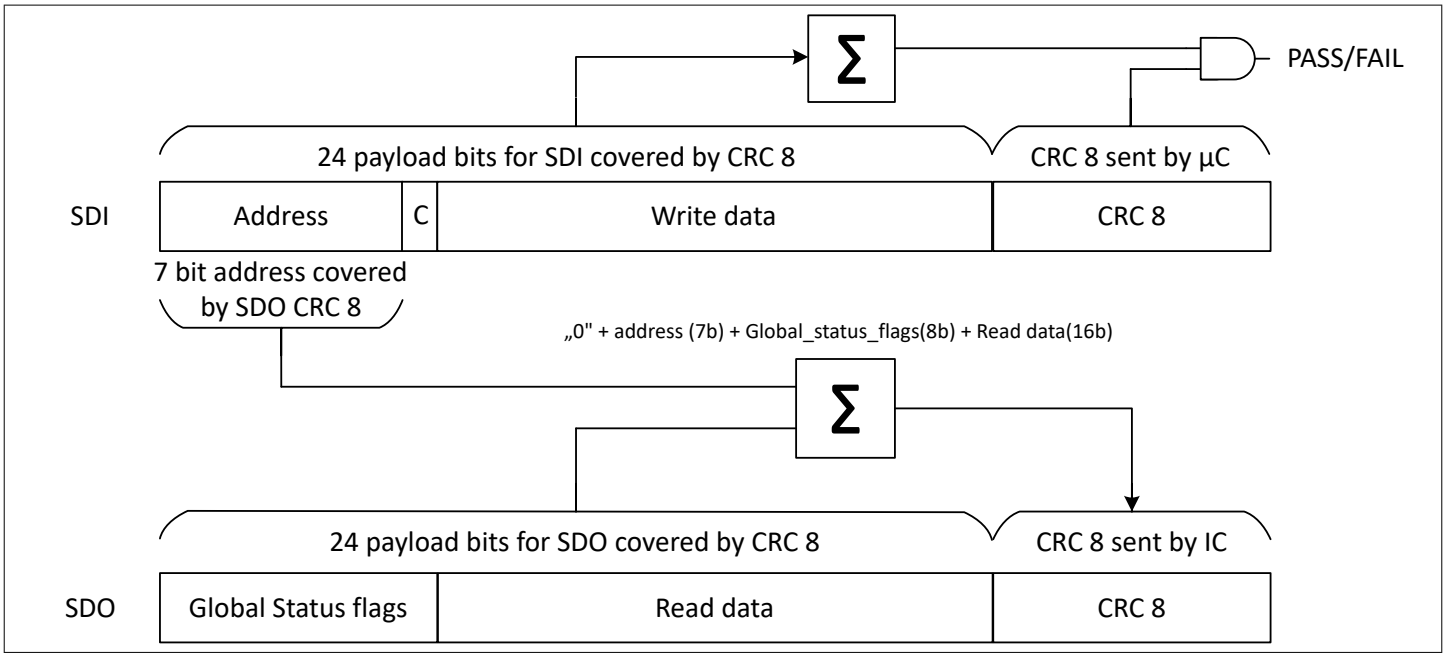

Figure 20 SPI CRC8 calculation for in-frame response (IFR)

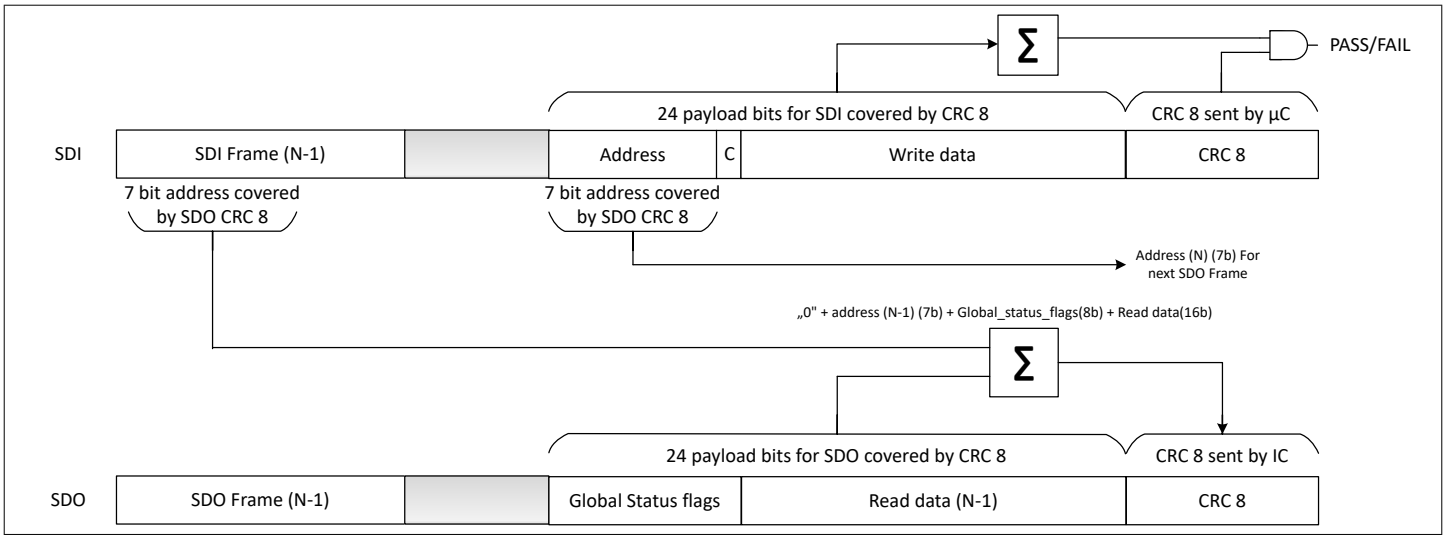

Figure 21 SPI CRC8 calculation for next-frame response (NFR)

8.1.2 Global error flag (GEF)

The global error flag (GEF) bit is reported on SDO pin between the CSN falling edge after t_{SDO_EN} and the first SCK rising edge.

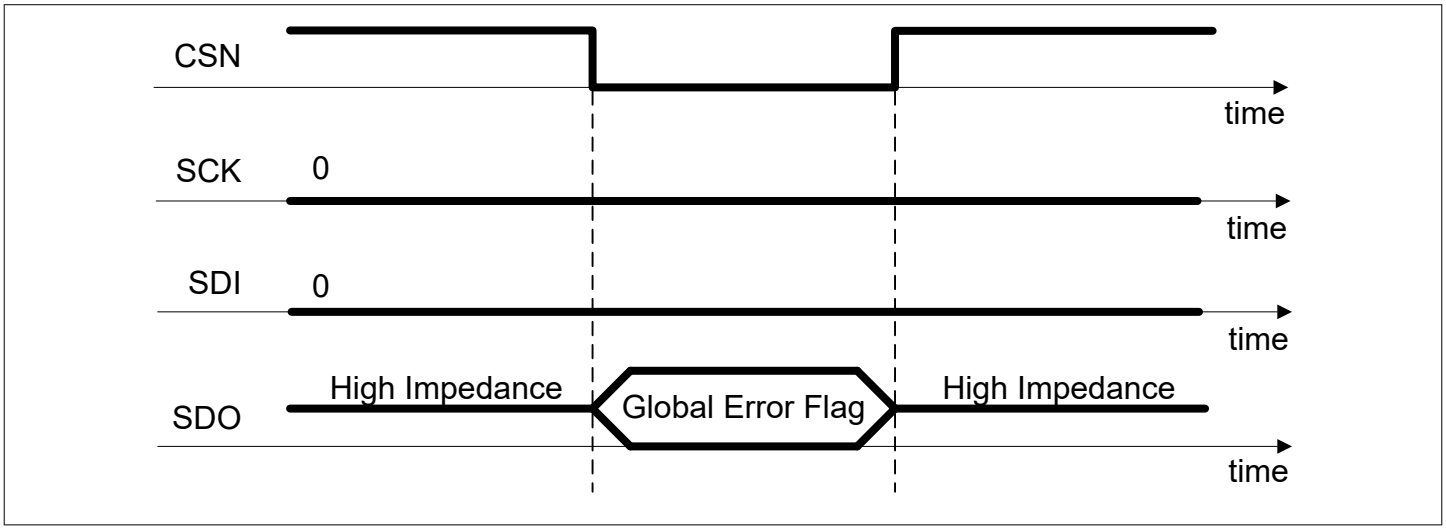

Figure 22 GEF - diagnostic with 0 - clock cycle

Global error flag indication is not configurable

***Note**: GEF status is updated continuously.*

With global error flag it is possible to have a quick diagnostic without any SPI clock pulse in case a fault condition is detected. The global error flag is a logic OR combination of following bits of the global status byte: *GEF = (OFC) OR NOT(LFOK) OR (VSUPE) OR (MISC) OR (BDRE) OR (DE) OR (POR)*

8.1.3 Global status byte

The SDO shifts out the global status register during the first eight SCK cycles to provide an overview of the device status shown list below. The global status register consists of following global status flags:

- B7 (OFC flag): at least one SPI frame corrupted
- B6 (LFOK flag): last received SDI frame correct
- B5 (VSUPE flag): supply overview status flag

- B4 (MISC flag): SPI and GPIO related status flag
- B3 (BDRE flag): Bridge driver signal path related status flag
- B2 (DE flag): device error indication using SPI register failure detection bits configured as error or latched error (LE1/LE2)
- B1 (DW flag): device warning indication using SPI register failure detection bits configured as warning (W)
- B0 (POR): power on reset indication

8.1.4 SPI error detection

The SPI incorporates an error flags LFOK and OFC in Chapter 8.1.3 to supervise and preserve the data integrity. The error flag OFC is set to "1" AND LFOK is set to "0" in the next SDO frame if following SPI errors are detected during a given frame:

- The number of SCK clock pulses received for the duration CSN = 0 is (protocol error):
  - Not zero
  - Or less than 32
  - Or more than 32
- Incorrect CRC8 detection in received SDI frame.
- The microcontroller sends an SPI command to an unused address (Chapter 8.1.4).
- A clock polarity error is detected: the incoming clock signal was high during CSN rising or falling edges (protocol error)
- Any write command to protected registers in normal mode after successful configuration of the device.
- Wrong checksum control bit received

In case an invalid address is detected within SDI frame by the device, then:

- Associated status bit is set
- The device sends data bits 0x00 in SDO frame
- The device sends CRC8 in SPI SDO frame. CRC8 is calculated according to SPI frame CRC8 integrity check including global status byte and received invalid SDI address

To ensure a correct SPI communication, the following conditions have to be fulfilled :

- SCK must be low for a minimum t_{BEF} before CSN falling edge and t_{lead} after CSN falling edge
- SCK must be low for a minimum t_{lag} before CSN rising edge and t_{BEH} after CSN rising edge

The last frame correct LFOK flag is set to "1" under the following conditions:

- A valid SDI frame has to be received by the bridge driver IC
- First SDO frame after every reset of the digital core (SPI reset command/ power-on reset)

***Notes**:*

1. *LFOK flag is automatically set to "0" by invalid SPI SDI frame and set to "1" with a valid SPI SDI frame.*

2. *The updated LFOK flag is visible in the global status byte of SDO frame for the next SPI command.*

The OFC flag can be reset in power-up mode and normal operation mode. The microcontroller must clear the associated register bit by a correct SPI write command.

8.2 Electrical characteristics (SPI)

Table 19 Electrical characteristics - SPI

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C; normal operating mode, power-up mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SPI frequency							
Maximum SPI frequency	$f_{SPI,max}$	–	–	5	MHz	*1) 2) 3)*	P_SPI_01_01
SPI interface (SDI, SCK, CSN)							
High level input voltage threshold of SPI logic input pins: SDI, SCK, CSN	V_{SPIH_IN}	0.7 x V_{VIO}	–	–	V	–	P_SPI_02_01
Low level input voltage threshold of SPI logic input pins: SDI, SCK, CSN	V_{SPIL_IN}	–	–	0.3 x V_{VIO}	V	–	P_SPI_02_02
Hysteresis of SPI logic input pins: SDI, SCK, CSN	V_{SPIHY_IN}	100	–	–	mV	–	P_SPI_02_03
Pull up resistor at pin CSN	R_{PU_CSN}	25	40	60	kΩ	V_{CSN} = 0.7 * V_{IO}	P_SPI_02_04
Pull down resistor at pin SDI, SCK	R_{PD_SDI}, R_{PD_SCK}	25	40	60	kΩ	V_{SDI}, V_{SCK} = 0.3 * V_{IO}	P_SPI_02_05
Input capacitance at pin CSN, SDI and SCK	C_I	–	–	10	pF	0 V < V_{IO} < 5.5 V	P_SPI_02_06
Serial data output SDO							
High level output voltage	V_{SDO_H}	0.8 x V_{IO}	–	–	V	I_{SDO_H} = -1.6 mA	P_SPI_03_01
Low level output voltage	V_{SDO_L}	–	–	0.2 * V_{VIO}	V	I_{SDO_L} = 1.6 mA	P_SPI_03_02
Tri-state leakage current	I_{SDO_LK}	-10	–	10	µA	V_{CSN} = V_{IO}; 0 V < V_{SDO} < V_{IO}	P_SPI_03_03
Tri-state input capacitance	C_{SDO}	–	–	20	pF	–	P_SPI_03_04
Data input timing							
SCK period	t_{pSCK}	200	–	–	ns	*1) 2) 3)*	P_SPI_04_01
SCK high time	t_{SCK_H}	70	–	–	ns	*1) 2) 3)*	P_SPI_04_02

(table continues...)

Table 19 (continued) Electrical characteristics - SPI

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C; normal operating mode, power-up mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SCK low time	t_{SCK_L}	70	–	–	ns	*1) 2) 3)*	P_SPI_04_03
SCK low before CSN low	t_{SCK_SETL}	200	–	–	ns	*1) 2) 3)*	P_SPI_04_04
SCK setup time	t_{CSN_TDEL}	200	–	–	ns	*1) 2) 3)*	P_SPI_04_05
SCK low after CSN high	t_{SCK_HDL}	200	–	–	ns	*1) 2) 3)*	P_SPI_04_06
SDI setup time	t_{SDI_SET}	30	–	–	ns	*1) 2) 3)*	P_SPI_04_07
SDI hold time	t_{SDI_HOLD}	40	–	–	ns	*1) 2) 3)*	P_SPI_04_08
CSN leading delay	t_{CSN_LDEL}	200	–	–	ns	*1) 2) 3)*	P_SPI_04_09
CSN time-out	t_{CSN_TO}	2	3	4	ms	CSN time-out enabled	P_SPI_04_10
Interframe time	t_{IF}	1	–	–	µs	*1) 2) 3)*	P_SPI_04_12
Serial data output timing							
SDO rise and fall time	$t_{SDO,r}$ $t_{SDO,f}$	–	15	25	ns	C_{Load} = 30 pF V_{SDO} from 0.2 x V_{IO} to 0.8 x V_{IO} OR V_{SDO} from 0.8 x V_{IO} to 0.2 x V_{IO}	P_SPI_05_01
SDO enable time after CSN falling edge	t_{SDO_EN}	–	–	50	ns	Delay until SDO pin shows valid GEF status	P_SPI_05_02
SDO disable time after CSN "low" to "high" transition	t_{SDO_DIS}	–	–	50	ns	*2)*	P_SPI_05_03
SDO valid time	t_{SDO_VDEL}	–	–	70	ns	*2)* delay time SCLK rising edge to V_{SDO} < 0.2 * V_{IO}, V_{SDO} > 0.8 * V_{IO} C_{load} = 30 pF	P_SPI_05_04

1) SPI command accepted after t_{core_up}
2) SPI timing parameters valid and derived from SPI frequency of 5 MHz. For lower SPI frequency min. t_{SDI_HOLD}, t_{SDI_SET}, t_{SCK_L} and t_{SCK_H} for correct SDI sampling and max. t_{SDO_VDEL} for correct microcontroller data reception are essential.
3) For calculation of minimum SPI operating frequency and maximum SPI CSN period t_{CSN_TO} has to be taken into account

9 Diagnostics

9.1 Supervision overview

The device provides extended protection and monitoring functions. All detected errors and warnings can be read by SPI, multiple thresholds and filter timings are configurable by SPI register settings. Safety relevant diagnostics can be tested during operation by dedicated self-test SPI command.

9.2 Failure reaction definition

The device has 4 different configuration possibilities for failure reaction in case of failure detection:

- Failure reaction: warning
- Failure reaction: error
- Failure reaction: latched error 1 (LE1)
- Failure reaction: latched error 2 (LE2)

The following table chose the priority of configured failure reaction of a failure detection. In case of multiple failure detections, then the failure reaction with highest priority is executed by the device.

Table 20 Failure reaction priority

Configured failure reaction	Priority
Latched error 1 (LE1) - safe state INH_N pin = "low"	1
Latched error 2 (LE2)	2
Warning (W) / error (E)	3

9.2.1 Failure reaction: warning (W)

In case a failure is detected and the failure reaction is configured as warning, then the following behavior will be executed:

- Related failure detection bit is set to "1" in associated SPI register
- Global status warning flag (DW) in global status byte is set to "1"

9.2.2 Failure reaction: error (E)

In case a failure is detected and the failure reaction is configured as error, then the following behavior will be executed:

- Related failure detection bit is set to "1" in associated SPI register
- ERR_N pin is set to "low" for the duration the failure detection bit is set to "1" in associated SPI registers but at least for t_{ERRN_EXT}
- Global status error flag (DE) in global status byte is set to "1"

9.2.3 Failure reaction: latched error (LE1 & LE2)

In case a failure is detected and the failure reaction is configured as latched error 1 (LE1), then the following behavior will be executed:

- Related failure detection bit is set to "1" in associated SPI register
- Global status error flag (DE) in global status byte is set to "1"
- ERR_N pin is set to "low"
- All output stages are actively turned off according to diagnostic switch off behavior
- Safe state is entered and safe state activation status bit is set to "1"

In case a failure is detected and the failure reaction is configured as latched error 2 (LE2), then the following behavior will be executed:

- Related failure detection bit is set to "1" in associated SPI register
- Global status error flag (DE) in global status byte is set to "1"
- ERR_N pin is set to "low"
- The affected half-bridge output stages is actively turned off according to diagnostic switch off behavior
- The affected half-bridge output stage are kept off with I_{HOLD}

9.2.4 ERR_N pin function

ERR_N pin is an open drain output pin. It can only be driven actively "low". Therefore an external pull-up resistor R_{ERR_PU} is needed.

ERR_N pin active low state indicates either the safe state entry or a configured error detection. Configured error detection when ERR_N pin is set to "low" are:

- Failure reaction: error
- Failure reaction: latched error 1 (LE1)
- Failure reaction: latched error 2 (LE2)

9.3 Reset of failure detection

In normal operation mode and power-up mode in case an error condition is detected and associated SPI status bit is set, the error condition is reset by a dedicated SPI write command to the associated SPI register sent by the microcontroller. By clear on write SPI command the microcontroller can reset selectively bits in a register. An SPI write command will clear the status bits for which the data bit position of the SPI write command is set to "1".

After correct reception of the clear on write SPI command:

- The associated bit is reset to "0"
- ERR_N pin is set to "high"

In normal operation mode in case an error is detected and the failure behavior is configured as latched error, then after a successful clear of the error via SPI command, the gate driver output stages Gxx follow the PWM input pins after t > t_{PEN_PD}.

9.4 Functional description (diagnostics)

This device provides protection and monitoring functions. All detected errors can be read-out via SPI command triggered by the microcontroller.

Shutdown errors or detected errors configured as error or latched error will be indicated at ERR_N pin as "low".

9.4.1 Overtemperature detection

The device offers two overtemperature thresholds:

- Overtemperature warning threshold T_{jW}
- Overtemperature shutdown threshold T_{jSD}

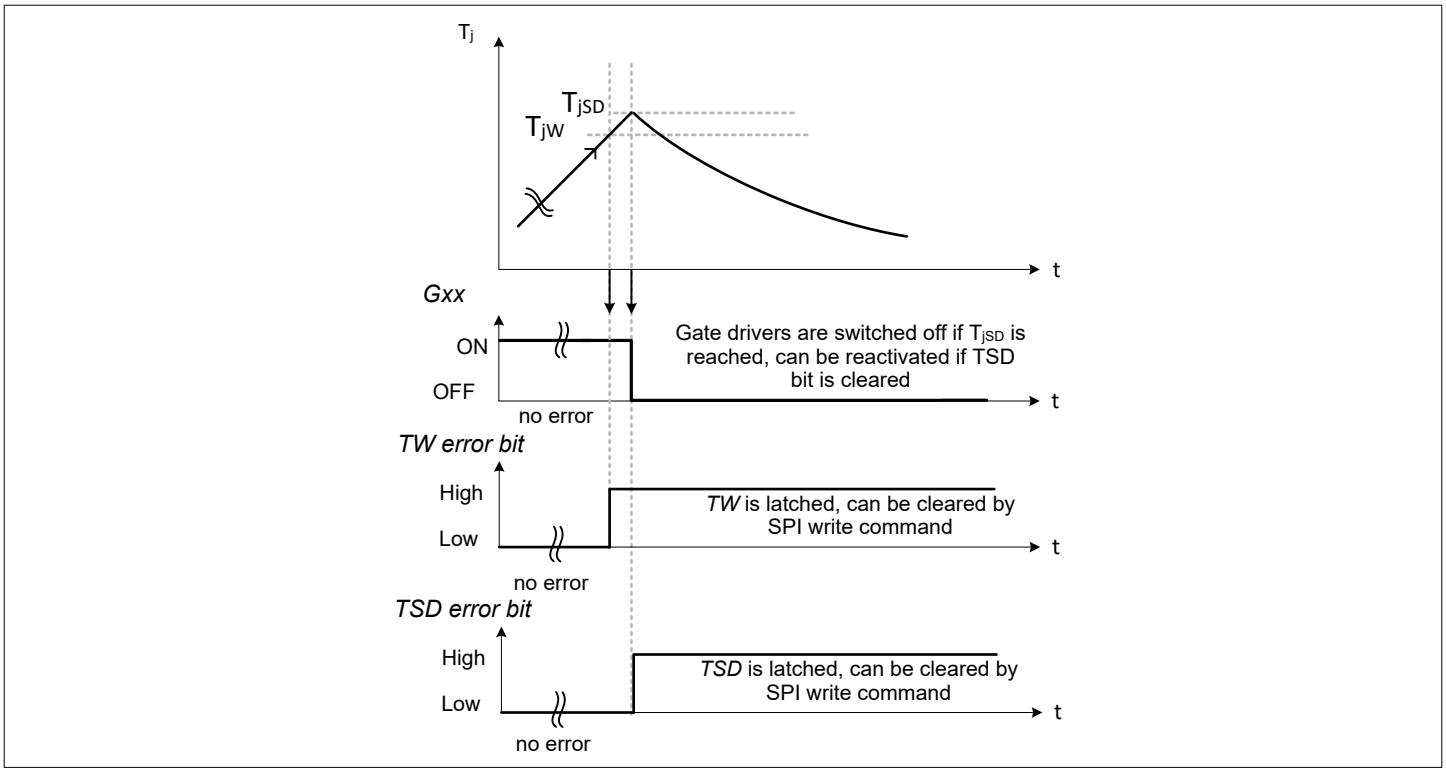

Figure 23 Overtemperature behavior

9.4.1.1 Overtemperature warning

Thermal temperature warning can be activated or deactivated by a control bit. If thermal warning is enabled AND the temperature sensor reaches T_{jW} for $t > t_{TSDf}$, then thermal warning status bit is set and related flag in global status byte is set.

In case thermal warning is activated, the failure reaction behavior is configurable:

- Setting 1: warning (default)
- Setting 2: latched error 1 (LE1)

Thermal warning temperature threshold is configurable by control bit settings:

Register setting	Parameter symbol	Overtemperature warning threshold nominal value
Setting 1	T_{jW130}	130°C
Setting 2	T_{jW140}	140°C
Setting 3	T_{jW150}	150°C
Setting 4	T_{jW160}	160°C

In order to clear the thermal warning status bit, the following conditions need to be met:

- The temperature warning condition has disappeared AND
- The microcontroller clears the thermal warning status bit by SPI write command

***Note**: In case the thermal warning is disabled, the thermal warning status bit is permanently set to "0". In case the status bit is set to "1", it will not be automatically reset by deactivation of the feature.*

9.4.1.2 Overtemperature shutdown

The device has two different temperature sensors for overtemperature shutdown:

- General IC overtemperature shutdown detection
- Charge pump overtemperature shutdown detection

In case the general temperature sensor reaches T_{jSD} for t > t_{TSDf} OR charge pump temperature sensor reaches T_{jSD_CP} for t > t_{TSDf}, the device reaches overtemperature shutdown threshold and behaves as follows:

- Failure reaction is latched error 1 (LE1). Safe state is entered
- In case of charge pump overtemperature shutdown detection bit is set to "1" AND charge pump is disabled
- In case of general IC overtemperature shutdown detection bit is set to "1" AND charge pump is disabled

9.4.2 Drain-source overvoltage monitoring

The drain-source voltage of each activated MOSFET is monitored to detect an overcurrent condition, for example caused by a short circuit of SHx to VSCP or to GND. An overcurrent for the external MOSFET results in a drain-source overvoltage, which is used for the failure detection.

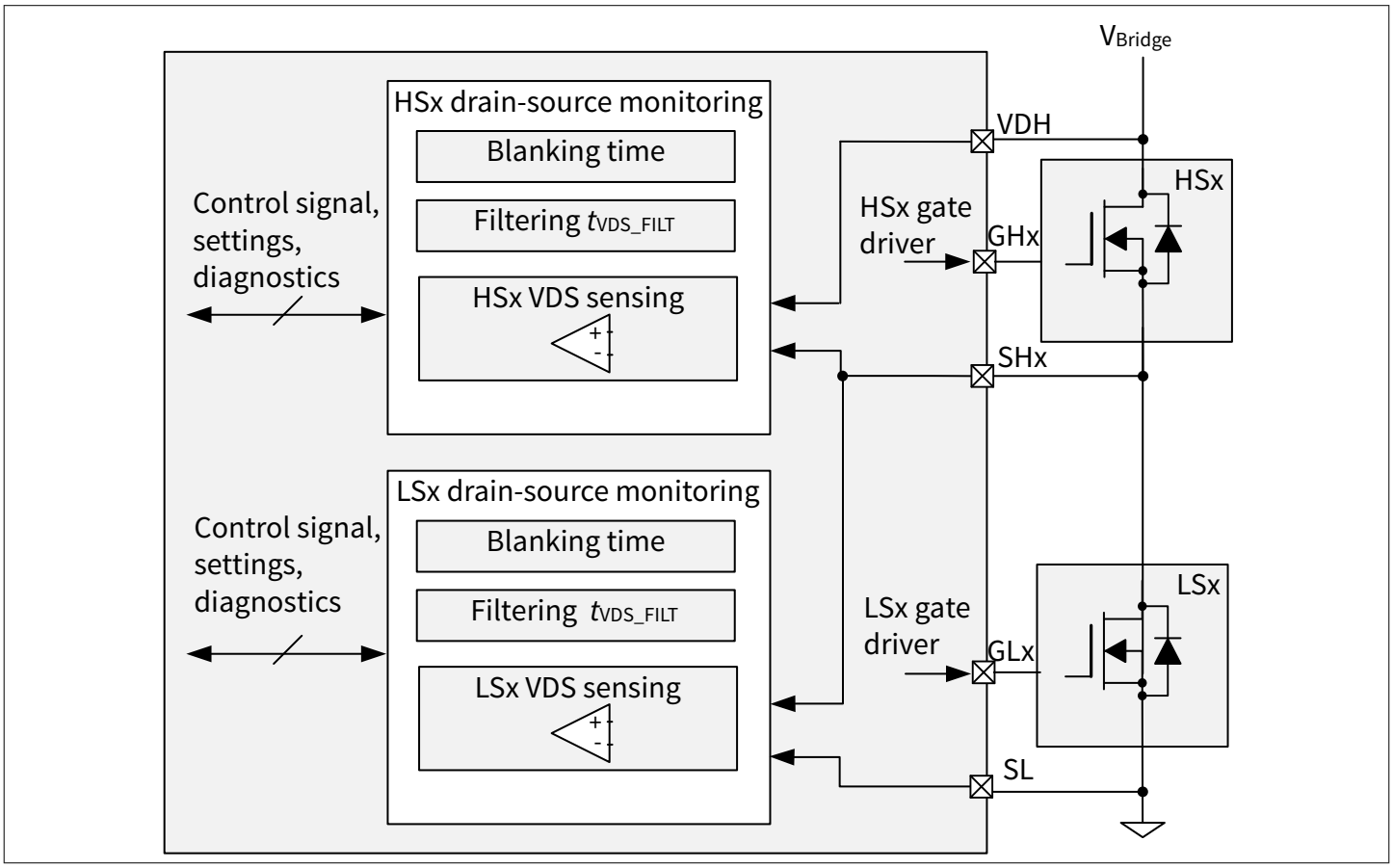

Figure 24 Block diagram: Drain-source overvoltage monitoring

For HSx: a drain-source overvoltage event is detected if HSx is on after blanking time (t_{VDS_BLK} or $t_{VDS\_BLK\_FW}$) and V_{VDH} - V_{SHx} > V_{DSOV_TH} for t > t_{VDS_FILT}.
For LSx: a drain-source overvoltage event is detected if LSx is on after blanking time (t_{VDS_BLK} or $t_{VDS\_BLK\_FW}$) and V_{SHx} - V_{SL} > V_{DSOV_TH} for t > t_{VDS_FILT}.

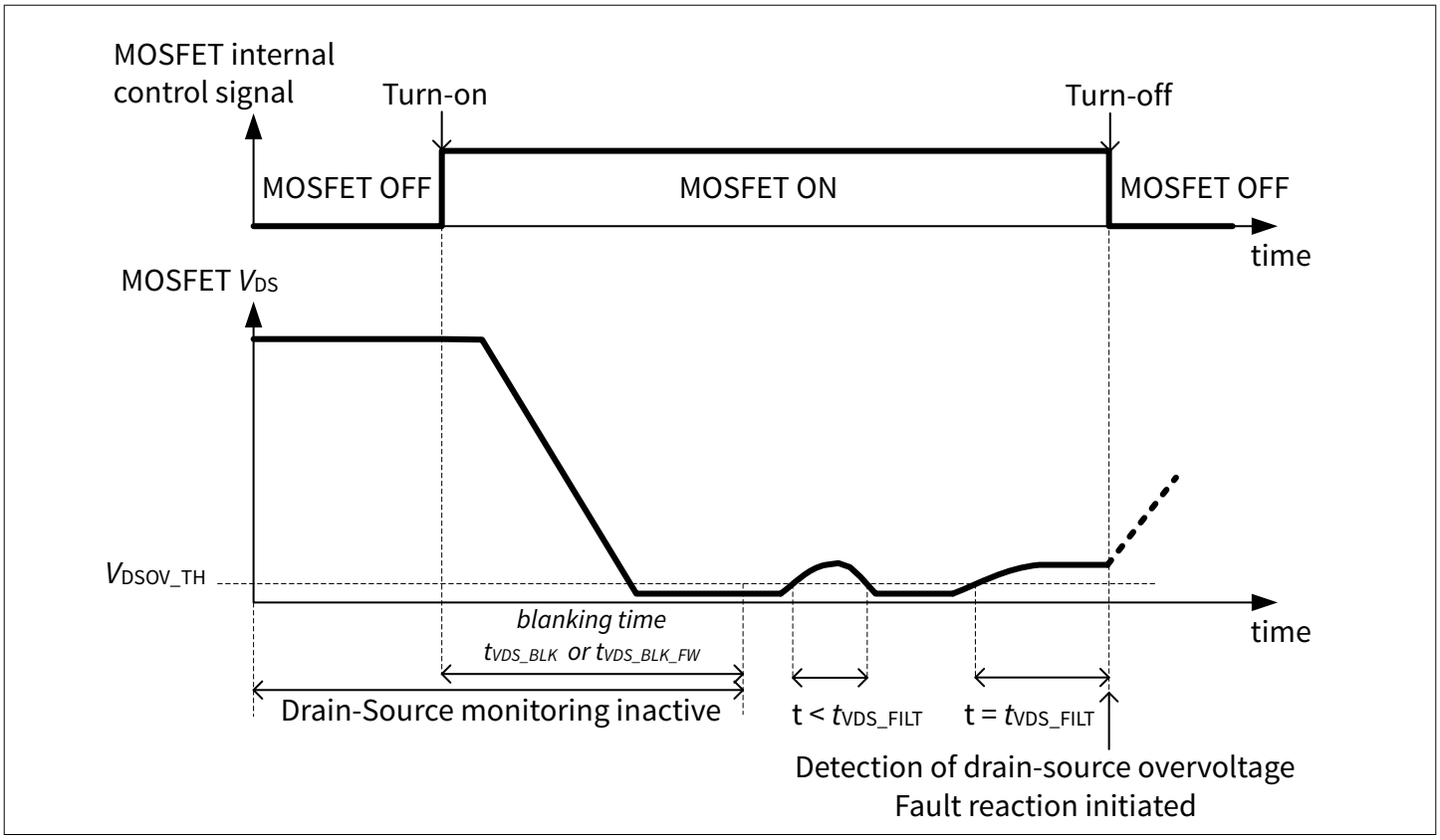

Figure 25 Drain-source overvoltage timing diagram

9.4.2.1 Drain-source blank time

A blank time t_{VDS_BLK} / $t_{VDS\_BLK\_FW}$ is applied when an output stage receives the internal control signal to turn on the external MOSFET. During t_{VDS_BLK} or $t_{VDS\_BLK\_FW}$ the drain-source monitoring of the MOSFET is deactivated.

The blank time is intended to avoid a wrong detection of a drain-source overvoltage condition during the turn-on phase of the MOSFETs.

t_{VDS_BLK} is configured by the control bits for the active MOSFET in 16 steps.

$t_{VDS\_BLK\_FW}$ is configured by the control bits for the active MOSFET in 16 steps.

Nominal drain-source overvoltage blank time for the active MOSFET is t_{VDS_BLK} = = 240 ns + 240 ns * [Register Setting]$_D$

Nominal drain-source overvoltage blank time for the FW MOSFET is $t_{VDS\_BLK\_FW}$ = = 240 ns + 240 ns * [Register Setting]$_D$

9.4.2.2 Drain-source threshold and filter time

After t_{VDS_BLK} has expired the drain-source monitoring is started. Following parameters can be configured for drain-source monitoring:

- Drain-source monitoring threshold: V_{DSOV_TH}
- Drain-source monitoring filter time: t_{VDS_FILT}

Drain-source overvoltage thresholds (V_{DSOV_TH}) is configurable for low-side and high-side output stages separately in eight steps.

Table 21 Table drain-source overvoltage threshold

Setting options	Drain - source overvoltage threshold for HSx and LSx nominal V_{DSOV_TH}
Setting 1	0.16 V

(table continues...)

Table 21 (continued) Table drain-source overvoltage threshold

Setting options	Drain - source overvoltage threshold for HSx and LSx nominal V_{DSOV_TH}
Setting 2	0.21 V (default)
Setting 3	0.25 V
Setting 4	0.3 V
Setting 5	0.35 V
Setting 6	0.4 V
Setting 7	0.5 V
Setting 8	0.6 V

Drain-source monitoring filter time t_{VDS_FILT} is configured by control bits in four steps.

Table 22 Settings of the drain-source monitoring filter time

Setting options	Nominal t_{VDS_FILT}
Setting 1	0.5 µs
Setting 2	1 µs
Setting 3	2 µs (default)
Setting 4	3 µs

9.4.2.3 Drain-source failure reaction

Failure reaction for drain-source monitoring is configurable via control bits. Following configuration possibilities are available:

- Setting 1: latched error 1 (LE1) - default
- Setting 2: latched error 2 (LE2)

If a drain-source overvoltage event is detected on one of the MOSFETs, then:

- The status bit of the affected MOSFET is set
- DE flag is set in global status byte

9.4.3 Phase feedback monitoring (PFB)

The device includes an internal phase feedback monitoring feature to check if the phase of the output stage has been driven correctly.

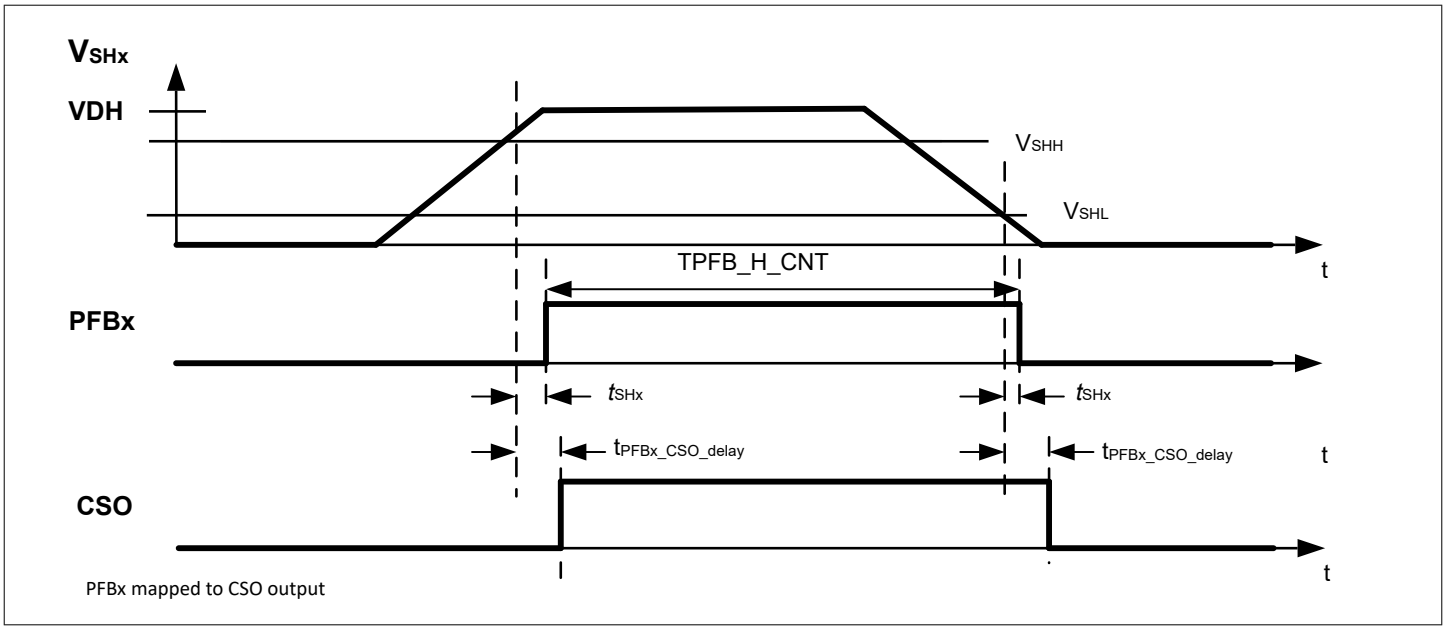

Figure 26 PFB monitoring timing diagram

Phase feedback monitoring is enabled by default and can be deactivated by a control bit.

In case PFB monitoring is enabled by the control bit, then PFB error reporting is disabled in case VDH undervoltage is detected by the device. PFB error reporting is automatically re-enabled in case VDH undervoltage event disappears.

In case an output stage is turned on, a configurable PFB monitoring blanking time extension is started after drain-source monitoring blanking time has elapsed. After the configurable PFB monitoring blanking time extension has expired the phase comparator signals are controlled if the phase has been driven towards V_{SHL} or V_{SHH}. V_{SHL} and V_{SHH} output are filtered with t_{PFB_filter}. In case the comparator feedback does not match to expected turn on output stage then a phase feedback monitoring error is detected.

Failure reaction is configurable:

- Setting 1 (default): latched error 1 (LE 1)
- Setting 2: warning

In case phase feedback monitoring error is detected, a status bit is set.

For phase feedback monitoring the device offers a configurable phase feedback monitoring blanking time extension after expiration of drain source voltage monitoring blanking time.

Phase feedback monitoring blanking time extension is configurable:

- Setting 1 (default): 2 x t_{VDS_FILT}
- Setting 2: 4 x t_{VDS_FILT}

The state of the SHx phases can be evaluated by the microcontroller at CSO pin of the device by redirecting the phase feedback (PFBx) signal to CSA output pin. PFBx state depends on the fast comparator thresholds V_{SHL} and V_{SHH}:

- PFBx is set to "0" in case $V_{SHx} < V_{SHL}$
- PFBx is set to "1" in case $V_{SHx} > V_{SHH}$
- In case $V_{SHx} > V_{SHL}$ AND $V_{SHx} < V_{SHH}$, then the previous detected state is shown at PFBx

XOR (PFBx) function changes its state with every change of one PFBx signal.

The PFBx signal redirected to CSO is the real time SHx monitoring by the fast comparator V_{SHL} and V_{SHH}.

The function of the CSO output pin configured by control bits as follows:

- Setting 1 (default): Current sense amplifier function selected
- Setting 2: PFB1 state redirected to CSO output pin
- Setting 3: PFB2 state redirected to CSO output pin
- Setting 4: Not used - CSO statically "low"
- Setting 5: XOR of PFB1, PFB2 redirected to CSO output pin

The device includes a counter to measure the PFBx "high" time. In case $V_{SHx} > V_{SHH}$, the counter starts to count until $V_{SHx} < V_{SHL}$. The value for each phase is stored in status register. The clock frequency of the counter is f_{PFB_CNT}.

9.4.4 OFF-state diagnostic

In order to support the off-state diagnostic, the gate driver of each MOSFET provides pull-up and pull-down currents at the SHx pins.

The pull-up current sources are active in case the charge pumps are active, half-bridge is enabled and OFF-state diagnostics is enabled by a SPI control bit in normal operation mode.

Following failure can be detected:

- Detection of open load conditions
- SHx shorted to VBAT
- SHx shorted to GND

The pull-down currents of each gate driver are activated by separate control bits. In case OFF-state diagnostics is enabled by the control bit, the PWM input signals are ignored.

9.4.5 Current sense amplifier monitoring (CSA)

In the following sub-chapters, the monitoring functions of the current sense amplifier module are described:

- CSA internal supply undervoltage
- CSA overcurrent detection

A simplified block diagram is shown in Figure 15. VIO pin is used as reference supply for the current sense amplifier. VIO under- and overvoltage detection is described in Chapter 9.4.6.2.

9.4.5.1 CSA internal supply monitoring

The internal supply for the current sense amplifier is monitored. In case an undervoltage is detected at CSA supply regulator then:

- CSA module is disabled
- Associated status bit for supply undervoltage is set

Failure reaction for internal CSA supply monitoring is configurable:

- Setting 1 - warning (W) (default): the device only reports the internal CSA supply undervoltage event (bit is set), without any change of the gate driver state
- Setting 2 - error (E): the device reports the internal CSA supply undervoltage event (bit is set), sets ERR_N pin "low" without any change of the gate driver state
- Setting 3 - latched error 1 (LE1): the device reports internal CSA supply undervoltage event (bit is set), sets ERR_N pin to "low" and actively turns off all MOSFETs

9.4.5.2 CSA overcurrent detection

The device includes an CSA overcurrent detection feature. For unidirectional CSA configuration an overcurrent event is detected if:

- CSO voltage is above V_{OCTH_Unidir} for $t > t_{OC\_FILT}$

For bidirectional CSA configuration an overcurrent event is detected if:

- CSO voltage is above V_{OCTH_BidirH} for $t > t_{OC\_FILT}$ OR
- CSO voltage is below V_{OCTH_BidirL} for $t > t_{OC\_FILT}$

Overcurrent filter time is configurable via control bits. The following table shows the available settings for overcurrent filter time t_{OC_FILT}:

Table 23 Overcurrent filter settings

Setting options	Overcurrent nominal filter time t_{OC_FILT}
Setting 1	3 µs
Setting 2	6 µs (default)
Setting 3	10 µs
Setting 4	50 µs

The following table shows the selection of overcurrent threshold control bits depending on the configuration of unidirectional or bidirectional CSA setting:

Table 24 Overcurrent threshold settings

CSA configuration / CSA OC threshold		Setting 1	Setting 2	Setting 3	Setting 4
unidirectional configuration		0.75 x V_{VIO}	0.8 x V_{VIO}	0.85 x V_{VIO}	0.9 x V_{VIO}
bidirectional configuration	High OC threshold	0.75 x V_{VIO}	0.8 x V_{VIO}	0.85 x V_{VIO}	0.9 x V_{VIO}
	Low OC threshold	0.25 x V_{VIO}	0.2 x V_{VIO}	0.15 x V_{VIO}	0.1 x V_{VIO}

It is possible to program the device behavior when an overcurrent condition is detected:

- Setting 1 (default) - latched error 1 (LE1): the device reports the overcurrent event (bit is set), sets ERR_N pin to "low" and actively turns off all MOSFETs with static discharge current – the MOSFETs can be reactivated by clearing the error detection
- Setting 2 - warning (W): the device only reports the overcurrent event (bit is set)
- Setting 3 - error (E): the device only reports the overcurrent event (bit is set) AND ERR_N pin is set to "low", without any change of the gate driver state
- Setting 4 - latched error 1 (LE1) with PWM auto recovery: In case the overcurrent event has disappeared, the Gxx output stages remain deactivated until a new turn-on signal on ILx / IHx_N input pin is applied.

9.4.5.3 CSA accuracy check function

The device offers a feature to check the OpAmp accuracy at CSO pin by the microcontroller. Therefore an internal generated reference voltage $V_{CSA\_GAIN\_ACC}$ is applied at the selected input pins CSIP and CSIN. This feature can be enabled in normal operation mode or power-up mode for each CSA module separately by a control bit. The differential voltage $V_{CSA\_GAIN\_ACC}$ is internally applied at selected CSIP / CSIN inputs of the selected CSA channel and multiplied with configured gain setting. After t_{CSA_SET}, the microcontroller can check CSO voltage if it is in the expected range.

9.4.6 Supply pin monitoring

The device monitors its supply pins for overvoltage and undervoltage detection. Following monitoring functions are available at external supply pins:

- VSCP supply monitoring
- VIO supply monitoring
- VCPH charge pump monitoring
- VDH undervoltage detection

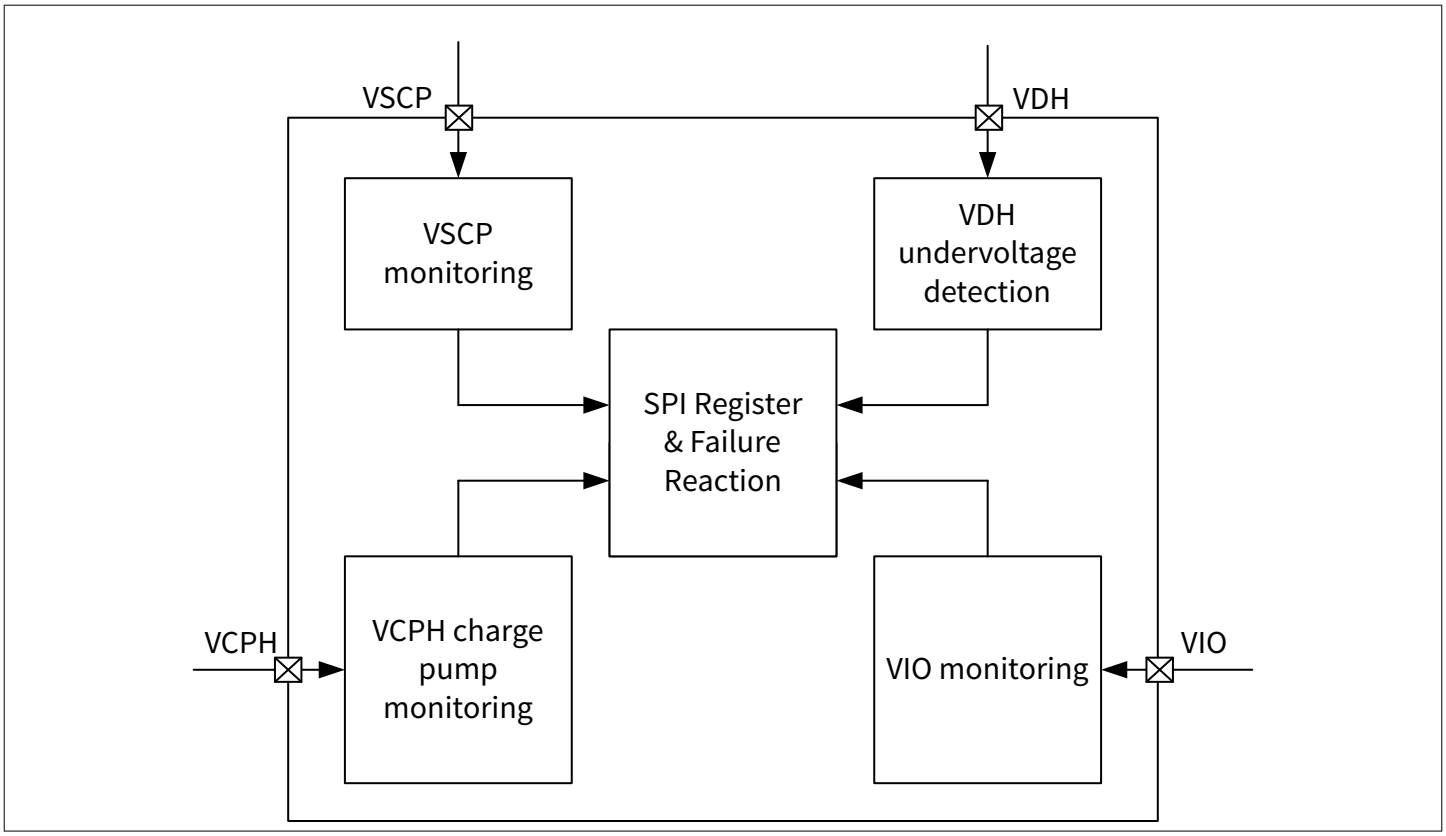

Figure 27 Supply pin monitoring block

9.4.6.1 VSCP monitoring

The device monitors the voltage at the VSCP pin:

- In case $V_{VSCP} > V_{VSCP\_OV\_SD}$ for t_{VSCP_FILT} an overvoltage shutdown is detected and associated status bit is set. The VSCP overvoltage shutdown failure behavior is fixed to latched error 1 (LE1)
- In case $V_{VSCP} < V_{VSCP\_UV\_SD}$ for t_{VSCP_FILT} an undervoltage shutdown is detected and associated status bit is set. The VSCP undervoltage shutdown failure behavior is fixed to latched error 1 (LE1)

For both VSCP overvoltage and VSCP undervoltage detection additionally the charge pump is deactivated.

9.4.6.2 VIO supply monitoring

To assure a high level of system integrity, the bridge driver provides a VIO monitoring function. The VIO voltage is monitored for under- and overvoltage.

- An undervoltage event at pin VIO is detected if the microcontroller supply $V_{VIO} < V_{VIO\_UV}$ for $t > t_{VIO\_FILT}$
- An overvoltage event at pin VIO is detected if the microcontroller supply $V_{VIO} > V_{VIO\_OV}$ for $t > t_{VIO\_FILT}$

VIO undervoltage and overvoltage detection is configurable.

Table 25 VIO threshold configuration

VIO supply monitoring setting	Nominal VIO undervoltage detection threshold	Nominal VIO overvoltage detection threshold
Setting 1: (default) V_{IO} supply functional range monitoring	2.94 V	5.6 V
Setting 2: 3.3 V supply	2.94 V	3.73 V
Setting 3: 5 V supply	4.4 V	5.6 V

(table continues...)

Table 25 (continued) VIO threshold configuration

VIO supply monitoring setting	Nominal VIO undervoltage detection threshold	Nominal VIO overvoltage detection threshold
Setting 4: V_{IO} supply functional range monitoring	2.94 V	5.6 V

VIO undervoltage and overvoltage failure reaction is not configurable and fixed as latched error 1 (LE1).

In normal operation mode and power-up mode as long as VIO under- or overvoltage is present then:

- Associated error detection bit for VIO under- or overvoltage is set
- SDO pin is set to tri-state
- LE1 failure reaction is triggered

In case of VIO undervoltage detection additionally all logic input pins are blocked.

The behavior of the CSA module during VIO undervoltage event is configurable. Following options are available:

- Setting 1 (default) : CSA module is disabled in case of a VIO undervoltage event and remains disabled as long as VIO undervoltage status bit is not cleared. Once the corresponding status bit is cleared, the CSA recovers functionality as configured.
- Setting 2: CSA module is disabled in case of a VIO undervoltage event and automatically restarts when the VIO undervoltage event is not present anymore, independent of the corresponding status bit.

9.4.6.3 VCPH charge pump monitoring

To assure enough supply voltage to drive the output stages, the bridge driver provides a VCPH pin undervoltage monitoring function. The differential voltage between pin VCPH and VSCP is monitored for undervoltage. An undervoltage event at pin VCPH is detected in case $V_{VCPH} - V_{VSCP} < V_{VCPH\_UV}$ for $t > t_{VCPH\_UV}$.

The charge pump undervoltage detection threshold is configurable:

Table 26 VCPH undervoltage monitoring configuration

Parameter	Symbol	Nominal value	Unit	Default	Tolerance	Note
VCPH undervoltage threshold	V_{VCPH_UV}	7.5 8.5	V	8.5 V	$V_{VCPH\_UV\_ACC}$	

Failure reaction of VCPH pin undervoltage detection is fixed to latched error 1 (LE1).

9.4.6.4 VDH undervoltage detection

The device includes a VDH undervoltage detection feature. The VDH undervoltage detection is enabled in power-up mode and normal-operation mode.

A VDH undervoltage event is detected if the voltage at pin VDH is $V_{VDH} < V_{VDH\_UV}$ for for $t > t_{VDH\_FILT}$.

Failure reaction of VDH undervoltage detection is fixed to warning (W).

9.4.7 Internal IC supervision function

9.4.7.1 Internal clock monitoring

The internal clock frequency of the IC is monitored. Failure behavior is not configurable and set as latched error 1 (LE1).

Additionally an internal power-on reset is triggered. In case the internal clock recovers to normal operation, the device recovers in power-up mode with all SPI register values to default values.

9.4.7.2 Internal digital core supply monitoring

The device includes monitoring function for the internal power supply - VREG.

Internal VREG is required for the internal digital core.

In case an undervoltage is detected at VREG then:

- power-on-reset occurs
- device reinitializes the power-up sequence
- after t_{core_up} SPI commands are accepted while VIO within functional range
- all registers are reset to default values
- device is in power-up mode, internally forced safe state

9.4.8 Window watchdog

An integrated window watchdog supervises the integrity of the communication with microcontroller.

The watchdog period t_{WDPER} is configurable by control bits in the range from 2 ms to 256 ms. Window watchdog ratio is fixed to 40% open window period and 60% locked window period.

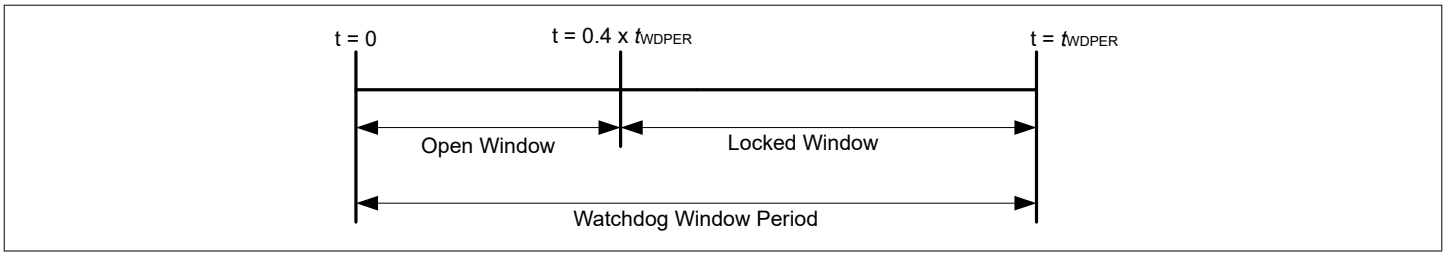

Figure 28 Window watchdog timing

After a power-on reset, in power-up mode by default the window watchdog is disabled. The micrcoontroller can enable the feature by a SPI write command.

In case the window watchdog function is enabled the window watchdog failure reaction is configurable:

- Setting 1 - (default) latched error 1 (LE1). DE flag is set in case error counter reaches the configured error counter value. In case latched error is detected, additionally all half-bridges are disabled
- Setting 2 - error (E): DE flag and corresponding status bit is set in case error counter reaches the configured error counter value

9.4.8.1 Window watchdog configuration

The window watchdog period starts with an open window first. During open window the window watchdog can be serviced. A correct SPI SDI frame write command to the window watchdog configuration register is a successful servicing of the window watchdog.

Window watchdog period and watchdog failure counter is configurable via SPI by the microcontroller in power-up mode and normal operation mode.

The window watchdog clock counter counts the internal clock cycles between two consecutive correct SPI window watchdog serving commands. The window watchdog error counter counts failed or missed window watchdog serving commands.

The result of the error counter and the clock counter is stored in SPI registers.

In case of correct window watchdog servicing, then:

- Internal clock counter will be stored in associated register
- Internal clock counter is restarted
- Error counter is decremented by 1
- Locked window is started

A check sum bit is part of the SPI command to trigger the watchdog and to set the watchdog setting. The sum of the data bits in the window watchdog configuration register requires even parity. This is realized by either setting a control bit to "0" or "1". If the check sum is wrong, then the SPI command is ignored, i.e. the watchdog is not triggered or the settings are not changed and SPI error is signalized.

In case window watchdog servicing fails, by servicing within locked window watchdog period OR a wrong SPI command OR no SPI write command to window watchdog configuration has been sent during open window watchdog period, then:

- The window watchdog is restarted with an open window
- The error counter is incremented by 2
- The clock counter will continue counting until correct window watchdog servicing is performed. Maximum value for window watchdog clock counter is written into the associated register

As soon as the first window watchdog service fails a status bit is set to "1". If the error counter reaches the configured watchdog failure counter, then the configured failure behavior executed and an additional watchdog latched status bit is set. Additionally any incorrect window watchdog servicing will set the global status device warning (DW) flag. Any correct window watchdog servicing will reset the global status device warning (DW) flag, unless WDLE status bit is set

Table 27 Configuration possibilities for window watchdog

Bit fields in window watchdog configuration register	Description
Window watchdog period	Setting 1: 2 ms Setting 2: 4 ms Setting 3: 8 ms Setting 4: 16 ms Setting 5: 32 ms Setting 6: 64 ms (default) Setting 7: 128 ms Setting 8: 256 ms
Window watchdog failure counter value	Setting 1: 2 Setting 2: 4 Setting 3: 6 Setting 4: 8 (default) Setting 5: 10 Setting 6: 12 Setting 7: 14 Setting 8: 15

The Window watchdog clock counter counts the internal clock cycles between two consecutive correct SPI window watchdog serving commands.

For every valid window watchdog servicing command the window watchdog clock counter result is stored in a register. The result is stored until the next valid window watchdog servicing.

The window watchdog clock counter is restarted if:

- A correct window watchdog servicing is triggered OR
- Watchdog latched error status bit is cleared by SPI command

9.4.9 PWM input pin monitoring

In bridge applications it has to be assured that the external complementary high-side and low-side MOSFETs are not turned “on” at the same time, connecting directly the battery voltage to GND. Therefore the bridge driver includes various PWM input pin features:

- Shoot-through protection
- Cross current protection
- Input pattern violation reporting

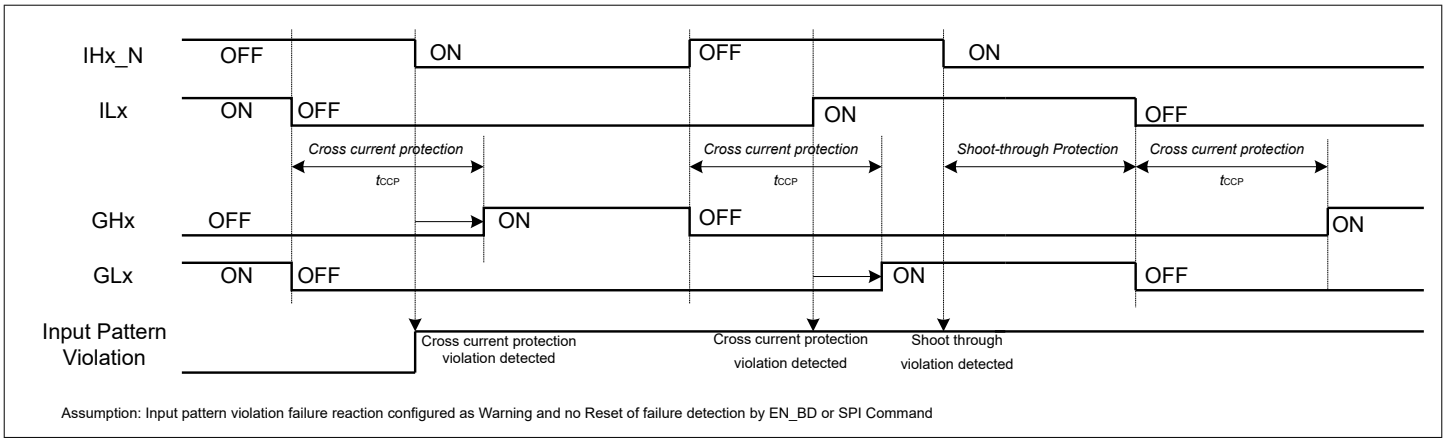

Figure 29 PWM input pin monitoring

9.4.9.1 Shoot-through protection

Shoot-through protection is active in normal operation mode for configured activated half-bridges.

The implemented locking mechanism (shoot through protection) avoids two complementary output stages Gxx of a half-bridge to be turned on at the same time. In case one output stages is turned on, any turn-on signal (including glitches) of the complementary output stage is blocked. Hence a short circuit of the bridge due to faulty input signals or faulty input driving sequences cannot occur.

A violation of the shoot-through protection is detected if:

1) IHx_N is set to "low" for t > t_{STP_filt}, while ILx is already "high". A status bit for the affected half-bridge is set.

2) ILx is set to "high" for t > t_{STP_filt}, while IHx_N is already "low". A status bit for the affected half-bridge is set.

Failure reaction for shoot through protection is configurable:

- Setting 1 (default): latched error 1 (LE1)
- Setting 2: warning

***Note**: In case the half-bridge is deactivated, shoot-through protection is disabled and no error is detected.*

9.4.9.2 Cross current protection

The bridge driver protects the external MOSFETs of each half-bridge against cross-conduction. The cross current protection time defines the time frame between one MOSFET is turned off and the complementary MOSFET of the half bridge is turned on.

The cross current protection time is configurable for active MOSFET (t_{CCP}) and freewheeling MOSFET (t_{CCP_FW}) separately.

If IHx_N is set to "low" OR ILx is set to "high" in the duration of the other input's TCCP, to avoid the cross current the device will switch on the corresponding MOSFET with a delay defined by cross-current protection time.

***Note**: The cross-conduction protection of the bridge driver is only able to increase the effective dead time between the complementary control signals of one half-bridge (LSx ON, HSx ON) to the selected cross-conduction protection time. If the dead time of the programmed control signals at IHx_N and ILx is already longer than the configured cross-conduction protection time this feature has no effect.*

Nominal cross-current protection time for active and free wheeling output stage is defined as:

- t_{CCP_FW} = 240 ns + 240 ns * [Register Setting]$_D$
- t_{CCP} = 240 ns + 240 ns * [Register Setting]$_D$

The device offers the possibility to reduce the configured TCCP, TCCP_FW and $t_{OFF\_timeout}$ value by factor 2 by a dedicated control bit.

9.4.9.3 Input pattern violation

A monitoring of the PWM input pins IHx_N & ILx has been integrated to check if the output pattern of the microcontroller violates the cross current protection time of the bridge driver IC. Therefore the synchronized IHx_N and ILx signals are compared and checked against the configured cross current protection time.

In case input pattern violation feature is enabled, a status bit for each half-bridge indicates if the affected input pin ILx OR IHx_N violates the configured cross current protection time.

Input pattern violation monitoring feature can be disabled via SPI configuration:

- Setting 1: enabled (default)
- Setting 2: disabled

Failure behavior is configurable:

- Setting 1: Latched error 1 (LE1) - default
- Setting 2: Warning (W)

9.4.9.4 PWM alternation monitoring

The device includes a PWM alternation monitoring. While the corresponding half-bridge enabled, the device monitors if PWM turn ON request is periodically alternating between HS and LS gate drivers of the same half-bridge. In case of failure detection a status bit is set and configured failure reaction is triggered. Turn ON request is detected by device at PWM input pins (ILx/IHx_N) for pulses $t > t_{SYNC}$.

A PWM alternation monitoring failure is detected in case one PWM input pin of a half bridge receives four consecutive turn ON requests, while on the complementary input pin no turn ON request has been detected.

The PWM alternation monitoring feature is by default deactivated and can be enabled by a control bit. Failure behavior is configurable:

- Setting 1: error (default)
- Setting 2: warning

9.4.10 ERR_N pin stuck "high" detection

The digital output pin SDO is protected against short to GND or VIO supply. The error indication pin ERR_N is protected against short to VIO supply. Furthermore a stuck "high" detection is implemented for ERR_N pin.

The ERR_N stuck "high" detection can detect a short circuit condition to supply:

In case ERR_N pin is detected as stuck "high", then:

- ERR_N output pad is disabled
- Status bit is set accordingly
- Configured failure reaction is executed

***Note**: In order to detect a ERR_N stuck condition, the device has to pull ERR_N pin to "low".*

ERR_N stuck "high" detection is enabled by default. Failure reaction is configurable:

- Setting 1 (default): latched error 1 (LE 1)
- Setting 2: warning (W)

ERR_N pin stuck "high" detection is only active in case ERR_N output stage is driven actively "low". A failure ERR_N stuck "high" is detected in case $V_{ERR\_N} > V_{ERRN\_H}$.

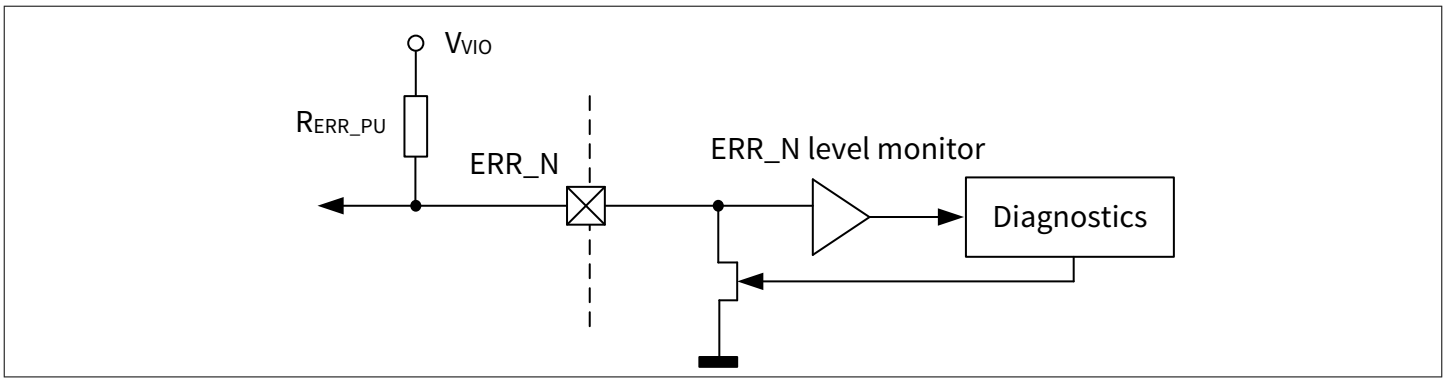

Figure 30 Block diagram: ERR_N pin stuck "high" detection

9.5 Electrical characteristics (diagnostics)

Table 28 Electrical characteristics - diagnostics

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C; normal operating mode, power-up mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Fault reaction and ERR_N pin							
ERR_N output voltage active low	V_{ERRN_LL}	–	0.6	1.0	V	I_{ERR_N} = 4.0 mA	P_DIAG_01_01
ERR_N fault extension time	t_{ERRN_EXT}	10	20	50	µs	–	P_DIAG_01_02
Propagation time enable driver output stages after passive discharge phase	t_{PEN_PD}	5	10	12.5	µs	Valid after any transition from output stage in passive discharge phase to at least one gate driver in active phase	P_DIAG_01_03
Fault reaction time	t_{FRT}	20	–	200	ns	$C_{ERR\_N\_load}$ < 100pF; ERR_N pulled up to VIO	P_DIAG_01_04
Overtemperature detection							
Thermal warning junction temperature threshold accuracy	T_{jW_ACC}	-10	–	+10	°C	Refer to Table 21 for nominal T_{jW}	P_DIAG_02_01
Thermal shutdown junction temperature: IC	T_{jSD}	175	185	195	°C	rising edge	P_DIAG_02_02
Thermal warning and thermal shutdown hysteresis	T_{jHYS}	5	10	15	°C	applicable for T_{jSD} and T_{jSD_CP}	P_DIAG_02_03

(table continues...)

Table 28 (continued) Electrical characteristics - diagnostics

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C; normal operating mode, power-up mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal warning and thermal shutdown filter time	t_{TSDf}	5	10	15	µs	–	P_DIAG_02_04
Thermal shutdown junction temperature: charge pump	T_{jSD_CP}	185	195	205	°C	rising edge	P_DIAG_02_05
Drain-Source monitoring threshold							
Drain-source monitoring blank time accuracy	$t_{VDS\_BLK\_ACC}$	- 15	–	+ 15	%	Refer to Chapter 9.4.2.1 for nominal t_{VDS_BLK}	P_DIAG_03_01
Drain-source monitoring filter time accuracy	$t_{VDS\_FILT\_ACC}$	- 15	–	+ 15	%	Refer to Table 22 for nominal t_{VDS_FILT}	P_DIAG_03_02
Drain source overvoltage threshold accuracy	$V_{DSOV\_TH\_ACC}$	- 20	–	+ 20	%	Refer to Table 21 for the nominal value V_{DSOV_TH} setting 1-2	P_DIAG_03_03
Drain source overvoltage threshold accuracy	$V_{DSOV\_TH\_ACC}$	- 15	–	+ 15	%	Refer to Table 21 for the nominal value V_{DSOV_TH} setting 3-4	P_DIAG_03_04
Drain source overvoltage threshold accuracy	$V_{DSOV\_TH\_ACC}$	- 10	–	+ 10	%	Refer to Table 21 for the nominal value V_{DSOV_TH} setting 5-8	P_DIAG_03_05
Off state diagnostics							
Pull-down diagnosis current	I_{PDDiag}	2.5	3.5	15.0	mA	$V_{SHx} > V_{SL}$ + 2 V,	P_DIAG_05_01
Pull-up diagnosis current	I_{PUDiag}	-0.8	-0.4	-0.3	mA	$V_{SHx} < V_{VSCP}$	P_DIAG_05_02
Pull-down Pull-up diagnosis current ratio	I_{PDDiag}/I_{PUDiag}	2.7	–	–	–	–	P_DIAG_05_03

(table continues...)

Table 28 (continued) Electrical characteristics - diagnostics

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C; normal operating mode, power-up mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current sense amplifier monitoring							
Overcurrent thresholds unidirectional	V_{OCTH1_Unidir} V_{OCTH2_Unidir} V_{OCTH3_Unidir} V_{OCTH4_Unidir}	-2.5%	0.75 x V_{VIO} 0.80 x V_{VIO} 0.85 x V_{VIO} 0.90 x V_{VIO}	+2.5%	–	CSA OC setting configurable via SPI Unidirectional CSA configuration	P_DIAG_06_01
High overcurrent thresholds bidirectional	V_{OCTH1_BidirH} V_{OCTH2_BidirH} V_{OCTH3_BidirH} V_{OCTH4_BidirH}	-2.5%	0.75 x V_{VIO} 0.80 x V_{VIO} 0.85 x V_{VIO} 0.90 x V_{VIO}	+2.5%	–	CSA OC setting configurable via SPI Bidirectional CSA configuration	P_DIAG_06_02
Low overcurrent thresholds bidirectional	V_{OCTH1_BidirL} V_{OCTH2_BidirL} V_{OCTH3_BidirL} V_{OCTH4_BidirL}	-4%	0.25 x V_{VIO} 0.20 x V_{VIO} 0.15 x V_{VIO} 0.10 x V_{VIO}	+4%	–	CSA OC setting configurable via SPI Bidirectional CSA configuration	P_DIAG_06_03
Overcurrent filter time accuracy	$t_{OC\_FILT\_ACC}$	- 20	–	+ 20	%	Refer to Chapter 9.4.5.2 for nominal t_{fOC} *1)*	P_DIAG_06_04
CSA gain accuracy test differential voltage	$V_{CSA\_GAIN\_ACC}$	28	32	36	mV	–	P_DIAG_06_05
Supply monitoring							
VIO monitoring threshold accuracy	$V_{VIO\_MON\_ACC}$	-4	–	+4	%	Refer to Table 25 for nominal V_{VIO_UV} and V_{VIO_OV} threshold	P_DIAG_07_01
VIO undervoltage monitoring hysteresis	$V_{VIO\_UV\_HYS}$	20	50	85	mV	–	P_DIAG_07_02

(table continues...)

Table 28 (continued) Electrical characteristics - diagnostics

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C; normal operating mode, power-up mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
VIO overvoltage monitoring hysteresis	$V_{VIO\_OV\_HYS}$	70	100	220	mV	–	P_DIAG_07_03
VIO monitoring filter time	t_{VIO_FILT}	20	25	30	µs	–	P_DIAG_07_04
VSCP undervoltage threshold	V_{VSCP_UV}	4	4.25	4.5	V	–	P_DIAG_07_05
VSCP undervoltage hysteresis	$V_{VSCP\_UV\_HYS}$	50	150	400	mV	–	P_DIAG_07_06
VSCP overvoltage shutdown threshold	$V_{VSCP\_OV\_SD}$	31.5	33.25	35	V	–	P_DIAG_07_07
VSCP overvoltage shutdown hysteresis	$V_{VSCP\_OV\_SD\_HYS}$	350	500	900	mV	–	P_DIAG_07_08
VSCP shutdown filter time	t_{VSCP_FILT}	20	30	40	µs	–	P_DIAG_07_09
VCPH undervoltage threshold accuracy	$V_{VCPH\_UV\_ACC}$	-0.5	–	0.5	V	Refers to the nominal values of the programmable parameter V_{VCPH_UV} see Table 26	P_DIAG_07_10
VCPH undervoltage filter time	t_{VCPH_SD}	50	60	70	µs	–	P_DIAG_07_11
VDH undervoltage detection threshold	V_{VDH_UV}	-10%	5.0	+10%	V	falling edge PFB monitoring deactivated below V_{VDH_UV}	P_DIAG_07_12
VDH undervoltage detection hysteresis	$V_{VDH\_UV\_HY}$	0.2	0.4	0.6	V	–	P_DIAG_07_13
VDH undervoltage detection filter time	t_{VDH_FILT}	8	10	12	µs	–	P_DIAG_07_14
Phase feedback monitoring							
PFBx to CSO delay	$t_{PFBx\_CSO\_delay}$	–	125	150	ns	PFBx mapped to CSO pin	P_DIAG_08_01
PFB counter frequency	f_{PFB_CNT}	3.45	3.75	4.05	MHz	Derived by internal clock frequency	P_DIAG_08_02

(table continues...)

Table 28 (continued) Electrical characteristics - diagnostics

V_{IO} = 3.0 V to 5.5 V, V_{VSCP} = 8 V to 29 V, T_J = -40°C to +175°C; normal operating mode, power-up mode; all voltages with respect to ground; positive current defined flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
PFB output filter	t_{PFB_filter}	420	600	780	ns	–	P_DIAG_08_03
Internal IC supervision							
Internal clock frequency	f_{CLKint}	–	75	–	MHz	–	P_DIAG_09_01
Internal clock frequency accuracy	f_{CLKint_ACC}	-7.5	–	+7.5	%	related to f_{CLKint}	P_DIAG_09_02
Watchdog							
Watchdog period accuracy	t_{WDPER_ACC}	-15	–	+15	%	Refer to Table 27 for nominal watchdog period	P_DIAG_10_01
PWM monitoring							
Cross current protection time of active output stage	t_{CCP}	-15%	-	+15%	µs	t_{CCP} = 250 ns + 250 ns x register setting	P_DIAG_11_01
Cross current protection time of freewheeling output stage	t_{CCP_FW}	-15%	-	+15%	µs	t_{CCP_FW} = 250 ns + 250 ns x register setting	P_DIAG_11_02
Shoot through protection detection time	t_{STP_filt}	400	500	600	ns	–	P_DIAG_11_03
Output pin failure							
ERR_N stuck detection threshold	V_{ERRN_H}	–	–	1.0	V	–	P_DIAG_12_03
Self-test							
Self-test timeout	$t_{ST\_timeout}$	64	80	96	µs	After valid SPI command reception to execute self-test	P_DIAG_13_01

1) t_{FOC} refers to the output of the current sense amplifier. The settling time t_{SET} and the analog propagation delay are not taken into account by the overcurrent filter time.

10 Safe state

The safe state of the device is defined as turn OFF and keep OFF at least three Gxx-Sxx output stage pairs

Safe state is defined as:

- The product turns off and keeps off three Gxx-Sxx pin pairs in all specified operation modes. (Disable gate driver, Gxx-Sxx passive clamping enabled AND Gxx-GND passive discharge enabled)

In case safe state is entered in normal-operation mode or power-up mode due to an error detection configured as latched error 1 (LE1), then following functions are available:

- SPI communication is available as long as $V_{VIO\_OV} > V_{VIO} > V_{VIO\_UV}$ AND no internal VREG regulator undervoltage condition
- ERR_N is set to "low"
- Status bit for Safe state activation is set
- In case of failure detection the dedicated status bit of each of the detected failures is set
- Global status flag is set accordingly (OR function of all relevant internal detected failures)
- Passive discharge Gxx to GND enabled

Following events trigger safe state entry:

- INH_N set to "low" in normal operation
- Failure detected configured as latched error 1 (LE1)
- SPI command to enter safe state
- Internal IC supervision error detection
- Sleep mode
- Power-up mode
- $V_{VIO} < V_{VIO\_PORf}$ (digital core of device unsupplied)

11 Application information

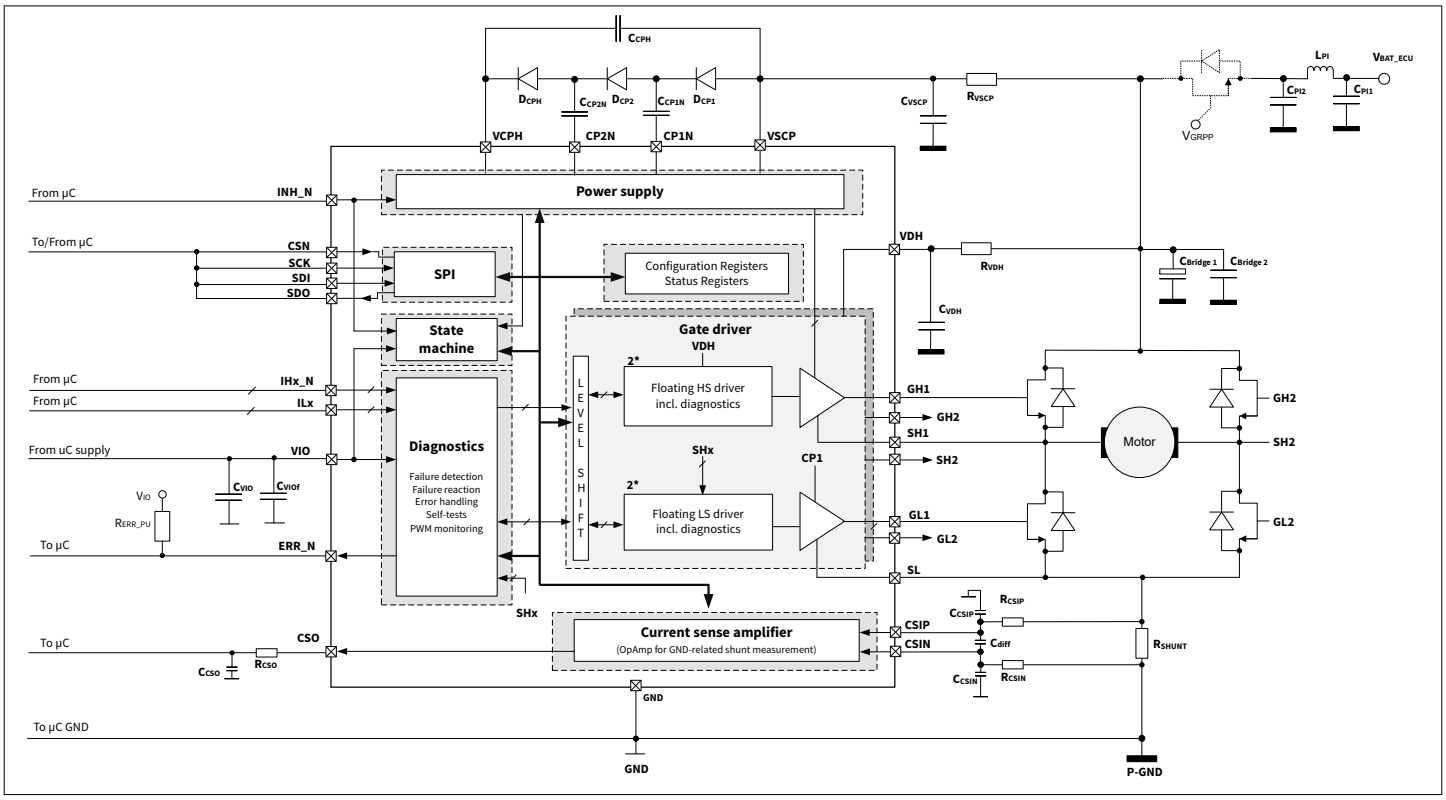

Figure 31 Simplified application example

12 Package

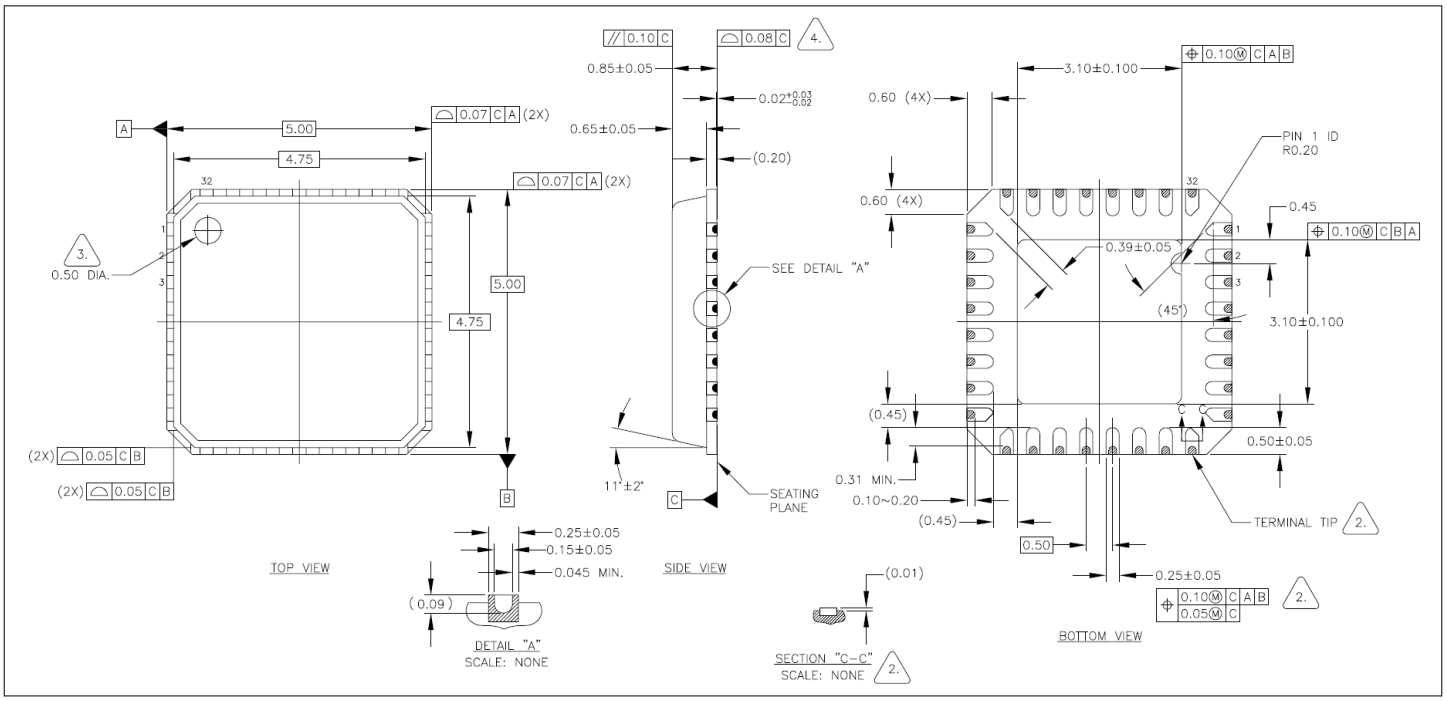

Figure 32 Package outline drawing

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations, the device is available as a green product. Green products are RoHS-compliant (that is, Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Revision History

Table 29 Revision History

Revision number	Date of release	Description of changes
1.00	2025-12-05	Datasheet available

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