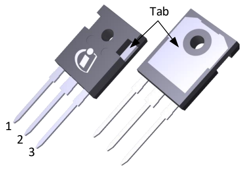
SiC MOSFET

CoolSiC™ MOSFET 650 V G2

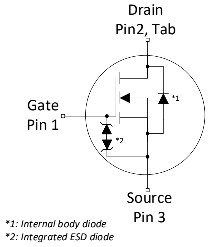
PG-TO247-3

Built on Infineon's robust 2nd generation Silicon Carbide trench technology, the 650 V CoolSiC™ MOSFET delivers unparalleled performance, superior reliability, and great ease of use. It enables cost effective, highly efficient, and simplified designs to fulfill the ever-growing system and market needs.



Features

- Ultra-low switching losses
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.5 V
- Robust against parasitic turn-on even with 0 V turn-off gate voltage
- Flexible driving voltage and compatible with bipolar driving scheme
- Robust body diode operation under hard commutation events
- .XT interconnection technology for best-in-class thermal performance



Benefits

- Enables high efficiency and high power density designs
- Facilitates great ease of use and integration
- Provides the best price performance ratio compared to Industry's most ambitious roadmaps
- Reduces the size, weight and bill of materials of the systems
- Enhances system robustness and reliability

Potential applications

- SMPS
- Solar PV inverters
- Energy storage and battery formation
- UPS
- EV charging infrastructure
- Motor drives

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DSS} over full $T_{j,range}$	650	V
$R_{DS(on),typ}$	75	mΩ
$R_{DS(on),max}$	95	mΩ
$Q_{G,typ}$	14.9	nC
$I_{D,pulse}$	74	A
Q_{oss} @ 400 V	32	nC
E_{oss} @ 400 V	4.4	µJ

Part number	Package	Marking	Related links
IMW65R075M2H	PG-TO247-3	65R075M2	see Appendix A

Table of contents

1 Maximum ratings

at $T_j = 25°C$, unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous DC drain current [1]	I_{DDC}	-	-	26.6	A	$T_c = 25°C$
				18.7		$T_c = 100°C$
Peak drain current [2]	I_{DM}	-	-	74	A	$T_c = 25°C$, $V_{GS} = 18$ V
Avalanche energy, single pulse	E_{AS}	-	-	68	mJ	$I_D = 2.5$ A, $V_{DD} = 50$ V; see table 11
Avalanche energy, repetitive	E_{AR}			0.34		
Avalanche current, single pulse	I_{AS}	-	-	2.5	A	-
MOSFET *dv/dt* ruggedness	*dv/dt*	-	-	200	V/ns	$V_{DS} = 0...400$ V
Gate source voltage (static) [3]	V_{GS}	-7	-	23	V	-
Gate source voltage (transient)	V_{GS}	-10	-	25	V	$t_p \leq 500$ ns, duty cycle ≤ 1%
Power dissipation	P_{tot}	-	-	111	W	$T_c = 25°C$
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j			175		
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous reverse drain current [1]	I_{SDC}	-	-	26.6	A	$V_{GS} = 18$ V, $T_c = 25°C$
				18.4		$V_{GS} = 0$ V, $T_c = 25°C$
Peak reverse drain current [2]	I_{SM}	-	-	74	A	$T_c = 25°C$, $t_p \leq 250$ ns
				22.3		$T_c = 25°C$
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, $T_c = 25°C$, $t = 1$ min

[1] Limited by $T_{j,max}$.

[2] Pulse width t_{pulse} limited by $T_{j,max}$.

[3] The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th(j-c)}$	-	-	1.35	°C/W	Not subject to production test. Parameter verified by design/characterization according to JESD51-14.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

3 Operating range

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$		0			

4 Electrical characteristics

at T_j = 25°C, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source voltage	V_{DSS}	650	-	-	V	V_{GS} = 0 V, I_D = 0.24 mA
Gate threshold voltage [4]	$V_{GS(th)}$	3.5	4.5	5.6	V	V_{DS} = V_{GS}, I_D = 2.4 mA
Zero gate voltage drain current	I_{DSS}	-	1	75	µA	V_{DS} = 650 V, V_{GS} = 0 V, T_j = 25°C
			3	-		V_{DS} = 650 V, V_{GS} = 0 V, T_j = 175°C
Gate-source leakage current	I_{GSS}	-	-	1000	nA	V_{GS} = 20 V, V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	98	-	mΩ	V_{GS} = 15 V, I_D = 11.9 A, T_j = 25°C
			75	95		V_{GS} = 18 V, I_D = 11.9 A, T_j = 25°C
			68	-		V_{GS} = 20 V, I_D = 11.9 A, T_j = 25°C
			123	-		V_{GS} = 18 V, I_D = 11.9 A, T_j =175°C
Internal gate resistance	$R_{G,int}$	-	4.3	-	Ω	f = 1 MHz

[4] Tested after 1 ms pulse at V_{GS} = +20 V. “Linear mode” operation is not recommended. For assessment of potential “linear mode” operation, please contact Infineon sales office.

Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.
Stray inductances and coupling capacitances must be minimized.
For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	516	-	pF	V_{GS} = 0 V, V_{DS} = 400 V, f = 250 kHz
Reverse transfer capacitance	C_{rss}		3.6	-		
Output capacitance [5]	C_{oss}		44	57		
Output charge [5]	Q_{oss}	-	32	42	nC	calculation based on C_{oss}
Effective output capacitance, energy related [6]	$C_{o(er)}$	-	55	-	pF	V_{GS} = 0 V, V_{DS} = 0...400 V
Effective output capacitance, time related [7]	$C_{o(tr)}$	-	81	-	pF	I_D = constant, V_{GS} = 0 V, V_{DS} = 0... 400 V
Turn-on delay time	$t_{d(on)}$	-	15	-	ns	V_{DD} = 400 V, V_{GS} = 0/18 V, I_D = 11.9 A, $R_{G,ext}$ = 1.8 Ω; see table 10
Rise time	t_r		10.6			
Turn-off delay time	$t_{d(off)}$		12.8			
Fall time	t_f		5.5			

Table 6 Dynamic characteristics

External parasitic elements (PCB layout) influence switching behavior significantly.
Stray inductances and coupling capacitances must be minimized.
For layout recommendations please use provided application notes or contact Infineon sales office.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Turn-ON switching losses [8]	E_{on}	-	44	-	µJ	V_{DD} = 400 V, V_{GS} = 0/18 V, I_D = 11.9 A, $R_{G,ext}$ = 1.8 Ω
Turn-OFF switching losses [8]	E_{off}		11			
Total switching losses [8]	E_{tot}		55			

[5] Maximum specification is defined by calculated six sigma upper confidence bound.

[6] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.

[7] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V.

[8] MOSFET used in half-bridge configuration without external diode.

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Plateau gate to source charge	$Q_{GS(pl)}$	-	3.7	-	nC	V_{DD} = 400 V, I_D = 11.9 A, V_{GS} = 0 to 18 V
Gate to drain charge	Q_{GD}		2.9			
Total gate charge	Q_G		14.9			

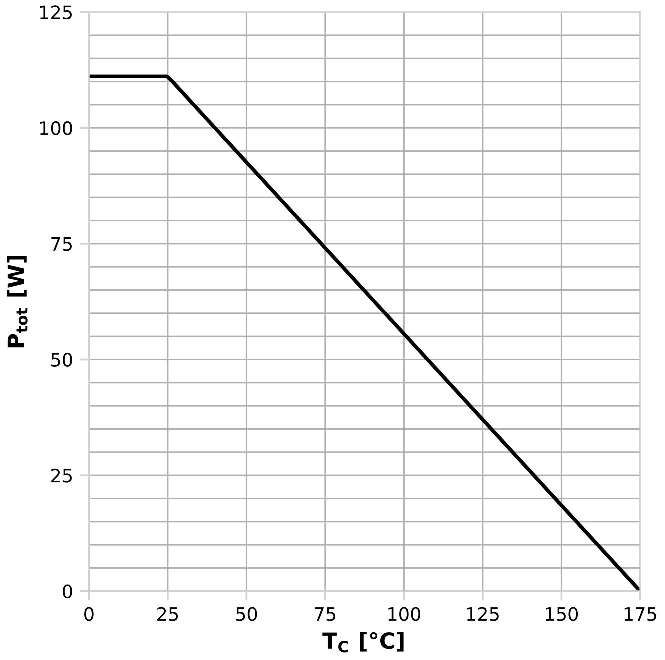
Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source reverse voltage	V_{SD}	-	4.3	-	V	V_{GS} = 0 V, I_S = 11.9 A, T_j = 25°C
MOSFET forward recovery time	t_{fr}	-	23	-	ns	V_{DD} = 400 V, I_S = 11.9 A, di_S/dt = 1000 A/µs; see table 9
MOSFET forward recovery charge [9]	Q_{fr}		60		nC	
MOSFET peak forward recovery current	I_{frm}		5.3		A	

[9] Q_{fr} includes Q_{oss}.

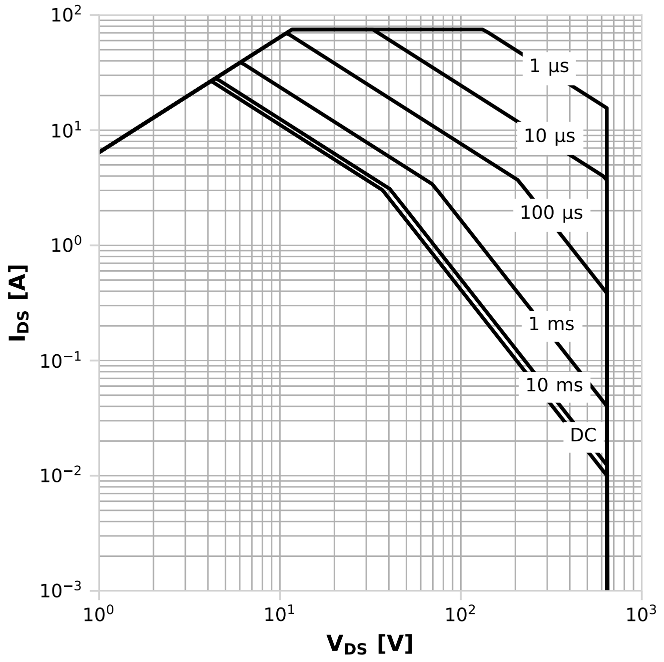
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



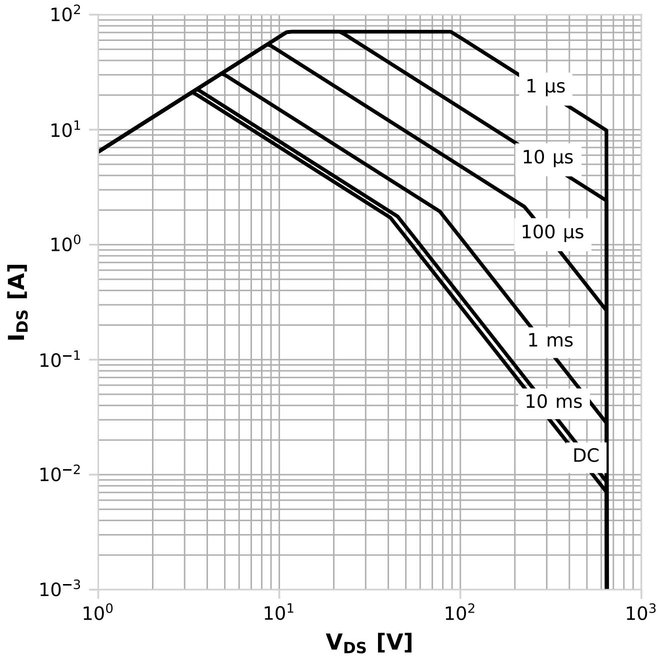
P_{tot}=f(T_C)

Diagram 2: Safe operating area



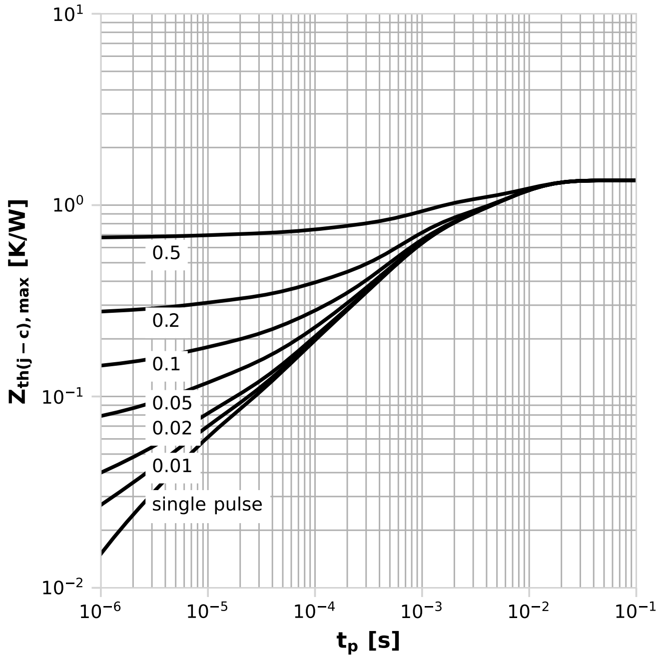
I_{DS}=f(V_{DS}); T_C=25°C; D=0; parameter: t_p

Diagram 3: Safe operating area



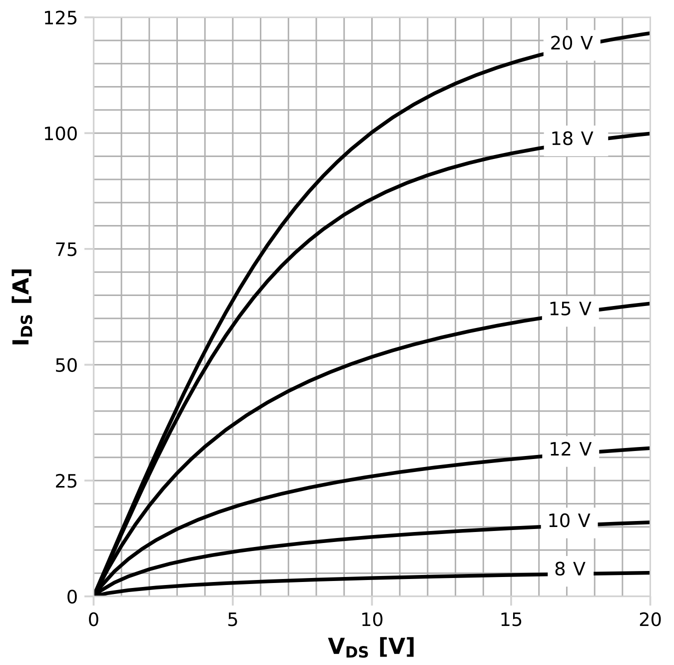
I_{DS}=f(V_{DS}); T_C=80°C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



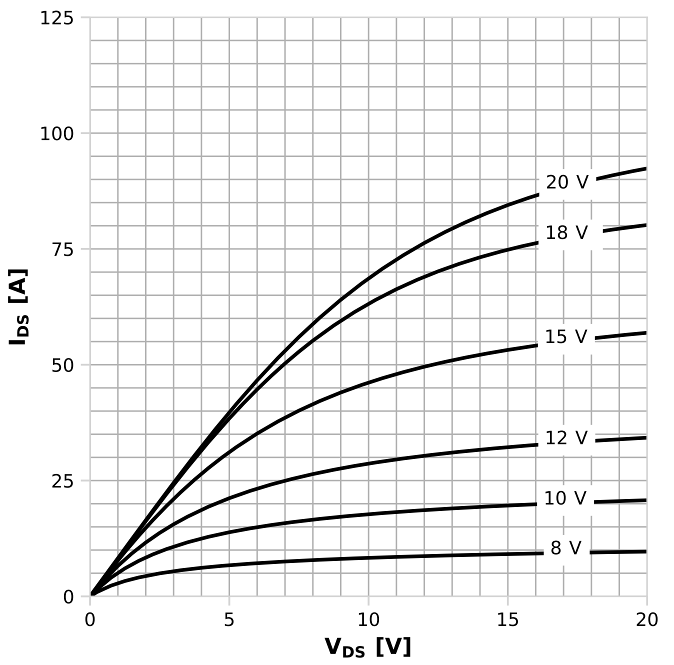
$Z_{th(j\text{-}c),max}$=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



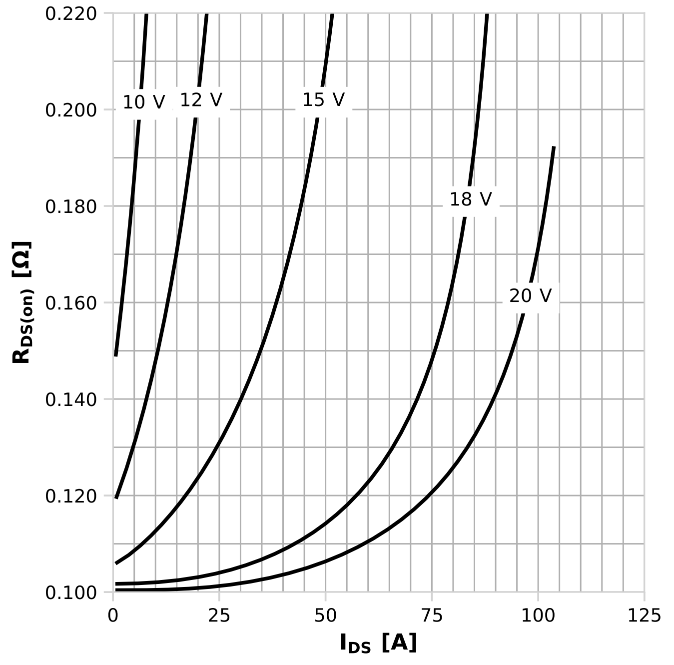
I_{DS}=f(V_{DS}); T_j=25°C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



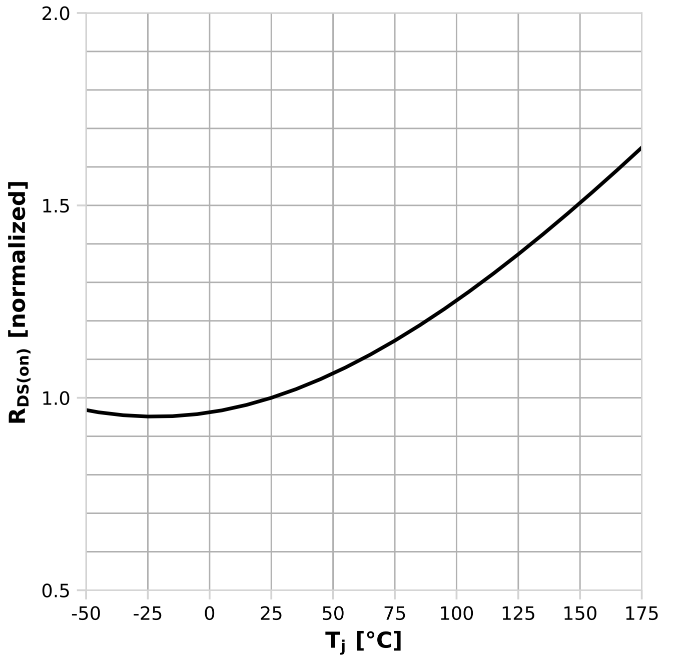
I_{DS}=f(V_{DS}); T_j=175°C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



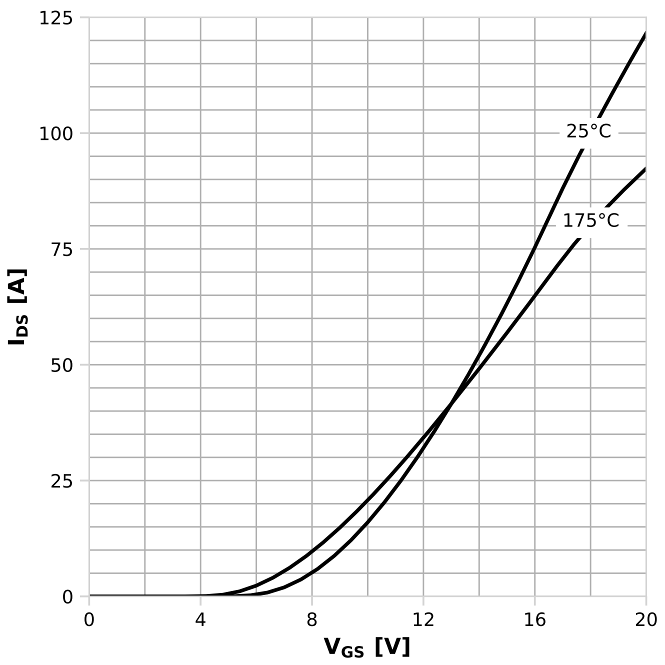
$R_{DS(on)}$=f(I_{DS}); T_j=125°C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



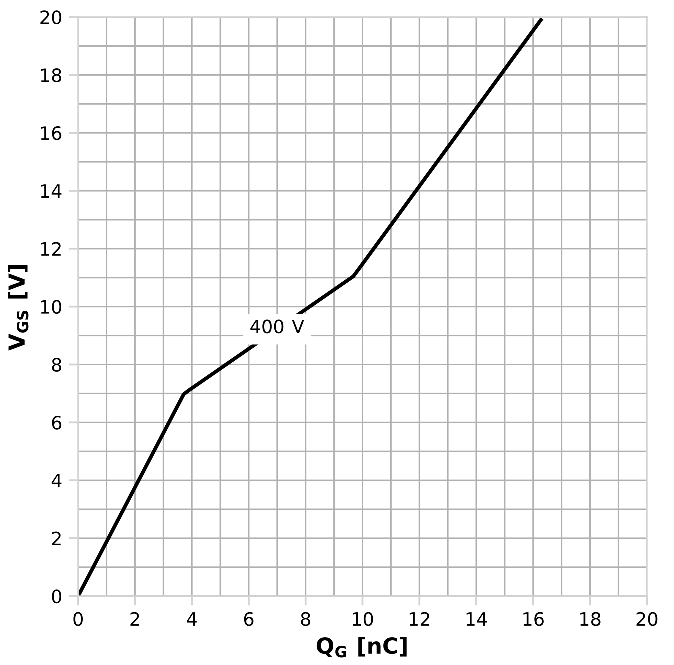
$R_{DS(on)}$=f(T_j); I_D=11.9 A; V_{GS}=18 V

Diagram 9: Typ. transfer characteristics



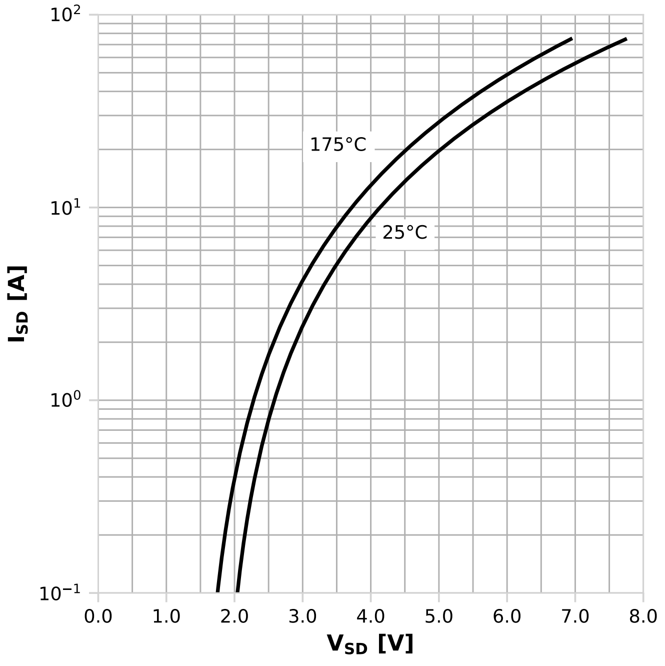
I_{DS}=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



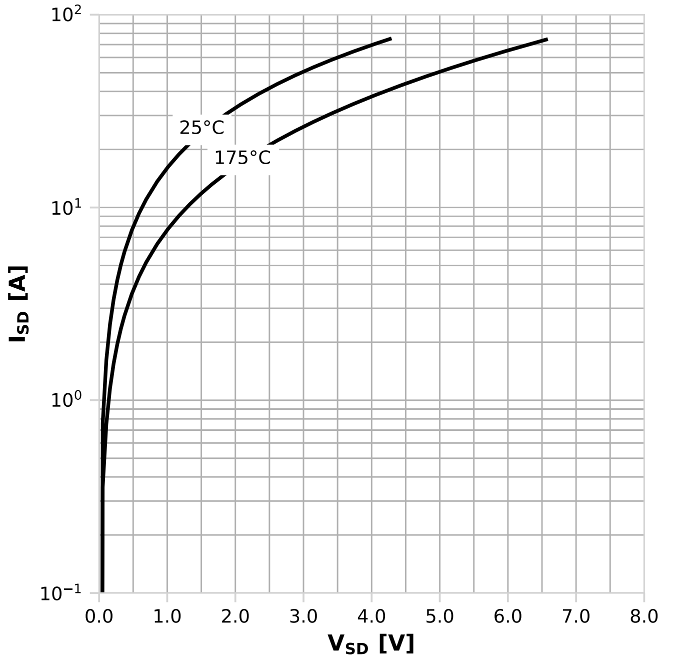
V_{GS}=f(Q_G); I_D=11.9 A pulsed; parameter: V_{DD}

Diagram 11: Typ. reverse drain current characteristics



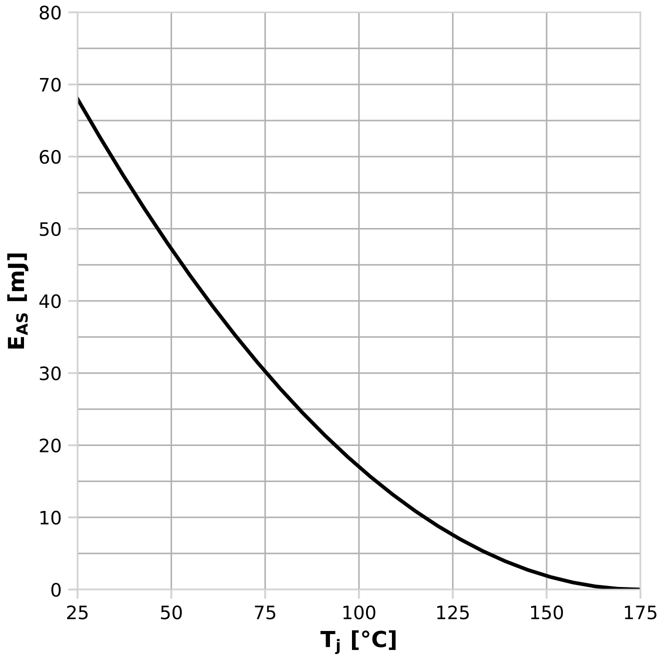
I_{SD}=f(V_{SD}); V_{GS}=0 V; parameter: T_j

Diagram 12: Typ. reverse drain current characteristics



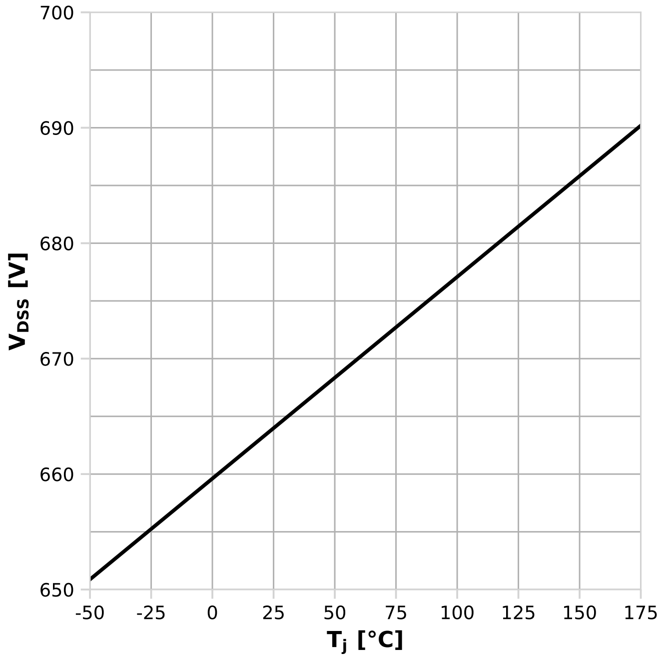
I_{SD}=f(V_{SD}); V_{GS}=18 V; parameter: T_j

Diagram 13: Avalanche energy



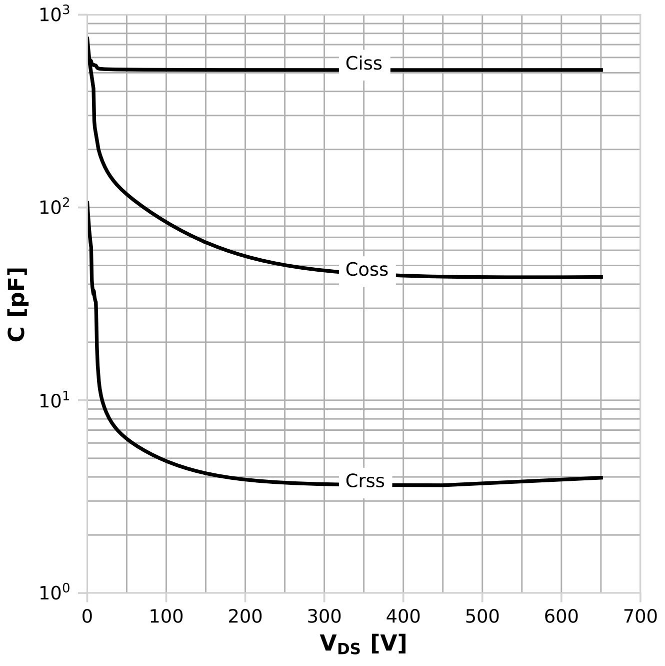
E_{AS}=f(T_j); I_D=2.5 A; V_{DD}=50 V

Diagram 14: Drain-source breakdown voltage



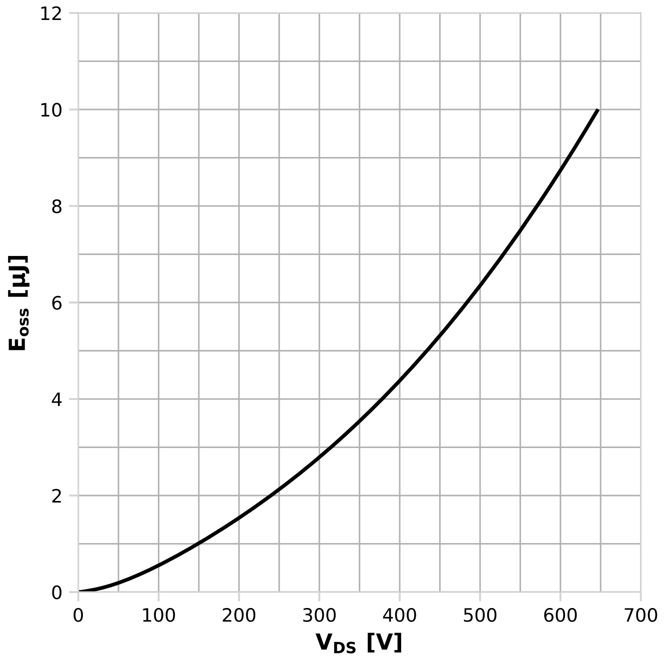
V_{DSS}=f(T_j); I_D=0.24 mA

Diagram 15: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 16: Typ. Coss stored energy



E_{oss}=f(V_{DS})

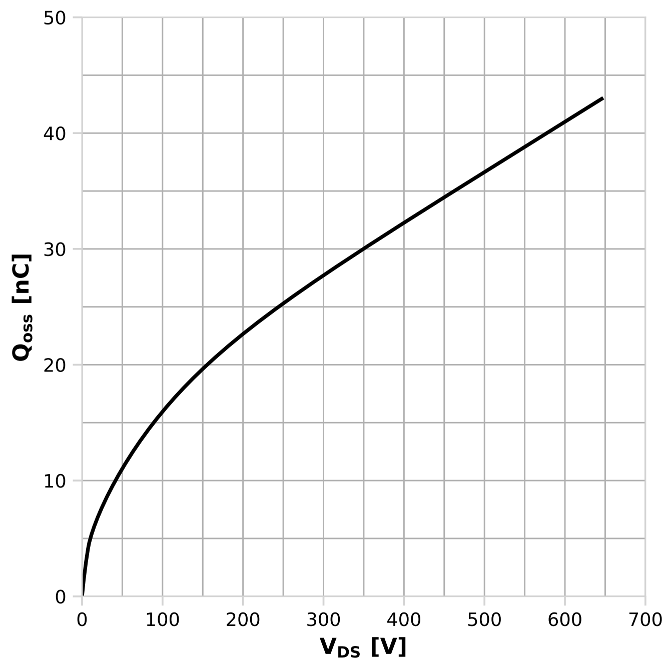
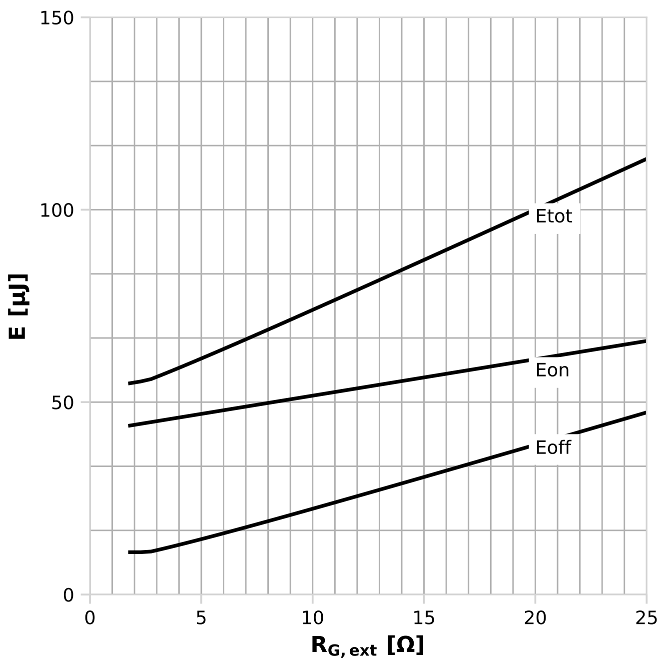
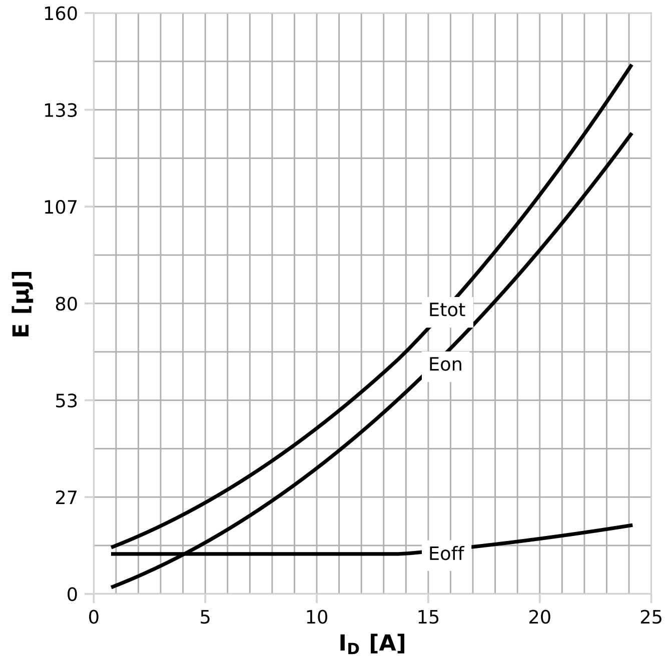
Diagram 17: Typ. Qoss output charge	Diagram 18: Typ. Switching Losses vs $R_{G,ext}$
	
$Q_{oss}=f(V_{DS})$	$E=f(R_{G,ext})$; $V_{DD}=400$ V; $V_{GS}=0\text{-}18$ V; $I_D=11.9$ A

Diagram 19: Typ. Switching Losses vs switching current

$E=f(I_D)$; $V_{DD}=400$ V; $V_{GS}=0\text{-}18$ V; $R_{G,ext}=1.8\ \Omega$

6 Test circuits

Table 9 Body diode characteristics

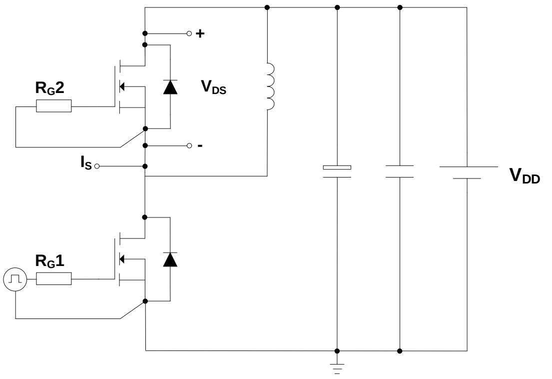
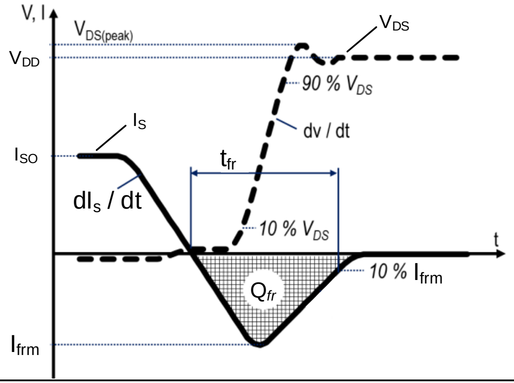
Test circuit for body diode characteristics	Body diode recovery waveform
	

Table 10 Switching times

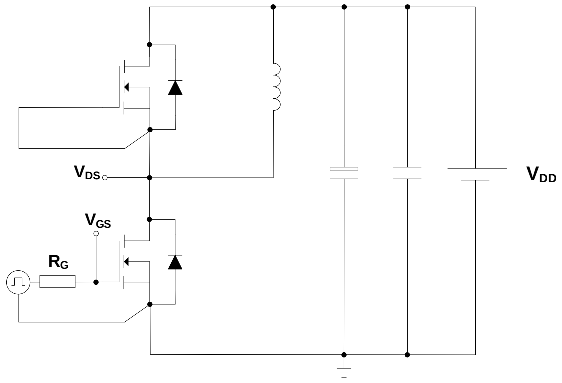
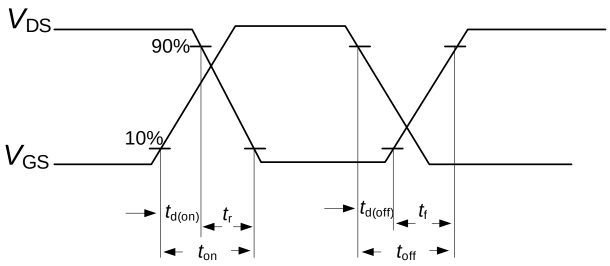
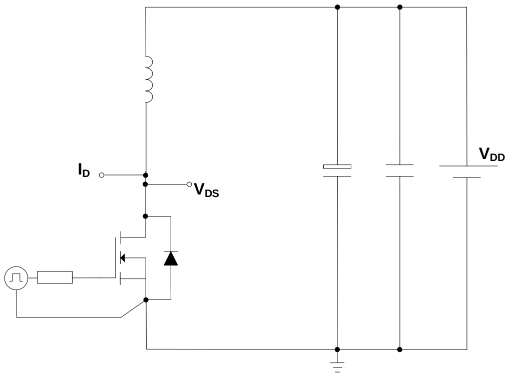
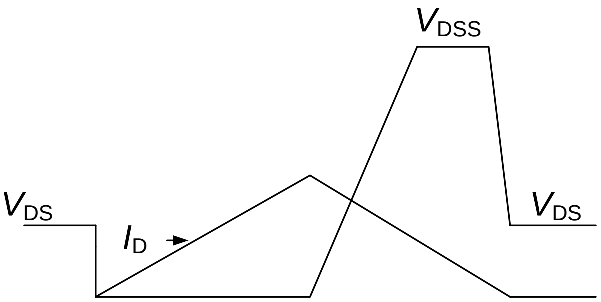
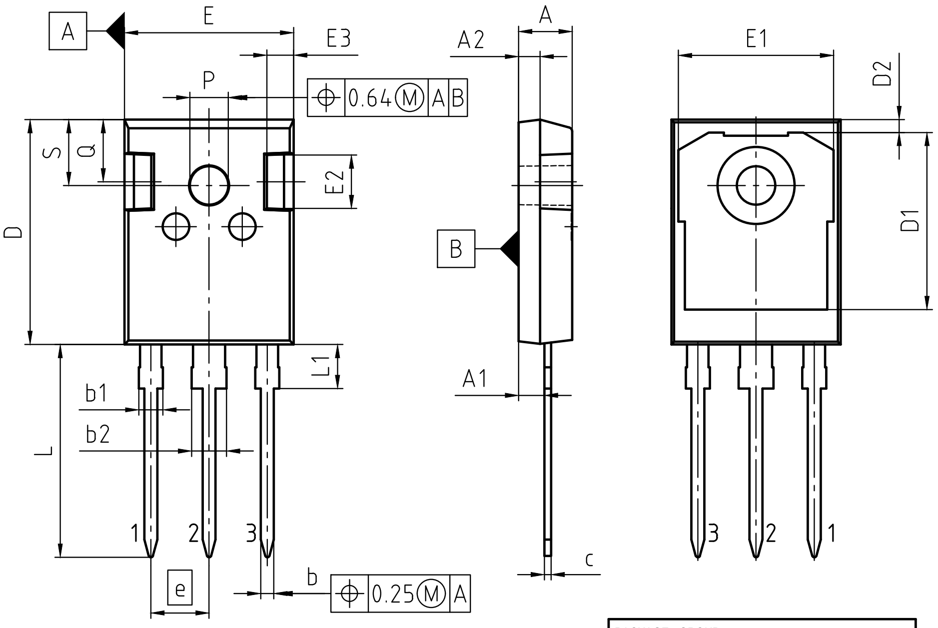
Switching times test circuit for inductive load	Switching times waveform
	

Table 11 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package outlines



PACKAGE - GROUP NUMBER:	PG-TO247-3	
DIMENSIONS	**MILLIMETERS**	
	MIN.	MAX.
A	4.70	5.30
A1	2.20	2.60
A2	1.50	2.50
b	1.00	1.40
b1	1.60	2.41
b2	2.57	3.43
c	0.38	0.89
D	20.70	21.50
D1	13.08	17.65
D2	0.51	1.35
E	15.50	16.30
E1	12.38	14.15
E2	3.40	5.10
E3	1.00	2.60
e	5.44	
N	3	
L	19.80	20.40
L1	3.85	4.50
øP	3.50	3.70
Q	5.35	6.25
S	6.04	6.30

NOTE:
DIMENSIONS DO NOT INCLUDE MOLDFLASH; PROTRUSION OR GATE BURRS

Figure 1 Outline PG-TO247-3, dimensions in mm

8 Appendix A

Table 12 Related links

- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Webpage
- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Application Note
- IFX CoolSiC CoolSiC™ MOSFET 650 V G2 Simulation Model
- IFX Design tools

Revision history

IMW65R075M2H

Revision 2025-07-23, Rev. 2.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2025-05-08	Release of final version
2.1	2025-07-23	Minor layout changes

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