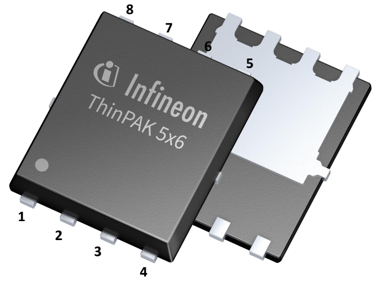
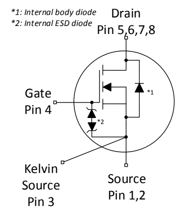
MOSFET

700V CoolMOS™ P7 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.
The latest CoolMOS™ P7 is an optimized platform tailored to target cost sensitive applications in consumer markets such as charger, adapter, lighting, TV, etc.
The new series provides all the benefits of a fast switching Superjunction MOSFET, combined with an excellent price/performance ratio and state of the art ease-of-use level. The technology meets highest efficiency standards and supports high power density, enabling customers going towards very slim designs.

ThinPAK 5x6





Features

- Extremely low losses due to very low FOM $R_{DS(on)}$*Q_g and $R_{DS(on)}$*E_{oss}
- Excellent thermal behavior
- Integrated ESD protection diode
- Low switching losses (E_{oss})
- Fully qualified acc. JEDEC for Industrial Applications

Benefits

- Cost competitive technology
- Lower temperature
- High ESD ruggedness
- Enables efficiency gains at higher switching frequencies
- Enables high power density designs and small form factors

Potential applications

Recommended for Flyback topologies in Chargers and Adapters

Please note: For MOSFET paralleling the use of ferrite beads on the gate or seperate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j=25°C}$	700	V
$R_{DS(on),max}$	1.2	Ω
$Q_{g,typ}$	4.8	nC
$I_{D,pulse}$	9.4	A
E_{oss} @ 400V	0.7	µJ
$V_{(GS)th,typ}$	3	V
ESD class (HBM)	1C	

Type / Ordering Code	Package	Marking	Related Links
IPLK70R1K2P7	ThinPAK 5x6 SMD	70R1K2P7	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	4.4 2.7	A	T_C = 20°C T_C = 100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	9.4	A	T_C=25°C
Application (Flyback) relevant avalanche current, single pulse[3]	I_{AS}	-	1.6	-	A	measured with standard leakage inductance of transformer of 5µH
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	V_{DS} =0...400V
Gate source voltage	V_{GS}	-16 -30	- -	16 30	V	static; AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	25.5	W	T_C=25°C
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-
Continuous diode forward current	I_S	-	-	5.6	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	9.4	A	T_C = 25°C
Reverse diode dv/dt[4]	dv/dt	-	-	1	V/ns	V_{DS} =0...400V, I_{SD}<=I_S, T_j=25°C
Maximum diode commutation speed[4]	di_f/dt	-	-	50	A/µs	V_{DS} =0...400V, I_{SD}<=I_S, T_j=25°C
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction	R_{thJC}	-	-	4.9	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	Device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	62	°C/W	Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm^2 (one layer 70µm thickness) copper area for drain connection and cooling. PCB is vertical without airflow.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

[1] Limited by $T_{j\,max}$. T_j = 20°C. Maximum duty cycle D=0.5
[2] Pulse width t_p limited by $T_{j,max}$
[3] Proven during verification test. Avalanche value is assuming only the energy from a Flyback transformer leakage inductance is transferred to the MOSFET. For less common avalanche situations it is recommended to contact Infineon for more information. For explanation please read AN - CoolMOS™ 700V P7.
[4] V_{DClink}=400V; $V_{DS,peak}$<$V_{(BR)DSS}$; identical low side and high side switch with identical R_G

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	700	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	2.50	3	3.50	V	V_{DS}=V_{GS}, I_D=0.04mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=700V, V_{GS}=0V, T_j=25°C V_{DS}=700V, V_{GS}=0V, T_j=150°C
Gate-source leakage current incl. Zener diode	I_{GSS}	-	-	1	µA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.98 2.24	1.20 -	Ω	V_{GS}=10V, I_D=0.9A, T_j=25°C V_{GS}=10V, I_D=0.9A, T_j=150°C
Gate resistance	R_G	-	1.6	-	Ω	f=1 MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	174	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	3.6	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	10	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	132	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=0.6A, R_G=8.2Ω
Rise time	t_r	-	4.8	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=0.6A, R_G=8.2Ω
Turn-off delay time	$t_{d(off)}$	-	60	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=0.6A, R_G=8.2Ω
Fall time	t_f	-	48	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=0.6A, R_G=8.2Ω

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	0.8	-	nC	V_{DD}=400V, I_D=0.6A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	1.9	-	nC	V_{DD}=400V, I_D=0.6A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	4.8	-	nC	V_{DD}=400V, I_D=0.6A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	4.3	-	V	V_{DD}=400V, I_D=0.6A, V_{GS}=0 to 10V

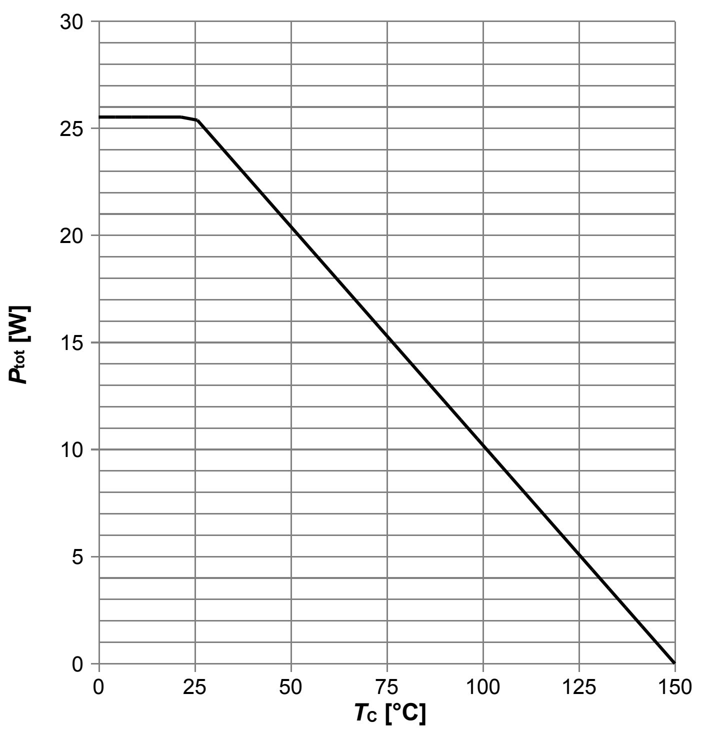
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=1.1A, T_j=25°C
Reverse recovery time	t_{rr}	-	270	-	ns	V_R=400V, I_F=0.6A, di_F/dt=50A/µs
Reverse recovery charge	Q_{rr}	-	0.5	-	µC	V_R=400V, I_F=0.6A, di_F/dt=50A/µs
Peak reverse recovery current	I_{rrm}	-	6	-	A	V_R=400V, I_F=0.6A, di_F/dt=50A/µs

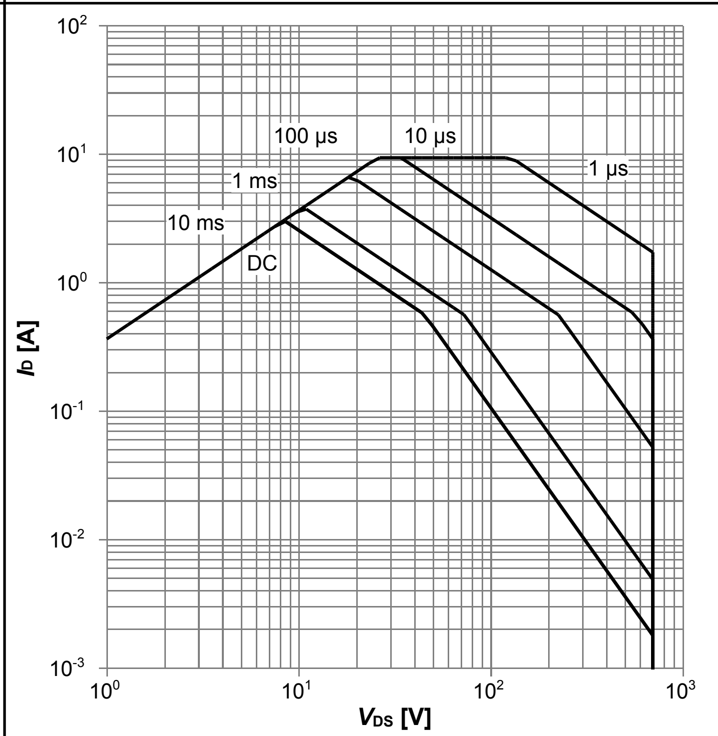
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



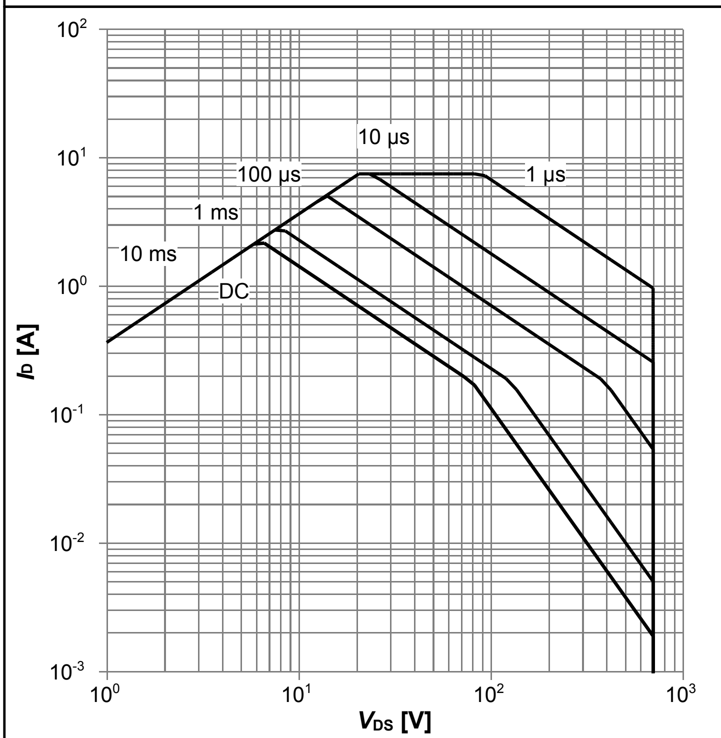
P_{tot}=f(T_C)

Diagram 2: Safe operating area



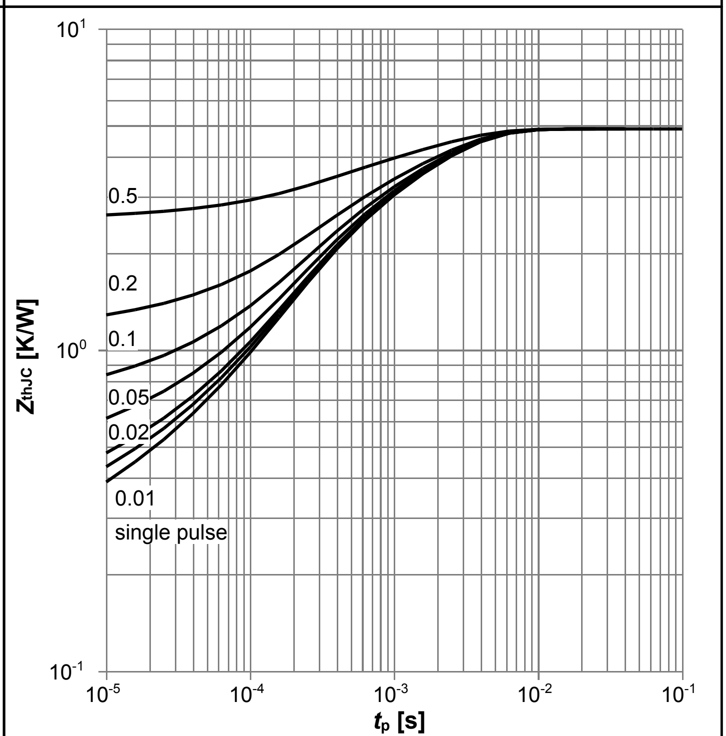
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



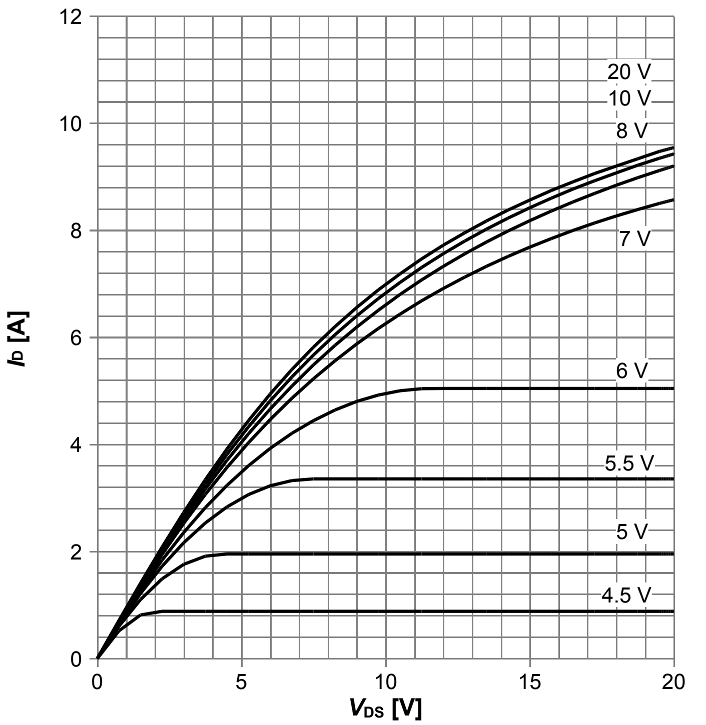
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



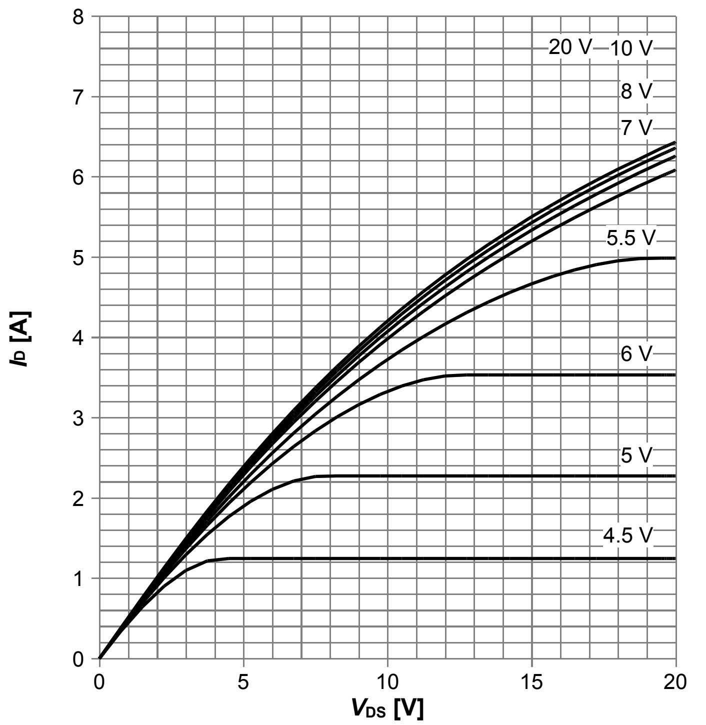
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



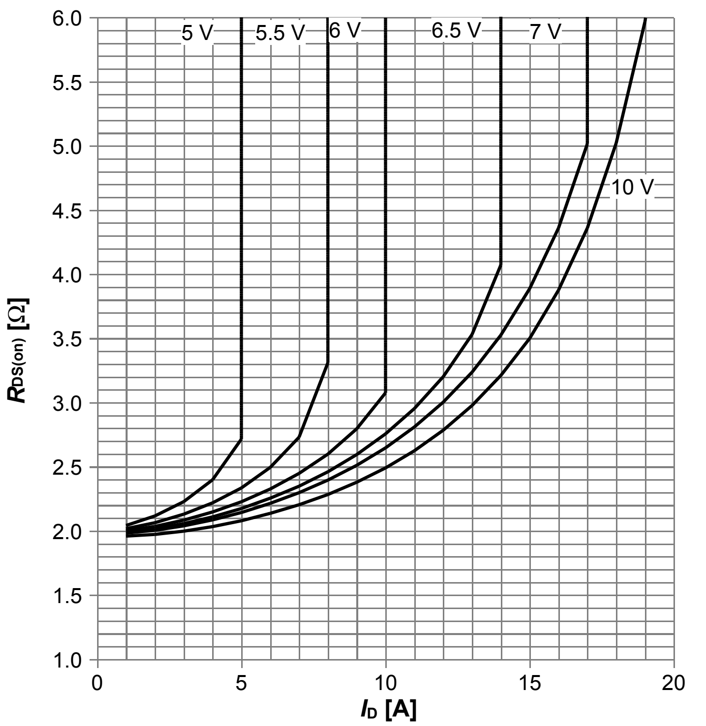
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



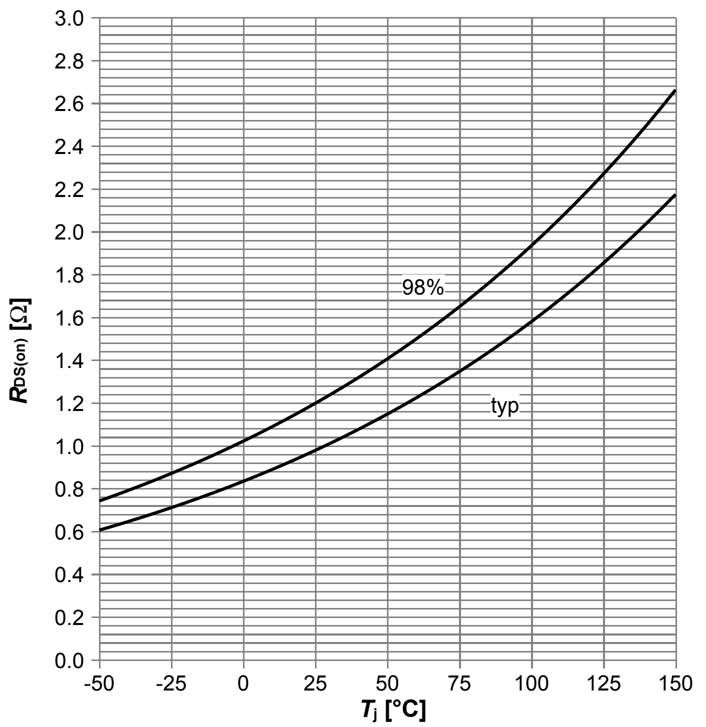
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



$R_{DS(on)}$=f(T_j); I_D=0.9 A; V_{GS}=10 V

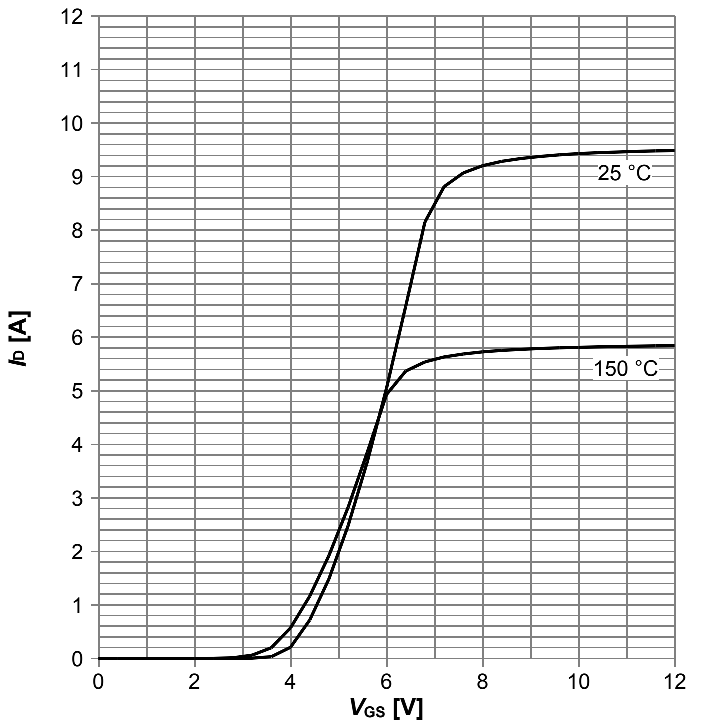
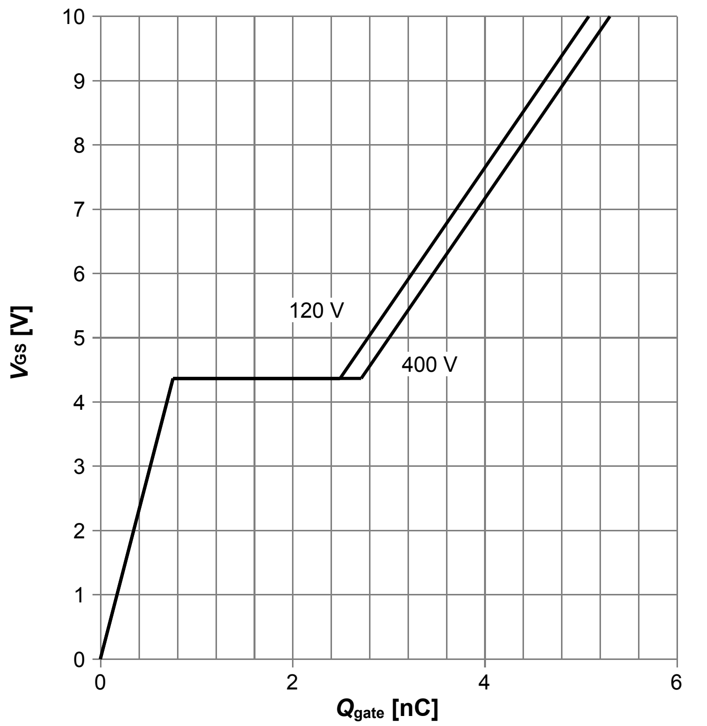
Diagram 9: Typ. transfer characteristics	Diagram 10: Typ. gate charge
	
$I_D=f(V_{GS})$; V_{DS}=20V; parameter: T_j	$V_{GS}=f(Q_{gate})$; I_D=0.6 A pulsed; parameter: V_{DD}

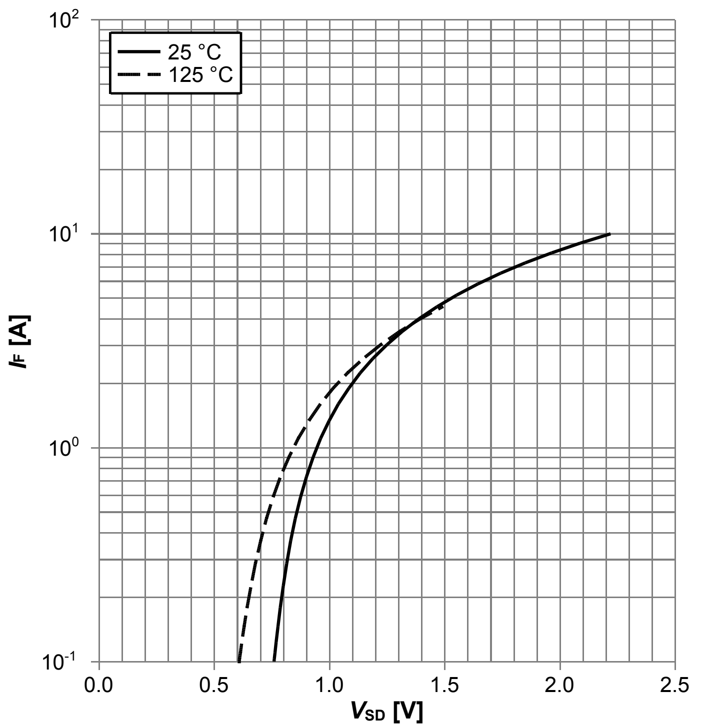
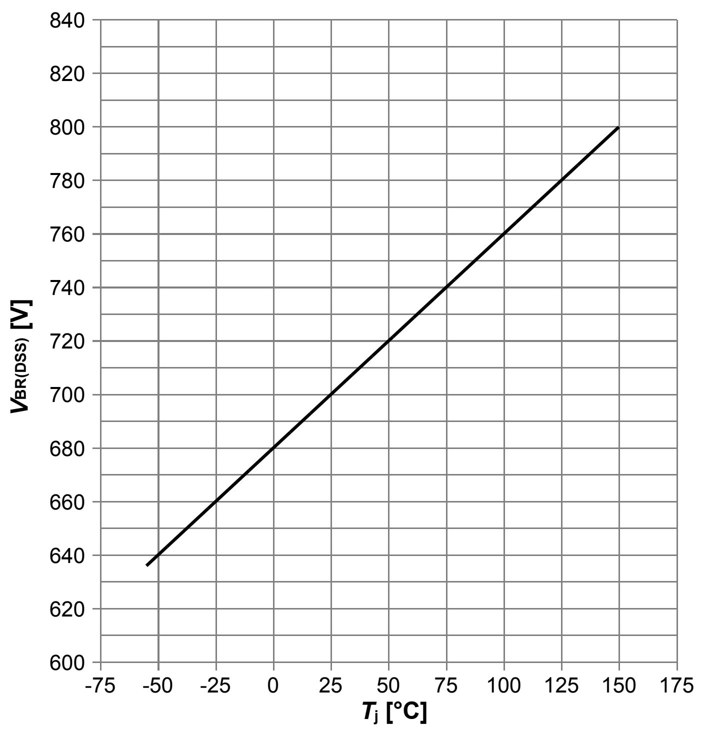
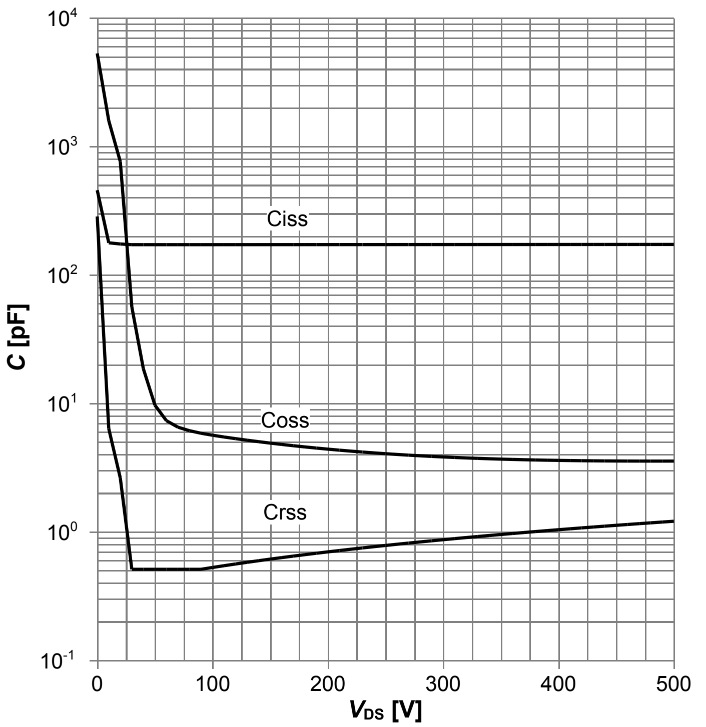
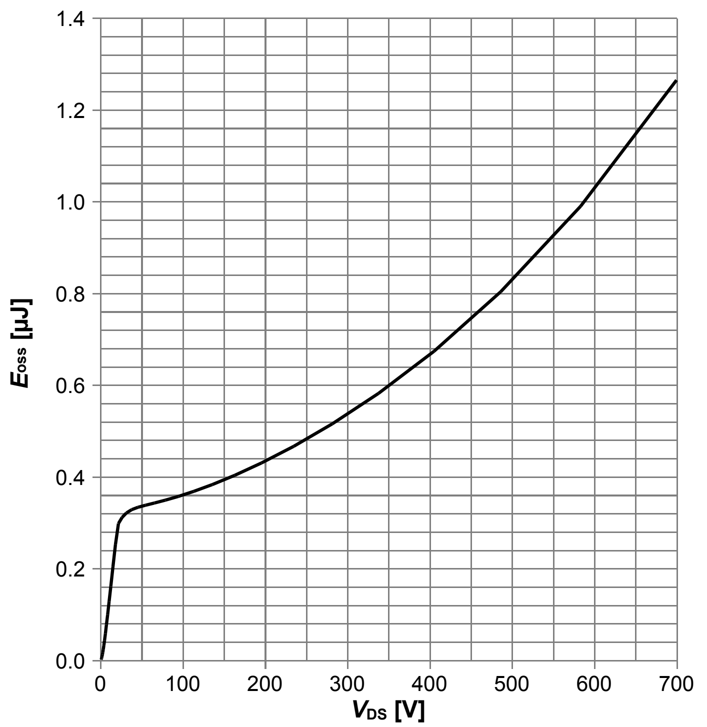
Diagram 11: Forward characteristics of reverse diode	Diagram 13: Drain-source breakdown voltage
	
$I_F=f(V_{SD})$; parameter: T_j	$V_{BR(DSS)}=f(T_j)$; I_D=1 mA

Diagram 14: Typ. capacitances	Diagram 15: Typ. Coss stored energy
	
C=f(V_{DS}); V_{GS}=0 V; f=250 kHz	E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

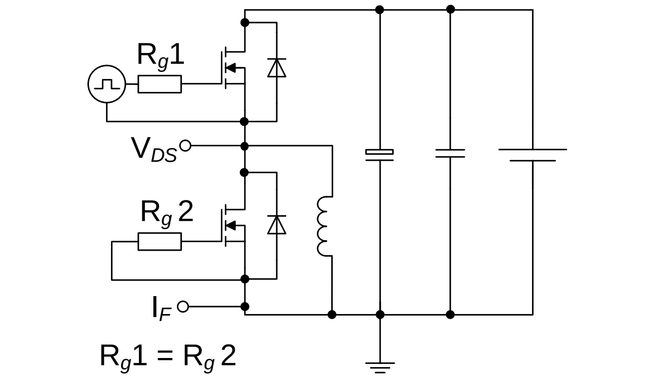
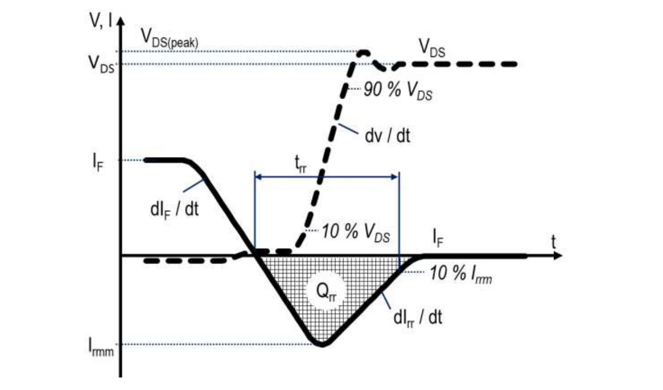
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

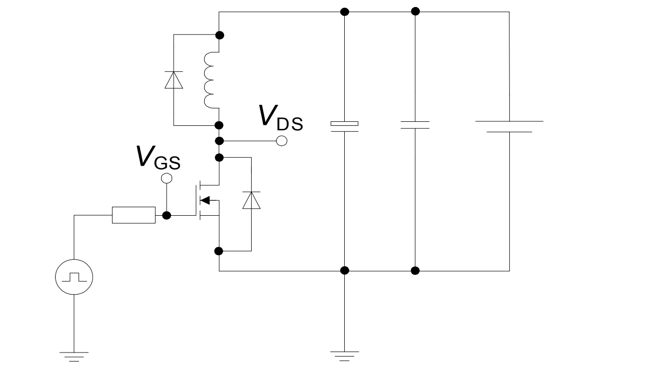
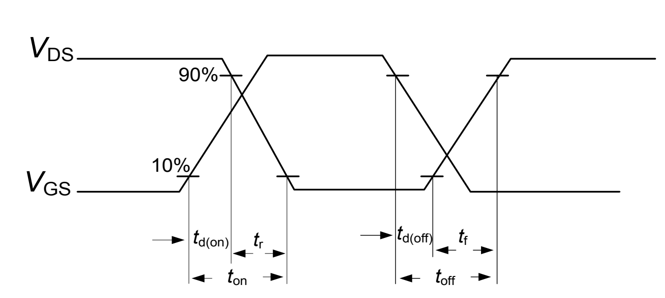
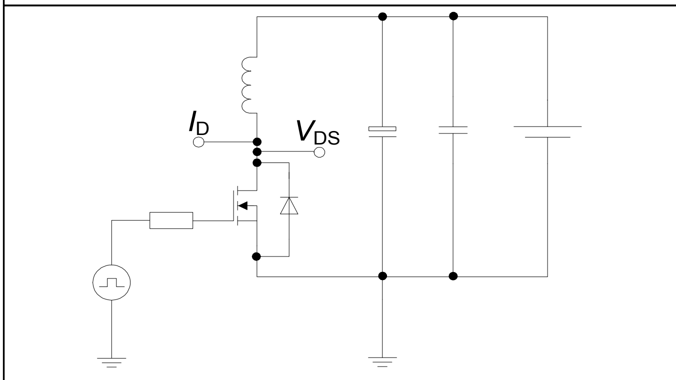
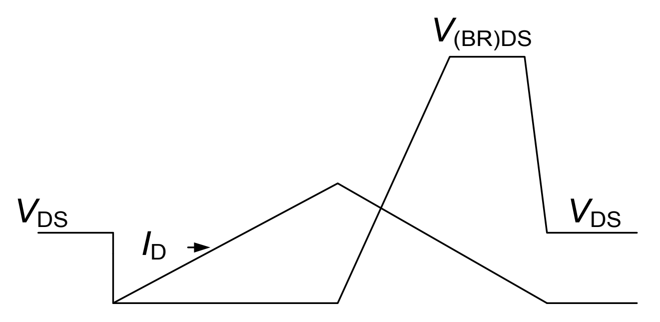
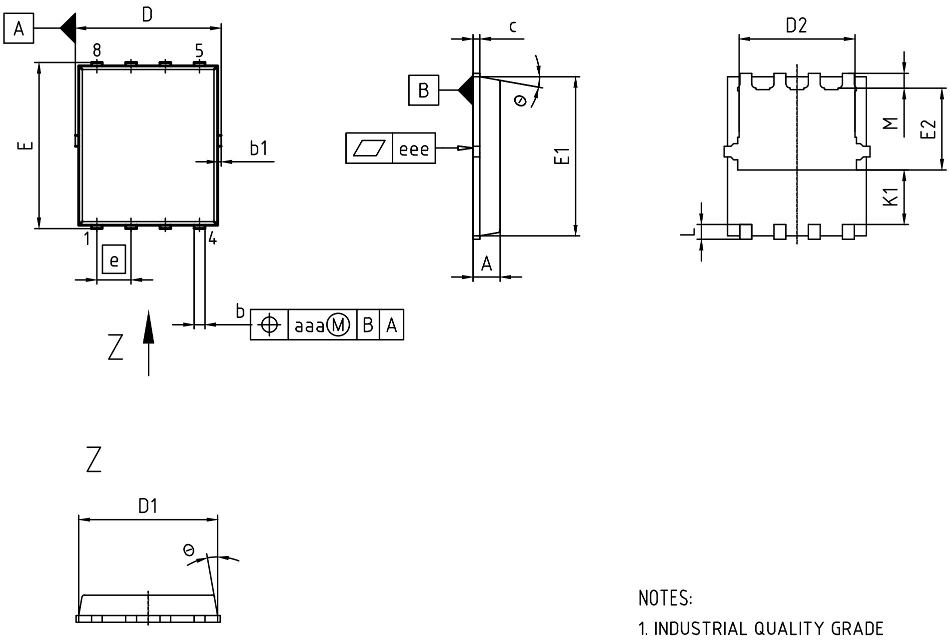
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



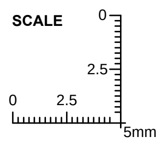
NOTES:

1. INDUSTRIAL QUALITY GRADE
2. ALL DIMENSIONS REFER TO JEDEC STANDARD MO240A NOT INCLUDE MOLD FLASH
3. REMOVAL ON MOLD GATE, INTRUSION 0.1mm; PROPRUSION 0.1mm
4. ALL METAL SURFACE ARE PLATEDEXCEPT AREA OF CUT

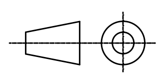
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.34	0.54	0.013	0.021
b1	0.03	0.23	0.001	0.009
c	0.15	0.35	0.006	0.014
D	5.15	5.51	0.203	0.217
D1	4.95	5.35	0.195	0.211
D2	4.20	4.40	0.165	0.173
E	5.95	6.35	0.234	0.250
E1	5.70	6.10	0.224	0.240
E2	2.93	3.13	0.115	0.123
e	1.27		0.050	
N	8		8	
K1	1.92	2.12	0.076	0.083
L	0.45	0.65	0.018	0.026
M	0.45	0.65	0.018	0.026
Θ	8.5°	12°	8.5°	12°
aaa	0.25		0.010	
eee	0.08		0.003	

DOCUMENT NO.
Z8B00181453

SCALE



EUROPEAN PROJECTION



ISSUE DATE
13-05-2016

REVISION
01

Figure 1 Outline ThinPAK 5x6 SMD, dimensions in mm/inches - Industrial Grade

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS™ P7 Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPLK70R1K2P7

Revision: 2018-09-26, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2018-09-26	Release of final version

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