

## CoolGaN™ G5

### CoolGaN™ Transistor 650 V G5

Infineon's CoolGaN™ is a highly efficient gallium nitride (GaN) transistor designed for power conversion at 650 V. It enables higher power density, supports reduced system BOM cost, and facilitates miniaturized form factors. Produced using 200 mm (8 inch) wafer technology and fully automated production lines, it features narrow production tolerances and the highest product quality. This makes it suitable for a wide range of applications, from consumer electronics to industrial applications.

### Features

- Enhancement mode transistor
- Ultra-fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate and output charge
- Superior commutation ruggedness
- 2 kV HBM ESD standards

### Benefits

- Normally OFF transistor technology ensures safe operation
- Enables rapid and precise power delivery control
- Improves system efficiency and reliability
- Ensures robust performance under challenging conditions

These features collectively make CoolGaN™ a game-changer in the realm of power conversion, offering a compelling combination of efficiency, compactness, and reliability.

### Potential applications

Industrial, telecom, datacenter SMPS based on half-bridge hard and soft switching topologies such as totem pole PFC and high frequency LLC, as well as charger and adapter.

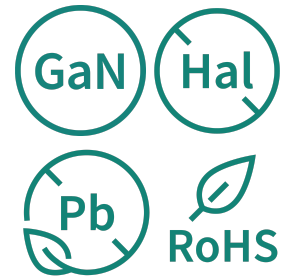
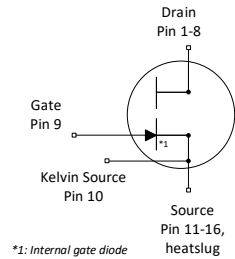
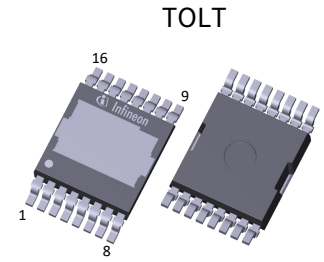
### Product validation

Fully qualified according to JEDEC for Industrial Applications

**Table 1** Key performance parameters

Parameter	Value	Unit
$V_{DS,max}$	650	V
$V_{DS,trans-max}$	900	V
$R_{DS(on),max}$	140	mΩ
$Q_{g,typ}$	2.4	nC
$I_{D,pulse}$	30	A
$Q_{oss @ 400 V}$	18	nC
$Q_{rr}$	0	nC

Type / Ordering code	Package	Marking	Related links
IGLT65R110D2	PG-HDSOP-16	65R110D2	see Appendix A



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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80% of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain source voltage, continuous	$V_{DS,max}$	-	-	650	V	$V_{GS} = 0\text{ V}$ , derating recommendation according JEDEC JEP198
Leakage current at drain source transient voltage	$I_{DS,trans}$	-	-	6.2	mA	$V_{GS} = 0\text{ V}$ , $V_{DS,trans} = 900\text{ V}$
Drain source voltage transient	$V_{DS,trans}$	-	-	900	V	<1% duty cycle, <1 $\mu\text{s}$ , 1 million pulses
Drain source voltage, pulsed	$V_{DS,pulsed}$	-	-	750 650	V	$T_j = 25^\circ\text{C}$ ; $V_{GS} \leq 0\text{ V}$ ; cumulated stress time $\leq 1\text{ h}$ $T_j = 125^\circ\text{C}$ ; $V_{GS} \leq 0\text{ V}$ ; cumulated stress time $\leq 1\text{ h}$
Switching surge voltage, pulsed	$V_{DS,surge}$	-	-	750	V	DC bus voltage = 700 V; turn off $V_{DS,pulse} = 750\text{ V}$ ; turn on $I_{D,pulse} = 13\text{ A}$ ; $T_j = 105^\circ\text{C}$ ; $f \leq 100\text{ kHz}$ , $t \leq 100\text{ s}$ (10 million pulses)
Continuous current, drain source <sup>1)</sup>	$I_D$	-	-	15	A	$T_c = 25^\circ\text{C}$ ; $T_j = T_{j,max}$
Pulsed current, drain source	$I_{D,pulse}$	-30 -18	-	30 18	A	$T_j = 25^\circ\text{C}$ ; $I_G = 13\text{ mA}$ ; See Diagram 3, 5 $T_j = 125^\circ\text{C}$ ; $I_G = 13\text{ mA}$ ; See Diagram 4, 6
Gate current, continuous <sup>2)</sup>	$I_{G,avg}$	-	-	10	mA	$T_j = -55^\circ\text{C}$ to $T_j = 150^\circ\text{C}$ ; See Table 9
Gate current, pulsed <sup>2)</sup>	$I_{G,pulsed}$	-1	-	1	A	$T_j = -55^\circ\text{C}$ to $T_j = 150^\circ\text{C}$ ; $t_{pulse} = 50\text{ ns}$ , $f = 100\text{ kHz}$ ; See Table 9
Gate source voltage, continuous <sup>2)</sup>	$V_{GS}$	-10	-	-	V	$T_j = -55^\circ\text{C}$ to $T_j = 150^\circ\text{C}$ ; See Diagram 12
Gate source voltage, pulsed <sup>2)</sup>	$V_{GS,pulse}$	-25	-	-	V	$T_j = -55^\circ\text{C}$ to $T_j = 150^\circ\text{C}$ ; $t_{pulse} = 50\text{ ns}$ , $f = 100\text{ kHz}$ ; open drain
Power dissipation	$P_{tot}$	-	-	55	W	$T_c = 25^\circ\text{C}$
Operating junction temperature	$T_j$	-55	-	150	$^\circ\text{C}$	-
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	Max shelf life depends on storage conditions
Drain-source voltage slew-rate	$dv/dt$	-	-	200	V/ns	-

<sup>1)</sup> Limited by  $T_{j,max}$ . Maximum duty cycle  $D = 0.75$

<sup>2)</sup> We recommend using an advanced driving technique to optimize the device performance. Please see gate drive application note for more details.

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	2.3	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	94	°C/W	Device on PCB, minimum footprint
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	-	68	°C/W	Device on 40 mm*40 mm*1.5 mm epoxy PCB FR4 with 6 cm <sup>2</sup> (one layer, 70 μm thickness) copper area. PCB is vertical without air stream cooling.
Reflow soldering temperature	$T_{sold}$	-	-	260	°C	reflow MSL1

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless specified otherwise

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9 -	1.2 1	1.6 -	V	$I_{DS}=1.3\text{ mA}; V_{DS}=10\text{ V}; T_j=25^\circ\text{C}$ $I_{DS}=1.3\text{ mA}; V_{DS}=10\text{ V}; T_j=150^\circ\text{C}$
Gate-Source reverse clamping voltage	$V_{GS, clamp}$	-	-	-8	V	$I_{GS}=-1\text{ mA}$
Drain-Source leakage current	$I_{DSS}$	-	0.51 10	51 -	$\mu\text{A}$	$V_{DS}=650\text{ V}, V_{GS}=0\text{ V}, T_j=25^\circ\text{C}$ $V_{DS}=650\text{ V}, V_{GS}=0\text{ V}, T_j=150^\circ\text{C}$
Drain-Source on-state resistance	$R_{DS(on)}$	-	0.110 0.240	0.140 -	$\Omega$	$I_G=13\text{ mA}; I_D=4.0\text{ A}; T_j=25^\circ\text{C}$ $I_G=13\text{ mA}; I_D=4.0\text{ A}; T_j=150^\circ\text{C}$
Gate resistance	$R_{G,int}$	-	0.96	-	$\Omega$	LCR impedance measurement; $f=f_{res}$ , open drain;

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	170	-	pF	$V_{GS}=0\text{ V}; V_{DS}=400\text{ V}, f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	29	-	pF	$V_{GS}=0\text{ V}, V_{DS}=400\text{ V}, f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	0.39	-	pF	$V_{GS}=0\text{ V}, V_{DS}=400\text{ V}, f=1\text{ MHz}$
Effective output capacitance, energy related <sup>3)</sup>	$C_{o(er)}$	-	33	-	pF	$V_{DS}=0\text{ to }400\text{ V}$
Effective output capacitance, time related <sup>4)</sup>	$C_{o(tr)}$	-	45	-	pF	$V_{GS}=0\text{ V}; V_{DS}=0\text{ to }400\text{ V}; I_D=const$
Output charge	$Q_{oss}$	-	18	-	nC	$V_{DS}=0\text{ to }400\text{ V}$
Coss stored energy	$E_{oss}$	-	2.6	-	$\mu\text{J}$	$V_{DS}=0\text{ to }400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	8	-	ns	$I_D=4\text{ A}; R_{ON}=10\text{ Ohm}; R_{OFF}=10\text{ Ohm}; R_{SS}=680\text{ Ohm}; C_C=1.5\text{ nF}; V_{DRV}=12\text{ V};$ see Table 8
Turn-off delay time	$t_{d(off)}$	-	10	-	ns	$I_D=4\text{ A}; R_{ON}=10\text{ Ohm}; R_{OFF}=10\text{ Ohm}; R_{SS}=680\text{ Ohm}; C_C=1.5\text{ nF}; V_{DRV}=12\text{ V};$ see Table 8
Rise time	$t_r$	-	7	-	ns	$I_D=4\text{ A}; R_{ON}=10\text{ Ohm}; R_{OFF}=10\text{ Ohm}; R_{SS}=680\text{ Ohm}; C_C=1.5\text{ nF}; V_{DRV}=12\text{ V};$ see Table 8
Fall time	$t_f$	-	20	-	ns	$I_D=4\text{ A}; R_{ON}=10\text{ Ohm}; R_{OFF}=10\text{ Ohm}; R_{SS}=680\text{ Ohm}; C_C=1.5\text{ nF}; V_{DRV}=12\text{ V};$ see Table 8

- 3)  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V  
 4)  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V

**Table 6 Gate charge characteristics**

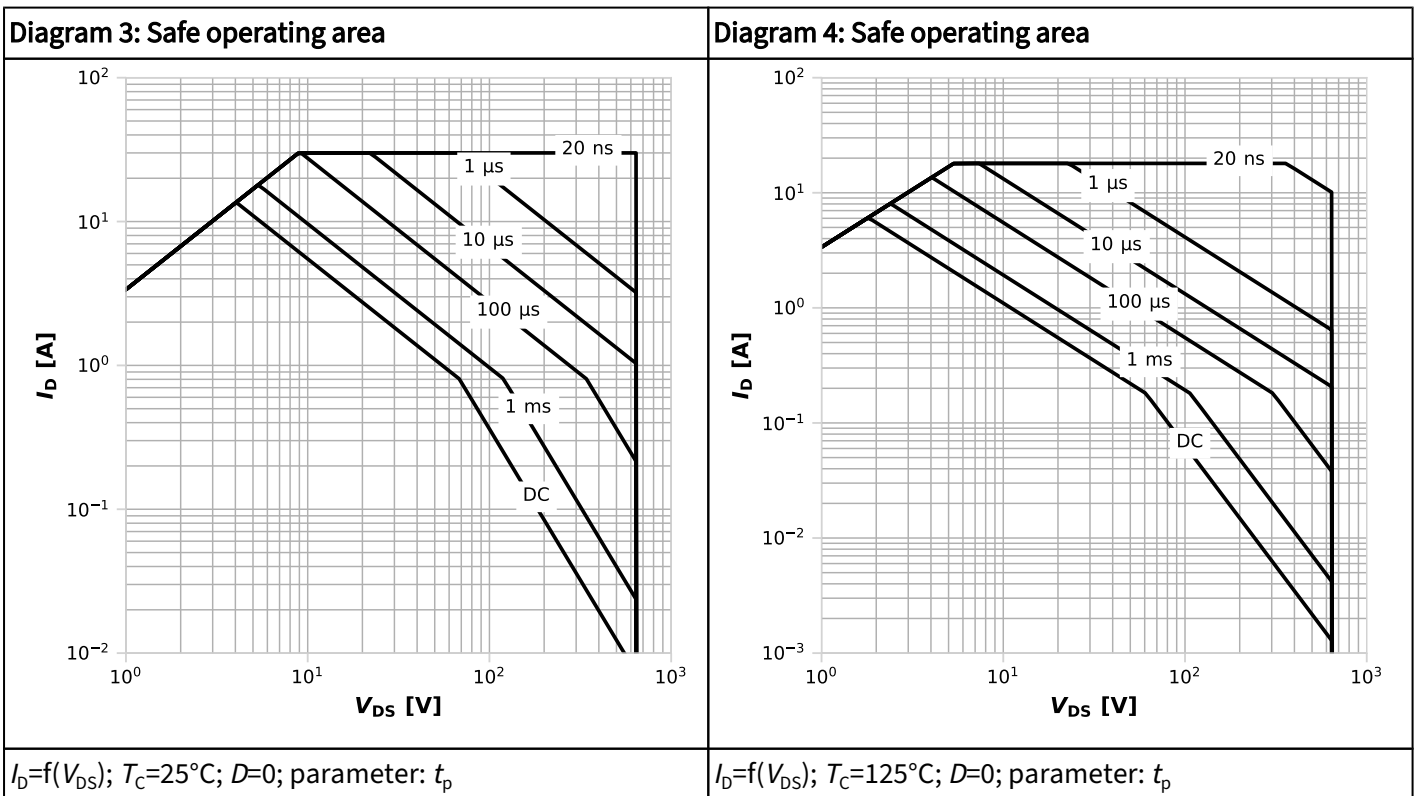
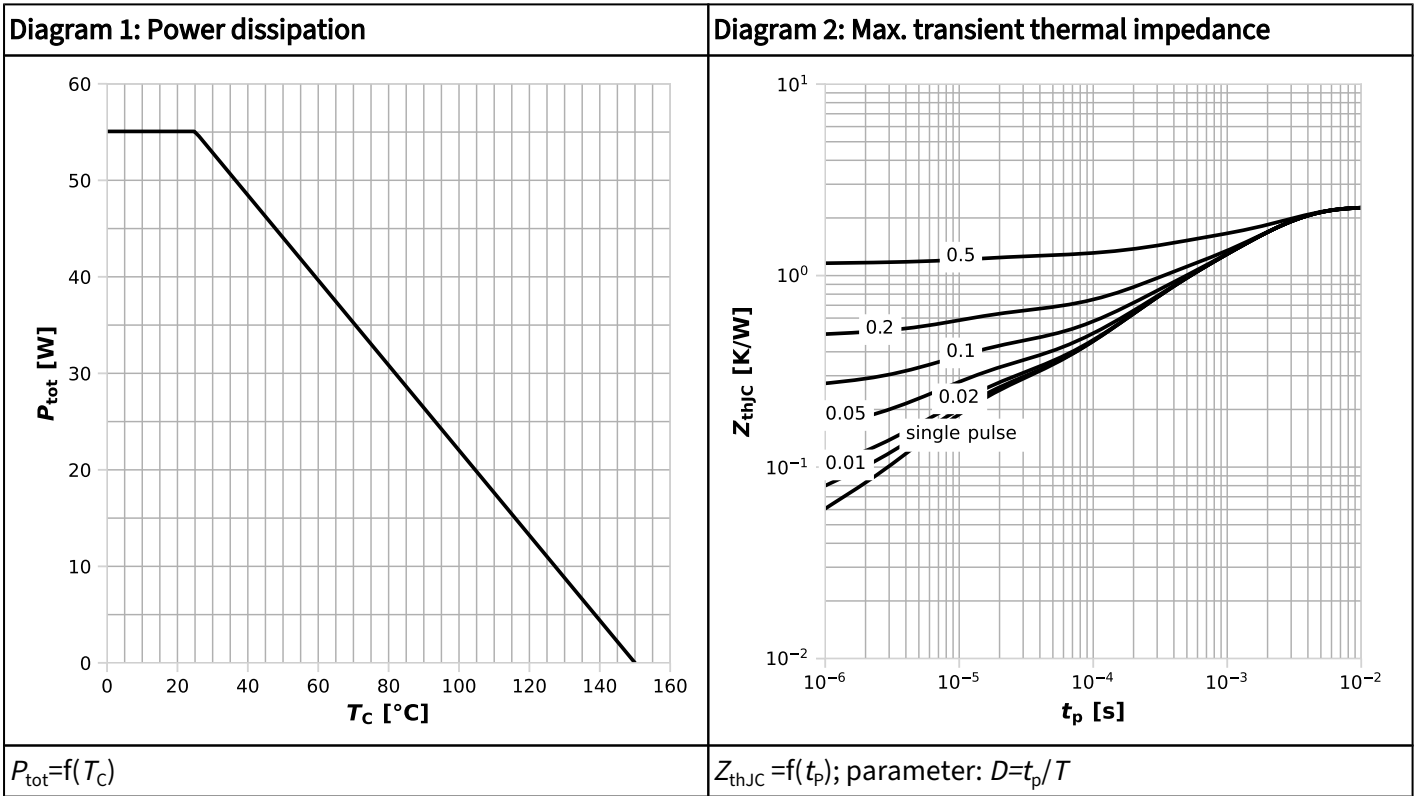
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate charge	$Q_G$	-	2.4	-	nC	$V_{GS}=0$ to 3 V; $V_{DS}=400$ V, $I_D=4.0$ A

**Table 7 Reverse conduction characteristics**

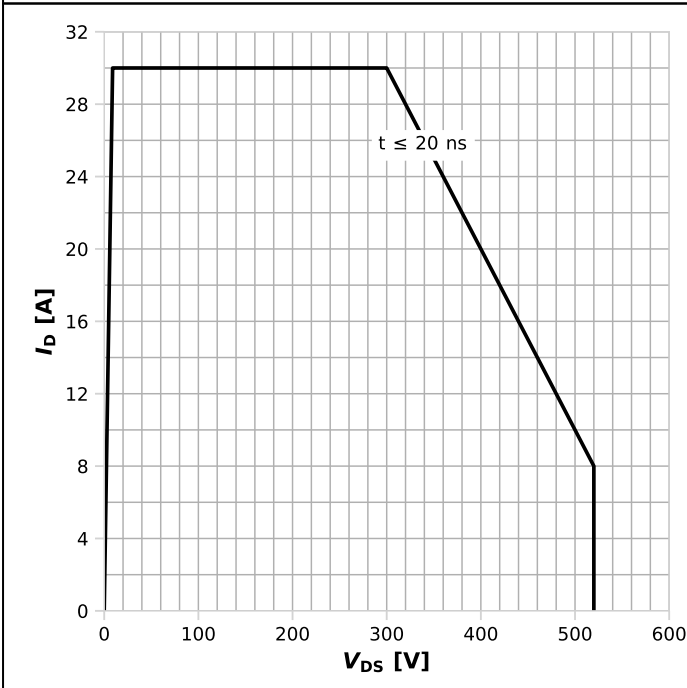
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	$V_{SD}$	-	2.0	2.4	V	$V_{GS}=0$ V; $I_{SD}=4$ A
Pulsed current, reverse	$I_{SD,pulse}$	-	-	30	A	$I_G=13$ mA
Reverse recovery charge <sup>5)</sup>	$Q_{rr}$	-	0	-	nC	$I_{SD}=4$ A; $V_{DS}=400$ V

- <sup>5)</sup> Excluding  $Q_{oss}$

## 4 Electrical characteristics diagrams

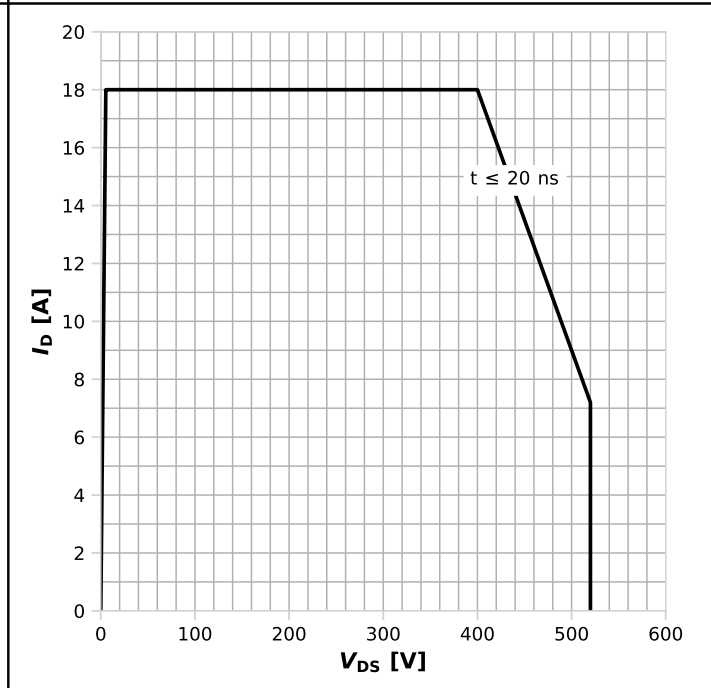


**Diagram 5: Repetitive safe operating area**



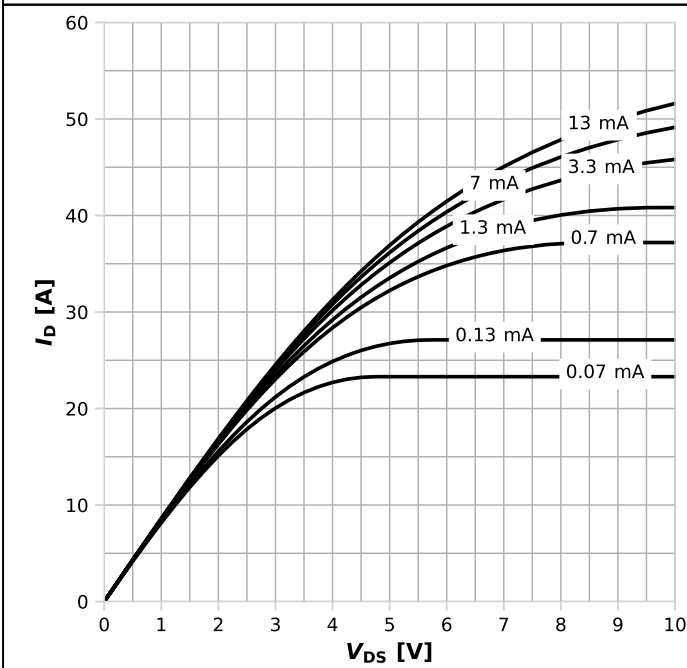
$I_D=f(V_{DS}); T_c=25^\circ\text{C}; T_j \leq 150^\circ\text{C}$ ; parameter:  $t_p$

**Diagram 6: Repetitive safe operating area**



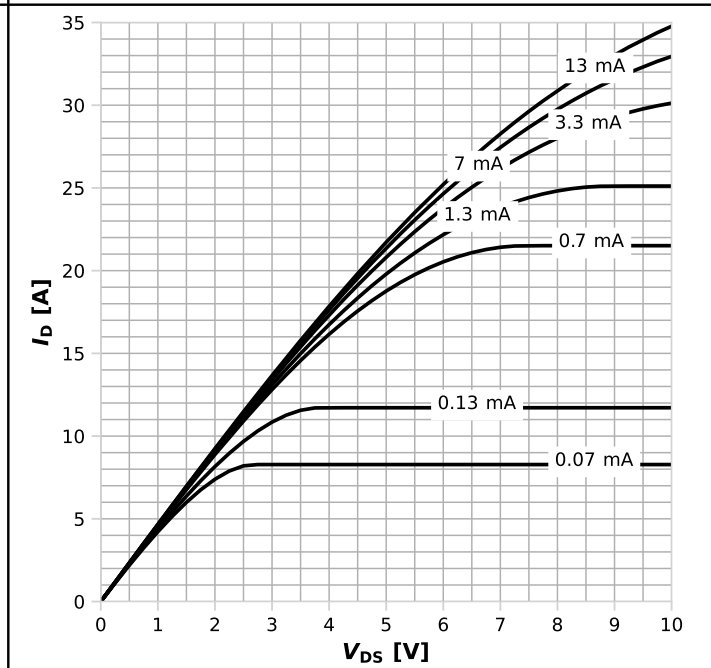
$I_D=f(V_{DS}); T_c=125^\circ\text{C}; T_j \leq 150^\circ\text{C}$ ; parameter:  $t_p$

**Diagram 7: Typ. output characteristics**



$I_D=f(V_{DS}); T_j=25^\circ\text{C}$ ; parameter:  $I_{GS}$

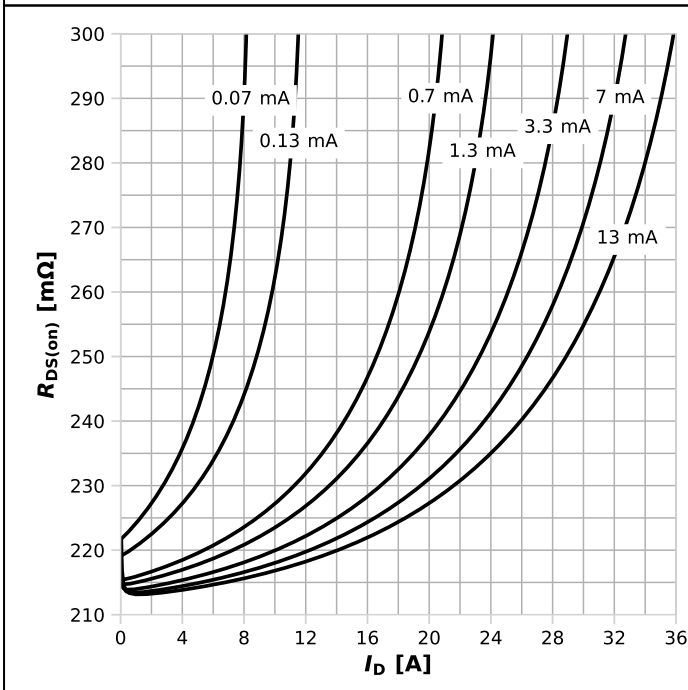
**Diagram 8: Typ. output characteristics**



$I_D=f(V_{DS}); T_j=125^\circ\text{C}$ ; parameter:  $I_{GS}$

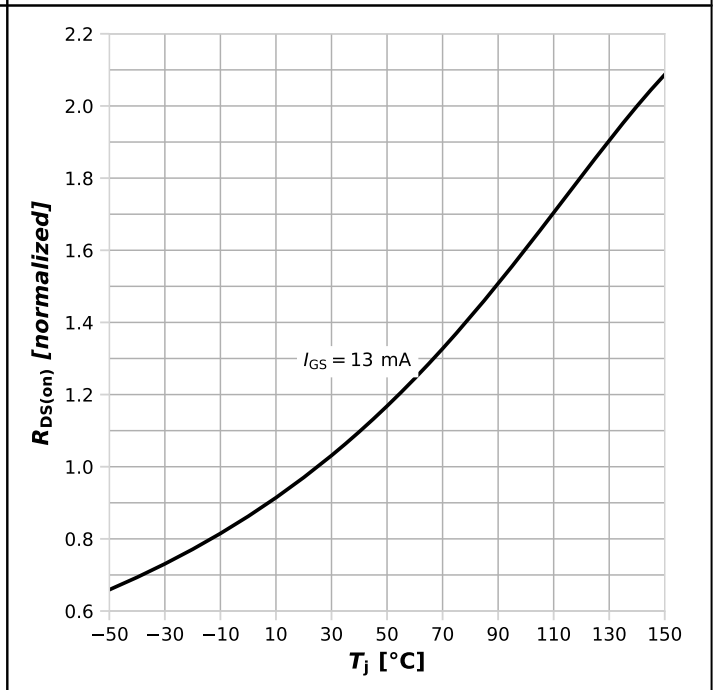


Diagram 9: Typ. Drain-source on-state resistance



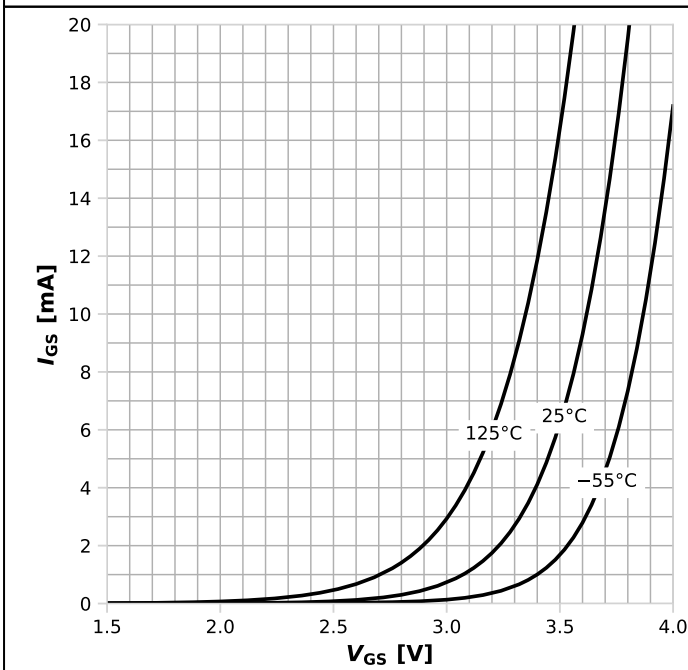
$R_{DS(on)}=f(I_D); T_j=125^\circ\text{C}; \text{parameter: } I_{GS}$

Diagram 10: Drain-source on-state resistance



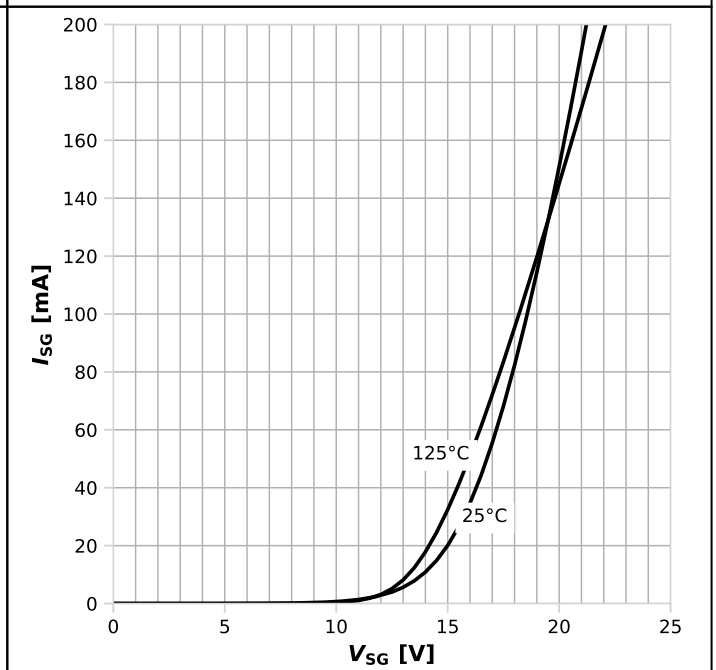
$R_{DS(on)}=f(T_j); I_D=4.0 \text{ A}$

Diagram 11: Typ. gate characteristics forward



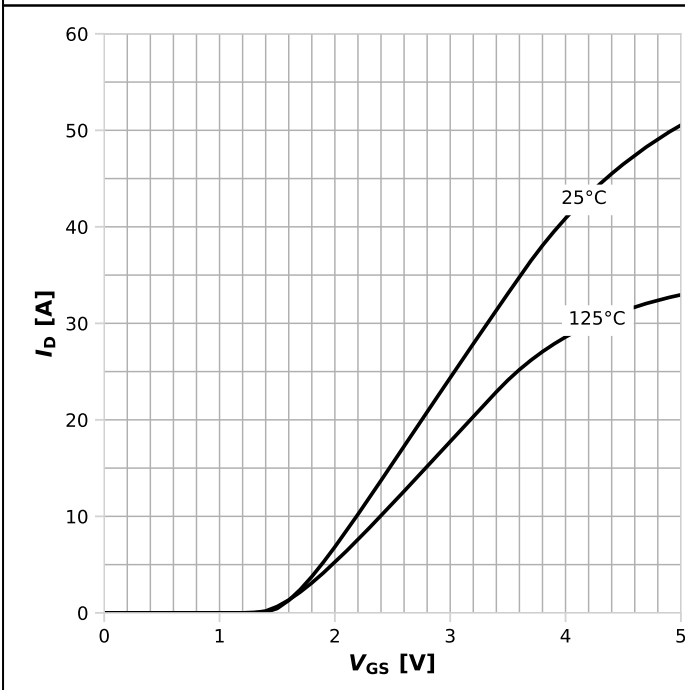
$I_{GS}=f(V_{GS}); \text{open drain}; \text{parameter: } T_j$

Diagram 12: Typ. gate characteristics reverse



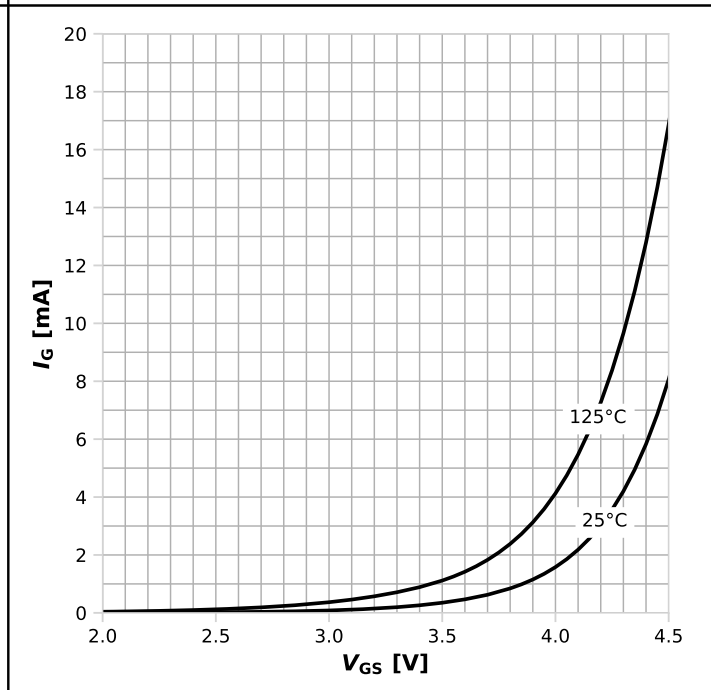
$I_{SG}=f(V_{SG}); \text{parameter: } T_j$

Diagram 13: Typ. transfer characteristics



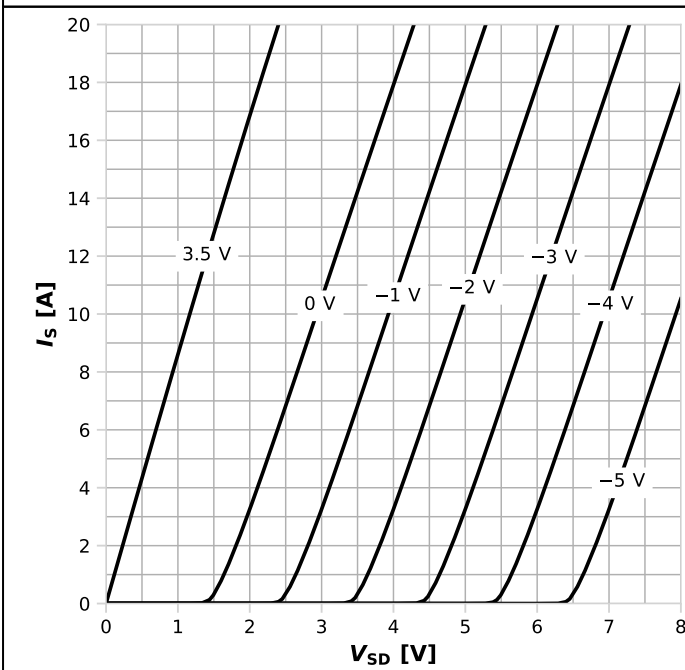
$I_D = f(V_{GS}); V_{DS} = 8V; \text{parameter: } T_j$

Diagram 14: Typ. transfer gate current characteristic



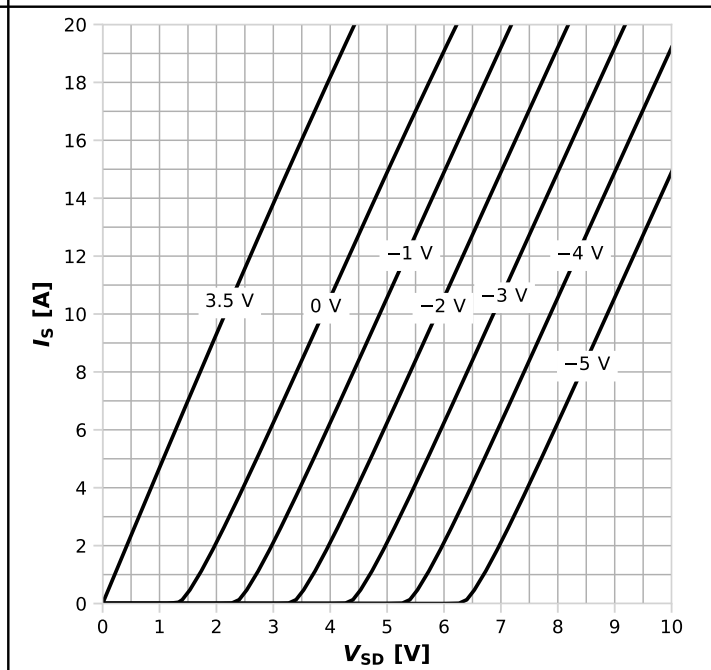
$I_G = f(V_{GS}); V_{DS} = 8V; \text{parameter: } T_j$

Diagram 15: Typ. channel reverse characteristics

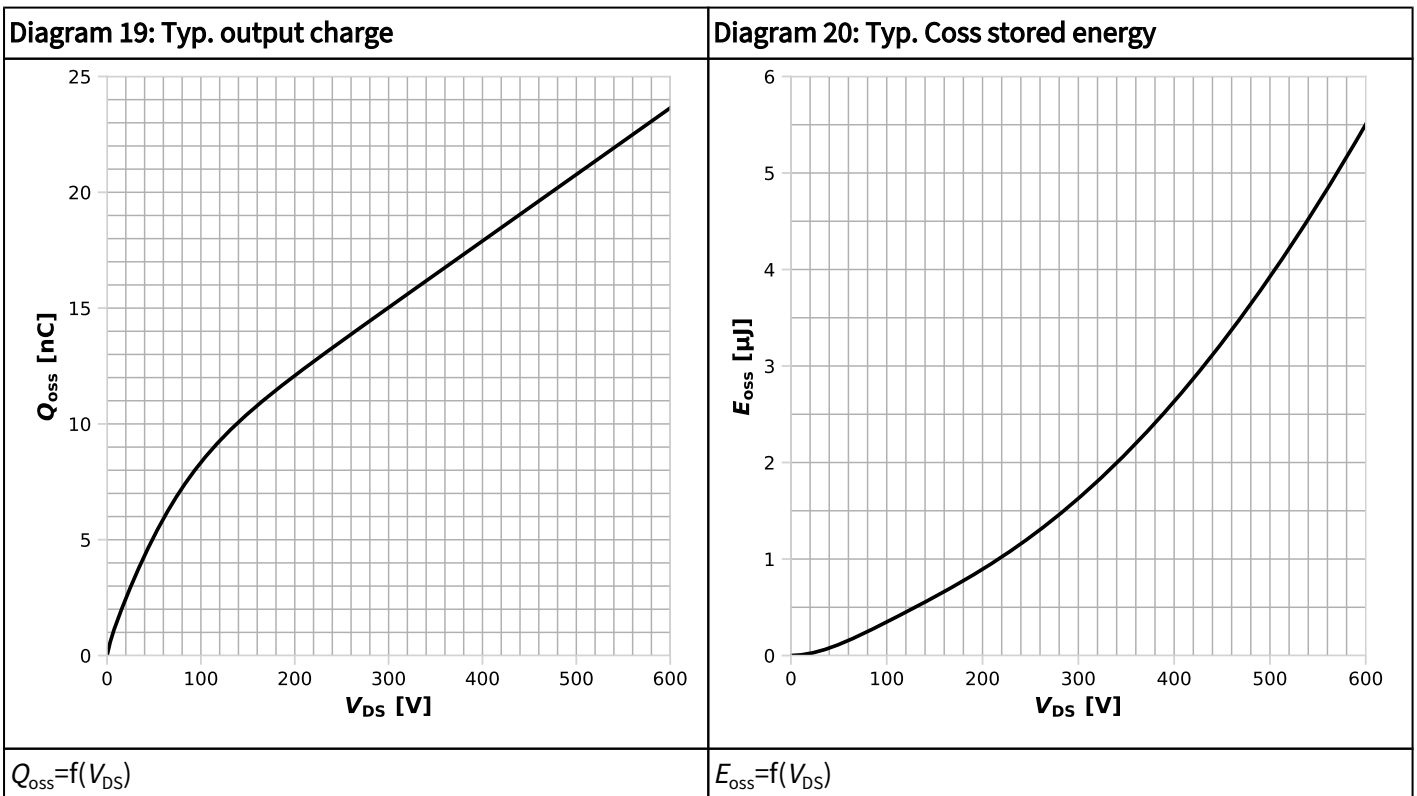
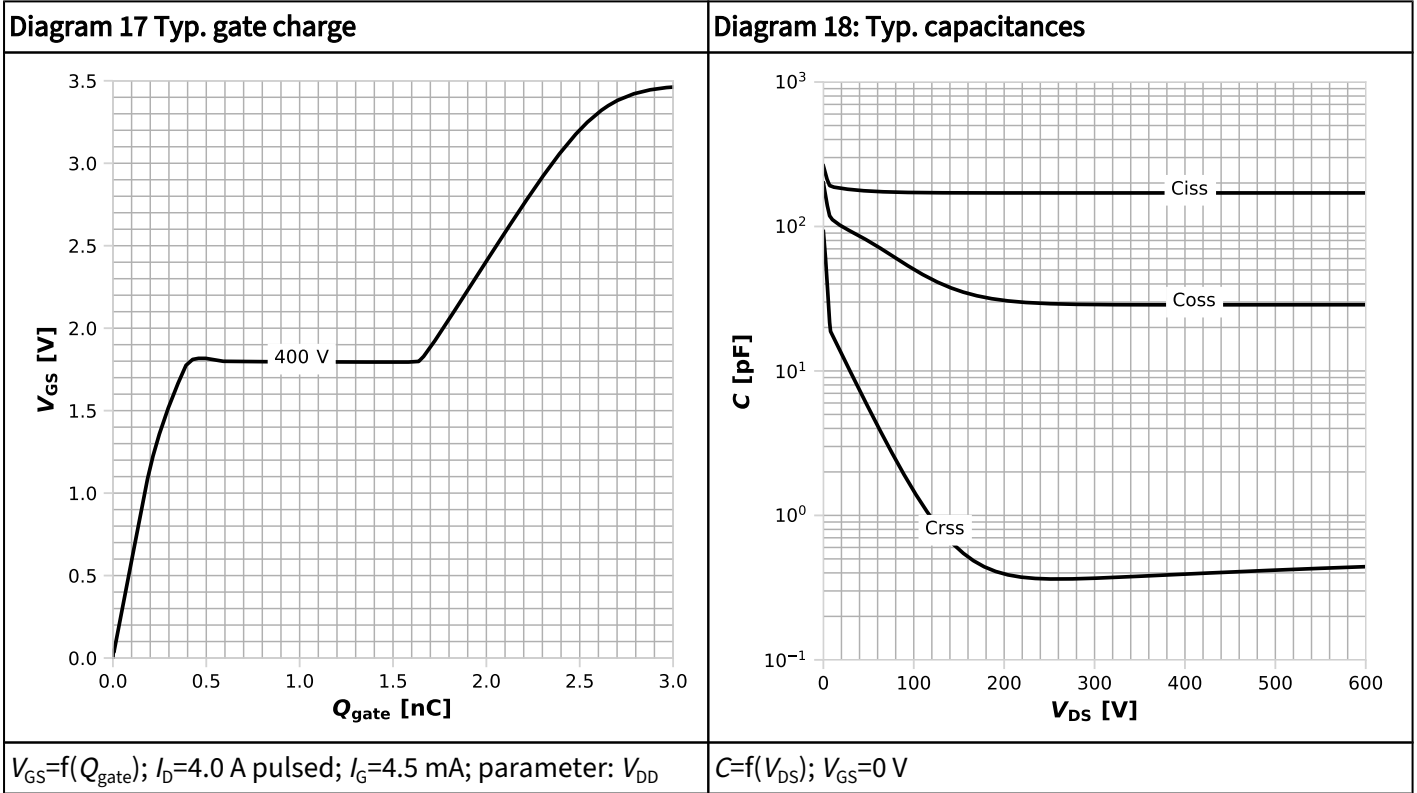


$I_S = f(V_{SD}); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 16: Typ. channel reverse characteristics

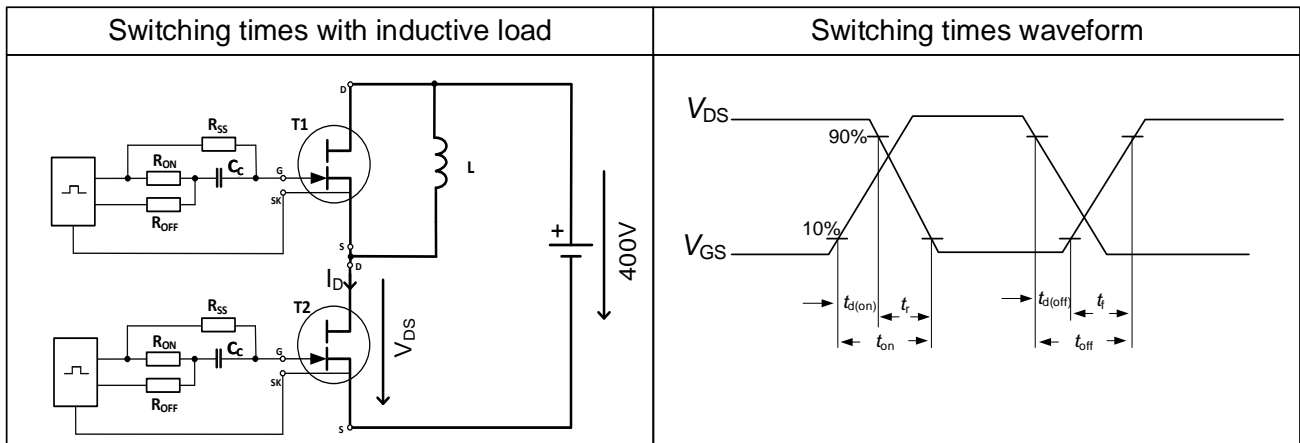


$I_S = f(V_{SD}); T_j = 125^\circ\text{C}; \text{parameter: } V_{GS}$

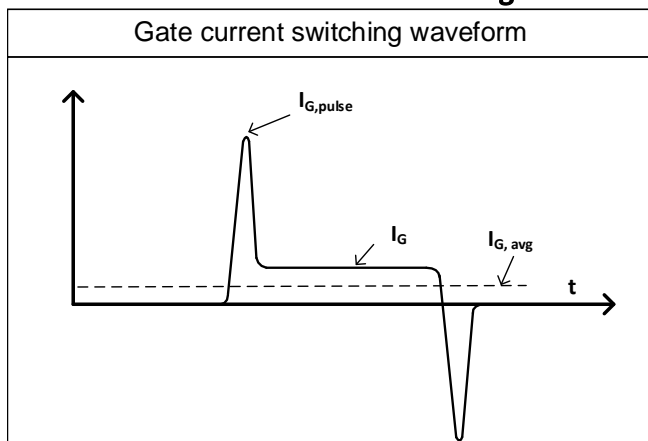


## 5 Test circuits

**Table 8 Reverse channel characteristics test**



**Table 9 Gate current switching waveform**



## 6 Package outlines

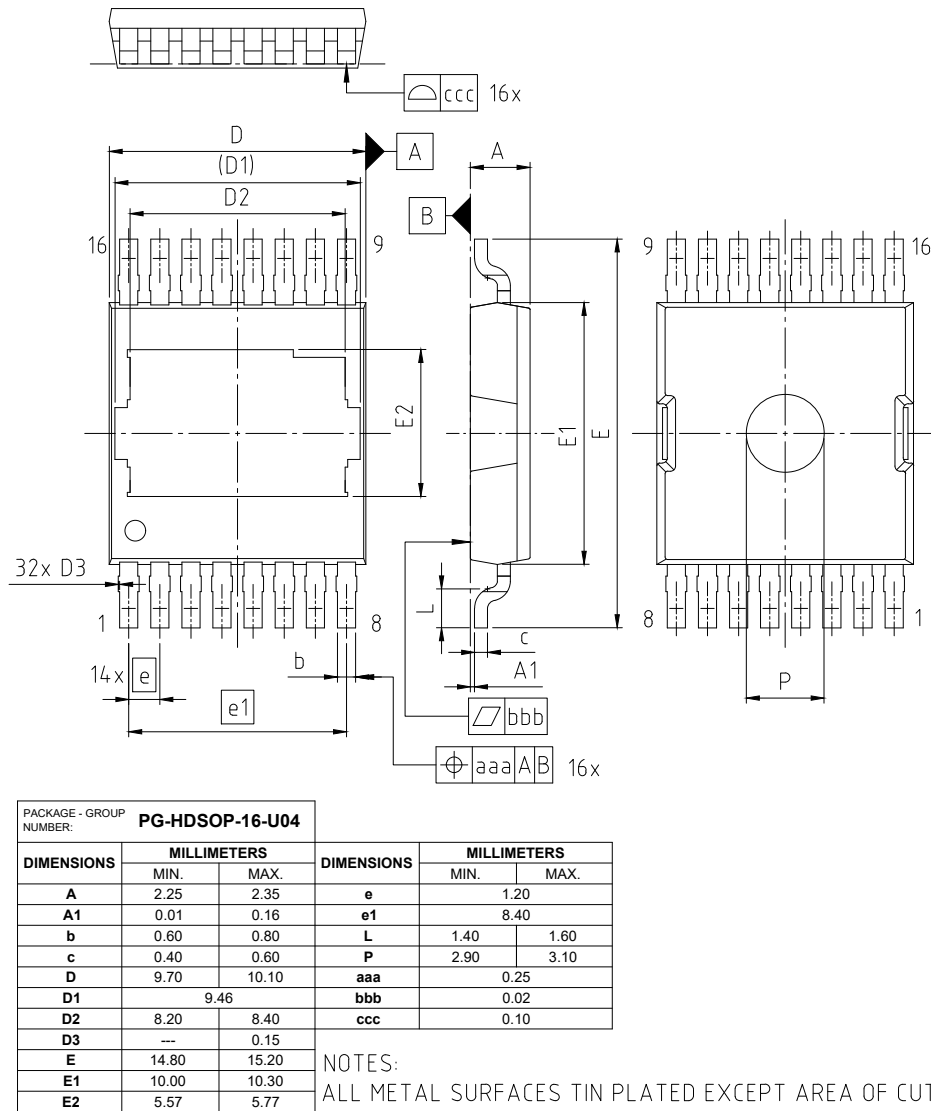
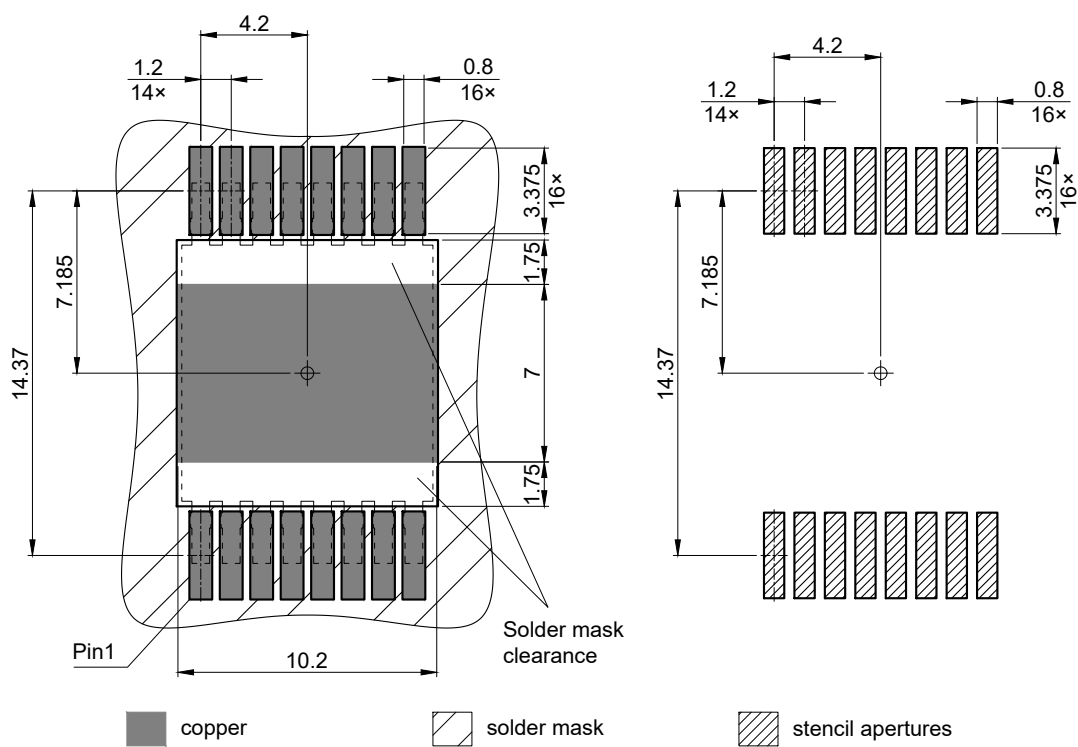
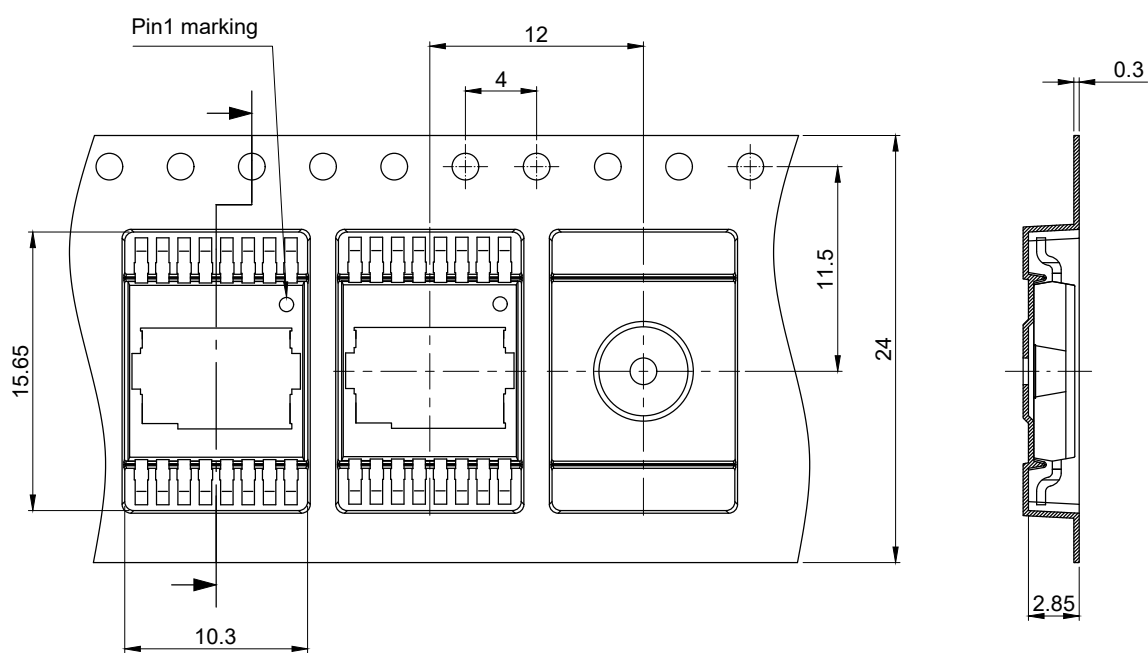


Figure 1 Outline PG-HDSOP-16, dimensions in mm



All dimensions are in units mm  
 Based on stencil thickness 0.2 mm  
 All pads are non-solder mask defined

**Figure 2 Footprint drawing PG-HDSOP-16, dimensions in mm**



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

**Figure 3** Packaging variant PG-HDSOP-16, dimensions in mm

## 7 Appendix A

Table 10 Related links

- [CoolGaN™ GaN 650 V webpage](#)
- [CoolGaN™ GaN 650 V reliability white paper](#)
- [CoolGaN™ GaN 650 V gate driver application note](#)
- [CoolGaN™ GaN 650 V applications information](#)



## Revision history

IGLT65R110D2

### Revision 2024-10-29, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2024-10-29	Release of final

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