RAMXEED

DS501-00097-2v0-E

*Memory FeRAM*

RAMXEED ULTIMATE

# 1M (128 K × 8) Bit I²C

# MS85RC1MTY

## ■ DESCRIPTION

The MS85RC1MTY is an FeRAM (Ferroelectric Random Access Memory) chip in a configuration of 131,072 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

Unlike SRAM, the MS85RC1MTY is able to retain data without using a data backup battery.

The read/write endurance of the nonvolatile memory cells used for the MS85RC1MTY has improved to be at least $10^{13}$ cycles, significantly outperforming other nonvolatile memory products in the number.

The MS85RC1MTY does not need a polling sequence after writing to the memory such as the case of Flash memory or $E^2$PROM.

## ■ FEATURES

- Bit configuration : 131,072 words × 8 bits
- Two-wire serial interface : Fully controllable by two ports: serial clock (SCL) and serial data (SDA).
- Operating frequency : 3.4 MHz (Max @HIGH SPEED MODE)
  1 MHz (Max @FAST MODE PLUS)
- Read/write endurance : $10^{13}$ times ( + 125 °C)
  $10^{14}$ times ( + 85 °C)
- Data retention : 193.9 years ( + 85 °C),
  40.7 years ( + 105 °C),
  10.1 years ( + 125 °C)
- Operating power supply voltage : 1.8 V to 3.6 V
- Low-power consumption : Operating power supply current 0.24mA (Typ @3.4 MHz)
  0.4 mA (Max @3.4 MHz)
  Standby current 12μA (Typ), 150μA (Max)
  Sleep current 0.3μA (Typ), 16μA (Max)
- Operation ambient temperature range
  : − 40 °C to + 125 °C
- Package : 8-pin plastic SOP (150mil)
  8-pin plastic DFN (5mm × 6mm)
  RoHS compliant

Fujitsu Semiconductor Memory Solutions Limited has changed its name to RAMXEED Limited. RAMXEED Limited will continue to offer and support existing products while maintaining Fujitsu's part number unchanged.

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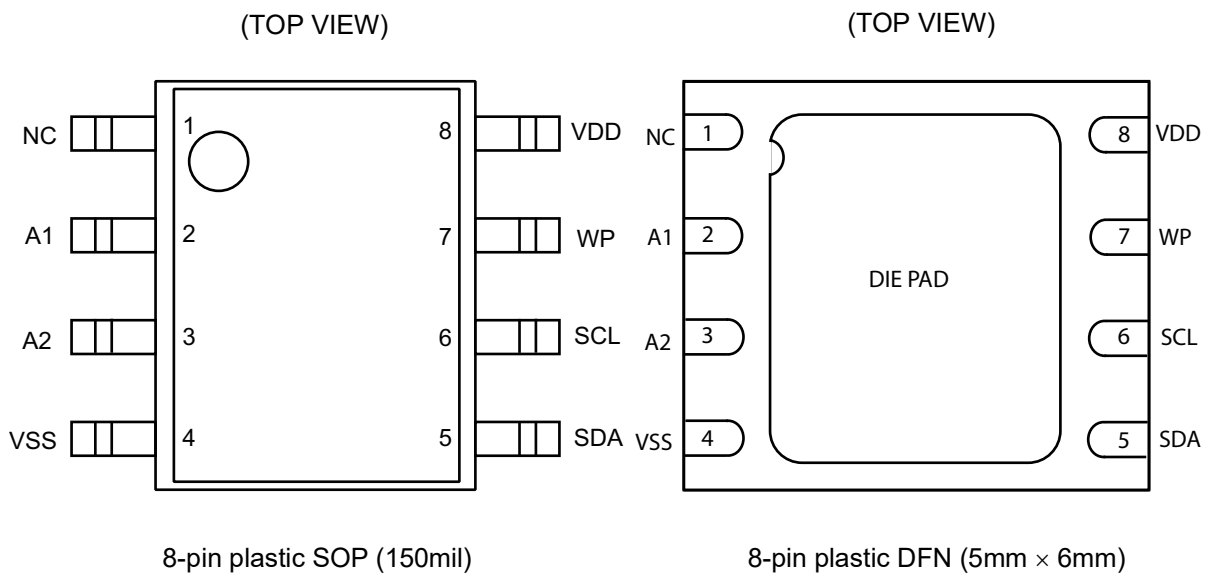
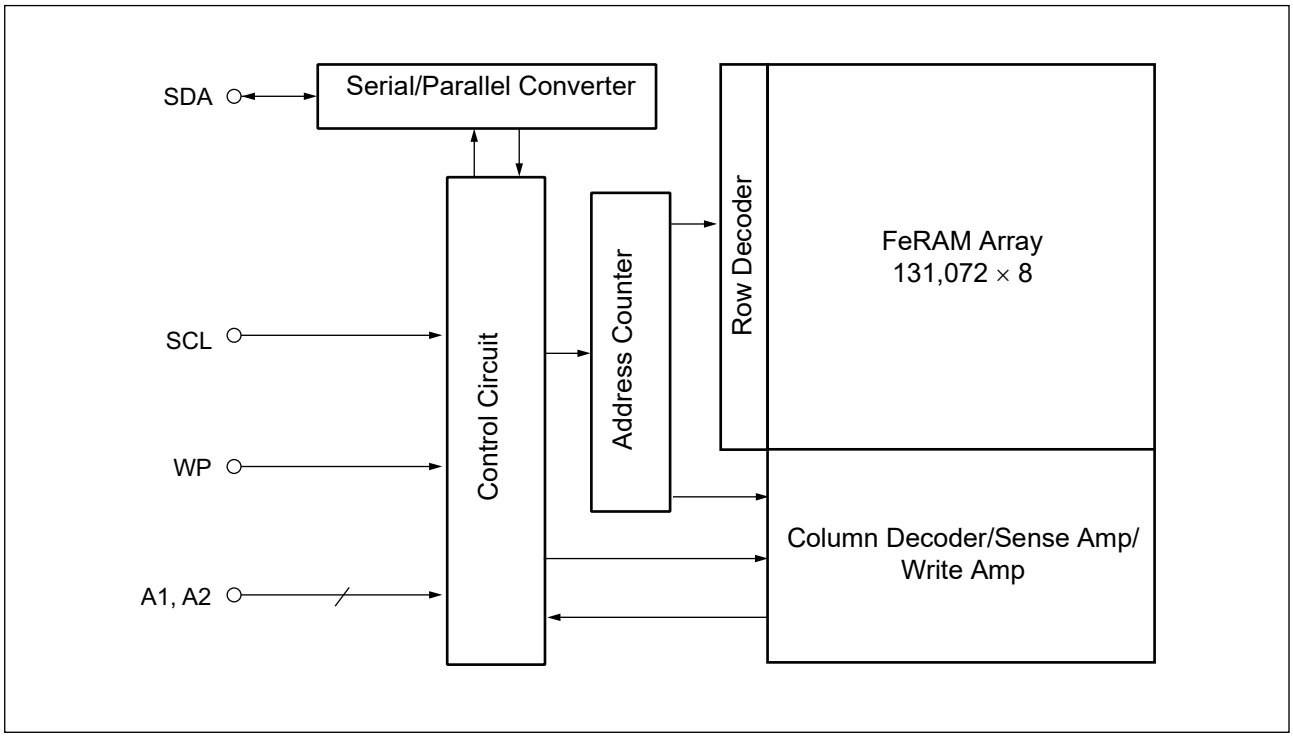
## ■ PIN ASSIGNMENT




## ■ PIN FUNCTIONAL DESCRIPTIONS

| Pin Number | Pin Name | Functional Description |
|---|---|---|
| 1 | NC | Not used. Floating or connect to VDD or VSS. |
| 2 to 3 | A1 to A2 | Device Address pins<br>The MS85RC1MTY can be connected to the same data bus up to 4 devices. Device addresses are used in order to identify each of these devices. Connect these pins to VDD pin or VSS pin externally. Only if the combination of VDD and VSS pins matches Device Address Code inputted from the SDA pin, the device operates. In the open pin state, A1 and A2 pins are internally pulled-down and recognized as the "L" level. |
| 4 | VSS | Ground pin |
| 5 | SDA | Serial Data I/O pin<br>This is an I/O pin which performs bidirectional communication for both memory address and writing/reading data. It is possible to connect multiple devices. It is an open drain output, so a pull-up resistor is required to be connected to the external circuit. |
| 6 | SCL | Serial Clock pin<br>This is a clock input pin for input/output serial data. Data is sampled on the rising edge of the clock and output on the falling edge. |
| 7 | WP | Write Protect pin<br>When the Write Protect pin is the “H” level, the writing operation is disabled. When the Write Protect pin is the “L” level, the entire memory region can be overwritten. The reading operation is always enabled regardless of the Write Protect pin input level. The Write Protect pin is internally pulled down to VSS pin, and that is recognized as the “L” level (write enabled) when the pin is the open state. |
| 8 | VDD | Supply Voltage pin |

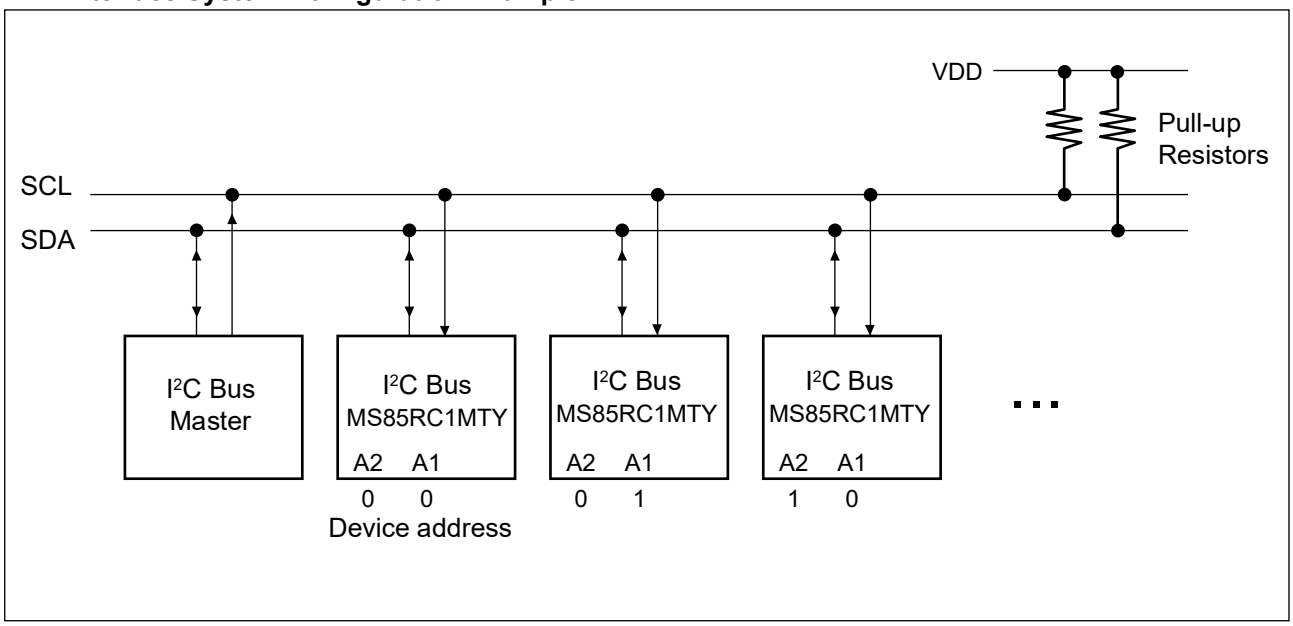
## ■ BLOCK DIAGRAM




## ■ I²C (Inter-Integrated Circuit)

The MS85RC1MTY has the two-wire serial interface; the I²C bus, and operates as a slave device. The I²C bus defines communication roles of “master” and “slave” devices, with the master side holding the authority to initiate control. Furthermore, the I²C bus connection is possible where a single master device is connected to multiple slave devices in a party-line configuration. In this case, it is necessary to assign a unique device address to the slave device, the master side starts communication after specifying the slave to communicate by addresses.

- **I²C Interface System Configuration Example**



## ■ I²C COMMUNICATION PROTOCOL

The I²C bus is a two wire serial interface that uses a bidirectional data bus (SDA) and serial clock (SCL). A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The SDA signal should change while the SCL is the “L” level. However, as an exception, when starting and stopping communication sequence, the SDA is allowed to change while the SCL is the “H” level.

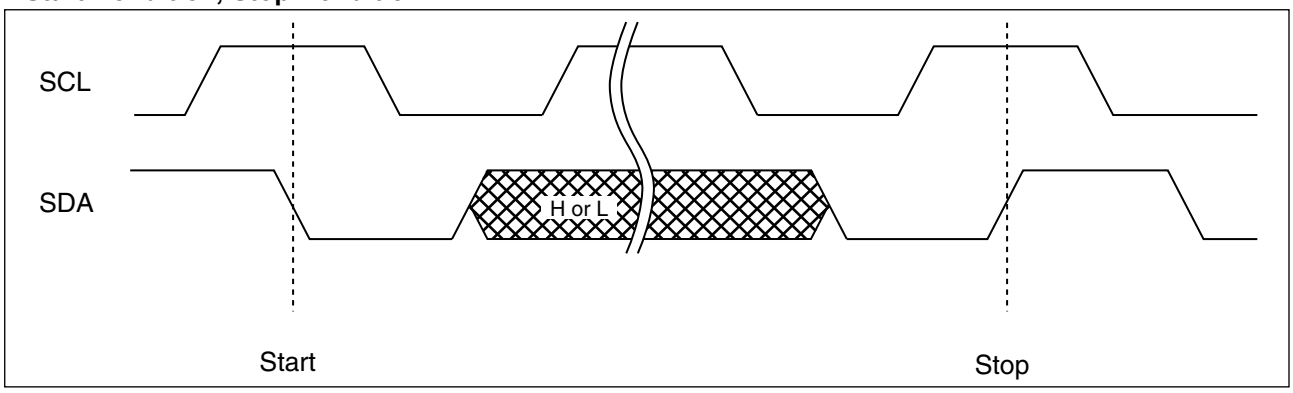
- Start Condition

To start read or write operations by the I²C bus, change the SDA input from the “H” level to the “L” level while the SCL input is in the “H” level.

- Stop Condition

To stop the I²C bus communication, change the SDA input from the “L” level to the “H” level while the SCL input is in the “H” level. In the reading operation, inputting the stop condition finishes reading and enters the standby state. In the writing operation, inputting the stop condition finishes inputting the rewrite data and enters the standby state.

**• Start Condition, Stop Condition**



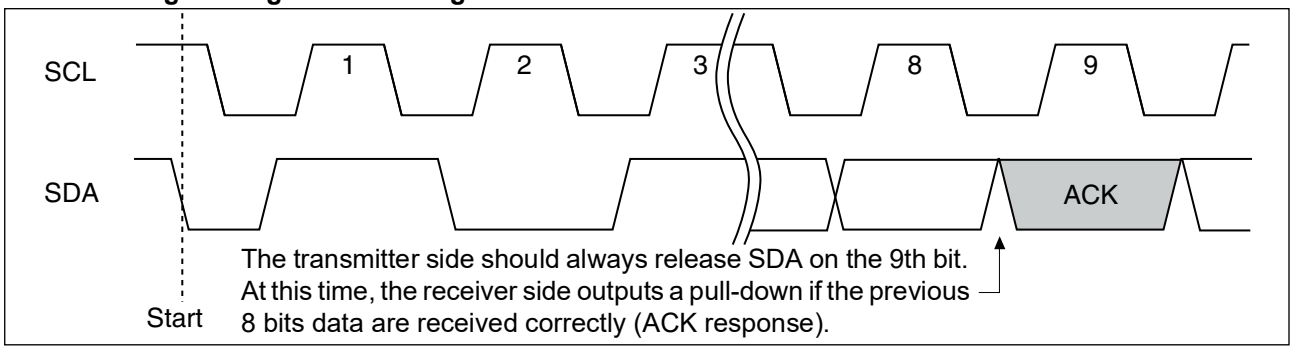

Note : At the write operation, the FeRAM device does not need the programming wait time ($t_{WC}$) after issuing the Stop Condition.

## ■ ACKNOWLEDGE (ACK)

In the I²C bus, serial data including memory address or memory information is sent and received in units of 8 bits. The acknowledge signal indicates that every 8 bits of the data is successfully sent and received. The receiver side usually outputs the “L” level every time on the 9th SCL clock after each 8 bits are successfully transmitted and received. On the transmitter side, the bus is temporarily released to Hi-Z every time on this 9th clock to allow the acknowledge signal to be received and checked. During this Hi-Z released period, the receiver side pulls the SDA line down to indicate the “L” level that the previous 8 bits communication is successfully received.

In case the slave side receives Stop condition before sending or receiving the ACK “L” level, the slave side stops the operation and enters to the standby state. On the other hand, the slave side releases the bus state after sending or receiving the NACK “H” level. The master side generates Stop condition or Start condition in this released bus state.

**• Acknowledge timing overview diagram**



## ■ DEVICE ADDRESS WORD (Slave address)

Following the start condition, the master inputs the 8 bits device address word to start I²C communication. The device address word (8 bits) consists of a device Type code (4 bits), device address code (2 bits), MSB(1bit) and a read/write code (1 bit).

- Device Type Code (4 bits)

The upper 4 bits of the device address word are a device type code that identifies the device type, and are fixed at “1010” for the MS85RC1MTY.

- Device Address Code (2 bits)

Following the device type code, the 2 bits of the device address code are input in order of A2 and A1. The device address code identifies one device from up to four devices connected to the bus. Each MS85RC1MTY is given a unique 2 bits code on the device address pin (external hardware pin A2 and A1). The slave only responds if the received device address code is equal to this unique 2 bits code.

- The most significant address(1 bit)

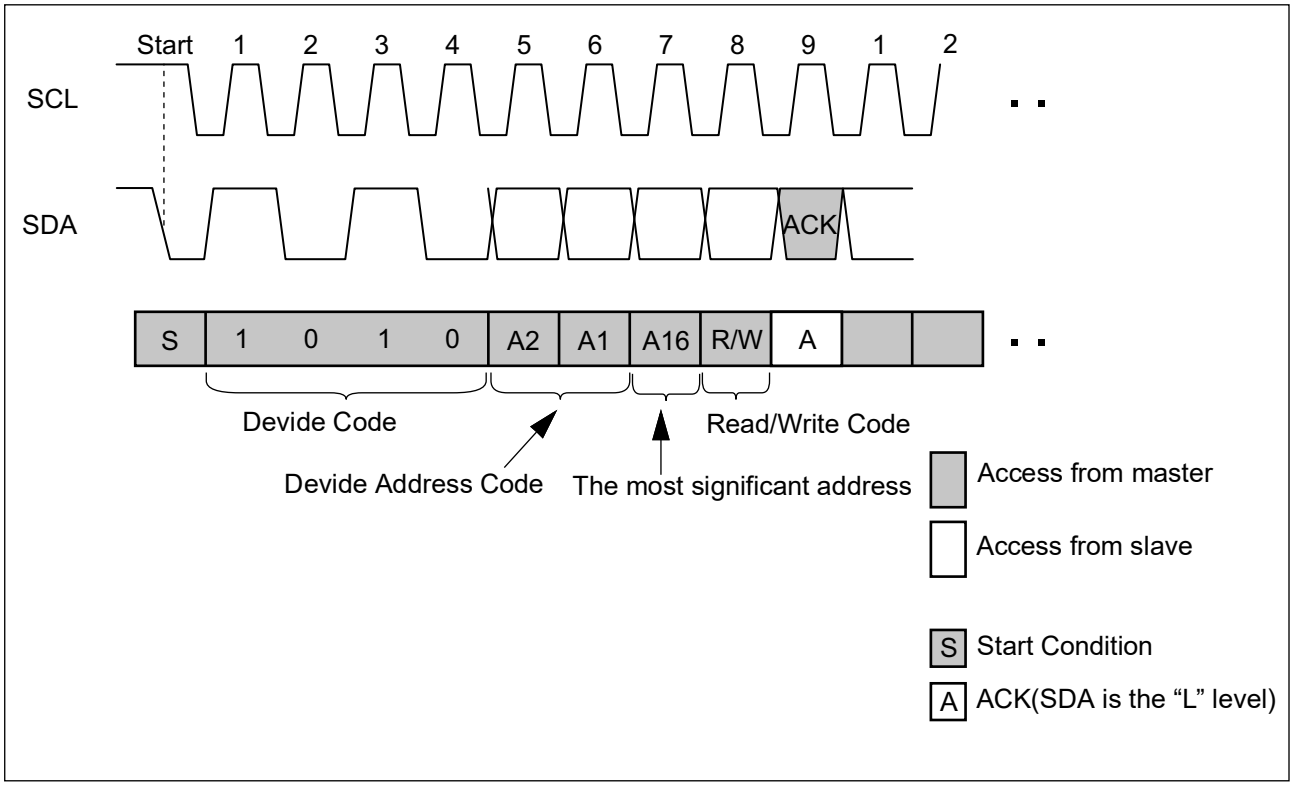
The seventh bit of device address word is A16(1 bit) that is the most significant address.

- Read/Write Code (1 bit)

The 8th bit of the device address word is the R/W (read/write) code. When the R/W code is “0”, a write operation is enabled, and the R/W code is “1”, a read operation is enabled for the MS85RC1MTY.

It turns to a stand-by state if the device code is not “1010” or device address code does not equal to pin A2 and A1.

**• Device Address Word**



## ■ DATA STRUCTURE

In the I²C bus, the acknowledge “L” level is output on the 9th bit by a slave, after the 8 bits of the device address word following the start condition are input by a master. After confirming the acknowledge response by the master, the master outputs remained 8 bits × 2 memory address to the slave. When the each memory address input ends, the slave again outputs the acknowledge “L” level. After this operation, the I/O data follows in units of 8 bits, with the acknowledge “L” level output after every 8 bits.

It is determined by the R/W code whether the data line is driven by the master or the slave. However, the clock line shall be driven by the master. For a write operation, the slave will accept 8 bits from the master, then send an acknowledge. If the master detects the acknowledge, the master will transfer the next 8 bits. For a read operation, the slave will place 8 bits on the data line, then wait for an acknowledge from the master.

## ■ FeRAM ACKNOWLEDGE -- POLLING NOT REQUIRED

The MS85RC1MTY performs the high speed write operations, so any waiting time for an ACK polling* does not occur.

*: In E²PROM, the Acknowledge Polling is performed as a progress check whether rewriting is executed or not. It is normal to judge by the 9th bit of Acknowledge whether rewriting is performed or not after inputting the start condition and then the device address word (8 bits) during rewriting.

## ■ WRITE PROTECT (WP)

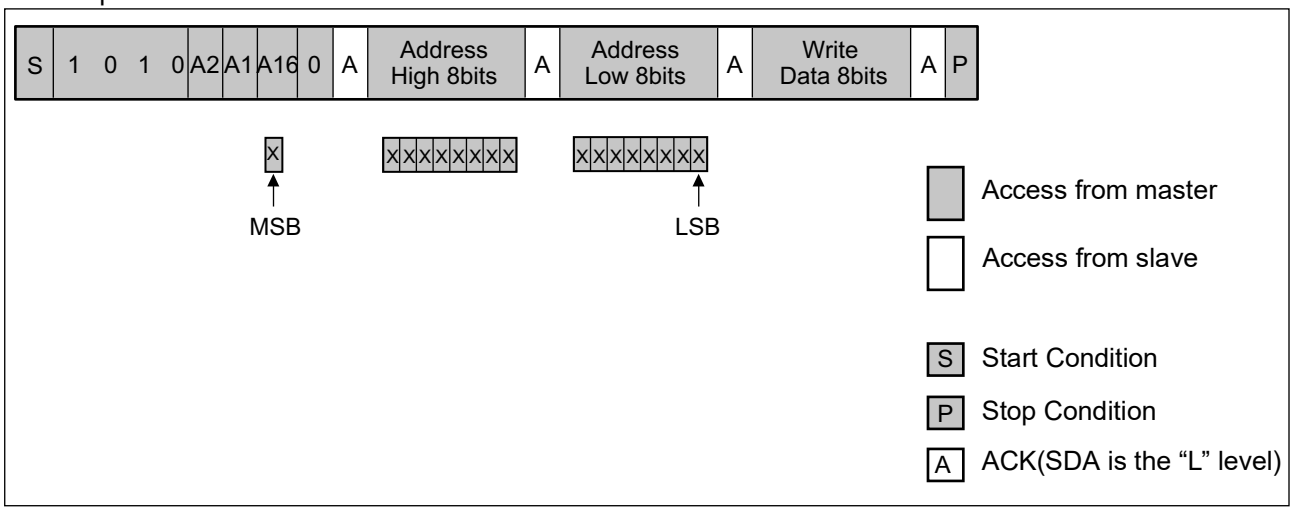
The entire memory array can be write protected using the Write Protect pin. When the Write Protect pin is set to the “H” level, the entire memory array will be write protected. When the Write Protect pin is the “L” level, the entire memory array will be rewritten. Reading is allowed regardless of the WP pin's “H” level or “L” level.

Note : The Write Protect pin is pulled down internally to the VSS pin, therefore if the Write Protect pin is open, the pin status is detected as the “L” level (write enabled).

## ■ COMMAND

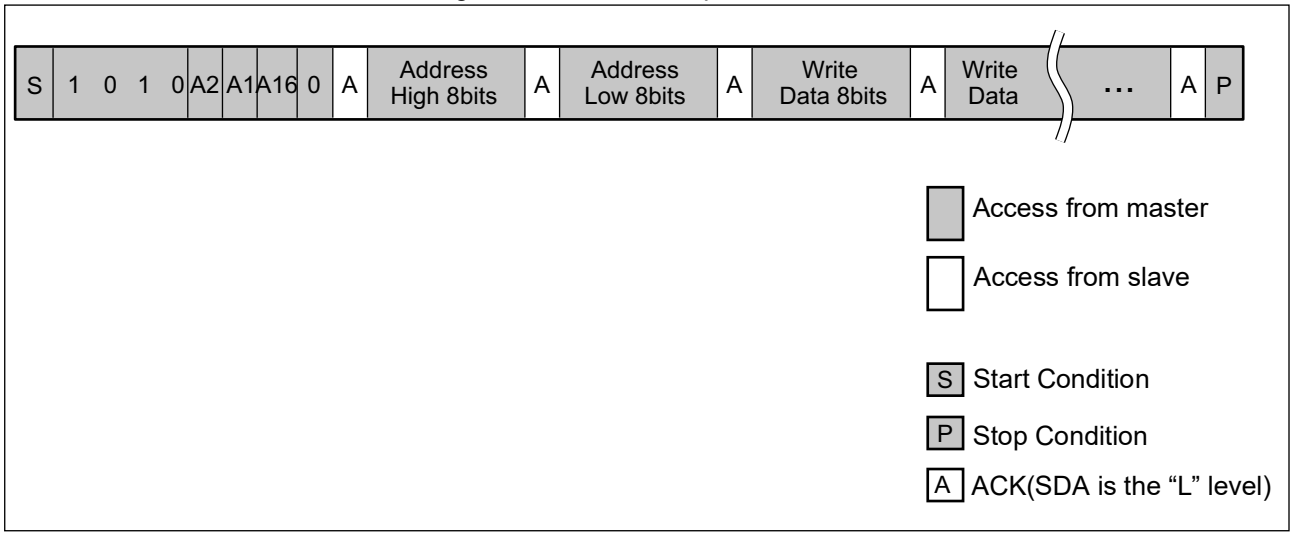
- Byte Write

If the device address word (R/W “0” input) is sent following the start condition, the slave responds with an ACK. After this ACK, write addresses and data are sent in the same way, and the write ends by generating a stop condition at the end.




- Page Write

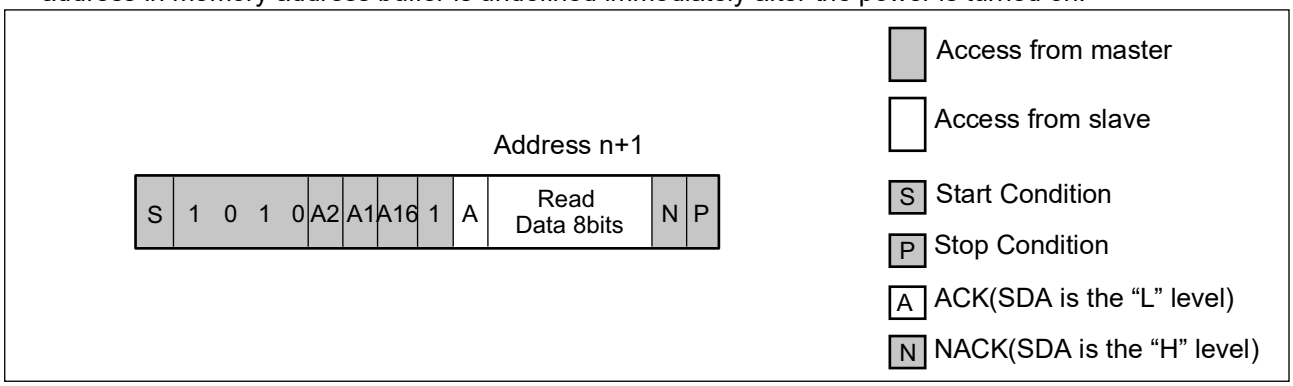
If additional 8 bits are continuously sent after the same command (except stop condition) as Byte Write, a page write is performed. The memory address rolls over to first memory address (0 0000H) at the end of the address. Therefore, if more than 128K bytes are sent, the data is overwritten in order starting from the start of the memory address that was written first. Because FeRAM performs the high-speed write operations, the data will be written to FeRAM right after the ACK response finished.




Note: It is not necessary to take a period for internal write operation cycles from the buffer to the memory after the stop condition is generated.

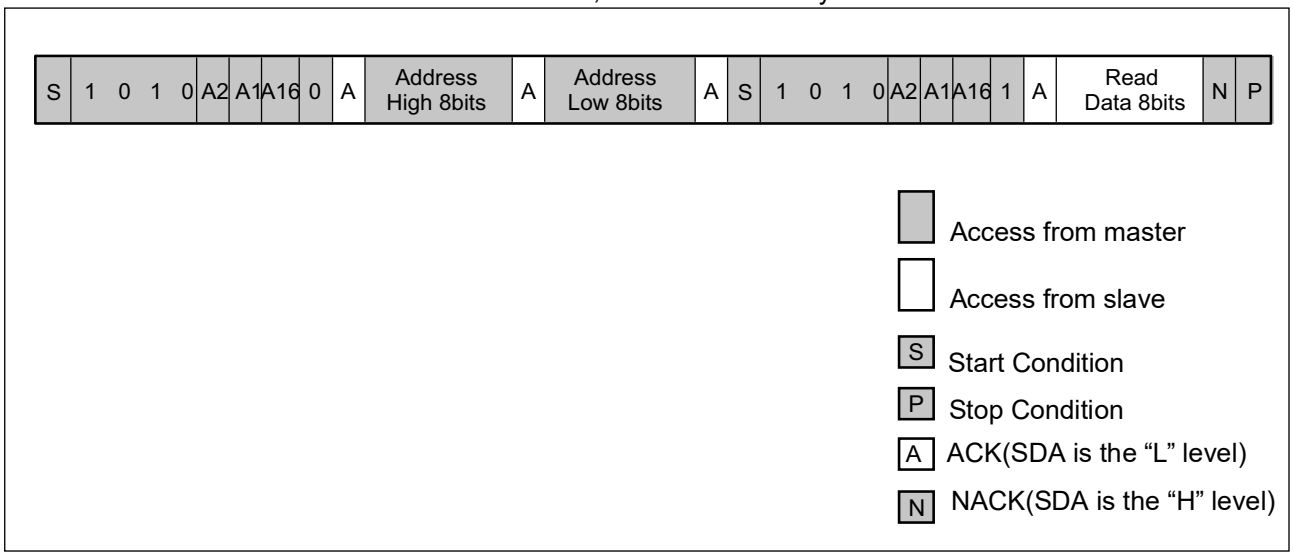
- Current Address Read

When the previous write or read operation finishes successfully up to the stop condition, the memory address accessed last time is remain in memory address buffer(17bits). As it is, then send the command without turning off the power, the memory address "n", total 17 bits consist of the 1 bit of the top memory address from the Device Address Word input and lower 16 bits of memory address buffer, is read from the address "n+1". If the memory address “n” is last address, the address counter will roll over to ($0000_H$). The current address in memory address buffer is undefined immediately after the power is turned on.



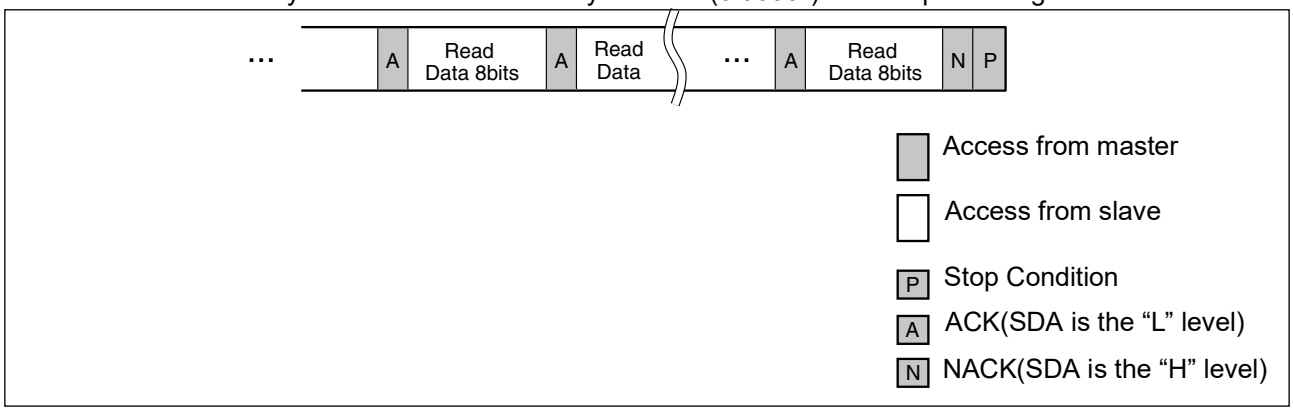

- Random Read

The one byte of data from the memory address saved in the memory address buffer can be read out synchronously to SCL by specifying the address in the same way as for a write, and then issuing another start condition and sending the Device Address Word (R/W “1” input). The top address input at second time need to same value as top address inputed first time. If input the different value at first time and second time, the second value is reflected as the address to access. The final NACK (SDA is the “H” level) is issued by the receiver that receives the data. In this case, this bit is issued by the master side.



- Sequential Read

Data can be received continuously following the Device address word (R/W “1” input) after specifying the address in the same way as for Random Read. If the read reaches the end of address, the internal read address automatically rolls over to first memory address (0 0000H) and keeps reading.

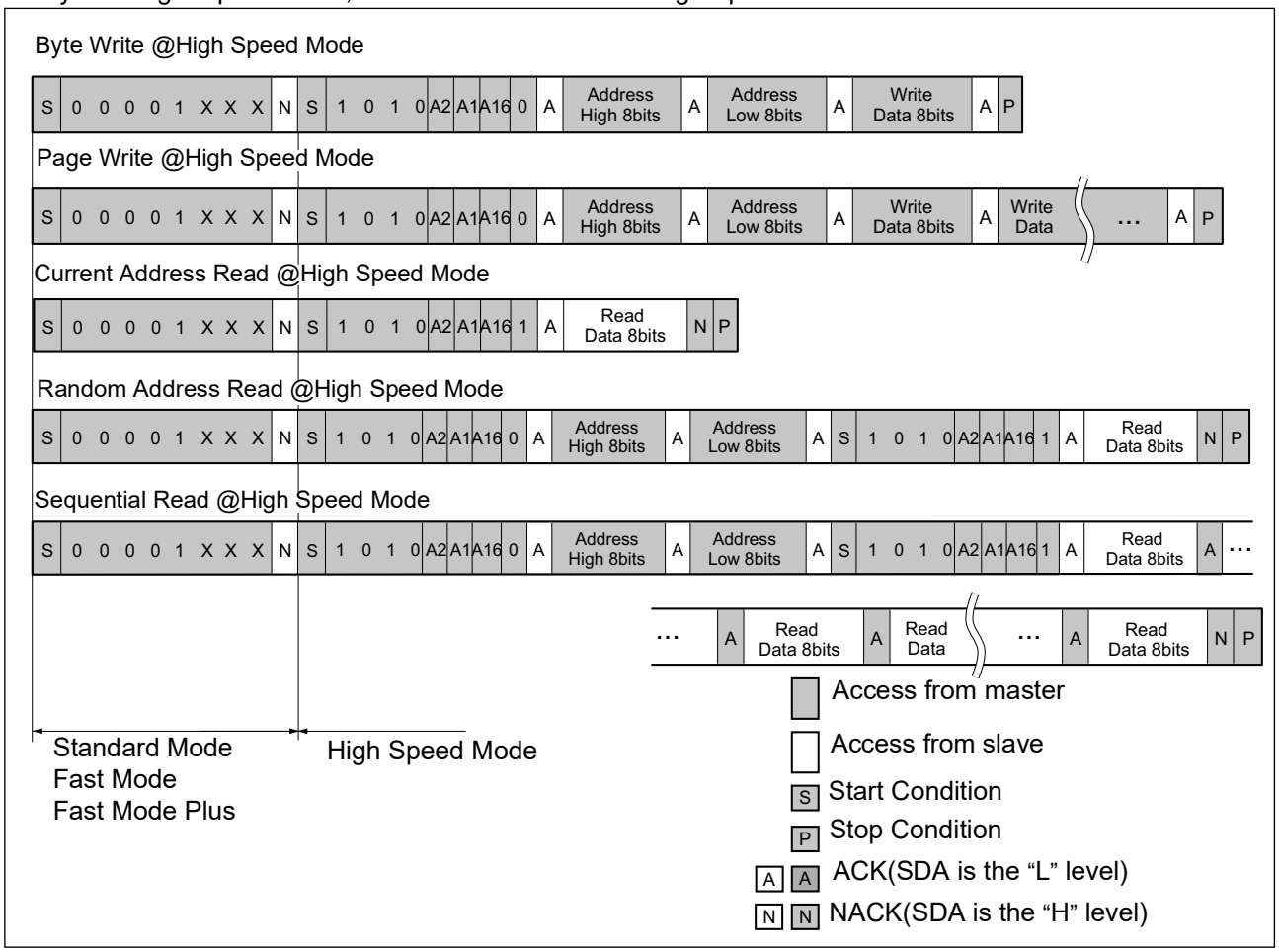



- High Speed Mode

MS85RC1MTY supports High Speed mode up to 3.4 MHz. By sending an entry command (0000 1XXX) after start condition from the master side, it informs to the slave that the data transmission with High Speed mode will start.

Since there is no slave side which is allowed to respond to this entry command, NACK response continues from the slave side. After the master side recognizes this NACK response, the master side changes its state to High Speed mode and enables the bidirectional communication up to 3.4 MHz.

By sending Stop condition, it exits out of the state in High Speed communication.

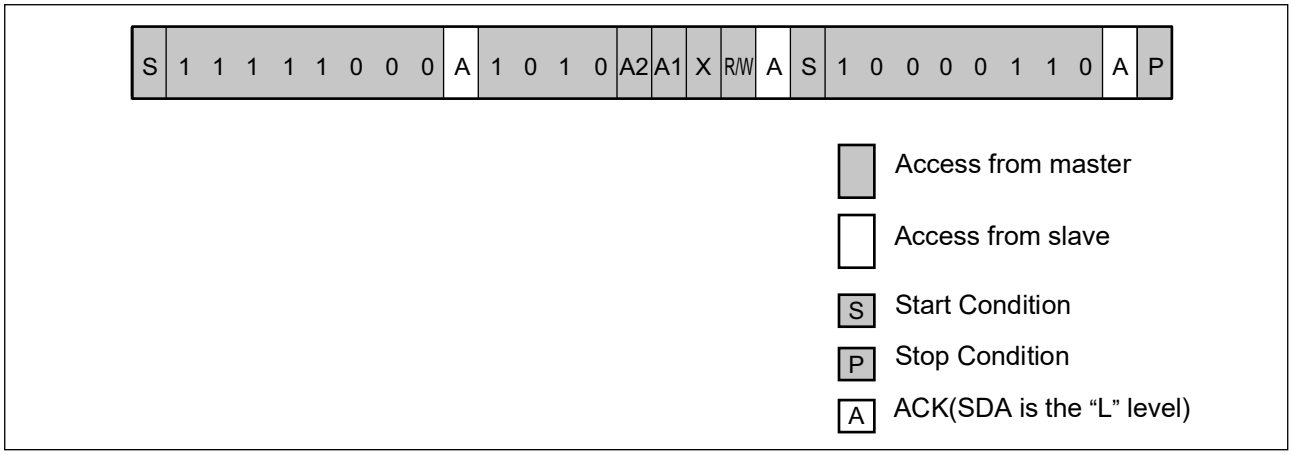


• Sleep Mode

MS85RC1MTY provides Sleep mode which reduces less current consumption than Standby mode, by stooping the internal regulator circuits. Following sequences enable the Sleep mode transition.

<Transition to Sleep mode>

a) The master sends start condition followed by F8h.
b) After ACK response from slave, the master sends the device address word.
In this device address word, Read/Write code is Don't care.
c) After ACK response from slave, the master re-sends the start condition followed by 86h.
d) The slave moves to Sleep mode after ACK response to the master.

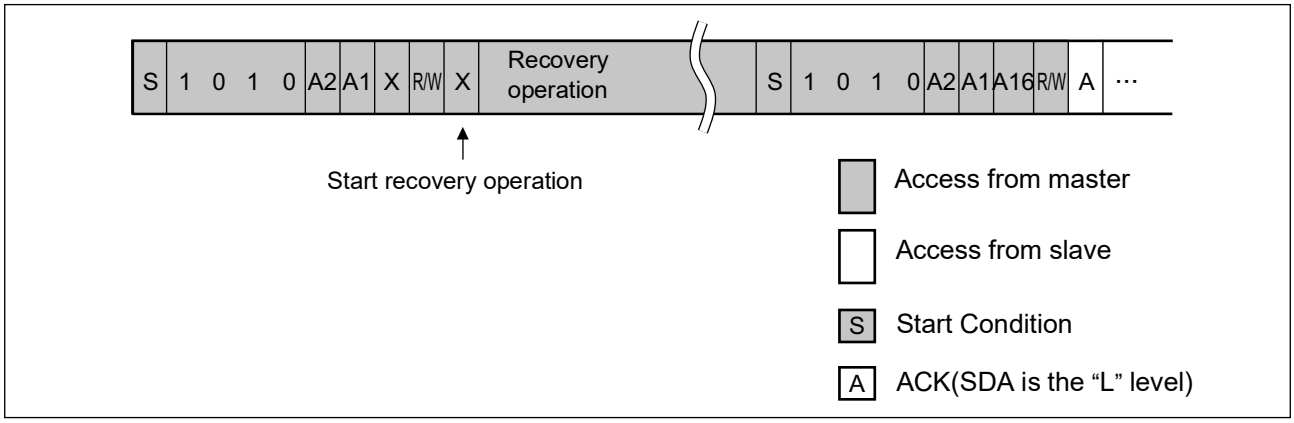



Even if the MS85RC1MTY stays in the Sleep mode, SDA and SCL signals are monitored. Following sequences enable the transition to Standby mode after recovery time ($t_{REC}$) of internal regulator circuits.

<Exit from Sleep mode>

a) The master sends start condition followed by device address word.
In this device address word, Read/Write code is Don't care.
b) At the rising edge of 9th clock from start condition, an internal regulator starts to operate its recovery sequence.
c) After the recovery time ($t_{REC}$) passed, standby mode enabled.

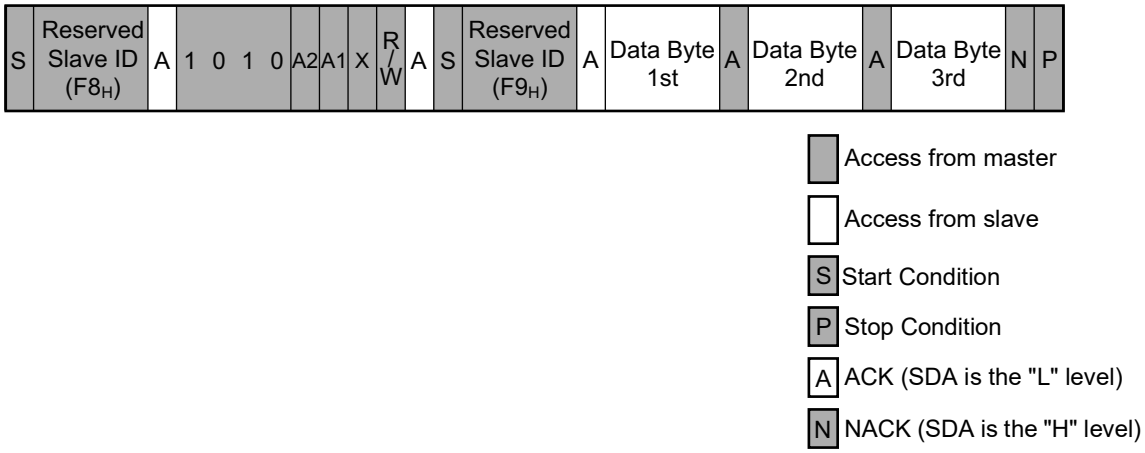
After returning to Standby mode, reading and writing are enabled by sending each command starts with start condition.



- Device ID

The Device ID command reads fixed Device ID. The size of Device ID is 3 bytes and consists of manufacturer ID and product ID. The Device ID is read-only and can be read out by following sequences.

a) The master sends the Reserved Slave ID $F8_H$ after the START condition.
b) The master sends the device address word after the ACK response from the slave.
In this device address word, R/W code is “Don't care”.
c) The master re-sends the START condition followed by the Reserved Slave ID $F9_H$ after the ACK response from the slave.
d) The master read out the Device ID succeedingly in order of Data Byte 1st / 2nd / 3rd after the ACK response from the slave.
e) The master responds the NACK (SDA is the “H” level) after reading 3 bytes of the Device ID.
In case the master respond the ACK after reading 3 bytes of the Device ID, the master re-reading the Device ID from the 1st byte.




| Data Byte 1st | | | | | | | | Data Byte 2nd | | | | Data Byte 3rd | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Manufacture ID = $00A_H$ | | | | | | | | | | | | Product ID = $798_H$ | | | | | | | | | | | |
| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | | | | | | | | | Density = $7_H$ | | | | Proprietary use | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

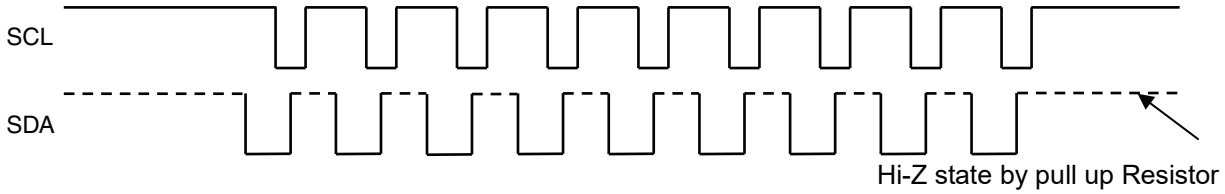
## ■ SOFTWARE RESET SEQUENCE OR COMMAND RETRY

In case the malfunction has occurred after power on, the master side stopped the I²C communication during processing, or unexpected malfunction has occurred, execute the following (1) software recovery sequence just before each command, or (2) retry command just after failure of each command.

### (1) Software Reset Sequence

Since the slave side may be outputting “L” level, do not force to drive “H” level, when the master side drives the SDA port. This is for preventing a bus conflict. The additional hardware is not necessary for this software reset sequence.

9 set of “Start Conditions and one “1” data”




Send “Start Condition and one data “1””.
Repeat these 9 times just before Write or Read command.

### (2) Command Retry

Command retry is useful to recover from failure response during I²C communication.

## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Power supply voltage* | $V_{DD}$ | – 0.5 | +4.0 | V |
| Input voltage* | $V_{IN}$ | – 0.5 | $V_{DD}$ + 0.5 ( ≤ 4.0) | V |
| Output voltage* | $V_{OUT}$ | – 0.5 | $V_{DD}$ + 0.5 ( ≤ 4.0) | V |
| Operation ambient temperature | $T_A$ | – 40 | + 125 | °C |
| Storage temperature | Tstg | – 55 | + 150 | °C |

*: These parameters are based on the condition that VSS is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Power supply voltage*1 | $V_{DD}$ | 1.8 | 3.3 | 3.6 | V |
| Operation ambient temperature*2 | $T_A$ | – 40 | — | + 125 | °C |

*1: These parameters are based on the condition that VSS is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ ($T_A$=25 °C) | Max | |
| Input leakage current*1 | $\|I_{LI}\|$ | $V_{IN}$ = 0 V to $V_{DD}$ | — | — | 1 | μA |
| Output leakage current*2 | $\|I_{LO}\|$ | $V_{OUT}$ = 0 V to $V_{DD}$ | — | — | 1 | μA |
| Operating power supply current | $I_{DD}$ | SCL = 0.1 MHz | — | — | — | mA |
| | | SCL = 1 MHz | — | 0.09 | 0.25 | mA |
| | | SCL = 3.4 MHz | — | 0.24 | 0.4 | mA |
| Standby current | $I_{SB}$ | SCL, SDA = $V_{DD}$<br>A1, A2, WP = 0 V or Open<br>Under Stop Condition | — | 12 | 150 | μA |
| Sleep current | $I_{ZZ}$ | SCL, SDA = $V_{DD}$<br>A1, A2, WP = 0 V | | 0.3 | 16 | μA |
| "H" level input voltage | $V_{IH}$ | $V_{DD}$ = 1.8 V to 3.6 V | $V_{DD}$ × 0.8 | — | $V_{DD}$ +0.5 | V |
| "L" level input voltage | $V_{IL}$ | $V_{DD}$ = 1.8 V to 3.6 V | -0.5 | — | $V_{DD}$ × 0.2 | V |
| "L" level output voltage | $V_{OL}$ | $I_{OL}$ = 3 mA | — | — | 0.4 | V |
| Input resistance for WP, A1 and A2 pins | $R_{IN}$ | — | 11 | 33 | 125 | kΩ |

*1: Applicable pin: SCL,SDA

*2: Applicable pin: SDA

## 2. AC Characteristics

| Parameter | Symbol | Value | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | STANDARD MODE | | FAST MODE | | FAST MODE PLUS | | HIGH SPEED MODE | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| SCL clock frequency | FSCL | 0 | 100 | 0 | 400 | 0 | 1000 | 0 | 3400 | kHz |
| Clock high time | $T_{HIGH}$ | 4000 | — | 600 | — | 260 | — | 60 | — | ns |
| Clock low time | $T_{LOW}$ | 4700 | — | 1300 | — | 500 | — | 160 | — | ns |
| SCL/SDA rising time | $T_r$ | — | 1000 | — | 300 | — | 300 | — | 80 | ns |
| SCL/SDA falling time | $T_f$ | — | 300 | — | 300 | — | 120 | — | 80 | ns |
| Start condition hold | $T_{HD:STA}$ | 4000 | — | 600 | — | 250 | — | 160 | — | ns |
| Start condition setup | $T_{SU:STA}$ | 4700 | — | 600 | — | 250 | — | 160 | — | ns |
| SDA input hold | $T_{HD:DAT}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| SDA input setup | $T_{SU:DAT}$ | 250 | — | 100 | — | 50 | — | 10 | — | ns |
| SDA output hold | $T_{DH:DAT}$ | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| Stop condition setup | $T_{SU:STO}$ | 4000 | — | 600 | — | 250 | — | 160 | — | ns |
| SDA output access after SCL falling | $T_{AA}$ | — | 3000 | — | 900 | — | 450 | — | 130 | ns |
| Pre-charge time | $T_{BUF}$ | 4700 | — | 1300 | — | 500 | — | 300 | — | ns |
| Noise suppression time (SCL and SDA) | $T_{SP}$ | — | 50 | — | 50 | — | 50 | — | 10 | ns |

AC characteristics were measured under the following measurement conditions.

Power supply voltage : 1.8 V to 3.6 V

Operation ambient temperature : – 40 °C to + 125 °C

Input voltage magnitude : $V_{DD} \times 0.2$ to $V_{DD} \times 0.8$

Input rising time : 5 ns

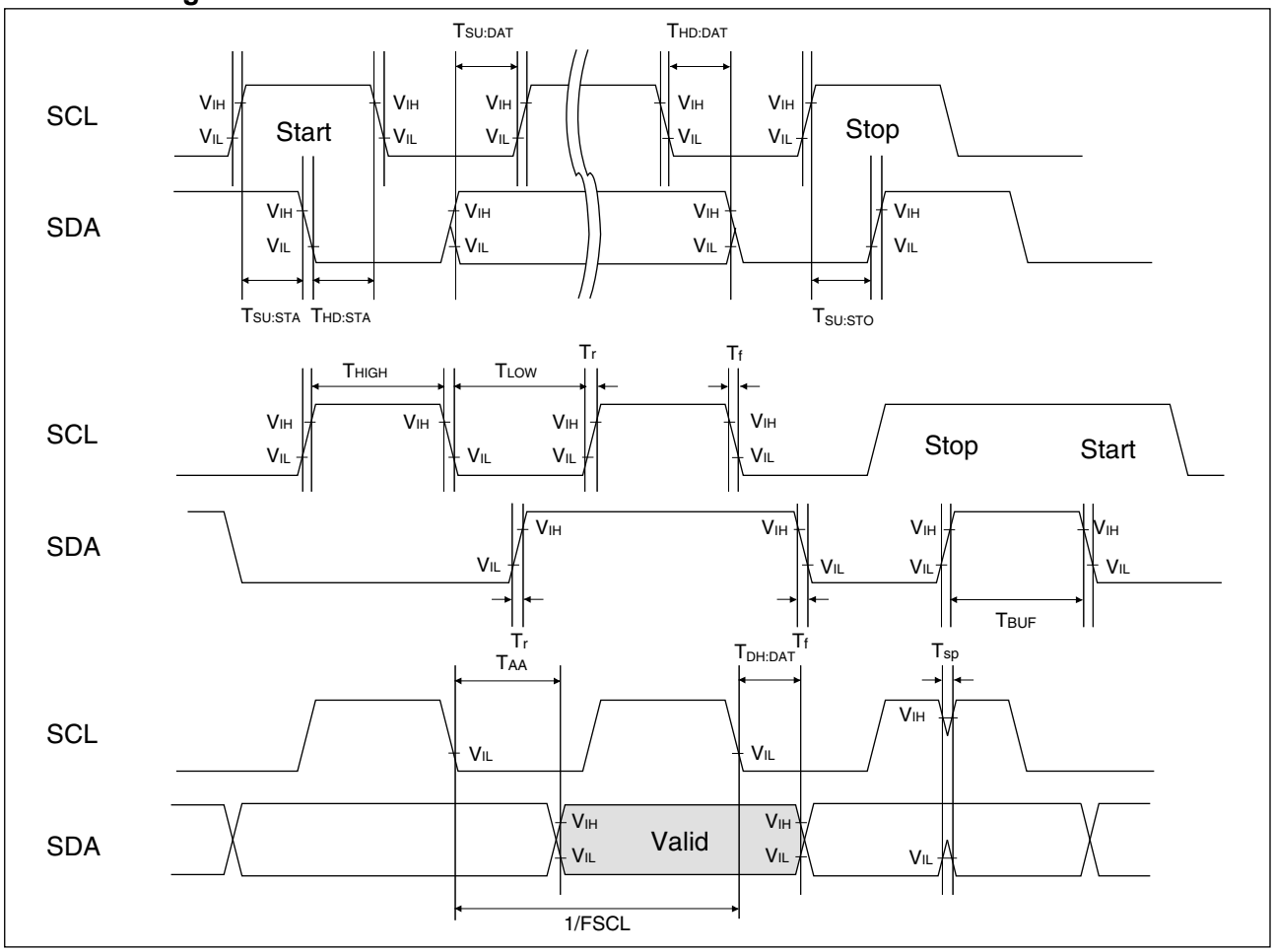
Input falling time : 5 ns

Input judge level : $V_{DD}/2$

Output judge level : $V_{DD}/2$

Output load capacitance : 100 pF

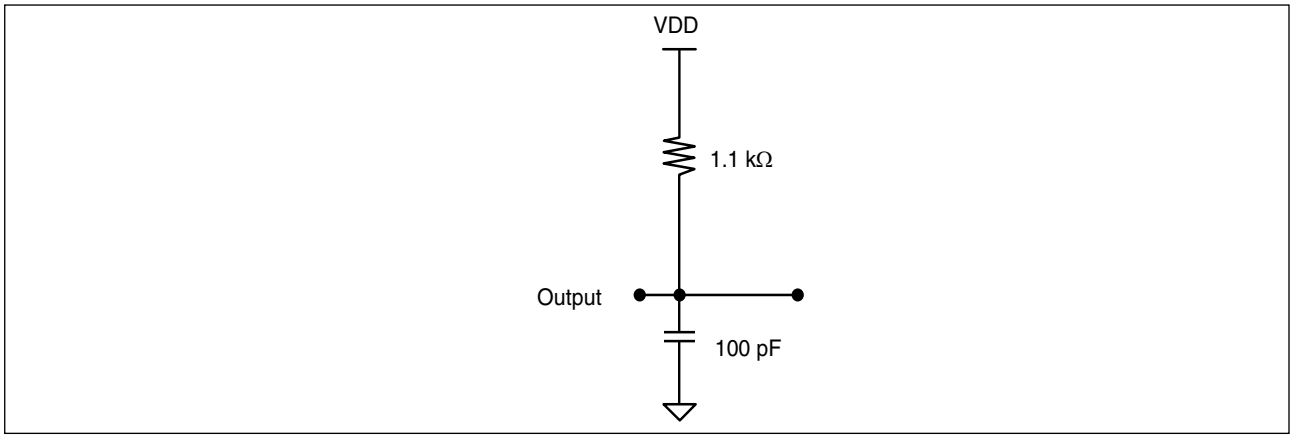
## 3. AC Timing Definitions



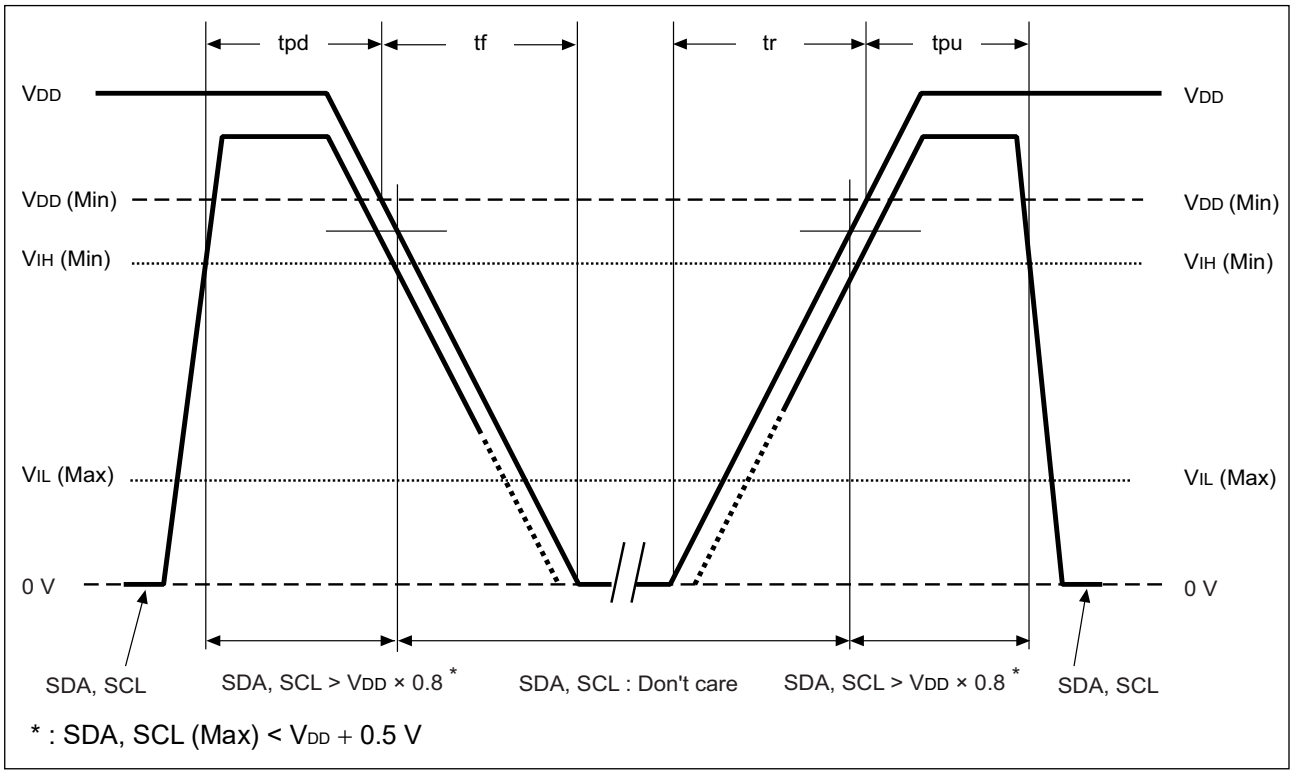

## 4. Pin Capacitance

| Parameter | Symbol | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| I/O capacitance | $C_{I/O}$ | $V_{DD}$ = 3.3 V, f = 1 MHz, $T_A$ = + 25 °C | — | — | 8 | pF |
| Input capacitance | $C_{IN}$ | | — | — | 8 | pF |

## 5. AC Test Load Circuit



## ■ POWER ON/OFF SEQUENCE




When applying relatively short term $V_{DD}$ pulse whose peak is more than 1.7V, it is required to set falling time, tf more than 0.4ms/V. (In case $V_{DD}$ rises over 1.7V and falls just after that, if this term is short, device may lose its function.)

.

| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SDA, SCL level hold time during power down | tpd | 85 | — | ns |
| SDA, SCL level hold time during power up | tpu | 450 | — | µs |
| Power supply rising time | tr | 0.05 | — | ms/V |
| Power supply falling time | tf | 0.1 | — | ms/V |
| Internal regulator recovery time | $t_{REC}$ | — | 450 | µs |

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

## ■ FeRAM CHARACTERISTICS

| Item | Min | Max | Unit | Parameter |
|---|---|---|---|---|
| Read/Write Endurance*1 | $10^{13}$ | — | Times | Operation Ambient Temperature $T_A$ = + 125 °C |
| | $10^{14}$ | — | | Operation Ambient Temperature $T_A$ = + 85 °C |
| Data Retention*2 | 10.1*3 | — | Years | Operation Ambient Temperature $T_A$ = + 125 °C |
| | 40.7 | — | | Operation Ambient Temperature $T_A$ = + 105 °C |
| | 193.9 | — | | Operation Ambient Temperature $T_A$ = + 85 °C |

*1 : The value for Read/Write endurance apply to the total number of read and write operations per row in FeRAM. This is because FeRAM needs writing operation after each reading operations.

*2 : Minimum values define retention time of the first reading/writing data right after shipment.

*3: Under evaluation for more than 10.1 years(+125 °C).
These values are calculated by qualification results.

## ■ NOTE ON USE

- We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.
- During the access period from the start condition to the stop condition, keep the level of WP, A1 and A2 pins to the “H” level or the “L” level.

## ■ ESD AND LATCH-UP

| Test | DUT | Value |
|---|---|---|
| ESD HBM (Human Body Model)<br>JEDEC JS001 compliant | MS85RC1MTYPNF-G-BDE1<br>MS85RC1MTYPNF-G-BDERE1<br>MS85RC1MTYPN-G-AME1<br>MS85RC1MTYPN-G-AMEWE1 | ≥ \|2000 V\| |
| ESD CDM (Charged Device Model)<br>JEDEC JS002 compliant | | ≥ \|1000 V\| |
| Latch-Up (I-test)<br>JESD78 compliant | | ≥ \|125mA\| |
| Latch-Up ($V_{supply}$ overvoltage test)<br>JESD78 compliant | | ≥ 5.4V |

## ■ REFLOW CONDITIONS AND FLOOR LIFE

[ JEDEC MSL ] : Moisture Sensitivity Level 1 (IPC/JEDEC J-STD-020E)

MS85RC1MTYPN-G-AME1/ MS85RC1MTYPN-G-AMEWE1

[ JEDEC MSL ] : Moisture Sensitivity Level 3 (IPC/JEDEC J-STD-020E)

MS85RC1MTYPNF-G-BDE1/ MS85RC1MTYPNF-G-BDERE1

## ■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

## ■ ORDERING INFORMATION

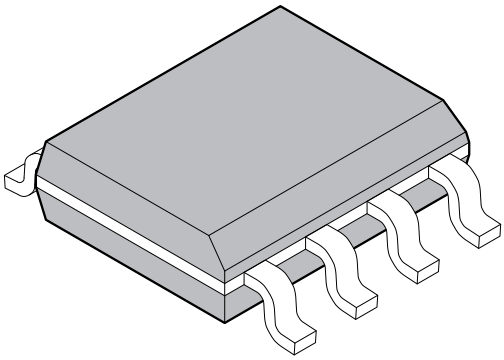
| Part number | Package | Shipping form | Minimum shipping quantity |
|---|---|---|---|
| MS85RC1MTYPNF-G-BDE1 | 8-pin, plastic SOP | Tube | —* |
| MS85RC1MTYPNF-G-BDERE1 | 8-pin, plastic SOP | Embossed Carrier tape | 1500 |
| MS85RC1MTYPN-G-AME1 | 8-pin, plastic DFN | Tray | —* |
| MS85RC1MTYPN-G-AMEWE1 | 8-pin, plastic DFN | Embossed Carrier tape | 1500 |

*: Please contact our sales office about minimum shipping quantity.

## ■ PACKAGE DIMENSION

(1) MS85RC1MTYPNF-G-BDE1/MS85RC1MTYPNF-G-BDERE1

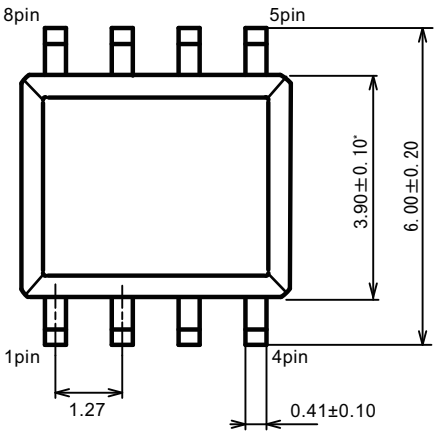
8-pin plastic SOP(150mil)

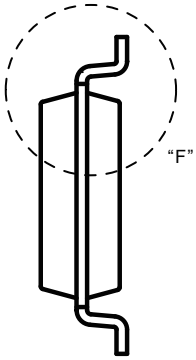


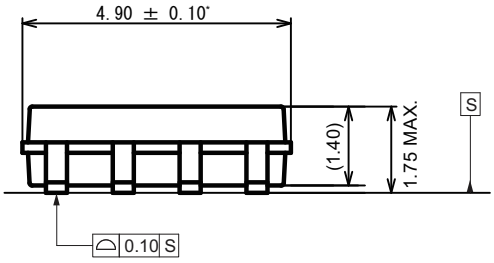
| | |
|---|---|
| Lead pitch | 1.27mm |
| Package width x Package length | 3.90mm x 4.90mm |
| Lead shape | Gullwing |
| Sealing method | Plastic mold |
| Mounting height | 1.75mm MAX. |
| | |
| | |

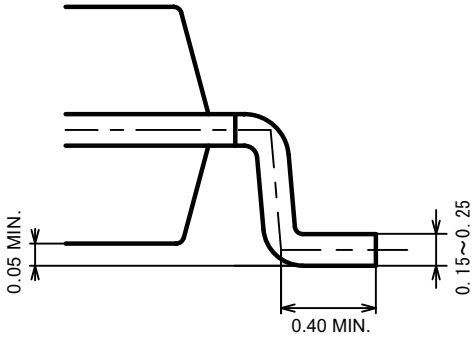
8-pin plastic SOP

Note *: These dimension do not include resin protrution.
Pins width do not include tie bar cutting remaindar.



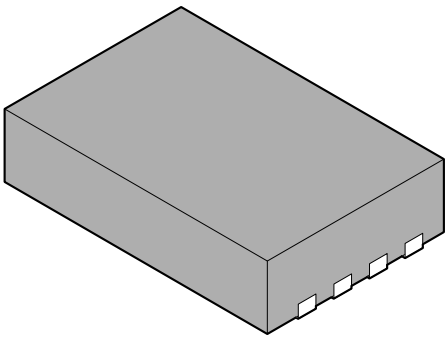



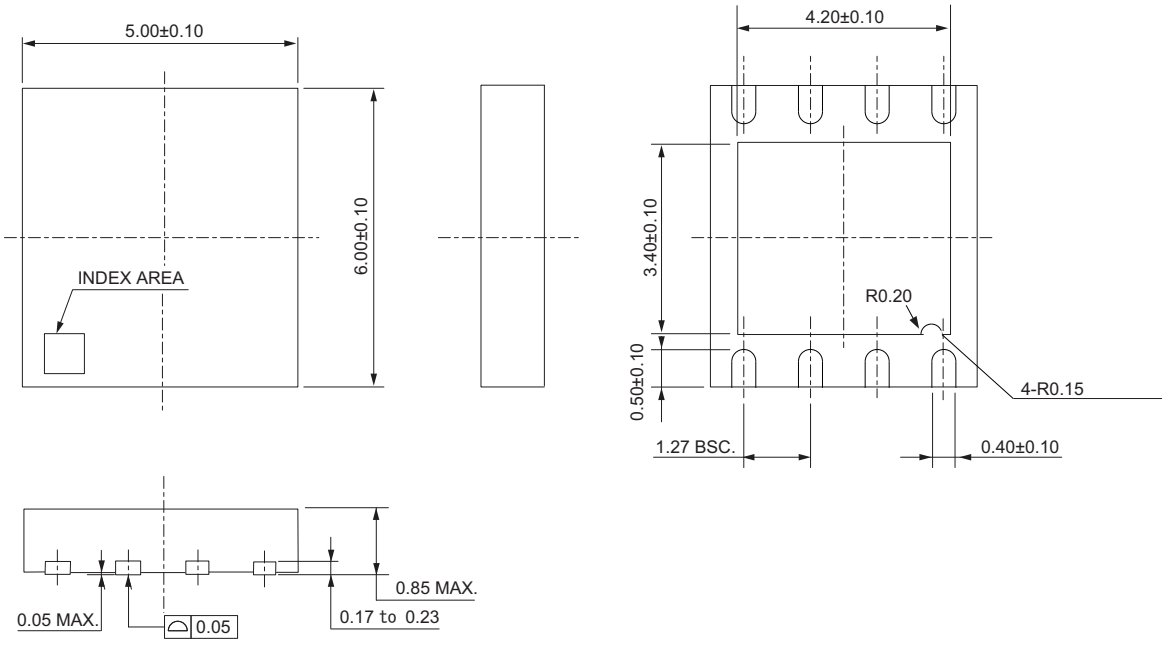

Details of "F"part

Dimension in mm

(2) MS85RC1MTYPN-G-AME1/MS85RC1MTYPN-G-AMEWE1

| 8-pin plastic DFN | | |
|---|---|---|
|  | Lead pitch | 1.27 mm |
| | Package width x Package length | 5.00 mm × 6.00 mm |
| | Sealing method | Plastic mold |
| | Mounting height | 0.85 mm MAX |
| | | |
| | | |

8-pin plastic DFN

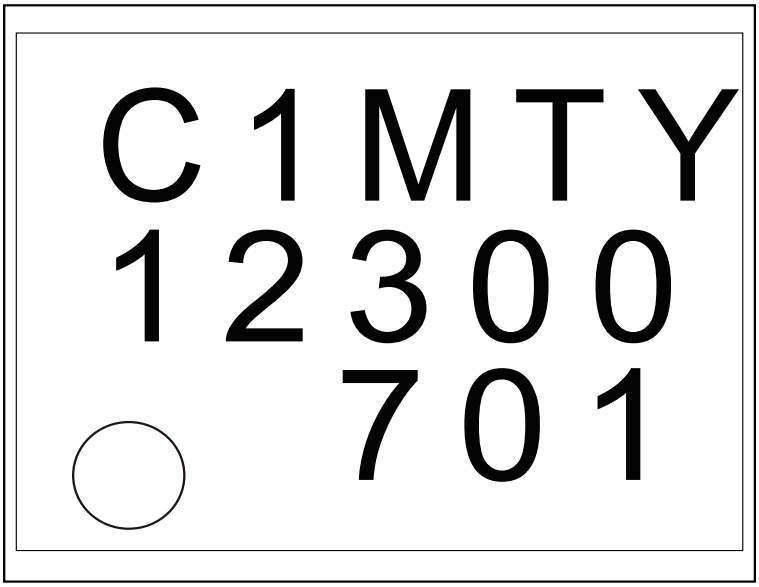



Dimensions in mm.

## ■ MARKING (Example)

(1) MS85RC1MTYPNF-G-BDE1/MS85RC1MTYPNF-G-BDERE1

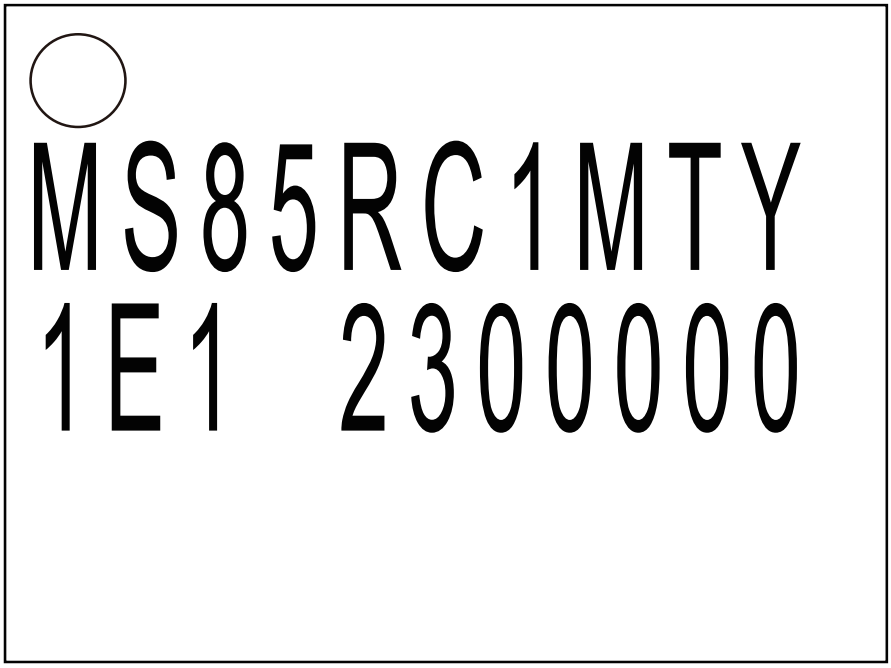
[MS85RC1MTYPNF-G-BDE1]
[MS85RC1MTYPNF-G-BDERE1]




C1MTY: Product name
12300 : 1(CS code) + 2300(Year and Week code)
701 : Trace code

(2) MS85RC1MTYPN-G-AME1/MS85RC1MTYPN-G-AMEWE1

[MS85RC1MTYPN-G-AME1]
[MS85RC1MTYPN-G-AMEWE1]




MS85RC1MTY: Product name
1E1 : 1(CS code) + E1(Lead free code)
2300000 : 2300(Year and Week code) + 000(Trace code)

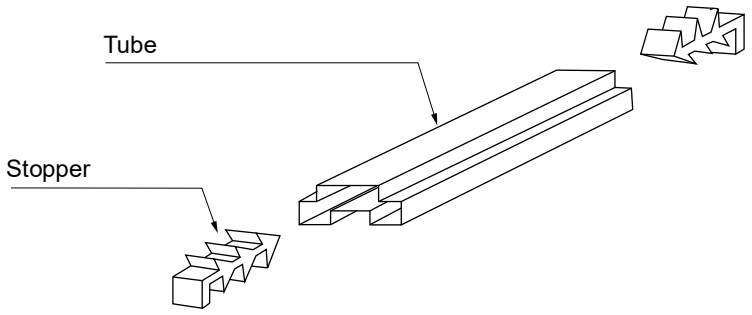
## ■ PACKING INFORMATION

(1) MS85RC1MTYPNF-G-BDE1/MS85RC1MTYPNF-G-BDERE1

### 1. Tube (MS85RC1MTYPNF-G-BDE1)

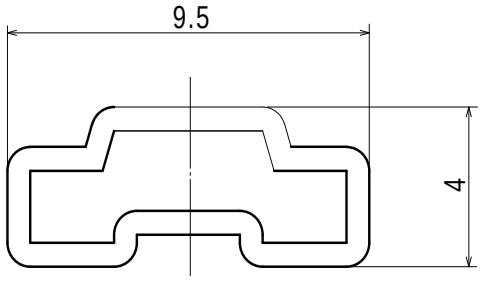
#### 1.1 Tube Dimensions

- Tube/stopper shape (example)




- **Tube cross-sections** and Maximum quantity

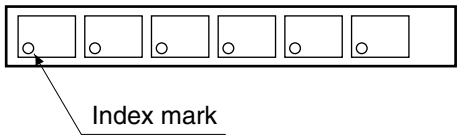
| Maximum quantity | | |
|---|---|---|
| pcs/tube(500mm) | pcs/inner box | pcs/outer box |
| 85 | 4,250 | 17,000 |




No heat resistance.
Package should not be baked by using tube.

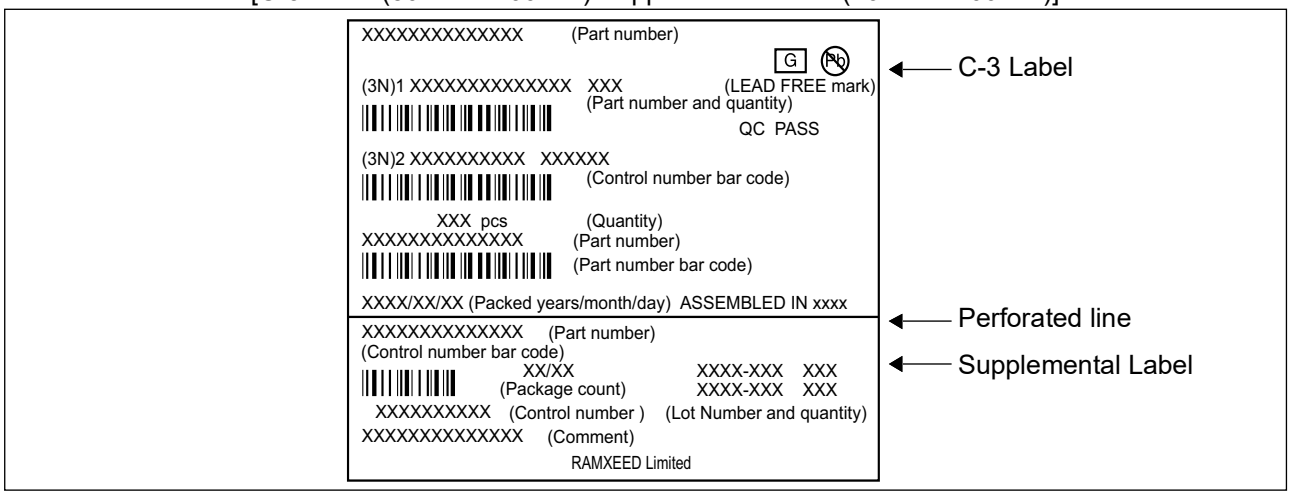
(Dimensions in mm)

- **Direction of index in tube**



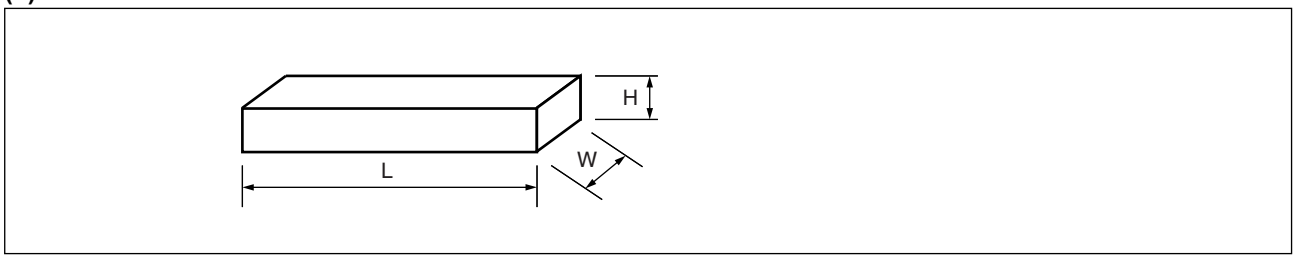
### 1.2 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]




### 1.3 Dimensions for Containers

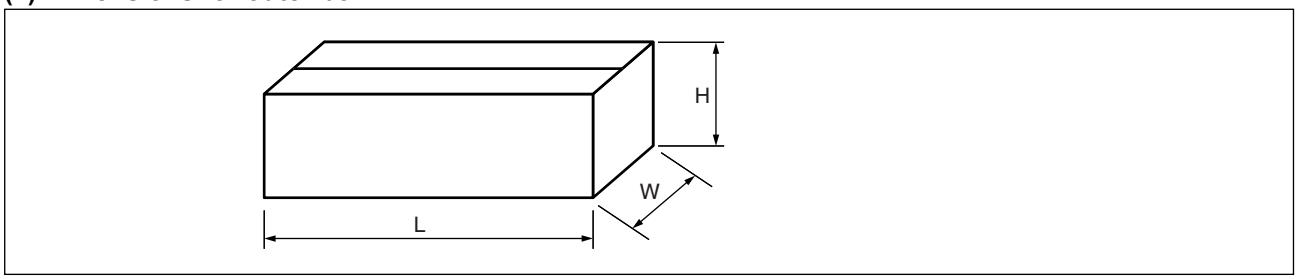
#### (1) Dimensions for inner box




| L | W | H |
|---|---|---|
| 540 | 125 | 75 |

(Dimensions in mm)

#### (2) Dimensions for outer box



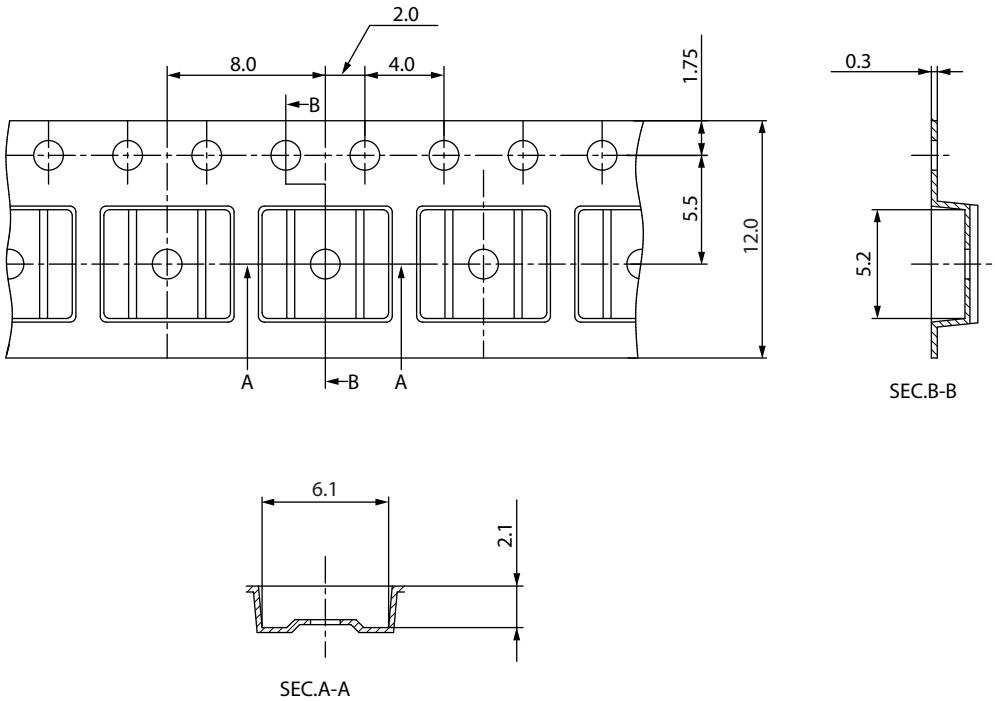

| L | W | H |
|---|---|---|
| 565 | 270 | 180 |

(Dimensions in mm)

## 2. Emboss Tape (MS85RC1MTYPNF-G-BDERE1)

### 2.1 Tape Dimensions (not drawn to scale) (8-pin plastic SOP)

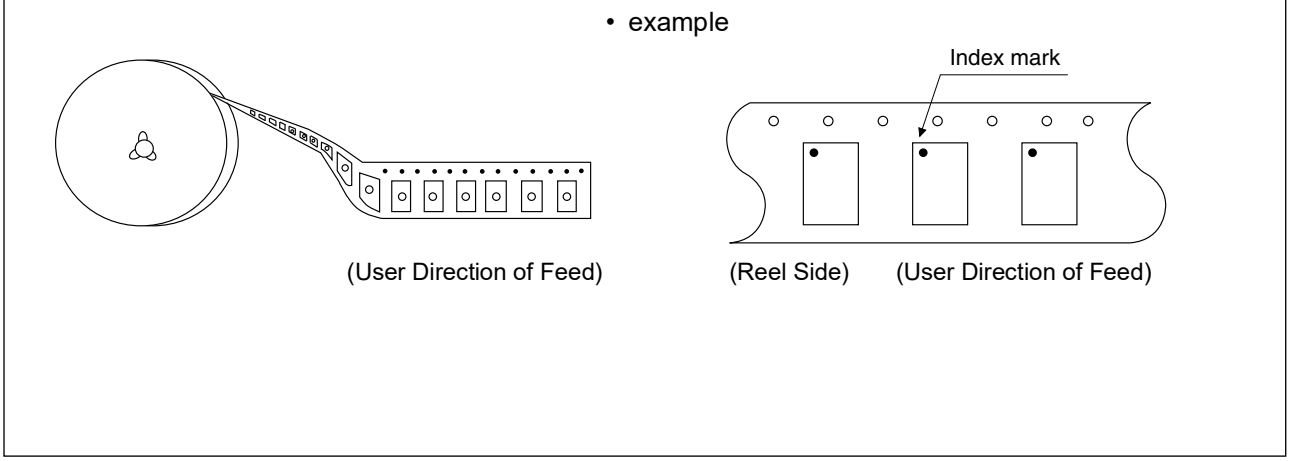
| Maximum storage capacity | | |
|---|---|---|
| pcs/reel(Φ254mm) | pcs/inner box | pcs/outer box |
| 1500 | 1500<br>(1 pack/inner box) | 9000<br>(6 inner boxes/outer box:Max) |



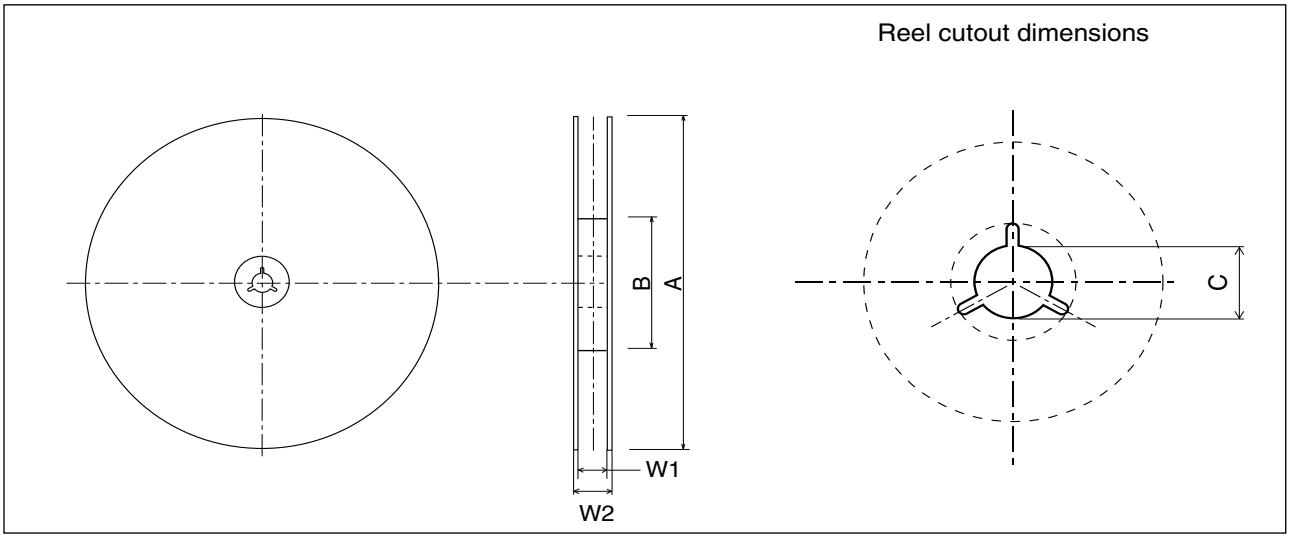

(Dimensions in mm)

Heat proof temperature : No heat resistance.
Package should not be baked by using tape and reel.

## 2.2 IC orientation




## 2.3 Reel dimensions

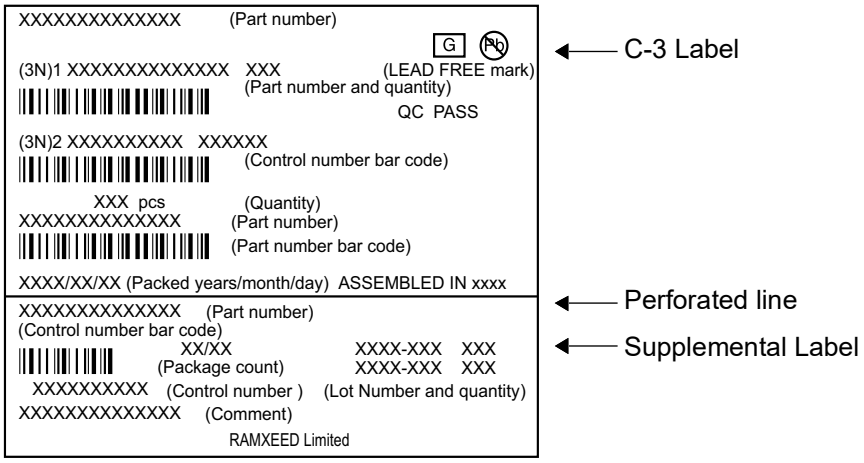



Dimensions in mm

| A | B | C | W1 | W2 |
|---|---|---|---|---|
| 254 | 100 | 13 | 13.5 | 17.5 |

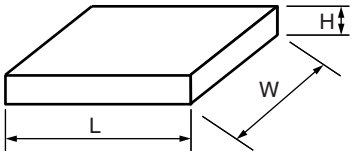
### 2.4 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]




### 2.5 Dimensions for Containers

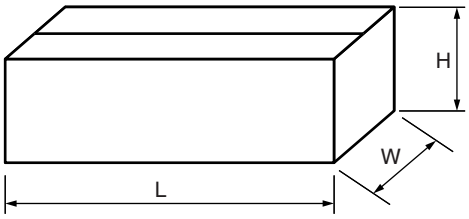
#### (1) Dimensions for inner box




| L | W | H |
|---|---|---|
| 265 | 260 | 50 |

(Dimensions in mm)

#### (2) Dimensions for outer box




| L | W | H |
|---|---|---|
| 565 | 270 | 180 |

(Dimensions in mm)

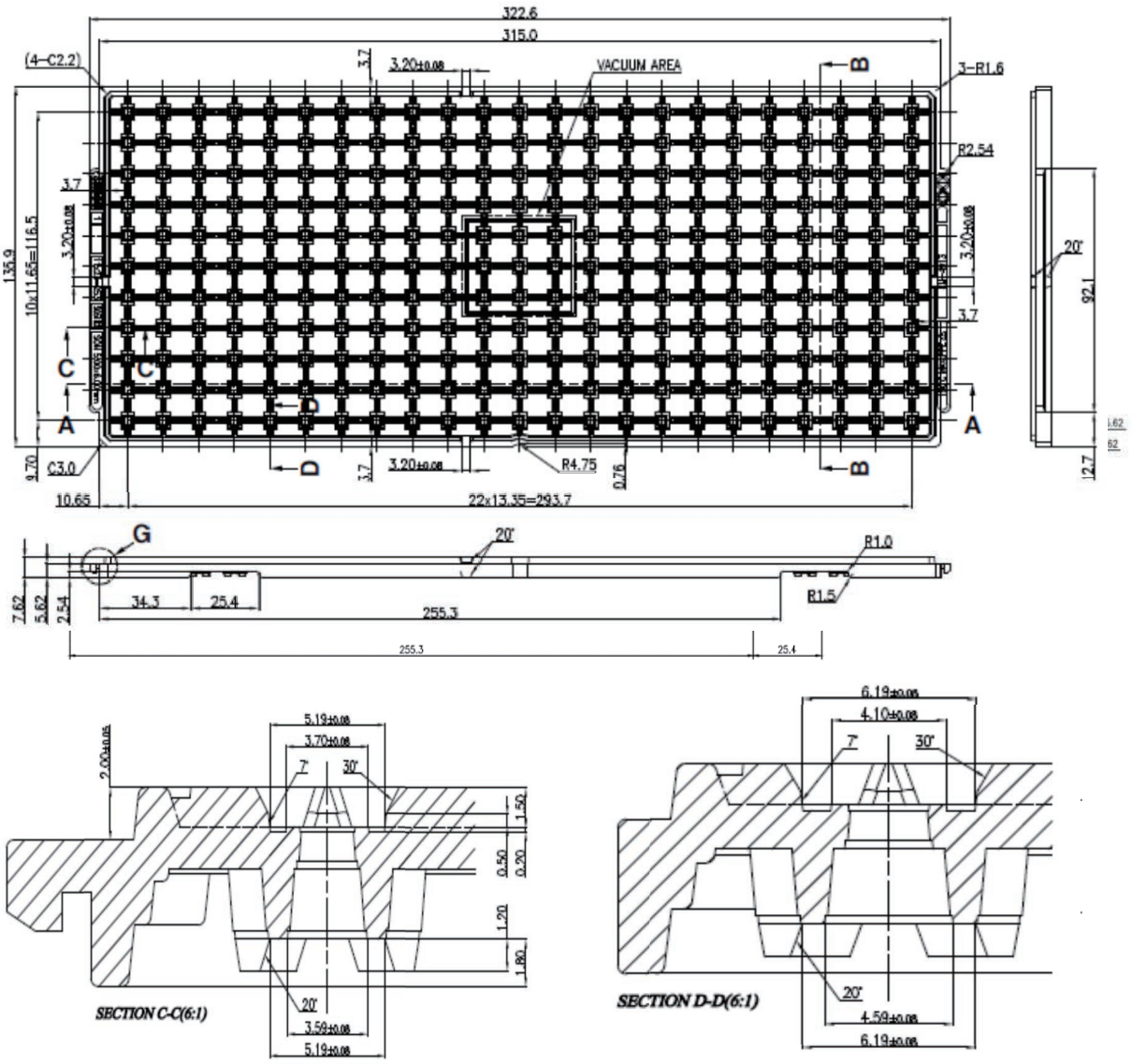
(2) MS85RC1MTYPN-G-AME1/MS85RC1MTYPN-G-AMEWE1

## 1. Tray (MS85RC1MTYPN-G-AME1)

### 1.1 Tray Dimensions

DFN8

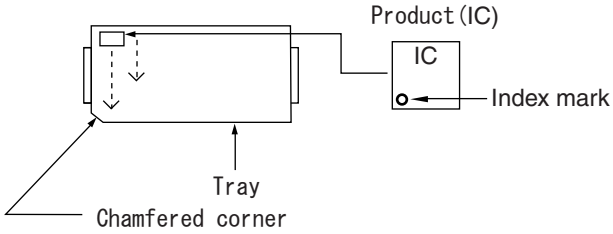
| Maximum storage capacity | | |
|---|---|---|
| pcs/tray | pcs/inner box | pcs/outer box |
| 253 | 2024 | 8096 |




(Dimensions in mm)

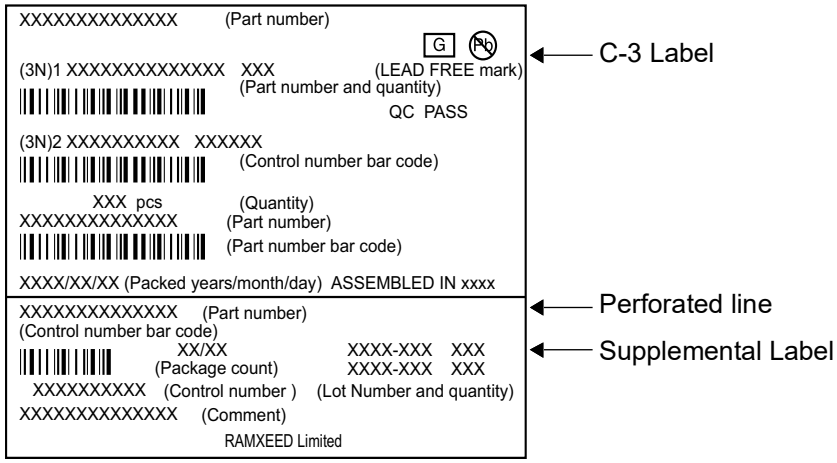
Heat proof temperature : 150 °C Max

### 1.2 IC orientation



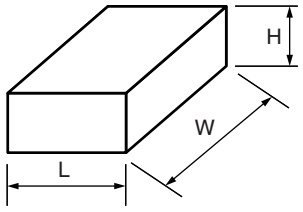

### 1.3 Product label indicators(example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]



### 1.4 Dimensions for Containers

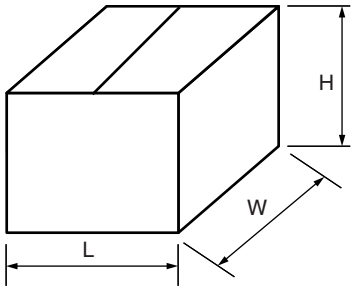
**(1) Dimensions for inner box**




| L | W | H |
|---|---|---|
| 165 | 360 | 75 |

(Dimensions in mm)

**(2) Dimensions for outer box**



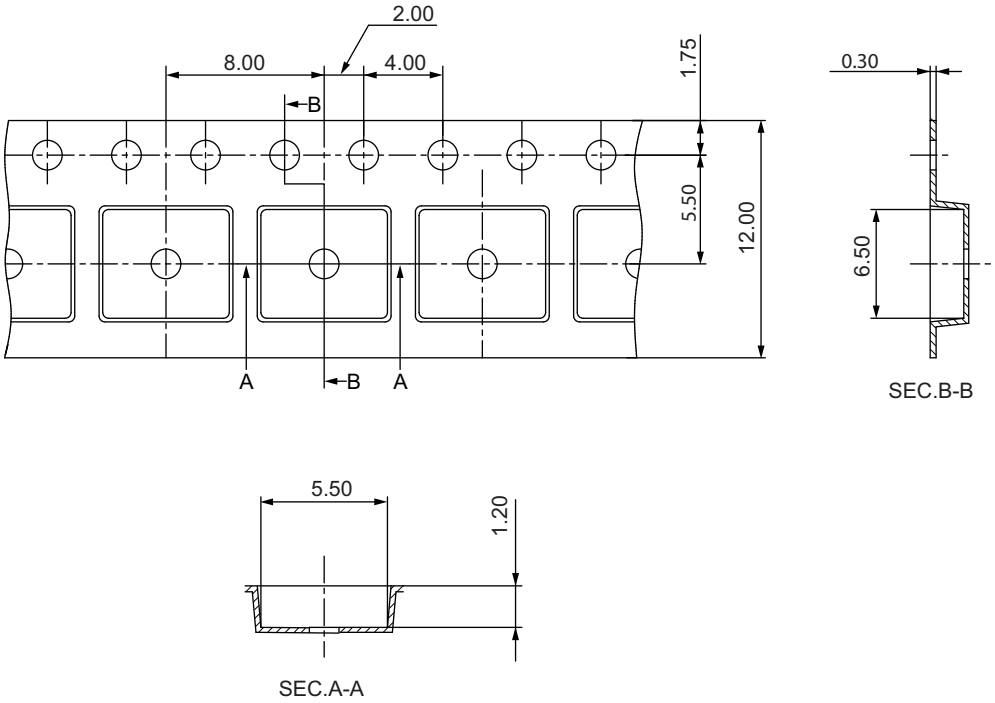

| L | W | H |
|---|---|---|
| 355 | 385 | 195 |

(Dimensions in mm)

## 2. Emboss Tape (MS85RC1MTYPN-G-AMEWE1)

### 2.1 Tape Dimensions (not drawn to scale)(8-pin plastic DFN 5mm × 6mm)

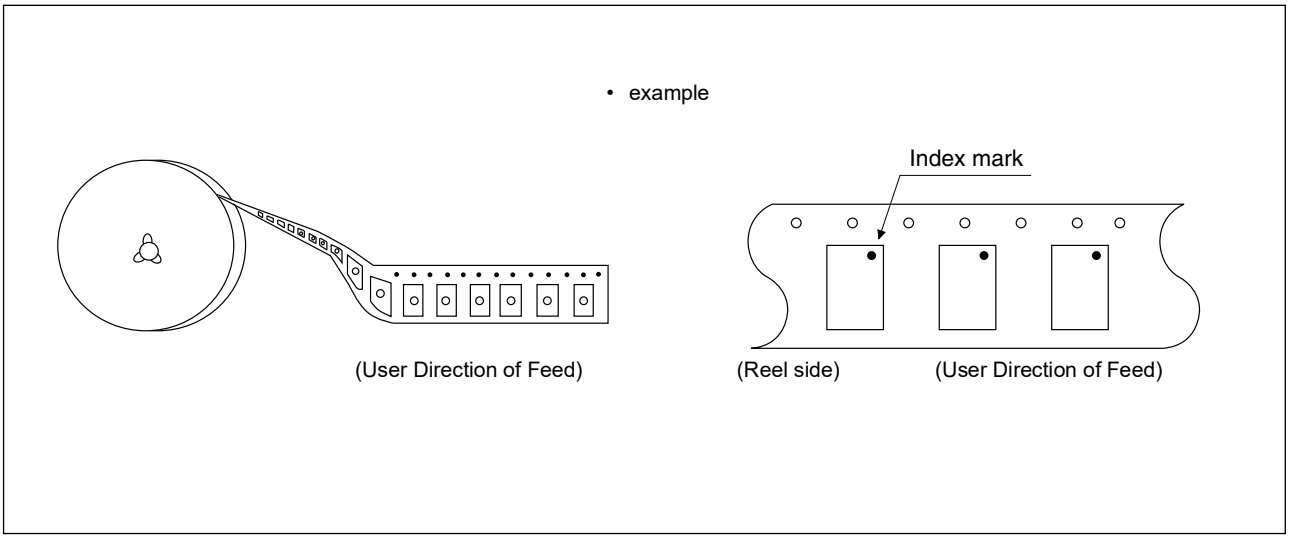
| Maximum storage capacity | | |
|---|---|---|
| pcs/reel(Φ254mm) | pcs/inner box | pcs/outer box |
| 1500 | 1500<br>(1 pack/inner box) | 9000<br>(6 inner boxes/outer box:Max) |



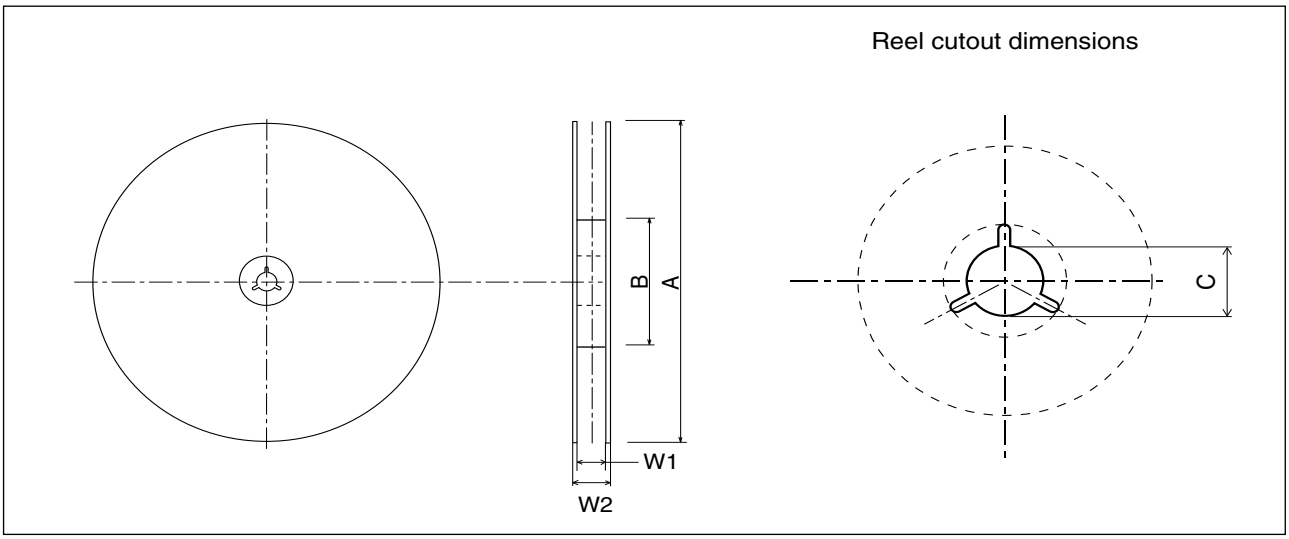

(Dimensions in mm)

Heat proof temperature : No heat resistance.
Package should not be baked by using tape and reel.

## 2.2 IC orientation




## 2.3 Reel dimensions

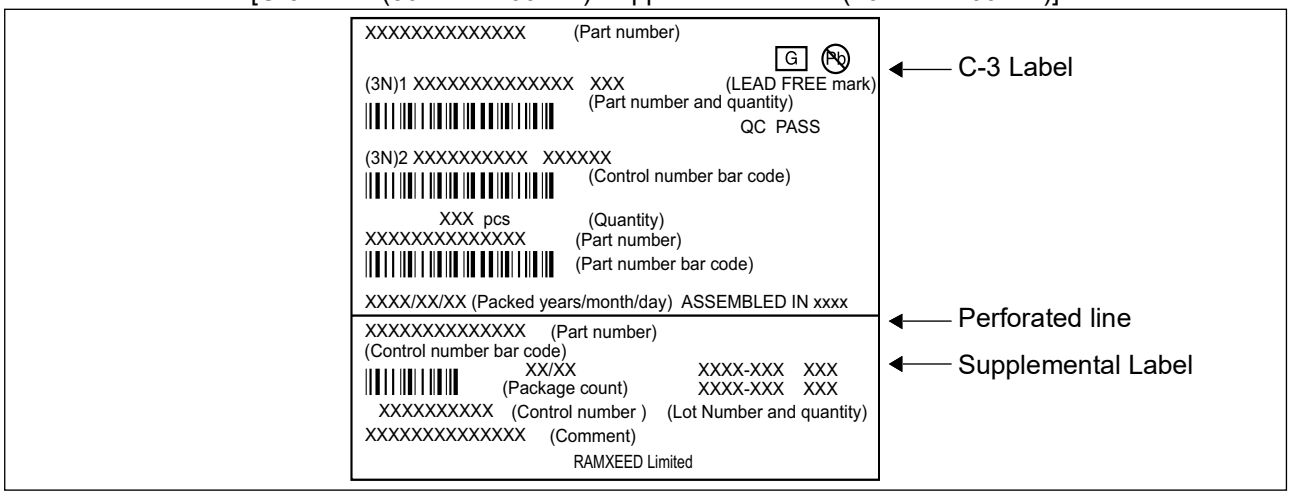



Dimensions in mm

| A | B | C | W1 | W2 |
|---|---|---|---|---|
| 254 | 100 | 13 | 13.5 | 17.5 |

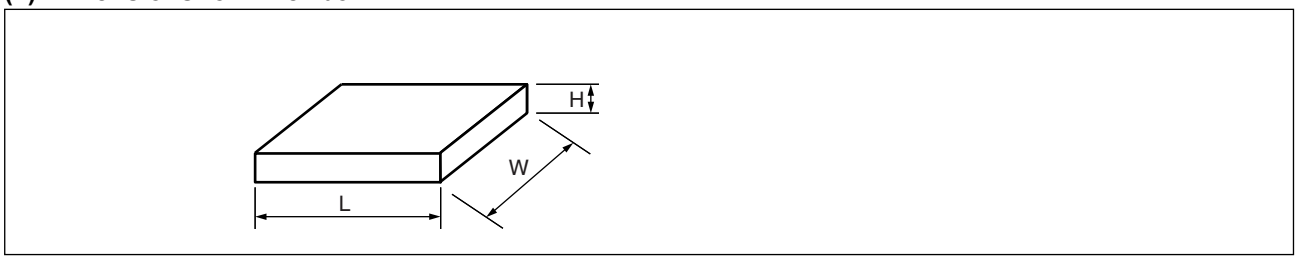
### 2.4 Product label indicators (example)

Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm × 100mm) Supplemental Label (20mm × 100mm)]




### 2.5 Dimensions for Containers

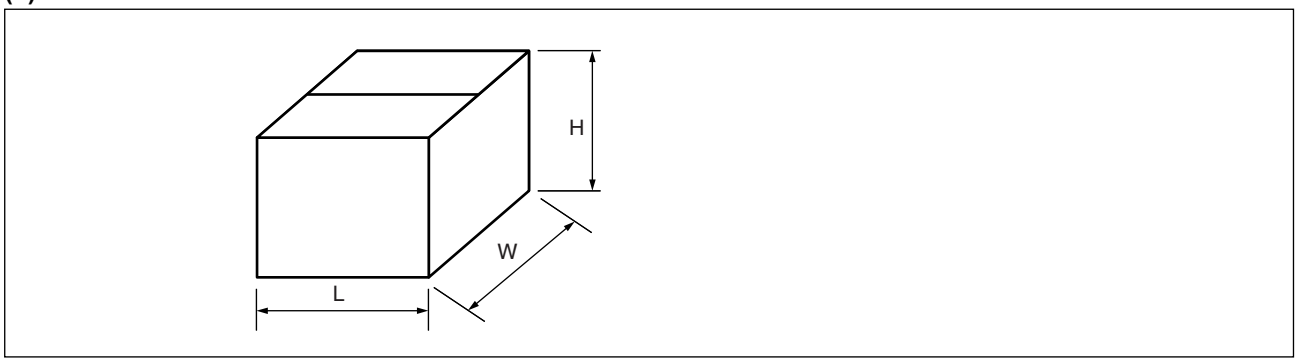
**(1) Dimensions for inner box**




| L | W | H |
|---|---|---|
| 265 | 260 | 50 |

(Dimensions in mm)

**(2) Dimensions for outer box**




| L | W | H |
|---|---|---|
| 565 | 270 | 180 |

(Dimensions in mm)

## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn left side of that page.

| Page | Section | Change Results |
|---|---|---|
| 1,17 | Data Retention | 10.1 years(+125 ℃ ), 40.7 years(+105 ℃ ), 193.9 years(+85 ℃ ) |
| 2 | PIN ASSIGNMENT | Change DFN8 Pin Assignment. |
| 18 | REFLOW CONDITIONS AND FLOOR LIFE | Add MSL1 information. |
| 19 | ORDERING INFORMATION | Change Part number for SOP8 and DFN8. |
| 21 | PACKAGE DIMENSION | Change DFN8 package dimension for new parts number. |
| 22 | MARKING (Example) | Change Marking information for new parts number. |
| 23~ | PACKING INFORMATION | Packaging information change due to part number change. |

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