

SuperQ® 200V N-Channel Power MOSFET

8.0mΩ, 132A, TOLT

FEATURES

- Low $R_{DS(on)}$ in TOLT package
- High short-circuit withstand capability (SCWC)
- 100% UIS tested in production
- Low switching losses, Q_{SW} and E_{OSS}
- Easier paralleling with + 0.5V gate threshold

APPLICATIONS

- Motor Control
- Boost converters and SMPS control FETs
- Secondary side synchronous rectifier

PRODUCT SUMMARY

Parameter	Typ	Max	Unit
V_{DS}	-	200	V
$R_{DS(on)}$ @ 10V	6.9	8.0	mΩ
I_D	132	-	A
Q_G	75	98	nC
Q_{SW}	4.9	-	nC
E_{OSS}	2.9	-	μJ

DESCRIPTION

Engineered for high-efficiency SMPS and motor drives, this 200V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust TOLT package. Featuring leading $R_{DS(on)}$ and Q_{SW} , it minimizes heat dissipation at both full and partial loads.

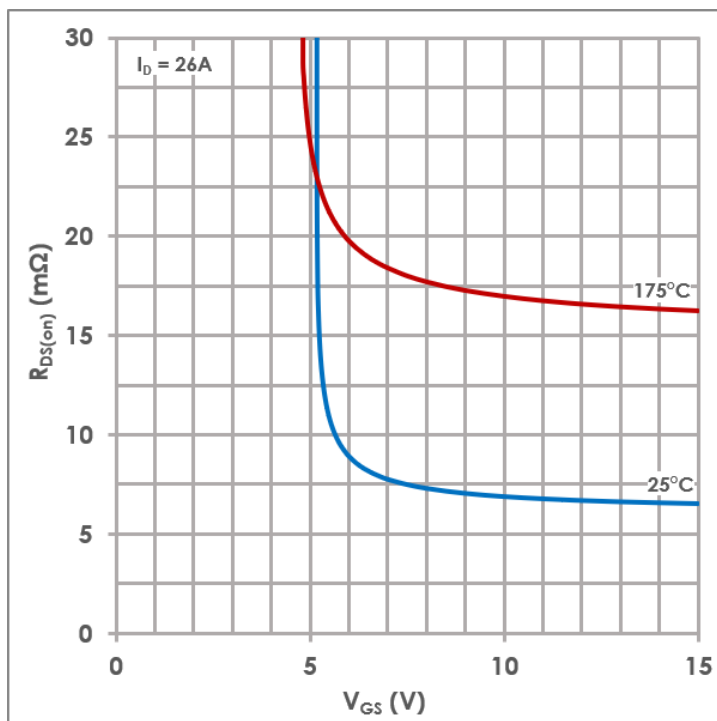
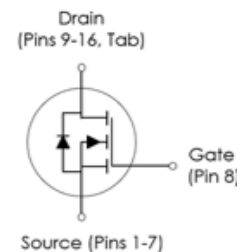


Figure 1: Typical Drain-Source On Resistance

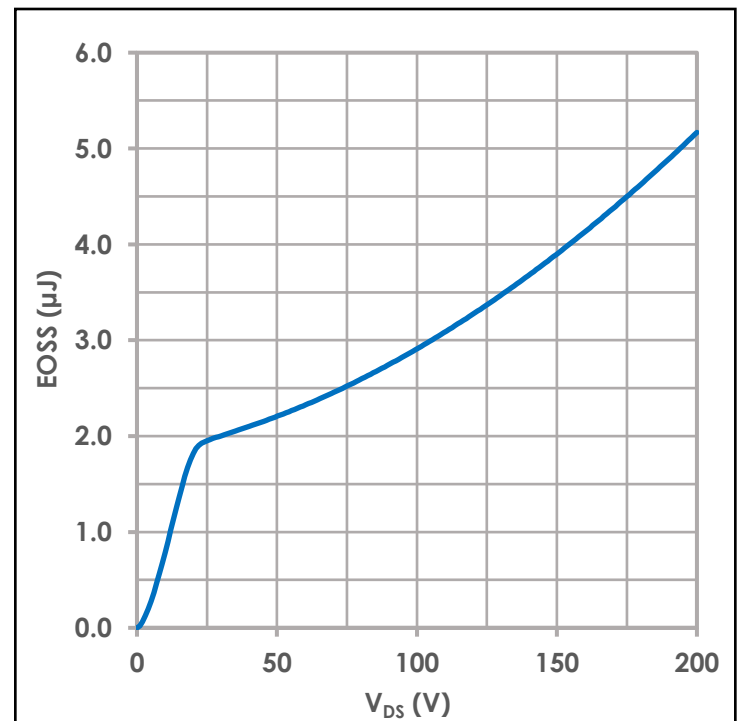


Figure 2: Typical C_{OSS} Stored Energy

ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS20M8R0S1TC	TOLT	iS20M8R0S1	13' 1,300pcs T&R

ABSOLUTE MAXIMUM RATINGS			
SYMBOL	PARAMETER ($T_A = 25^\circ\text{C}$ unless otherwise specified)	VALUE	UNIT
V_{GS}	Gate-to-source voltage	± 20	V
I_D	Continuous drain current (silicon limited), $T_C = 25^\circ\text{C}$	132	A
	Continuous drain current (silicon limited), $T_C = 100^\circ\text{C}$	93	
	Pulsed drain current	489	
	Continuous diode forward current, $T_C = 25^\circ\text{C}$	132	
I_{S_PULSE}	Diode pulse current	489	
P_D	Power dissipation, $T_C = 25^\circ\text{C}$	333	W
T_J, T_{SG}	Operating junction, storage temperature	-55 to 175	$^\circ\text{C}$
E_{AS}	Avalanche energy, single pulse $I_D = 56\text{A}$, $R_{GS} = 25\Omega$	373	mJ

THERMAL CHARACTERISTICS					
SYMBOL	PARAMETER (T _A = 25°C unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
R _{θJC}	Junction-to-case thermal resistance – TOLT	-	-	0.45	°C/W
R _{θJA}	Junction-to-ambient thermal resistance (1)	-	-	50	°C/W

(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0V, I _D = 1mA	200	-	-	V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0V, V _{DS} = 160V, T _J = 25°C	-	0.1	1	μA
		V _{GS} = 0V, V _{DS} = 160V, T _J = 125°C ⁽²⁾	-	-	100	
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0V, V _{GS} = 20V	-	1.7	100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 213μA	3.0	3.5	4.0	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 10V, I _D = 26A	-	6.9	8.0	mΩ
		V _{GS} = 15V, I _D = 26A	-	6.6	-	
g _{fs}	Transconductance	V _{DS} = 10V, I _D = 26A	39	78	-	S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance ⁽²⁾	V _{GS} = 0V, V _{DS} = 100V, f = 100kHz	-	5,703	7,413	pF
C _{rss}	Reverse transfer capacitance ⁽²⁾		-	15	19	
C _{oss}	Output capacitance ⁽²⁾		-	170	220	
C _{o(er)}	Effective output capacitance	V _{DS} = 0 to 100V, V _{GS} = 0V	-	292	-	
R _g	Series gate resistance	f = 1MHz	-	1.0	1.5	Ω
T _{d(on)}	Turn-on delay time	V _{DS} = 0 to 100V, V _{GS} = 10V, I _{DS} = 26A, R _{G,EXT} = 0Ω	-	16.4	-	ns
T _r	Rise time		-	4.3	-	
T _{d(off)}	Turn-off delay time		-	40.7	-	
T _f	Fall time		-	5	-	
GATE CHARGE CHARACTERISTICS						
Q _g	Gate charge total ⁽²⁾	V _{DS} = 100V, I _D = 26A, V _{GS} = 0 to 10V	-	75	98	nC
Q _{sw}	Switching charge ⁽³⁾		-	4.9	-	
Q _{gd}	Gate to drain charge ⁽²⁾⁽³⁾		-	1.9	2.4	
Q _{g(th)}	Gate charge at threshold ⁽³⁾		-	17	-	
Q _{gs2}	Gate to source charge ⁽³⁾		-	3.0	-	
V _{plateau}	Gate plateau voltage	V _{DS} = 0 to 100V, V _{GS} = 0V	-	5.3	-	V
Q _{oss}	Output charge ⁽²⁾		-	281	324	nC
E _{oss}	Capacitive stored energy		-	2.9	-	μJ
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 26A, V _{GS} = 0V	-	0.9	1.0	V
Q _{RR}	Reverse recovery charge	V _{DS} = 100V, I _F = 26A,	-	608	-	nC
t _{rr}	Reverse recovery time	di/dt = 100A/μs	-	133	-	ns

(2) Defined by design. Not subject to production test

(3) Q_{sw} should be used for switching loss calculations. See Figure 16 for definitions of gate charge. For more information, see Q_{sw} application note on www.idealsemi.com

Ratings and Characteristics Curves ($T_A = 25^\circ\text{C}$ unless otherwise specified)

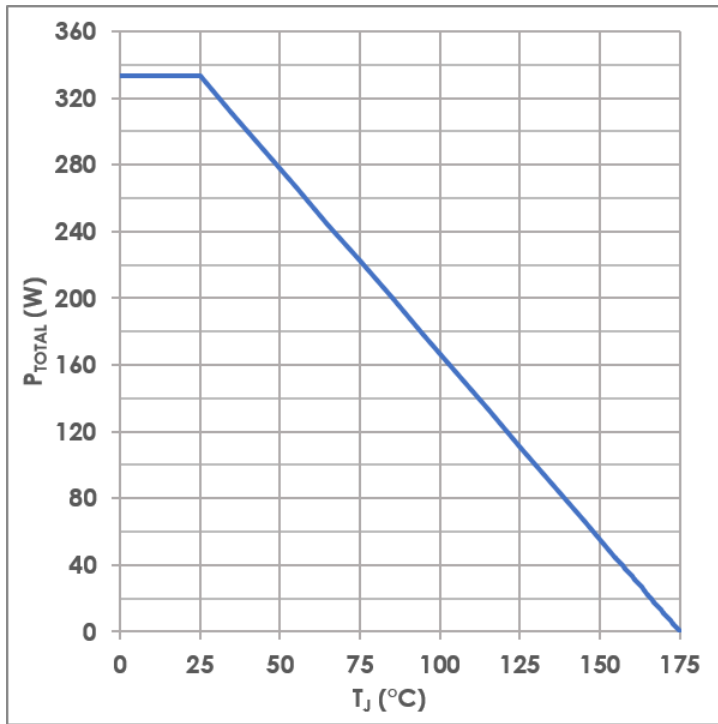


Figure 3: Power Dissipation

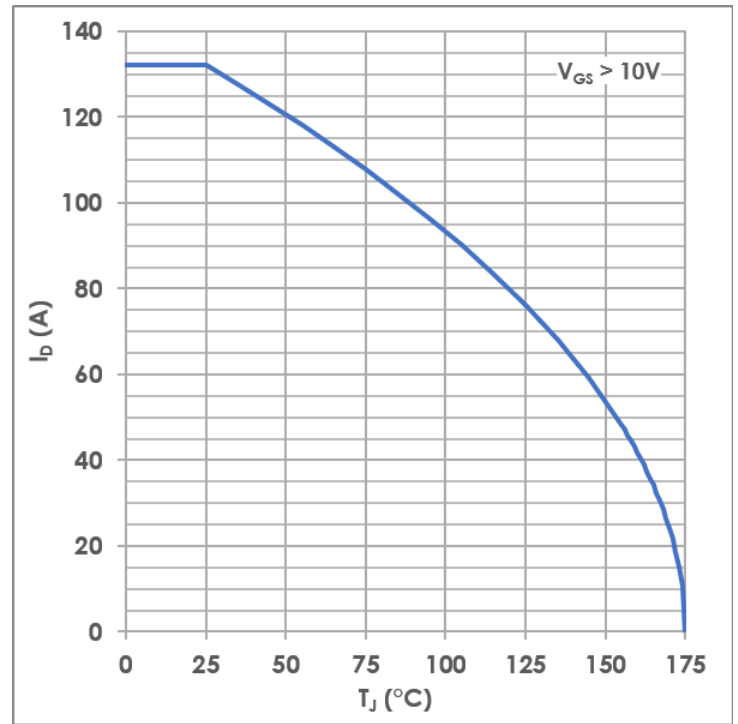


Figure 4: Drain Currents

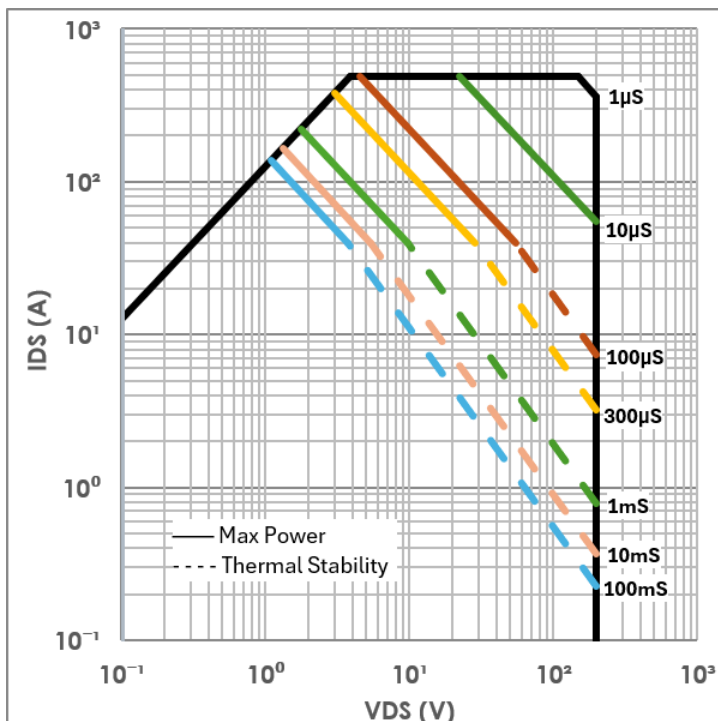


Figure 5: Safe Operating Area

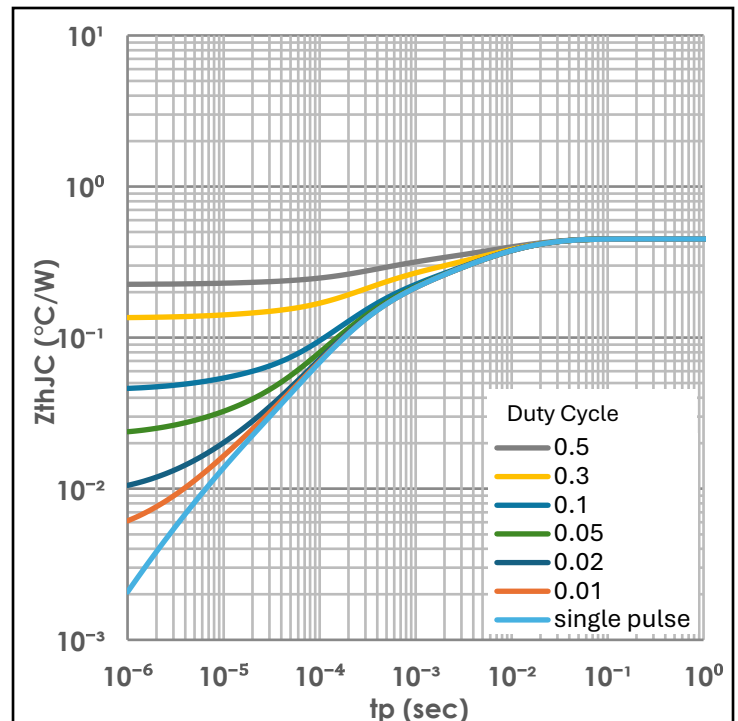


Figure 6: Max Transient Thermal Impedance

Ratings and Characteristics Curves ($T_A = 25^\circ\text{C}$ unless otherwise specified)

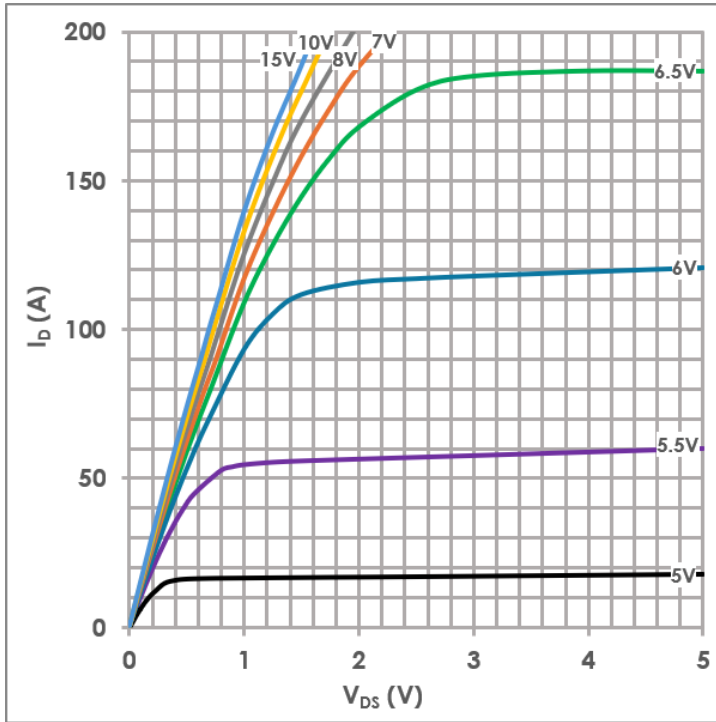


Figure 7: Typical Output Characteristics

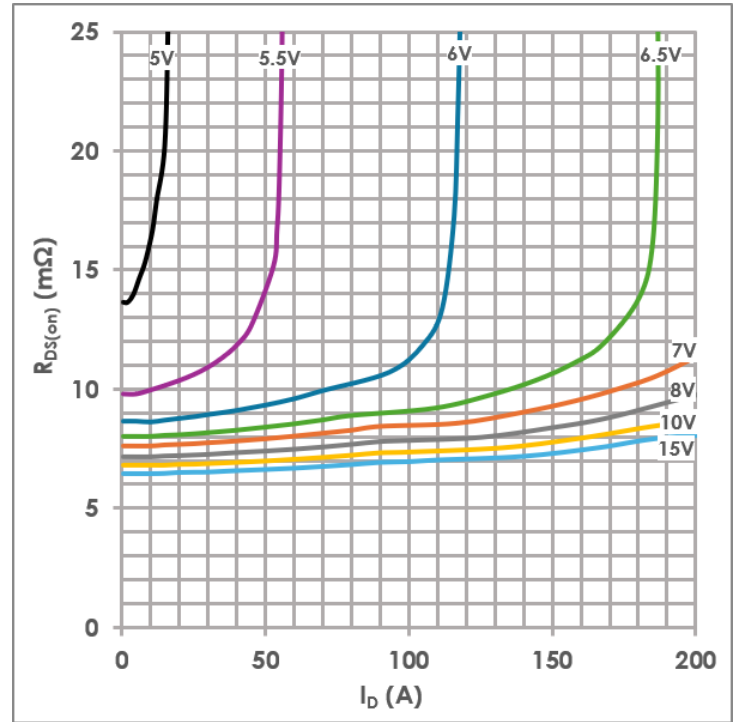


Figure 8: Typical Drain-Source On-Resistance

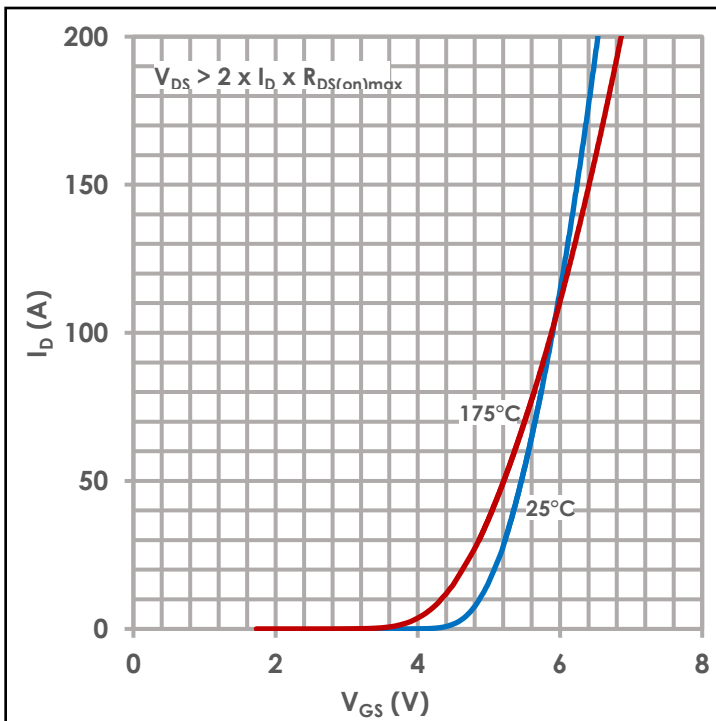


Figure 9: Typical Transfer Characteristics

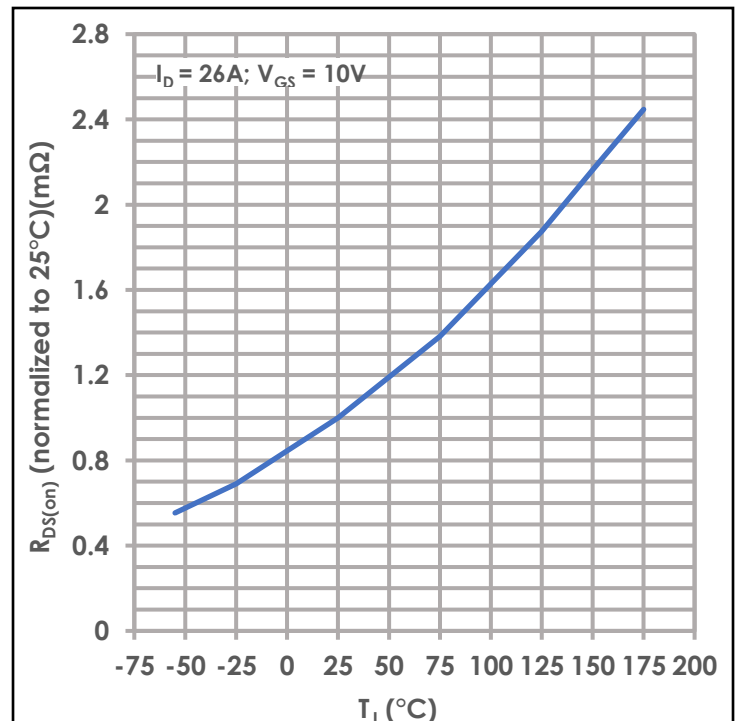


Figure 10: Normalized On-State Resistance vs. Temperature

Ratings and Characteristics Curves ($T_A = 25^\circ\text{C}$ unless otherwise specified)

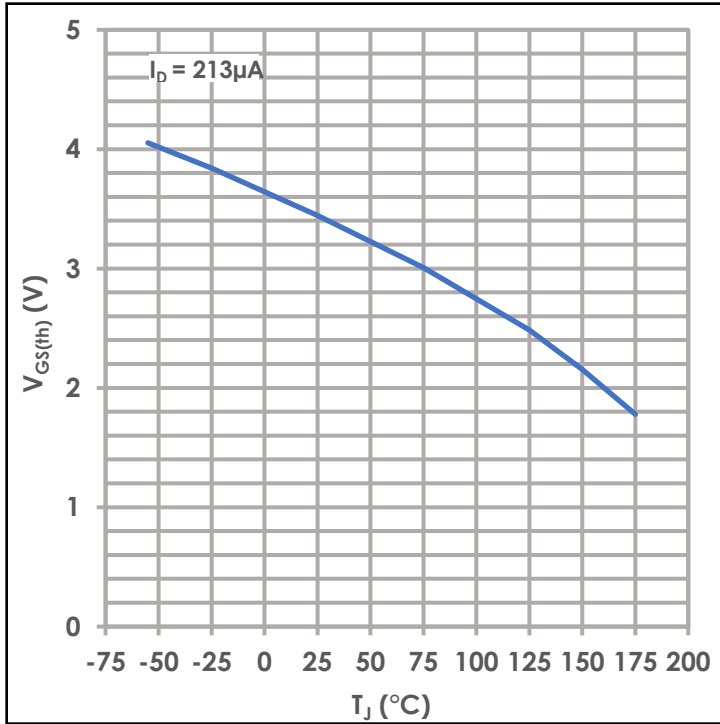


Figure 11: Typical Threshold Voltage

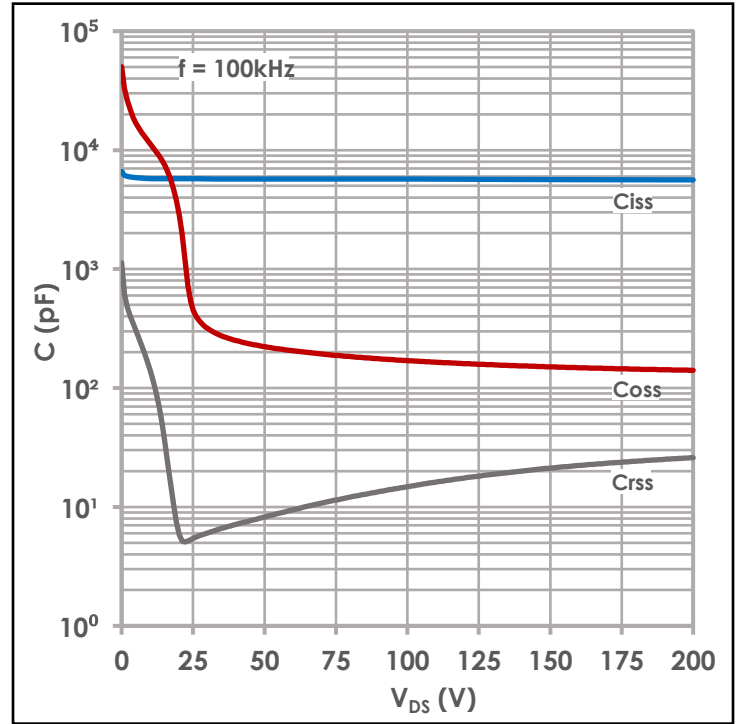


Figure 12: Typical Capacitance

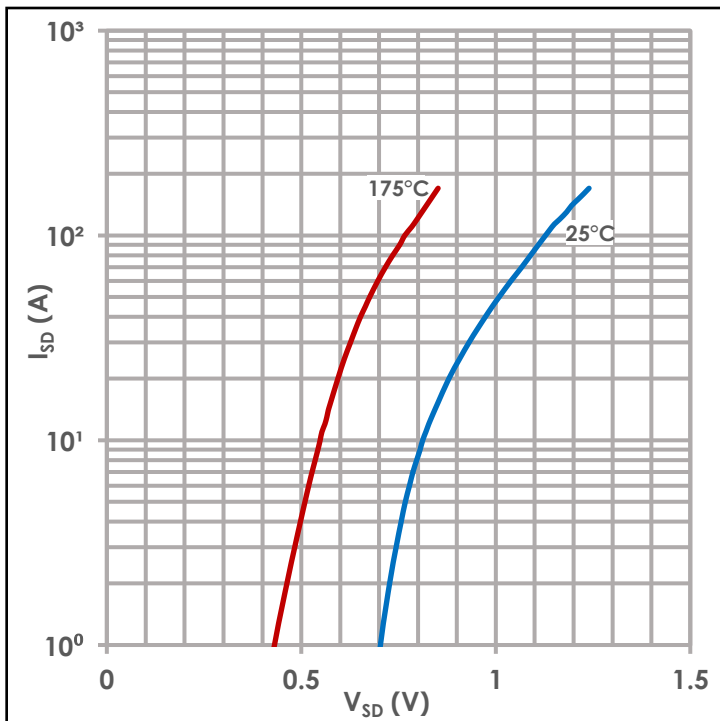


Figure 13: Typical Diode Forward Voltage

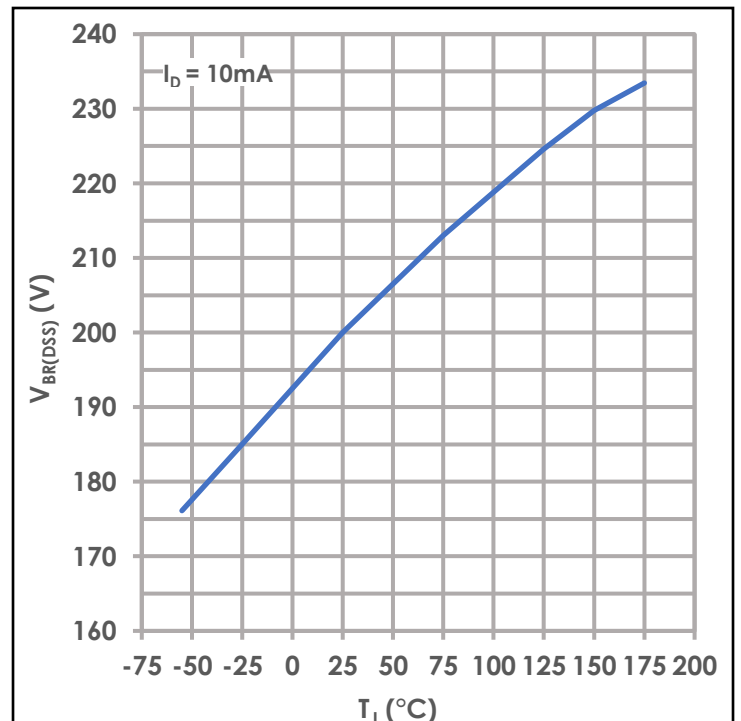


Figure 14: Min Drain-Source Breakdown Voltage

Ratings and Characteristics Curves ($T_A = 25^\circ\text{C}$ unless otherwise specified)

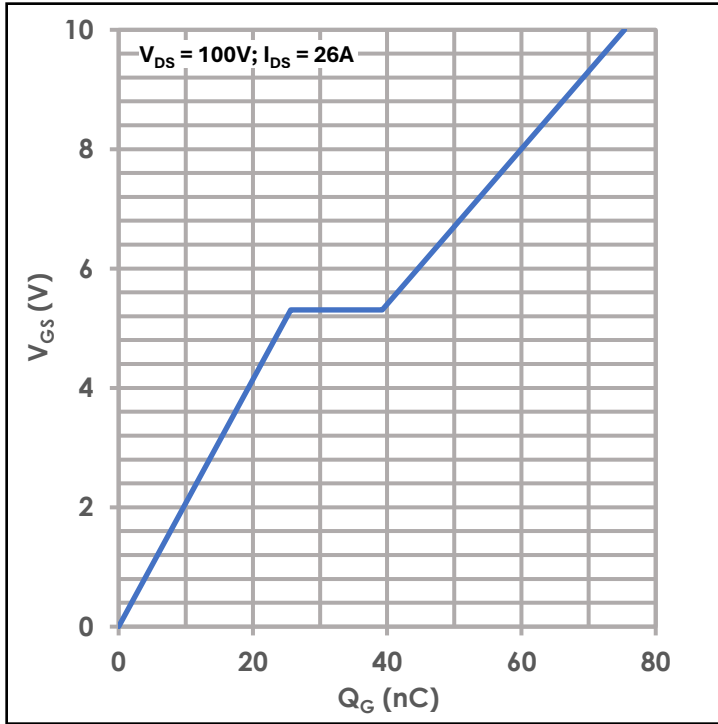


Figure 15: Typical Gate Charge

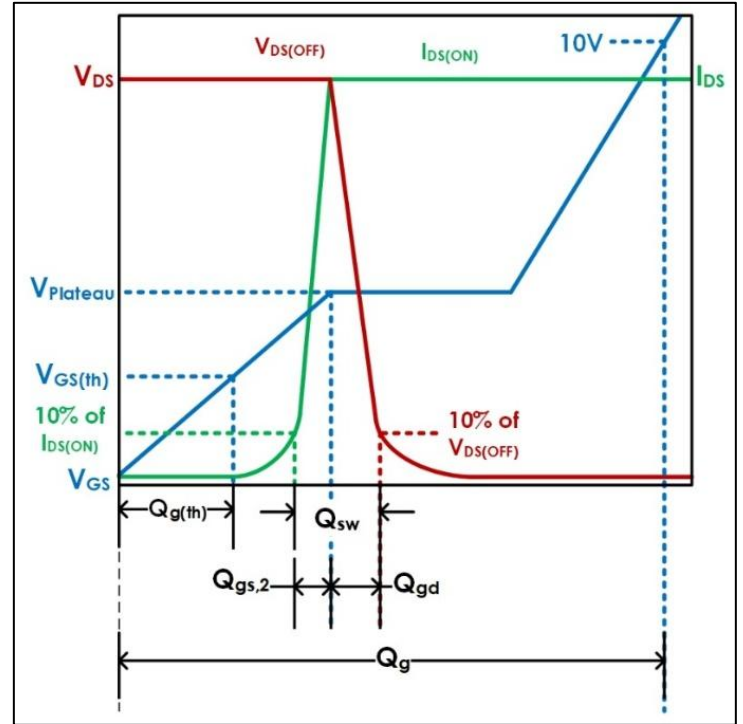
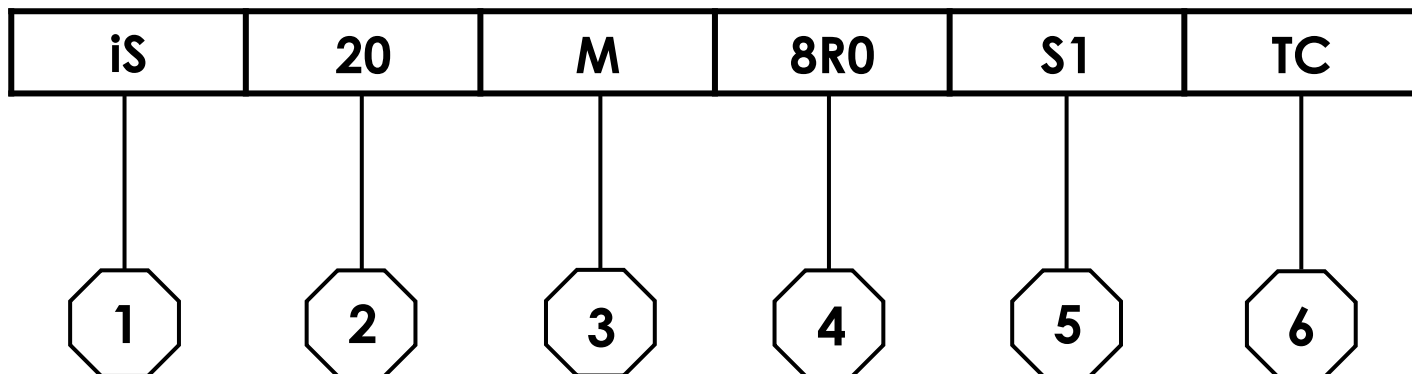


Figure 16: Gate Charge Definitions

DEVICE DECODER RING

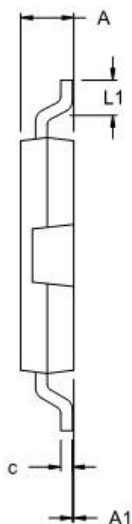
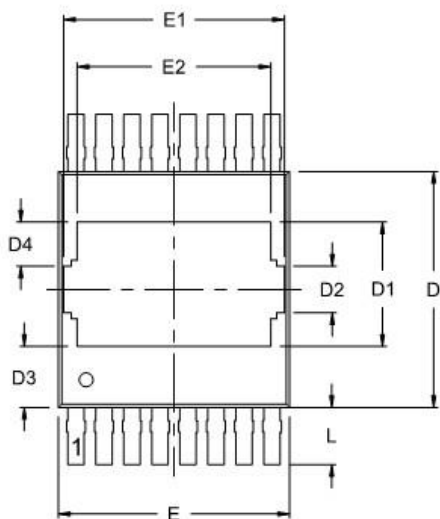
DEVICE CODE:



	— iDEAL Semiconductor product
	— Voltage rating divided by 10 (200V)
	— M = N-Channel MOSFET, Standard Threshold
	— Maximum drain-to-source resistance
	— SuperQ® Generation
	— TC = TOLT

Package Drawing

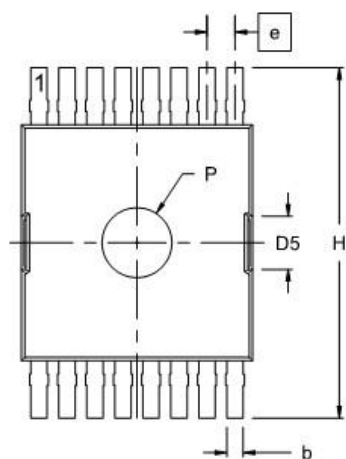
TOLT Package



SYMBOL	MIN	MAX
A	2.20	2.35
A1	0.01	0.11
b	0.60	0.85
c	0.45	0.65
D	10.00	10.30
D1	4.76	5.87
D2	1.80	2.20
D3	2.42	2.82
D4	1.33	2.44
D5	2.08	2.48
E	9.70	10.10
E1	9.26	9.66
E2	8.10	8.50
e	1.20 BSC	
H	14.80	15.20
L	2.25	2.65
L1	1.30	1.70
P	2.90	3.10

Notes:

1. All linear dimensions in millimeters



Revision History

Revision History		
Version	Date	Comments
1.0	August 2026	Initial Release

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for more information and
design resources:



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