

SuperQ™ 200V N-Channel Power MOSFET

FEATURES

- Industry leading $R_{DS(on)}$ in D2PAK-7L package
- High short-circuit withstand capability (SCWC)
- 100% UIS tested in production
- Low switching losses, Q_{sw} and E_{oss}
- Easier parallelling with $\pm 0.5V$ gate threshold

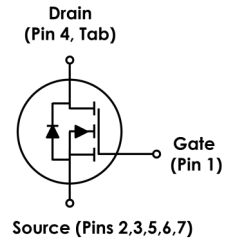
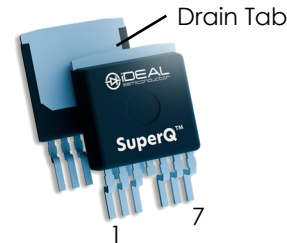
APPLICATIONS

- Motor control
- Boost converters and SMPS control FETs
- Secondary side synchronous rectifier

DESCRIPTION

Engineered for high-efficiency SMPS and motor drives, this 200V SuperQ MOSFET delivers ultra-low conduction and switching losses in a robust D2PAK-7L package. Featuring best-in-class $R_{DS(on)}$ and Q_{sw} , it minimizes heat dissipation at both full and partial loads.

PRODUCT SUMMARY



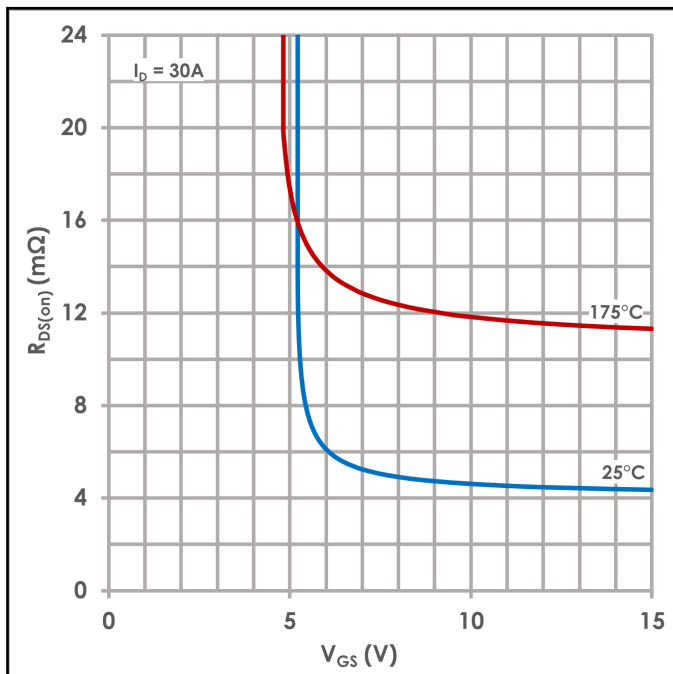
D2PAK-7L

Parameter	Value	Unit
$T_A = 25^\circ C$		
V_{DS}	200	V
$R_{DS(on),max}$	5.5	m Ω
I_D	148	A
Q_G	110	nC
Q_{sw}	7.8	nC
E_{oss}	3.9	μJ

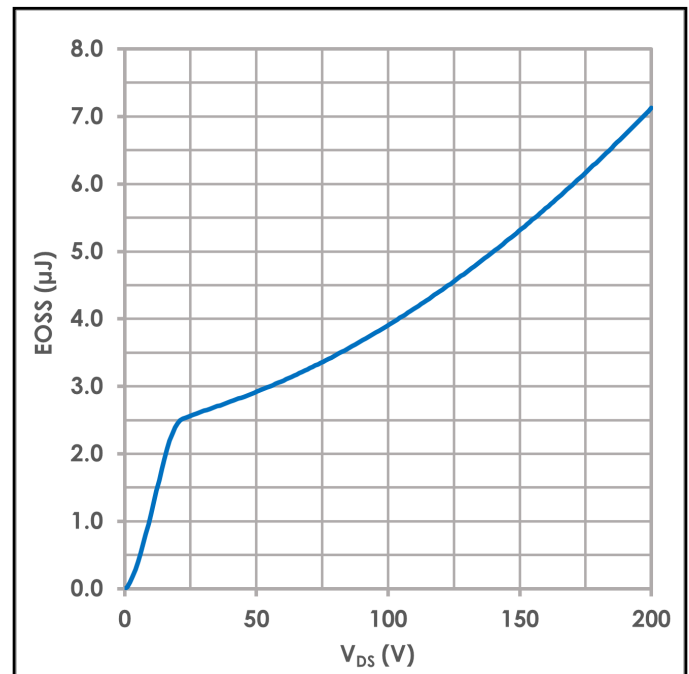


ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS20M5R5S1H	D2PAK-7L	iS20M5R5S1	13" 1,000pcs T&R



Typical Drain-Source On Resistance



Typical C_{oss} Stored Energy

ABSOLUTE MAXIMUM RATINGS			
SYMBOL	PARAMETER (T _A = 25°C unless otherwise specified)	VALUE	UNIT
V _{GS}	Gate-to-source voltage	± 20	V
I _D	Continuous drain current (silicon limited), T _C = 25°C	148	A
	Continuous drain current (silicon limited), T _C = 100°C	104	
I _{DM}	Pulsed drain current	556	A
P _D	Power dissipation, T _C = 25°C	300	W
T _J , T _{stg}	Operating junction, storage temperature	-55 to 175	°C
E _{AS}	Avalanche energy, single pulse I _D = 105A, R _{GS} = 25Ω	553	mJ

THERMAL CHARACTERISTICS					
SYMBOL	PARAMETER (T _A = 25°C unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
R _{θJC}	Junction-to-case thermal resistance - D2PAK-7L	-	-	0.5	°C/W
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	-	-	40	°C/W

(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
B _{V_{DSS}}	Drain-to-source voltage	V _{GS} = 0V, I _D = 1mA	200	-	-	V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0V, V _{DS} = 160V, T _J = 25°C	-	0.1	1	μA
		V _{GS} = 0V, V _{DS} = 160V, T _J = 125°C ⁽²⁾	-	-	100	
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0V, V _{GS} = 20V	-	2	100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 300μA	3.1	3.5	4.1	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 10V, I _D = 30A	-	4.6	5.5	mΩ
g _{fs}	Transconductance	V _{DS} = 10V, I _D = 30A	49	97	-	S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance ⁽²⁾	V _{GS} = 0V, V _{DS} = 100V, f = 100kHz	-	8,321	10,817	pF
C _{rss}	Reverse transfer capacitance ⁽²⁾		-	29	37	
C _{oss}	Output capacitance ⁽²⁾		-	239	311	
C _{o(er)}	Effective output capacitance	V _{DS} = 0 to 100V, V _{GS} = 0V	-	392	-	
R _G	Series gate resistance	f = 1MHz	-	0.7	1.1	Ω
t _{d(on)}	Turn-on delay time	V _{DS} = 100V, V _{GS} = 10V, I _{DS} = 30A, R _{G,EXT} = 0 Ω	-	21.6	-	ns
t _r	Rise time		-	6.6	-	
t _{d(off)}	Turn-off delay time		-	47.3	-	
t _f	Fall time		-	4.7	-	
GATE CHARGE CHARACTERISTICS						
Q _G	Gate charge total ⁽²⁾	V _{DS} = 100V, I _D = 30A, V _{GS} = 0 to 10V	-	110	142	nC
Q _{sw}	Switching charge ⁽³⁾		-	7.8	-	
Q _{gd}	Gate to drain charge ^{(2) (3)}		-	3.7	4.8	
Q _{G(th)}	Gate charge at threshold ⁽³⁾		-	25.0	-	
Q _{Gs2}	Gate to source charge ⁽³⁾		-	4.1	-	
V _{plateau}	Gate plateau voltage		-	5.5	-	V
Q _{oss}	Output charge ⁽²⁾	V _{DS} = 0 to 100V, V _{GS} = 0V	-	399	458	nC
E _{oss}	Capacitive stored energy		-	3.9	-	μJ
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 30A, V _{GS} = 0V	-	0.9	1.1	V
Q _{rr}	Reverse recovery charge	V _{DS} = 100V, I _F = 30A,	-	727	-	nC
t _{rr}	Reverse recovery time	di/dt = 100A/μs	-	156	-	ns

(2) Defined by design. Not subject to production test.

(3) Q_{sw} should be used for switching loss calculations. See Figure 16 for gate charge definitions. For more information see Q_{sw} application note on www.idealsemi.com

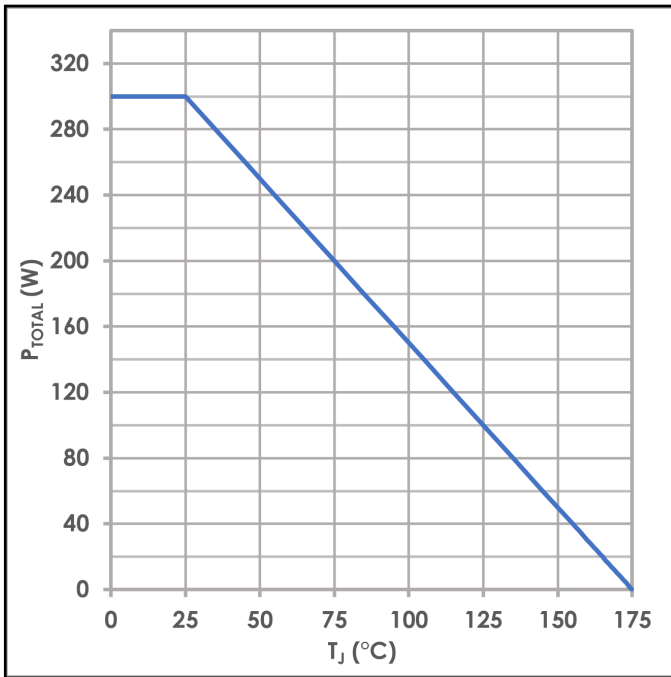


Figure 3: Power Dissipation

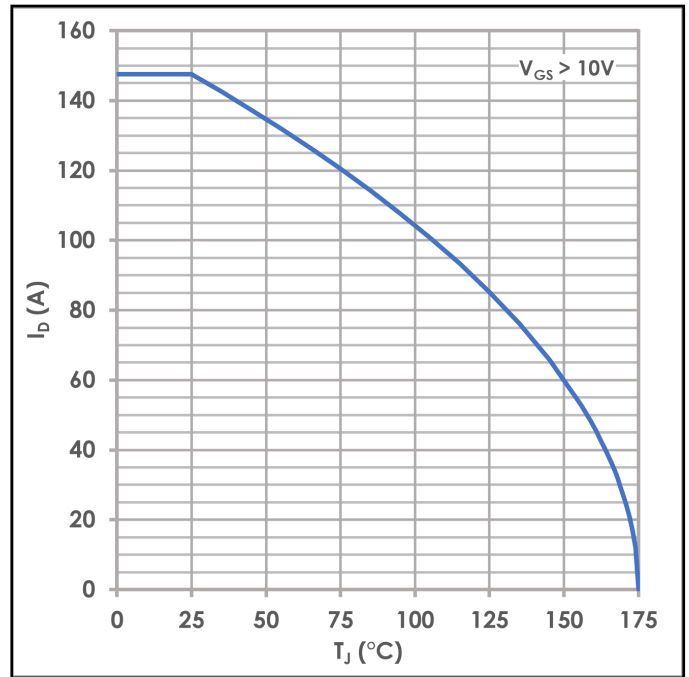


Figure 4: Drain Current

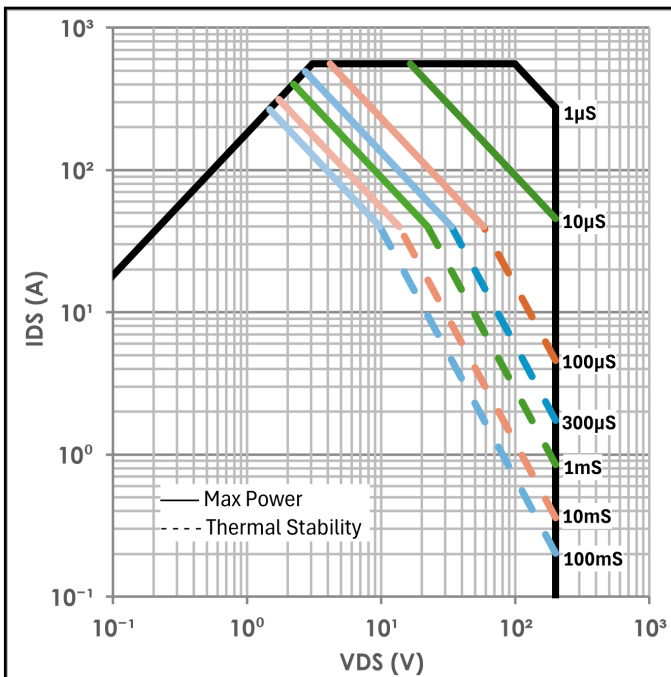


Figure 5: Safe Operating Area

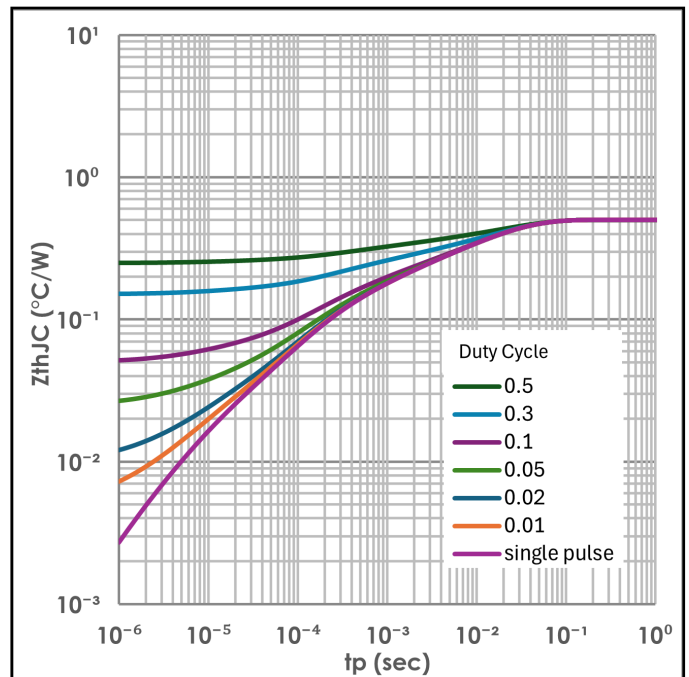


Figure 6: Max Transient Thermal Impedance

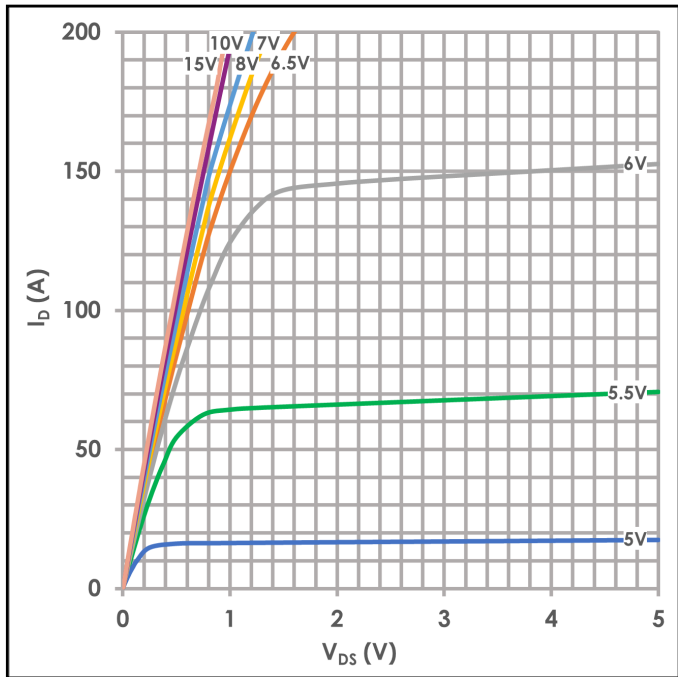


Figure 7: Typical Output Characteristics

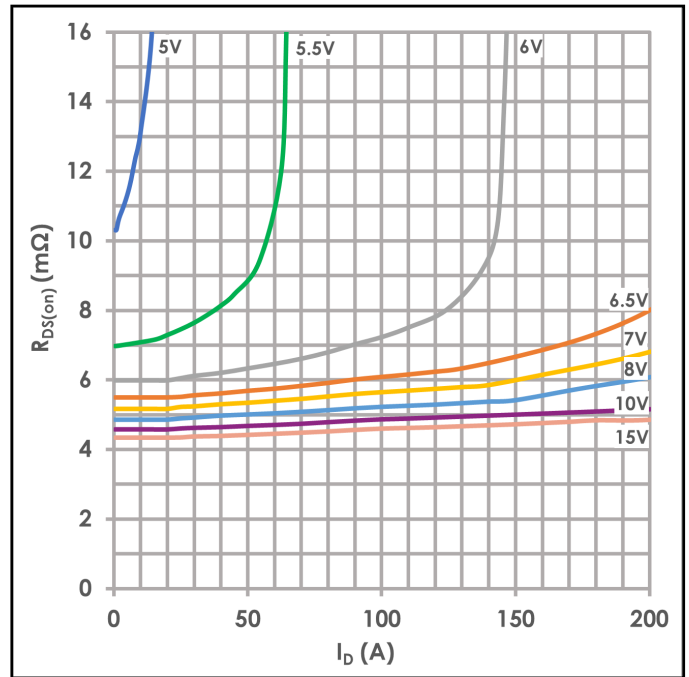


Figure 8: Typical Drain-Source On-Resistance

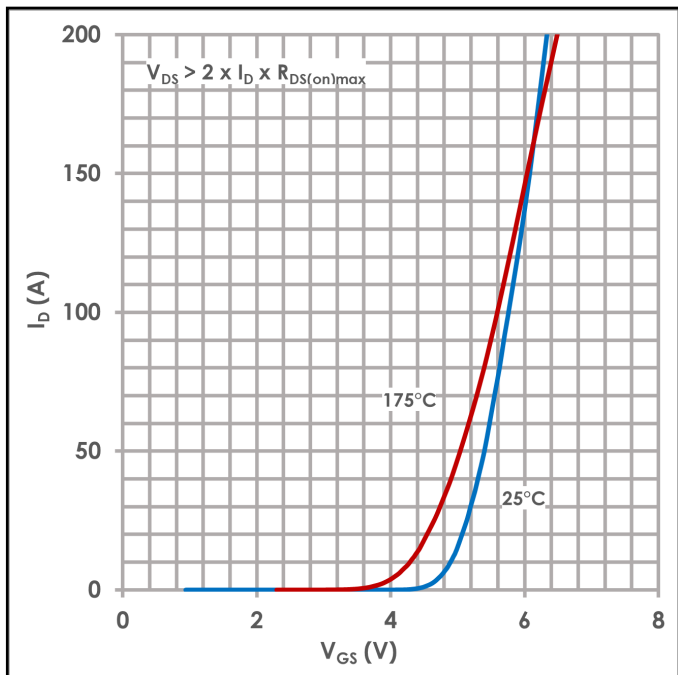


Figure 9: Typical Transfer Characteristics

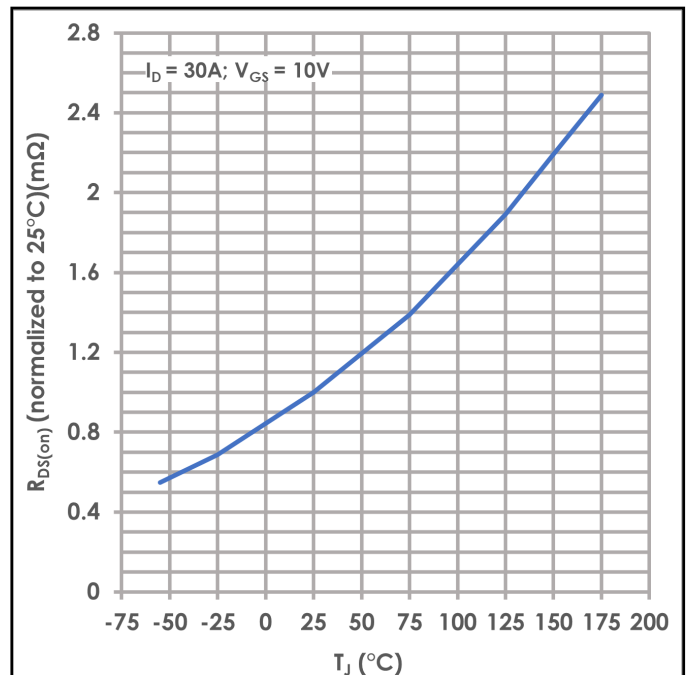


Figure 10: Normalized On-State Resistance vs. Temperature

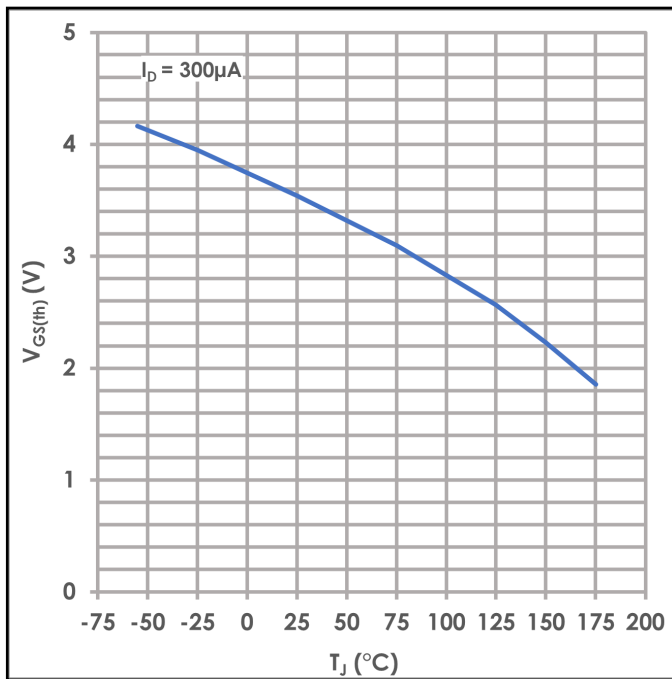


Figure 11: Typical Threshold Voltage

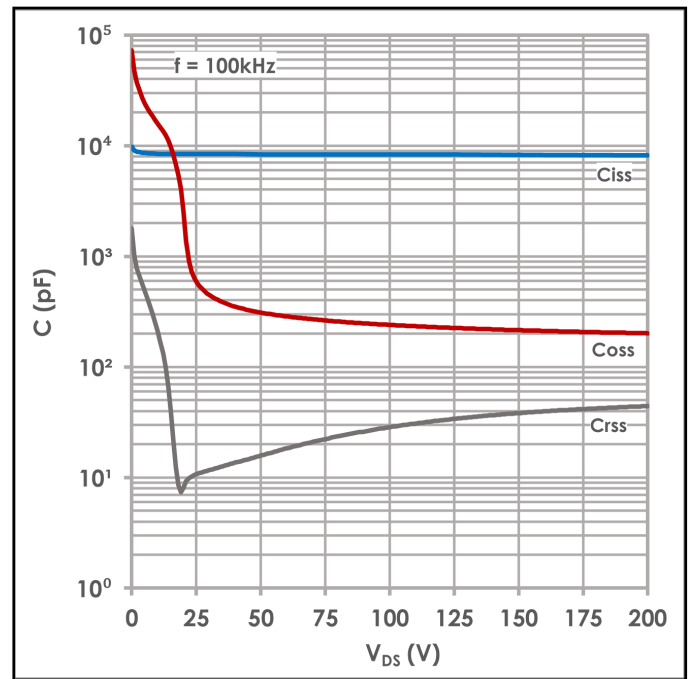


Figure 12: Typical Capacitances

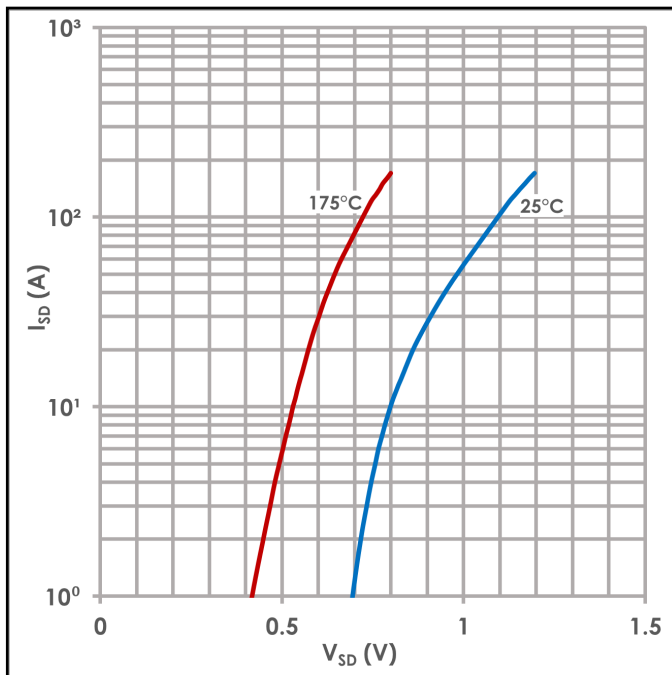


Figure 13: Typical Diode Forward Voltage

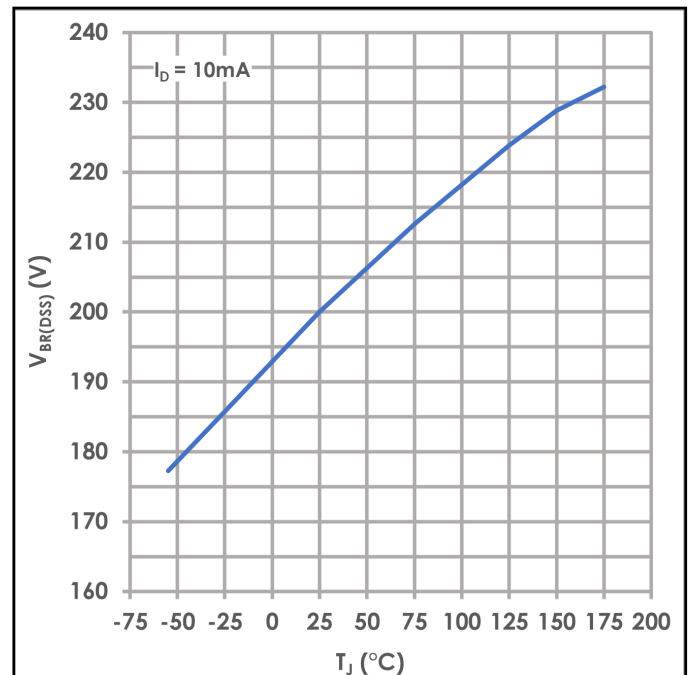


Figure 14: Min Drain-Source Breakdown Voltage

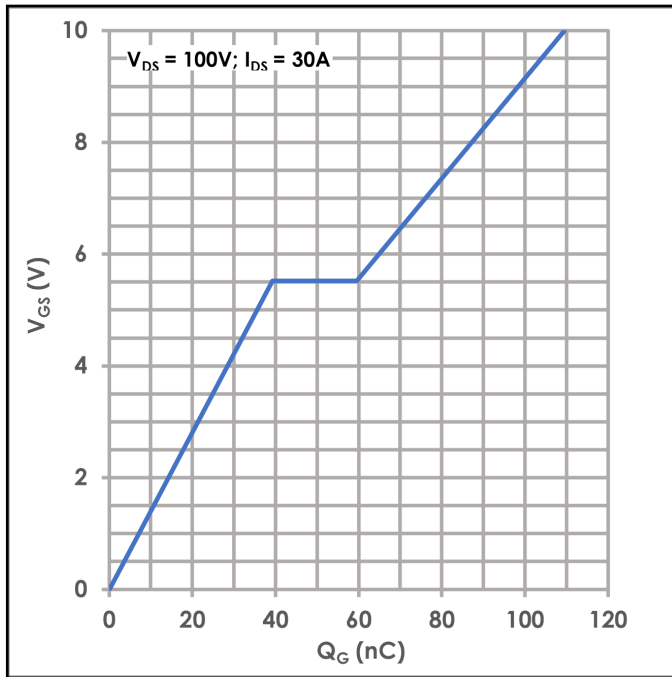


Figure 15: Typical Gate Charge

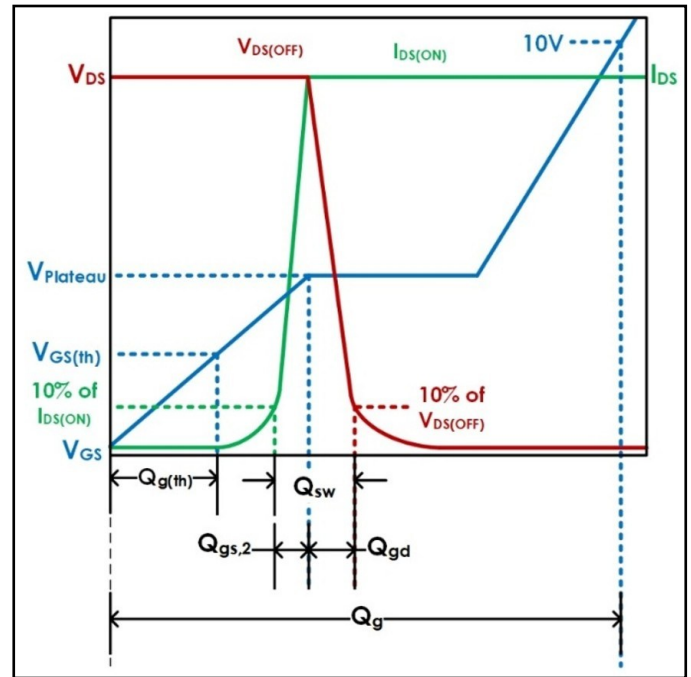
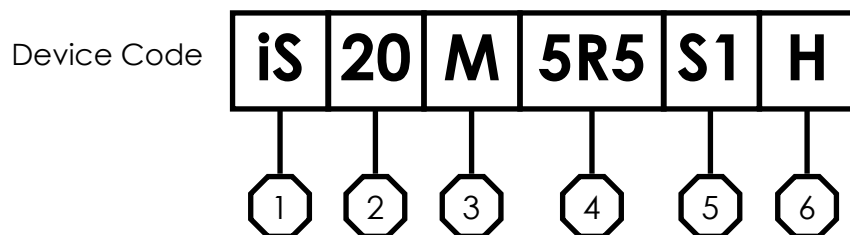








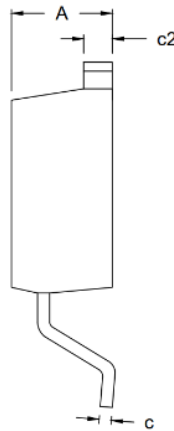
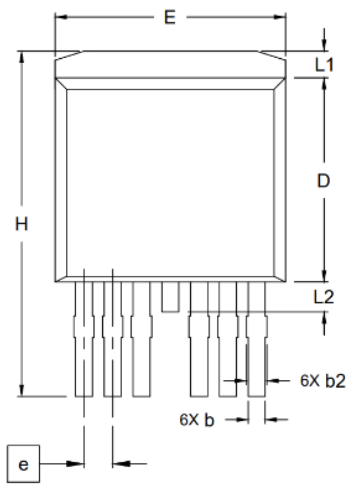
Figure 16: Gate Charge Definitions

DEVICE DECODER RING



-  — iDEAL Semiconductor product
-  — Voltage rating divided by 10 (200V)
-  — M = N-Channel MOSFET, Standard Threshold
-  — Maximum drain-to-source resistance
-  — SuperQ™ Generation
-  — H = D2PAK-7L

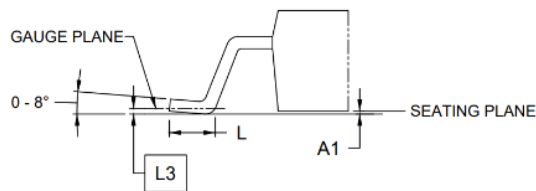
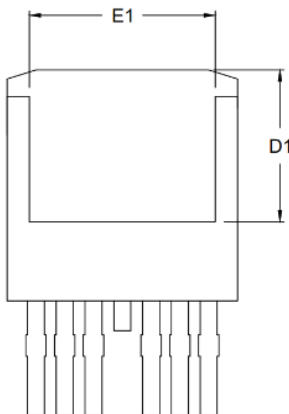
D2PAK-7L Package Drawing



SYMBOL	MIN	MAX
A	4.30	4.70
A1	--	0.25
b	0.50	0.85
b2	0.80	1.00
c	0.40	0.65
c2	1.20	1.40
D	8.50	9.40
D1	6.86	--
E	9.65	10.10
E1	6.50	--
e	1.27 BSC	
H	14.61	15.88
L	1.78	2.79
L1	--	1.60
L2	--	1.78
L3	0.25 BSC	

Notes:

1. All linear dimensions in millimeters
2. Dimensions D and E do not include mold flash or protrusions



Revision History		
Version	Date	Comments
1.0	April 2026	Initial Release

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