

SuperQ™ 150-V N-Channel Power MOSFET

FEATURES

- Low on-resistance, $R_{DS(on)}$
- Ultra low energy stored, E_{oss}
- Ultra low turn-off energy, E_{off}
- Optimized Q_{sw} for hard switching
- Low reverse recovery time T_{rr} and Q_{rr}

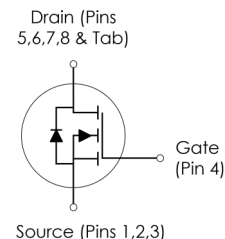
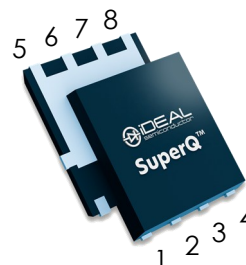
APPLICATIONS

- Boost converters and SMPS control FETs
- Secondary side synchronous rectifier
- Motor control

DESCRIPTION

This 150V, 5.4mΩ_{TYP} SuperQ power MOSFET is designed to minimize losses in SMPS applications through leading $R_{ds,on}$, ultra low energy storage, fast turn-off time and minimal switching charge.

PRODUCT SUMMARY



PDFN 5x6mm

Parameter	Value	Unit
$T_A = 25^\circ\text{C}$		
V_{DS}	150	V
$R_{DS(on),max}$	6.4	mΩ
I_D	133	A
Q_G	48	nC
Q_{sw}	4.9	nC
E_{oss}	1	μJ



ORDERING INFORMATION

Part Number	Package	Marking	Packaging
iS15M7R1S1C	PDFN 5X6	15M7R1S1	13" 5,000pcs T&R

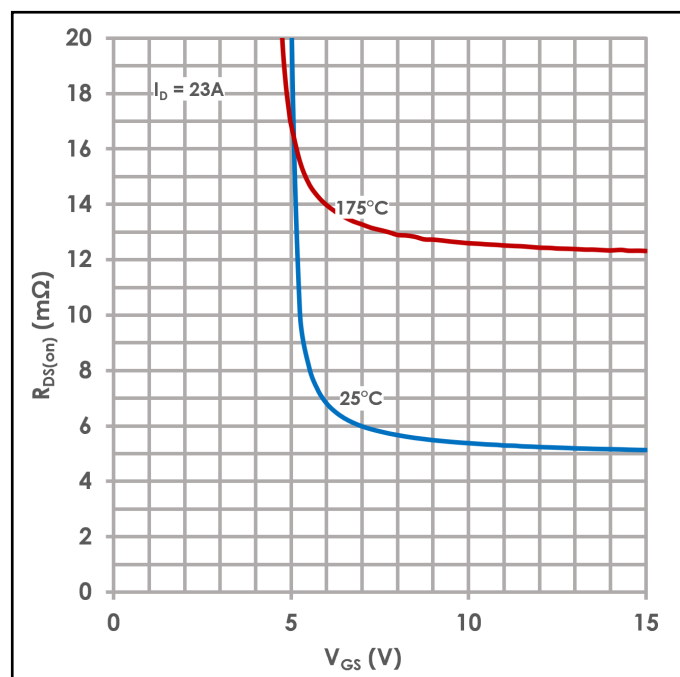


Figure 1: Typical Drain-Source On Resistance

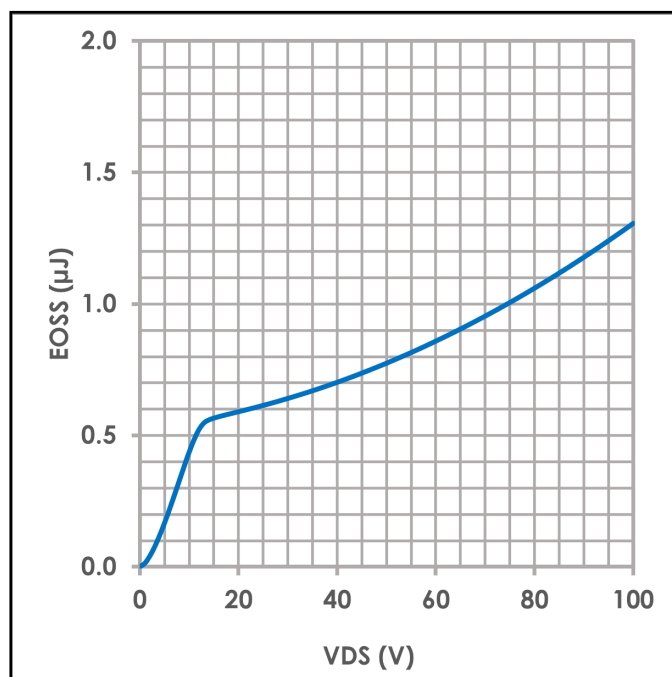


Figure 2: Typical COSS Stored Energy

ABSOLUTE MAXIMUM RATINGS			
SYMBOL	PARAMETER (T _A = 25°C unless otherwise specified)	VALUE	UNIT
V _{GS}	Gate-to-source voltage	± 20	V
I _D	Continuous drain current (silicon limited), T _C = 25°C	133	A
	Continuous drain current (silicon limited), T _C = 100°C	94	
I _{DM}	Pulsed drain current	459	A
P _D	Power dissipation, T _C = 25°C	250	W
T _J , T _{stg}	Operating junction, storage temperature	-55 to 175	°C
E _{AS}	Avalanche energy, single pulse I _D = 11.3A, R _{GS} = 25Ω	641	mJ

THERMAL CHARACTERISTICS					
SYMBOL	PARAMETER (T _A = 25°C unless otherwise specified)	VALUE			UNIT
		MIN	TYP	MAX	
R _{θJC}	Junction-to-case thermal resistance - PDFN 5x6	-	-	0.6	°C/W
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	-	-	50	°C/W

(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0V, I _D = 1mA	150	-	-	V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0V, V _{DS} = 120V, T _J = 25°C	-	0.1	1	μA
		V _{GS} = 0V, V _{DS} = 120V, T _J = 125°C ⁽²⁾	-	-	100	
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0V, V _{GS} = 20V	-	1	100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 127μA	2.5	3.3	4.1	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 10V, I _D = 23A	-	5.4	6.4	mΩ
		V _{GS} = 8V, I _D = 12A	-	5.8	7.0	mΩ
g _{fs}	Transconductance	V _{DS} = 10V, I _D = 23A	41	82	-	S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance ⁽²⁾	V _{GS} = 0V, V _{DS} = 75V, f = 100kHz	-	2,949	3,893	pF
C _{rss}	Reverse transfer capacitance ⁽²⁾		-	37	64	
C _{oss}	Output capacitance ⁽²⁾		-	144	187	
C _{o(er)}	Effective output capacitance	V _{DS} = 0 to 75V, V _{GS} = 0V	-	356	-	
R _G	Series gate resistance	f = 1MHz	-	1.1	1.5	Ω
t _{d(on)}	Turn-on delay time	V _{DS} = 75V, V _{GS} = 10V, I _{DS} = 23A, R _{G,EXT} = 0 Ω	-	8.5	-	ns
t _r	Rise time		-	1.7	-	
t _{d(off)}	Turn-off delay time		-	25	-	
t _f	Fall time		-	8.4	-	
GATE CHARGE CHARACTERISTICS						
Q _g	Gate charge total ⁽²⁾	V _{DS} = 75V, I _D = 23A, V _{GS} = 0 to 10V	-	48	63	nC
Q _{sw}	Switching charge ⁽³⁾		-	4.9	-	
Q _{gd}	Gate to drain charge ⁽²⁾⁽³⁾		-	3	4.2	
Q _{g(th)}	Gate charge at threshold ⁽³⁾		-	8.6	-	
Q _{gs2}	Gate to source charge ⁽³⁾		-	1.9	-	
V _{plateau}	Gate plateau voltage		-	5.2	-	V
Q _{oss}	Output charge ⁽²⁾	V _{DS} = 0 to 75V, V _{GS} = 0V	-	132	170	nC
E _{oss}	Capacitive stored energy		-	1	-	μJ
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 23A, V _{GS} = 0V	-	0.8	1.0	V
Q _{rr}	Reverse recovery charge	V _{DS} = 75V, I _F = 23A, di/dt = 100A/μs	-	107	-	nC
t _{rr}	Reverse recovery time		-	74	-	ns

(2) Defined by design. Not subject to production test.

(3) Q_{sw} should be used for switching loss calculations. See Figure 16 for gate charge definitions. For more information see Q_{sw} application note on www.idealsemi.com

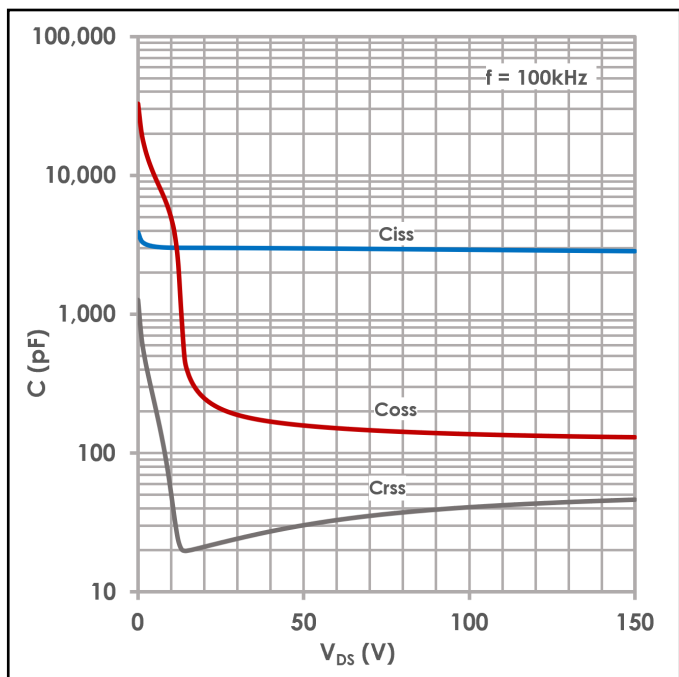


Figure 3: Typical Capacitances

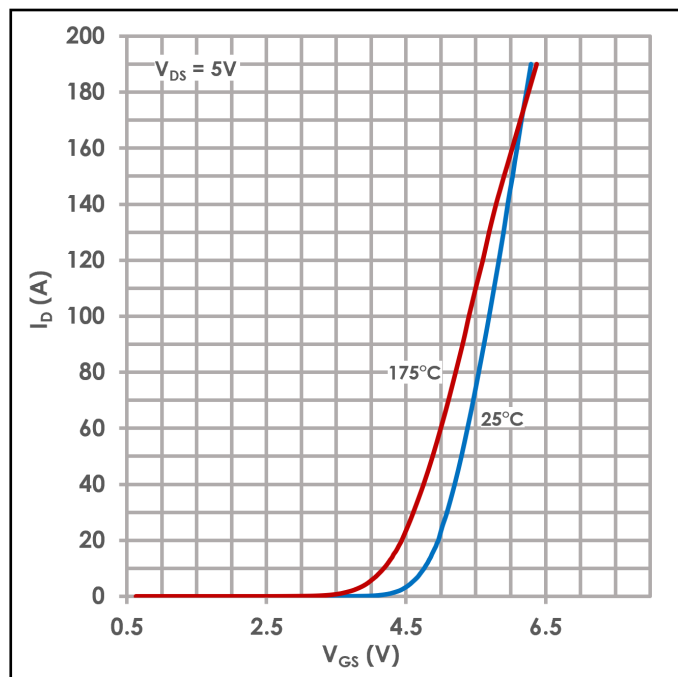


Figure 4: Typical Transfer Characteristics

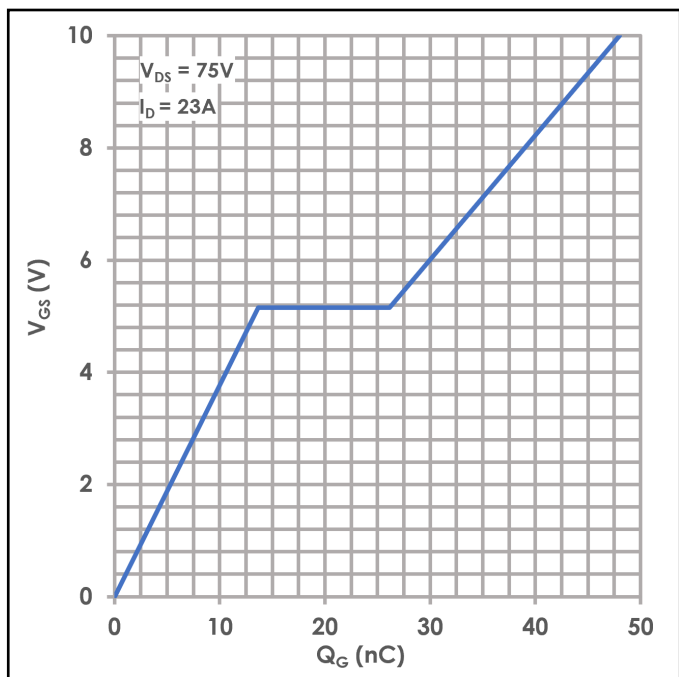


Figure 5: Typical Gate Charge

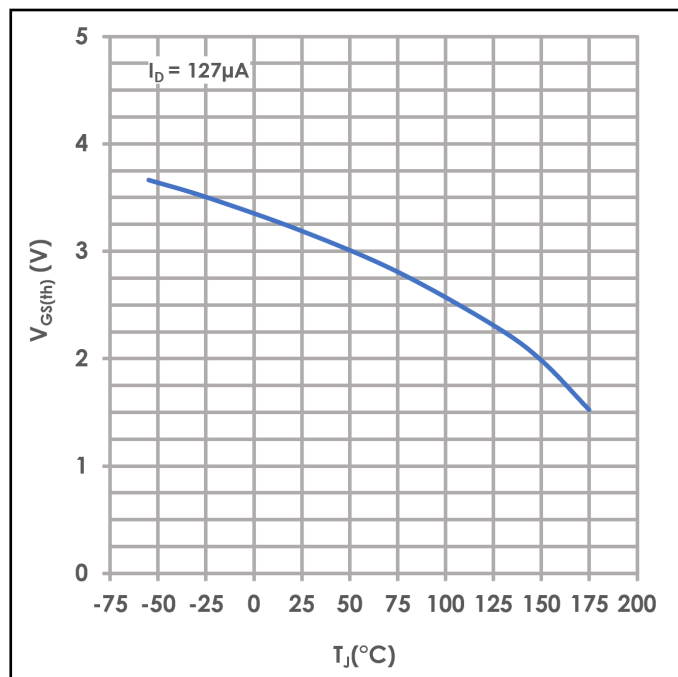


Figure 6: Typical Threshold Voltage

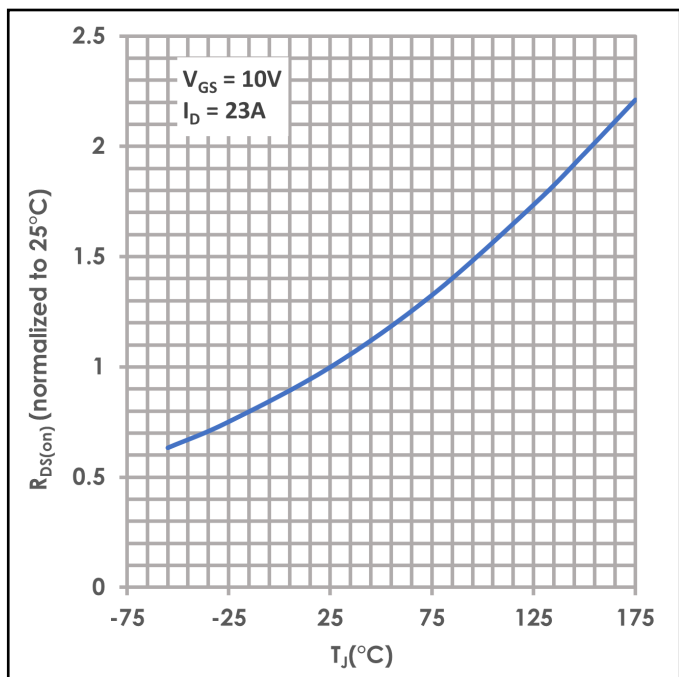


Figure 7: Normalized On-State Resistance vs. Temperature

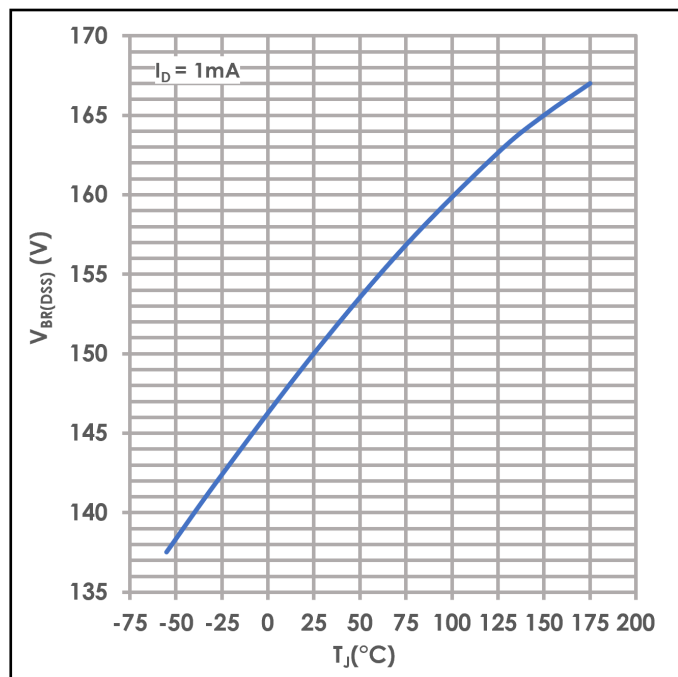


Figure 8: Drain-Source Breakdown Voltage

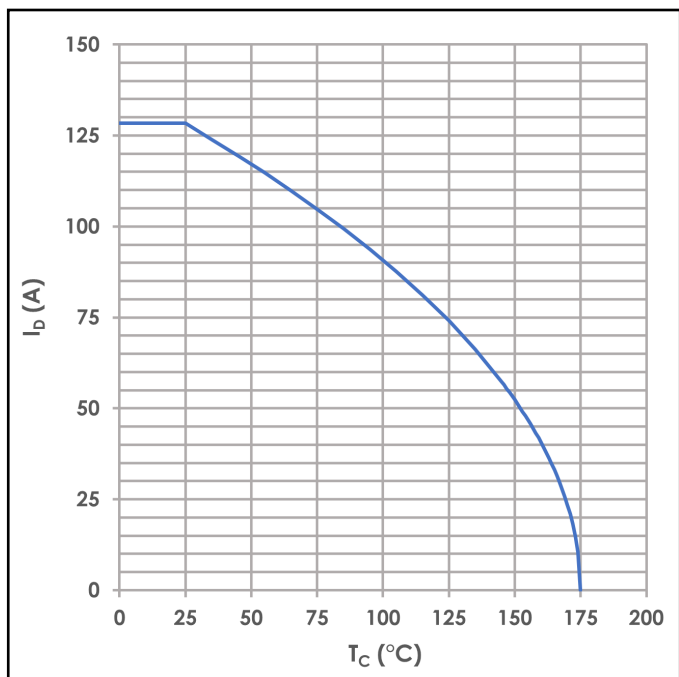


Figure 9: Drain Current

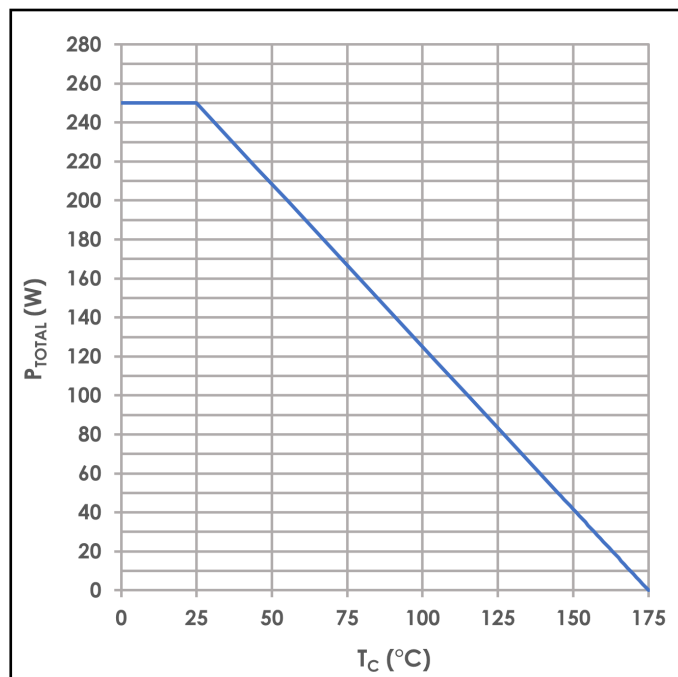


Figure 10: Power Dissipation

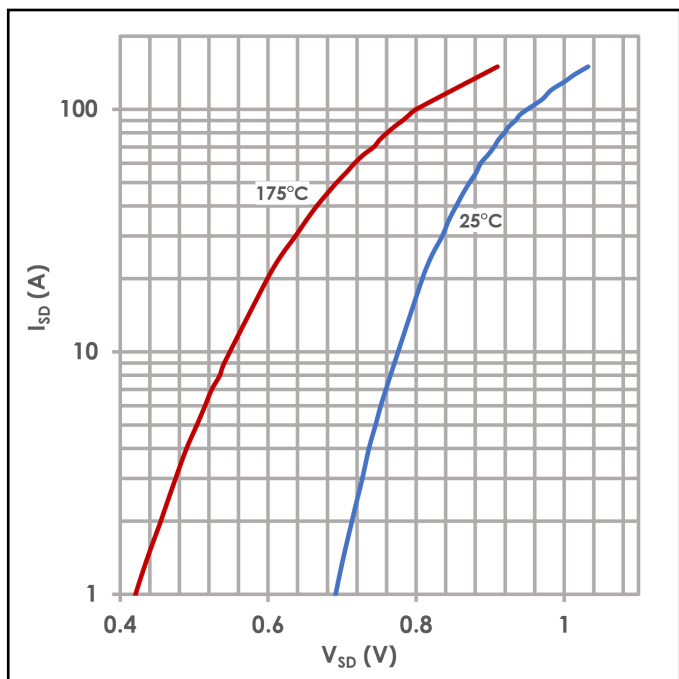


Figure 11: Typical Diode Forward Voltage

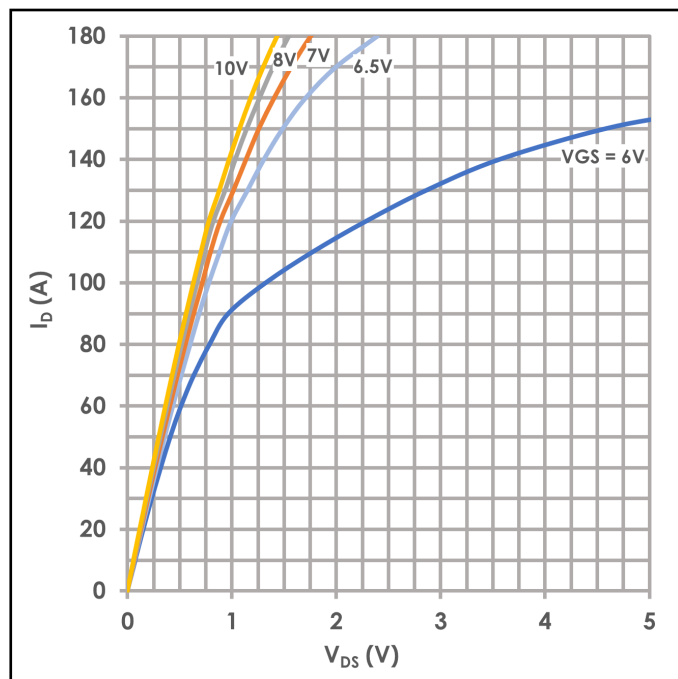


Figure 12: Typical Output Characteristics

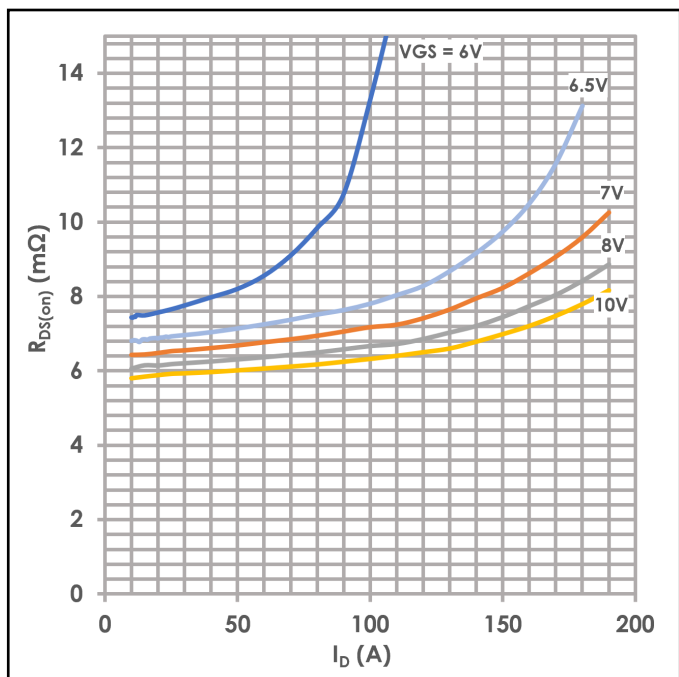


Figure 13: Typical Drain-Source On-Resistance

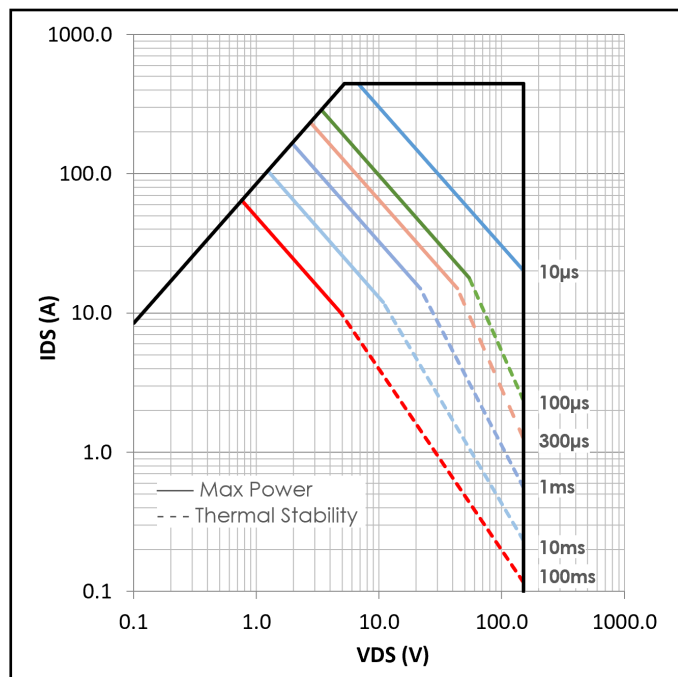


Figure 14: Safe Operating Area

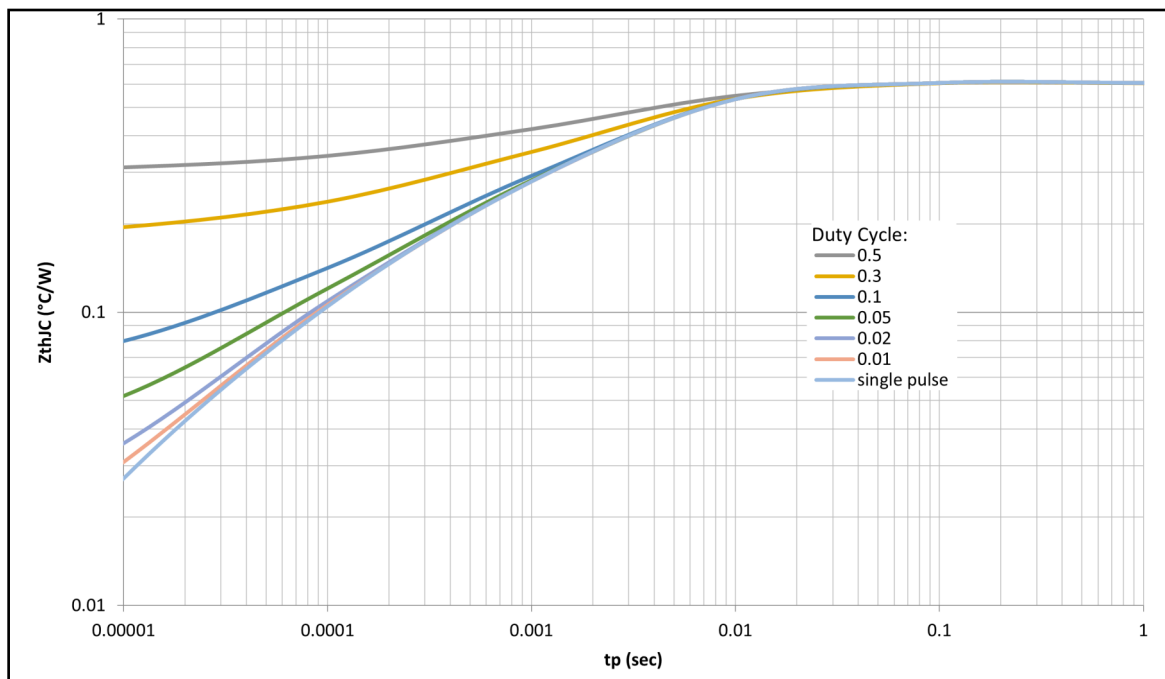


Figure 15: Max Transient Thermal Impedance

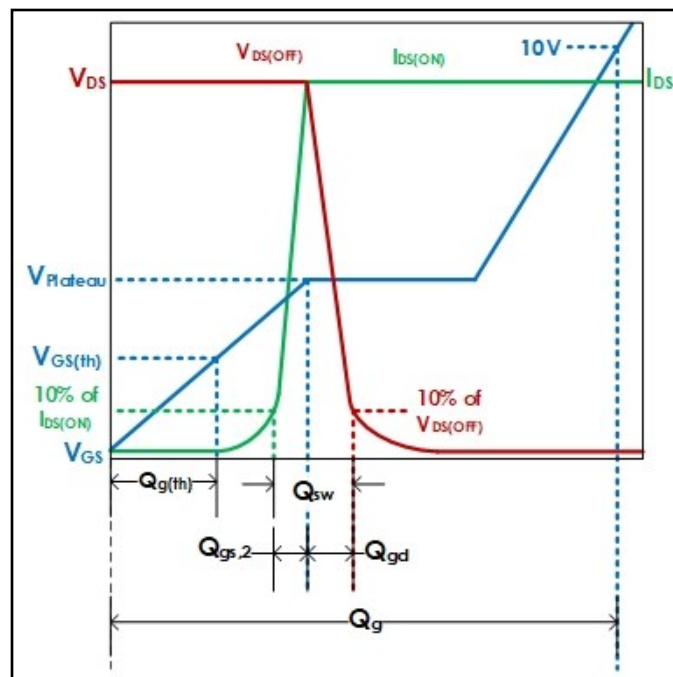
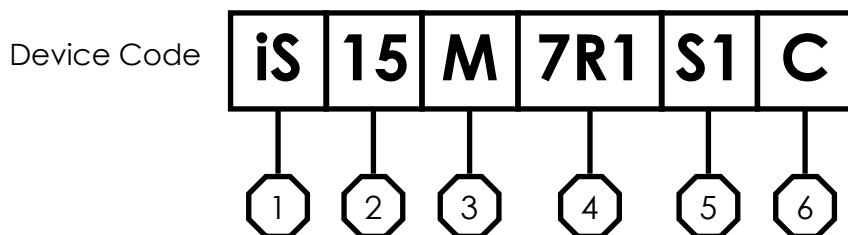


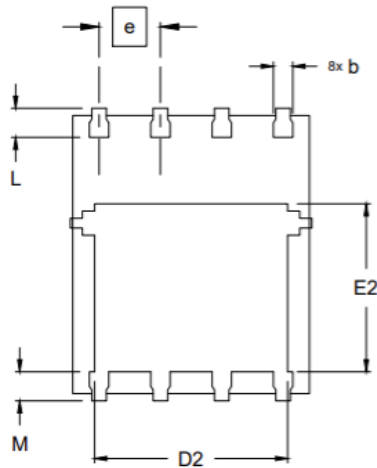
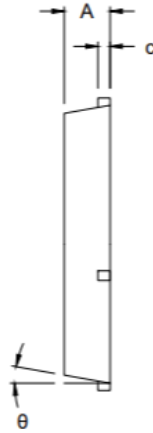
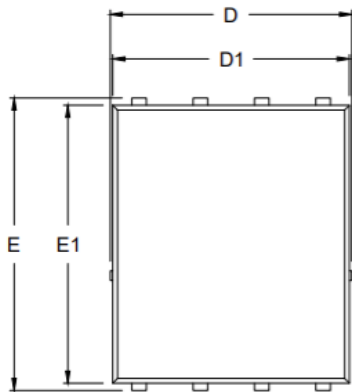
Figure 16: Gate Charge Definitions

DEVICE DECODER RING



- 1 — iDEAL Semiconductor product
- 2 — Voltage rating divided by 10 (150V)
- 3 — M = N-Channel MOSFET, Standard Threshold
- 4 — Maximum drain-to-source resistance
- 5 — SuperQ™ Generation
- 6 — C = PDFN 5x6mm

PDFN 5x6mm



SYMBOL	MIN	MAX
A	0.95	1.05
b	0.31	0.51
c	0.25 REF	
D	4.94	5.30
D1	4.80	5.1
D2	3.70	4.10
E	5.97	6.35
E1	5.67	6.10
E2	3.37	3.76
e	1.27 TYP	
L	0.51	0.71
M	0.51	0.73
θ	0°	10°

Revision History		
Version	Date	Comments
1.0	June 2025	Initial Release
1.1	September 2025	Gate charge characteristics table update
1.2	January 2026	Gate charge characteristics table update & Figure 16 update

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