IS32LT3132

12 CHANNELS, LINEAR LED DRIVER WITH UART INTERFACE

August 2025

1 GENERAL DESCRIPTION

The IS32LT3132 is a linear programmable current regulator featuring 12 high-side output channels, with each channel capable of up to 100mA. It is equipped with a UART interface that is compatible with CAN PHY for communication with a master microcontroller or ECU. The host microcontroller employs a command and response protocol to effectively manage the read and write operations of registers on one or multiple IS32LT3132 devices. Each output can individually support 12-bit PWM dimming and 8-bit DC current adjustment. The output channels can be combined to provide a higher current drive capability up to a maximum of 1.2A.

For added system reliability, the IS32LT3132 integrates fault detection circuitry for open/short string, single LED short, and over temperature conditions. Faults are recorded in registers which can be accessed by an external MCU. To optimize EMI performance, the IS32LT3132 features spread spectrum on the internal PWM and LED channel outputs have programmable slew rate control and phase delay to mitigate EMI and power supply inrush current.

The IS32LT3132 is targeted at pixel-controlled automotive lighting market, such as interior and exterior animation light. It is offered in a thermally enhanced eTSSOP-24 and WFQFN-32 (5mm×5mm) packages.

2 APPLICATIONS

- Automotive LED Lighting
  - Animation taillight
  - Animation daytime running light
  - Cluster display

3 FEATURES

- Wide input voltage supply from 4.5V to 16V
- UART Communication Interface with LumiBus protocol
  - UART compatible with CAN physical layer, 100kbps~1Mbps baud rate
  - CRC to ensure robustness of communication
  - Support up to maximum 64 addressable devices
  - Watchdog timer to support fail-safe mode
- 12 channels high-side current output
  - Up to 100mA channel current set by resistor
  - ±3% device-to-device output current accuracy
  - Combined for higher current capability with same current accuracy
  - Low headroom voltage of 650mV (Typ.) at 100mA
- Individual PWM dimming to each channel
  - 4096 steps (12-bit) PWM duty cycle setting
    - 7+5-bit
    - 12-bit
    - 8-bit
  - Phase delay minimizes inrush current (6 groups)
- Programmable PWM frequency up to 64kHz
- Current slew rate control and spread spectrum optimize EMI performance
- Individual 8-bit DC current adjustment to each channel
- 64-step global DC current setting
- Fault protection with reporting
  - Fail safe modes selection
  - LED string open/short detect
  - Single LED short detect
  - Programmable fault reporting delay time
  - Programmable over temperature current roll off
  - Thermal shutdown
  - CRC error detection
  - Overcurrent (ISET pin short to GND)
  - ISET pin open
  - Fault pin pull down fault
  - LED undervoltage
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C
- Operating temperature range (-40°C ~ +150°C)
- eTSSOP-24 and WFQFN-32 (5mm×5mm) packages
- RoHS & Halogen-Free Compliance
- TSCA Compliance

4 TYPICAL APPLICATION CIRCUIT

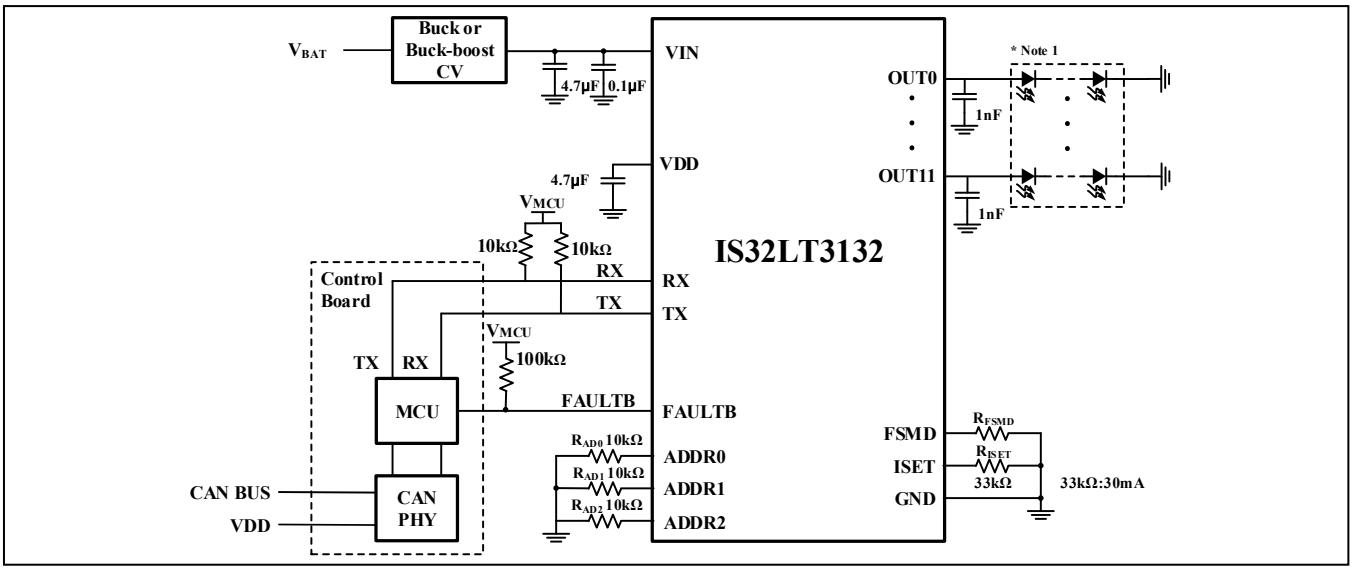


Figure 1 Typical Application Circuit of IS32LT3132 with UART Interface

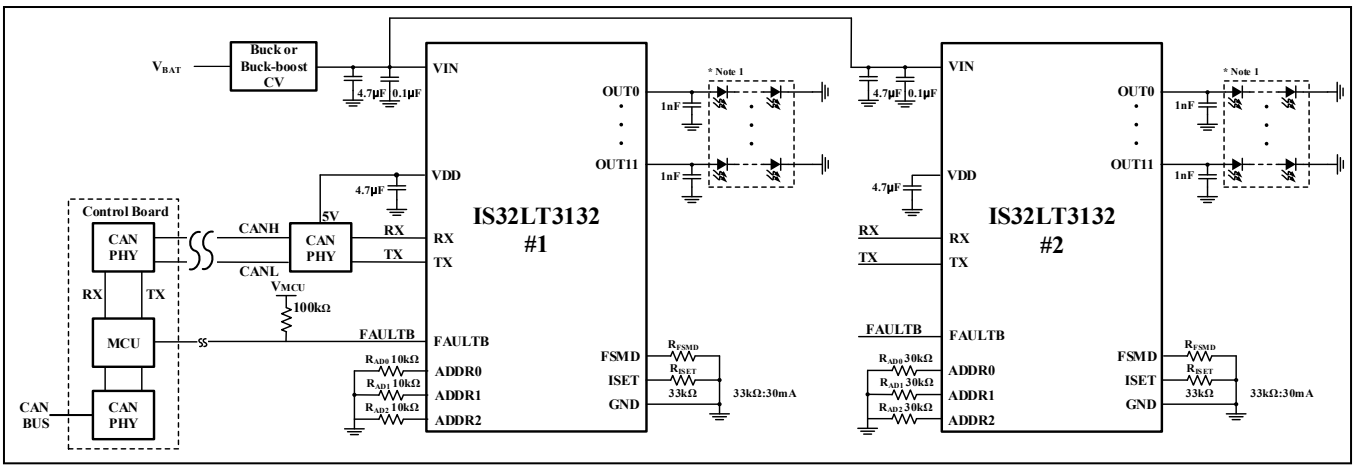


Figure 2 Typical Application Circuit of Multiple IS32LT3132 with External CAN Transceiver for Off-board Long Distance Communication

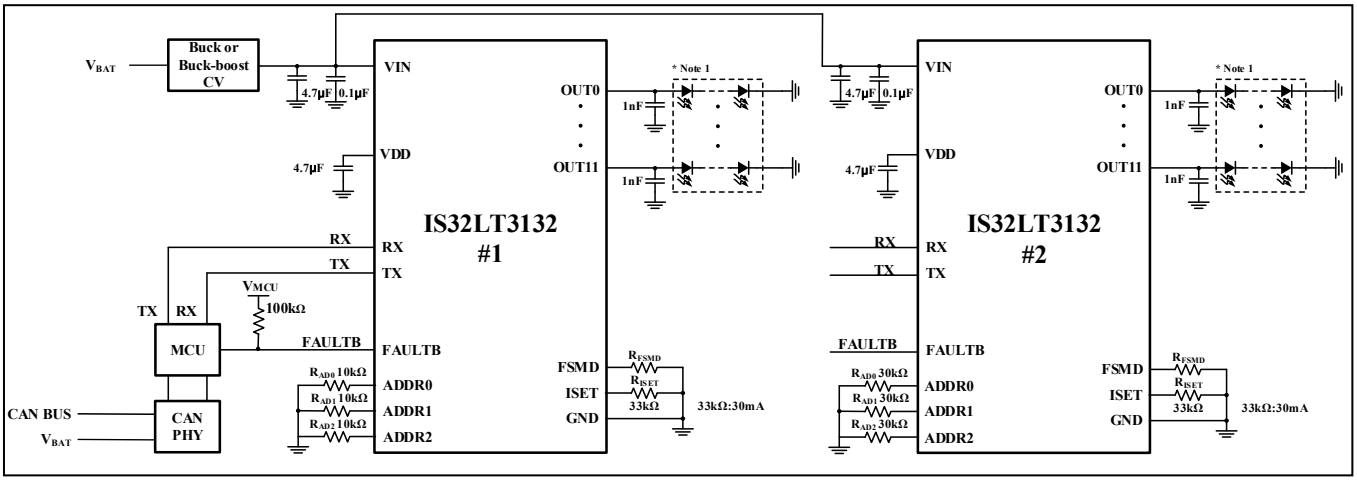
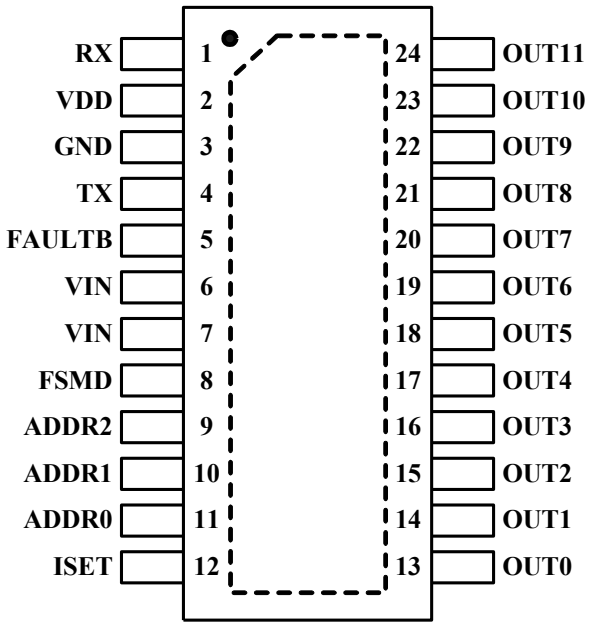
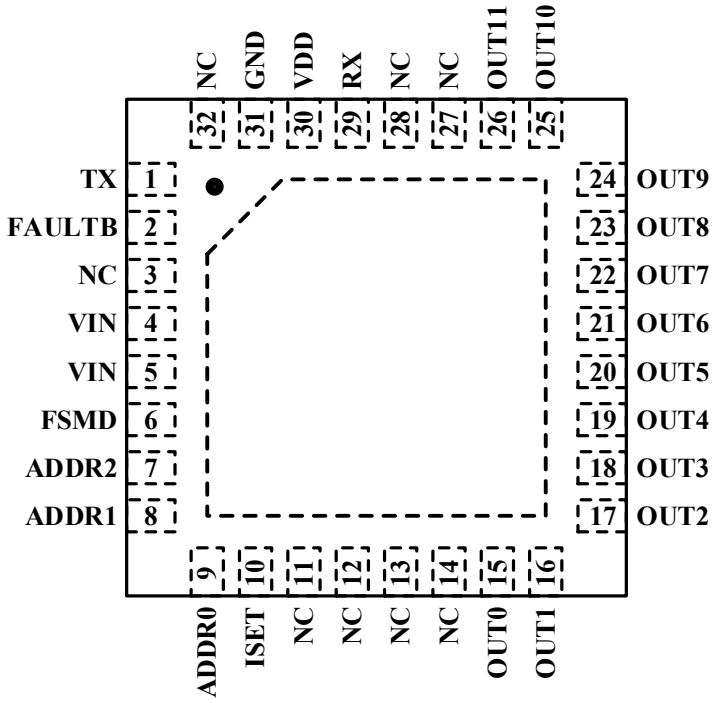


Figure 3 Typical Application Circuit of Multiple IS32LT3132 with UART Interface for On-board Communication

Note 1: The capacitors C_{OUT0}~C_{OUT11} are recommended for most applications. These capacitors must be placed as close to the corresponding OUTx pin as possible to optimize the EMI and ESD performance, especially the LEDs are connected to OUTx with long wires. The recommended value is 1nF.

5 PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-24	
WFQFN-32	

PIN DESCRIPTION

No.		Pin	Description
eTSSOP	WFQFN		
1	29	RX	UART interface received data pin.
2	30	VDD	5V internal LDO output. Connect a 4.7μF X7R ceramic capacitor to GND.
3	31	GND	Ground pin.
4	1	TX	UART interface transmitted data pin.
5	2	FAULTB	Open drain fault reporting pin. In the “One Fail All Fail” mode, this pin also is an input pin. Pulling this pin low will disable the outputs.
6~7	4~5	VIN	Power supply input.
8	6	FSMD	Connect different value resistor to GND to select fail safe mode.
9~11	7~9	ADDR2~ADDR0	Address setting. Connect a proper valued resistor from this pin to GND to assign the address.
12	10	ISET	Resistor on this pin to GND sets the maximum output current for channel OUT0~OUT11.
13~24	15~26	OUT0~OUT11	Current output channels.
	3,11~14, 27~28,32	NC	Not connect.
		Thermal Pad	Must be connected to GND.

6 ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3132-ZLCA3-TR (Note 2) IS32LT3132-QWLCA3-TR (Note 2)	eTSSOP-24, Lead-free WFQFN-32, Lead-free	2500

Note 2: IS32LT3132-ZLCA3-TR and IS32LT3132-QWLCA3-TR are with copper wire bonding.

7 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

Supply voltage, VIN	-0.3V ~ 20.0V
Voltage at TX, RX, ADDRx, ISET, VDD, FSMD	-0.3V ~6V
Voltage at OUT0 to OUT11, FAULTB	+20V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	28°C/W (eTSSOP) 37.5°C/W (WFQFN)
Package thermal resistance, junction to case (bottom) (4-layer standard test PCB based on JESD 51-14), θ_{JC_BOT}	9.5°C/W (eTSSOP) 10.1°C/W (WFQFN)
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.2 ELECTRICAL CHARACTERISTICS

V_{IN}= 12V, T_J= -40°C ~125°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IN}	Supply voltage		4.5		16	V
I_{OUT}	Maximum output current	R_{ISET}= 10kΩ, GCC= 0x3F, SCAx= 0xFF, PWM= 0xFFF		100		mA
	Output current	R_{ISET}= 33kΩ, GCC= 0x3F, SCAx = 0xFF, PWM= 0xFFF		30.3		mA
ΔI_{MAT}	I_{OUT} mismatch (bit to bit) (Note 4)	I_{OUT}= 30.3mA	-3		3	%
		I_{OUT}= 100mA	-3		3	%
ΔI_{OUT}	I_{OUT} accuracy (device to device) (Note 5)	I_{OUT}= 30.3mA	-3		3	%
		I_{OUT}= 100mA	-3		3	%
V_{HR}	Headroom voltage	I_{OUT}= 100mA		0.65	1.1	V
		I_{OUT}= 30.3mA		0.4	0.7	V
I_{CC}	Quiescent power supply current	R_{ISET}= 33kΩ, GCC= 0x3F, SCAx= 0xFF, PWM= 0		4.8	5.8	mA
V_{ISET}	ISET voltage	R_{ISET}= 10kΩ, GCC= 0x3F, SCAx= 0xFF, PWM= 0xFFF	1.95	2.0	2.05	V
I_{OZ}	Output leakage current	V_{IN} =16V, V_{out} = 0V			1	μA
f_{OUT}	PWM frequency of output	Frequency setting= 32kHz, 8bit PWM mode	28.8	32	35.2	kHz
		Frequency setting= 500Hz 12bit PWM mode		500		Hz
T_{SD}	Thermal shutdown (Note 6)			168		°C
T_{SD_HYS}	Thermal shutdown hysteresis (Note 6)			13		°C

7.3 ELECTRICAL CHARACTERISTICS (CONTINUE)

V_{IN}= 12V, T_J= -40°C ~125°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{PD_FAULTB}	FAULTB pin pull-down capability	I_{SINK}= 2mA		0.1	0.2	V
I_{LKG_FAULTB}	FAULTB pin leakage current	$V_{PULL-UP}$= 16V			2	μA
V_{IH_FAULTB}	Logic “1” input voltage		2			V
V_{IL_FAULTB}	Logic “0” input voltage				0.7	V
V_{IH_RX}	Logic “1” input voltage		2			V
V_{IL_RX}	Logic “0” input voltage				0.7	V
$V_{OL(TX)}$	LOW level output voltage	I_{SINK}= 5mA			0.3	V
$V_{OH(TX)}$	High level output voltage	I_{SOURCE}=5mA	V_{DD}-0.3		V_{DD}	V
$V_{T1\_AD/FS}$	ADDR0/ADDR1/ADDR2/ FSMD threshold1		0.9	1	1.1	V
$V_{T2\_AD/FS}$	ADDR0/ADDR1/ ADDR2/ FSMD threshold2		1.85	2	2.15	V
$V_{T3\_AD/FS}$	ADDR0/ADDR1/ ADDR2/ FSMD threshold3		2.8	3	3.2	V
$I_{AD/FS}$	ADDR/FS source current		47	50	53	μA
V_{SC_FL}	LED string short detection falling threshold	Measured at OUTx to GND	0.5	0.8		V
V_{SC_RS}	LED string short detection rising threshold	Measured at OUTx to GND		1	1.3	V
V_{OC_FL}	LED string open detection falling threshold	Measured at (VIN-VOUTx)	60	200		mV
V_{OC_RS}	LED string open detection rising threshold	Measured at (VIN-VOUTx)		300	450	mV
V_{DD}	V_{DD} output voltage		4.75	5	5.2	V
I_{DD_MAX}	V_{DD} output current capability	V_{IN}> 5V, V_{DD}>4.75V			80	mA
I_{DD_LIM}	V_{DD} output current limit	V_{IN}=12V, V_{DD}=0V	100			mA
V_{DD_UV}	V_{DD} undervoltage-lockout threshold	Voltage falling, IC disabled	3.6	3.7	3.8	V
V_{DD_UVHY}	V_{DD} undervoltage-lockout hysteresis		90	190	290	mV
V_{SLSH}	Single LED short detect threshold	SLSTH (28h~2Dh) = “0010”	3.7	3.9	4.1	V
V_{F_UVLO}	Single LED short/ String open detect UVLO	FS_FLTL (2Eh) = “00000100”	7.3	7.8	8.3	V
V_{VIN_UV}	V_{IN} undervoltage-lockout threshold	Voltage falling, IC disable	3.6	3.7	3.8	V
V_{VIN_UVHY}	V_{IN} undervoltage-lockout hysteresis		90	190	290	mV
f_{OSC}	System clock frequency		31.36	32	32.64	MHz

7.4 ELECTRICAL CHARACTERISTICS (CONTINUE)

V_{IN}= 12V, T_J= -40°C ~125°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ADC (10-Bit)						
V_{REFADC}	Reference voltage		2.48	2.5	2.52	V
DNL	Differential nonlinearity	(Note 6)	-5		+5	LSB
INL	Integral nonlinearity	(Note 6)	-8		+8	LSB
RESADC	Quantization steps			1024		LSB
ADCERR	Quantification error	(Note 6)	-0.5		+0.5	LSB
t_{CONV}	Min. conversion Time (Note 6)	For max. ADC input frequency = 1MHz		25		μs

Note 4: I_{OUT} mismatch (bit to bit) $\triangle I_{MAT}$ is calculated:

$$\Delta I_{MAT} = MAX\left(ABS\left(\frac{I_{OUTn}(n = 1\sim12)}{\frac{I_{OUT1} + I_{OUT2} + \cdots + I_{OUT12}}{12}} - 1 \right) \right) \times 100\%$$

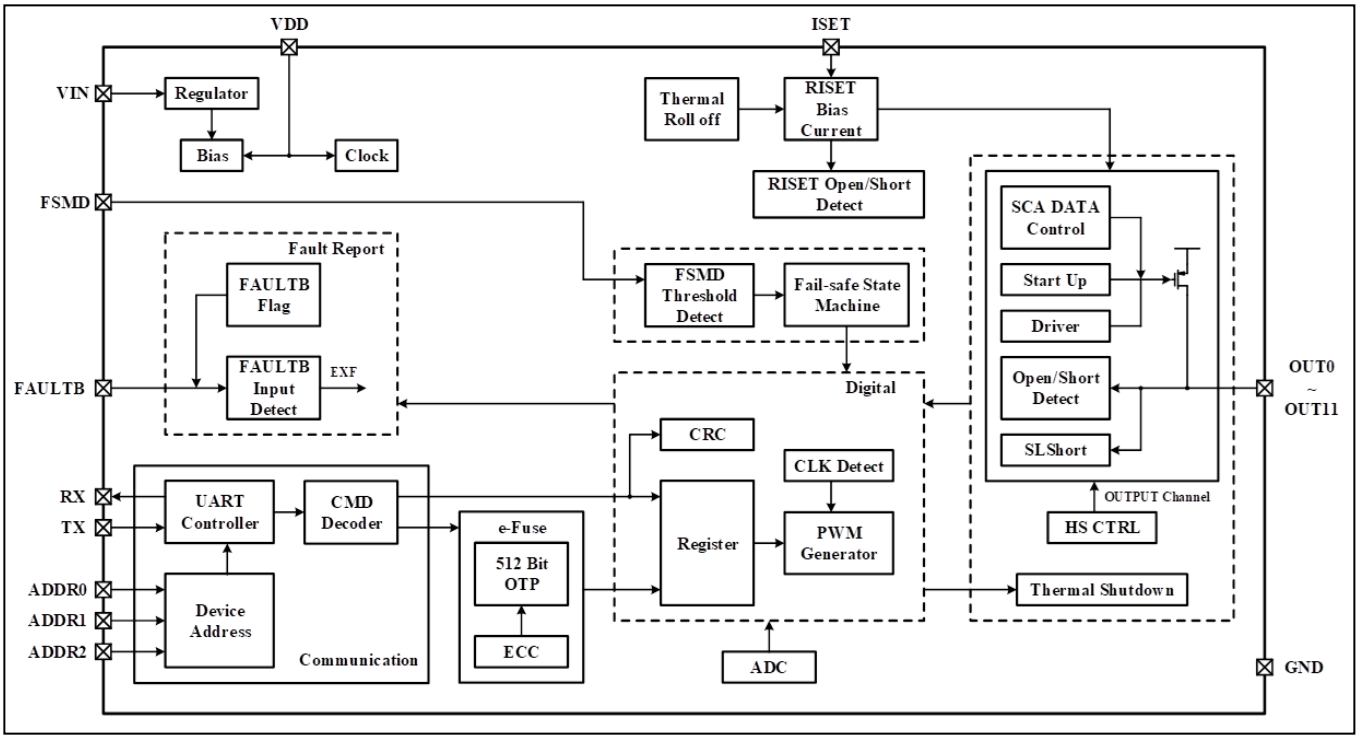
Note 5: I_{OUT} accuracy (device to device) $\triangle I_{OUT}$ is calculated:

$$\Delta I_{OUT} = ABS\left(\frac{\frac{I_{OUT1} + I_{OUT2} + \cdots + I_{OUT12}}{12} - I_{OUT(TYP)}}{I_{OUT(TYP)}} \right) \times 100\%$$

When R_{ISET}=10kΩ, $I_{OUT(TYP)}$ = 100mA; and when R_{ISET}=33kΩ, $I_{OUT(TYP)}$ = 30mA.

Note 6: Guaranteed by design.

8 FUNCTIONAL BLOCK DIAGRAM



9 APPLICATION INFORMATION

9.1 OVERVIEW

The IS32LT3132 is an automotive 12-channel LED driver with a UART interface for individual control of each LED string. Each channel is a high-side output channels, capable of up to 100mA and supports both DC adjustment and PWM dimming. The output current and PWM duty cycle of each channel can be individually configured through the UART interface. For high current LED applications, multiple output channels can be combined in parallel.

For added system reliability, the IS32LT3132 features various fault protections, including LED string open, LED string shorted, single LED shorted, overcurrent (ISET pin shorted), over temperature, CRC error and watchdog timeout (fail-safe modes) conditions for robust operation. Detection of these failures is reported by a dedicated reporting pin, FAULTB. There are also dedicated flag bits in registers for each failure which can be read back by the external host MCU through the interfaces. To optimize EMI performance, the IS32LT3132 features spread spectrum on the internal PWM base clock to spread the total electromagnetic emitting energy into a wider range that significantly degrades the peak energy of EMI. In addition, the output current source ON/OFF transitions during PWM dimming have a slew rate control and programmable phase delay to mitigate EMI and power supply inrush current.

The IS32LT3132 interface is UART, and it supports up to 64 slave IS32LT3132 devices. The device address can be configured by the three address pins. The UART receives data to control all output channels and sends back fault information to the host MCU. The UART interface in conjunction with an external standard CAN transceiver enables long distance communication with a host MCU placed outside of the lamp module (as shown in Figure 1). Based on the CAN physical layer, it achieves excellent EMC and EMI performance. The embedded CRC correction of the UART data stream can ensure robust communication in automotive environments. The UART interface is easily supported by most MCUs in the market.

To further increase robustness, the fail-safe mode of the device allows automatic switching to fail-safe state in case of communication loss, for example, host MCU failure or communication cables broken. The device supports different fail-safe modes configured by the FSMD pin.

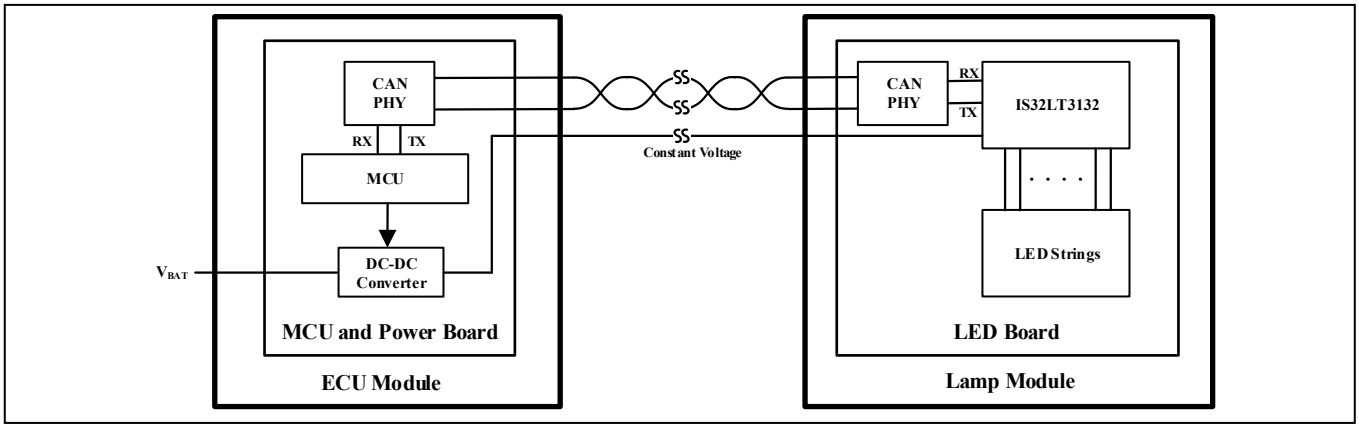


Figure 4 UART Interface with External CAN Transceiver for Outside Module Long Distance Communication

9.2 POWER SUPPLY

9.2.1 VIN UNDERVOLTAGE-LOCKOUT (UVLO)

The IS32LT3132 features an undervoltage-lockout (UVLO) function on the VIN pin to prevent unintended operation at too low supply voltages. UVLO threshold is an internally fixed value and cannot be adjusted. Entering UVLO will reset all registers to their default value. The device is disabled when the VIN voltage drops below V_{VIN_UV} and automatically resumes normal operation when the VIN voltage rises above (V_{VIN_UV}+ V_{VIN_UVHY}).

9.2.2 INTERNAL 5V LINEAR REGULATOR (VDD)

The IS32LT3132 device integrates an internal linear regulator (VDD) with 5V (Typ.) and I_{DD_MAX} current capability to provide power supply to the internal analog and digital circuits. During operation, the internal circuitry can be subject to transient currents from this linear regulator. Therefore, a 4.7μF low ESR, X7R type ceramic capacitor is necessary from VDD pin to GND, it must be placed as close to the VDD pin as possible. This linear regulator also has the UVLO feature. The device is disabled when the V_{DD} voltage drops below V_{DD_UV} and resumes normal operation when the VDD voltage rises above (V_{DD_UV}). Entering UVLO will reset all registers to their default value. An I_{DD_LIM} current limit on VDD pin protects the IS32LT3132 from VDD output overload or short-circuit conditions.

9.3 OUTPUT CURRENT SETTING

The full DC output current (I_{OUT_FU}) for each channel is set with resistor (R_{ISET}) connected from the ISET pin to GND. This current set resistor is computed using the following equation:

$$I_{OUT\_FU} = \frac{V_{ISET}}{R_{ISET}} \times 500 \qquad (1)$$

Where V_{ISET} is the voltage of ISET pin, is 2V (Typ.)

(10kΩ ≤ R_{ISET} ≤ 75kΩ)

It is recommended that R_{ISET} be a 1% accuracy resistor with good temperature characteristic to ensure stable output current. R_{ISET} must be placed as close to ISET pin as possible on PCB layout to avoid noise interference and ground bounce. The device is protected from an output overcurrent condition caused by R_{ISET} resistor. The output current is reduced to 17mA (Typ.) if the ISET pin is shorted to ground or R_{ISET} resistor value is too low.

When R_{ISET} is fixed, the DC output current for each channel can be further adjusted in 64-steps by the GCC[5:0] bits in the GC_CTRL register (01h). Furthermore, based on the GCC[5:0] setting, each channel also supports individual 256-step programmable DC output current adjustment. This feature can be used to set binning values for output LEDs or to calibrate the LEDs to achieve high brightness homogeneity based on an external visual calibration system to further save binning cost. The 8-bit Scaling Registers SCAx (04h~0Fh) individually set the DC output current of each channel.

GCC[5:0] and SCAx control the OUTx current (I_{OUTx}) as shown in following equation:

$$I_{OUTx} = I_{OUT\_FU} \times \frac{GCC}{63} \times \frac{SCAx}{255} \qquad (2)$$

Where, x is from 1 to 12 for different output channel.

$$GCC = \sum_{n=0}^{5} D[n] \cdot 2^n \qquad (3)$$

$$SCAx = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (4)$$

For example: assume GCC[5:0] = 0x05 and SCA1 = 0x40. GCC = 5. Then the DC output current of OUT1 is:

$$I_{OUT1} = I_{OUT\_FU} \times \frac{5}{63} \times \frac{64}{255}$$

9.4 PWM DIMMING

The IS32LT3132 integrates independent 12-bit PWM generators for each output channel. The output current for each channel is turned on and off as controlled by the PWM generator. The average current of each output channel can be adjusted by its PWM duty cycle to control the LED channel brightness. The PWM Registers (10h~27h) individually set the PWM duty cycle for each channel.

The PWM dimming frequency is programmable by the PWM Configuration register (02h). The maximum PWM frequency can be up to 64kHz (Typ.). Due to the output current slew rate control, a high frequency PWM signal has a shorter period time that will degrade the PWM dimming linearity. Therefore, a low frequency PWM signal is good for achieving better dimming contrast ratio. Select the PWM dimming frequency based on the minimum brightness requirement for the application.

The PWM generators dim the LEDs by its duty cycle:

$$I_{OUTx\_PWM} = I_{OUTx} \times D_{PWMx} \qquad (5)$$

Where, D_{PWMx} is duty cycle of each channel independently programmed by PWM Registers (10h~27h), in 12bit or 7+5-bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=0}^{11} D[n] \cdot 2^n}{4096} \qquad (6)$$

In 8bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=4}^{11} D[n] \cdot 2^n}{256} \qquad (7)$$

9.4.1 PWM SPREAD SPECTRUM

The IS32LT3132 includes a spread spectrum feature on PWM base clock to optimize EMI performance. The spread spectrum function helps spread the total electromagnetic emitting energy into a wider range that significantly degrades the peak energy of EMI. With spread spectrum, the EMI test can be passed with smaller size and lower

cost filter circuit. Spread spectrum is enabled/disabled by the SYSCFG register (03h).

9.4.2 PWM PHASE DELAY

To mitigate transient current generation and power supply ripple, the IS32LT3132 features PWM phase delay. When PWM phase delay is disabled (PDE (00h) is set to “0”, default value is “1” phase delay enable), all channels are simultaneously turned on at the beginning of each PWM cycle. This will result in large current draw from the power supply leading to high voltage ripple on the power supply rail. As shown in figure 3.

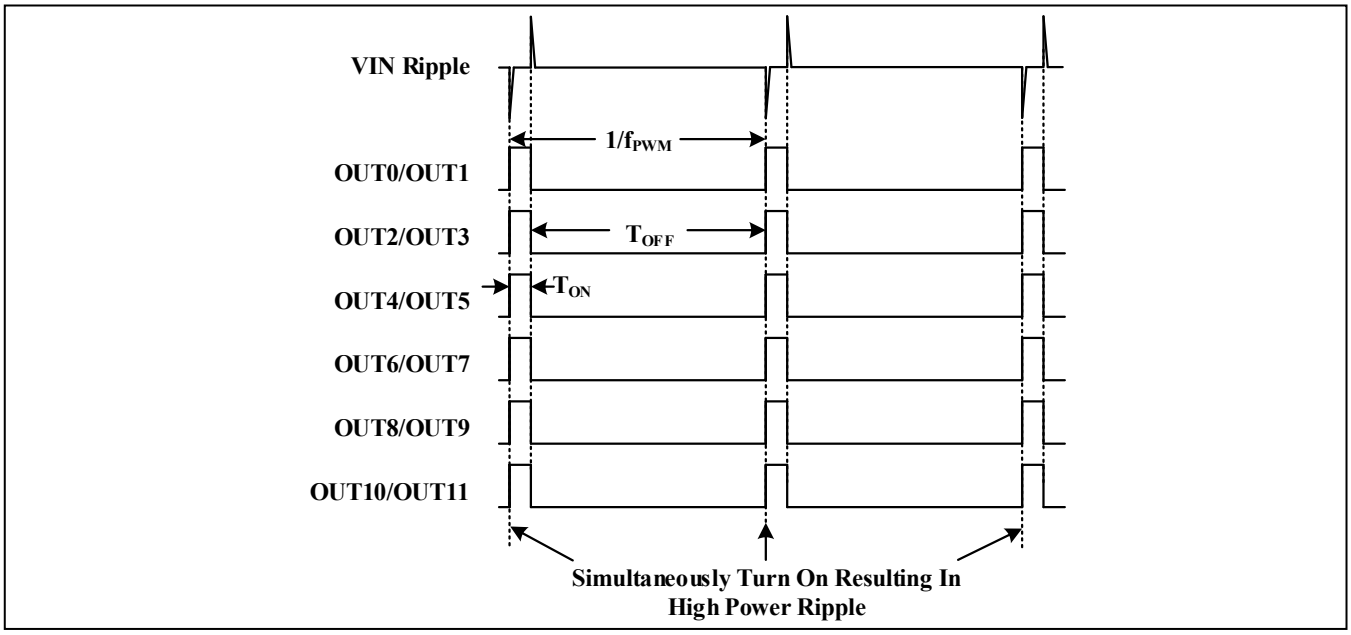


Figure 5 PWM Phase Delay Disabled

The IS32LT3132 divides 12 output channels into 6 groups to perform PWM phase delay, OUT0&OUT1 are group 1, OUT2&OUT3 are group 2, …OUT10&OUT11 are group 6. When the PDE bit in the CONFIG register (00h) is set to "1", the phase delay is enabled, starting each group in turn from each PWM cycle. The t_{DELAY_1} is interval delay time between group n & group n+1, and t_{DELAY_1} is 1/6 PWM cycle ($1/f_{PWM}$). This minimizes the voltage ripple on the VIN power supply rail. As shown in figure 4.

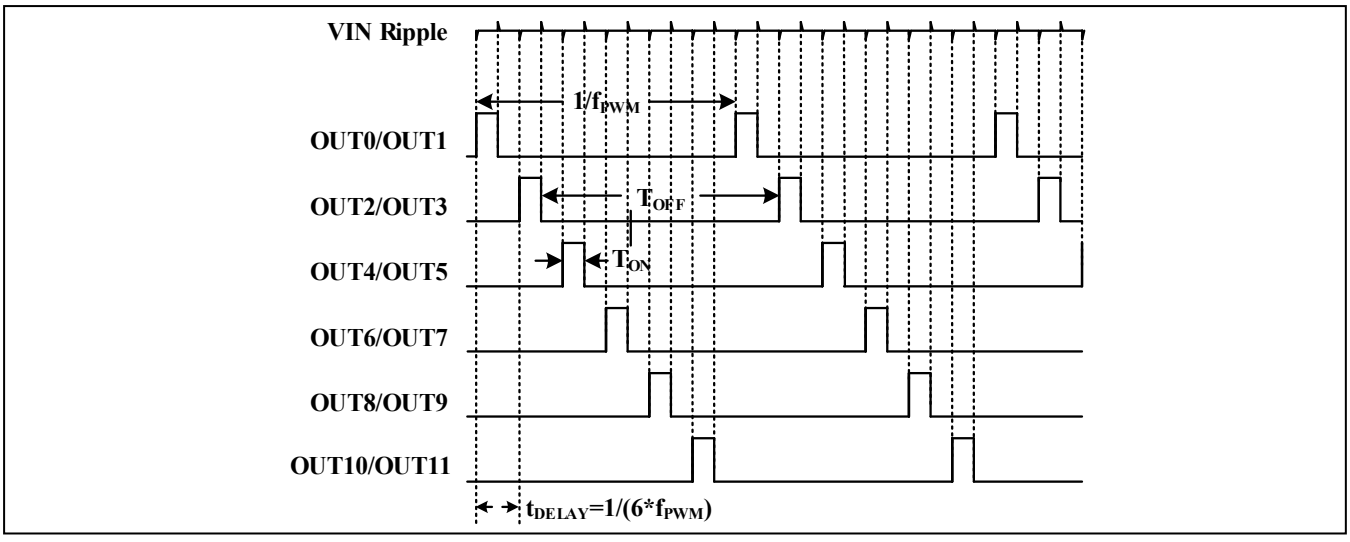


Figure 6 PWM Phase Delay Enabled

9.5 FAULT PROTECTION

9.5.1 FAULT REPORTING

For added system reliability, the IS32LT3132 integrates various fault detections for LED string open/short, single LED short, overcurrent (ISET shorted), over temperature, CRC error and watchdog timeout (fail-safe modes) conditions. The open drain pin FAULTB can be used for fault condition reporting. If any fault occurs, the

corresponding bit in FAULT_TYPE_1/2 register(38h/39h) will be set to “1” and the FAULTB pin will go low after a delay time (programmed by FT[3:0] bits in FLT_CONFIG register(30h)) to report fault condition. When it’s monitored by a host MCU, a pull-up resistor R_{FPU} (10kΩ recommended) from the FAULTB pin to the supply of the host MCU is required.

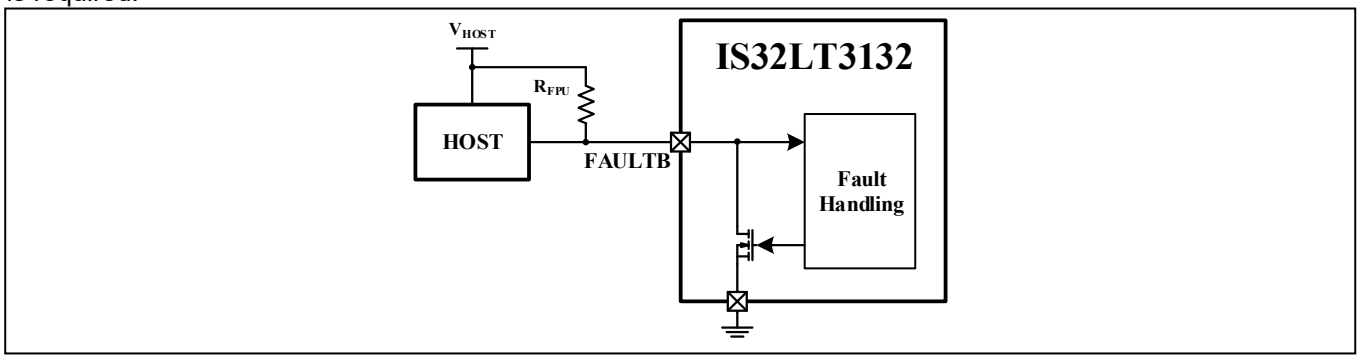


Figure 7 Host Monitors the Fault Reporting

9.5.2 LED STRING OPEN PROTECTION

The LED string open detection is enabled by setting the ODE and ODF bits in FLT_DET_EN register (2Fh) to “1”. If any LED string is opened, the corresponding OUTx pin voltage will be pulled up close to VIN. When the voltage(VIN-VOUTx) falls below the LED string open detection voltage, VOC_FL and persists for longer than a deglitch time (typical 10μs), the LED string open protection will be triggered. The corresponding fault flag bits in OPEN_FLT register (33h & 34h) and the OPENF bit in FAULT_TYPE_2 register (39h) will be set to “1”. The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register(30h)) to report the fault condition. The faulty channel will reserve a 4mA retry current for recovery detection.

No matter in which fault protection mode, the device will recover to normal operation and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) expires once the open condition is removed, i.e. VIN-VOUTx rising above the LED string open detection voltage, VOC_RS. The corresponding fault flag bit in OPEN_FLT register will reset to “0”. However, the OPENF bit in FAULT_TYPE_2 register (39h) is latched, which means that it cannot automatically reset to “0” after open condition being removed but must be cleared by the host MCU writing it back to “0”.

When PWM dimming is implemented, the LED string open detection is only enabled during the PWM ON phase. If the PWM on-time is less than the deglitch time (typical 10μs), the device does not report any LED string open fault.

9.5.3 LED STRING SHORT PROTECTION

The LED string short detection is enabled by setting the SDE and SDF bits in FLT_DET_EN register (2Fh) to “1”. If any LED string is short, the corresponding OUTx pin will be pulled down close to GND. When dropout voltage from the OUTx pin, VOUTx, falls below the LED string short detection voltage, VSC_FL, and persists for longer than a deglitch time (typical 10μs), the LED string short protection will be triggered. The corresponding fault flag bits in SHORT_FLT register (31h & 32h) and the SHORTF bit in FAULT_TYPE_2 register (39h) will be set to “1”. The FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The faulty channel will reserve a 4mA retry current for recovery detection.

No matter in which fault protection mode, the device recovers to normal operation and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the short condition is removed, V_{OUTx} rising above the LED string short detection voltage, V_{SC_RS}. The corresponding fault flag bit in SHORT_FLT register will reset to “0”. However, the SHORTF bit in FAULT_TYPE_2 register (39h) is latched, which means that it cannot automatically reset to “0” after short condition being removed but must be cleared by the host MCU writing it back to “0”.

When PWM dimming is implemented, the LED string short detection is only enabled during PWM ON phase. If the PWM on-time is less than the deglitch time (typical 10μs), the device does not report any LED string short fault.

When the device is operated in DC mode, the PWM function is disabled. It is recommended to not enable both LED string short and single LED short, because the IS32LT3132 may incorrectly report an LED string short as a single LED short. Individually enable either LED string short or single LED short detection. If a single LED short is reported, double check for LED string short or single LED short in software.

9.5.4 SINGLE LED SHORT PROTECTION

The single LED short detection is enabled by setting the SLSDE and SLSDF bits in FLT_DET_EN register (2Fh) to “1”. Then the single LED short detection is active after VIN voltage rising above the fault undervoltage-lockout voltage threshold FLT_UV. That helps to prevent false fault detection due to the insufficient power supply voltage, such as power up transience. The single LED short detect threshold VSLSTH of each channel is individually programmed by the corresponding LEDx_SLS[3:0] bits in LEDx_SLSTH registers (28h~2Dh). If single LED of any string is shorted, the corresponding OUTx pin voltage will fall. When the OUTx pin voltage, VOUTx, fall below single LED short detect threshold, VSLSTH, and persists for longer than a deglitch time (typical 10μs), the single LED short protection will be triggered.

The device recovers to normal operation and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the single LED short condition is removed, VOUTx rising above the LED string short detection voltage, VSLSTH. The corresponding fault flag bit in SLS_FLT register will reset to “0”. However, the SLSHORTF bit in FAULT_TYPE_2 register (39h) is latched, which means that it cannot automatically reset to “0” after single LED short condition being removed but must be cleared by the host MCU writing it back to “0”.

When PWM dimming is implemented, the single LED string short detection is only enabled during PWM ON phase. If the PWM on-time is less than the deglitch time (typical 10μs), the device does not report any single LED short fault.

9.5.5 OVERCURRENT (ISET PIN SHORT TO GND)

The device is protected from an output overcurrent condition caused by the R_{ISET} resistor. All output current is limited to 170mA (Typ.) in case of the ISET pin shorted to ground or too low value R_{ISET} resistor is connected to ISET pin. If the condition persists for longer than a deglitch time (typical 1μs), the ISET pin short protection will be triggered. All output current will be reduced to 17mA (Typ.). If the RSET_SHE bit in FAULT_EN register (37h) is set to 1,the RSET_SH bit in FAULT_TYPE_1 register (38h) will be set to “1” and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

Once the resistance from the ISET pin to GND resumes to a normal range, all channels will recover to normal operation and the FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register). However, the RSET_SH bit in FAULT_TYP_1 register (38h) is latched, which means that it cannot automatically reset to “0” after ISET short condition being removed but must be cleared by the host MCU writing it back to “0”.

9.5.6 ISET PIN OPEN

In case of the ISET pin open or too High value RISET resistor is connected to ISET pin. If the condition persists for longer than a deglitch time (typical 1μs), the ISET pin open protection will be triggered. If the RSET_OPE bit in FAULT_EN register (37h) is set to 1, the RSET_OP bit in FAULT_TYPE_1 register (38h) will be set to "1" and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition.

Once the resistance from the ISET pin to GND resumes to a normal range, all channels will recover to normal operation and the FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register). However, the RSET_OP bit in FAULT_TYPE_1 register (38h) is latched, which means that it cannot automatically reset to “0” after ISET open condition being removed but must be cleared by the host MCU writing it back to “0”.

9.5.7 EXTERNAL FAULT

External fault is to achieve the One Fail All Fail function, multiple IS32LT3132 applications by connecting the FAULTB pins of each IS32LT3132 in parallel, And set the OFA[1:0] bit of CONFIG register (00h) to One Fail All Fail, When FAULTB pins are pulled down externally persists for longer than a deglitch time, the EXF bit in FAULT_TYPE_2 register (39h) will be set to "1".

FAULT_TYPE_2 register (39h) is latched, which means that it cannot automatically reset to “0” after External fault condition being removed but must be cleared by the host MCU writing it back to “0”.

9.5.8 THERMAL SHUTDOWN

If the junction temperature exceeds T_{SD} (Typ. 168˚C), all output channels will go to the OFF state and the TSD bit in FAULT_TYPE_1 register (38h) will be set to “1”. If the TSDE bit in FAULT_EN register (37h) to “1”, the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. At this point, the device presumably begins to cool off. Any attempt to toggle the channels back to the source

condition before the device has cooled to below (T_{SD}-T_{SD_HYS}) (Typ. 155˚C) will be blocked and the device will not be allowed to restart. The FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the device cools down. However, the TSD bit in FAULT_TYPE_1 register (38h) is latched, which means that it cannot automatically reset to “0” but must be cleared by the host MCU writing it back to “0”.

9.5.9 THERMAL ROLL-OFF PROTECTION

The device integrates the thermal shutdown protection to prevent the device from overheating. In addition, to prevent the LEDs from flickering due to rapid thermal changes, the device also includes a programmable thermal roll-off feature to reduce power dissipation at high junction temperature.

The output current will be equal to the set value I_{OUTx} if the junction temperature of the device remains below thermal roll-off temperature threshold 140˚C. If the junction temperature exceeds the temperature threshold, the output current of all channels will begin to linearly reduce following the junction temperature ramping up until thermal shutdown. The TF bit in FAULT_TYPE_1 register (38h) will be set to “1”. If the TFE bit in FAULT_EN register (37h) to “1”, the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) to report the fault condition. The percentage of the output current before thermal shutdown is programmable by the TROF[2:0] bits in the CONFIG register (00h).

The output current will linearly resume to the set value I_{OUTx} and the FAULTB pin will recover to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register) once the junction temperature cools down below the thermal roll-off temperature threshold 140˚C. However, the TF bit in FAULT_TYPE_1 register (38h) is latched, which means that it cannot automatically reset to “0” but must be cleared by the host MCU writing it back to “0”.

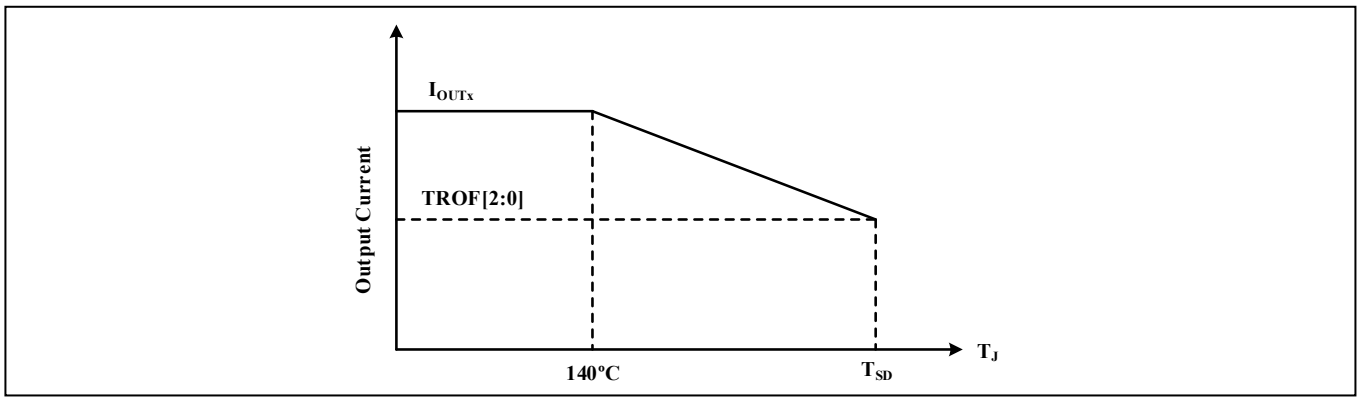


Figure 8 Thermal Roll-off Protection

By mounting the IS32LT3132 device on the same thermal substrate as the LEDs, use of this feature can also limit the dissipation of the LEDs.

9.5.10 Fault Action Table

Fault Action Table (Both Normal State And Fail-Safe State):

Fault Type	Detection	Conditions	Actions	Fault Flags	FAULTB Pin	Recovery
Supply UVLO	$V_{IN}<V_{VIN\_UV}$ or $V_{DD}<V_{DD\_UV}$	-	Turn off all channels and reset all registers to default value	-	No action	$V_{IN}>(V_{VIN\_UV}+V_{VIN\_UVHY})$ or $V_{DD}>(V_{DD\_UV}+V_{DD\_UVHY})$
LED string open	$V_{IN}>V_{FLT\_UV}$ and $(V_{IN} - V_{OUTx})<V_{OC\_FL}$	PWM pulse width greater than 10μs (Typ.) and ODE = 1	Faulty channel outputs 4mA and other channels on (ODF = 1)	OPEN_FLT and OPENF bit	Pull low (ODF = 1)	$(V_{IN} - V_{OUTx})>V_{OC\_RS}$ Write OPENF bit to “0”
LED string short	$V_{OUTX} <V_{SC\_FL}$ (SHORT_FLT≠000)	PWM pulse width greater than 10μs (Typ.) and SDE = 1	Faulty channel outputs 4mA and other channels on (SDF = 1)	SHORT_FLT and SHORTF bit	Pull low (SDF = 1)	$V_{OUTx}>V_{SC\_FL}$ (SHORT_FLT=000) Write SHORTF bit to “0”
Single LED short	$V_{IN}>V_{FLT\_UV}$ and $V_{OUTx}<V_{SLSTH}$	PWM pulse width greater than 10μs (Typ.) and SLSDE = 1	Faulty channel outputs 4mA and other channels on (SLSDF = 1)	SLST_FLT and SLSHORTF bit	Pull low (SLSDF = 1)	$V_{OUTx}>V_{SLSTH}$ Write SLSHORTF bit to “0”
ISET pin short (Overcurrent)	I_{OUTx} limited to 110mA (Typ.)	Longer than 1μs (Typ.) deglitch time and RSET_OPE = 1	All channels reduced to 17mA (Typ.)	RSET_SH bit	Pull low	ISET pin to GND resistance resumes to normal range, Write RSET_SH bit to “0”
ISET pin open	ISET pin open	Longer than 1μs (Typ.) deglitch time and RSET_SHE = 1	-	RSET_OP bit	Pull low	ISET pin to GND resistance resumes to normal range, Write RSET_SH bit to “0”
External fault	FAULTB pins are pulled down	OFA [1:0] ≠ 11	All channels off	EXF bit	Pull low	FAULTB pins are pull up Write EXF bit to “0”
PWM duty verification	Any output occurs PWM duty verification failure	-	-	LPBF bit	Pull low (DUTYF_EN = 1)	Disabled loop back, Write DUTYF_EN bit to “0”
Thermal shutdown	$T_J>T_{SD}$	-	All channels off	TSD bit	Pull low (TSDE = 1)	$T_J<(T_{SD}-T_{SD\_HYS})$ Write TSD bit to “0”
Thermal roll-off	$T_J>120^{\circ}C$	TROF[2:0] ≠ 00	All channels linearly reduce output current	TF bit	Pull low (TFE = 1)	$T_J<120^{\circ}C$ Write TF bit to “0”
CRC error	Calculated CRC does not match CRC data	-	Increments CRC Error Count register	CRCF bit	Pull low	Write CRCF bit to “0”
Communication loss	Watchdog 1 times out	R_{FSMD}=30kΩ, 51kΩ or 75kΩ and no error-free communication	Enter fail-safe modes	CMWF1 bit	Pull low	Write CMWF1 bit to “0” or Exit fail-safe modes
Communication loss	Watchdog 2 times out	R_{FSMD}=30kΩ, 51kΩ or 75kΩ and no error-free communication	Enter fail-safe modes	CMWF2 bit	Pull low	Write CMWF2 bit to “0” Feed the dog within the set WDT2 time range or Exit fail-safe modes
OTP data verification	OTP data ECC error	ECC2F_EN = 1	-	ECC_ST	Pull low	-

Note 7: OPENF, SHORTF, SLSHORTF, ISETSF, TSD, TF, RSET_SH, RSET_OP,EXF, CMWF1, CMWF2 and CRCF bits are latched. Even though the fault conditions are removed, they cannot automatically reset to “0” but must be cleared by the host MCU writing it back to “0”.

9.6 UART INTERFACES

The host MCU can communicate with the IS32LT3132 device using a Universal Asynchronous Receiver and Transmitter (UART). The UART communication process uses a command and response protocol (LumiBus protocol) mastered by the host MCU to write and read the registers to and from each IS32LT3132 device. The IS32LT3132 UART interface utilizes half-duplex communications (transmit and receive cannot overlap). A tri-state buffer in the IS32LT3132 drives the TX out pin, so it is recommended to place an external pull-up resistor on the RX input return line of the host MCU. An external pull-up on the MCU TX output will allow multiple IS32LT3132 devices to share a common pair of TX and RX signals by connecting all IS32LT3132 TX lines together and all IS32LT3132 RX lines

together. The baud rate can support 100kbps~1Mbps.

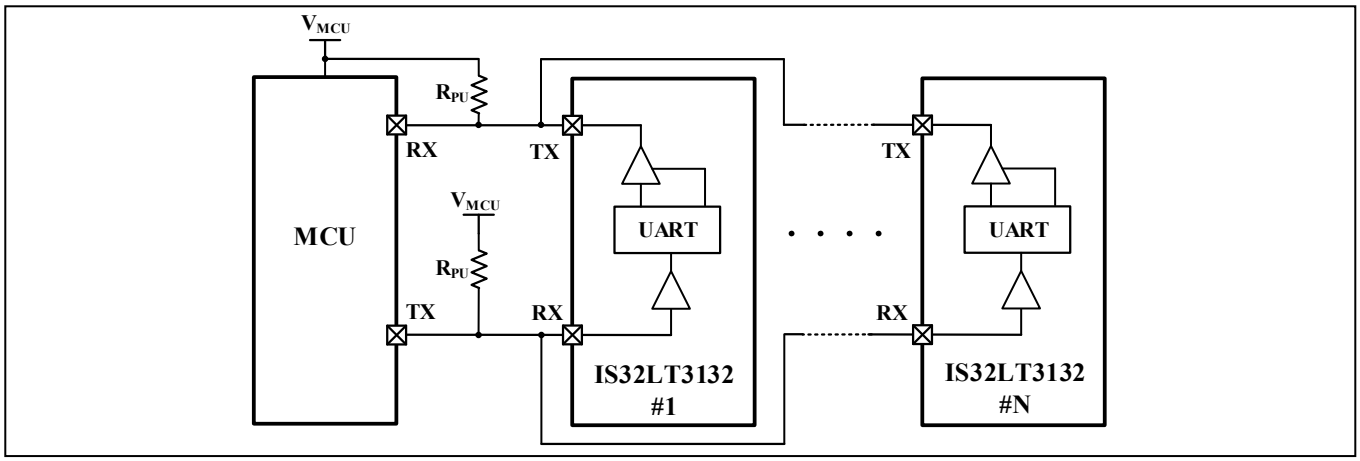


Figure 9 UART Interface Connection

Additionally, the physical TX and RX connections of IS32LT3132 can be joined together through a standard CAN transceiver (CAN PHY), as shown in Figure 13. This has the added advantage of protection from shorts to battery and/or shorts to ground on the cables and/or harnesses between the host MCU board and the IS32LT3132 board. The CAN physical layer has excellent EMI and EMS performance with long distance off-board connection.

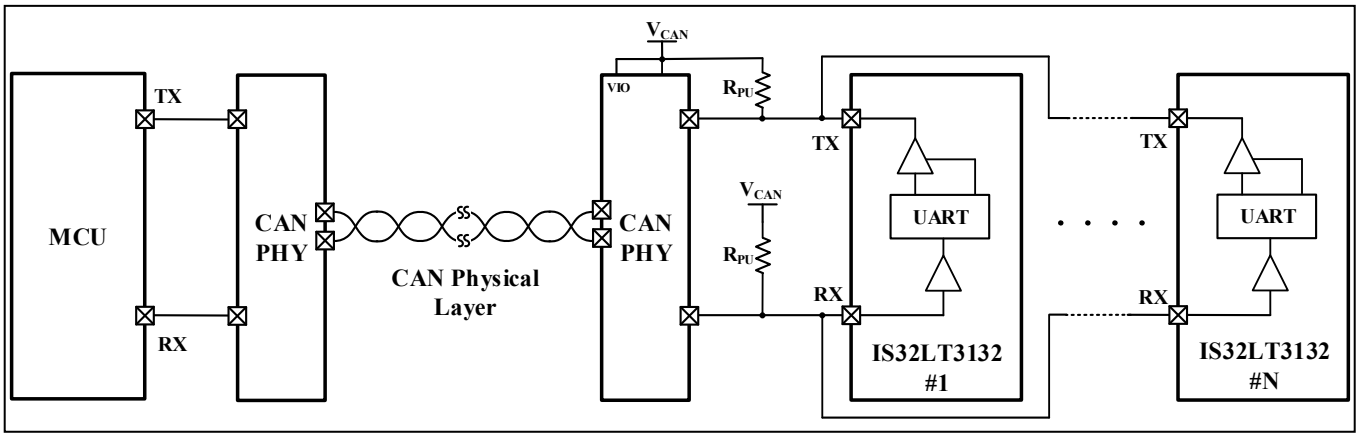


Figure 10 UART Interface with Standard CAN Transceiver Connection

9.6.1 UART DATA FORMAT

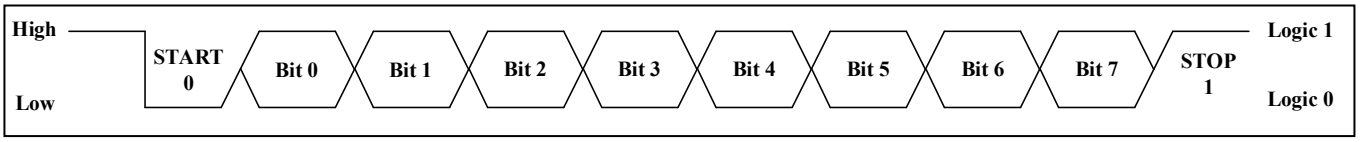


Figure 11 UART Data Byte Format

The UART operates with one start bit, eight data bits (LSbit first) and one stop bit. Above figure shows the waveform for an individual byte transfer on the UART. A logic “1” state occurs when the device drives the line to high voltage. A logic “0” state occurs when the device drives the line to ground. Below figure shows actual data bytes with UART data format.

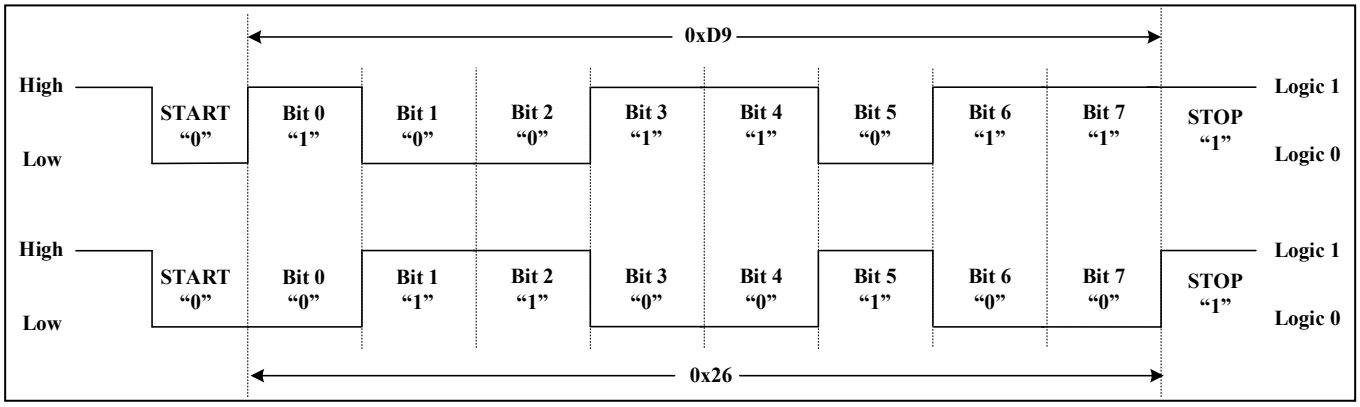


Figure 12 UART Data Transaction Example

The baud rate of UART communication can be 100kbps to 1Mbps which is synchronized by the baud rate of the SYNC byte of the BUS Reset command. The UART uses 32x over-sampling on the incoming asynchronous RX signal. Between UART data bytes, at least one bit is required as STOP bit.

9.6.2 LUMIBUS PROTOCOL

The communication uses the LumiBus protocol which is a UART-based protocol supported by most MCUs. The communication process of all three interfaces uses a command and response protocol mastered by the host MCU to write and read the registers to and from each IS32LT3132 device. This means that the IS32LT3132 device never initiates traffic onto the network. The LumiBus protocol maps the registers into an address space on each device. The host MCU uses the LumiBus protocol to initiate a communication transaction by sending a command frame. This command frame addresses either one IS32LT3132 device directly or broadcasts to all IS32LT3132 devices on the network. This addressing may cause a response frame to be sent back from the slave IS32LT3132 device depending on the command type of the command frame. There are four types of commands:

1) BUS Reset Command: resets the UART
2) Write Command: writes data from host MCU to specific IS32LT3132 device(s)
3) Read Command: reads data from specific IS32LT3132 device to host MCU
4) Special Command: specifies IS32LT3132 device(s) to implement specific function.

There is no response frame given following a broadcast write command frame. Therefore, only two types of response frames exist that an IS32LT3132 device sends back to the host MCU: Write Acknowledge (if enabled) and Read Response.

9.6.3 COMMAND FRAME TYPES

9.6.3.1 BUS Reset Command Frame

The host MCU can reset the device UART and LumiBus protocol state machine at any time by sending BUS Reset command. The BUS Reset command consists of reset signal and SYNC byte (0x55). The reset signal includes at 150μs~10ms break low and at 2μs~100us logic high break delimiter. Upon receiving the bus reset signal, the LumiBus protocol state machine of all IS32LT3132 devices on the bus will be reset to a known-good state. The bus reset signal must be followed by a SYNC byte (0x55) send by desired baud rate (within 100kbps to 1Mbps) to synchronize the baud rate to all IS32LT3132 devices. The subsequent communication must use the identical baud rate. With this synchronization approach, the cost of an external crystal oscillator is saved. To avoid clock drift over time and ambient temperature, it's recommended to periodically send a BUS Reset Command to the IS32LT3132 devices.

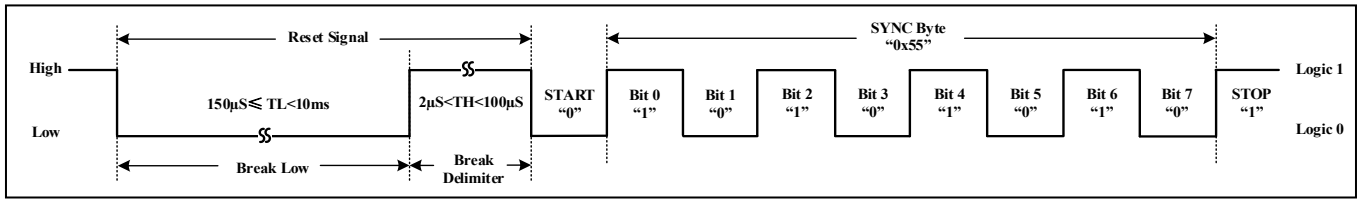


Figure 13 BUS Reset Command

Upon system power up, the host MCU must initialize the BUS by sending a BUS Reset Command before communication. This BUS reset operation can be optionally performed by the host MCU for several application

scenarios: (1) upon system power up, (2) communication watchdog times out, (3) communication fault is detected, illustrated as in the following diagram:

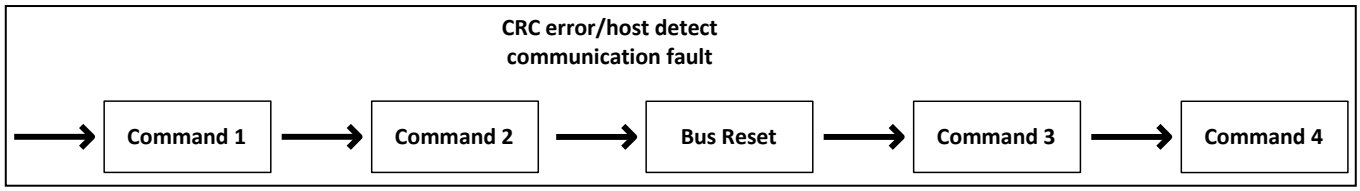


Figure 14 Communication Fault is Detected

Note that the BUS Reset command only resets the interface state machine (including stored communication baud rate). It does not reset the registers and does not halt normal LED PWM operation.

Note 8: If TX or RX anyone disconnect, there will cause CRC error, communication again need send Bus reset.

9.6.3.2 Write Command Frame

The Write Command Frame is comprised of the following sequence.

CMD Frame Header (One Byte)	Device ID (One Byte)	Start Register Address (One Byte)	Data 1 (One Byte)	…	Data N (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

9.6.3.3 Acknowledge Frame

If the ACKEN bit is set in the SYSCFG register, the addressed device transmits an acknowledge back to the host MCU upon a successful single device write. The Acknowledge Frame is comprised of a single byte (ACK=0x7F or 0x7E) as the following sequence.

ACK (0x7F or 0x7E)

9.6.3.4 Read Command Frame (transferred by the host MCU)

The Read Command Frame is comprised of the following sequence.

CMD Frame Header (One Byte)	Device ID (One Byte)	Start Register Address (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

A successfully-addressed IS32LT3132 device then transfers back the appropriate Read Response Frame.

The Read Response Frame is comprised of the following sequence.

RSP Frame Header (One Byte)	Device ID (One Byte)	Data 1 (One Byte)	…	Data N (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

9.6.3.5 Special Command Frame

The special command specifies the IS32LT3132 device to implement specific function which includes:

1) Update Command

   This special command is used for below scenarios:

   - Update the configuration of the PWM registers data and Scaling registers data into output stages at the next PWM boundary after this command is issued.
   - Update the configuration of the DC_PWM register and PDE(PHASE) register (00h).

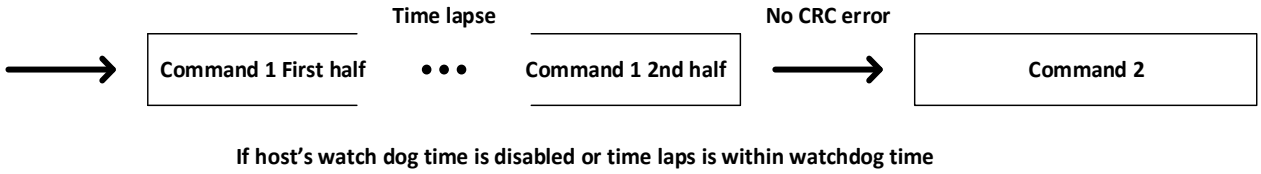
2) Registers Reset Command

   Resets all registers to default value, excluding the PWR bit in SYSCFG register (03h) and OTP registers (B0h~BCh)

The Special Command Frame is comprised of the following sequence:

CMD Frame Header (One Byte)	Device ID (One Byte)	CRC_L (One Byte)	CRC_H (One Byte)

One complete command frame can be received successfully even if the bytes in the frame are not sent continuously. CRC error could be determined by reading back the written data byte.



9.6.4 TRANSACTION FRAME DESCRIPTION

Command frames include the following byte types:

1) Frame Header Byte
2) Device ID Byte
3) Start Register Address Byte
4) N Data Byte(s) (N = 1~16, 32)
5) CRC Bytes (CRC_L and CRC_H)
6) Acknowledge Byte (ACK)

9.6.4.1 Frame Header Byte

The Frame Header Byte identifies the transaction as either a write/read command frame or a response frame. In addition, the Frame Header Byte indicates how many data bytes are being written/read or responded. The number of data bytes to be written/read or responded can be 1~16 or 32.

Frame Header Type	D7	D6	D5	D4:D0
CMD Frame Header	FRM_TYPE	W/R	BCON	CMD
RSP Frame Header	FRM_TYPE	RSVD	RSVD	RSP

The fields shown in the Frame Header Byte above are described in the table below.

	Value (BIN)	Description
FRM_TYPE (Bit 7)	0	Response frame sent back from the IS32LT3132 device to host MCU
	1	Command frame sent from host MCU to the IS32LT3132 device
W/R (Bit 6)	0	Write command frame
	1	Read command frame
BCON (Bit 5)	0	Single device write or read.
	1	Broadcast write. The Device ID Byte must be 0xBF to broadcast to all IS32LT3132 devices. Broadcast only accepts write command
CMD (Bit 4:0)	**Specify transmit data length for write/read command frame:**	
	00000 ~ 01111	1 byte ~ 16 bytes of data length
	10000	32 bytes of data length
	For special commands (W/R bit must be set to "0"):	
	11000	Update Command. Valid for both single device and broadcast write
	11110	Registers Reset Command. Valid for both single device and broadcast write
RSP (Bit 4:0)	**Specify transmit data length for response frame:**	
	00000 ~ 01111	1 byte ~ 16 bytes of data length
	10000	32 bytes of data length

9.6.4.2 Device ID Byte

	D7	D6	D5:D0
Device ID	p[1]	p[0]	DEV_ID [5:0]

There are six DEV_ID bits and two parity bits. The parity bits for the Device ID byte are calculated with the equations below:

p[1] = ~(dev_id[1] ^ dev_id[3] ^ dev_id[4] ^ dev_id[5])

p[0] = dev_id[0] ^ dev_id[1] ^ dev_id[2] ^ dev_id[4]

The device ID of each IS32LT3132 device is determined by the resistors connected from three address pins of ADDR0, ADDR1 and ADDR2 to GND. As following mapping for the Device ID byte. For a broadcast command of UART interface, the DEV_ID[5:0] must be 0b 111111, otherwise the broadcast command will be invalid.

AD2	R_{AD1}	R_{AD0}	D7	D6	D5	D4	D3	D2	D1	D0	DEVICE ID (HEX)
(kΩ, Note 9)											
10k	10k	10k	1	0	0	0	0	0	0	0	80
10k	10k	30k	0	1	0	1	0	0	0	0	50
10k	10k	51k	0	0	1	0	0	0	0	0	20
10k	10k	75k	1	1	1	1	0	0	0	0	F0
10k	30k	10k	1	1	0	0	0	1	0	0	C4
10k	30k	30k	0	0	0	1	0	1	0	0	14
10k	30k	51k	0	1	1	0	0	1	0	0	64
10k	30k	75k	1	0	1	1	0	1	0	0	B4
10k	51k	10k	0	0	0	0	1	0	0	0	08
10k	51k	30k	1	1	0	1	1	0	0	0	D8
10k	51k	51k	1	0	1	0	1	0	0	0	A8
10k	51k	75k	0	1	1	1	1	0	0	0	78
10k	75k	10k	0	1	0	0	1	1	0	0	4C
10k	75k	30k	1	0	0	1	1	1	0	0	9C
10k	75k	51k	1	1	1	0	1	1	0	0	EC
10k	75k	75k	0	0	1	1	1	1	0	0	3C
30k	10k	10k	1	1	0	0	0	0	0	1	C1
30k	10k	30k	0	0	0	1	0	0	0	1	11
30k	10k	51k	0	1	1	0	0	0	0	1	61
30k	10k	75k	1	0	1	1	0	0	0	1	B1
30k	30k	10k	1	0	0	0	0	1	0	1	85
30k	30k	30k	0	1	0	1	0	1	0	1	55
30k	30k	51k	0	0	1	0	0	1	0	1	25
30k	30k	75k	1	1	1	1	0	1	0	1	F5
30k	51k	10k	0	1	0	0	1	0	0	1	49
30k	51k	30k	1	0	0	1	1	0	0	1	99
30k	51k	51k	1	1	1	0	1	0	0	1	E9
30k	51k	75k	0	0	1	1	1	0	0	1	39
30k	75k	10k	0	0	0	0	1	1	0	1	0D
30k	75k	30k	1	1	0	1	1	1	0	1	DD
30k	75k	51k	1	0	1	0	1	1	0	1	AD
30k	75k	75k	0	1	1	1	1	1	0	1	7D
51k	10k	10k	0	1	0	0	0	0	1	0	42

51k	10k	30k	1	0	0	1	0	0	1	0	92
51k	10k	51k	1	1	1	0	0	0	1	0	E2
51k	10k	75k	0	0	1	1	0	0	1	0	32
51k	30k	10k	0	0	0	0	0	1	1	0	06
51k	30k	30k	1	1	0	1	0	1	1	0	D6
51k	30k	51k	1	0	1	0	0	1	1	0	A6
51k	30k	75k	0	1	1	1	0	1	1	0	76
51k	51k	10k	1	1	0	0	1	0	1	0	CA
51k	51k	30k	0	0	0	1	1	0	1	0	1A
51k	51k	51k	0	1	1	0	1	0	1	0	6A
51k	51k	75k	1	0	1	1	1	0	1	0	BA
51k	75k	10k	1	0	0	0	1	1	1	0	8E
51k	75k	30k	0	1	0	1	1	1	1	0	5E
51k	75k	51k	0	0	1	0	1	1	1	0	2E
51k	75k	75k	1	1	1	1	1	1	1	0	FE
75k	10k	10k	0	0	0	0	0	0	1	1	03
75k	10k	30k	1	1	0	1	0	0	1	1	D3
75k	10k	51k	1	0	1	0	0	0	1	1	A3
75k	10k	75k	0	1	1	1	0	0	1	1	73
75k	30k	10k	0	1	0	0	0	1	1	1	47
75k	30k	30k	1	0	0	1	0	1	1	1	97
75k	30k	51k	1	1	1	0	0	1	1	1	E7
75k	30k	75k	0	0	1	1	0	1	1	1	37
75k	51k	10k	1	0	0	0	1	0	1	1	8B
75k	51k	30k	0	1	0	1	1	0	1	1	5B
75k	51k	51k	0	0	1	0	1	0	1	1	2B
75k	51k	75k	1	1	1	1	1	0	1	1	FB
75k	75k	10k	1	1	0	0	1	1	1	1	CF
75k	75k	30k	0	0	0	1	1	1	1	1	1F
75k	75k	51k	0	1	1	0	1	1	1	1	6F
75k	75k	75k	1	0	1	1	1	1	1	1	BF
-	-	-	1	0	1	1	1	1	1	1	BF (Note 7) (for broadcast command only)

Note 9: The tolerance range of resistance accuracy could be ±1% for 10k, 30k, 51k and 75k.
Note 10: The Device ID Byte must be 0xBF to broadcast to all IS32LT3132 devices. Broadcast only accepts write command.

9.6.4.3 Start Register Address Byte

The LumiBus protocol allows up to 32 successive register locations from the addressed register to be written or read by a single command frame. The Start Register Address Byte is single byte which specifies the first register being written or read. The Start Register Address byte is present in only Write and Read Command transactions, not in Read Response and Special command transactions.

9.6.4.4 2N Data Byte (s)

The Frame Header Byte specifies the number of data bytes to be included in the frame.

9.6.4.5 CRC Bytes (CRC_L and CRC_H)

The host MCU sends command to IS32LT3132 using CRC-16-IBM standard for CRC checksum calculation, which will cover the whole frame bytes, e.g., Frame Header Byte, Device ID Byte, Start Register Address Byte, N Data Bytes. Lower byte first followed by higher byte. The CRC Bytes allow detection of errors within the transaction frame. The device increments the CRC Error Count Register CERRCNT (3Ah) each time a CRC error occurs on an incoming command frame and the CRCF bit in FAULT_TYPE_1 register (38h) will be set to “1” and the FAULTB

pin will go low to report fault condition after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register(30h)).The CRCF bit in FAULT_TYPE_1 register (38h) is latched, which means that it cannot automatically reset to “0” when no CRC error occurs but must be cleared by the host MCU writing it back to “0”. Once the CRCF bit is cleared, the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register(30h)).
The CRC bytes are also calculated by the addressed device during its Read Response. The CRC bytes are then appended to the end of the read data, lower byte first followed by higher byte. This allows the host MCU to check the read data coming from the IS32LT3132 device for any transmission errors. The following is a reference CRC checksum C code for a transmission to the IS32LT3132 devices.

```
Uint16 crc_16_ibm (Uint8 *buf, Uint8 len)
{
        Uint16 crc = 0;
        Uint16 I;
        while (len--)
        {
                crc ^= *buf++;
                for (I = 0; I < 8; I++){
                crc = (crc >> 1) ^ ((crc & 1) ? 0xa001 : 0);
                }
        }
        return crc;
}
```

Upon reading data from the IS32LT3132 device, the host MCU should calculate and compare the CRC to determine whether valid data was received. When IS32LT3132 sends back CRC bytes to the host MCU, the calculated CRC bytes must be bit-reversed before comparison to the received CRC bytes. The following is a reference code to perform received CRC bit reversal.

```
Uint8 reverse_byte(Uint8 byte)
{
        // First, swap the nibbles
        byte = (((byte & 0xF0) >> 4)| | ((byte & 0x0F) << 4));
        // Then, swap bit pairs
        byte = (((byte & 0xCC) >> 2) | ((byte & 0x33) << 2));
        // Finally, swap adjacent bits
        byte = (((byte & 0xAA) >> 1) | ((byte & 0x55) << 1));
        // We should now be reversed (bit 0 <--> bit 7, bit 1 <--> bit 6, etc.)
        return byte;
}
```

The following is a reference code for checking the read data against received CRC bytes.

```
bool is_crc_valid(Uint8 *rx_buf, Uint8 crc_start)
{
        Uint16 crc_calc; // Calculated CRC
        Uint8 crc_msb, crc_lsb; // Individual bytes of calculated CRC
        // Calculate the CRC based on bytes received
        crc_calc = crc_16_ibm(rx_buf, crc_start);
        crc_lsb = (crc_calc & 0x00FF);
        crc_msb = ((crc_calc >> 8) & 0x00FF);
        // Perform the bit reversal within each byte
        crc_msb = reverse_byte(crc_msb);
        crc_lsb = reverse_byte(crc_lsb);
        // Do they match?
        if((*(rx_buf + crc_start) == crc_lsb) && (*(rx_buf + crc_start + 1) == crc_msb))
        {
                return TRUE;
        }
        else
        {
```

```
                return FALSE;
        }
}
```

9.6.4.6 Acknowledge Byte

The Acknowledge Byte (“ACK”) consists of a single byte (ACK=0x7F or 0x7E):

ACK is sent back by the addressed IS32LT3132 device only if the ACKEN bit is set in the SYSCFG register (03h) and only if the write is successful. And when FAULTB pull down it will return 0x7E. A successful write yields no CRC checksum error or parity errors. Note that the acknowledge is only valid for single device write transaction of IS32LT3132.

9.6.4.7 Turnaround Time

When considering back-to-back data transfer, the turnaround time (additional time required between the end of the previous byte stop bit and the beginning of the next byte start bit) is required, that means a finite amount of dead time must be inserted between two bytes or two command frames. It’s recommended to use dual stop bits mode for the UART interface.

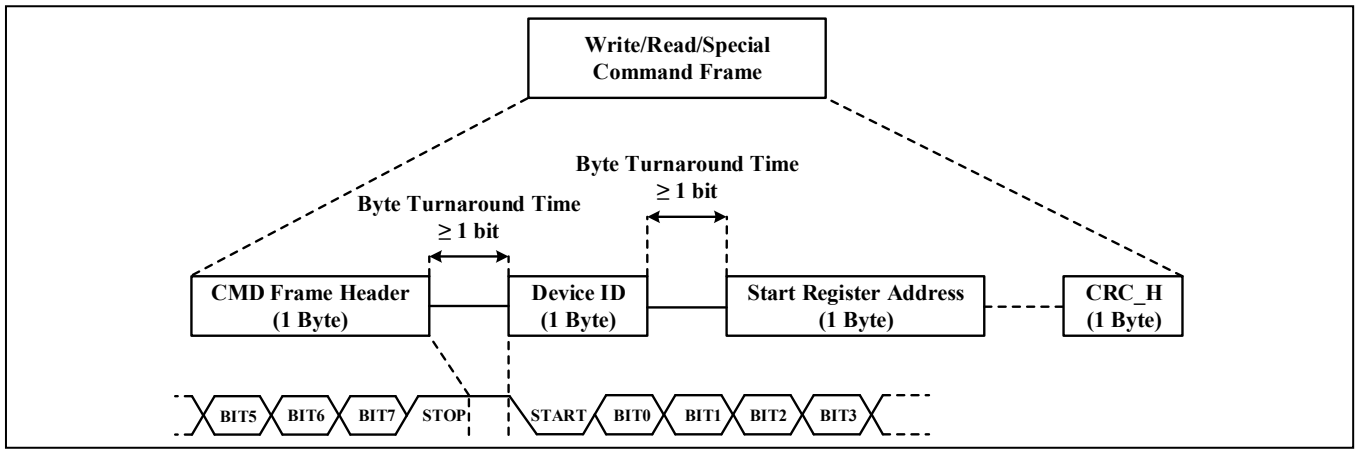


Figure 15 Turnaround Time Between Byte to Byte

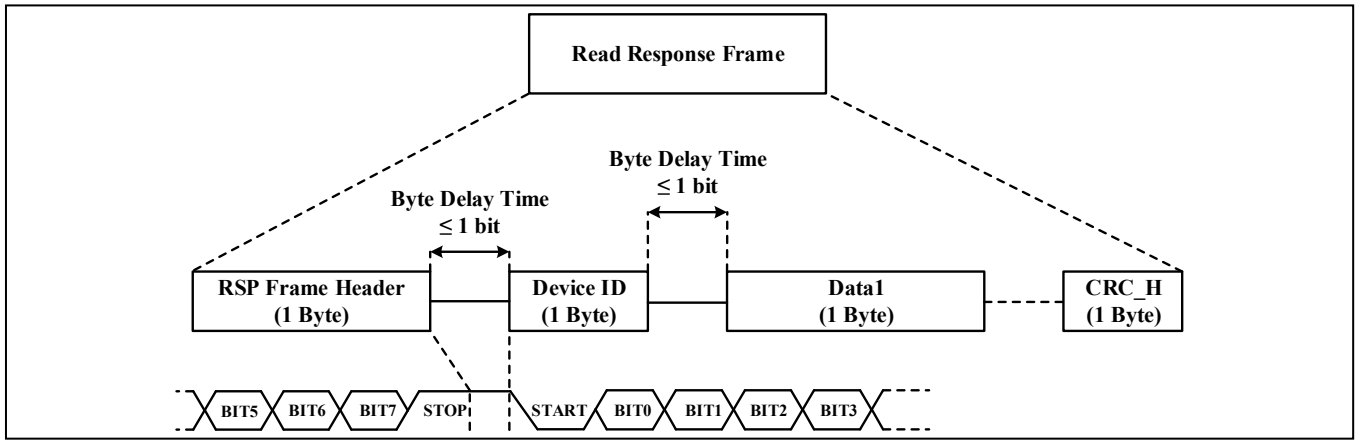


Figure 16 Delay Time Between Byte to Byte of Read Response Frame

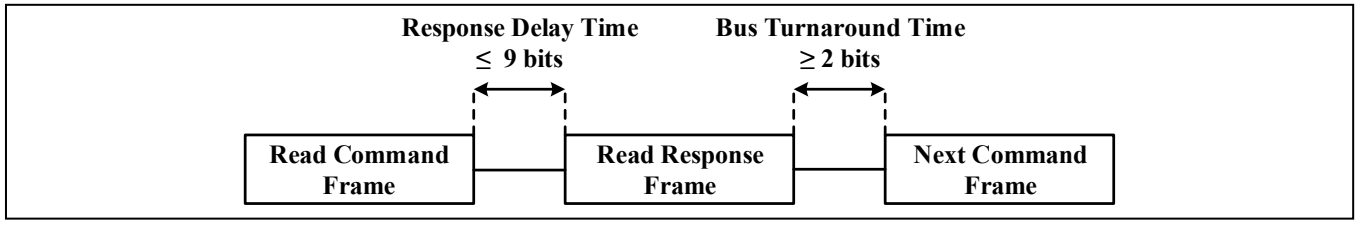


Figure 17 Turnaround Time Between Read Response Frame to Next Command Frame

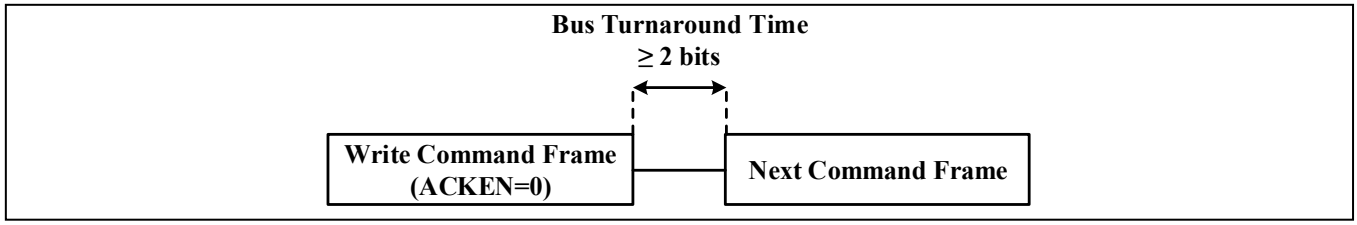


Figure 18 Turnaround Time Between Write Command Frame to Next Command Frame (ACK Disabled)

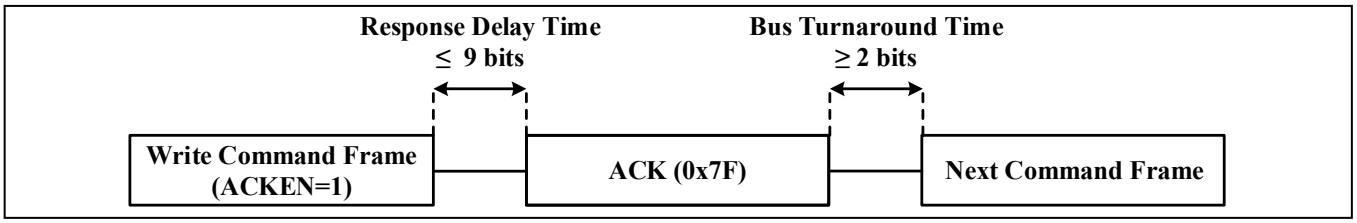


Figure 19 Turnaround Time Between ACK to Next Command Frame (ACK Enabled)

9.7 COMMUNICATIONS EXAMPLES

The total number of transmitted bytes depends on the specific task being performed. The examples below show the sequence of transmitted bytes for a given transaction.

9.7.1 Example 1: Single Device Write of 3 Bytes

Write to Device ID with parity = 0x55, R_{AD0}=30kΩ, R_{AD1}=30kΩ, R_{AD2}=30kΩ: beginning at register 26h, PWM0_H=0x1F, PWM1_H=0x2F, PWM2_H=0x3F

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
Data Bytes	3
CRC Bytes	2
Total	8

	Command Frame							
Interface	CMD Frame Header	Device ID	Start Register Address	Data 1	Data 2	Data 3	CRC_L	CRC_H
UART	0x82 (0b10000010)	0x55	0x10	0x1F	0x2F	0x3F	0x7B	0x08

Acknowledge from addressed device (if enabled ACKEN bit for IS32LT3132)

Acknowledge Frame
ACK
0x7F

9.7.2 Example 2: Single Device Read of 2 Bytes

Read from Device ID with parity = 0xA3, R_{AD0}=51kΩ, R_{AD1}=10kΩ, R_{AD2}=75kΩ: beginning at register 38H, read FAULT_TYPE_1/2

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
CRC Bytes	2
Total	5

	Command Frame				
Interface	CMD Frame Header	Device ID	Start Register Address	CRC_L	CRC_H
UART	0XC1 (0b11000001)	0xA3	0x38	0x28	0XDE

Read Response: FLT_TYPE1/2=0x00

Byte Types	Number of Bytes
RSP Frame Header Byte	1
Device ID Byte	1
Data Bytes	2
CRC Bytes	2
Total	6

	Command Frame					
Interface	RSP Frame Header	Device ID	Data 1	Data 2	CRC_L	CRC_H
UART	0x01 (0b00000001)	0XA3	0x00	0x00	0x8F	0x7B

9.7.3 Example 3: Broadcast Write of 3 Bytes

Broadcast write to all devices (fixed Device ID with parity = 0xBF): beginning at register 04h, SCA0=0x0F, SCA1=0x1F, SCA2=0x2F.

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
Start Register Address Byte	1
Data Bytes	3
CRC Bytes	2
Total	8

	Command Frame							
Interface	CMD Frame Header	Device ID	Start Register Address	Data 1	Data 2	Data 3	CRC_L	CRC_H
UART	0xA2 (0b10100010)	0xBF	0x04	0x0F	0x1F	0x2F	0x74	0x46

9.7.4 Example 4: Broadcast Registers Reset Command (Special Command)

Broadcast Registers Reset Command to all devices (fixed Device ID with parity = 0xBF):

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
CRC Bytes	2
Total	4

	Command Frame			
Interface	**CMD Frame Header**	**Device ID**	**CRC_L**	**CRC_H**
UART	0xBE (0b10111110)	0xBF	0x30	0x10

9.7.5 Example 5: Broadcast Update Command (Special Command)

Broadcast Update Command to all devices (fixed Device ID with parity = 0xBF):

Byte Types	Number of Bytes
CMD Frame Header Byte	1
Device ID Byte	1
CRC Bytes	2
Total	4

	Command Frame			
Interface	**CMD Frame Header**	**Device ID**	**CRC_L**	**CRC_H**
UART	0xB8 (0b10111000)	0xBF	0x33	0xB0

9.8 DEVICE FUNCTIONAL MODES

The IS32LT3132 device operates in one of several states.

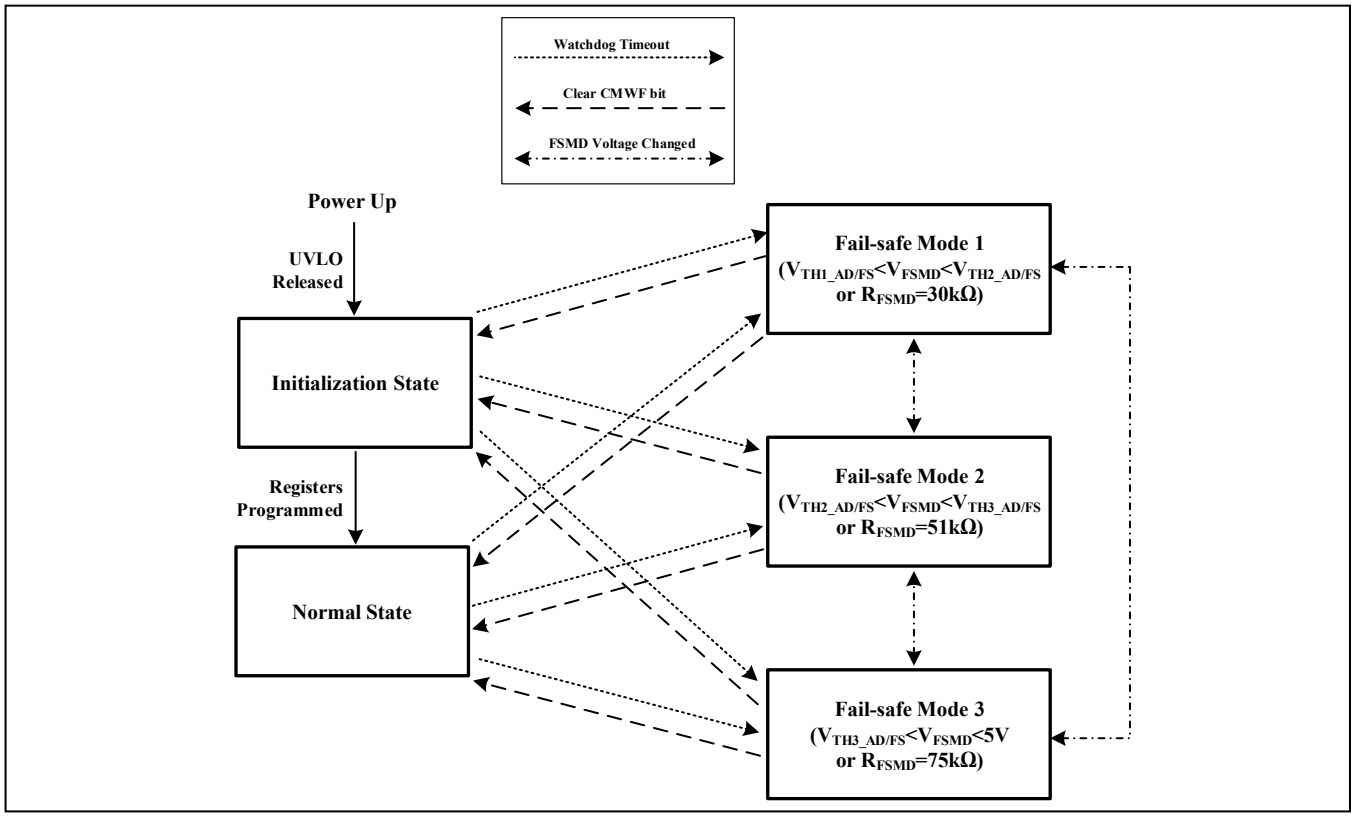


Figure 20 Operation States

9.8.1 INITIALIZATION STATE

On power up and once released from UVLO, the device enters an initialization state. In this state, all registers are reset to default values and all outputs are in off state. The device waits to receive commands from the MCU master.

9.8.2 NORMAL STATE

In normal state, the IS32LT3132 registers control its outputs by accepting interface commands and by monitoring and responding to realtime events on the inputs associated with the analog and power circuitry. This allows dimming of the LED outputs using the registers settings.

9.8.3 FAIL-SAFE STATE

This state allows the user to preset the outputs' state if the communication is broken. The device integrates a communication watchdog timer that operates based on the system clock pulse. IS32LT3132 has two internal watchdog timers, watchdog timer 1 is a communication watchdog timer, programmed through the CMWT1 register (58h), defining the time of the communication watchdog timer. The watchdog timer 2 is the command watchdog timer, programmed through the CMWT2 register (59h), which defines the maximum/minimum feeding time range of the command watchdog timer. If the communication watchdog times out (no error-free communication is successfully received within the set number of system clock cycles) or the command watchdog overflows (no feeding command is successfully received within the set time range of feeding dog), the device will enter the fail-proof mode, including three modes: Mode 1 ~ Mode 3.

The FSMD pin is used to configure the fail-safe modes. When the resistor R_{FSMD} is connected from the FSMD pin to ground, the internal $I_{AD/FS}$ (typical 50μA) current source creates a voltage on the FSMD pin, V_{FSMD}. The device compares the V_{FSMD} with internal different reference voltage levels ($V_{TH1\_AD/FS}$, $V_{TH2\_AD/FS}$ and $V_{TH3\_AD/FS}$) to determine the fail-safe mode. It also allows to externally apply proper voltage on the FSMD pin to either choose or change the fail-safe mode. Refer to the Fail-safe Mode Setting Table.

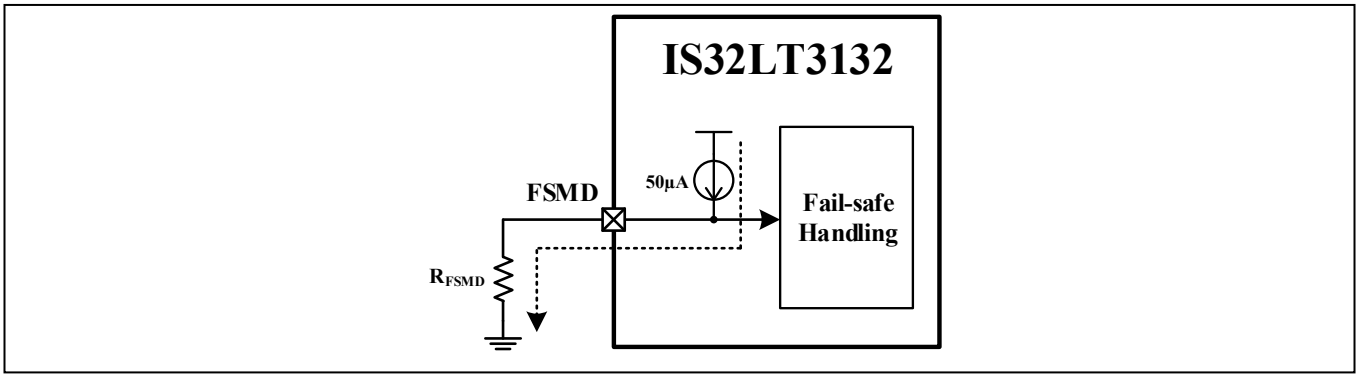


Figure 21 Fail-safe Mode Setting

When 0V<V_{FSMD}<$V_{TH1\_AD/FS}$, or R_{FSMD}=10kΩ, the internal communication watchdog is invalid, and the fail-safe mode is disabled. The outputs are always controlled by the scaling and PWM registers (10h~27h).

When $V_{TH1\_AD/FS}$<V_{FSMD}<$V_{TH2\_AD/FS}$, or R_{FSMD}=30kΩ, the internal communication watchdog 1 and command watchdog 2 is active, and the fail-safe mode is Mode 1. If the watchdog times out, the device will enter fail-safe Mode 1 and the outputs will be determined by the OTP-A DEFAULT registers (B0h~BCh). The CMWF 2 or CMW F1 bit in FAULT_TYPE_1 register (38h) will be set to “1” and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register(30h)) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF1 and CMWF2 bit in FAULT_TYPE_1 register (38h) must be cleared by the host MCU writing it to “0”, and feed the watchdog 2 for the set time. The watchdog timer will be reset and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register(30h)).

When $V_{TH2\_AD/FS}$<V_{FSMD}<$V_{TH3\_AD/FS}$, or R_{FSMD}=51kΩ, the internal communication watchdog is active, and the fail-safe mode is Mode 2. If the watchdog times out, the device will enter fail-safe Mode 2 and all outputs will be forced into completely off. The CMWF2 or CMWF1 bit in FAULT_TYPE_1 register (38h) will be set to “1” and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register(30h)) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF1 and CMWF2 bit in FAULT_TYPE_1 register (38h) must be cleared by the host MCU writing it to “0”. The watchdog timer will be reset and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register(30h)).

When VTH3_AD/FS<VFSMD<5V, or RFSMD=75kΩ, the internal communication watchdog is active, and the fail-safe mode is Mode 3. If the watchdog times out, the device will enter fail-safe Mode 3 and all outputs will be forced into fully on (with 98% PWM duty cycle). The CMWF2 or CMWF1 bit in FAULT_TYPE_1 register (38h) will be set to “1” and the FAULTB pin will go low after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register(30h)) to report the fault condition. To quit from the fail-safe mode to normal state, the CMWF1 and CMWF2 bit in FAULT_TYPE_1 register (38h) must be cleared by the host MCU writing it to “0”. The watchdog timer will be reset and the FAULTB pin will go back to high impedance after the delay time (programmed by FT[3:0] bits in FLT_CONFIG register).

In the fail-safe modes, the fault protections also are valid, including LED string open/short, single LED short, overcurrent (ISET shorted), and over temperature.

Note that the device must be re-initialized after quitting from the fail-safe mode to normal state.

9.8.4 Fail-safe Mode Setting Table

FSMD Pin	Fail-Safe Mode	LED State In Fail-Safe Mode
0V<V_{FSMD}<$V_{TH1\_AD/FS}$ or R_{FSMD}=10kΩ	Disabled	-
$V_{TH1\_AD/FS}$<V_{FSMD}<$V_{TH2\_AD/FS}$ or R_{FSMD}=30kΩ	Mode 1	Determined by OTP (B0h~BAh)
$V_{TH2\_AD/FS}$<V_{FSMD}<$V_{TH3\_AD/FS}$ or R_{FSMD}=51kΩ	Mode 2	All Completely Off
$V_{TH3\_AD/FS}$<V_{FSMD}<5V or R_{FSMD}=75kΩ	Mode 3	All On with 98% PWM duty cycle

10 REGISTERS

10.1 REGISTER MAP

ADDR HEX	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	R/W	DEFAULT
00	CONFIG	-	TROF [2:0]			OFA[1:0]		PDE	DC_PWM	R/W	0b 00001110
01	GC_CTRL	-	-	GCC [5:0]						R/W	0b 00111111
02	PWM_ CONFIG	-	-	PMS[1:0]		OFS[3:0]				R/W	0b 00000011
03	SYSCFG	SSCEN	SSC [1:0]		ACKEN	-	-	-	PWR	R/W	0b 00000000
04	SCA0	SCA0_DATA [7:0]								R/W	0b 00000000
05	SCA1	SCA1_DATA [7:0]								R/W	0b 00000000
06	SCA2	SCA2_DATA [7:0]								R/W	0b 00000000
07	SCA3	SCA3_DATA [7:0]								R/W	0b 00000000
08	SCA4	SCA4_DATA [7:0]								R/W	0b 00000000
09	SCA5	SCA5_DATA [7:0]								R/W	0b 00000000
0A	SCA6	SCA6_DATA [7:0]								R/W	0b 00000000
0B	SCA7	SCA7_DATA [7:0]								R/W	0b 00000000
0C	SCA8	SCA8_DATA [7:0]								R/W	0b 00000000
0D	SCA9	SCA9_DATA [7:0]								R/W	0b 00000000
0E	SCA10	SCA10_DATA [7:0]								R/W	0b 00000000
0F	SCA11	SCA11_DATA [7:0]								R/W	0b 00000000
10	PWM0_H	PWM0_DATA [11:4]								R/W	0b 00000000
11	PWM1_H	PWM1_DATA [11:4]								R/W	0b 00000000
12	PWM2_H	PWM2_DATA [11:4]								R/W	0b 00000000
13	PWM3_H	PWM3_DATA [11:4]								R/W	0b 00000000
14	PWM4_H	PWM4_DATA [11:4]								R/W	0b 00000000
15	PWM5_H	PWM5_DATA [11:4]								R/W	0b 00000000
16	PWM6_H	PWM6_DATA [11:4]								R/W	0b 00000000
17	PWM7_H	PWM7DATA [11:4]								R/W	0b 00000000
18	PWM8_H	PWM8_DATA [11:4]								R/W	0b 00000000
19	PWM9_H	PWM9_DATA [11:4]								R/W	0b 00000000
1A	PWM10_H	PWM10_DATA [11:4]								R/W	0b 00000000
1B	PWM11_H	PWM11_DATA [11:4]								R/W	0b 00000000
1C	PWM0_L	-	-	-	-	PWM0_DATA [3:0]				R/W	0b 00000000
1D	PWM1_L	-	-	-	-	PWM1_DATA [3:0]				R/W	0b 00000000
1E	PWM2_L	-	-	-	-	PWM2_DATA [3:0]				R/W	0b 00000000
1F	PWM3_L	-	-	-	-	PWM3_DATA [3:0]				R/W	0b 00000000
20	PWM4_L	-	-	-	-	PWM4_DATA [3:0]				R/W	0b 00000000
21	PWM5_L	-	-	-	-	PWM5_DATA [3:0]				R/W	0b 00000000

22	PWM6_L	-	-	-	-	PWM6_DATA [3:0]				R/W	0b 00000000
23	PWM7_L	-	-	-	-	PWM7_DATA [3:0]				R/W	0b 00000000
24	PWM8_L	-	-	-	-	PWM8_DATA [3:0]				R/W	0b 00000000
25	PWM9_L	-	-	-	-	PWM9_DATA [3:0]				R/W	0b 00000000
26	PWM10_L	-	-	-	-	PWM10_DATA [3:0]				R/W	0b 00000000
27	PWM11_L	-	-	-	-	PWM11_DATA [3:0]				R/W	0b 00000000
28	LED0_1_SLS	LED1_SLSTH[3:0]				LED0_SLSTH [3:0]				R/W	0b 00000000
29	LED2_3_SLS	LED3_SLSTH[3:0]				LED2_SLSTH [3:0]				R/W	0b 00000000
2A	LED4_5_SLS	LED5_SLSTH[3:0]				LED4_SLSTH [3:0]				R/W	0b 00000000
2B	LED6_7_SLS	LED7_SLSTH[3:0]				LED6_SLSTH [3:0]				R/W	0b 00000000
2C	LED8_9_SLS	LED9_SLSTH[3:0]				LED8_SLSTH [3:0]				R/W	0b 00000000
2D	LED10_11_SLS	LED11_SLSTH[3:0]				LED10_SLSTH [3:0]				R/W	0b 00000000
2E	FS_FLTL	-	-	-	-	FLT_UV[3:0]				R/W	0b 00000100
2F	FLT_DET_EN	-	-	SLSDF	SLSDE	SDF	SDE	ODF	ODE	R/W	0b 00001111
30	FLT_CONFIG	-	SHCR	OPENCR	SLSHCR	FT[3:0]				R/W	0b 01100011
31	SHORT_FLT1	-	-	SHORT_FLT[5:0]						R	0b 00000000
32	SHORT_FLT2	-	-	SHORT_FLT[11:6]						R	0b 00000000
33	OPEN_FLT1	-	-	OPEN_FLT[5:0]						R	0b 00000000
34	OPEN_FLT2	-	-	OPEN_FLT[11:6]						R	0b 00000000
35	SLS_FLT1	-	-	SLS_FLT[5:0]						R	0b 00000000
36	SLS_FLT2	-	-	SLS_FLT[11:6]						R	0b 00000000
37	FAULT_EN	ECC2F_EN	-	-	TFE	CRCFE	RSET_OPE	RSET_SHE	TSDE	R/W	0b 10011111
38	FAULT_TYPE_1	-	CMWF2	CMWF1	TF	CRCF	RSET_OP	RSET_SH	TSD	R/W	0b 00000000
39	FAULT_TYPE_2	-	-	-	-	EXF	SLSHORTF	SHORTF	OPENF	R/W	0b 00000000
3A	CERRCNT	CERRCNT [7:0]								R/W	0b 00000000
3B	CHSEL_1	CHSEL[7:0]								R/W	0b 00000000
3C	CHSEL_2	CHSEL[15:8]								R/W	0b 00000000
3D	ADCCFG	VIN_FCH [3:0]				-	ADCSH[1:0]		ADCEN	R/W	0b 00000000
3E	ADCCTL	ADCCYC_F	-	-	ADCRST	ADCCYC_T[1:0]		LOOP	SADC	R/W	0b 00000010
3F	ADC_OUT0_H	ADC_OUT0[9:2]								R	0b 00000000
40	ADC_OUT1_H	ADC_OUT1[9:2]								R	0b 00000000
41	ADC_OUT2_H	ADC_OUT2[9:2]								R	0b 00000000
42	ADC_OUT3_H	ADC_OUT3[9:2]								R	0b 00000000
43	ADC_OUT0_1_2_3_L	ADC_OUT3[1:0]		ADC_OUT2[1:0]		ADC_OUT1[1:0]		ADC_OUT0[1:0]		R	0b 00000000
44	ADC_OUT4_H	ADC_OUT4[9:2]								R	0b 00000000
45	ADC_OUT5_H	ADC_OUT5[9:2]								R	0b 00000000

46	ADC_OUT6_H	ADC_OUT6[9:2]								R	0b 00000000
47	ADC_OUT7_H	ADC_OUT7[9:2]								R	0b 00000000
48	ADC_OUT4_5_6_7_L	ADC_OUT7[1:0]		ADC_OUT6[1:0]		ADC_OUT5[1:0]		ADC_OUT4[1:0]		R	0b 00000000
49	ADC_OUT8_H	ADC_OUT8[9:2]								R	0b 00000000
4A	ADC_OUT9_H	ADC_OUT9[9:2]								R	0b 00000000
4B	ADC_OUT10_H	ADC_OUT10[9:2]								R	0b 00000000
4C	ADC_OUT11_H	ADC_OUT11[9:2]								R	0b 00000000
4D	ADC_OUT8_9_10_11_L	ADC_OUT11[1:0]		ADC_OUT10[1:0]		ADC_OUT9[1:0]		ADC_OUT8[1:0]		R	0b 00000000
4E	ADC_VPTAT_H	ADC_VPTAT [9:2]								R	0b 00000000
4F	ADC_VPTAT _L	-	-	-	-	-	-	ADC_VPTAT [1:0]		R	0b 00000000
50	ADC_VDD_H	ADC_VDD [9:2]								R	0b 00000000
51	ADC_VDD _L	-	-	-	-	-	-	ADC_VDD [1:0]		R	0b 00000000
52	ADC_VIN _H	ADC_VIN [9:2]								R	0b 00000000
53	ADC_VIN _L	-	-	-	-	-	-	ADC_VIN [1:0]		R	0b 00000000
54	ADC_VBG _H	ADC_VBG [9:2]								R	0b 00000000
55	ADC_VBG _L	-	-	-	-	-	-	ADC_VBG [1:0]		R	0b 00000000
56	MAX_OUT _H	MAX_OUT [9:2]								R	0b 00000000
57	MAX_OUT _L	-	-	-	-	-	-	MAX_OUT [1:0]		R	0b 00000000
58	CMWT1	-	-	-	-	-	CMWTAP [2:0]			R/W	0b 00000011
59	CMWT2	-	WDT2CLR	WDT2_MAX[2:0]			WDT2_MIN[2:0]			R/W	0b 00011000
OTP-Registers											
AD	OTP_CTRL	p1	p0	Cmd[1:0]		Sel[3:0]				R/W	0b 00000000
AE	OTP_ST	-	-	-	-	-	FAIL	FINISH	BUSY	R	0b 00000000
AF	ECC_ST	-	IMD_2Err_ecc A	-	IMD_1Err_ecc A	-	-	-	-	R	0b 00000000
OTP-A											
B0	DEFCONF1	DEFDC_PWM	-	DEFPFMS[1:0]		DEFFPS[3:0]				R/W	0b 00000000
B1	DEFGCC	-	-	DEF_GCC[5:0]						R/W	0b 00000000
B2	DEFCONF2	-		DEFSSC [1:0]		DEFSSC EN	DEFTROF [2:0]			R/W	0b 00000000
B3	DEFLED1	-	-	DEFLED[5:0]						R/W	0b 00000000
B4	DEFLED2	-	-	DEFLED[11:6]						R/W	0b 00000000
B5	DEFPWM1	PWM1[3:0]				PWM0[3:0]				R/W	0b 00000000
B6	DEFPWM2	PWM3[3:0]				PWM2[3:0]				R/W	0b 00000000
B7	DEFPWM3	PWM5[3:0]				PWM4[3:0]				R/W	0b 00000000
B8	DEFPWM4	PWM7[3:0]				PWM6[3:0]				R/W	0b 00000000
B9	DEFPWM5	PWM9[3:0]				PWM8[3:0]				R/W	0b 00000000
BA	DEFPWM6	PWM11[3:0]				PWM10[3:0]				R/W	0b 00000000

BB	ECC_A	ECCA	W	0b 00000000
BC	W_PROTECT_A	WPROTECTA	W	0b 00000000
FCh	OTP_UNLOCK	OTPUNLOCK	W	0b 00000000

Note 11: "RSVD" means "Reserved".

10.2 REGISTERS DEFINITION

10.2.1 00h CONFIG Register

ADDR	REG NAME	D7	D6:D4	D3:D2	D1	D0	DEFAULT
00h	CONFIG	-	TROF [2:0]	OFA[1:0]	PDE	DC_PWM	0b 00001110

The current of thermal roll off will not be a fixed proportion, and the slope of roll off can be calculated by formula. $I_{ROLL} = I_{SET} \times (2V\text{-}V_x)/2)$, I_{ROLL} is the current after roll off, I_{SET} is the current before roll off, and V_x is the optional voltage (TROF bits) of the register.

TROF	Percentage of output current before thermal shutdown happens
000	0V
001	0.2V
010	0.4V
011	0.6V
100	0.8V
101	1.0V
110	1.2V
111	1.4V

OFAx	“One Fail Others On” or “One Fail All Fail” fault action mode setting
0X	“One Fail All Fail” (single LED short fault latches all outputs off, open or short auto recover)
10	“One Fail All Fail” (auto recover)
11	“One Fail Others On”

PDE	Phase delay enable
0	Disable
1	Enable (6 groups phase delay)

DC_PWM	DC or PWM output select for all outputs
0	PWM dimming. PWM duty cycle is determined by PWM registers 10h~21h
1	DC output. PWM dimming is disabled, and all outputs are DC current (IOUTx)

10.2.2 01h GC_CTRL Register

ADDR	REG NAME	D7:D6	D5:D0	DEFAULT
01h	GC_CTRL	-	GCC [5:0]	0b 00111111

GCC and SCAx control the I_{OUT} as shown in following formula:

$$I_{OUT\_F} = I_{OUT(MAX)} \times \frac{GCC}{64} \times \frac{SCAx}{256} \quad (8)$$

$$GCC = \sum_{n=0}^{5} D[n] \cdot 2^n \quad (9)$$

$$SCAx = \sum_{n=0}^{7} D[n] \cdot 2^n \quad (10)$$

10.2.3 02h PWM Configuration Register

ADDR	REG NAME	D7:D6	D5:D4	D3:D0	DEFAULT
02h	PWM_ CONFIG	-	PMS[1:0]	OFS[3:0]	0b 00000011

PMS	PWM Mode Select
00/11	12bit (Default)
01	7+5bit
10	8bit

OFS	OSC Frequency Select
0000	12bit, 2kHz 7+5bit, 64kHz 8bit, 32kHz

0001	12bit, 1kHz 7+5bit, 32kHz 8bit, 16kHz
0010	12bit, 700Hz 7+5bit, 21.3kHz 8bit, 10.7kHz
0011	12bit, 500Hz (Default) 7+5bit, 16kHz 8bit, 8kHz
0100	12bit, 400Hz 7+5bit, 12.8kHz 8bit, 6.4kHz
0101	12bit, 333Hz 7+5bit, 10.7kHz 8bit, 5.3kHz
0110	12bit, 285Hz 7+5bit, 9.1kHz 8bit, 4.6kHz
0111	12bit, 250Hz 7+5bit, 8kHz 8bit, 4kHz
1000	12bit, 222Hz 7+5bit, 7.1kHz 8bit, 3.6kHz
1001	12bit, 200Hz 7+5bit, 6.4kHz 8bit, 3.2kHz
1010	12bit, 182Hz 7+5bit, 5.8kHz 8bit, 2.9kHz
1011	12bit, 20.8Hz 7+5bit, 666Hz 8bit, 333Hz
1100	12bit, 9.6Hz 7+5bit, 307Hz 8bit, 154Hz
1101	12bit, 7.8Hz 7+5bit, 250Hz 8bit, 125Hz
1110	12bit, 5.9Hz 7+5bit, 188Hz 8bit, 94Hz
1111	12bit, 2.95Hz 7+5bit, 94Hz 8bit, 47Hz

10.2.4 03h System Configuration Register (SYSCFG)

ADDR	REG NAME	D7	D6:D5	D4	D3:D1	D0	DEFAULT
03h	SYSCFG	SSCEN	SSC [1:0]	ACKEN	-	PWR	0b 00000000

ACKEN Acknowledge Enable
0 No acknowledge is transmitted following successfully received writes
1 Return 0x7F or 0x7E, when FAULTB pull down return 0x7E.

PWR This bit is reset to 0 upon power-up. It may be written to a 1 by the MCU. Reading this bit allows the MCU to detect if there has been a power cycle.
0 A power cycle has occurred since last write to a '1'
1 No power cycle has occurred since the last write to a '1'

SSCEN Spread Spectrum Enable
0 Disable
1 Enable-not allowed when PWM frequency is 250Hz

SSC Spread Spectrum frequency Range
00 125Hz
01 250Hz
10 500Hz
11 1kHz

10.2.5 04h~0Fh Scaling Registers

ADDR	REG NAME	D7:D0	DEFAULT
04h	SCA0	SCA0_DATA [7:0]	0b 00000000
05h	SCA1	SCA1_DATA [7:0]	0b 00000000
06h	SCA2	SCA2_DATA [7:0]	0b 00000000
07h	SCA3	SCA3_DATA [7:0]	0b 00000000
08h	SCA4	SCA4_DATA [7:0]	0b 00000000
09h	SCA5	SCA5_DATA [7:0]	0b 00000000
0Ah	SCA6	SCA6_DATA [7:0]	0b 00000000
0Bh	SCA7	SCA7_DATA [7:0]	0b 00000000
0Ch	SCA8	SCA8_DATA [7:0]	0b 00000000
0Dh	SCA9	SCA9_DATA [7:0]	0b 00000000
0Eh	SCA10	SCA10_DATA [7:0]	0b 00000000
0Fh	SCA11	SCA11_DATA [7:0]	0b 00000000

The 8-bit Scaling Registers SCAx (04h~0Fh) individually set the DC output current of each channel.

GCC[5:0] and SCAx control the OUTx current (I_{OUTx}) as shown in following equation:

$$I_{OUTx} = I_{OUT\_FU} \times \frac{GCC}{64} \times \frac{SCAx}{256} \qquad (11)$$

Where, x is from0 to 11 for different output channel.

$$GCC = \sum_{n=0}^{5} D[n] \cdot 2^n \qquad (12)$$

$$SCAx = \sum_{n=0}^{7} D[n] \cdot 2^n \qquad (13)$$

10.2.6 10h~27h PWM Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
10h	PWM0_H	PWM0_DATA [11:4]								0b 00000000
11h	PWM1_H	PWM1_DATA [11:4]								0b 00000000
12h	PWM2_H	PWM2_DATA [11:4]								0b 00000000
13h	PWM3_H	PWM3_DATA [11:4]								0b 00000000
14h	PWM4_H	PWM4_DATA [11:4]								0b 00000000
15h	PWM5_H	PWM5_DATA [11:4]								0b 00000000
16h	PWM6_H	PWM6_DATA [11:4]								0b 00000000
17h	PWM7_H	PWM7DATA [11:4]								0b 00000000
18h	PWM8_H	PWM8_DATA [11:4]								0b 00000000
19h	PWM9_H	PWM9_DATA [11:4]								0b 00000000
1Ah	PWM10_H	PWM10_DATA [11:4]								0b 00000000
1Bh	PWM11_H	PWM11_DATA [11:4]								0b 00000000
1Ch	PWM0_L	-	-	-	-	PWM0_DATA [3:0]				0b 00000000
1Dh	PWM1_L	-	-	-	-	PWM1_DATA [3:0]				0b 00000000
1Eh	PWM2_L	-	-	-	-	PWM2_DATA [3:0]				0b 00000000
1Fh	PWM3_L	-	-	-	-	PWM3_DATA [3:0]				0b 00000000
20h	PWM4_L	-	-	-	-	PWM4_DATA [3:0]				0b 00000000
21h	PWM5_L	-	-	-	-	PWM5_DATA [3:0]				0b 00000000
22h	PWM6_L	-	-	-	-	PWM6_DATA [3:0]				0b 00000000
23h	PWM7_L	-	-	-	-	PWM7_DATA [3:0]				0b 00000000
24h	PWM8_L	-	-	-	-	PWM8_DATA [3:0]				0b 00000000
25h	PWM9_L	-	-	-	-	PWM9_DATA [3:0]				0b 00000000
26h	PWM10_L	-	-	-	-	PWM10_DATA [3:0]				0b 00000000
27h	PWM11_L	-	-	-	-	PWM11_DATA [3:0]				0b 00000000

10.2.7 28h~2Dh Single LED Short Threshold Setting Registers

ADDR	REG NAME	D7:D4	D3:D0	DEFAULT
28h	LED0_1_SLS	LED1_SLSTH[3:0]	LED0_SLSTH [3:0]	0b 00000000
29h	LED2_3_SLS	LED3_SLSTH[3:0]	LED2_SLSTH [3:0]	0b 00000000
2Ah	LED4_5_SLS	LED5_SLSTH[3:0]	LED4_SLSTH [3:0]	0b 00000000
2Bh	LED6_7_SLS	LED7_SLSTH[3:0]	LED6_SLSTH [3:0]	0b 00000000
2Ch	LED8_9_SLS	LED9_SLSTH[3:0]	LED8_SLSTH [3:0]	0b 00000000
2Dh	LED10_11_SLS	LED11_SLSTH[3:0]	LED10_SLSTH [3:0]	0b 00000000

LEDx_SLSTH	Singe LED short threshold voltage)
0000	2.5V
0001	3.2V
0010	3.9V
0011	4.6V
0100	5.3V
0101	6.0V

0110	6.7V
0111	7.4V
1000	8.1V
1001	8.8V
1010	9.5V
1011	10.2V
1100	11.4V
1101	12.6V
1110	13.8V
1111	15.0V

10.2.8 2Eh FS_FLTL Register

ADDR	REG NAME	D7:D4	D3:D0	DEFAULT
2Eh	FS_FLTL	-	FLT_UV	0b 00000100

FLT_UV set UVLO threshold VFLT_UV for the LED open fault detection and single LED short fault detection to prevent false fault triggering due to insufficient power supply voltage:

FLT_UV	UVLO threshold voltage for the LED open fault detection and single LED short fault detection
0000	4.3V
0001	5V
0010	5.8V
0011	6.8V
0100	7.8V(default)
0101	8.8V
0110	9.8V
0111	10.8V
1000	11.8V
1001	12.8V
1010	13.8V
1011	14.8V
1100	15.8V
1101	15.8V
1110	15.8V
1111	15.8V

10.2.9 2Fh Diagnostic Register

ADDR	REG NAME	D7:D6	D5	D4	D3	D2	D1	D0	DEFAULT
2Fh	FLT_DET_EN	-	SLSDF	SLSDE	SDF	SDE	ODF	ODE	0b 00001111

SLSDF	Single LED Short Report Enable at FAULTB pin
0	Report disabled
1	Report enabled

SLSDE	Single LED Short Detect Enable
0	Detect disabled
1	Detect enabled

SDF	Short Report Enable at FAULTB pin
0	Report disabled
1	Report enabled

SDE	Short Detect Enable
0	Detect disabled
1	Detect enabled

ODF Open Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

ODE Open Detect Enable
0 Detect disabled
1 Detect enabled

10.2.10 30h~36h Diagnostic Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
30h	FLT_CONFIG	-	SHCR	OPENCR	SLSHCR	FT[3:0]				0b 01100011
31h	SHORT_FLT1	-	-	SHORT_FLT[5:0]						0b 00000000
32h	SHORT_FLT2	-	-	SHORT_FLT[11:6]						0b 00000000
33h	OPEN_FLT1	-	-	OPEN_FLT[5:0]						0b 00000000
34h	OPEN_FLT2	-	-	OPEN_FLT[11:6]						0b 00000000
35h	SLS_FLT1	-	-	SLS_FLT[5:0]						0b 00000000
36h	SLS_FLT2	-	-	SLS_FLT[11:6]						0b 00000000

FT Fault report delay time setting
0000 32μs
0001 64μs
0010 128μs
0011 256μs (Default)
0100 512μs
0101 1.024ms
0110 2.048ms
0111 4.096ms
1000 7.8125ms
1001 15.625ms
1010 31.25ms
1011 62.5ms
1100 0.125s
1101 0.25s
1110 0.5s
1111 1s

SLSHCR single LED short output current reduce
0 No reduce
1 Output current reduced to 4mA (Typ.)

SHCR LED short output current reduce
0 No reduce
1 Output current reduced to 4mA (Typ.)

OPENCR LED OPEN output current reduce
0 No reduce
1 Output current reduced to 4mA (Typ.)

SHORT_FLTx LED string short fault flag for each OUT0~OUT11
0 No LED string shorted
1 LED string shorted

OPEN_FLTx LED string open fault flag for each OUT0~OUT11
0 No LED string open
1 LED string open

SLS_FLTx Single LED short fault flag for each OUT0~OUT11
0 No single LED shorted
1 Single LED shorted

10.2.11 37h Fault Diagnostic Register

ADDR	REG NAME	D7	D6:D5	D4	D3	D2	D1	D0	DEFAULT
37h	FAULT_EN	ECC2F_EN	-	TFE	CRCFE	RSET_OPE	RSET_SHE	TSDE	0b 10011111

ECC2F_EN ECC2 error Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

TFE Thermal rolloff Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

CRCFE Interface communication Check Sum Failure Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

RSET_OPE ISET pin open Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

RSET_SHE ISET pin short Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

TSDE Thermal shutdown Report Enable at FAULTB pin
0 Report disabled
1 Report enabled

10.2.12 38h Fault Type Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
38h	FAULT_TYPE_1	-	CMWF2	CMWF1	TF	CRCF	RSET_OP	RSET_SH	TSD	0b 00000000

Fault flags. When bit=1, fault flag is asserted.

CMWF2 Watch dog 2 Communication Time-Out fault flag
0 No communication time-out
1 Communication time-out

CMWF1 Watch dog 1 Communication Time-Out fault flag
0 No communication time-out
1 Communication time-out

TF Thermal rolloff fault flag
0 No thermal rolloff
1 Thermal rolloff

CRCF Interface communication Check Sum Failure fault flag
0 No communication Check Sum Failure
1 Communication Check Sum Failure

RSET_OP ISET pin open fault flag
0 No open
1 Opened

RSET_SH ISET pin short fault flag
0 No short
1 Shorted

TSD Thermal shutdown fault flag
0 No thermal shutdown
1 Thermal shutdown

10.2.13 39h Fault Type Register

ADDR	REG NAME	D7:D4	D3	D2	D1	D0	DEFAULT
39h	FAULT_TYPE_2	-	EXF	SLSHORTF	SHORTF	OPENF	0b 00000000

Fault flags. When bit=1, fault flag is asserted.

EXF external fault flag
0 No fault pin pulled down externally
1 Fault pin pulled down externally

SLSHORTF Single LED Short fault flag. Any out occurs single LED short, this bit will set to 1.
0 No single LED short
1 Single LED short

SHORTF LED Short fault flag. Any out occurs LED short, this bit will set to 1.
0 No LED short
1 LED short

OPENF LED Open fault flag. Any out occurs LED open, this bit will set to 1.
0 No LED open
1 LED open

10.2.14 3Ah Diagnostic Register (Continue)

ADDR	REG NAME	D7:D0	DEFAULT
3Ah	CERRCNT	CERRCNT [7:0]	0b 00000000

This register value is incremented each time a CRC error is received. This register may be read by the MCU and then written back to 0 to clear the count. The CERRCNT value saturates at FFh; it does not wrap back to 0 when it reaches FFh. The CERRCNT register is not automatically cleared when a communications reset is received. It must be cleared manually by writing it back to 0. Note that the CERRCNT register can be written to any 8-bit value. This is intended for diagnostic purposes.

10.2.15 3Bh~3Ch ADC Input Channels Select Registers

ADDR	REG NAME	D7:D0	DEFAULT
3Bh	CHSEL_1	CHSEL[7:0]	0b 00000000
3Ch	CHSEL_2	CHSEL[15:8]	0b 00000000

CHSELx ADC sampling channels select.
The ADC has fifteen multiplexed input channels (CH0~CH17) which can be respectively selected by the CHSEL[0]~CHSEL[17] bits. As below table. Multiple channels can be selected which will be periodically measured in turn.

Input Channel Select Bit	Channel No.	Input Signal	Setting
CHSEL[0]	CH0	V_{OUT0}	"0" = Not Selected "1" = Selected
CHSEL[1]	CH1	V_{OUT1}	
…	…	…	
CHSEL[11]	CH11	V_{OUT11}	
CHSEL[12]	CH12	V_{PTAT}	
CHSEL[13]	CH13	V_{DD}	
CHSEL[14]	CH14	VIN	
CHSEL[15]	CH15	VBG	

10.2.16 3Dh ADC Configuration Register

ADDR	REG NAME	D7:D4	D3	D2:D1	D0	DEFAULT
3Dh	ADCCFG	VIN_FCH[3:0]	-	ADCSH[1:0]	ADCEN	0b 00000000

VIN_FCH VIN follow channel
0000 DC detect
0001 OUT0
0010 OUT1
0011 OUT2
0100 OUT3
0101 OUT4
0110 OUT5
0111 OUT6
1000 OUT7
1001 OUT8
1010 OUT9
1011 OUT10
1100 OUT11
Others DC detect

ADCSHx ADC sample/hold time setting
00/01 ADC sample/hold time = 4 ADC CLK (Default)
10 ADC sample/hold time = 8 ADC CLK
11 ADC sample/hold time = 16 ADC CLK

ADCEN ADC Enable
0 Disabled
1 Enabled

10.2.17 3Eh ADC Control Register

ADDR	REG NAME	D7	D6:D5	D4	D3:D2	D1	D0	DEFAULT
3Eh	ADCCTL	ADCCYC_F	-	ADCRST	ADCCYC_T[1:0]	LOOP	SADC	0b 00000010

ADCCYC_F ADC sampling finished flag (Read only)
0 ADC sampling in progress, ADC result is not valid
1 ADC sampling finished, ADC result is valid reading for host MCU

ADCCYC_Tx ADC cycle sampling period
00 ADC Cycle sampling for 2 PWM cycles (Default)
01 ADC Cycle sampling for 4 PWM cycles

10 ADC Cycle sampling for 8 PWM cycles
11 ADC Cycle sampling for 16 PWM cycles
To get more stable and precise result, OUTx voltage is always sampled for multiple PWM cycles to calculate the average value.

LOOP ADC sampling mode
ADC single conversion
Enable continue ADC conversion (Default)

SADC Start ADC measurement
0 ADC measurement stops (Default)
1 ADC measurement starts
Please set ADCEN bit at first, then set SADC bit, otherwise ADC cannot measure voltage.

ADCRST Reset all ADC result registers (39h~51h) to default value when ADC measurement starts
0 Not reset (Default)
1 Reset

10.2.18 3Fh~4Dh ADC Output detect Result Registers

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
3Fh	ADC_OUT0_H	ADC_OUT0[9:2]								0b 00000000
40h	ADC_OUT1_H	ADC_OUT1[9:2]								0b 00000000
41h	ADC_OUT2_H	ADC_OUT2[9:2]								0b 00000000
42h	ADC_OUT3_H	ADC_OUT3[9:2]								0b 00000000
43h	ADC_OUT0_1_2_3_L	ADC_OUT3[1:0]		ADC_OUT2[1:0]		ADC_OUT1[1:0]		ADC_OUT0[1:0]		0b 00000000
44h	ADC_OUT4_H	ADC_OUT4[9:2]								0b 00000000
45h	ADC_OUT5_H	ADC_OUT5[9:2]								0b 00000000
46h	ADC_OUT6_H	ADC_OUT6[9:2]								0b 00000000
47h	ADC_OUT7_H	ADC_OUT7[9:2]								0b 00000000
48h	ADC_OUT4_5_6_7_L	ADC_OUT7[1:0]		ADC_OUT6[1:0]		ADC_OUT5[1:0]		ADC_OUT4[1:0]		0b 00000000
49h	ADC_OUT8_H	ADC_OUT8[9:2]								0b 00000000
4Ah	ADC_OUT9_H	ADC_OUT9[9:2]								0b 00000000
4Bh	ADC_OUT10_H	ADC_OUT10[9:2]								0b 00000000
4Ch	ADC_OUT11_H	ADC_OUT11[9:2]								0b 00000000
4Dh	ADC_OUT8_9_10_11_L	ADC_OUT11[1:0]		ADC_OUT10[1:0]		ADC_OUT9[1:0]		ADC_OUT8[1:0]		0b 00000000

ADC_OUTx The ADC result of each OUTx pin voltage.

This result can be used to calculate the OUTx pin voltage by following equation:

$$V_{OUTx}(V) = \frac{\sum_{n=0}^{9} D[n] \cdot 2^n}{1024} \times V_{REFADC} \times 8 \qquad (14)$$

10.2.19 4Eh~4Fh ADC PTAT Voltage Result Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
4Eh	ADC_VPTAT_H	ADC_VPTAT [9:2]								0b 00000000
4Fh	ADC_VPTAT _L	-	-	-	-	-	-	ADC_VPTAT [1:0]		0b 00000000

ADC_VPTATx The ADC result of internal PTAT voltage.

This result can be used to estimate the device junction temperature by following equation:

$$T_J(°C) = \frac{(\frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times V_{REFADC} - 0.982)}{0.003752} + 25 \qquad (15)$$

Where, V_{REFADC} is the reference voltage of the ADC, typical 2.5V.

10.2.20 50h~51h ADC VDD Voltage Result Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
50h	ADC_VDD_H	ADC_VDD [9:2]								0b 00000000
51h	ADC_VDD _L	-	-	-	-	-	-	ADC_VDD [1:0]		0b 00000000

ADC_VDDx The ADC result of VDD voltage.

This result can be used to calculate the VDD voltage by following equation:

$$V_{VDD}(V) = \frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times V_{REFADC} \times 5 \qquad (16)$$

10.2.21 52h~53h ADC VIN Voltage Result Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
52h	ADC_VIN _H	ADC_VIN [9:2]								0b 00000000
53h	ADC_VIN _L	-	-	-	-	-	-	ADC_VIN [1:0]		0b 00000000

ADC_VINx The ADC result of VIN voltage.

This result can be used to calculate the VIN voltage by following equation:

$$V_{VIN}(V) = \frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times V_{REFADC} \times 8 \qquad (17)$$

10.2.22 54h~55h ADC BG Result Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
54h	ADC_VBG _H	ADC_VBG [9:2]								0b 00000000
55h	ADC_VBG _L	-	-	-	-	-	-	ADC_VBG [1:0]		0b 00000000

ADC_ VBG x The ADC result of internal BG voltage.

This result can be used to calculate the BG voltage by following equation:

$$V_{VBG}(V) = \frac{\sum_{n=0}^{9} D[n]\cdot 2^n}{1024} \times V_{REFADC} \qquad (18)$$

10.2.23 56h~57h VOUT maximum Result Register

ADDR	REG NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
56h	MAX_OUT _H	MAX_OUT [9:2]								0b 00000000
57h	MAX_OUT _L	-	-	-	-	-	-	MAX_OUT [1:0]		0b 00000000

VOUT maximum value.

10.2.24 58h Watchdog Timer 1 Register

ADDR	REG NAME	D7:D3	D2:D0	DEFAULT
58h	CMWT1	-	CMWTAP [2:0]	0b 00000011

CMWTAP [2:0] This 3-bit value selects the tap point (i.e., bit number, starting from 0) on the 24-bit communications watchdog timer to establish the time-out condition.

000 8ms
001 16ms
010 32ms
011 64ms(default)
100 128ms
101 256ms
110 512ms
111 1024ms

10.2.25 59h Watchdog Timer 2 Register

ADDR	REG NAME	D7	D6	D5:D3	D2:D0	DEFAULT
59h	CMWT2	-	WDT2CLR	WDT2_MAX[2:0]	WDT2_MIN[2:0]	0b 00011000

WDT2CLR WDT2 Counter Clear.

Writing “1” to WDT2CLR clears the WDT2 count to 0. It is self-cleared by hardware.

WDT2MAX with 8M clock

000 8ms
001 16ms
010 32ms
011 64ms(default)
100 128ms
101 256ms
110 512ms
111 1024ms

WDTMAX hold the timeout value for watchdog timer 2. When the counter reaches WDT2 timeout value, a fault flag is generated.

WDT2MIN with 8M clock

000 8ms(default)
001 16ms
010 32ms
011 64ms
100 128ms
101 256ms
110 512ms
111 1024ms

WDTMIN hold the minimum value for watchdog timer 2. If WDT2 is cleared before reaching WDT2MIN, a fault flag is also generated.

10.2.26 ADh OTP Control Register

ADDR	REG NAME	D7	D6	D5:D4	D3:D0	DEFAULT
ADh	OTP_CTRL	p1	p0	Cmd[1:0]	Sel[3:0]	0b 00000000

This register must be written after a special command
There are four select OTP ZoneX bits, two OTP operation bits and two parity bits.
The parity bits for the OTP control byte are calculated with the equations below:
p[1] = ~(Sel[1] ^ Sel[3] ^ Cmd[0] ^ Cmd[1])
p[0] = Sel[0] ^ Sel[1] ^ Sel[2] ^ Cmd[0]

Cmd Comand Select
01 OTP write operation
11 OTP read operation

Sel Zone Select
0001 select OTP Zone A
Other no operation

10.2.27 AEh OTP Status Register

ADDR	REG NAME	D7:D3	D2	D1	D0	DEFAULT
AEh	OTP_ST	-	FAIL	FINISH	BUSY	0b 00000000

FAIL OTP write fail
FINISH OTP write finish
BUSY OTP operation in progress

10.2.28 AFh ECC Status Register

ADDR	REG NAME	D7	D6	D5	D4	D3:D0	DEFAULT
AFh	ECC_ST	-	IMD_2Err_ecc A	-	IMD_1Err_ecc A	-	0b 00000000

IMD_2Err_ecc A ECC detects 2bit or more errors
IMD_1Err_ecc A ECC detected 1bit error

10.2.29 B0h DEFCONFIG-1 Register (fail safe mode 1)

ADDR	REG NAME	D7	D6	D5:D4	D3:D0	DEFAULT
B0h	DEFCONF1	DEFDC_PWM	-	DEFPFMS[1:0]	DEFPFS[3:0]	0b 00000000

DEFDC_PWM DC or PWM output select for all outputs
0 PWM dimming. PWM duty cycle is determined by PWM registers B6h~BEh
1 DC output. PWM dimming is disabled, and all outputs are DC current (IOUTx)

DEFPFMS PWM Frequency multiple Select
00/11 1x (Default)
01 32x
10 16x

DEFPFS PWM Frequency Select

0000	1x,	2kHz (Default)
	16x,	32kHz
	32x	64kHz
0001	1x,	1kHz
	16x,	16kHz
	32x	32kHz
0010	1x,	700Hz
	16x,	21.3kHz
	32x	10.7kHz
0011	1x,	500Hz
	16x,	16kHz
	32x	8kHz
0100	1x,	400Hz
	16x,	12.8kHz
	32x	6.4kHz

0101	1x,	333Hz
	16x,	10.7kHz
	32x	5.3kHz
0110	1x,	285Hz
	16x,	9.1kHz
	32x	4.6kHz
0111	1x,	250Hz
	16x,	8kHz
	32x	4kHz
1000	1x,	222Hz
	16x,	7.1kHz
	32x	3.6kHz
1001	1x,	200Hz
	16x,	6.4kHz
	32x	3.2kHz
1010	1x,	182Hz
	16x,	5.8kHz
	32x	2.9kHz
1011	1x,	20.8Hz
	16x,	333Hz
	32x	666Hz
1100	1x,	9.6Hz
	16x,	154Hz
	32x	307Hz
1101	1x,	7.8Hz
	16x,	125Hz
	32x	250Hz
1110	1x,	5.9Hz
	16x,	94Hz
	32x	188Hz
1111	1x,	2.95Hz
	16x,	47Hz
	32x	94Hz

10.2.30 B1h DEFGCC Register (fail safe mode 1)

ADDR	REG NAME	D7:D6	D5:D0	DEFAULT
B1h	DEFGCC	-	DEFGCC [5:0]	0b 00000000

DEFGCC control the I_{OUT} as shown in following formula:

$$I_{OUT\_F} = I_{OUT(MAX)} \times \frac{GCC}{63} \quad (19)$$

$$GCC = \sum_{n=0}^{5} D[n] \cdot 2^n \quad (20)$$

10.2.31 B2h DEFCONFIG-2 Register (fail safe mode 1)

ADDR	REG NAME	D7:D6	D5:D4	D3	D2:D0	DEFAULT
B2h	DEFCONF2	-	DEFSSC [1:0]	DEFSSCEN	DEFTROF [2:0]	0b 00000000

The current of thermal roll off will not be a fixed proportion, and the slope of roll off can be calculated by formula. I_{ROLL}= Iset * (2V-Vx) / 2, I_{ROLL} is the current after roll off, I_{SET} is the current before roll off, and Vx is the optional voltage (TROF bits) of the register.

EDFTROF	Percentage of output current before thermal shutdown happens
000	0V
001	0.2V
010	0.4V
011	0.6V
100	0.8V
101	1.0V
110	1.2V
111	1.4V

DEFSSCEN	Spread Spectrum Enable
0	Disable
1	Enable-not allowed when PWM frequency is 250Hz

DEFSSC	Spread Spectrum frequency Range
00	125Hz
01	250Hz
10	500Hz
11	1kHz

10.2.32 B3h~B4h DEFLED Register (fail safe mode 1)

ADDR	REG NAME	D7:D6	D5:D0	DEFAULT
B3h	DEFLED1	-	DEFLED[5:0]	0b 00000000
B4h	DEFLED2	-	DEFLED[11:6]	0b 00000000

DEFLEDx	LED State Bit
0	LED off
1	LED on

10.2.33 B5h~BAh DEFPWM Register (fail safe mode 1)

ADDR	REG NAME	D7:D4	D3:D0	DEFAULT
B5h	DEFPWM1	PWM1[3:0]	PWM0[3:0]	0b 00000000
B6h	DEFPWM2	PWM3[3:0]	PWM2[3:0]	0b 00000000
B7h	DEFPWM3	PWM5[3:0]	PWM4[3:0]	0b 00000000
B8h	DEFPWM4	PWM7[3:0]	PWM6[3:0]	0b 00000000
B9h	DEFPWM5	PWM9[3:0]	PWM8[3:0]	0b 00000000
BAh	DEFPWM6	PWM11[3:0]	PWM10[3:0]	0b 00000000

Each OUTx has 4-bit to modulate the PWM duty cycle in 16 steps.

The value of the PWM Registers decides the average current of each OUTx LED noted I_{LED}.

I_{LED} computed by following formula:

$$I_{OUTx\_PWM} = I_{OUTx} \times D_{PWMx} \qquad (21)$$

Where, $DEFPWM_X$ is duty cycle of each channel independently programmed by PWM Registers (B5h~BAh),

In 4bit PWM mode:

$$D_{PWMx} = \frac{\sum_{n=0}^{3} D[n] \cdot 2^n}{16} \qquad (22)$$

10.2.34 BBh ECC_A Register

ADDR	REG NAME	D7:D0	DEFAULT
BBh	ECC_A	ECCA	0b 00000000

Data check byte 0xB0~0xBA.

10.2.35 BCh Write Protect area A Register

ADDR	REG NAME	D7:D0	DEFAULT
BCh	W_PROTECT_A	WPROTECTA	0b 00000000

OTP-A data protect byte, it must be written 0xFF.

10.2.36 FCh OTP Write Unlock Register

ADDR	REG NAME	D7:D0	DEFAULT
FCh	OTP_UNLOCK	OTPUNLOCK	0b 00000000

OTP register unlock byte, unlock OTP registers (B0h~BCh)

Write 0xA5->0x69 unlock OTPA

Other lock OTPA mode.

11 CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

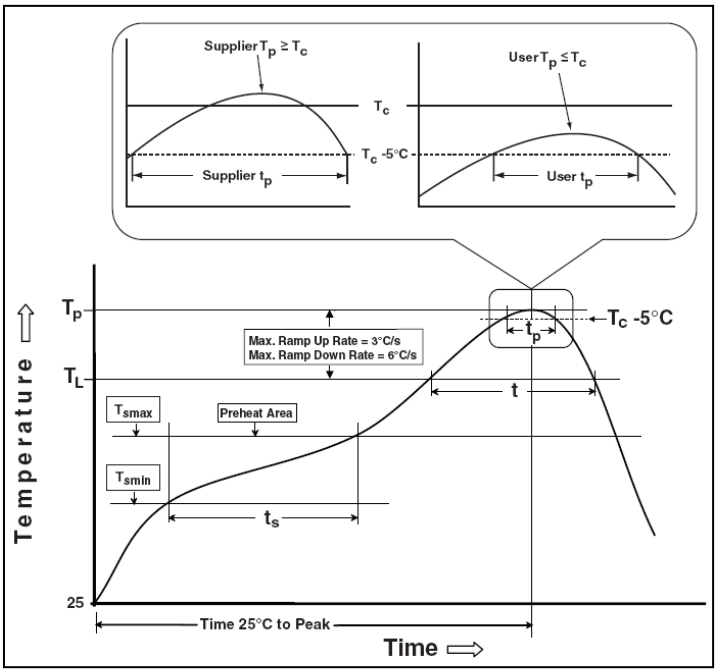
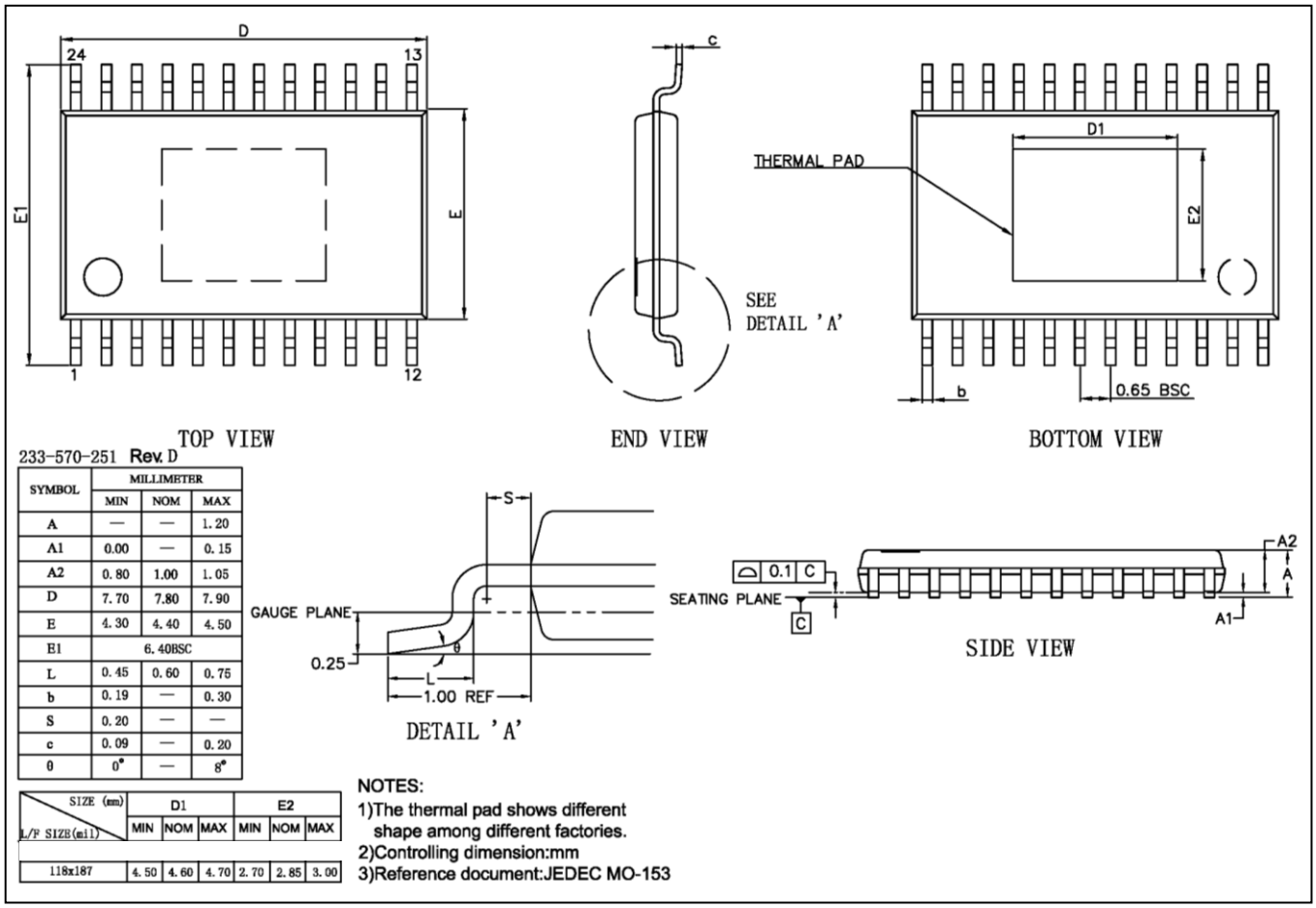


Figure 22 Classification Profile

12 PACKAGE INFORMATION

eTSSOP-24

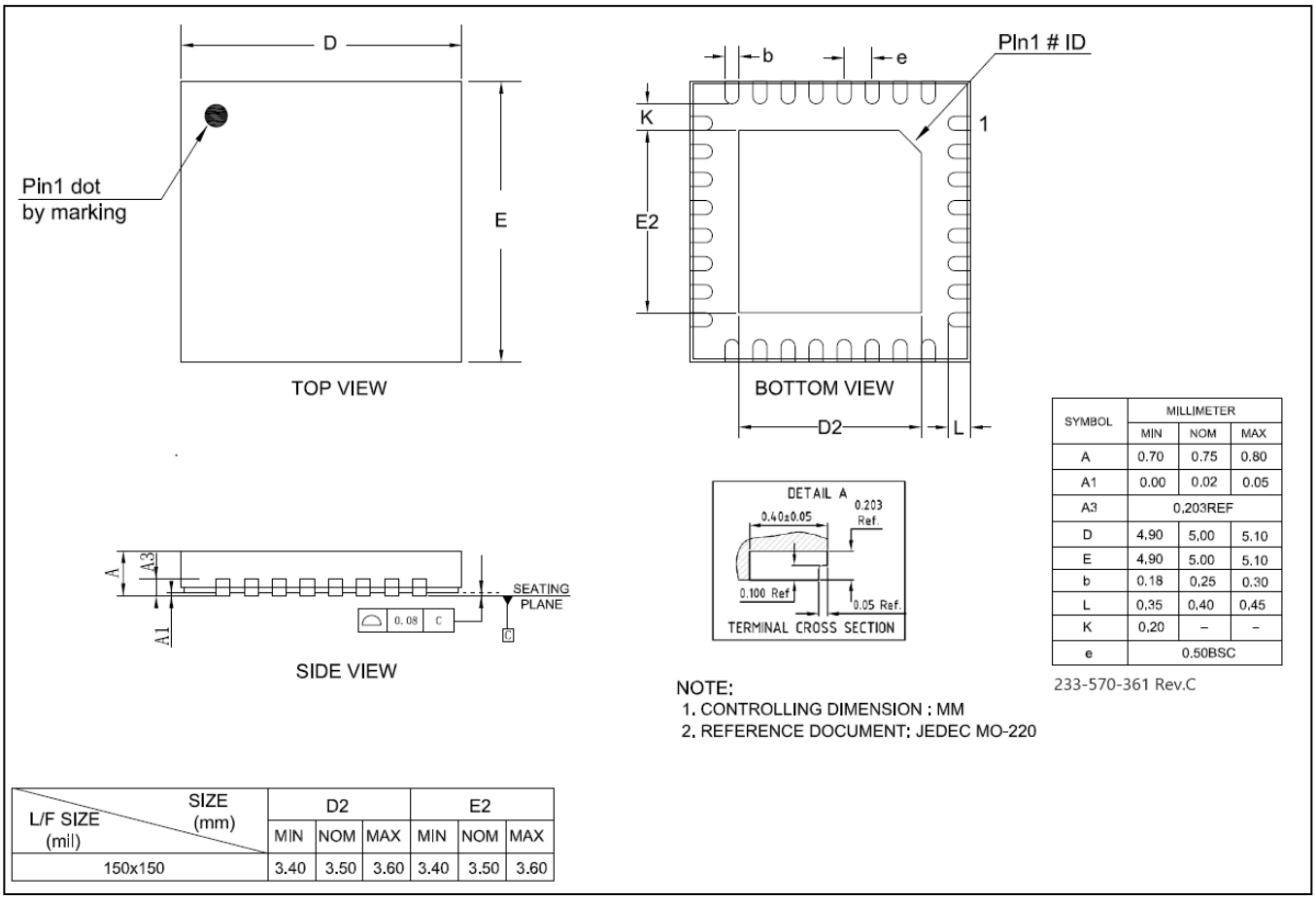


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	1.00	1.05
D	7.70	7.80	7.90
E	4.30	4.40	4.50
E1	6.40BSC		
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20	—	—
c	0.09	—	0.20
θ	0°	—	8°

SIZE (mm) / L/F SIZE(mil)	D1			E2		
	MIN	NOM	MAX	MIN	NOM	MAX
118x187	4.50	4.60	4.70	2.70	2.85	3.00

NOTES:
1)The thermal pad shows different shape among different factories.
2)Controlling dimension:mm
3)Reference document:JEDEC MO-153

WFQFN-32



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203REF		
D	4.90	5.00	5.10
E	4.90	5.00	5.10
b	0.18	0.25	0.30
L	0.35	0.40	0.45
K	0.20	–	–
e	0.50BSC		

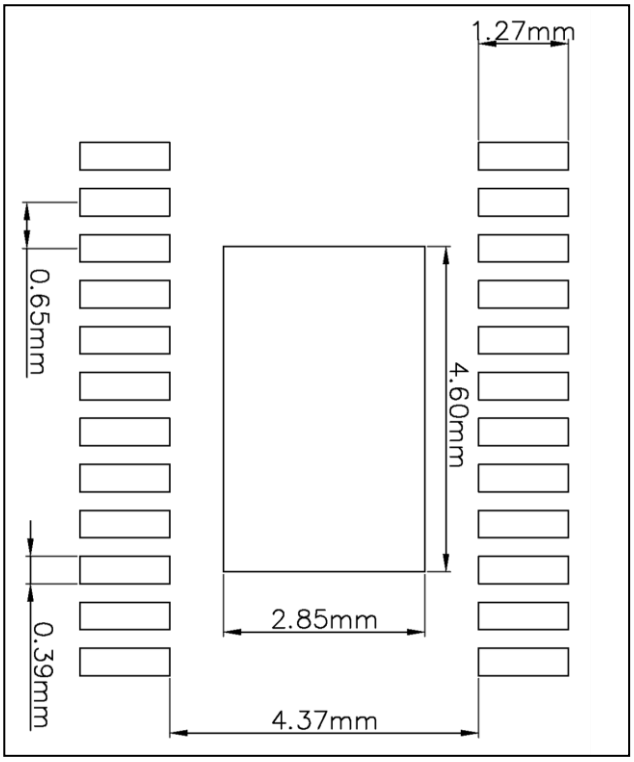
233-570-361 Rev.C

NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220

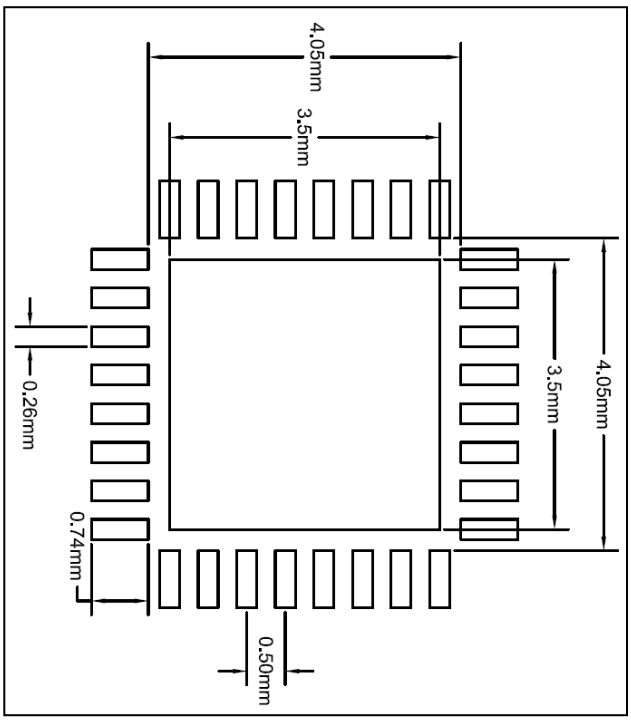
L/F SIZE (mil) \ SIZE (mm)	D2			E2		
	MIN	NOM	MAX	MIN	NOM	MAX
150x150	3.40	3.50	3.60	3.40	3.50	3.60

13 RECOMMENDED LAND PATTERN

eTSSOP-24



WFQFN-32



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

14 REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2024.06.05
0B	1. Update ESD data 2. Update the functional block diagram	2024.07.15
0C	1. Update figure 7 RFSMD 68kΩ to 75kΩ 2. Update ACK function (when FAULTB pull down return 0x7E) 3. Add detailed description of FAULT protection 4. Complete communication protocol 5. Update some description errors	2024.10.15
A	Release to final version	2025.06.25
B	1. Update the “FAIL-SAFE STATE” error describe 2. Update the “Fault Action Table” error describe 3. Delete ADC current detection formula 4. 59h register TDT2CLR changed to WDT2CLR 5. Update the “One Fail all On” to “One Fail Others On” 6. Update R_{JP} to R_{JC_BOT} 7. Update POD	2025.08.01