

IS31SE5117B

16-CH PROGRAMMABLE CAPACITIVE TOUCH SENSOR

GENERAL DESCRIPTION

IS31SE5117B is an ultra-low-power, 16-channel capacitive touch controller. The controller allows sleep mode (under 10uA) and uses auto-detection for wakeup. It also provides a shield output to increase moisture immunity. The built-in hardware monitor and calibration for the environment is to prevent false triggers.

A host MCU is required to communicate with IS31SE5117B. An on-chip I²C slave controller with 400kHz capability serves as the communication port for the host MCU. An interrupt, INT, can be configured and it is generated when a touch trigger event occurs. Trigger conditions can be configured by setting the interrupt register. IS31SE5117B can support proximity sensing.

IS31SE5117B is available in the QFN-24 package. It operates from 2.7V to 5.5V over the temperature range from -40°C to +105°C.

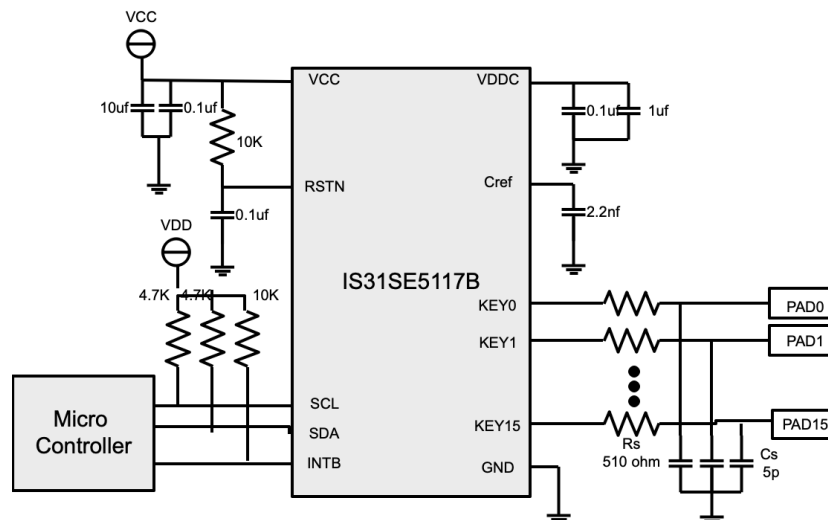
APPLICATIONS

- Touch keys for home appliances
- Touch keys for industrial control

FEATURES

- 16-channel capacitive touch controller with readable key value
- Touch threshold setting for individual key
- Optional multiple-key function
- GPIO toggle/invert function
- Automatic calibration
- Individual key calibration
- Interrupt output with auto-clear and repeating
- Auto sleep mode for extremely low power
- Keys wake up from sleep mode
- Shield output shared with touch key channels
- Buzzer/Melody Generator shared with touch key channels
- 400kHz fast-mode I²C interface
- Operating temperature between -40°C ~ +105°C
- QFN-24
- ROHS & Halogen-Free compliant package
- TSCA compliance

TYPICAL APPLICATION CIRCUIT (QFN-24)



Note 1: The IC should be placed far away from the noise source to prevent EMS.

Note 2: The RS and CS should be placed as close to the IC as possible to reduce EMI.

Note 3: The AD pin can be configured as KEY15.

Note 4: The capacitors connected to VDD and VDDC should be as close to the IC as possible to reduce EMI.

Note 5: The capacitor 1uF connected to VDDC might need to be removed for quick VDD rising time application.

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PINOUT

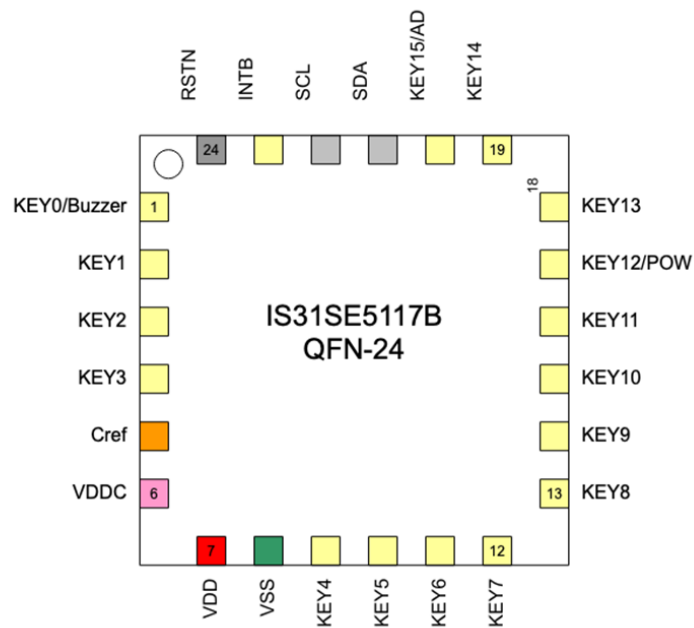


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1. Pin Description

No.	Pin	Description
1	KEY0/Buzzer	Multiple function key. Can be configured to input sense channel 0, or Buzzer output.
2 - 4	KEY1 – KEY3	Input sense channel 1 – 3
5	Cref	External reference Capacitor for touch sense
6	VDDC	Internal 1.5V power supply. Typical decoupling capacitors of 0.1μF and 1μF should be connected. between VDDC and GND.
7	VDD	Power supply
8	VSS	Ground
9 – 16	KEY4 – KEY11	Input sense channel 4 - 11
17	KEY12/POW	Multiple function key. Can be configured to input sense channel 12, or Melody power control.
18 – 19	KEY13 – KEY14	Input sense channel 13 - 14
20	AD/KEY15	Multiple function key. Can be configured to I ² C address or input sense channel 15.
21	SDA	I ² C serial data
22	SCL	I ² C serial clock
23	INTB	Interrupt output (active low)
24	RSTN	Reset Low Active

Table 1-1 PIN Description

IS31SE5117B

2. Ordering Information

Industrial Range: -40°C to +105°C

Order Part No.	Package	QTY
IS31SE5117B-QFLS3-TR	QFN-24, Lead-free	2500/Reel

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- a.) the risk of injury or damage has been minimized;
- b.) the user assumes all such risks; and
- c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances.

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3. Absolute Maximum Ratings

Supply voltage, VDD	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ VDD+0.3V
Maximum junction temperature, TJMAX	+150°C
Storage temperature range, TSTG	-65°C ~ +150°C
Operating temperature range TA	-40°C ~ +105°C
Junction Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA} (QFN-24)	29°C/W
ESD (HBM) ESD (CDM)	± 2 kV ± 750 V

Table 3-1 Absolute maximum ratings

Note 6: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.1 Electrical Characteristics

TA = 25°C, VDD = 2.7V ~ 5.5V, unless otherwise noted. Typical values are TA = 25°C, VDD = 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage		2.7		5.5	V
IDD	IDD core current per frequency	VDD = 5.5V		150		μ A/Mhz
IDD sleep	IDD, sleep mode, 25°C	VDD = 5.5V		4		μ A
ΔC_S	Minimum detectable capacitance	CS = 5pF (Note 7)		0.2		pF
Logic Electrical Characteristics						
VIL	Logic “0” input voltage	VDD = 2.7V			0.4	V
VIH	Logic “1” input voltage	VDD = 5.5V	1.4			V
IIL	Logic “0” input current	VINPUT = 0V (Note 7)		5		nA
IIH	Logic “1” input current	VINPUT = VDD (Note 7)		5		nA

3.2 Digital Input Switching Characteristics (Note 7)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
fSCL	Serial-Clock frequency				400	kHz
tBUF	Bus free time between a STOP and a START condition		1.3			μ s
tHD, STA	Hold time (repeated) START condition		0.6			μ s
tSU, STA	Repeated START condition setup time		0.6			μ s
tSU, STO	STOP condition setup time		0.6			μ s
tHD, DAT	Data hold time				0.9	μ s
tSU, DAT	Data setup time		100			ns
tLOW	SCL clock low period		1.3			μ s
tHIGH	SCL clock high period		0.7			μ s
tR	Rise time of both SDA and SCL signals.	(Note 8)		20+0.1Cb	300	ns
tF	Fall time of both SDA and SCL signals.	(Note 8)		20+0.1Cb	300	ns

Note 7: Guaranteed by design.

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Note 8: C_b = total capacitance of one bus line in pF. $I_{SINK} \leq 6\text{mA}$. t_R and t_F measured between $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.

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4. Function Block Diagram

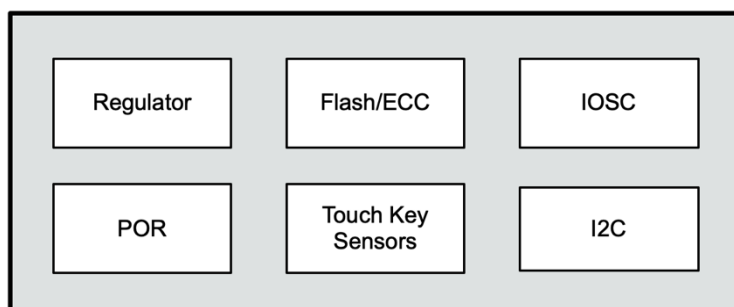


Figure 4-1 Function Block Diagram

4.1 Basic introduction for touch sense data process flow

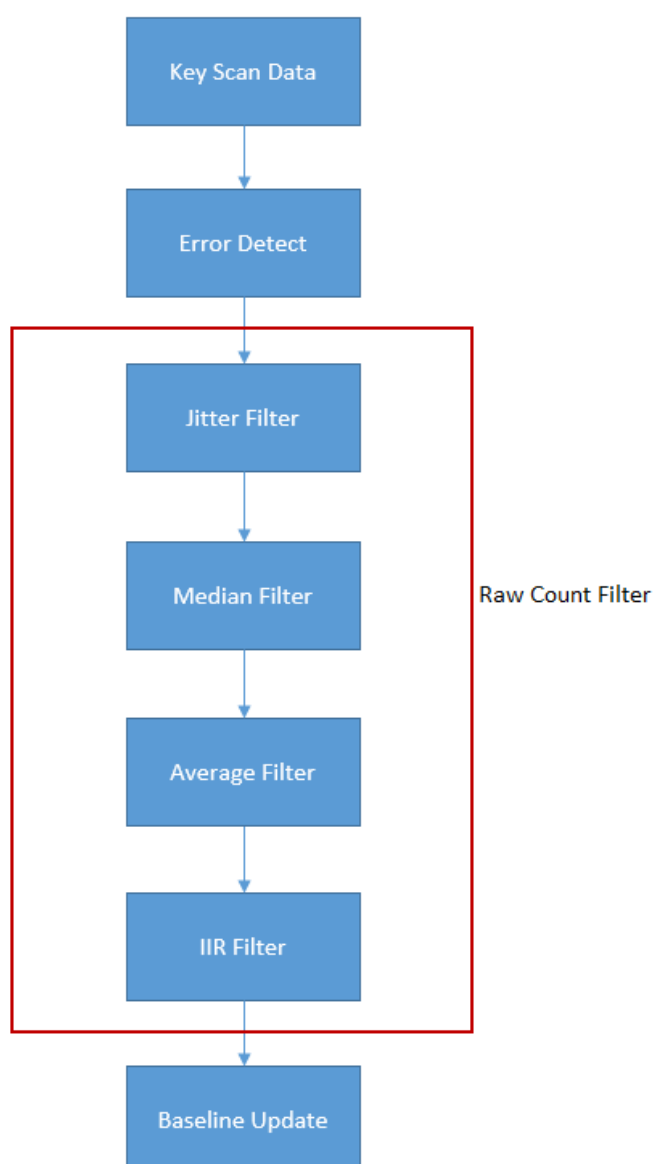


Figure 4-2 Touch Sense Data Process Flow

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4.2 Baseline process based on difference of baseline and raw count

Baseline will be updated to the current raw count based on the below factors. For detailed information about baseline, please refer to Section 4.4.2 Key parameter in “IS31SE5117B Eval Board User's Manual with Safety Self-Test” application note.

4.2.1 Positive noise threshold

Baseline is updated if the difference count of baseline count and raw count is below the positive noise threshold.

4.2.2 Negative noise threshold

It is used with the low baseline reset count to reset baseline count to the current raw count. Please refer to the description of **Low baseline reset**.

4.2.3 Low baseline reset

Low baseline reset count of each key. A reset count increases one if the absolute $|\text{raw count} - \text{baseline}| > \text{negative noise threshold}$. Once the reset count exceeds the low baseline reset register value, the baseline is reset to the current raw count. The reset count will be reset to 0 if the absolute $|\text{raw count} - \text{baseline}| \leq \text{negative noise threshold}$.

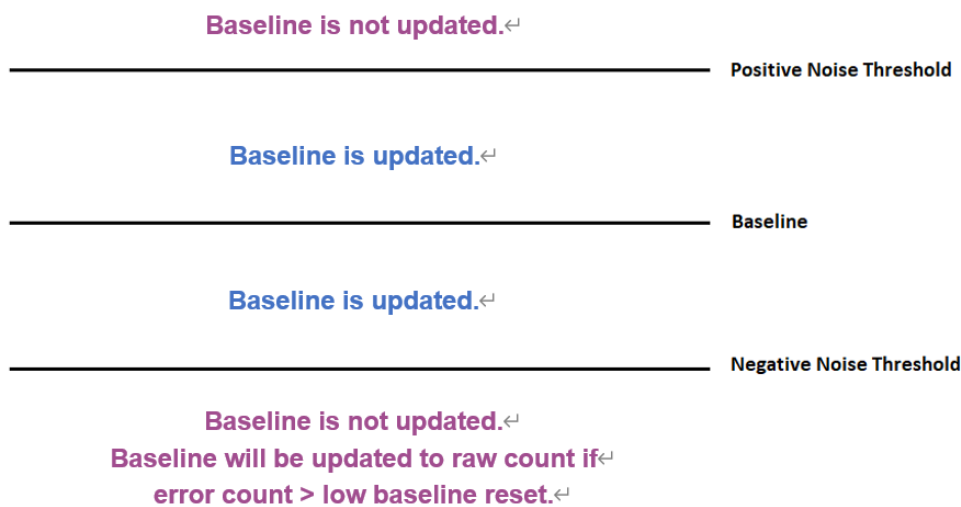


Figure 4-3 Baseline Process based on difference of baseline and raw count

4.2.4 Touch sense data identification

Ignore touch key scan if the signal exceeds the lock threshold.

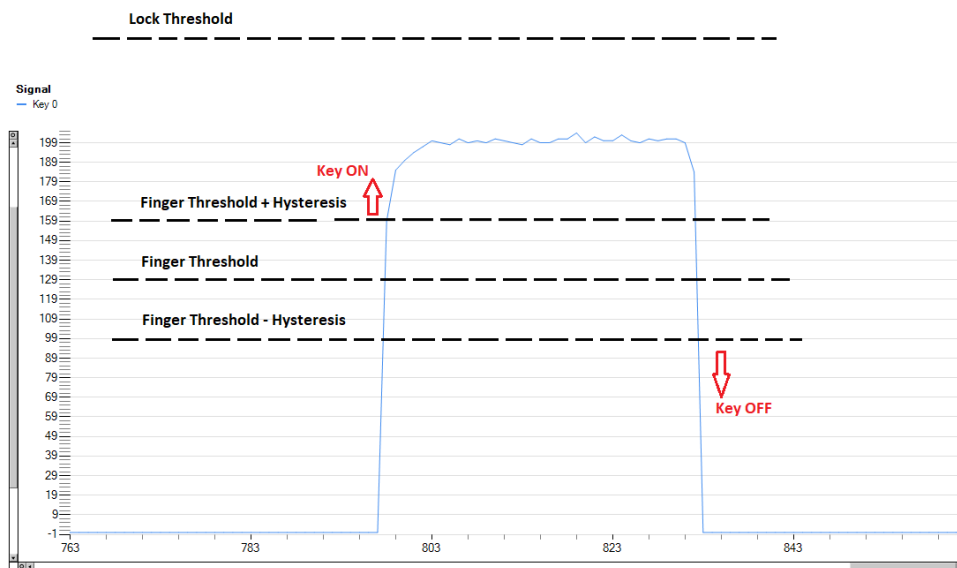


Figure 4-4 Touch Sense Data Identification

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5. Detailed Description

5.1 I²C Interface

The IS31SE5117B uses a serial bus, which conforms to the I²C protocol, to control the chip's functions with two wires: SCL and SDA. IS31SE5117B has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 "0" for a write command and set A0 "1" for a read command. The value of bits A1 and A2 are determined by the connection of the AD pin, to GND, VDD, or Floating.

The complete slave address is:

Bit	A7:A3	A2:A1	A0
Value	01111	AD	1/0

AD floating, AD = 00;

AD connected to GND, AD = 01;

AD connected to VDD, AD = 10;

AD pin can also be configured as a Touch Key channel. When AD pin is used for a Touch Key channel, A2: A1 = 00.

The SCL line is uni-directional. The SDA line is bi-directional (open collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I²C standard is 400kHz. During communication, the microcontroller is the master and IS31SE5117B is the slave.

The timing diagram for the I²C is shown in Figure 5-1. The SDA is latched on to the stable high level of the SCL. When there is no bus activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I²C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, and the most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for IS31SE5117B acknowledgement. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If IS31SE5117B has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31SE5117B, the register address byte is sent, and the most significant bit first. IS31SE5117B must generate another acknowledgment indicating that the register address has been received.

Then 8-bit of data bytes are sent next, the most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, IS31SE5117B must generate another acknowledgment to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

5.2 Reading Port Registers

To read the device data, the bus master must first send the address of IS31SE5117B with the R/W bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must send IS31SE5117B address with the R/W bit set to "1". Data from the register defined by the command byte is sent from IS31SE5117B to the master (Figure 5-4).

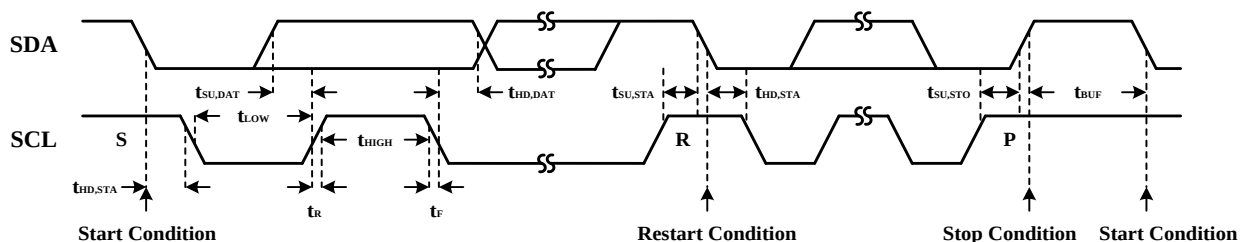


Figure 5-1 Interface Timing

IS31SE5117B

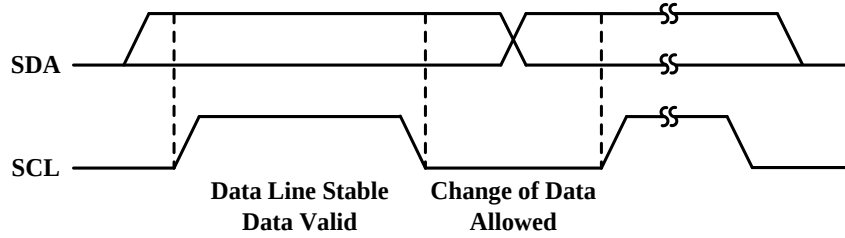


Figure 5-2 Bit Transfer

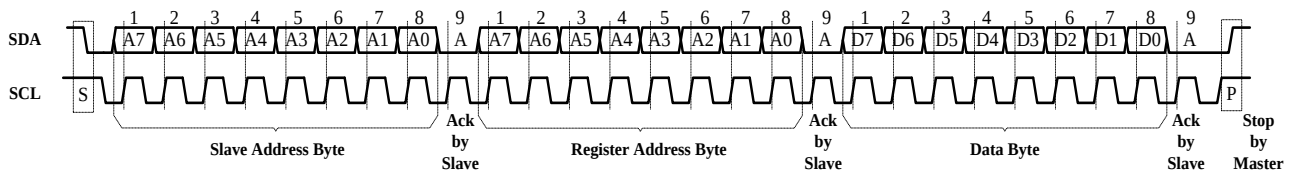


Figure 5-3 Writing to IS31SE5117B

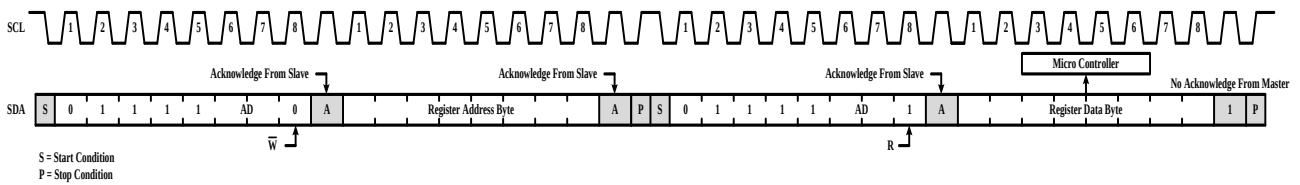


Figure 5-4 Reading from IS31SE5117B

Note: Successive read or write protocol is supported.

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6. Register Definition

6.1 Page 0 Register list

Address	Name	Definition	R/W	Default
00h	Chip Part Number	Chip's part number	R	17h
01h-02h	Chip Version	Chip's version	R	-
03h	Firmware Version	Firmware version	R	60h
04h	Run Version	Run version	R/W	60h
05h	Main Control	System reset, power saving, and parameters management	W	00h
06h	Switch Page	Switch for Page 0 and Page 1	R/W	00h
07h-08h	Key Status	Key 0-Key 15 status bits	R	00h
09h	BM	Buzzer data or stop command	W	-
09h	BM	Available buzzer buffer size	R	0Ah
0Ah-19h	Key Signal	Key 0-Key 15 signal value	R	00h
1Ah-39h	Key Raw Count	Key 0-Key 15 raw count value	R	00h
3Ah-59h	Key Baseline	Key 0-Key 15 baseline value	R	00h
5Ah	Raw Count Filter	Raw count filter setting	R/W	00h
5Bh	Baseline IIR Ratio	Baseline IIR ratio setting	R/W	01h
5Ch-5Dh	Lock Threshold	Lock threshold setting	R/W	03E8h
5Eh	Lock Scan Cycle	Lock scan cycle setting	R/W	08h
5Fh	Raw Count Difference Limit	Raw count difference limit setting	R/W	64h
60h	Multi Touch Key Configure	Multiple touch key function setting	R/W	03h
61h	Max Duration Time	Maximum duration time setting	R/W	1Ah
62h	Interrupt Configuration	Interrupt configuration	R/W	0Ah
63h	Interrupt Repeat Time	Repeat cycle for pressing key interrupt setting	R/W	00h
64h	Key Pin Select	Select pins as Key0-Key7	R/W	00h
65h	Key Pin Select	Select pins as Key8-Key15	R/W	00h
66h-67h	Shield Pin Select	Select pin as shield	R/W	0040h
68h-69h	INT Pin Select	Select pin as INT	R/W	0000h
6Ah-6Bh	Buzzer Pin Select	Select pin as buzzer	R/W	0100h
6Ch-6Dh	POW Pin Select	Select pin as buzzer power	R/W	0000h
6Eh	GPIO Pin Select	Select pin as GPIO0-GPIO7	R/W	0Eh
6Fh	GPIO Pin Select	Select pin as GPIO8-GPIO15	R/W	00h
70h-71h	Slider 1 Key Select	Select Key as slider 1, max 8 keys	R/W	003Fh
72h-73h	Slider 2 Key Select	Select Key as slider 2, max 8 keys	R/W	0000h
74h	TKIII Control register 1	Repeat sequence, initial setting delay, auto mode start delay, and low-frequency noise filter	R/W	13h
75h	TKIII Control register 2	Pseudo random sequence setting	R/W	20h
76h	TKIII Control register 3	Multi frequency scan/cycle count setting	R/W	03h
77h	TKIII CCHG and CSEN	Internal charge capacitance setting	R/W	00h
78h	TKIII PUD	Pull-up current/ pull-up resistors setting	R/W	00h
79h	System Clock Select	System clock setting	R/W	01h

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Address	Name	Definition	R/W	Default
7Ah	Spread Spectrum	Spread spectrum setting	R/W	0Ch
7Bh	Auto Sleep Mode	Auto-enter sleep mode time setting	R/W	0Fh
7Ch	Sleep Mode Control	Sleep mode control setting	R/W	00h
7Dh-7Eh	Wake Up Key Select	Select Key0~Key15 to exit sleep mode	R/W	0000h
7Fh	Wake Up Threshold	Wake up threshold setting	R/W	08h
80h	TKIII Sleep Mode CCHG and CSEN	Sleep mode internal charge capacitance setting	R/W	00h
81h	TKIII Sleep Mode PUD	Sleep mode pull-up current/ pull-up resistors setting	R/W	00h
82h-83h	SLP_RAW	Sleep mode raw count value	R	0000h
84h-85h	SLP_Baseline	Sleep mode baseline value	R	0000h
86h-8Bh	Slider 1-2 status	3 slider status registers for each slider	R/W	Addr. 88h Value 80h, others Value 00h
8Ch	Slider 1 Mapping	Slider 1 Key 1 position	R/W	08h
8Dh	Slider 1 Mapping	Slider 1 Key 2 position	R/W	09h
8Eh	Slider 1 Mapping	Slider 1 Key 3 position	R/W	0Ah
8Fh	Slider 1 Mapping	Slider 1 Key 4 position	R/W	0Bh
90h	Slider 1 Mapping	Slider 1 Key 5 position	R/W	0Ch
91h	Slider 1 Mapping	Slider 1 Key 6 position	R/W	0Dh
92h	Slider 1 Mapping	Slider 1 Key 7 position	R/W	00h
93h	Slider 1 Mapping	Slider 1 Key 8 position	R/W	00h
94h-9Bh	Slider 2 Mapping	Slider 2 Key 1 – 8 positions	R/W	00h
9Ch	Self-Test Item	Safety function self-test item	R/W	00h
9Dh-9Eh	Self-Test Ram Start Addr	Safety function self-test ram start address	R/W	00h
9Fh-A0h	Self-Test Ram Size	Safety function ram size	R/W	00h
A1h	Self-Test Result	Safety function self-test test result	R	00h
A2h	Reference Voltage Selection	Comparator Reference Select	R/W	00h
A3h	TKIII Sleep Mode Reference Voltage Selection	Sleep Mode Comparator Reference Select	R/W	00h
A4h-FFh	Reserved	Reserved	-	-

Table 6-1 Page 0 Register list

6.2 Page 1 Register list (extension memory)

Address	Name	Definition	R/W	Default
0100h	Chip Part Number	Chip's part number	R	17h
0101h-0102h	Chip Version	Chip's version	R	-
0103h	Firmware Version	Firmware version	R	60h
0104h	Run Version	Run version	R/W	60h

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Address	Name	Definition	R/W	Default
0105h	Main Control	System reset, power saving, and parameters management	W	00h
0106h	Switch Page	Switch for Page 0 and Page 1	R/W	00h
0107h-0108h	Key Status	Key 0-Key 15 status bits	R	00h
0109h	BM	Buzzer data or stop command	W	-
0109h	BM	Available buzzer buffer size	R	0Ah
010Ah-0119h	Key Finger Threshold	Key 0-Key 15 finger threshold setting	R/W	50h or 28h
011Ah-0129h	Key Noise Threshold	Key 0-Key 15 noise threshold setting	R/W	28h or 14h
012Ah-0139h	Key Negative Noise Threshold	Key 0-Key 15 negative noise threshold setting	R/W	28h or 14h
013Ah-0149h	Key Low Baseline Reset	Key 0-Key 15 low baseline reset setting	R/W	1Eh
014Ah-0159h	Key Hysteresis	Key 0-Key 15 hysteresis setting	R/W	08h or 04h
015Ah-0169h	Key ON Debounce	Key 0-Key 15 debounce setting	R/W	03h
016Ah-016Bh	Key Interrupt Enable	Key 0-Key 15 enables Interrupts associated with capacitive touch sensor inputs	R/W	00h
016Ch	GPIO Value 1	Default GPIO values for GPIO0 – GPIO7	R/W	0Eh
016Dh	GPIO Value 2	Default GPIO values for GPIO8 – GPIO15	R/W	00h
016Eh	GPIO Enable 1	Enable KEY0- KEY7 to do GPIO mapping	R/W	70h
016Fh	GPIO Enable 2	Enable KEY8- KEY15 to do GPIO mapping	R/W	00h
0170h	GPIO Mapping 1	Key to GPIO mapping	R/W	00h
0171h	GPIO Mapping 2	Key to GPIO mapping	R/W	00h
0172h	GPIO Mapping 3	Key to GPIO mapping	R/W	12h
0173h	GPIO Mapping 4	Key to GPIO mapping	R/W	03h
0174h-0177h	GPIO Mapping 5-8	Key to GPIO mapping	R/W	00h
0178h	GPIO Toggle EN 1	Enable GPIO Toggle mode for KEY0 – KEY7	R/W	10h
0179h	GPIO Toggle EN 2	Enable GPIO Toggle mode for KEY8 – KEY15	R/W	00h
017Ah	Key Scan Once	I ² C control key scan	R/W	00h
017Bh	Table Ready Mark	Mark for flash data ready	R	00h

Table 6-2 Page 1 Register list (extension memory)

6.3 Page 0 Registers

00h Chip Part Number Register (RO)

Bit	D7:D0
Name	CPN[7:0]
Default	0001 0111

CPN

Chip Part Number

Chip's part number 17h

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01h Chip Version Register 1 (RO)

Bit	D7:D0
Name	CV1[7:0]
Default	-

CV1 Chip Version information 1

02h Chip Version Register 2 (RO)

Bit	D7:D0
Name	CV2[7:0]
Default	-

CV2 Chip Version information 2
CV1 & CV2 bytes contain chip revision. CV1 indicates mask set version. CV2 indicates minor version.

03h Firmware Version Register (RO)

Bit	D7:D0
Name	FV1[2:0] FV2[2:0] FV3[1:0]
Default	011 000 00

FV Firmware Version
Default version is 3.0.0
FV1[2:0] Major version
FV2[2:0] Minor version
FV3[1:0] Patch version

04h Run Version Register (RW)

Bit	D7:D0
Name	RV1[2:0] RV2[2:0] RV3[1:0]
Default	011 000 00

RV Run Version
Set run firmware version and the default value equals to the default value of the firmware version register.
RV1[2:0] Major version
RV2[2:0] Minor version
RV3[1:0] Patch version

05h Main Control Register (WO)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR	RD	-	SP	SS	DW	DS	-
Default	0	0	0	0	0	0	0	0

SR System Reset
1 System reset
RD Reset All Parameters to Manufacturer Default Setting.
1 Reset all user-defined parameters to manufacture default setting.
SP Sleep Mode
1 Sleep mode
SS Save User-Defined Parameters
1 Save current parameters into flash.
DW Deep Sleep Wake Up Reset Baseline
1 Reset touch key baseline after waking up from deep sleep mode.
DS Deep Sleep Mode
1 Keep sleep until waking up by I²C SDA falling edge.

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06h Switch Page (RW)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	FLAG
Default	0	0	0	0	0	0	0	0

FLAG=0 Page 0 (Address: 0x00~0xFF)

FLAG=1 Page 1 (Address: 0x100~0x1FF)

07h Key Status Register 1 (RO)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

KSx

Key0~Key7 Status

If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".

0 Not detected.

1 Key is detected.

08h Key Status Register 2 (RO)

Bit	D7:D0
Name	KS[15:8]
Default	0000 0000

KSx

Key8~Key15 Status

If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".

0 Not detected.

1 Key is detected.

09h Buzzer Register (W)

Bit	D7:D0
Name	BM[7:0]
Default	-

BM

Buzzer Register Write

Buzzer data or stop command

09h Buzzer Register (R)

Bit	D7:D0
Name	BM[7:0]
Default	0000 1010

BM

Buzzer Register Read

It shows the available tone buffer size. IS31SE5117B has 10 built-in note buffers.

0Ah~19h KEY0~KEY15 Signal Register (RO)

Bit	D7:D0
Name	KEYx_SIGNAL[7:0]
Default	0000 0000

KEYx_SIGNAL

Key Signal Count

The difference between baseline and raw count.

The maximum value is 254. It will keep 254 if the value is over 254. Value 255 means noise existence.

1Ah, 1Ch..., 36h, 38h KEY0~KEY15 Raw Count High Byte Register (RO)

Bit	D7:D0
Name	KEYx_RAWCOUNT[15:8]
Default	0000 0000

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1Bh, 1Dh..., 37h, 39h KEY0~KEY15 Raw Count Low Byte Register (RO)

Bit	D7:D0
Name	KEYx_RAWCOUNT[7:0]
Default	0000 0000

KEYx_RAWCOUNT Raw count of each key provides an indication of the magnitude of the sensor's capacitance.

3Ah, 3Ch ..., 56h, 58h KEY0~KEY15 Baseline High Byte Register (RO)

Bit	D7:D0
Name	KEYx_BASELINE[15:8]
Default	0000 0000

3Bh, 3Dh ..., 57h, 59h KEY0~KEY15 Baseline Low Byte Register (RO)

Bit	D7:D0
Name	KEYx_BASELINE[7:0]
Default	0000 0000

KEYx_Baseline Baseline of each key

5Ah Raw Count Filter Register (RW)

Bit	D7	D6	D5:D4	D3	D2:D1	D0
Name	MF	AF	IIR[1:0]	JF	JD[1:0]	-
Default	0	0	00	0	00	0

MF Median Filter
0 Disable
1 Enable

AF Average Filter
0 Disable
1 Enable

IIR IIR Filter
00 Disable
01 1/2
10 1/4
11 1/8

JF Jitter Filter
0 Disable
1 Enable

JD Jitter Delta
00 1
01 2
10 4
11 8

5Bh Baseline IIR Ratio Register (RW)

Bit	D7:D0
Name	RATIO[7:0]
Default	0000 0001

RATIO Range 1 ~ 255

5Ch Lock Threshold High Byte Register (RW)

Bit	D7:D0
Name	LT[15:8]
Default	0000 0011

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5Dh Lock Threshold Low Byte Register (RW)

Bit	D7:D0
Name	LT[7:0]
Default	1110 1000

LT Lock Threshold

5Eh Lock Scan Cycle Register (RW)

Bit	D7:D0
Name	LSC[7:0]
Default	0000 1000

LSC Lock Scan Cycle
Ignore the key scan data for the setting Lock scan cycle if the |raw count – baseline| > Lock threshold.

5Fh Raw Count Difference Limit Register (RW)

Bit	D7:D0
Name	RCDL[7:0]
Default	0110 0100

RCDL Raw Count Difference Limit
Ignore the key scan data if the difference between previous raw count and current raw count exceeds the limit.

60h Multiple Touch Key Configure Register (RW)

Bit	D7:D2	D1:D0
Name	-	MTK[1:0]
Default	000000	11

MTK Multi Touch Key
00 Allow all keys to be triggered at one time.
01 Allow one key to be triggered at one time.
10 Allow two keys to be triggered at one time.
11 Allow three keys to be triggered at one time.

61h Max Duration Time Register (RW)

Bit	D7	D6	D5	D4	D3:D0
Name	-	-	-	MDEN	MDT[3:0]
Default	0	0	0	1	1010

MDEN Maximum Duration Time Enable
0 Disable
1 Enable

MDT Maximum Duration Time
0000 0.5s
0001 1s
0010 2s
0011 3s
0100 4s
0101 5s
0110 6s
0111 7s
1000 8s
1001 9s
1010 10s
1011 11s
1100 12s

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1101 13s
1110 14s
1111 15s

MDT bits set the pressed time. When key pressed duration exceeds the programmed time (MDT), device will be forced to calibrate the pressed key. Set MDEN to “1” will enable this function.

62h Interrupt Configuration Register (RW)

Bit	D7	D6:D4	D3	D2:D0
Name	INE	-	ACEN	ACT[2:0]
Default	0	000	1	010

INE Interrupt Function Enable
0 Disable
1 Enable

ACEN Auto-Clear Interrupt Enable
0 Disable
1 Enable

ACT Auto-Clear Interrupt Time
000 10ms
001 20ms
010 30ms
011 40ms
100 50ms
101 100ms
110 150ms
111 200ms

When ACEN=0, the INT will keep low until device 07h and 08h registers are read, or the key is released. When ACEN=1, the INT will be released after ACT setting time is expired even 07h and 08h registers are not read, or key is still pressed.

63h Interrupt Repeat Time Register (RW)

Bit	D7:D4	D3:D0
Name	-	INTRT[3:0]
Default	0000	0000

INTRT Interrupt Repeat Time
0000 disable
0001 50ms
0010 100ms
0011 150ms
0100 200ms
0101 250ms
0110 300ms
0111 350ms
1000 400ms
1001 450ms
1010 500ms
1011 600ms
1100 700ms
1101 800ms
1110 900ms
1111 1s

After INTRT is set, a second interrupt will be generated after the interrupt repeat time is expired If there is a key keeping pressed.

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64h~65h Key Pin Select Register (RW)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

Bit	D7:D0
Name	KS[15:8]
Default	0000 0000

KS Key Pin Selection Setting
 0 Disable
 1 Enable

66h~67h Shield Pin Select Register (RW)

Bit	D7:D0
Name	SHDE[7:0]
Default	0000 0000

Bit	D7:D0
Name	SHDE[15:8]
Default	0100 0000

SHDE Shield Enable (default for SHDE[14])
 0 Disable shield driver
 1 Enable shield driver

68h~69h INT Pin Select Register (RW)

Bit	D7:D0
Name	IPS1[7:0]
Default	0000 0000

Bit	D7:D0
Name	IPS1[15:8]
Default	0000 0000

IS31SE5117B interrupt Pin has been fixed at Pin 23 INTB and it doesn't work to set INT Pin Select Register C9h and CAh.

6Ah~6Bh Buzzer Pin Select Register 1 (RW)

Bit	D7:D0
Name	BPS1[7:0]
Default	---- --- 1

Bit	D7:D0
Name	BPS2[7:0]
Default	---- ----

BPS1/2 Buzzer output Select 1/2
 Enable BPS1[0] will set Pin1 as Buzzer output pin.

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BPS1[7:1] & BPS2[7:0] unused register bits.

6Ch Enable Buzzer Power Register 1 (RW)

Bit	D7:D0
Name	EBP1 [7:0]
Default	---- ----

6Dh Enable Buzzer Power Register 2 (RW)

Bit	D7:D0
Name	EBP2 [0]
Default	--- 0 ----

EBP1/2

Buzzer Power Select 1/2

EBP1[7:0] unused register bits.

EBP2[4] maps to KEY12, write 1 will enable KEY12 as Buzzer Power. Setting other EBP2 bits doesn't work.

6Eh~6Fh GPIO Pin Select Register (RW)

Bit	D7:D0
Name	GPIO[7:0]
Default	0000 1110

Bit	D7:D0
Name	GPIO[15:8]
Default	0000 0000

70h~71h Slider1 Key Select Register (RW)

Bit	D7:D0
Name	GPIO[7:0]
Default	0000 0000

Bit	D7:D0
Name	GPIO[15:8]
Default	0011 1111

72h~73h Slider2 Key Select Register (RW)

Bit	D7:D0
Name	GPIO[7:0]
Default	0000 0000

Bit	D7:D0
Name	GPIO[15:8]
Default	0000 0000

74h TKIII Control Register 1 (RW)

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	RPT	INI	ASTDLY	LFNF
Default	00	01	00	11

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RPT	Repeat Sequence Count
	00 No repeat
	01 Repeat 4 times
	10 Repeat 8 times
	11 Repeat 16 times
INI	Initial Setting Delay
	INI[1-0] defines the number of TKCLK periods for the initial settling of pin Cref. The delay is (INI[1-0] + 1) * 4 * TKCLK.
ASTDLY	Auto Mode Start Delay
	ASTDLY[1-0] inserts an inter-sequence idle time of (ASTDLY[1-0] + 1) * 256 TKCLK at each sequence start. This delay allows the stabilization time from normal mode to sleep mode.
LFNF	Low-Frequency Noise Filter Setting
	00 Disable LFNE
	If the scan count with noise injection detection is larger than (LFNF [1-0] * 8), the scan result is ignored.

75h TKIII Control Register 2 (RW)

Bit	D7	D6	D5	D4	D3	D2:D1	D0
Name	-	-	PRS	-	-	-	-
Default	0	0	1	0	0	00	0

PRS Pseudo Random Sequence
0 Disable PRS
1 Enable PRS

76h TKIII Control Register 3 (RW)

Bit	D7:D4	D3	D2:D0
Name	-	MFEN	CCNT[2:0]
Default	0000	0	011

MFEN Multi Frequency Scan
0 Disable MF
1 Enable MF

CCNT Cycle Count of Each Conversion Sequence

000	1024
001	2048
010	4096
011	8192
100	12288
101	16384
110	32768
111	65536

77h TKIII CCHG Register (RW)

Bit	D7:D5	D4:D3	D2:D0
Name	CCHG[2:0]	CSEN[1:0]	-
Default	000	00	000

CCHG Internal Reference Capacitance Select
CCHG[0] = 5pf
CCHG[1] = 10pf
CCHG[2] = 20pf
Charge capacitance is used to compensate the parasitic capacitance of the key. The setting can be key-specific and should be set along with DC pull-up and CSEN[1-0] (Sensing Capacitance) to obtain a reasonable duty count in 25% to 80% of full count.

CSEN Sensing Capacitance Setting
 Δ KEY/CSEN is represented in the change of duty count. Therefore, the smaller

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CSEN is the higher the sensitivity of the touch key detection. An intrinsic CSEN of 5pF is always there. CSEN[1-0] adds CSEN to a larger value to reduce the sensitivity in case of a noisy environment.
CSEN[0] adds 5pF.
CSEN[1] adds 10pF.

78h TKIII PUD Register (RW)

Bit	D7	D6	D5:D4	D3:D0
Name	PUDIEN	PUDREN	-	PUD [3:0]
Default	0	00	00	0000

TK3PUD is to configure a constant DC pull-up/pull-down on pin Cref to allow high capacitance touch-key detection. A DC pull-up/pull-down can compensate for the equivalent resistance which is caused by a high capacitance key. Connecting a constant current source or resistor can thus maintain touch key detection sensitivity. In general, we will try to maintain the raw count around half of CCNT for the case without key touched.

For DC current, PUD [3:0] enables 8uA/4uA/2uA/1uA current source. For Resistor, PUD [3:0] enables 5K/10K/20K/40K resistor.

PUDIEN Pull-up/Pull-down DC Current Enable
PUDREN Pull-up/Pull-down DC Resistor Enable
PUD Pull up DC Current
1000 Enable 8uA current source.
0100 Enable 4uA current source.
0010 Enable 2uA current source.
0001 Enable 1uA current source.
PUD Pull up Resistor
1000 Enable 5K resistor source.
0100 Enable 10K resistor source.
0010 Enable 20K resistor source.
0001 Enable 40K resistor source.

79h System Clock Select Register (RW)

Bit	D7:D4	D3	D2:D0
Name	SCS[3:0]	CLKS	TKCS[2:0]
Default	0000	0	001

SCS System Clock Select
0000 16MHz / 1
0001 16MHz / 2
0010 16MHz / 4
0011 16MHz / 6
0100 16MHz / 8
0101 16MHz / 10
0110 16MHz / 12
0111 16MHz / 14
1000 16MHz / 16
1001 16MHz / 32
1010 16MHz / 64
1011 16MHz / 128
1100 16MHz / 256
1101 16MHz / 256
1110 16MHz / 256
1111 16MHz / 256
CLKS Clock Stretching (For I²C)
0 Disable stretching
1 Enable stretching
TKCS Touch Key Clock Select

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000	System Clock / 4
001	System Clock / 8
010	System Clock / 16
011	System Clock / 20
100	System Clock / 24
101	System Clock / 32
110	System Clock / 64
111	64KHz

7Ah Spread Spectrum Register (RW)

Bit	D7:D2			
Name	SSR[3:0]	SSA[1:0]	ASEN	-
Default	0000	11	0	-

SS	Spread Spectrum Setting With spread spectrum technique, electromagnetic energy produced over a particular bandwidth is spread in the frequency domain, and that can reduce EMI. Two parameters are listed as follows:
SSR	Defines the spread spectrum sweep rate. If the SSR[3:0] =0, then spread spectrum is disabled.
SSA	Defines how to adjust the spread spectrum frequency bandwidth. The frequency is adjusted by adding SSA [1:0] range to the actual internal OSC control register. SSA[1:0] = 11 +/- 32 SSA[1:0] = 10 +/- 16 SSA[1:0] = 01 +/- 8 SSA[1:0] = 00 +/- 4
ASEN	Asymmetric Clock Enable ASEN=1 uses asymmetric clock for charge sharing ASEN=0 uses symmetric clock for charge sharing ASEN is only meaningful when SYSCLK is the clock source

7Bh Auto Sleep Mode Register (RW)

Bit	D7	D6	D5:D4	D3:D0
Name	ASEN	-	BLMA[1:0]	AST[3:0]
Default	0	0	00	1111

ASEN	N Auto-SLEEP Enable 0 Disable 1 Enable
BLMA	Baseline moving average Hardware baseline can be generated by slow moving average setting. 00 32 average 01 64 average 10 128 average 11 256 average
AST	Auto Sleep Time 0000 0.5s 0001 1s 0010 1.5s 0011 2s 0100 2.5s 0101 3s 0110 3.5s 0111 4s 1000 4.5s 1001 5s 1010 6s 1011 7s

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1100 8s
1101 9s
1110 10s
1111 11s

7Ch Sleep Mode Control Register (RW)

Bit	D7	D6	D5	D4	D3:D2	D1:D0
Name	-	PW	-	SC	T2[1:0]	T1[1:0]
Default	0	0	0	0	00	00

PW Proximity Wakeup
Disable: wake up>>scan key once>>go to sleep again
Enable: wake up>> generates INT signal (optional) >>go to sleep after Auto Sleep Time is expired if no key is detected.
0 Disable
1 Enable

SC Sleep Calibration
0 Disable
1 Enable

T2 Wake Up Period with Key Disable
Device will be woken up according to the T2 setting by polling the status of Key.
00 50ms
01 100ms
10 200ms
11 300ms

T1 Wake Up Period with Key Enable
Device will be woken up according to the T1 setting to maintain the baseline to prevent the change of environment from stopping Key waking up device.
00 2s
01 4s
10 8s
11 16s

7Dh~7Eh Wake Up Key Select Register (RW)

Bit	D7:D0
Name	WK[7:0]
Default	0000 0000

Bit	D7:D0
Name	WK[15:8]
Default	0000 0000

WK Wakeup Key Select Setting
0 Disable
1 Enable

7Fh Wake Up Threshold Register (RW)

Bit	D7:D0
Name	WTH[7:0]
Default	0000 1000

Wake up threshold range from 0 to 255

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80h TKIII Sleep Mode CCHG Register (RW)

Bit	D7:D5	D4:D3	D2:D0
Name	CCHG[2:0]	CSEN[1:0]	-
Default	000	00	000

CCHG

Internal Reference Capacitance Select

CCHG[0] = 5pf

CCHG[1] = 10pf

CCHG[2] = 20pf

Charge capacitance is used to compensate the parasitic capacitance of the key. The setting can be key-specific and should be set along with DC pull-up and CSEN[1-0] (Sensing Capacitance) to obtain a reasonable duty count in 25% to 80% of full count.

CSEN

Sensing Capacitance Setting

Δ KEY/CSEN is represented in the change of duty count. Therefore, the smaller CSEN is the higher the sensitivity of the touch key detection. An intrinsic CSEN of 5pF is always there. CSEN[1-0] adds CSEN to a larger value to reduce the sensitivity

in case of a noisy environment.

CSEN[0] adds 5pF.

CSEN[1] adds 10pF.

81h TKIII Sleep Mode PUD Register (RW)

Bit	D7	D6	D5:D4	D3:D0
Name	PUDIEN	PUDREN	-	PUD[3:0]
Default	0	0	00	0000

TK3 PUD is to configure a constant DC pull-up/pull-down on pin Cref to allow high capacitance touch-key detection. A DC pull-up/pull-down can compensate for the equivalent resistance caused by a high capacitance key. Connecting a switching current source or resistor can thus maintain touch key detection sensitivity.

For DC current, PUD[3:0] can enable 8uA/4uA/2uA/1uA current source. For Resistor, PUD[3-0] can enable 5K/10K/20K/40K resistor

PUDIEN Pull-up/Pull-down DC Current Enable

PUDREN Pull-up/Pull-down DC Resistor Enable

PUD

Pull up DC Current

1000 Enable 8uA current source.

0100 Enable 4uA current source.

0010 Enable 2uA current source.

0001 Enable 1uA current source.

PUD

Pull up Resistor

1000 Enable 5K resistor source.

0100 Enable 10K resistor source.

0010 Enable 20K resistor source.

0001 Enable 40K resistor source.

82h Sleep Mode Raw Count Register 1 (RO)

Bit	D7:D0
Name	SLRC[15:8]
Default	0000 0000

83h Sleep Mode Raw Count Register 2 (RO)

Bit	D7:D0
Name	SLRC[7:0]
Default	0000 0000

SLRC

Sleep Mode Raw Count

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Read only. Value for reference

84h Sleep Mode Baseline Register 1 (RO)

Bit	D7:D0
Name	SLB[15:8]
Default	0000 0000

85h Sleep Mode Baseline Register 2 (RO)

Bit	D7:D0
Name	SLB[7:0]
Default	0000 0000

SLB
Sleep Mode Baseline
Read only. Value for reference

86h Slider1 Status Register 1 (RO)

Bit	D7	D6:D0
Name	ACT	INIP
Default	0	0000000

ACT
Slider is active
0 Disable slider
1 Enable slider
INIP
Initial position

87h Slider1 Status Register 2 (RO)

Bit	D7	D6:D0
Name	DIR	ENDP
Default	0	0000000

DIR
Direction of Slide1
0 Rotate to left
1 Rotate to right
ENDP
End position of the slider

88h Slider1 Status Register 3 (RW)

Bit	D7	D6:D0
Name	STA	DUR
Default	1	0000000

STA
Status of Slider1
0 Wheel
1 Slider
STA is the only bit for write.
DUR
Duration
The duration between initial position to end position. Every DUR bit increase presents 0.1s.

89h Slider2 Status Register 1 (RO)

Bit	D7	D6:D0
Name	ACT	INIP
Default	0	0000000

ACT
Slider2 is active
0 Disable slider
1 Enable slider
INIP
Initial position

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8Ah Slider2 Status Register 2 (RO)

Bit	D7	D6:D0
Name	DIR	ENDP
Default	0	0000000

DIR Direction of Slide2
 0 Rotate to left
 1 Rotate to right

ENDP End position of the slider

8Bh Slider2 Status Register 3 (RW)

Bit	D7	D6:D0
Name	STA	DUR
Default	0	0000000

STA Status of Slider2
 0 Wheel
 1 Slider

DUR Duration
 The duration between initial position to end position. Every DUR bit increase presents 0.1s.

Qwertyui+8Ch Slider1 Map Register 1 (RW)

Bit	D7:D0
Name	S1K1[7:0]
Default	0000 1000

8Dh Slider1 Map Register 2 (RW)

Bit	D7:D0
Name	S1K2[7:0]
Default	0000 1001

8Eh Slider1 Map Register 3 (RW)

Bit	D7:D0
Name	S1K3[7:0]
Default	0000 1010

8Fh Slider1 Map Register 4 (RW)

Bit	D7:D0
Name	S1K4[7:0]
Default	0000 1011

90h Slider1 Map Register 5 (RW)

Bit	D7:D0
Name	S1K5[7:0]
Default	0000 1100

91h Slider1 Map Register 6 (RW)

Bit	D7:D0
Name	S1K6[7:0]
Default	0000 1101

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92h Slider1 Map Register 7 (RW)

Bit	D7:D0
Name	S1K7[7:0]
Default	0000 0000

93h Slider1 Map Register 8 (RW)

Bit	D7:D0
Name	S1K8[7:0]
Default	0000 0000

S1Kx Slider1 Keyx Map table
 Slider1 KEYx is mapped to Touch Key S1Kx[7:0]

94h-9Bh Slider2 Map Register 1-8 (RW)

Bit	D7:D0
Name	S2Kx[7:0]
Default	0000 0000

S2Kx Slider2 Keyx Map table
 Slider2 KEYx is mapped to Touch Key S2Kx[7:0]

9Ch Self-Test Item Register (RW)

Bit	D7:D0
Name	STI [7:0]
Default	0000 0000

STI Self-Test Item WRITE
 01 CPU
 02 PC
 03 Stack
 04 Flash
 05 SRAM
 06 Clock
 07 INT
 08 Touch Key
 READ 00 Self-Test is completed
 Not 00 Self-Test is busy

9Dh Self-Test Ram Start Address Register 1 (RW)

Bit	D7:D0
Name	STADR[15:8]
Default	0000 0000

9Eh Self-Test Ram Start Address Register 2 (RW)

Bit	D7:D0
Name	STADR [7:0]
Default	0000 0000

STADR Self-Test Ram Start Address

9Fh Self-Test Ram Size Register 1 (RW)

Bit	D7:D0
Name	STRAMSIZE[15:8]
Default	0000 0000

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A0h Self-Test Ram Size Register 2 (RW)

Bit	D7:D0
Name	STRAMSIZE[7:0]
Default	0000 0000

STRAMSIZE Self-Test Ram Size

A1h Self-Test Result Register (RO)

Bit	D7:D0
Name	STR[7:0]
Default	0000 0000

STR Self-Test Result
5Ah Test Result OK
Not 5Ah Error

A2h Comparator Reference Select

Bit	D7	D6	D5	D4	D3:D0
Name	-	CHOPEN	CMPHYS	REFSEL-	-
Default	0-	0	0	0	0000

CHOPEN0 0 Disables comparator offset cancellation.
1 Enables comparator offset cancellation. CHOPEN = 1 can be used to reduce thermal noise impact on measurements taking longer than 10 msec.

CMPHYS 0 Disables the comparator hysteresis.
1 Enables the comparator hysteresis
Hysteresis helps immunity to external EMI disturbance, but it also increases the noise under normal conditions.

REFSEL 0 Use 1/2 VDDC as the reference
1 Use 3/4 VDDC as the reference
When TK3 starts a conversion sequence, CREF is first equalized to REFSEL voltage.
3/4 VDDC has higher EMCI immunity but with less dynamic range.

A3h TKIII Sleep Mode Comparator Reference Select

Bit	D7	D6	D5	D4	D3:D0
Name	-	CHOPEN	CMPHYS	REFSEL-	-
Default	0-	0	0	0	0000

CHOPEN0 0 Disables comparator offset cancellation.
1 Enables comparator offset cancellation. CHOPEN = 1 can be used to reduce thermal noise impact on measurements taking longer than 10 msec.

CMPHYS 0 Disables the comparator hysteresis.
1 Enables the comparator hysteresis
Hysteresis helps immunity to external EMI disturbance, but it also increases the noise under normal conditions.

REFSEL 0 Use 1/2 VDDC as the reference
1 Use 3/4 VDDC as the reference
When TK3 starts a conversion sequence, CREF is first equalized to REFSEL voltage.
3/4 VDDC has higher EMCI immunity but with less dynamic range.

A4h – FFh Reserved

Bit	D7:D0
Name	-
Default	-

Reserved

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6.4 Page 1 Registers (For Expand Memory)

100h Chip Part Number Register (RO)

Bit	D7:D0
Name	CPN[7:0]
Default	0001 0111

CPN Chip Part Number
Chip's part number 17h

101h Chip Version Register 1 (RO)

Bit	D7:D0
Name	CV1[7:0]
Default	-

CV1 Chip Version information 1

102h Chip Version Register 2 (RO)

Bit	D7:D0
Name	CV2[7:0]
Default	-

CV2 Chip Version information 2
CV1 & CV2 bytes contain chip revision. CV1 indicates mask set version. CV2 indicates minor version.

103h Firmware Version Register (RO)

Bit	D7:D0		
Name	FV1[2:0]	FV2[2:0]	FV3[1:0]
Default	011	000	00

FV Firmware Version
Default version is 3.0.0
FV1[2:0] Major version
FV2[2:0] Minor version
FV3[1:0] Patch version

104h Run Version Register (RW)

Bit	D7:D0		
Name	RV1[2:0]	RV2[2:0]	RV3[1:0]
Default	011	000	00

RV Run Version
Set run firmware version and the default value equals to the default value of the firmware version register.
RV1[2:0] Major version
RV2[2:0] Minor version
RV3[1:0] Patch version

105h Main Control Register (WO)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR	RD	-	SP	SS	DW	DS	-
Default	0	0	0	0	0	0	0	0

SR System Reset
1 System reset
RD Reset All Parameters to Manufacturer Default Setting.
1 Reset all user-defined parameters to manufacture default setting.
SP Sleep Mode

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- SS 1 Sleep mode
Save User-Defined Parameters
1 Save current parameters into flash.
- DW Deep Sleep Wake Up Reset Baseline
1 Reset touch key baseline after waking up from deep sleep mode.
- DS Deep Sleep Mode
1 Keep sleep until waking up by I²C SDA falling edge.

106h Switch Page (RW)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	-	-	-	-	-	-	-	FLAG
Default	0	0	0	0	0	0	0	0

FLAG=0 Page 0 (Address: 0x00~0xFF)

FLAG=1 Page 1 (Address: 0x100~0x1FF)

107h~108h Key Status Register 1 (RO)

Bit	D7:D0
Name	KS[7:0]
Default	0000 0000

- KSx Key0~Key7 Status
If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".
0 Not detected.
1 Key is detected.

Key Status Register 2 (RO)

Bit	D7:D0
Name	KS[15:8]
Default	0000 0000

- KSx Key8~Key15 Status
If the key is detected as pressed, the corresponding bit (KSx) will be set to "1".
0 Not detected.
1 Key is detected.

109h Buzzer Register (W)

Bit	D7:D0
Name	BM[7:0]
Default	-

- BM Buzzer Register Write
Buzzer data or stop command

109h Buzzer Register (R)

Bit	D7:D0
Name	BM[7:0]
Default	0000 1010

- BM Buzzer Register Read
It shows the available tone buffer size. IS31SE5117B has 10 built-in note buffers.

10Ah~119h KEY0~KEY15 Finger Threshold Register (RW)

Bit	D7:D0
Name	KEYx_TH[7:0]
Default Key0~Key7	0101 0000
Default Key8~Key15	0010 1000

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KEYx_TH

Finger threshold of each key. It is used with hysteresis to determine the key state.

11Ah~129h KEY0~KEY15 Noise Threshold Register (RW)

Bit	D7:D0
Name	KEYx_NTH[7:0]
Default Key0~Key7	0010 1000
Default Key8~Key15	0001 0100

KEYx_NTH

Noise threshold of each key

Baseline needs to be updated if the difference (baseline and raw count) is less than the noise threshold.

12Ah~139h KEY0~KEY15 Negative Noise Threshold Register (RW)

Bit	D7:D0
Name	KEYx_NNTH[7:0]
Default Key0~Key7	0010 1000
Default Key8~Key15	0001 0100

KEYx_NNTH

Negative noise threshold of each key.

13Ah~149h KEY0~KEY15 Low Baseline Reset Register (RW)

Bit	D7:D0
Name	RCx[7:0]
Default	0001 1110

RCx

Reset Count

Low baseline reset count of each key. A reset count increases one if the absolute $|\text{raw count} - \text{baseline}| > \text{absolute}[\text{negative noise threshold}]$. Once the reset count exceeds the low baseline reset register value, the baseline is reset to the current raw count. The reset count will be reset to 0 if the absolute $|\text{raw count} - \text{baseline}| \leq \text{absolute}[\text{negative noise threshold}]$.

14Ah~159h KEY0~KEY15 Hysteresis Register (RW)

Bit	D7:D0
Name	HYSTERESISx[7:0]
Default Key0~Key7	0000 1000
Default Key8~Key15	0000 0100

HYSTERESISx

Hysteresis of each key

15Ah~169h KEY0~KEY15 On Debounce Register (RW)

Bit	D7:D0
Name	DEBOUNCEx[7:0]
Default	0000 0011

DEBOUNCEx

Debounce number of each key. When the acquired number $>$ debounce setting value, then the key is granted as ON state.

16Ah~16Bh Key Interrupt Enable Register (RW)

Bit	D7:D0
Name	INTEN[7:0]
Default	0000 0000

The Interrupt Enable Register determines whether a key causes the interrupt pin to be asserted when it is detected touched with the key's interrupt enable bit set.

INTEN

Key Interrupt Enable

0 Disable

1 Enable

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The default value for Interrupt Enable Registers is interrupt disable. Setting INE bit of Interrupt Configuration Register (C3h) to “1”, INTB pin will generate an interrupt signal.

16Ch GPIO Value Register 1 (R/W)

Bit	D7:D1
Name	GPV [7:0]
Default	0000 1110

16Dh GPIO Value Register 2 (R/W)

Bit	D7:D0
Name	GPV [15:8]
Default	0000 0000

GPV GPIO Value
Define GPIO values.
0 GPIO=0, when GPE is enabled.
1 GPIO=1, when GPE is enabled.

16Eh GPIO Enable Register 1 (R/W)

Bit	D7:D0
Name	GPE [7:0]
Default	0111 0000

16Fh GPIO Enable Register 2 (R/W)

Bit	D7:D0
Name	GPE [15:8]
Default	0000 0000

GPE GPIO Enable
0 Disable GPIO function
1 Enable GPIO function

170h GPIO Map Register 1 (R/W)

Bit	D7:D4	D3:D0
Name	GM1[3:0]	GM0[3:0]
Default	0000	0000

171h GPIO Map Register 2 (R/W)

Bit	D7:D4	D3:D0
Name	GM3[3:0]	GM2[3:0]
Default	0000	0000

172h GPIO Map Register 3 (R/W)

Bit	D7:D4	D3:D0
Name	GM5[3:0]	GM4[3:0]
Default	0001	0010

173h GPIO Map Register 4 (R/W)

Bit	D7:D4	D3:D0
Name	GM7[3:0]	GM6[3:0]
Default	0000	0011

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174h GPIO Map Register 5 (R/W)

Bit	D7:D4	D3:D0
Name	GM9[3:0]	GM8[3:0]
Default	0000	0000

175h GPIO Map Register 6 (R/W)

Bit	D7:D4	D3:D0
Name	GM11[3:0]	GM10[3:0]
Default	0000	0000

176h GPIO Map Register 7 (R/W)

Bit	D7:D4	D3:D0
Name	GM13[3:0]	GM12[3:0]
Default	0000	0000

177h GPIO Map Register 8 (R/W)

Bit	D7:D4	D3:D0
Name	GM15[3:0]	GM14[3:0]
Default	0000	0000

GMx [3:0]

Map touch key channel to GPIOx

The variable x is used to express which touch key channel. GMx [3:0] shows which GPIO maps to the touch key channel.

Below is GMx [3:0] value mapping to IS31SE5117B Pin number for your reference.

IS31SE5117B Pin #	GMx [3:0]
P1	0
P2	1
P3	2
P4	3
P9	4
P10	5
P11	6
P12	7
P13	8
P14	9
P15	10
P16	11
P17	12
P18	13
P19	14
P20	15

178h GPIO Toggle Enable Register 1 (R/W)

Bit	D7:D0
Name	TOEN [7:0]
Default	0001 0000

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179h GPIO Toggle Enable Register 2 (R/W)

Bit	D7:D0
Name	TOEN [15:8]
Default	0000 0000

TOENx Enable GPIO Toggle Mode
0 Disable Touch Key channel to enter GPIO Toggle Mode.
1 Enable Touch Key channel to enter GPIO Toggle Mode.

17Ah Key Scan Once Register (RW)

Bit	D7:D2	D1	D0
Name	SC	TR	EN
Default	0000	00	00

TR Write 1 Trigger one scan
Read 1 Busy
Read 0 Data ready
EN Enable Key Scan Once
0 Continuous scan of all enabled keys
1 Scan all enabled keys once

17Bh Table Ready Mark Register (RO)

Bit	D7	D6:D0
Name	INIRDY	MARK[6:0]
Default	0	0000000

INIRDY Touch Key Init Ready
1 Touch key is initializing
0 Touch key initialization is completed
MARK This register is used by the firmware to indicate parameters are correctly programmed.
Ready/Fail status
00 ready
Others not ready

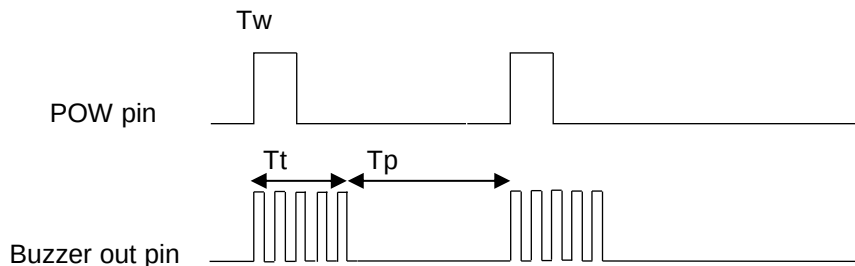
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7. Buzzer / Melody Application

09h Buzzer/Melody Register (W)

Bit	D7:D0
Name	BM
Default	-

1st byte	2nd byte	3rd byte	4th byte
Scale ID	Tt	Tw	Tp



Tt, Tw, and Tp range from 0 to 255 @ 4ms step

A Tone played duration is defined as Tt + Tp.

The support scale is from 3A to 8G#.

Frequencies for equal-tempered scale, A4 = 440 Hz "Middle C" is C4												
	3	freq	divisor	freq error	4	freq	divisor	freq error	5	freq	divisor	freq error
C					3	261.6	1911	0.01%	15	523.3	956	-0.05%
C#					4	277.2	1804	-0.01%	16	554.4	902	-0.01%
D					5	293.7	1703	-0.02%	17	587.3	851	0.04%
D#					6	311.1	1607	0.00%	18	622.3	804	-0.06%
E					7	329.6	1517	-0.01%	19	659.3	758	0.06%
F					8	349.2	1432	-0.02%	20	698.5	716	-0.02%
F#					9	370.0	1351	0.03%	21	740.0	676	-0.05%
G					10	392.0	1276	-0.04%	22	784.0	638	-0.04%
G#					11	415.3	1204	-0.01%	23	830.6	602	-0.01%
A	0	220.0	2273	-0.01%	12	440.0	1136	0.03%	24	880.0	568	0.03%
A#	1	233.1	2145	0.01%	13	466.2	1073	-0.04%	25	932.3	536	0.05%
B	2	246.9	2025	-0.01%	14	493.9	1012	0.04%	26	987.8	506	0.04%

Frequencies for equal-tempered scale, A4 = 440 Hz "Middle C" is C4												
	6	freq.	divisor	freq error	7	freq	divisor	freq error	8	freq	divisor	freq error
C	27	1046.5	478	-0.05%	39	2093.0	239	-0.05%	51	4186.0	119	0.37%
C#	28	1108.7	451	-0.01%	40	2217.5	225	0.21%	52	4434.9	113	-0.23%
D	29	1174.7	426	-0.08%	41	2349.3	213	-0.08%	53	4698.6	106	0.39%
D#	30	1244.5	402	-0.06%	42	2489.0	201	-0.06%	54	4978.0	100	0.44%
E	31	1318.5	379	0.06%	43	2637.0	190	-0.21%	55	5274.0	95	-0.21%
F	32	1396.9	358	-0.02%	44	2793.8	179	-0.02%	56	5587.7	89	0.54%

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Frequencies for equal-tempered scale, A4 = 440 Hz "Middle C" is C4												
F#	33	1480.0	338	-0.05%	45	2960.0	169	-0.05%	57	5919.9	84	0.55%
G	34	1568.0	319	-0.04%	46	3136.0	159	0.28%	58	6271.9	80	-0.35%
G#	35	1661.2	301	-0.01%	47	3322.4	150	0.33%	59	6644.9	75	0.33%
A	36	1760.0	284	0.03%	48	3520.0	142	0.03%				
A#	37	1864.7	268	0.05%	49	3729.3	134	0.05%				
B	38	1975.5	253	0.04%	50	3951.1	127	-0.36%				

Scale ID(Sid): 0 is 3A, 1 is 3A#, 2 is 3B

09h Buzzer/Melody Register (W)

Bit	D7:D0
Name	BM
Default	-

Clear Melody buffer and stop play.

09h Buzzer/Melody Register (R)

Bit	D7:D0
Name	BM
Default	0000 1010

BM Buzzer/Melody Register Read. It shows the available tone buffer size. IS31SE5117B has 10 built-in note buffers.

I²C command format - Each node is composed of 4-byte data, and the incomplete note will be ignored. The incoming note data will be ignored if the FIFO is full)

0x78, 0xF0, (Sid, Tt, Tw, Tp), (Sid, Tt, Tw, Tp),

0x78, 0xF0, 0xFF stop the melody play and clear the FIFO

0x78, 0xF0 Set the register number to 0xF0

0x79 Read FIFO remaining length

Reference schematic and tone waveform are introduced as follows:

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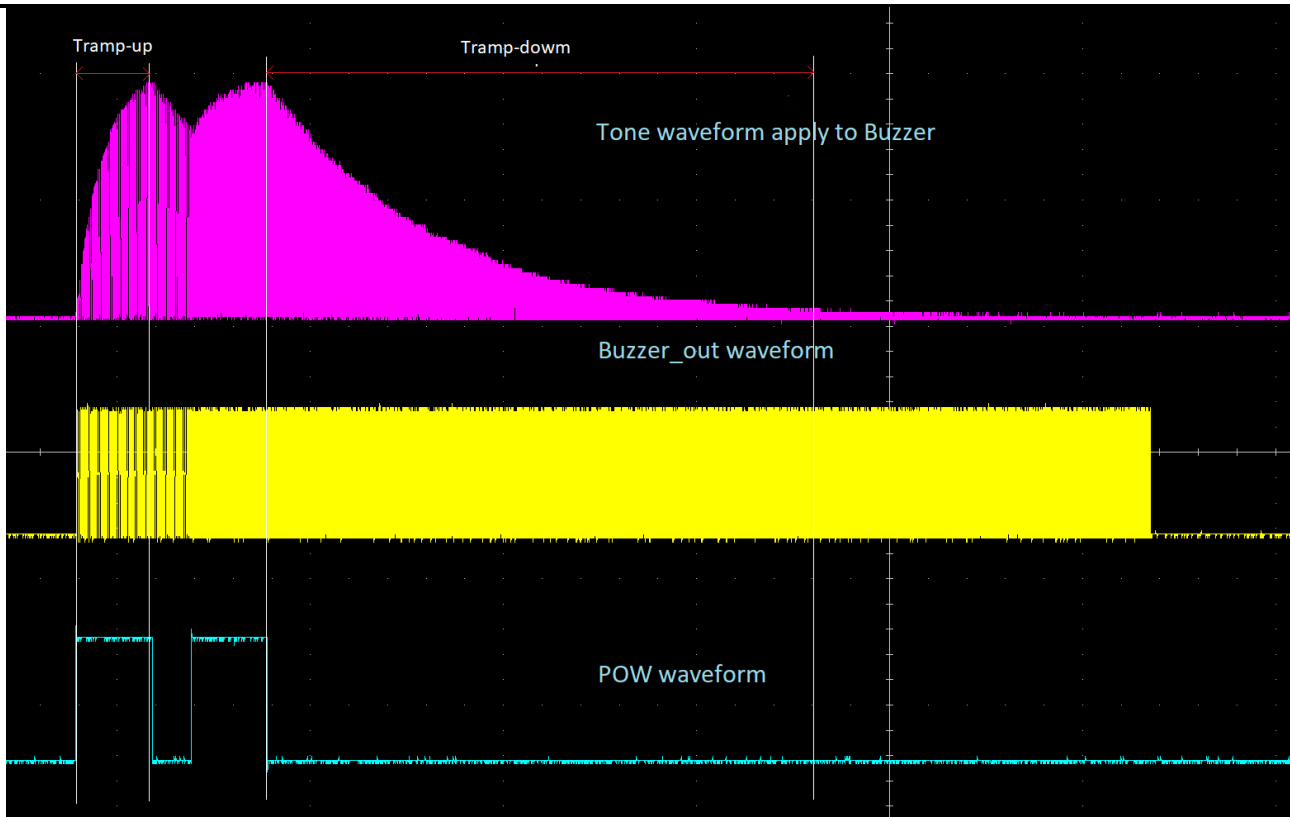


Figure 7-1 Buzzer/ Melody waveform example

Note:

Tramp-up: 100R as below figure 11 decides the signal ramp-up rate.

Tramp-down: The signal ramps down because POW is low and 47uF capacitor as below figure 11 decides the ramp-down rate.

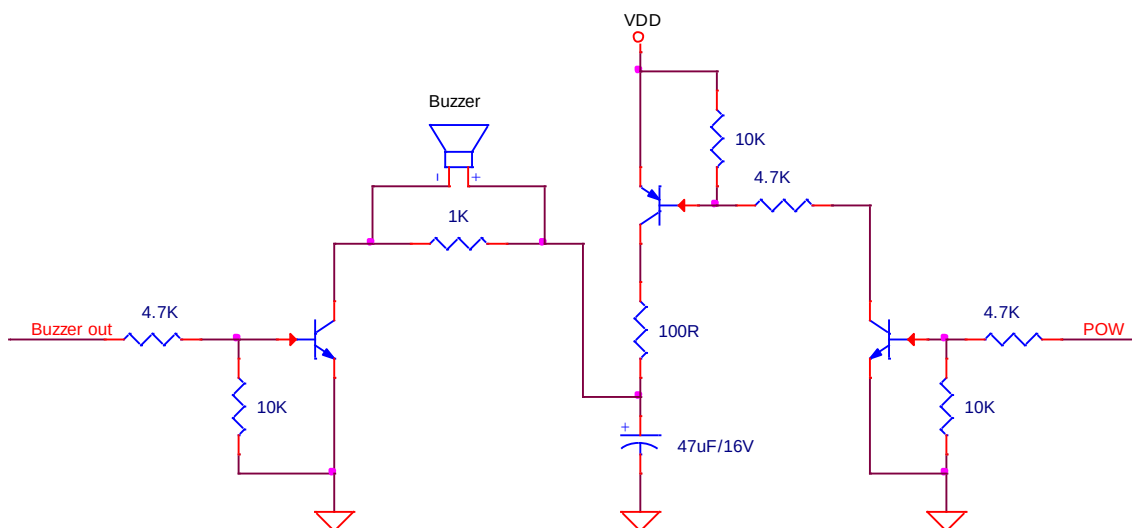


Figure 7-2 Typical application circuit for Melody

6Ah Buzzer Pin Select Register 1

Bit	D7:D0
Name	BPS1[7:0]
Default	---- -- 1

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6Bh Buzzer Pin Select Register 2

Bit	D0
Name	BPS2[7:0]
Default	---- --

BPS1/2

Buzzer output Select 1/2

Enable BPS1[0] will set Pin1 as the Buzzer output pin.

BPS1[7:1] & BPS2[7:0] unused register bits.

6Ch Enable Buzzer Power Register 1

Bit	D7:D0
Name	EBP1[7:0]
Default	---- --

6Dh Enable Buzzer Power Register 2

Bit	D7:D0
Name	EBP2[7:0]
Default	---0----

EBP1/2

Buzzer Power Select ½

EBP1[7:0] unused register.

EBP2[4] maps to KEY12. Writing 1 to EBP2[4] will enable KEY12 as the Buzzer Power. Setting other EBP2 bits doesn't work.

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8. Typical Application Information

The IS31SE5117B is an ultra-low power, fully integrated 16-channel solution for capacitive touch-buttons applications. The chip allows electrodes to project sense fields through any dielectric material such as glass or plastic.

8.1 Sensitivity Adjusting

Sensitivity can be adjusted by the external capacitor or the internal register.

A higher capacitor value will yield lower detection sensitivity. A lower capacitor value will yield higher detection sensitivity.

8.2 Interrupt

Touch key detection event will trigger INTB pin. The INTB pin will be driven low when the selected channel is pressed or released.

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9. Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (T _{smin}) Temperature max (T _{smax}) Time (T _{smin} to T _{smax}) (t _s)	150°C 200°C 60-120 seconds
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.
Liquidous temperature (T _L) Time at liquidous (t _L)	217°C 60-150 seconds
Peak package body temperature (T _p)*	Max 260°C
Time (t _p)** within 5°C of the specified classification temperature (T _c)	Max 30 seconds
Average ramp-down rate (T _p to T _{smax})	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

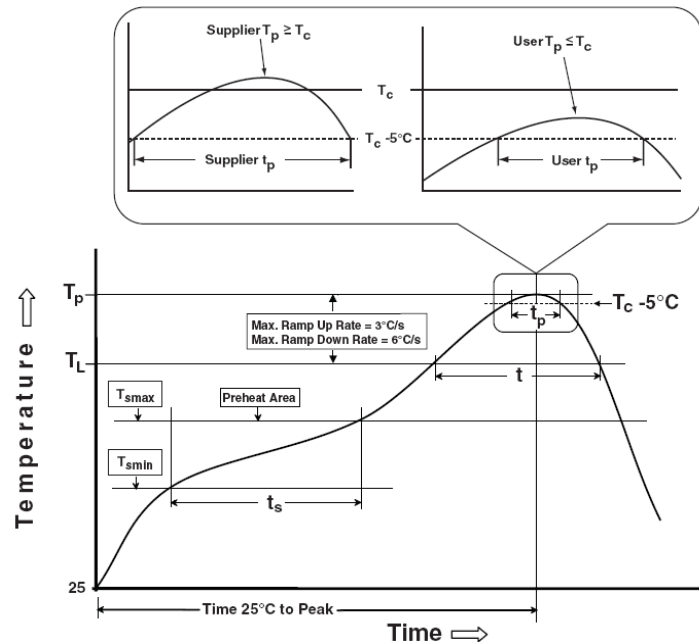


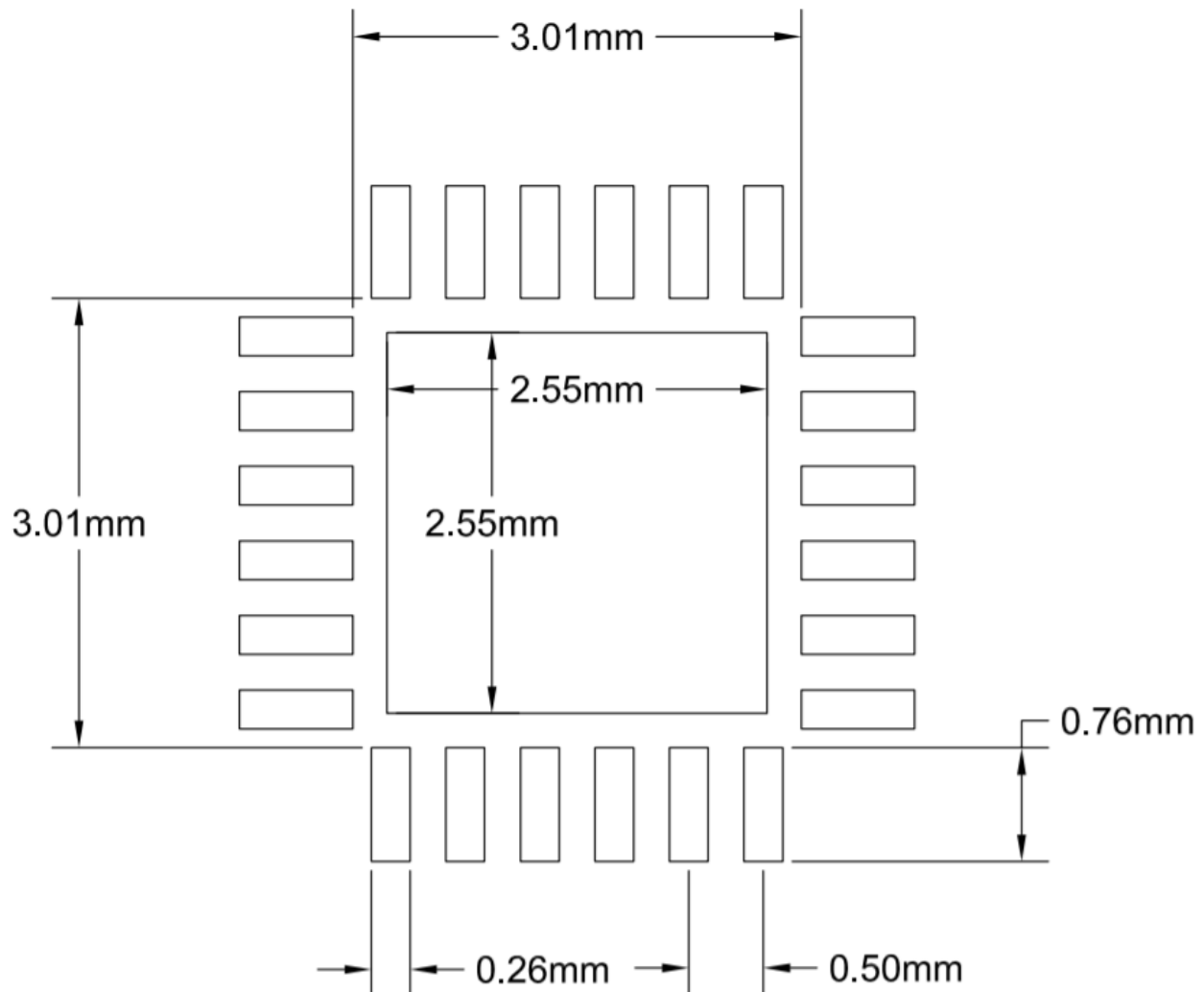
Figure 9-1 Classification Profile

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10. Package Information

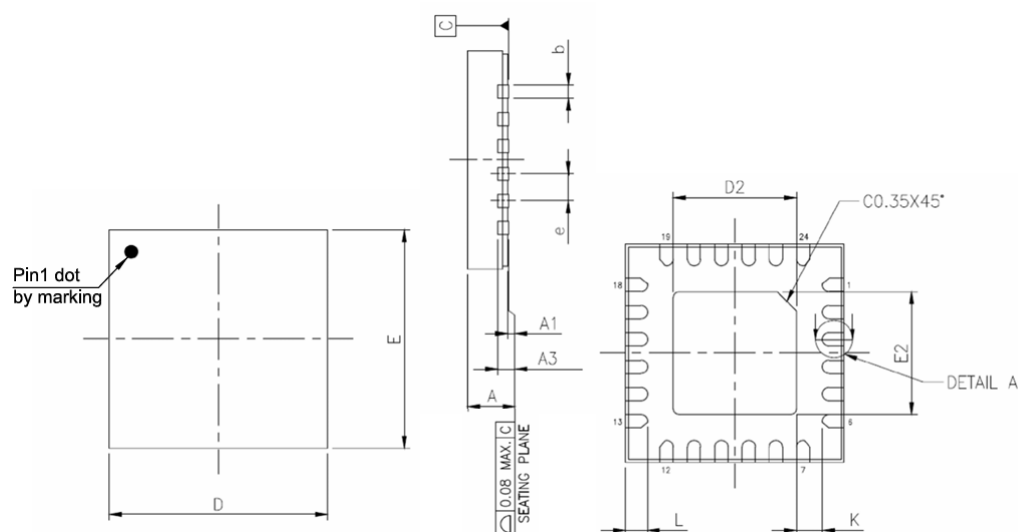
10.1 24-pin QFN

10.1.1 Recommended Land Pattern

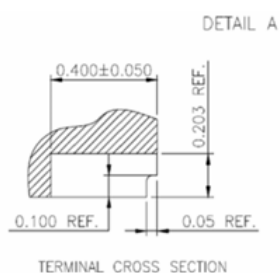


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10.1.2POD



SYM BOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203REF		
b	0.18	0.25	0.30
D	4.0BSC		
D2	2.40	2.50	2.60
E	4.0BSC		
E2	2.40	2.50	2.60
e	0.50BSC		
K	0.20	-	-
L	0.35	0.40	0.45



NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220

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11. Revisions

Revision	Detailed Information	Date
A	First formal release	2025.02.10