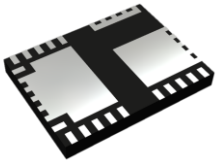
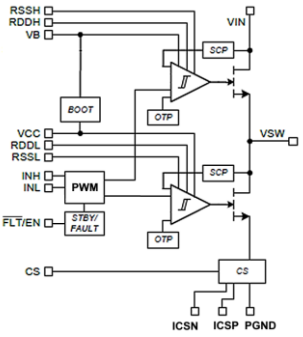
GaNSense™ Motor Drive IC
in half-bridge configuration



QFN 6 x 8 mm



Simplified schematic

1. Features

GaNSense™ Motor Drive half-bridge Power IC

- Wide V_{CC} range (10 to 24 V)
- Accurate loss-less bi-directional current sensing
- 3.3, 5, 12 V PWM input compatible
- Floating high-side with internal level shift
- Two independent logic inputs with hysteresis
- 200V/ns common mode transient immunity
- Integrated high-side bootstrap
- Shoot-through protection
- Turn-on and turn-off dV/dt control (low-side and high-side)
- Short circuit protection, low-side and high-side
- Over-temperature protection
- Autonomous low-current standby mode
- Autonomous synchronous rectification mode
- Fault output and enable input
- 800 V transient voltage rating
- 650 V continuous voltage rating
- 170 mΩ high-side FET, 170 mΩ low-side FET
- 2 KV ESD Rating (HBM)
- 2 MHz operation

Small, low profile SMT QFN

- 6x8 mm footprint, 0.85 mm profile
- Minimized package inductance
- Enlarged cooling pads

Sustainability

- RoHS, Pb-free, REACH-compliant
- Up to 40% energy savings vs Si solutions
- System level 4kg CO_2 Carbon Footprint reduction

Product Reliability

- 20-year limited warranty

2. Topologies / Applications

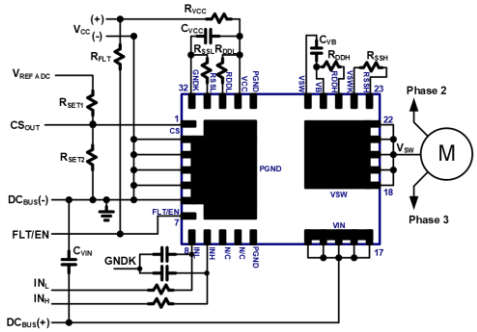
- AC-DC, DC-DC
- ACF, buck, boost, half bridge, full bridge, LLC, AHB, Class D, PFC, Motor Drive

3. Description

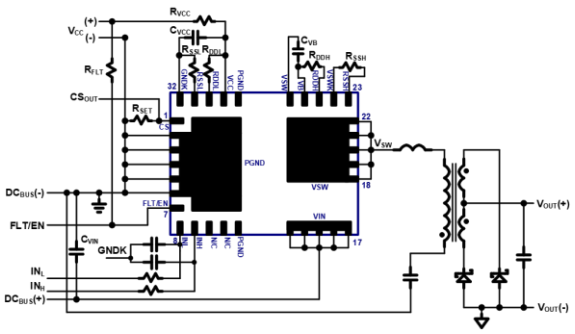
This half-bridge GaNFast™ power IC integrates high performance eMode GaN FETs with integrated gate drive, control and protection to achieve unprecedented high-frequency and high efficiency operation. GaNSense™ motor drive technology is also integrated which enables real-time, accurate sensing of voltage, current and temperature to further improve performance and robustness not achieved by any discrete GaN or discrete silicon device. GaNSense™ motor drive enables integrated loss-less current sensing which eliminates external current sensing resistors and increases system efficiency. GaNSense™ motor drive also enables short circuit and over-temperature protection to increase system robustness, while auto-standby mode increases light, tiny & no-load efficiency. These GaN ICs combine the highest dV/dt immunity, high-speed integrated drive and thermally optimized, low-inductance, QFN packaging to enable designers to achieve simple, quick, and reliable solutions. Navitas' GaN IC technology extends the capabilities of traditional topologies such as active clamp flyback, half-bridge, buck/boost, LLC and other resonant converters to reach MHz+ frequencies with very high efficiencies and low EMI to achieve unprecedented power densities at a very attractive cost structure.

4. Typical Application Circuits

Motor Drive



LLC



5. Device Configuration Options

Target Application(s)	Device Name	Auto-SR
-Uni-directional or bi-directional current sense -Power supply or Motor drive, SR disabled	NV6257-01	✘
-Motor drive, SR enabled, Standby mode disabled	NV6257-02	✓
-Motor drive, SR enabled, Standby mode disabled, External current sense	NV6257-03	✓
-Uni-directional current sense, no low current offset -Power supply or Motor drive, SR disabled	NV6257-04	✘

Table 1. Device Configuration Options

6. Table of Contents

7. Specifications

7.1. Absolute Maximum Ratings (1) (with respect to PGND unless noted)

SYMBOL	PARAMETER	MAX	UNITS
V_{IN}	HV input	0 to +650	V
$V_{SW(CONT)}$	Switch Node Continuous Voltage Rating	-7 to +657	V
$V_{SW(TRAN)}$ (2)	Switch Node Transient Voltage Rating	-10 to +800	V
I_{DSL} @ T_C=100ºC	Continuous Output Current (Low-side FET)	6.5	A
I_{DSL} PULSE@ T_C=25ºC	Pulsed Output Current (Low-side FET)	13	A
I_{DSH} @ T_C=100ºC	Continuous Output Current (High-side FET)	6.5	A
I_{DSH} PULSE@ T_C=25ºC	Pulsed Output Current (High-side FET)	13	A
V_B (to V_{SW})	High-side Gate Driver Bootstrap Rail	30	V
R_{DDH} (to V_{SW})	Hi-Side Turn-On dV/dt Setting Pin	-0.3 to V_B	V
R_{SSH} (to V_{SW})	Hi-Side Turn-Off dV/dt Setting Pin	-0.3 to 5.3	V
V_{CC}	Supply Voltage	30	V
R_{DDL}	Low-Side Turn-On DV/DT Setting Pin	-0.3 to V_{CC}	V
R_{SSL}	Low-Side Turn-Off DV/DT Setting Pin	-0.3 to 5.3	V
$V_{\overline{FLT}/EN}$	$\overline{FLT}$/EN Pin Voltage	-0.3 to V_{CC}	V
$I_{\overline{FLT}/EN}$	$\overline{FLT}$/EN Pull-Up Current	5	mA
V_{INH}, V_{INL}	PWM Input Pin Voltages	-0.6 to +20 or V_{CC}	V
V_{CS}	CS Pin Voltage	-0.3 to 5.3	V
ICSP	External Current Sense Positive Input Voltage	-0.3 to 5.3	V
ICSN	External Current Sense Negative Input Voltage	-0.3 to 5.3	V
dV/dt (3)	Slew Rate	±200	V/ns
T_J	Junction Temperature	-55 to 150	ºC
T_{STOR}	Storage Temperature	-55 to 150	ºC

(1) Absolute maximum ratings are stress ratings; devices subjected to stresses beyond these ratings may cause permanent damage.

(2) $V_{DS\ (TRAN)}$ rating allows for surge ratings during non-repetitive events that are <100us (for example start-up, line interruption). $V_{DS\ (TRAN)}$ rating allows for repetitive events that are <300ns, with 80% derating required (for example repetitive leakage inductance spikes).

(3) Max dV/dt rating is based on stress ratings and common mode transient immunity

7.2. Recommended Operating Conditions(3)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage	10	15	24	V
V_{INH}, V_{INL}	PWM Input Pin Voltage	0	5	15 or V_{CC}	V
$V_{\overline{FLT}/EN}$	$\overline{FLT}$/EN Pin Voltage	0	5	15 or V_{CC}	V
R_{DDL}, R_{DDH}	Gate drive turn-on current set resistor (see 8.5)		200		Ω
R_{SSL}, R_{SSH}	Gate drive turn-off current set resistor (see 8.5)	20	50		Ω
T_J	Operating Junction Temperature	-40		125	ºC

(3) Exposure to conditions beyond maximum recommended operating conditions for extended periods of time may affect device reliability.

7.3. ESD Ratings

SYMBOL	PARAMETER	MAX	UNITS
HBM	Human Body Model (per JS-001-2014)	2,000	V
CDM	Charged Device Model (per JS-002-2014)	750	V

7.4. Thermal Resistance

SYMBOL	PARAMETER	TYP	UNITS
$R_{\theta JC}$ (4)	Junction-to-Case	2	ºC/W
$R_{\theta JA}$ (4)	Junction-to-Ambient	40	ºC/W

(4) R_θ measured on DUT mounted on 1 square inch 2 oz Cu (FR4 PCB)

7.5. Electrical Characteristics

Typical conditions: V_{IN}=400V, V_{CC} =15V, F_{SW}=1MHz, T_{AMB}=25ºC, I_D=3.5A (unless otherwise specified)

Covered part numbers: NV6257-01, NV6257-02, NV6257-03, NV6257-04 (See Table 1)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{CC} and V_B UVLO Characteristics						
V_{CCUV+}	V_{CC} UVLO Rising Threshold		8.6		V	
V_{CCUV-}	V_{CC} UVLO Falling Threshold		6.05		V	
V_{BUV+}	V_B UVLO Rising Threshold (V_B – V_{SW})		8.6		V	
V_{BUV-}	V_B UVLO Falling Threshold (V_B – V_{SW})		6.05		V	
Bootstrap FET Characteristics						
I_{BOOT}	Bootstrap Charging Current		1.2		A	V_{CC}=12V, V_B=0V, V_{SW}=0V

Covered part numbers: NV6257-01, NV6257-04 (See Table 1)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{CC} and V_B Supply Characteristics						
$I_{QCC-STBY}$	V_{CC} Standby Current		300		µA	V_{INL} = 0V, V_{SW} >=V_{CC}
I_{QCC}	V_{CC} Static Operating Current		1.1		mA	V_{INL} = 5V, V_{INH} = 0 V
I_{QCC-SW}	V_{CC} Operating Current		6.8		mA	F_{SW} = 500 KHz (INL and INH @ 50% Duty cycle), V_{SW}=0V
$I_{QVB-STBY}$	V_B Standby Current		210		µA	V_{INH} = V_{INL}=0V, V_{SW}=0V, V_B = 15V
I_{QVB}	V_B Static Operating Current		520		µA	V_{INH}=5V, V_{INL}=0V, V_{SW}=0V, V_B = 15V
Standby Mode Characteristics						
t_{TO_STBY}	Time Out Delay Entering Standby Mode		90		µs	V_{CC} > V_{CCUV+} V_{INL}=0V
$t_{ON\_FP\_LS}$	First Pulse Propagation Delay, from INL		58		ns	V_{CC} > V_{CCUV+}, V_{INL}=5V
$t_{ON\_FP\_HS}$	First Pulse Propagation Delay, from INH		55		ns	V_{CC} > V_{CCUV+}, V_{INH}=5V

Covered part numbers: NV6257-02, NV6257-03 (See Table 1)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{CC} and V_B Supply Characteristics						
$I_{QCC-STBY}$	V_{CC} Standby Current		875		µA	V_{INL}=0V, V_{SW} >=V_{CC}
I_{QCC}	V_{CC} Static Operating Current		1.2		mA	V_{INL}=5V, V_{INH}=0V
I_{QCC-SW}	V_{CC} Operating Current		6.8		mA	F_{SW} = 500 KHz (INL and INH @ 50% Duty cycle), V_{SW}=0V
$I_{QVB-STBY}$	V_B Standby Current		340		µA	V_{INH} = V_{INL} = 0V, V_{SW}=0V, V_B=15V
I_{QVB}	V_B Static Operating Current		612		µA	V_{INH} = 5V, V_{INL} = 0V, V_{SW} = 0V, V_B = 15V

7.6. Electrical Characteristics (2, cont.)

Typical conditions: V_{IN}=400V, V_{CC} =15V, F_{SW}=1MHz, T_{AMB}=25ºC, I_D=3.5A (unless otherwise specified)

Covered part numbers: NV6257-01, NV6257-02, NV6257-03, NV6257-04 (See Table 1)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Input Logic Characteristics (INL,INH)						
$V_{LOGIC-H}$	Input Logic High Threshold (rising edge)		2.5	2.8	V	
$V_{LOGIC-L}$	Input Logic Low Threshold (falling edge)	1.1	1.2		V	
$V_{LOGIC-HYS}$	Input Logic Hysteresis		1.3		V	
Switching Characteristics						
F_{SW}	Switching Frequency			2	MHz	
t_{PW}(1)	Pulse width	15			ns	
t_{ONHS}	Prop Delay (IN_H from Low to High, V_{SW} pulled to V_{IN})		43		ns	Fig. 3
t_{OFFHS}	Prop Delay (IN_H from High to Low, V_{SW} tri-stated)		43		ns	Fig. 3
t_{ONLS}	Prop Delay (IN_L from Low to High, V_{SW} pulled to P_{GND})		53		ns	Fig. 4
t_{OFFLS}	Prop Delay (IN_L from High to Low, V_{SW} tri-stated)		60		ns	Fig. 4
High side turn on dvdt	Time for high side V_{DS} to transition from 90% voltage to 10% voltage		55		V/ns	R_{DDH}=200Ω, V_{CC}=15V, IL=3.5A
High side turn off dvdt	Time for high side V_{DS} to transition from 10% voltage to 90% voltage		30		V/ns	R_{SSH}=20Ω, IL=3.5A
Low side turn on dvdt	Time for low side V_{DS} to transition from 90% voltage to 10% voltage		55		V/ns	R_{DDL}=200Ω, V_{CC}=15V, IL=3.5A
Low side turn off dvdt	Time for low side V_{DS} to transition from 10% voltage to 90% voltage		30		V/ns	R_{SSL}=20Ω, IL=3.5A
Over-Temperature Protection						
T_{OTP+}	OTP Shutdown Threshold		165		ºC	
T_{OTP_HYS}	OTP Restart Hysteresis		60		ºC	
Short Circuit Protection (SCP)						
V_{SCP+}	$V_{DS(ON)}$ Short Circuit Detect Threshold		9.8		V	V_{INL}= 5V, V_{CC} > 12V
t_{SCP_DLY}	Short Circuit Detect Delay to Turn Off Switch, Gate already up		120		ns	V_{INL}= 5V
t_{SCP_SIS}	Short Circuit Detect Delay to Turn Off Switch, Switching Into Short		165		ns	V_{INL}= 0V --> 5V

(1) Deglitch filter provides protection below 20ns pulse widths

7.7. Electrical Characteristics (3, cont.)

Typical conditions: V_{DS}=400V, V_{CC} =15V, F_{SW}=1MHz, T_{AMB}=25ºC, I_D=3.5A (unless otherwise specified)

Covered part numbers: NV6257-01, NV6257-02, NV6257-04 (See Table 1)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Internal Current Sense Characteristics (CS pin) (NV6257-01, NV6257-02)						
V_{CS}	CS Pin Voltage Range Capability	0.5		3.5	V	Across full range of operation
I_{CS0}	CS Output Current at I_{SW} = 0A	-15	0	15	uA	V_{INL}=5V, V_{CS}=1.65V, I_{DS}=0A, see Section 9.6.2
I_{DS_MIN}	Minimum I_{DS} for accurate uni-direction current sense		70		mA	INL=5V, R_{CS} from CS to controller GND only, see Section 9.6.1
I_{CS50}	CS Output Current at I_{SW} = +/-50% * I_{DSMAX}	±1.188	±1.25	±1.3125	mA	V_{INL}=5 V, I_{DS}=4.5A, across temp
t_{CSDLY}	CS Pin Delay (from I_{DS} to I_{CS}, at 10% rated current)		65		ns	di/dt = 10 A/us, across temp
t_{CSDLY}	CS Pin Delay (from I_{DS} to I_{CS}, at 25% rated current)		35		ns	di/dt = 10 A/us, across temp
Internal Current Sense Characteristics (CS pin) (NV6257-04)						
I_{CS50}	CS Output Current at I_{SW} = 50% * I_{DSMAX}	1.188	1.25	1.3125	mA	V_{INL}=5 V, I_{DS}=4.5A, across temp
t_{CSDLY}	CS Pin Delay (from I_{DS} to I_{CS}, at 10% rated current)		65		ns	di/dt = 10 A/us, across temp
t_{CSDLY}	CS Pin Delay (from I_{DS} to I_{CS}, at 25% rated current)		35		ns	di/dt = 10 A/us, across temp

Covered part numbers: NV6257-03 (See Table 1)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
External Current Sense Characteristics (CS pin)						
V_{SNS}	Full Scale Input Voltage			±100	mV	Across full range of operation, R3=R4=392Ω see Section 9.7
V_{CS}	CS Pin Voltage Range Capability	0.5		3.5	V	Across full range of operation
I_{CS0}	CS Output Current at I_{SW} = 0A	-15	0	15	uA	V_{INL}=5V, V_{CS}=1.65V, I_{DS}=0A
I_{CS50}	CS Output Current	±1.231	±1.25	±1.269	mA	V_{INL}=5V, V_{SNS}=±50mV, R3=R4=392Ω
t_{CSDLY}	CS Pin Delay (from I_{DS} to I_{CS}, at 10% rated current)		70		ns	di/dt=10 A/us, across temp, R_{SNS}=12.5mΩ, across temp
t_{CSDLY}	CS Pin Delay (from I_{DS} to I_{CS}, at 25% rated current)		32		ns	di/dt=10 A/us, R_{SNS}=12.5mΩ, across temp

Covered part numbers: NV6257-02, NV6257-03 (See Table 1)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Synchronous Rectifier Mode (SREN)						
SR_{ARM}	Arming Voltage to Allow for Auto SR Mode Next Cycle (V_{DS} Rising)		11		V	See Section 9.9
SR_{ON}	VDS Falling Threshold to Turn On Switch		-1.05		V	$V_{INH} = V_{INL} = 0V$, see Section 9.9
$SR_{DEGLITCH}$	Time VDS must be below SR_{ON} to Trigger Gate On.		100		ns	$V_{INH} = V_{INL} = 0V$, see Section 9.9
SR_{MOT}	Minimum On-Time Of SR Switch		92		ns	$V_{INH} = V_{INL} = 0V$, see Section 9.9
SR_{OFF}	I_{DS} Rising Threshold to Turn Off Switch		-600		mA	$V_{INH} = V_{INL} = 0V$, see Section 9.9

7.8. Electrical Characteristics (4, cont.)

Typical conditions: V_{DS}=400V, V_{CC} =15V, F_{SW}=1MHz, T_{AMB}=25ºC, I_D=3.5A (unless otherwise specified)

Covered part numbers: NV6257-01, NV6257-02, NV6257-03, NV6257-04 (See Table 1)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Low side GaN FET Characteristics						
I_{DSS}	Drain-Source Leakage Current		0.75	25	µA	V_{DS} = 650 V, V_{INL} = 0 V
I_{DSS}	Drain-Source Leakage Current, TC =150 ºC		7		µA	V_{DS} =650V, V_{INL} =0V, T_C =150 ºC
$R_{DS(ON)}$	Low-side FET Drain-Source Resistance		170	238	mΩ	V_{INL} = 5 V, I_D = 3.5 A
V_{SD}	Source-Drain Reverse Voltage		3.3		V	V_{INL} = 0 V, V_{INH} = 0 V, I_{SD} = 3.5 A
Q_{OSS}	Output Charge		17.8		nC	V_{DS} = 400 V, V_{INL} = 0V, V_{INH} = 0 V
Q_{RR}	Reverse Recovery Charge		0		nC	V_{DS} = 400 V
C_{OSS}	Output Capacitance		26		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(er)}$ (1)	Effective Output Capacitance, Energy Related		32.1		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(tr)}$ (2)	Effective Output Capacitance, Time Related		44.7		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
High side GaN FET Characteristics						
I_{DSS}	Drain-Source Leakage Current		0.1	25	µA	V_{DS} = 650 V, V_{INL} = 0 V
I_{DSS}	Drain-Source Leakage Current, TC =150 ºC		7		µA	V_{DS} =650V, V_{INL} =0V, T_C =150 ºC
$R_{DS(ON)}$	High-side FET Drain-Source Resistance		170	238	mΩ	V_{INL} = 5 V, I_D = 3.5 A
V_{SD}	Source-Drain Reverse Voltage		3.4		V	V_{INL} = 0 V, V_{INH} = 0 V, I_{SD} = 3.5 A
Q_{OSS}	Output Charge		15.8		nC	V_{DS} = 400 V, V_{INL} = 0V, V_{INH} = 0 V
Q_{RR}	Reverse Recovery Charge		0		nC	V_{DS} = 400 V
C_{OSS}	Output Capacitance		19		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(er)}$ (1)	Effective Output Capacitance, Energy Related		28.5		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V
$C_{O(tr)}$ (2)	Effective Output Capacitance, Time Related		39.6		pF	V_{DS} = 400 V, V_{INL} = 0 V, V_{INH} = 0 V

(1) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

(2) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

7.9. Switching Waveforms

(T_C = 25 ºC unless otherwise specified)

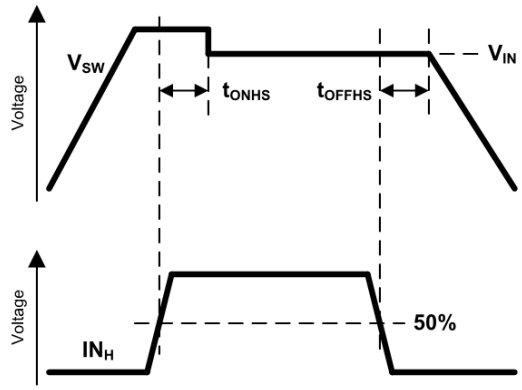


Fig. 1. Propagation Delay ZVS Mode $t_{ONHS/OFFHS}$

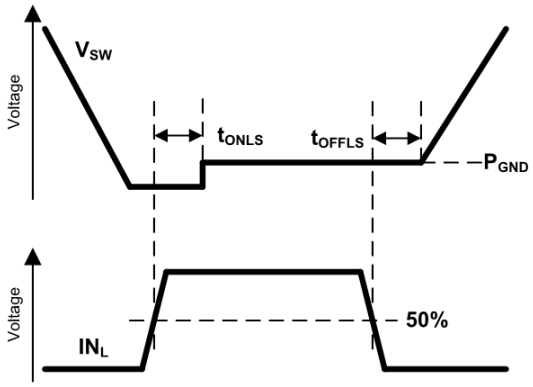


Fig. 2. Propagation Delay ZVS Mode $t_{ONLS/OFFLS}$

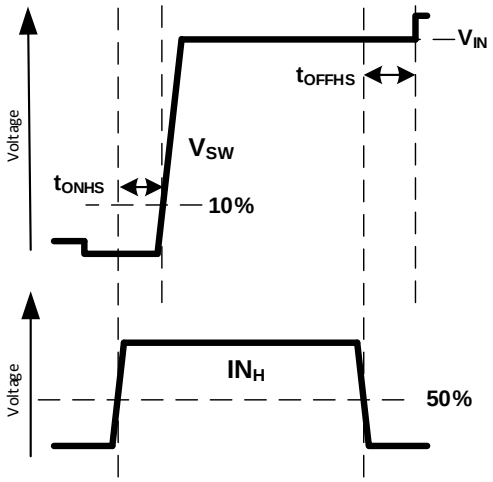


Fig. 3. Propagation Delay Hard Switching $t_{ONHS/OFFHS}$

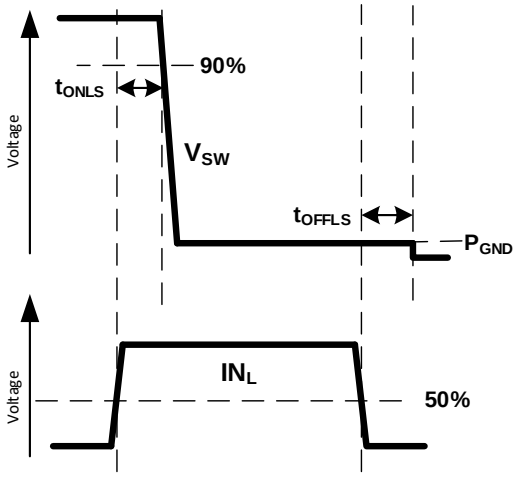


Fig. 4. Propagation Delay Hard Switching $t_{ONLS/OFFLS}$

7.10. Characteristic Graphs

(GaN FET, T_C = 25 ºC unless otherwise specified)

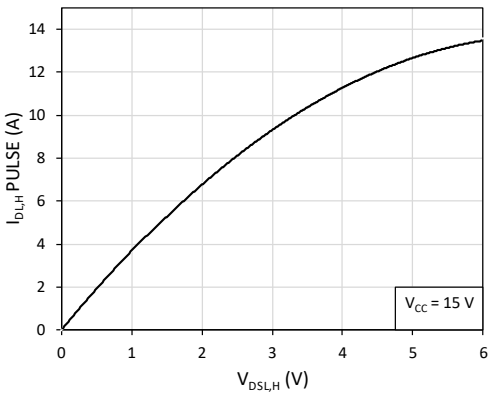


Fig. 5. Pulsed Drain current ($I_{DSL,H}$ PULSE) vs. drain-to-source voltage ($V_{DSL,H}$) at T = 25 °C

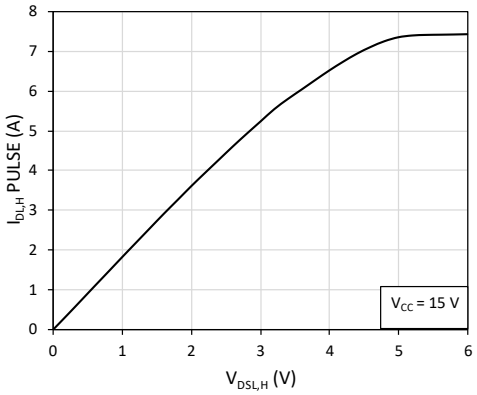


Fig. 6. Pulsed Drain current ($I_{DSL,H}$ PULSE) vs. drain-to-source voltage ($V_{DSL,H}$) at T = 125 °C

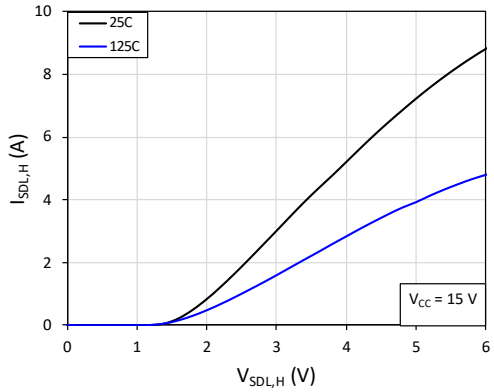


Fig. 7. Source-to-drain reverse conduction voltage ($I_{SDL,H}$)

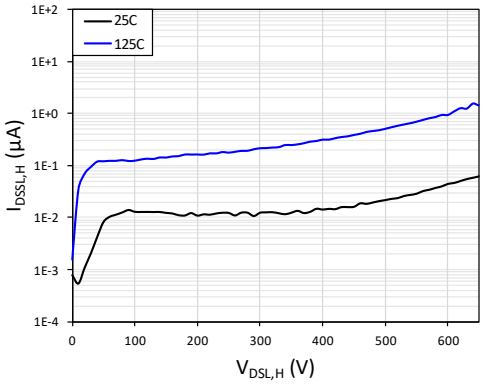


Fig. 8. Drain-to-source leakage current ($I_{DSSL,H}$) vs.drain-to-source voltage ($V_{DSL,H}$)

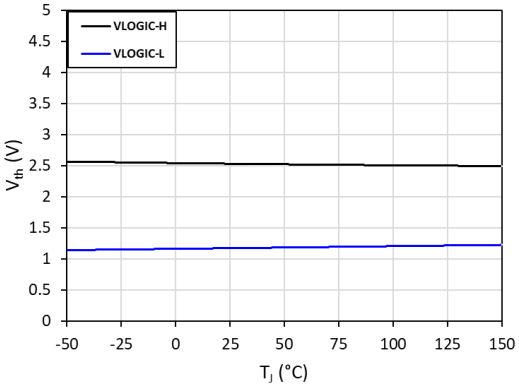


Fig. 9. $V_{LOGIC-H}$ and $V_{LOGIC-L}$ vs. junction temperature (T_J)

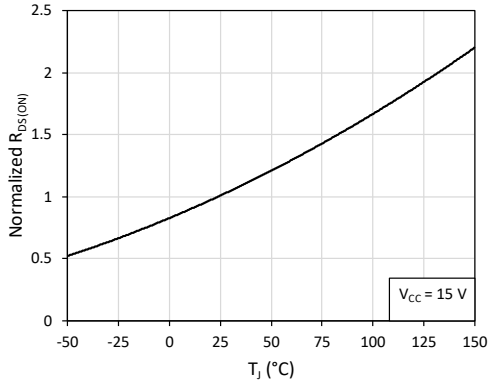


Fig. 10. Normalized on-resistance ($R_{DSL,H(ON)}$) vs. junction temperature (T_J)

Characteristic Graphs (Cont.)

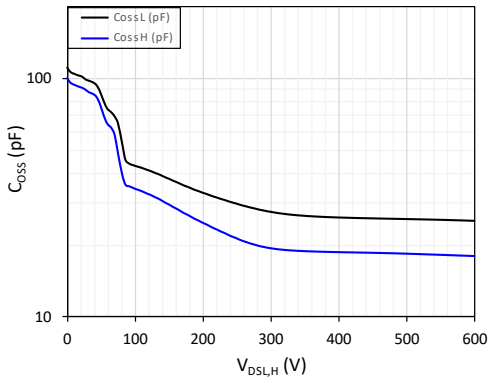


Fig. 11. Output capacitance ($C_{OSSL,H}$) vs. drain-to-source voltage ($V_{DSL,H}$)

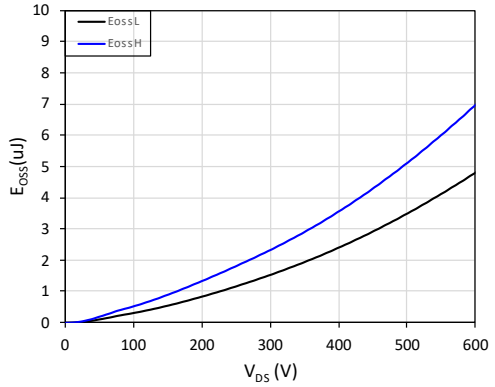


Fig. 12. Energy stored in output capacitance ($E_{OSSL,H}$) vs. drain-to-source voltage ($V_{DSL,H}$)

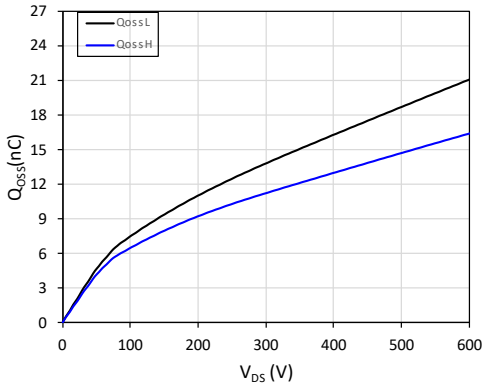


Fig. 13. Charge stored in output capacitance (Q_{OSS}) vs. drain-to-source voltage (V_{DS})

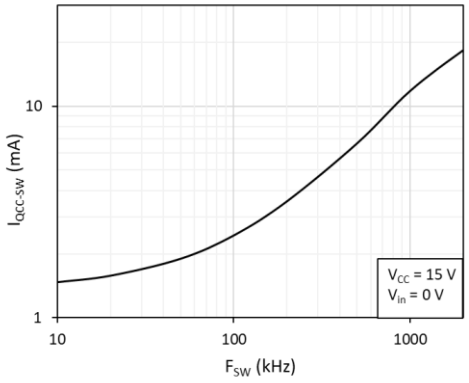


Fig. 14. V_{CC} operating current (I_{QCC-SW}) vs. operating frequency (F_{SW})

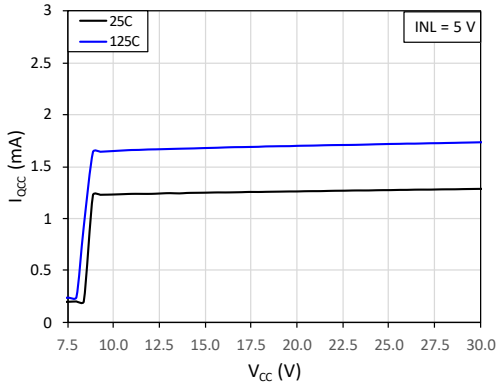


Fig. 15. V_{CC} quiescent current (I_{QCC}) vs. supply voltage (V_{CC})

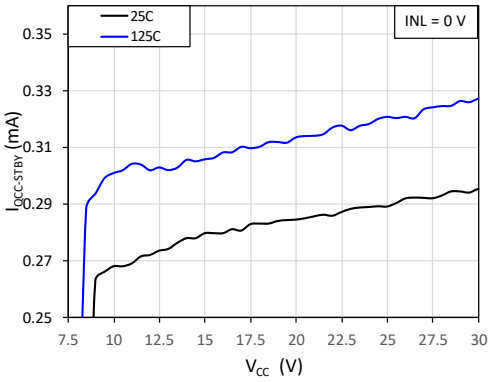


Fig. 16. V_{CC} stand-by quiescent current (I_{QCC}) vs. supply voltage (V_{CC})

Characteristic Graphs (Cont.)

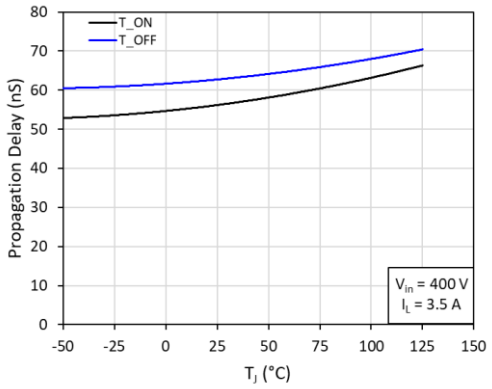


Fig. 17. Propagation delay (T_{ON} and T_{OFF}) vs. junction temperature (T_J) – low side

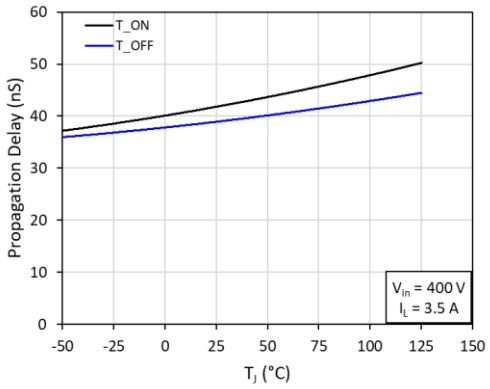


Fig. 18. Propagation delay (T_{ON} and T_{OFF}) vs. junction temperature (T_J) – high side

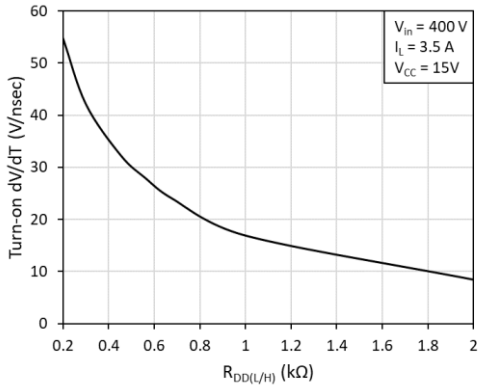


Fig. 19. Slew rate (dV/dt) vs. gate drive turn-on current set resistance ($R_{DD(L/H)}$) at T = 25 °C

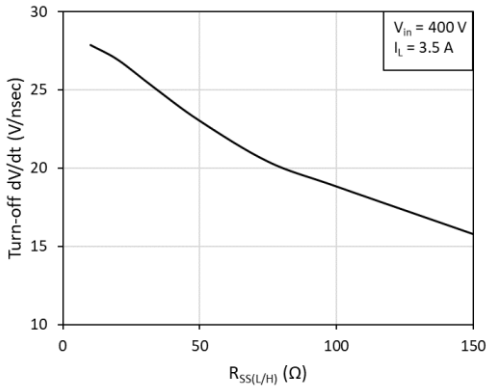


Fig. 20 Slew rate (dV/dt) vs. gate drive turn-off current set resistance ($R_{SS(L/H)}$) at T = 25 °C

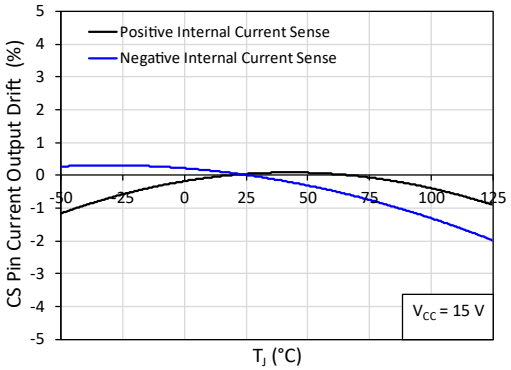


Fig. 21. CS Pin Current Output Drift vs. case temperature (T_C)

8. Pin Configurations and Functions

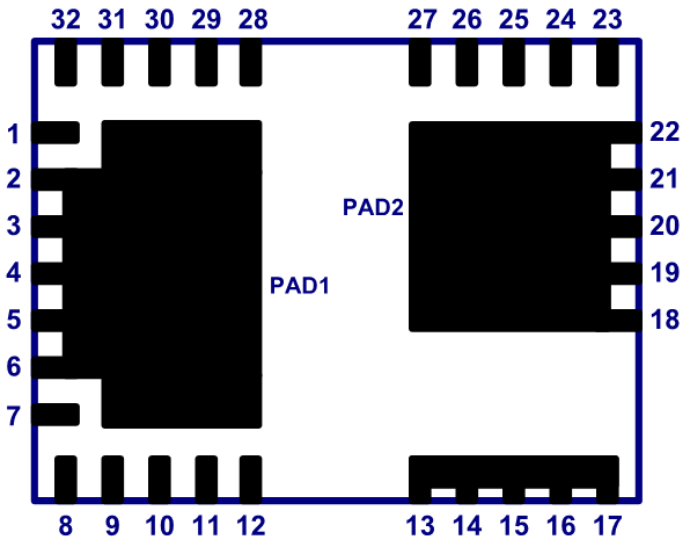


Fig. 22 Package Top View

Pin		I/O(1)	Description
Number	Symbol		
2 – 6, 12, 28, PAD1	P_{GND}	G	Power ground
1	CS	O	Current sense output pin that can sink/source current proportional to the IDS current for bi-directional current sense capability. Need external resistors to set voltage gain.
7	$\overline{FLT}$/EN	I/O	Internal fault output / Device enable
8	INL	I	Low-side logic input
9	INH	I	High-side logic input
10	ICSN	I	External Current sense negative input pin
11	ICSP	I	External Current sense positive input pin
13 - 17	VIN	P	Positive DC bus
18 – 22,27, PAD2	VSW	O	Half-bridge switch node
23	RSSH	I	High-side turn-off dV/dt control, with resistor to VSWK
24	VSWK	P	VSW Kelvin Connection for RSSH, connected internally to VSW
25	RDDH	I	High-side turn-on dV/dt control, with resistor to VB
26	VB	P	High-side gate driver bootstrap capacitor connection
29	VCC	P	IC supply voltage
30	RDDL	I	Low-side turn-on dV/dt control, with resistor to VCC
31	RSSL	I	Low-side turn-off dV/dt control, with resistor to GNDK
32	GNDK	P	PGND Kelvin Connection for RSSL connection, connected internally to PGND

(1) I = Input, O = Output, P = Power, G = Ground

9. Functional Description

The functional description contains additional information regarding the IC operating modes and pin functionality.

9.1. GaN Power IC Connections and Component Values

The typical connection diagram for this GaN Half-Bridge IC is shown in Fig. 23. The IC pins include the drain of the high-side GaN power FET (V_{IN}), the half-bridge mid-point switched node (V_{SW}), the source of the low-side GaN power FET and IC GND (P_{GND}), low-side IC supply (V_{CC}), low-side turn-on dV/dt control (R_{DDL}), low-side turn-off dV/dt control (R_{SSL}), low-side referenced PWM inputs (IN_L, IN_H), low-side current sensing output (CS), $\overline{FLT}$/EN pin for enabling the device and internal fault detection, high-side supply (V_B), high-side turn-on dV/dt control (R_{DDH}), high-side turn-off dV/dt control (R_{SSH}). The external low-side components around the IC include V_{CC} supply capacitor (C_{VCC}) connected between V_{CC} pin and P_{GND}, turn-on dV/dt set resistor (R_{DDL}) connected between V_{CC} pin and R_{DDL} pin, turn-off dV/dt set resistor (R_{SSL}) connected between the R_{SSL} pin and the GNDK pin, current sense amplitude set resistor ($R_{SET1,2}$) connected between CS pin, V_{REFADC} and P_{GND}, and the $\overline{FLT}$/EN pull-up resistor (R_{FLT}) connected to V_{CC} for enabling the device and for internal fault detection. The external high-side components around the IC include V_B supply capacitor (C_{VB}) connected between V_B pin and V_{SW}, V_{DDH} supply capacitor (C_{VDDH}) connected between V_{DDH} pin and V_{SW}, turn-on dV/dt set resistor (R_{DDH}) connected between V_B pin and R_{DDH} pin, turn-off dV/dt set resistor (R_{SSH}) connected between the R_{SSH} pin and the VSWK pin. The high side V_B bypass capacitor must be chosen carefully to accommodate various system considerations such as high side wake up time and high side hold up time.

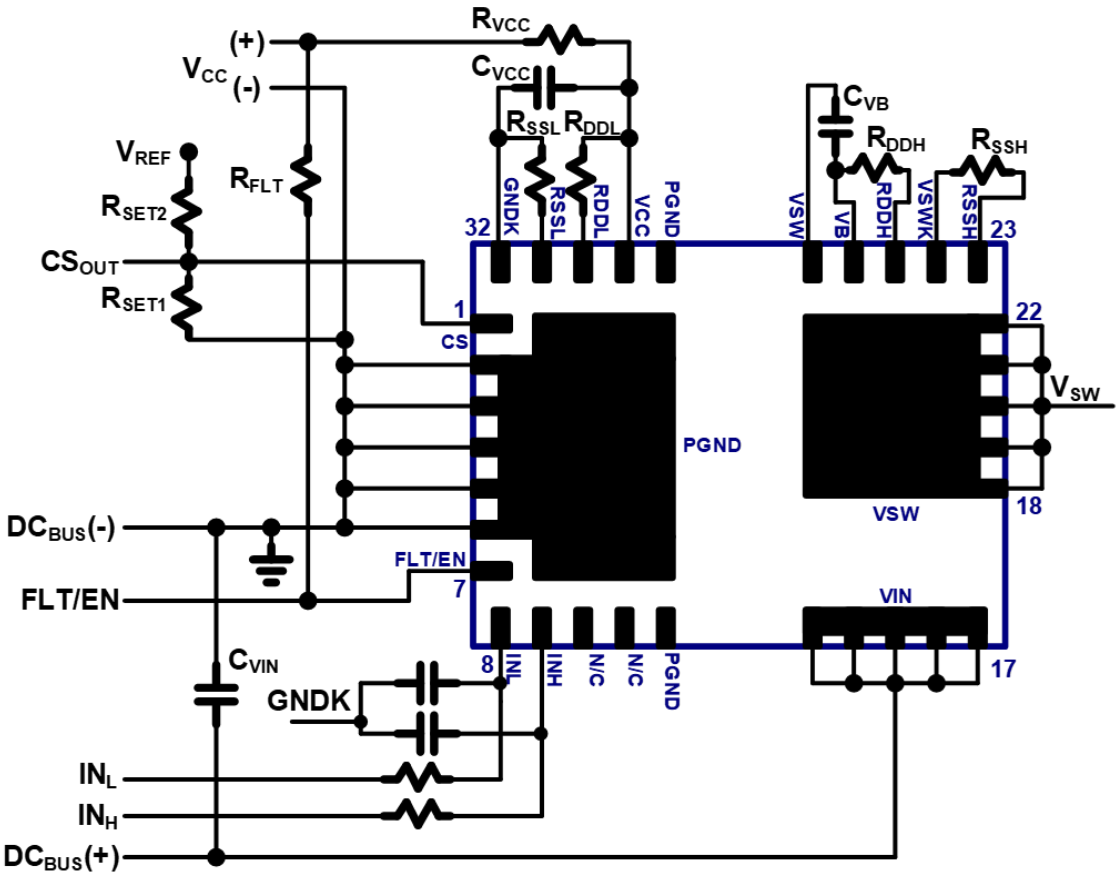


Fig. 23. IC connection diagram

The following table (Table 2) shows the recommended component values (typical only) for the external components connected to the pins of this Half-Bridge GaN power IC. These components should be placed as close as possible to the IC. Please see PCB Layout Guidelines for more information.

SYM	DESCRIPTION	TYP	UNITS
C_{VCC}	V_{CC} supply capacitor	0.22	µF
R_{VCC}	V_{CC} current limiting resistor	50	Ω
R_{INL}	IN_L input filter resistor	100	Ω
C_{INL}	IN_L filter capacitor	100	pF
R_{INH}	IN_H input filter resistor	100	Ω
C_{INH}	IN_H filter capacitor	100	pF
R_{SSL}	Low-side gate drive turn-off current set resistor	50	Ω
R_{DDL}	Low-side gate drive turn-on current set resistor	200	Ω
$R_{SET1,2}$	Current sense amplitude set resistor	See Section 9.6.2	Ω
R_{FLT}	$\overline{FLT}$/EN pull-up resistor for enabling of the device	5000	Ω
C_{VB}	V_B supply capacitor	0.01	µF
R_{SSH}	High-side gate drive turn-off current set resistor	50	Ω
R_{DDH}	High-side gate drive turn-on current set resistor	200	Ω

Table 2. Recommended component values (typical only).

The following table (Table 3) shows the correct reference location for the supply capacitors and input filter capacitors, as they should be connected when operating the Half-Bridge GaN power IC.

DESCRIPTION	SYM	REFERENCE LOCATION
V_{CC} supply capacitor	C_{VCC}	GNDK
IN_L filter capacitor	C_{INL}	GNDK
IN_H filter capacitor	C_{INH}	GNDK
V_B supply capacitor	C_{VB}	VSW

Table 3. Proper reference location for bypass and filter capacitors

9.2. UVLO Mode

This GaN Power IC includes under-voltage lockout (UVLO) circuits for both the high side and low side power supplies for properly disabling all the internal circuitry while ensuring that the gates of power FETs are kept in their OFF state. While V_{CC} is below the V_{CCUV+} threshold (8.6V, typical the low side power FET gate is kept in its OFF state while an analogous situation is applicable for the high side power FET gate while V_B is below its UVLO threshold. Once the V_{CC} supply voltage increases to exceed V_{CCUV+}, the IC enters Normal Operating Mode. The gate drive is enabled and the control signal at the IN_L input turns the internal low side power FET on and off normally. While the low side power FET is ON the bootstrap capacitor (V_B) is charged through the internal bootstrap FET. Analogous to the low side situation, once V_B rises above the UVLO threshold, the high side gate driver is enabled and can respond to IN_H. When the HS is in UVLO, the low side won't be impacted and will still switch, allowing the bootstrap capacitor to charge back up. During system power off, when V_{CC} decreases below the V_{CCUV-} threshold (6.05V, typical), the low side gate drive is disabled, and the IC enters UVLO Mode.

9.3. Normal Operating Mode

During normal operating mode, V_{CC} is set at a sufficient level (15 V typical) by the auxiliary power supply of the power converter, and V_B is at a sufficient level (as set by V_{CC} and the internal bootstrap circuit). The PWM input signals at the IN_L and IN_H pins turn the gates of the internal high- and low-side GaN power FETs on and off at the desired duty-cycle, frequency, and dead-time. The input logic signal at the IN_L pin turns the low-side half-bridge power FET on and off (0=OFF, 1=ON), and the input logic signal at the IN_H pin turns the high-side half-bridge power FET on and off (0=OFF, 1=ON). As the PWM inputs are turned on and off in a complementary manner each switching cycle, the V_{SW} pin (half-bridge mid-point) is then switched between P_{GND} (IN_L=1, IN_H=0) and V_{IN} (IN_L=0, IN_H=1) at the given frequency and duty-cycle (Fig. 24). This GaN Half-Bridge IC includes shoot-through protection circuitry that prevents both power FETs from turning on simultaneously. This IC also includes an internal bootstrap FET for supplying the high-side circuitry. The bootstrap FET is enabled during normal operating mode and is turned on each PWM switching cycle only when the IN_L pin is 'HIGH' and the low-side power FET is on. This will allow the V_B capacitor to be charged up each switching cycle for properly maintaining the necessary floating high-side supply voltage. The V_B capacitor value should be sized correctly such that the V_B voltage is maintained at a sufficient level above UVLO- during normal operation. Should the V_B-V_{SW} voltage decrease below the VB_{UV-} falling UVLO threshold (6.05 V typical) at any time, then the high-side GaN power FET will turn off and become disabled until V_B-V_{SW} increases again above the VB_{UV+} rising threshold (8.6 V typical).

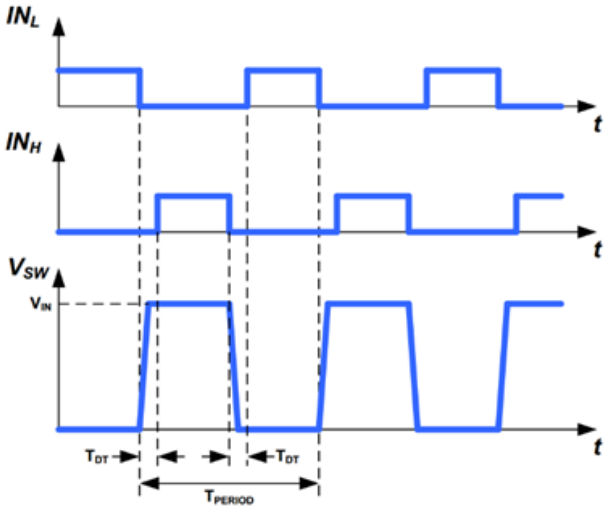


Fig. 24. Normal operating mode timing diagram

9.4. Low Power Standby Mode

This GaN Half-Bridge IC includes an autonomous low power standby mode for disabling the IC and reducing the V_{CC} current consumption. During normal operating mode, the PWM input signals at the IN_L and IN_H pins turn the gates of the internal high- and low-side GaN power FETs on and off at the desired duty-cycle, frequency, and dead-time. If the input pulses at the IN_L pin stop and stay below the lower V_{INL-} turn-off threshold (1.1V, typical) for the duration of the internal timeout standby delay (t_{TO_STBY}, 90usec, typical), then the low-side IC will automatically enter low power standby mode (Fig. 25). Low power standby mode is only available on NV6257-01, it is disabled when autonomous SR is active.

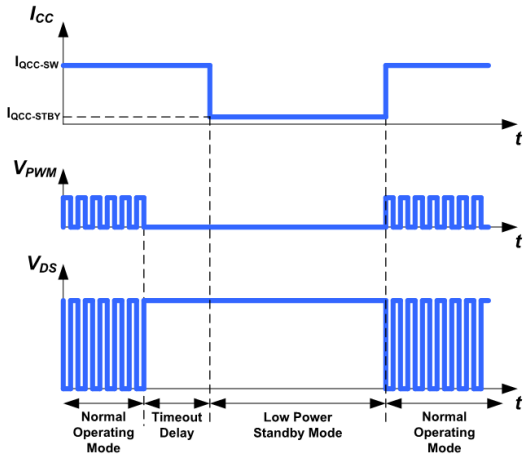


Fig. 25. Autonomous Low Power Standby Mode timing diagram

9.5. Programmable dV/dt Control

To program the turn-on dV/dt rate of the internal power FET, a resistor (R_{DD}) is placed in between the V_{CC}/V_B pin and the R_{DDL}/R_{DDH} pin. This resistor sets the turn-on current of the internal gate driver and therefore the turn-on edge dV/dt rate of the V_{DS} of the power FET (Fig. 26).

To program the turn-off dV/dt rate of the internal power FET, a resistor (R_{SS}) is placed in between the R_{SSL}/R_{SSH} pin and the GNDK/VSWK pin. This resistor sets the turn-off current of the internal gate driver and therefore the turn-off edge dV/dt rate of the V_{DS} of the power FET (Fig. 26).

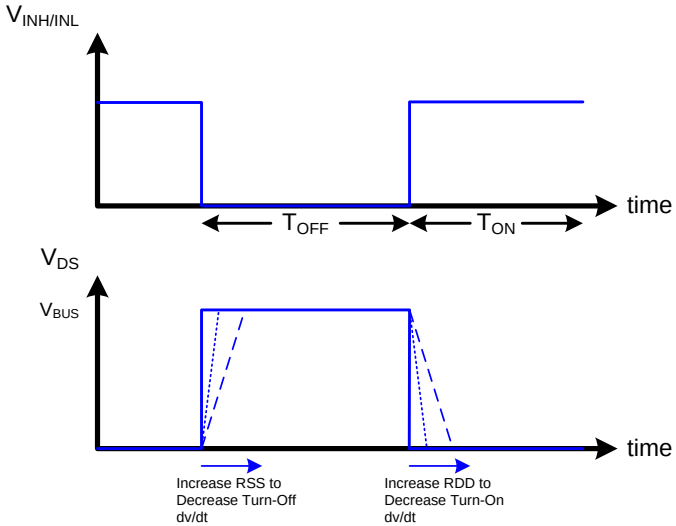


Fig. 26 Turn-on/off dV/dt slew rate control

9.6. GaNSense™ Motor Drive Technology Loss-less Current Sensing

For many applications it is necessary to sense the cycle-by-cycle current flowing through the power FET. Existing current sensing solutions include placing a current sensing resistor in between the source of the power FET and P_{GND}. This resistor method increases system conduction power losses, creates a hotspot on the PCB, and lowers overall system efficiency. To eliminate this external resistor and hotspot, and increase system efficiency, this IC includes GaNSense™ motor drive technology for integrated and accurate bidirectional loss-less current sensing.

When comparing GaNSense™ motor drive technology versus existing external resistor sensing methods (Fig. 27), the total ON resistance, $R_{ON(TOT)}$, can be substantially reduced. For a 300W high-frequency boost PFC circuit, for example, $R_{ON(TOT)}$ is reduced from 340mΩ to 170mΩ. The power loss savings by eliminating the external resistor results in a +0.5% efficiency benefit for the overall system and elimination of the R_{CS} PCB hotspot.

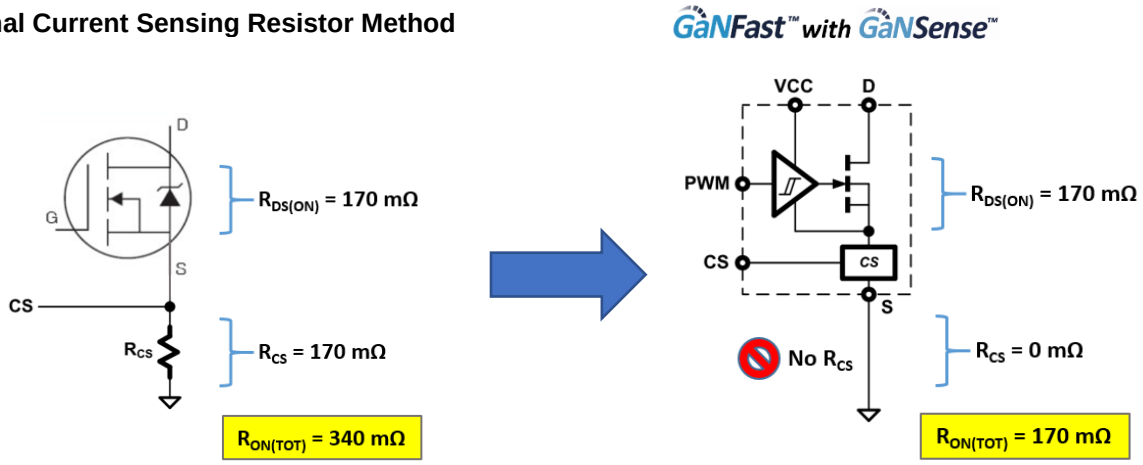


Fig. 27. External current sensing resistor vs. GaNSense™ Motor Drive Technology

9.6.1. Unidirectional Current Sensing

For compatibility with controllers/systems that are set up for unidirectional sensing, meaning the controller only wants information about current that flows from drain to source of the power FET (1st quadrant conduction), NV6257 should be configured as below:

Only populate a single resistor from the CS pin to controller GND (see Fig. 28).

Note: I_{DS} > 70mA for accurate sensing in uni-directional configuration (NV6257-01, NV6257-02, NV6257-03).

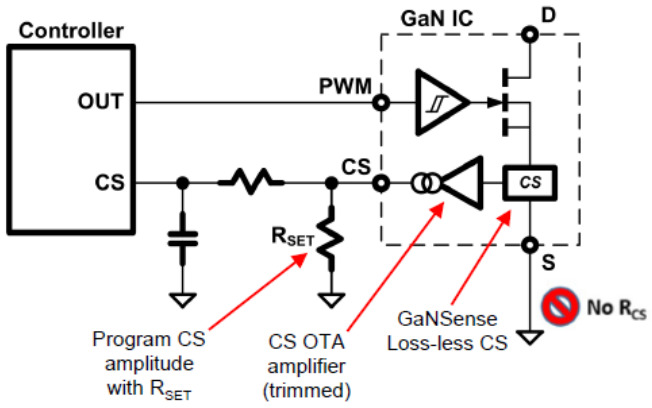


Fig. 28. Unidirectional CS System Schematic

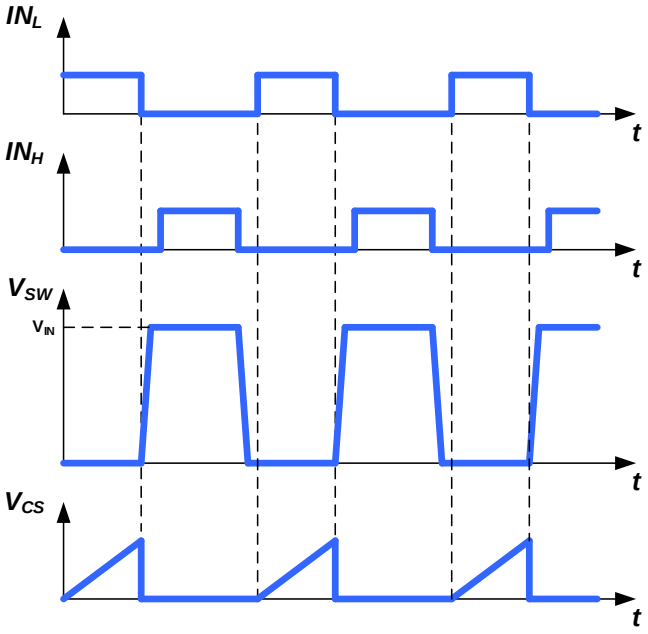


Fig. 29 Unidirectional CS Timing Diagram

9.6.2. Bidirectional Current Sensing

The current flowing through the internal low-side GaN power FET is sensed internally and then converted to a current at the current sensing output pin (CS). An external resistor divider (R_1, R_2) is connected to the CS pin and is used to set the amplitude of the CS pin voltage signal (Fig. 30). This allows for the CS pin signal to work with different controllers with different current sensing input thresholds. It is recommended to place the resistor divider close to the CS pin for improved robustness against system noise. The resistor divider is driven by an external voltage, allowing it to set the midpoint voltage at an arbitrary level. Positive current through the GaN power FET will result in a current out of the CS pin, increasing the voltage at the midpoint of the resistor divider, and negative current through the GaN power FET will result in a current into the CS pin, reducing this voltage. The CS pin current is a function of the gain factor and the absolute current in the power transistor (see Equation 1). Care should be taken in the choice of resistor values, to ensure that the voltage range corresponding to full positive to full negative current is adequately positioned within the ADC input voltage range, and the maximum voltage at the CS pin (see Equation 2).

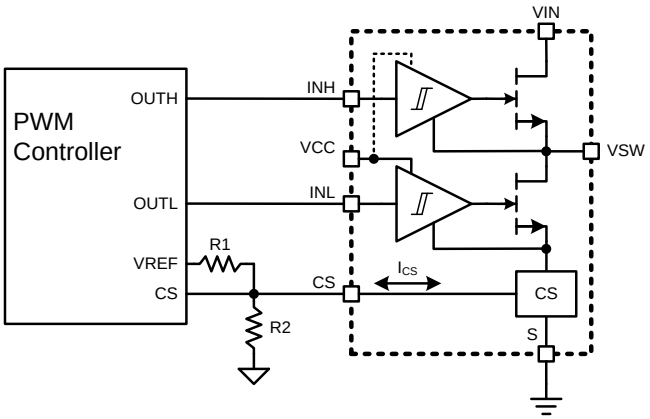


Fig. 30 Bidirectional CS System Schematic

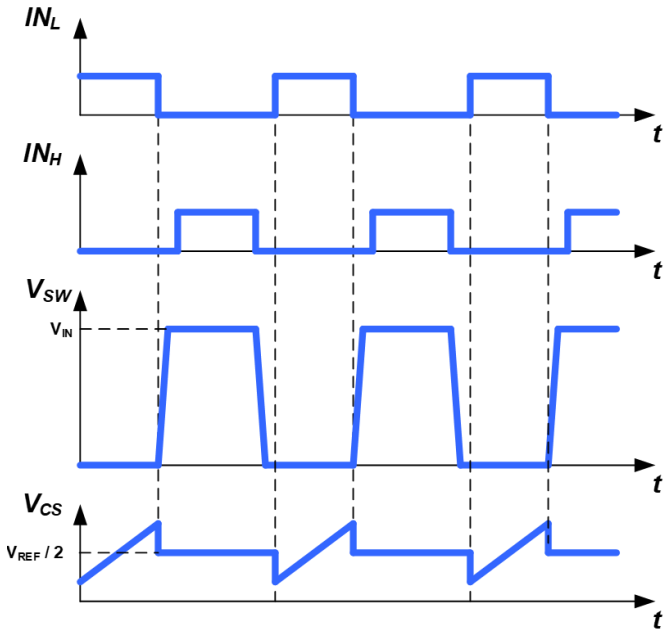


Fig. 31 Bidirectional Current Sense Timing Diagram

$$Gain = \frac{ICS}{IDS} = \frac{1.25mA}{4.5A} = 0.2778\frac{mA}{A}$$

Equation 1. Internal Current Sense Amplifier Gain Ratio

$$V_{CS} = \frac{R_{CS}}{2} * Gain * I_{DS} + \frac{VREF}{2}, with\ RCS = R1 = R2$$

Equation 2. Current Sense Pin Voltage – Internal Current Sensing

9.7. Current Sensing Using an External Sense Resistor

If more precise current sensing is required, an external current sense resistor can be used while still using the GaNSense™ Motor Drive internal amplifier to gain up the voltage across the external sense resistor (Fig. 32). Using the internal current sense amplifier to gain up the voltage across R_{SNS} allows for much smaller R_{SNS} values such that the maximum voltage drop can be sized to minimize the power loss in R_{SNS}. The maximum input dynamic range for the amplifier is +/-100mV with R3=R4=392Ω typical. The internal amplifier senses the voltage across R_{SNS} through two series resistors, R3 and R4, which are set to the same value. The voltage at CS can be calculated using Equation 3:

$$V_{CS} = V_{REF}\frac{R_1}{R_1 + R_2} + I_{SW}\frac{10(R_{SNS})}{R_{3,4}}\frac{R_1 R_2}{R_1 + R_2}$$

Equation 3 Current Sense Pin Voltage – External Current Sensing

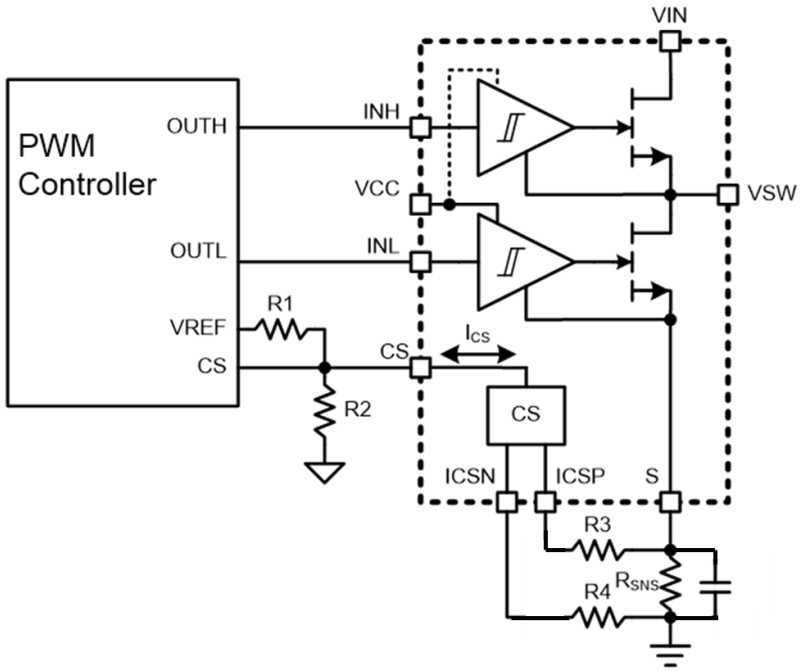


Fig. 32 Bidirectional External Current Sensing Circuit Using Internal Current Sense Amplifier

9.8. Over Temperature Protection (OTP)

This GaN Power IC includes over-temperature detection and protection (OTP) circuitry to protect the IC against excessively high junction temperatures (T_J). High junction temperatures can occur due to overload, high ambient temperatures, and/or poor thermal management. Should T_J exceed the internal T_{OTP+} threshold (165C, typical) then the IC will latch off safely, and the $\overline{FLT}$/EN pin will be pulled low. When T_J decreases again and falls below the internal T_{OTP-} threshold (105C, typical), then the OTP latch will be reset, and $\overline{FLT}$/EN will be released to go high. Until then, internal OTP latch is guaranteed to remain in the correct state while V_{CC} is greater than 5V. During an OTP event, this GaN IC will latch off and the system V_{CC} supply voltage will decrease due to the loss of the aux winding supply. The system V_{CC} will fall below the lower UV- threshold of the controller and the high-voltage start-up circuit will turn-on and V_{CC} will increase again (Fig. 33). V_{CC} will increase above the rising UV+ threshold and the controller turn on again and deliver PWM pulses again.

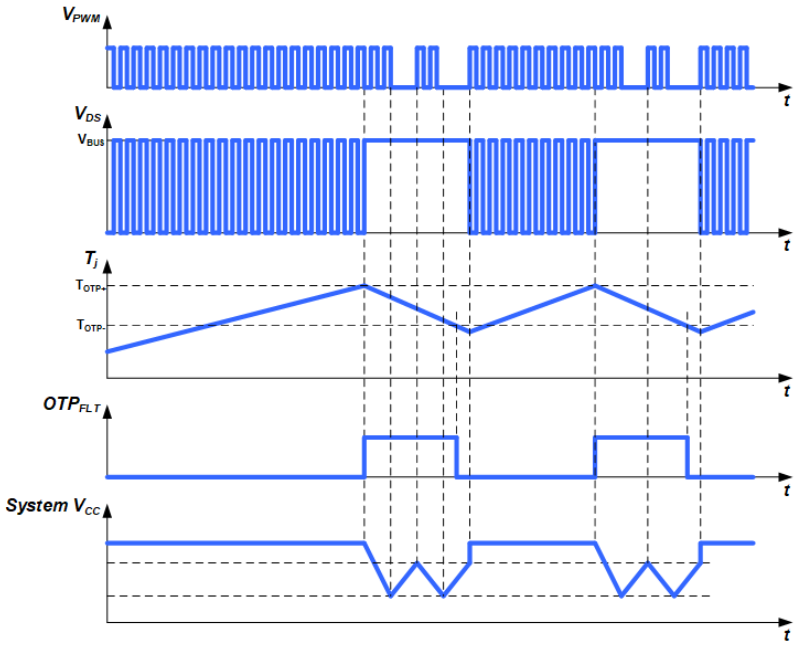


Fig. 33. OTP threshold timing diagram

9.9. Autonomous Synchronous rectification

In motor inverter and other applications where reverse current can flow through the power switches, also called “freewheeling”, the voltage across the switch in combination with the reverse current can create high power dissipation. In order to reduce the impact, multiple things can be done, including shortening the dead time (depending on the control algorithm), or driving the power switch as a synchronous rectifier (requiring appropriate control firmware). The NV6257-02 and NV6257-03 provides autonomous synchronous rectification, where upon detection of significant reverse current, the power switch is turned ON, and upon approaching zero current (SR_{OFF}) the switch is turned OFF, without any burden on the controller.

The section below describes the activation sequence of the SR functionality:

1. **Arming**
   - The chip will "arm" itself for SR operation if V_{DS} exceeds the SR_{ARM} voltage (9.8V typical) **ONLY** for versions NV6257-02 and NV6257-03.
2. **Turn-on (See Fig. 34)**
   - If the chip was previously "armed" **AND** V_{DS} falls below the SR_{ON} voltage (-1.05V typical) for more than the $SR_{DEGLITCH}$ interval (100ns typical), the driver will activate and bring up the power FET gate.
   - The gate will stay on for at least the SR_{MOT} minimum on time interval (90ns typical) to ensure switching noise does not falsely trip the turn-off detection circuit.
3. **Turn-off (See Fig. 35)**
   - Once the magnitude of current flowing from Source -> Drain falls below the SR_{OFF} threshold (600mA), the chip will turn off the power FET gate.
4. **Re-arming (See Fig. 35)**
   - VDS must rise above the SR_{ARM} voltage (9.8V typical) for the chip to be ready for the next SR cycle.

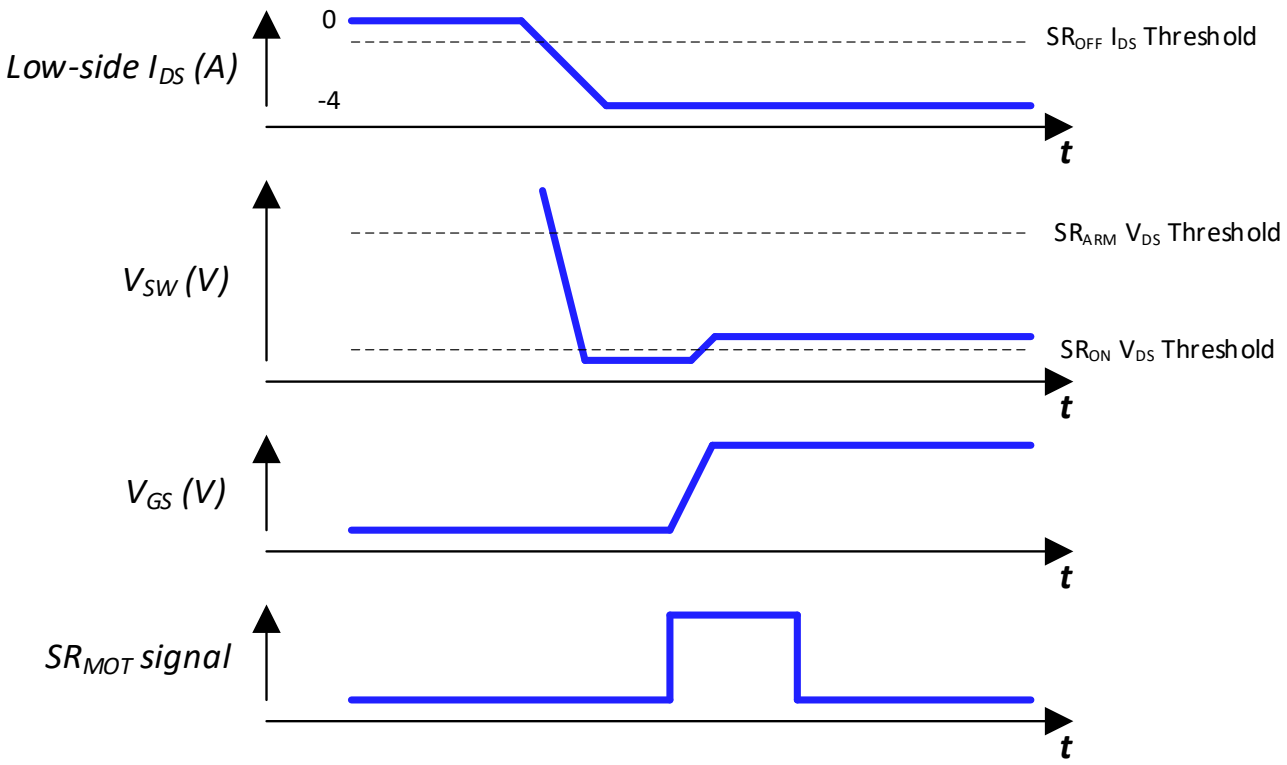


Fig. 34. SR turn-on timing diagram

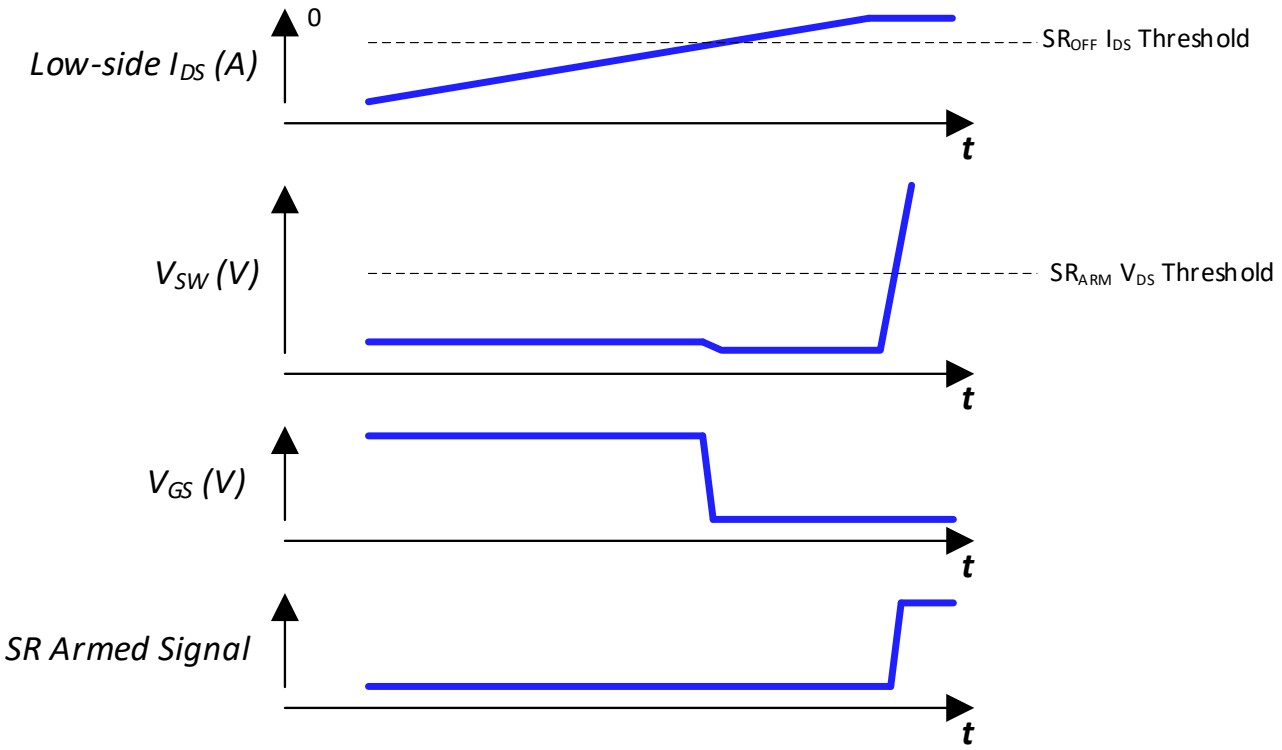


Fig. 35. SR turn-off timing diagram

9.10. Fault reporting and enable / disable function

The $\overline{\text{FLT}}$/EN pin is an open-drain pin and should be pulled up to the supply voltage of the system controller, in order to enable the GaN power IC. Should a fault occur (over-current or over-temperature), the GaN power IC will pull this pin LOW, signaling the fault to the system controller, and all switching will stop. Similarly, when the system controller decides to disable the power stage, it can pull this pin low, which the GaN power IC will monitor and all switching will stop. The open-drain architecture of this pin enables parallel connection of multiple GaN power ICs which then can be enabled or disabled all at the same time, and a fault in one of the half-bridges can trigger the whole power stage to stop switching. Using a capacitor on this pin to ground can be used to configure a minimum STOP time, where – once the fault is cleared, or the system controller has cleared the stop – the voltage on this pin will rise more slowly, as a function of the pull-up resistor and the capacitor, and once it reaches the turn-on threshold switching will resume.

9.11. Functional Schematic

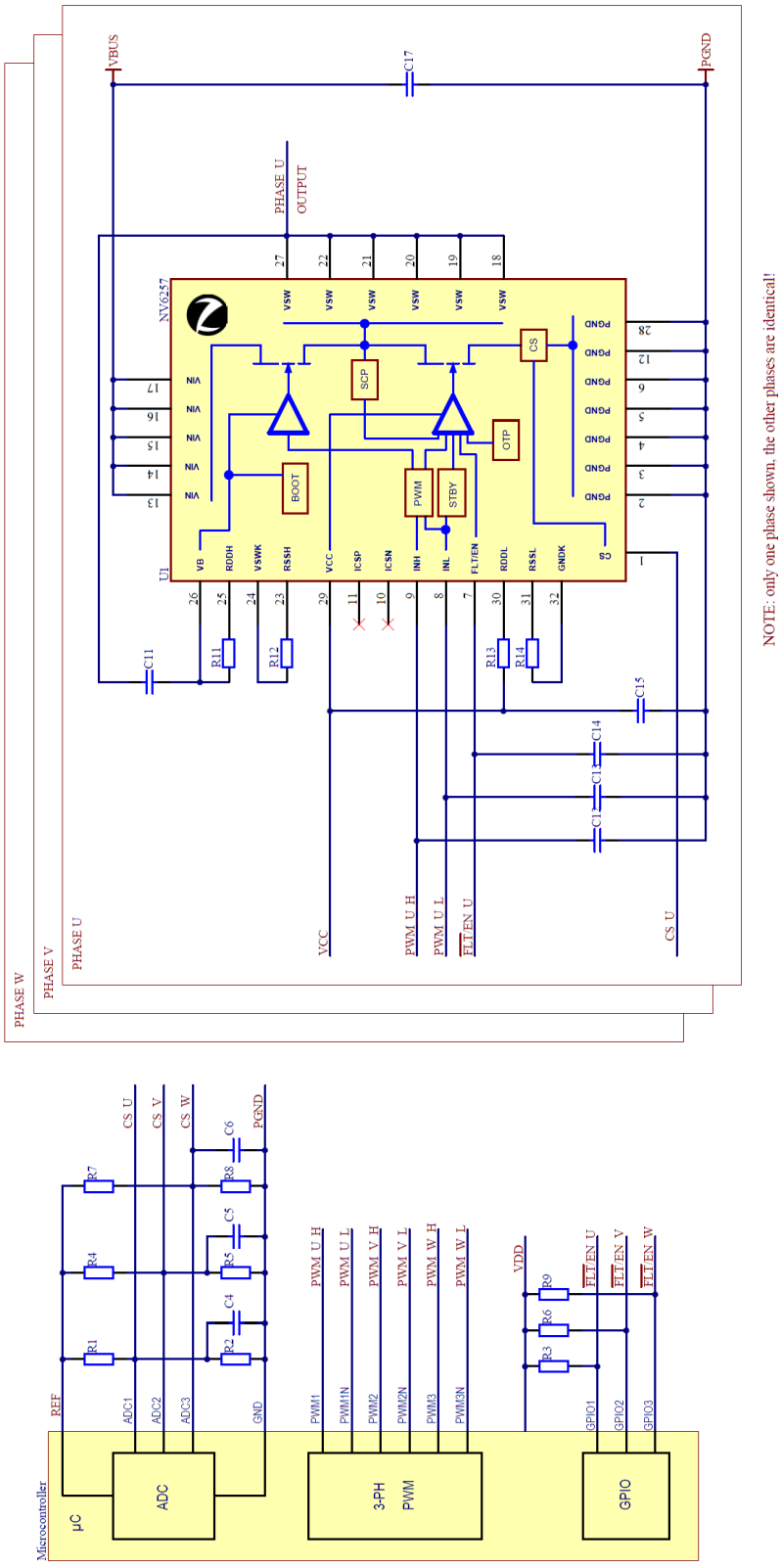


Fig. 36. Typical motor drive inverter schematic

10. PCB Layout Guidelines

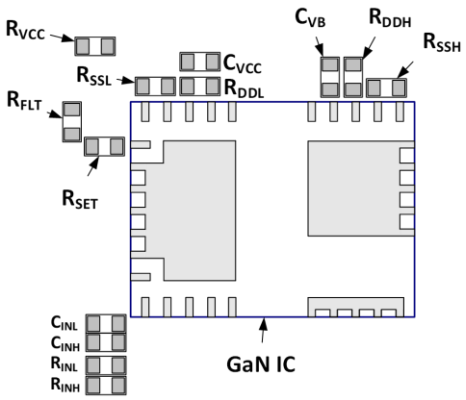
For best electrical and thermal results, these PCB layout guidelines (and 3 steps below) must be followed:

Place IC components as close as possible to the GaN IC. Place R_{SET} resistor directly next to CS pin to minimize high frequency switching noise. Connect the ground of the IC components as noted in the IC Connection Diagram to minimize high frequency switching noise. Connect controller ground to Source (P_{GND}). Route all connections on single layer. Place large copper areas on and around Pad1 and Pad2.

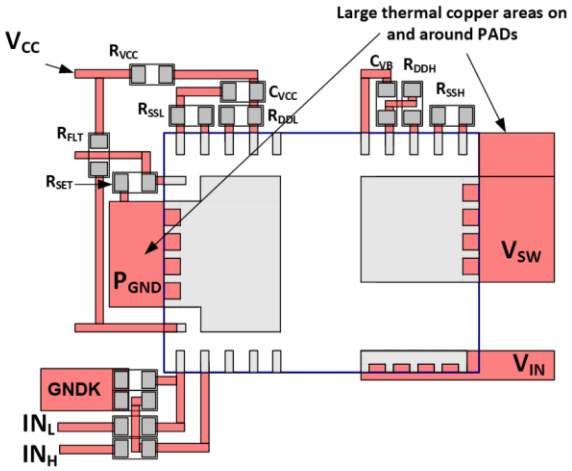
Place many thermal vias inside Pad1 and Pad2 and inside Pad1 and Pad2 copper areas.

Place large possible copper areas on all other PCB layers (bottom, top, mid1, mid2).

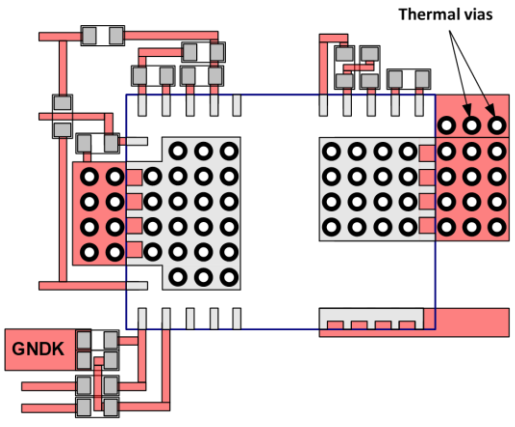
Do not extend copper planes from the low-side across the components or pads of the high-side; do not extend copper planes from the high-side across the components or pads of the low-side! Keep high and low-side layouts separate. Do not overlap!



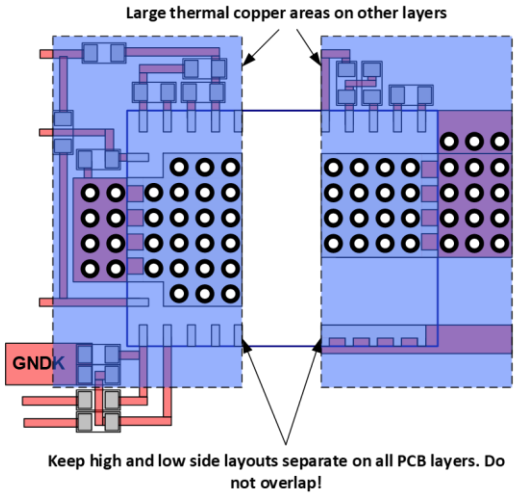
IC Component Placement



Step 1. Route all connections on single layer. Make large copper areas on and around Source pad

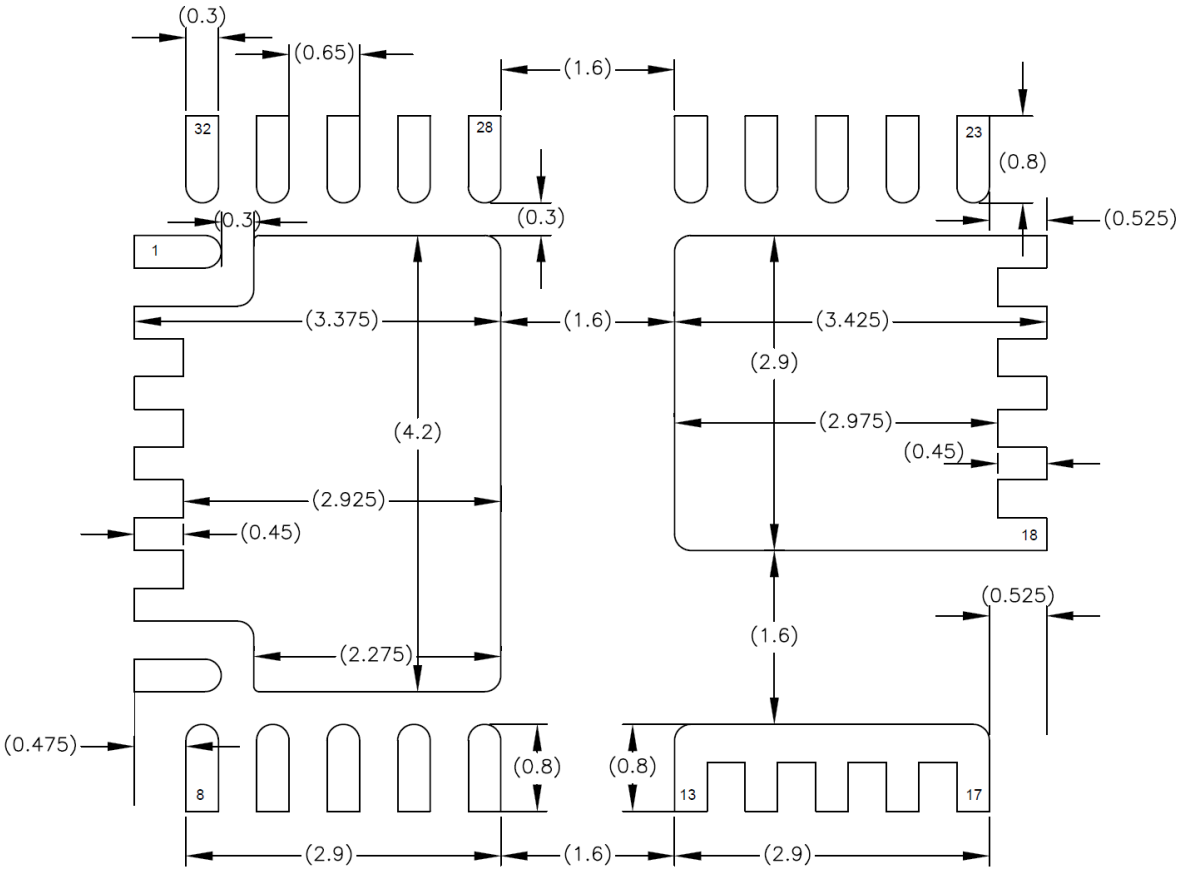


Step 2. Place many thermal vias inside source pad and inside source copper areas. (dia=0.65mm, hole=0.33mm, pitch=0.925mm, via wall=1mil)



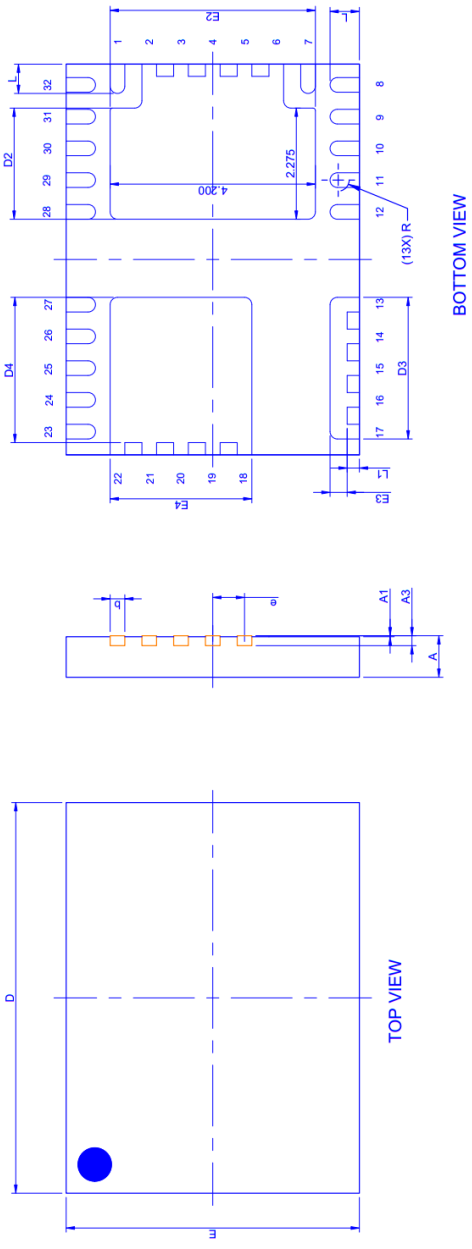
Step 3. Place large copper areas on other layers. Make all thermal copper areas as large as possible!

11. Recommended PCB Land Pattern



Top View
All dimensions are in mm

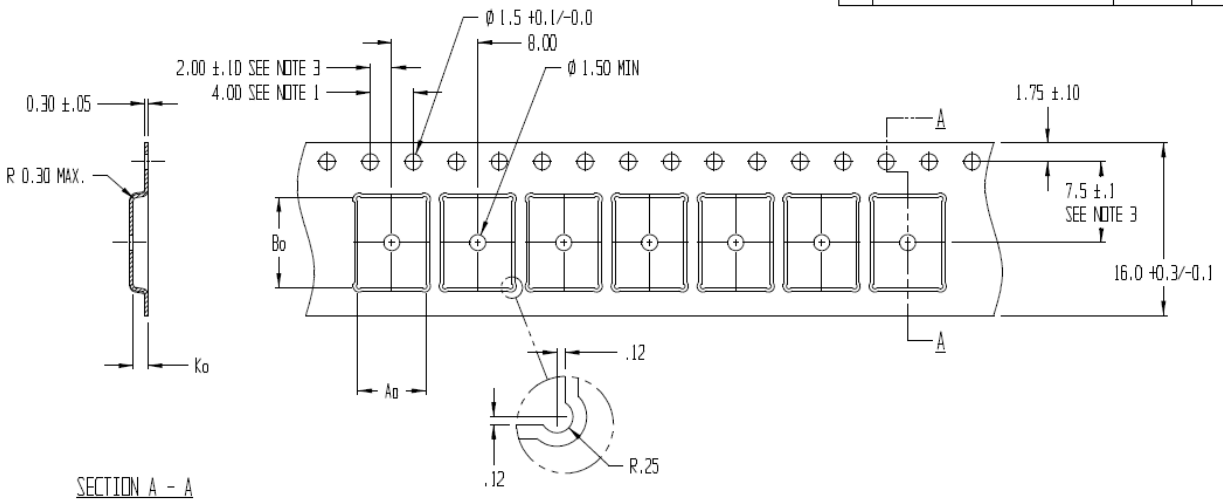
12. Package Outline (Power QFN)



SYM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	—	0.20 REF	—
D	7.93	8.00	8.07
E	5.93	6.00	6.07
D2	2.225	2.275	2.325
E2	4.15	4.20	4.25
D3	2.85	2.90	2.95
E3	0.30	0.35	0.40
D4	2.925	2.975	3.025
E4	2.85	2.90	2.95
L	0.55	0.60	0.65
L1	0.20	0.25	0.30
b	0.25	0.30	0.35
e		0.65 BSC	
R	—	0.15 REF	—

13. Tape and Reel Dimensions

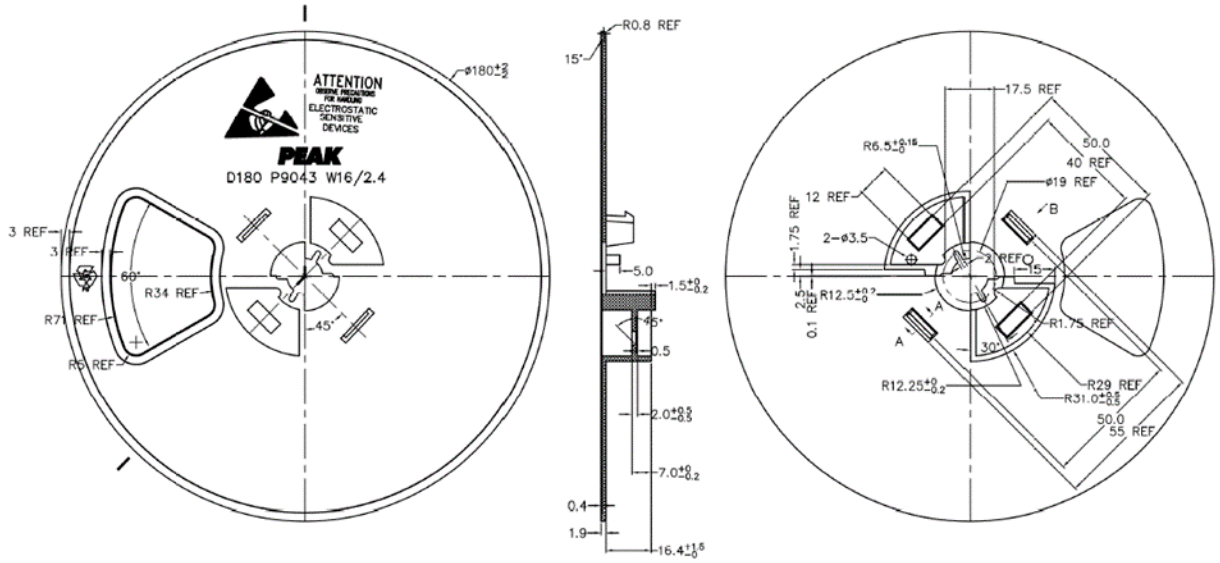
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



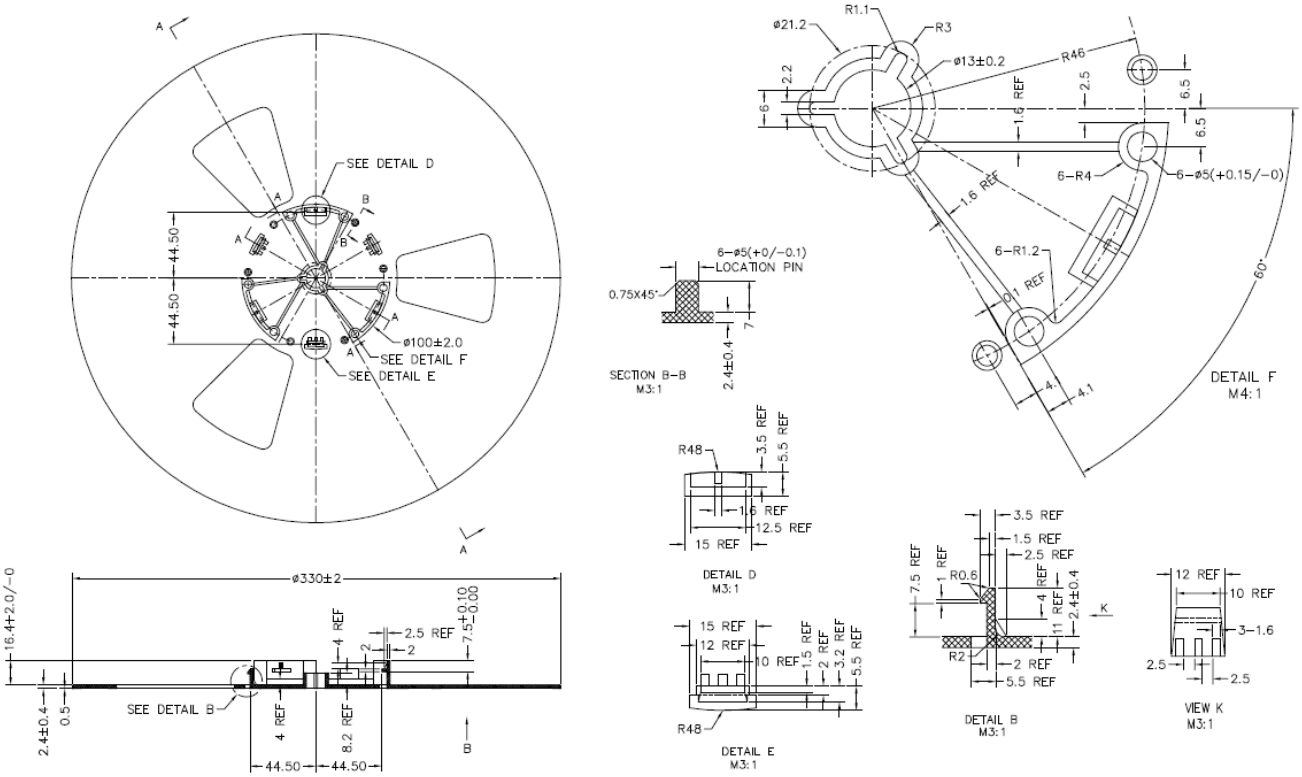
Ao = 6.35
Bo = 8.35
Ko = 1.40

13.1. Tape and Reel Dimensions (Cont.)

7" Reel



13" Reel



14. Ordering Information

Part Number	Operating Temperature Grade	Storage Temperature Range	Package	MSL Rating	Packing (Tape & Reel)
NV6257-01-RA NV6257-02-RA NV6257-03-RA NV6257-04-RA	-55°C to +150°C T_{CASE}	-55°C to +150°C T_{CASE}	6 x 8 mm PQFN	3	1000: 7” Reel
NV6257-01 NV6257-02 NV6257-03 NV6257-04	-55°C to +150°C T_{CASE}	-55°C to +150°C T_{CASE}	6 x 8 mm PQFN	3	5000: 13” Reel

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16. Revision History

Date	Status	Notes
Apr. 29, 2025	Final Datasheet	First revision

Additional Information

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