1. Features

GaNFast™ Power FET

- eMode GaN power FET
- Low 210 mΩ resistance
- 10 MHz switching frequency capability
- Ultra-low gate charge
- Zero reverse recovery charge
- Low output charge
- 800 V Transient Voltage Rating
- 700 V Continuous Voltage Rating
- TO252 PCB footprint
- Minimized package inductance
- Low thermal resistance
- Source pad cooled

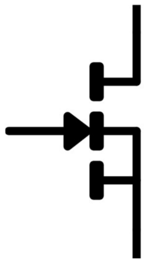
Environmental

- RoHS, Pb-free, REACH-compliant

2. Topologies / Applications

- AC-DC, DC-DC, DC-AC
- QR flyback, ACF, buck, boost, half bridge, full bridge, LLC resonant, Class D, PFC
- Wireless power
- LED lighting
- Solar Micro-inverters
- TV SMPS
- Server, Telecom

DPAK TO252-2L


Simplified Schematic

3. Description

This GaNFast™ power FET is a high performance eMode GaN FET that achieves excellent high-frequency and high efficiency operation.

This GaN power FET is source pad cooled TO252-2L packaging to enable designers to achieve simple, and excellent thermal dissipation.

Navitas' GaN technology extends the capabilities of traditional topologies such as flyback, half-bridge, buck/boost, LLC and other resonant converters to reach MHz+ frequencies with very high efficiencies and low EMI to achieve unprecedented power densities at a very attractive cost structure.

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5. Specifications

5.1. Absolute Maximum Ratings[1]

(with respect to Source (pad) unless noted)

SYMBOL	PARAMETER	MAX	UNITS
$V_{DS(TRAN)}$	Transient Drain-to-Source Voltage[2]	800	V
$V_{DS(CONT)}$	Continuous Drain-to-Source Voltage	-7 to +700	V
V_{GS}	Continuous Gate-to-Source Voltage	-2 to +7	V
V_{TGS}	Transient Gate-to-Source Voltage[3]	-6 to +10	V
I_D	Continuous Drain Current (@ T_C = 100ºC)	6.5	A
I_D PULSE	Pulsed Drain Current (10 µs @ T_J = 25°C)	13	A
P_{TOT}	Power Dissipation	43	W
T_J	Operating Junction Temperature	-55 to 150	ºC
T_{STOR}	Storage Temperature	-55 to 150	ºC

(1) Absolute maximum ratings are stress ratings; devices subjected to stresses beyond these ratings may cause permanent damage.

(2) VDS (TRAN) allows for surge ratings during non-repetitive events that are < 100 µs (for example start-up, line interruption) and repetitive events that are < 100 ns (for example repetitive leakage inductance spikes).

(3) < 1 µs

5.2. Thermal Resistance

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$R_{θJC}$ [4]	Junction-to-Case		2.36		ºC/W	
$R_{θJA}$ [4]	Junction-to-Ambient		58.57		ºC/W	
T_{sold}	Soldering temperature, wave- & reflow soldering allowed			260	ºC	Reflow MSL1

(4) $R_θ$ measured on DUT mounted on 1 square inch 2 oz Cu (FR4 PCB)

5.3. Electrical Characteristics

Typical conditions: V_{DS} = 400 V, F_{SW} = 1 MHz, T_{AMB} = 25 ºC, I_D = 3.25 A (or specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
GaN FET Characteristics						
I_{DSS}	Drain-Source Leakage Current		0.1	25	µA	V_{DS} = 700 V, V_{GS} = 0 V
I_{DSS}	Drain-Source Leakage Current		5		µA	V_{DS} = 700 V, V_{GS} = 0 V, T_C = 150 ºC
$R_{DS(ON)}$	Drain-Source Resistance		210	294	mΩ	V_{GS} = 6.8 V, I_D = 3.25 A
$V_{GS(th)}$	Gate Threshold Voltage	1.0	1.7	2.8	V	I_D = 4.5 mA, V_{DS} = 0.1 V
V_{SD}	Source-Drain Reverse Voltage		3.2	5	V	V_{GS} = 0 V, I_{SD} = 3.25 A
Q_{RR}	Reverse Recovery Charge		0		nC	
trr	Reverse Recovery time		0		nS	
R_G	Internal Gate Resistance		0.6		Ω	
C_{ISS}	Input Capacitance		54		pF	V_{DS} = 400 V, V_{GS} = 0 V
C_{OSS}	Output Capacitance		15		pF	V_{DS} = 400 V, V_{GS} = 0 V
C_{RSS}	Reverse Transfer Capacitance		0.4		pF	V_{DS} = 400 V, V_{GS} = 0 V
Q_G	Total Gate Charge		1.1		nC	V_{GS} = 0-6 V, I_D = 6.5 A, V_{DS} = 400 V
Q_{GD}	Gate-to-Drain Charge		0.5		nC	V_{GS} = 0-6 V, I_D = 6.5 A, V_{DS} = 400 V
Q_{GS}	Gate-to-Source Charge		0.2		nC	V_{GS} = 0-6 V, I_D = 6.5 A, V_{DS} = 400 V
Q_{OSS}	Output Charge		11.6		nC	V_{GS} = 0 V, V_{DS} = 400 V
$C_{O(er)}$ (5)	Effective Output Capacitance, Energy Related		29		pF	V_{DS} = 400 V, V_{GS} = 0 V
$C_{O(tr)}$ (6)	Effective Output Capacitance, Time Related		20		pF	V_{DS} = 400 V, V_{GS} = 0 V

(5) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

(6) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

5.4. Characteristic Graphs

(GaN FET, T_C = 25 ºC unless otherwise specified)

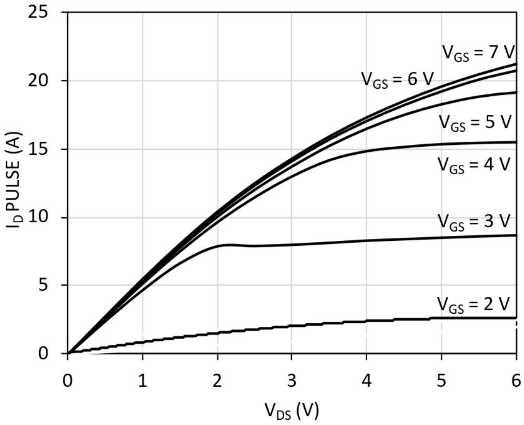


Fig. 1. Pulsed drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at T = 25 °C

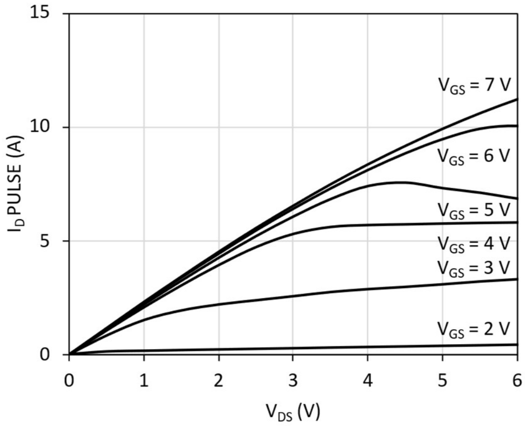


Fig. 2. Pulsed drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at T = 150 °C

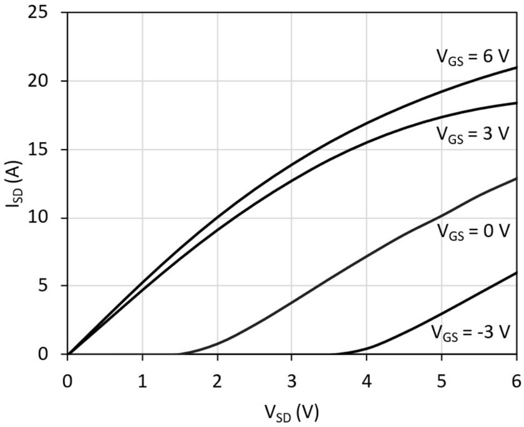


Fig. 3. Source-to-drain reverse conduction voltage at T = 25 °C

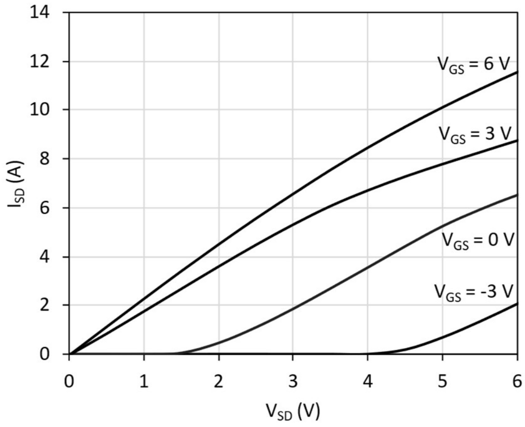


Fig. 4. Source-to-drain reverse conduction voltage at T = 150 °C

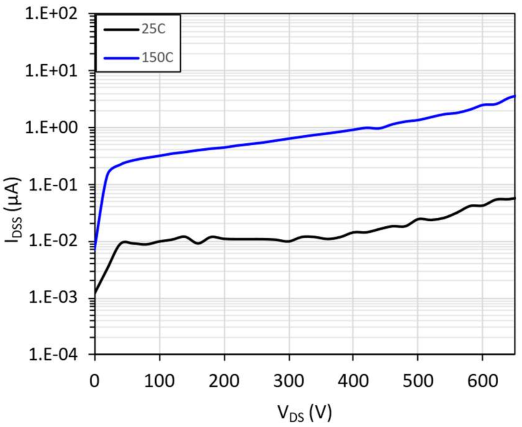


Fig. 5. Drain-to-source leakage current (I_{DSS}) vs. drain-to-source voltage (V_{DS})

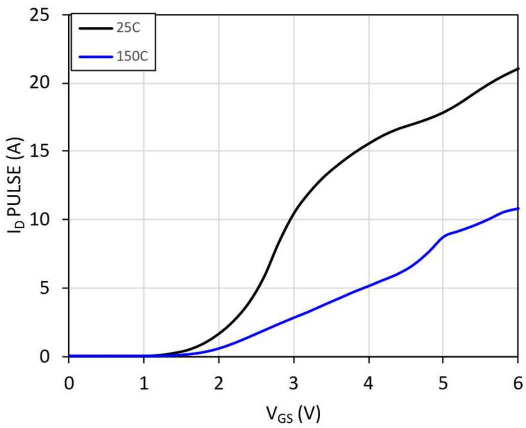


Fig. 6. Pulsed drain current (I_D PULSE) vs. gate-to-source voltage (V_{GS})

Characteristic Graphs (Cont.)

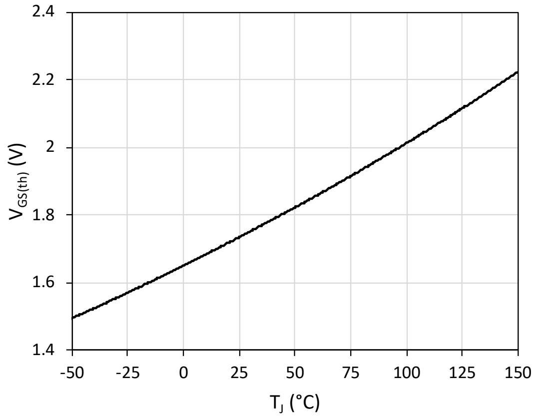


Fig. 7. Gate threshold voltage ($V_{GS(th)}$) vs. junction temperature (T_J)

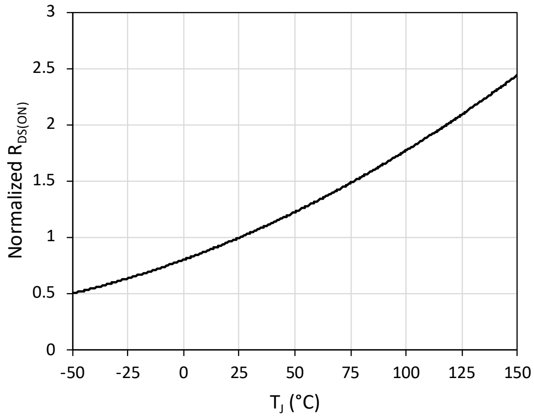


Fig. 8. Normalized on-resistance ($R_{DS(ON)}$) vs. junction temperature (T_J)

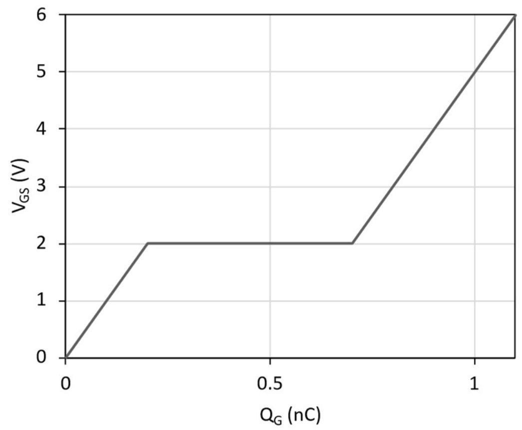


Fig. 9. Gate-to-source voltage (V_{GS}) vs. total gate Charge (Q_G)

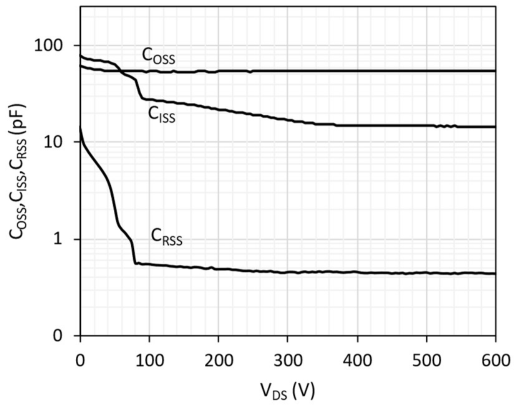


Fig. 10. Input Capacitance (C_{ISS}), Output capacitance (C_{OSS}), Reverse Transfer capacitance (C_{RSS}), vs. drain-to-source voltage (V_{DS})

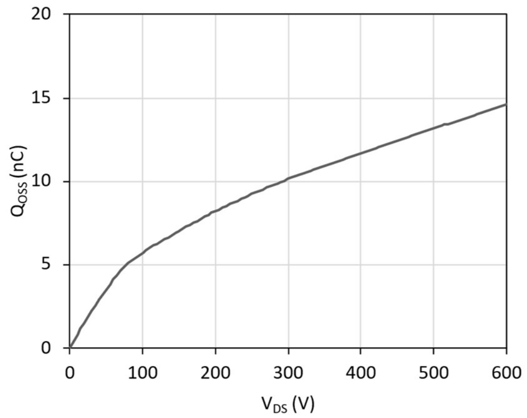


Fig. 11. Charge stored in output capacitance (Q_{OSS}) vs. drain-to-source voltage (V_{DS})

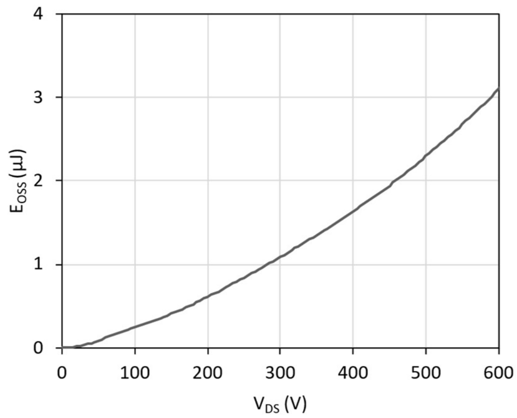


Fig. 12. Energy stored in output capacitance (E_{OSS}) vs. drain-to-source voltage (V_{DS})

Characteristic Graphs (Cont.)

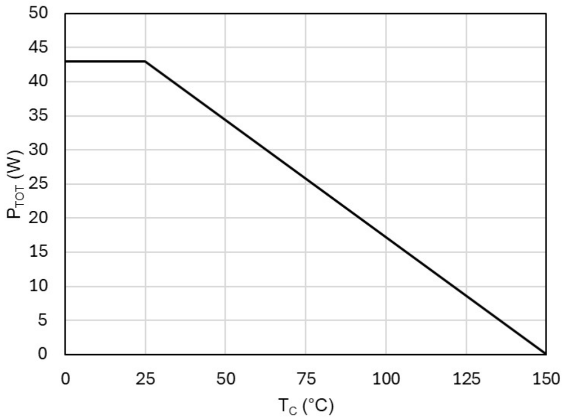


Fig. 13. Power Dissipation (P_{TOT}) vs case temperature

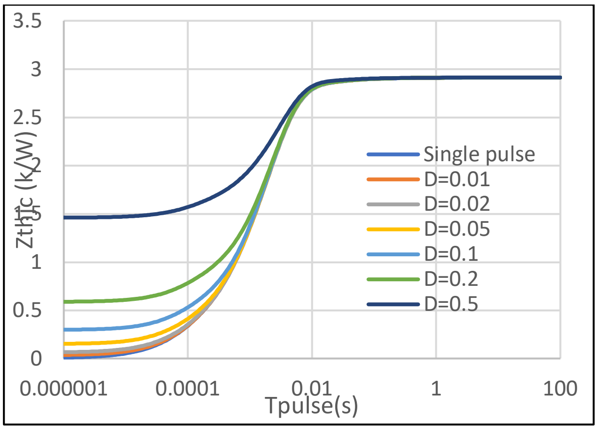


Fig. 14. Max. thermal transient impedance (Z_{thJC}) vs. pulse width (t_P)

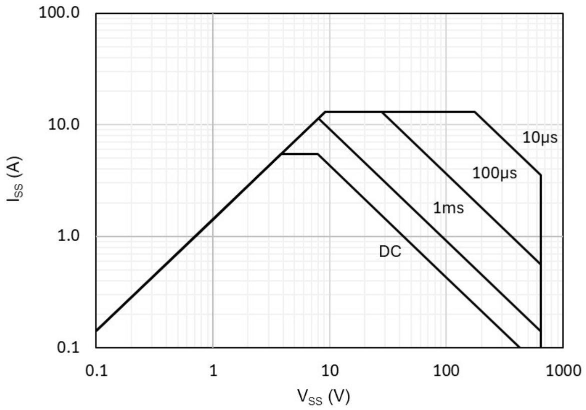
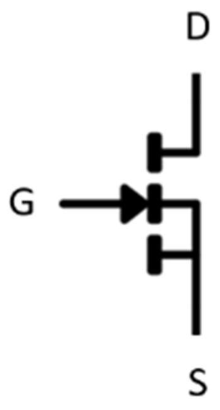


Fig. 15. Safe Operation Area (SOA) @ T_{CASE} = 25°C

6. Pin Configurations and Functions



Package Top View

Pin Number	Pin Name	Description
1	**G**	Gate of power FET
2	**S**	Source of power FET
3	**D**	Drain of power FET

7. Drain-to-Source Voltage Considerations

GaN Power ICs have been designed and tested to provide significant design margin to handle transient and continuous voltage conditions that are commonly seen in single-ended topologies, such as quasi-resonant (QR) flyback applications.

The different voltage levels and recommended margins in a typical QR flyback can be analyzed using Fig. 14. When the device is switched off, the energy stored in the transformer leakage inductance will cause V_{DS} to overshoot to the level of V_{SPIKE}. The clamp circuit should be designed to control the magnitude of V_{SPIKE}. It is recommended to apply an 80% derating from $V_{DS(TRAN)}$ rating (800V) to 700V max for repetitive V_{DS} spikes under the worst case steady-state operating conditions. After dissipation of the leakage energy, the device V_{DS} will settle to the level of the bus voltage plus the reflected output voltage which is defined in Fig. 14 as $V_{PLATEAU}$. It is recommended to design the system such that $V_{PLATEAU}$ follows a typical derating of 80% (560V) from $V_{DS\,(CONT)}$ (700V). Finally, $V_{DS(TRAN)}$ (800V) rating is also provided for events that occur on a non-repetitive basis, such as line surge, lightning strikes, start-up, over-current, short-circuit, load transient, and output voltage transition. 800V $V_{DS(TRAN)}$ ensures excellent device robustness and no-derating is needed for these non-repetitive events, assuming the surge duration is < 100 µs.

For half-bridge based topologies, such as LLC, V_{DS} voltage is clamped to the bus voltage. V_{DS} should be designed such that it meets the $V_{PLATEAU}$ derating guideline (560V).

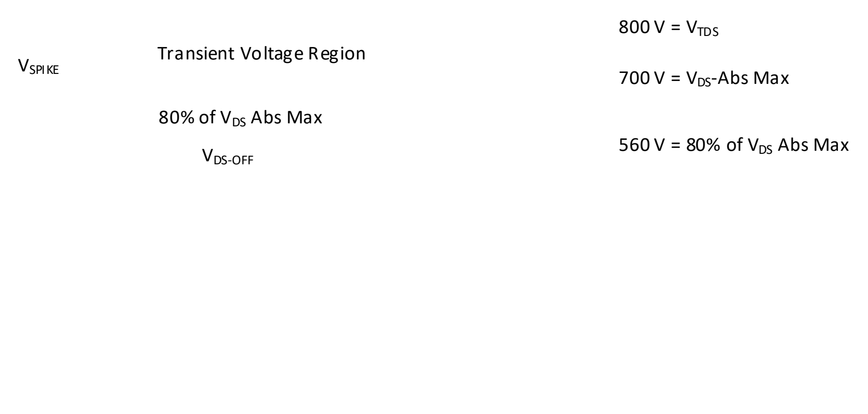


Fig. 16. QR flyback drain-to-source voltage stress diagram

8. PCB Layout Guidelines

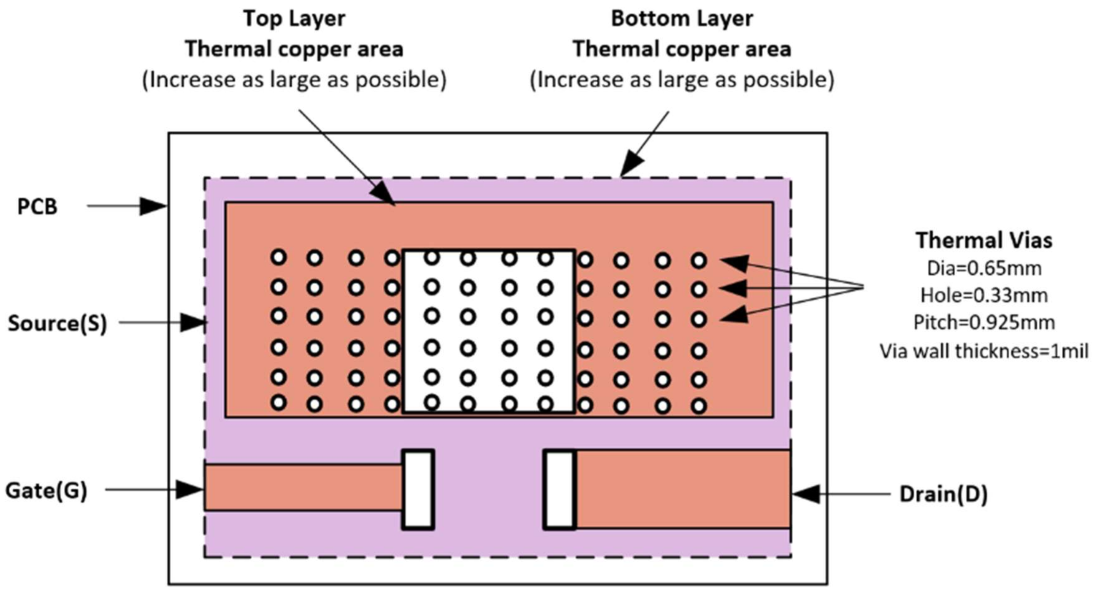
For best electrical and thermal results, the following PCB layout guidelines must be followed:

1) Route all connections on single layer. This allows for large thermal copper areas on other layers.

2) Place large copper areas on and around Source pad.

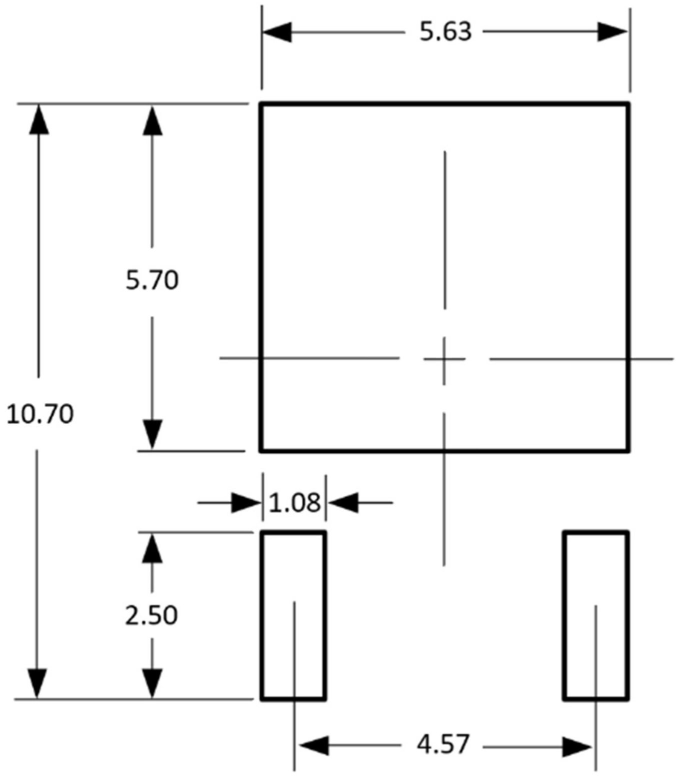
3) Place many thermal vias inside Source pad and inside source copper areas.

4) Place as large as possible copper areas on all other layers (bottom, top, mid1, mid2).



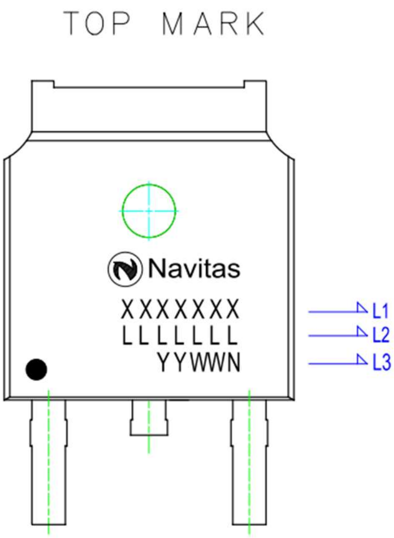
Top View (device on top layer)

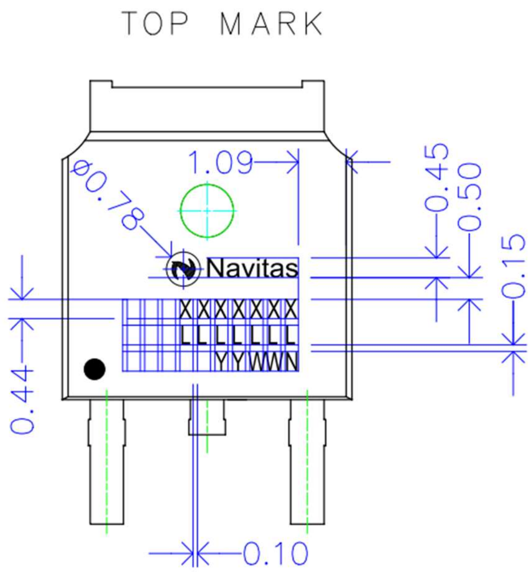
9. Recommended PCB Land Pattern



Top View
All dimensions are in mm

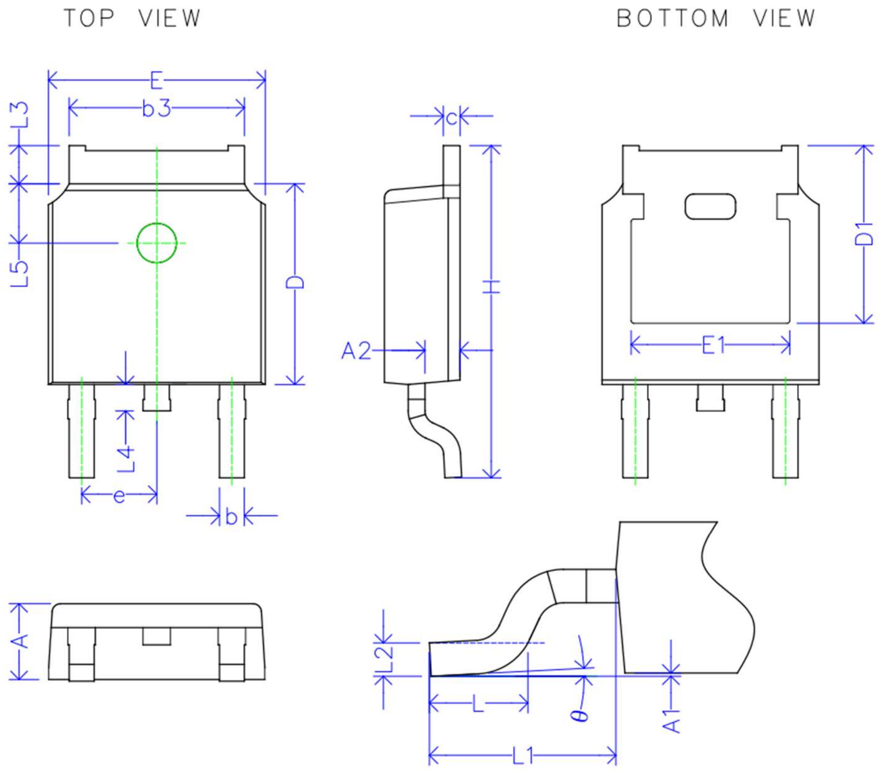
10. TO-252 Package Outline





Marking Line	Marking Symbol	Content Description
L1	XXXXXXX	Part Number : Example : NV6044C
L2	LLLLLLL	Lot Number : Max 7 digits assembly lot number for marking Example : NC31900
L3	YY	Year Code : Last 2 digits of the year Example : 2023, YY=23
	WW	Week Code : 01 - 53
	N	Supplier Site Code : Y = HYME

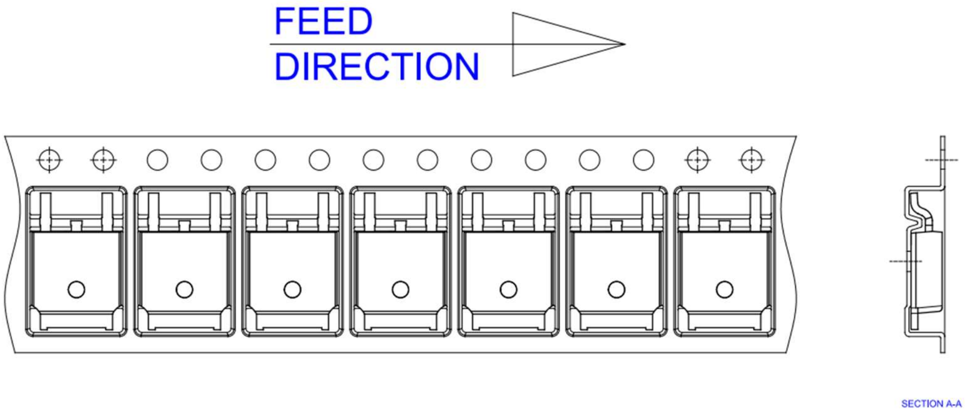
10. TO-252 Package Outline (Cont.)



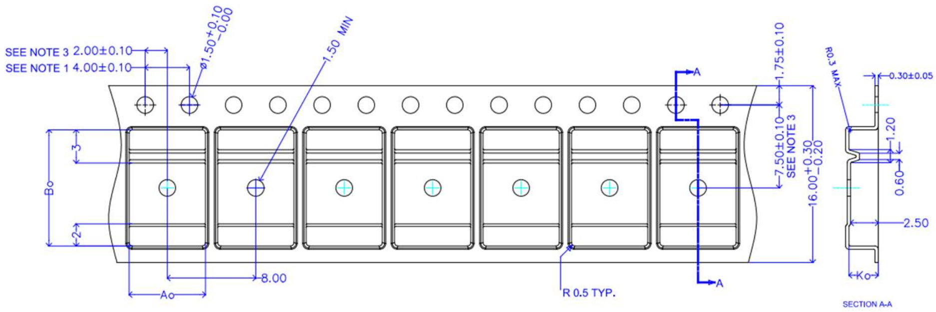
SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.36
A1	0.00	-	0.12
A2	0.97	1.07	1.17
b	0.68	0.78	0.90
b3	5.20	5.33	5.46
c	0.43	0.53	0.61
D	5.98	6.10	6.22
D1		5.30REF	
E	6.40	6.60	6.73
E1	4.63	-	-
e		2.286BSC	
H	9.40	10.10	10.50
L	1.38	1.50	1.75
L1		2.90REF	
L2		0.51BSC	
L3	0.88	-	1.28
L4	0.50	-	1.0
L5	1.65	1.8	1.95
θ°	0°	-	8°

Notes :
1. All dimentions in mm.
2. Reference JEDEC TO-252 AA
3. Do not include mold flash or protrusions.
4. 100% Sn Plating

11. Tape and Reel Dimensions



Reel Quantity			Pin 1 Orientation
Reel Size	Unit qty in reel		2 1 / 3 4 — Pin 1 on quadrant 1
13 "	2500 units		
Leader empty pockets		50	
Trailer empty pockets		140	



Notes	
Ao	6.90 ±0.10
Bo	10.50 ±0.10
Ko	2.70 ±0.10
1. 10 sproket hole pitch cumulative tolerance ±0.2	
2. Camber in compliance with EIA 481	
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.	

12. Ordering Information

Part Number	Operating Temperature Grade	Storage Temperature Range	Package	MSL Rating	Packing (Tape & Reel)
NV6045C	-55 °C to +150 °C T_{CASE}	-55 °C to +150 °C T_{CASE}	TO252	3	2500: 13” Reel

13. Revision History

Date	Status	Notes
Nov 21, 2025	Datasheet	First publication
Dec 2, 2025	Datasheet	Update Pd/Zthjc/SOA charts

Additional Information

Navitas Semiconductor Ltd., 22 Fitzwilliam Square South, Saint Peter's, Dublin, D02 FH68, Republic of Ireland.

Contact info@navitassemi.com