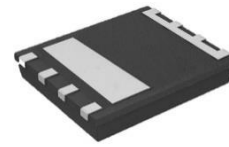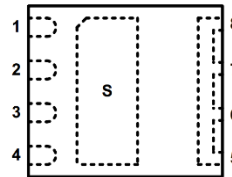# GaNFast™ Power FET

1. Features
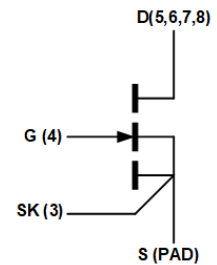
GaNFast™ Power FET

- eMode GaN power FET
- Low 430 mΩ resistance
- 10 MHz switching frequency capability
- Ultra-low gate charge
- Zero reverse recovery charge
- Low output charge
- 800 V Transient Voltage Rating
- 700 V Continuous Voltage Rating
- Source Kelvin (SK) pin for gate noise immunity
- Small, low-profile SMT PQFN
- 5x6 mm PCB footprint
- Minimized package inductance
- Low thermal resistance
- Bottom-side cooled

Environmental

- RoHS, Pb-free, REACH-compliant

PQFN 5x6 mm

Package Outline (Top View)   Simplified Schematic

2. Topologies / Applications

- AC-DC, DC-DC, DC-AC
- QR flyback, ACF, buck, boost, half bridge, full bridge, LLC resonant, Class D, PFC
- Wireless power
- LED lighting
- Solar Micro-inverters
- TV SMPS
- Server, Telecom

3. Description

This GaNFast™ power FET is a high performance eMode GaN FET that achieves excellent high-frequency and high efficiency operation. Features include a simple gate input and a Source Kelvin pin for noise immunity.

This GaN power FET combines the highest dV/dt immunity and industry-standard low-profile, low-inductance, bottom-side cooled SMT QFN packaging to enable designers to achieve simple, quick and reliable solutions.

Navitas' GaN technology extends the capabilities of traditional topologies such as flyback, half-bridge, buck/boost, LLC and other resonant converters to reach MHz+ frequencies with very high efficiencies and low EMI to achieve unprecedented power densities at a very attractive cost structure.

4. Table of Contents

5. Specifications

5.1. Absolute Maximum Ratings[1]

(with respect to Source (pad) unless noted)

SYMBOL	PARAMETER	MAX	UNITS
$V_{DS(TRAN)}$	Transient Drain-to-Source Voltage[2]	800	V
$V_{DS(CONT)}$	Continuous Drain-to-Source Voltage	-7 to +700	V
V_{GS}	Continuous Gate-to-Source Voltage	-10 to +7	V
V_{TGS}	Transient Gate-to-Source Voltage[3]	-20 to +10	V
I_D	Continuous Drain Current (@ T_C = 100ºC)	2.7	A
I_D PULSE	Pulsed Drain Current (10 µs @ T_J = 25°C)	5.4	A
dV/dt	Slew Rate on Drain-to-Source	200	V/ns
P_{TOT}	Power Dissipation (T_C = 25ºC)	25.4	W
T_J	Operating Junction Temperature	-55 to 150	ºC
T_{STOR}	Storage Temperature	-55 to 150	ºC

(1) Absolute maximum ratings are stress ratings; devices subjected to stresses beyond these ratings may cause permanent damage.

(2) $V_{DS (TRAN)}$ rating allows for surge ratings during non-repetitive events that are < 100us (for example start-up, line interruption). $V_{DS (TRAN)}$ rating allows for repetitive events that are < 100ns, with 80% derating required (for example repetitive leakage inductance spikes). Refer to Section 7 for detailed recommended design guidelines.

(3) < 1 µsec

5.2. Thermal Resistance

SYMBOL	PARAMETER	TYP	UNITS
$R_{\theta JC}$[4]	Junction-to-Case	4.93	ºC/W
$R_{\theta JA}$[4]	Junction-to-Ambient	40	ºC/W

(4) R_θ measured on DUT mounted on 1 square inch 2 oz Cu (FR4 PCB)

5.3. Electrical Characteristics

Typical conditions: V_{DS} = 400 V, F_{SW} = 1 MHz, T_{AMB} = 25 ºC, I_D = 1.35 A (or specified)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
	GaN FET Characteristics					
I_{DSS}	Drain-Source Leakage Current		0.2		µA	V_{DS} = 700 V, V_{GS} = 0 V
I_{DSS}	Drain-Source Leakage Current		5		µA	V_{DS} = 700 V, V_{GS} = 0 V, T_C = 150 ºC
I_{GSS}	Gate-Source Leakage Current		35		µA	V_{GS} = 7V, V_{DS} = 0V
$R_{DS(ON)}$	Drain-Source Resistance		430	600	mΩ	V_{GS} = 7 V, I_D = 1.35 A
$V_{GS(th)}$	Gate Threshold Voltage	1	1.7	2.8	V	I_D = 2.3 mA, V_{DS} = 0.1 V
V_{SD}	Source-Drain Reverse Voltage		3.2	5	V	V_{GS} = 0 V, I_{SD} = 1.35 A
T_{ON}	Turn-On Delay Time		4.6		ns	V_{DS}=400V,V_{GS}=5.2V,I_D=1.35A,R_G=10Ω
T_{OFF}	Turn-Off Delay Time		5.4		ns	V_{DS}=400V,V_{GS}=5.2V,I_D=1.35A,R_G=10Ω
T_R	Turn-Off Rise Time		10		ns	V_{DS}=400V,V_{GS}=5.2V,I_D=1.35A,R_G=10Ω
T_F	Turn-On Fall Time		6		ns	V_{DS}=400V,V_{GS}=5.2V,I_D=1.35 A,R_G=10Ω
Q_{RR}	Reverse Recovery Charge		0		nC	
R_G	Internal Gate Resistance		2.5		Ω	
C_{ISS}	Input Capacitance		28		pF	V_{DS} = 400 V, V_{GS} = 0 V
C_{OSS}	Output Capacitance		8		pF	V_{DS} = 400 V, V_{GS} = 0 V
C_{RSS}	Reverse Transfer Capacitance		0.22		pF	V_{DS} = 400 V, V_{GS} = 0 V
Q_G	Total Gate Charge		0.85		nC	V_{GS} = 0-6 V, I_D = 2.7 A, V_{DS} = 400 V
Q_{GD}	Gate-to-Drain Charge		0.26		nC	V_{GS} = 0-6 V, I_D = 2.7 A, V_{DS} = 400 V
Q_{GS}	Gate-to-Source Charge		0.15		nC	V_{GS} = 0-6 V, I_D = 2.7 A, V_{DS} = 400 V
Q_{OSS}	Output Charge		6		nC	V_{GS} = 0 V, V_{DS} = 400 V
$C_{O(er)}$ [5]	Effective Output Capacitance, Energy Related		10		pF	V_{DS} = 400 V, V_{GS} = 0 V
$C_{O(tr)}$ [6]	Effective Output Capacitance, Time Related		14		pF	V_{DS} = 400 V, V_{GS} = 0 V

(5) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

(6) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

5.4. Characteristic Graphs
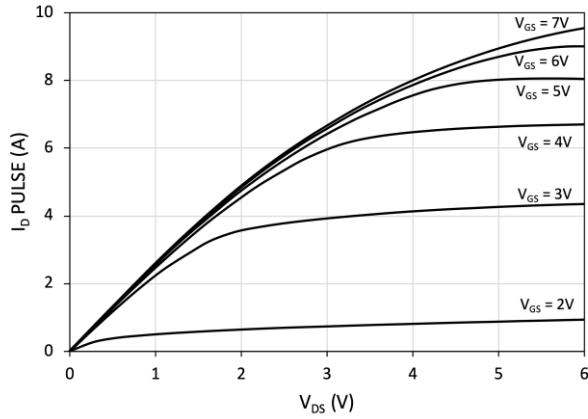
(GaN FET, T_C = 25 ⁰C unless otherwise specified)

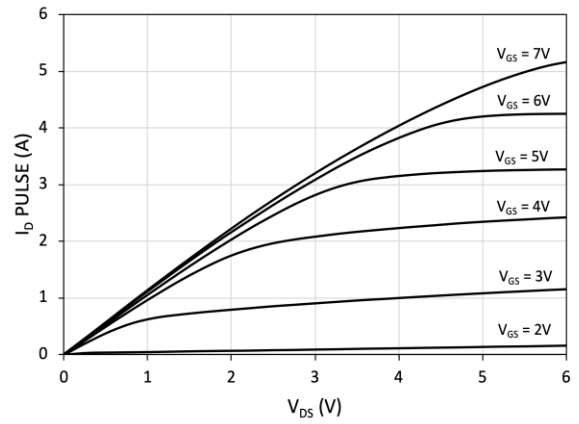Fig. 1. Pulsed drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at T = 25 °C

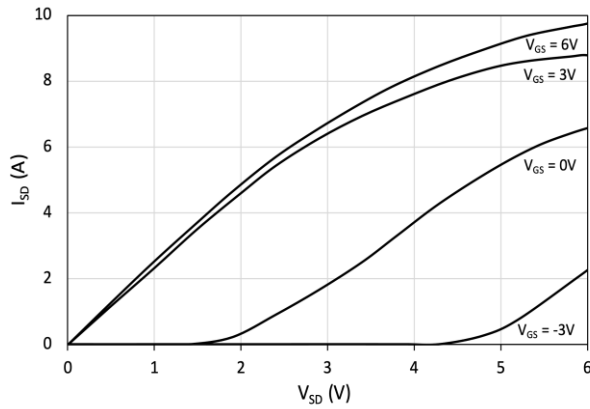Fig. 2. Pulsed drain current (I_D PULSE) vs. drain-to-source voltage (V_{DS}) at T = 150 °C

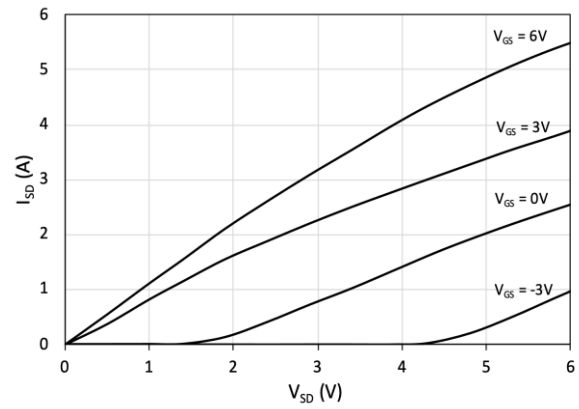Fig. 3. Source-to-drain reverse conduction voltage at T = 25 °C

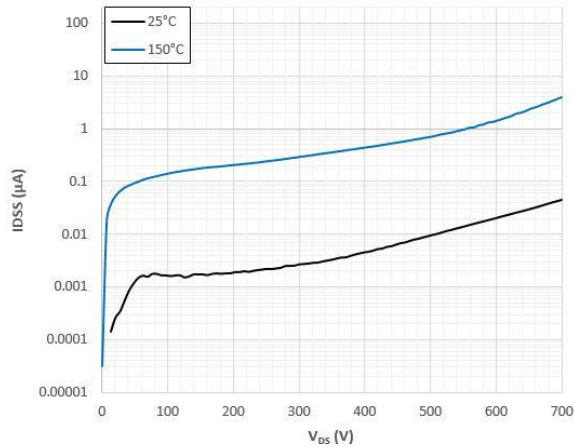Fig. 4. Source-to-drain reverse conduction voltage at T = 150 °C

Fig. 5. Drain-to-source leakage current (I_{DSS}) vs. drain-to-source voltage (V_{DS})
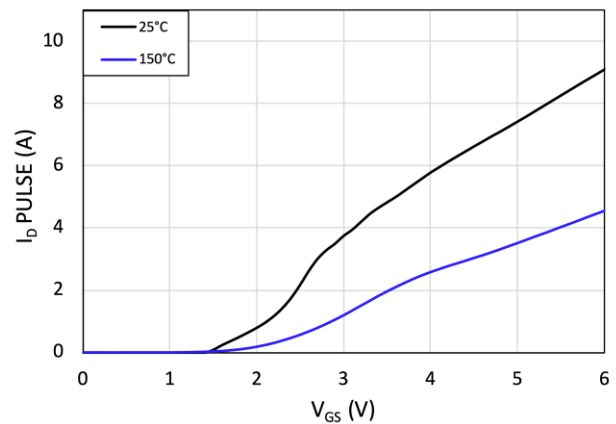

Fig. 6. Pulsed drain current (I_D PULSE) vs. gate-to-source voltage (V_{GS})
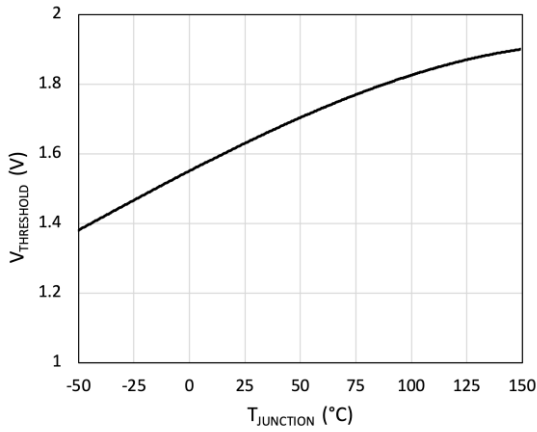
Characteristic Graphs (Cont.)

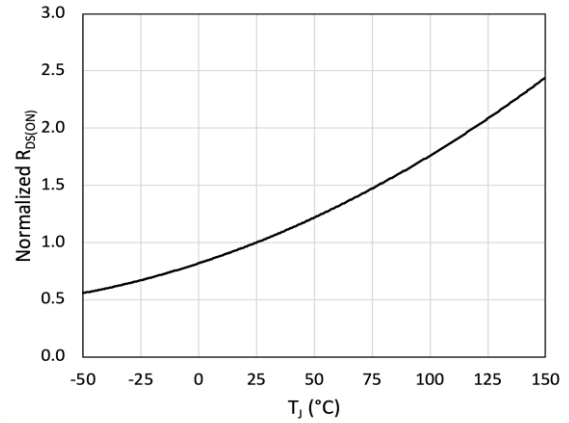Fig. 7. Gate threshold voltage ($V_{GS(th)}$) vs. junction temperature (T_J)

Fig. 8. Normalized on-resistance ($R_{DS(ON)}$) vs. junction temperature (T_J)
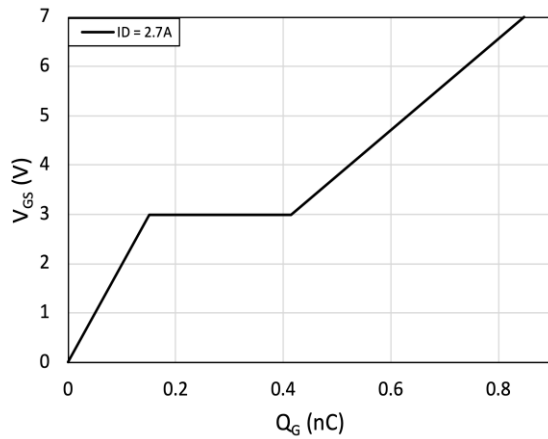

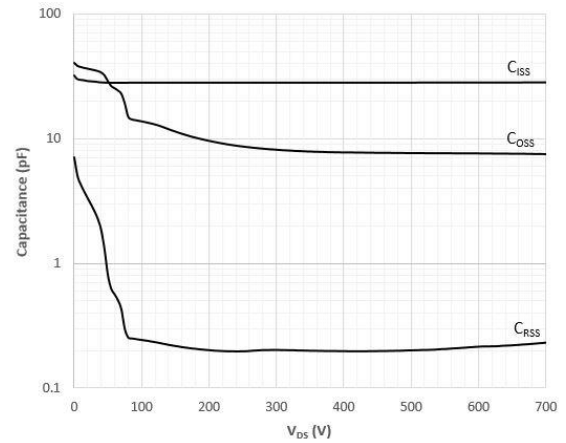Fig. 9. Gate-to-source voltage (V_{GS}) vs. total gate Charge (Q_G)

Fig. 10. Input Capacitance (C_{ISS}), Output capacitance (C_{OSS}), Reverse Transfer capacitance (C_{RSS}), vs. drain-to-source voltage (V_{DS})
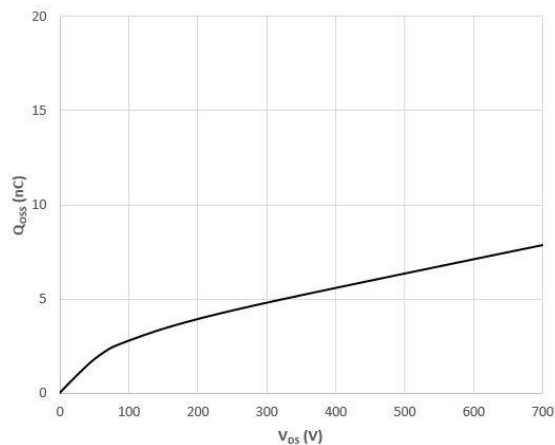

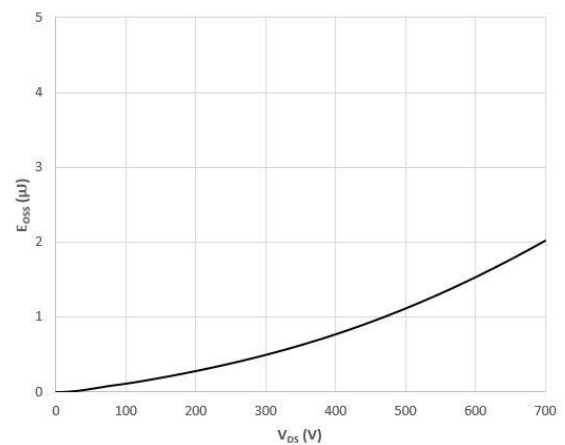Fig. 11. Charge stored in output capacitance (Q_{OSS}) vs. drain-to-source voltage (V_{DS})

Fig. 12. Energy stored in output capacitance (E_{OSS}) vs. drain-to-source voltage (V_{DS})
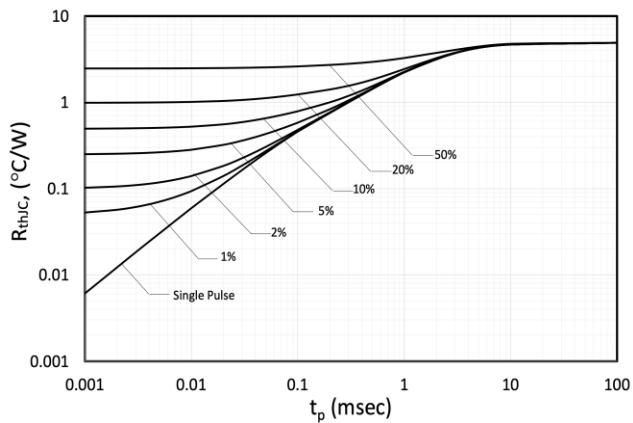
Characteristic Graphs (Cont.)

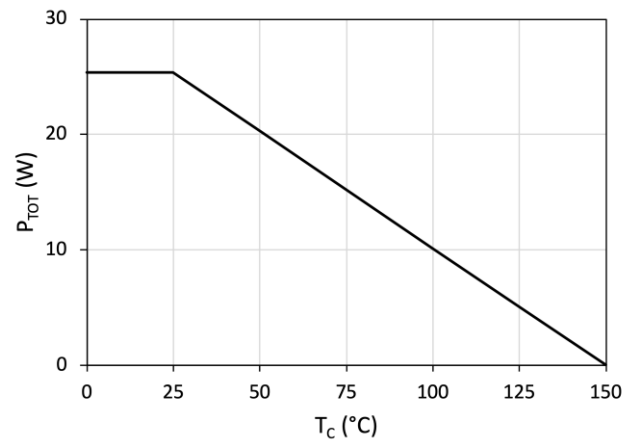Fig. 13. Max. thermal transient impedance (Z_{thJC}) vs. pulse width (t_P)

Fig. 14. Power dissipation (P_{TOT}) vs. case temperature (T_C)

Fig. 15 Safe Operation Area (SOA) @ T_{CASE} = 25°C

6. Pin Configurations and Functions

Package Top View

Pin Number	Pin Name	Description
1, 2	NC	No connection, leave floating or connect to Source PAD
3	SK	Kelvin sense of FET source. Use for driver connection
4	G	Gate of power FET
5, 6, 7, 8	D	Drain of power FET
PAD	S	Source of power FET. Metal pad on bottom of package.

7. Drain-to-Source Voltage Considerations

GaN Power ICs have been designed and tested to provide significant design margin to handle transient and continuous voltage conditions that are commonly seen in single-ended topologies, such as quasi-resonant (QR) flyback applications. The different voltage levels and recommended margins in a typical QR flyback can be analyzed using Fig. 16. When the device is switched off, the energy stored in the transformer leakage inductance will cause V_{DS} to overshoot to the level of V_{SPIKE}. The clamp circuit should be designed to control the magnitude of V_{SPIKE}. After dissipation of the leakage energy, the device V_{DS} will settle to the level of the bus voltage plus the reflected output voltage which is defined in Fig. 16 as V_{DS-OFF}.

- For repetitive events, 80% derating should be applied from $V_{DS\,(TRAN)}$ rating (800V) to 640V max under the worst case operating conditions.
- It is recommended to design the system such that V_{DS-OFF} is derated 80% from the $V_{DS(CONT)}$ (700V) max rating to 560V.
- For half-bridge based topologies, such as LLC, V_{DS} voltage is clamped to the bus voltage. V_{DS} should be designed such that it meets the V_{DS-OFF} derating guideline (560V).
- Non-repetitive events are infrequent, one-time conditions such as line surge, ESD, and lightning. No derating from the $V_{DS(TRAN)}$ rating (800V) is needed for non-repetitive V_{SPIKE} durations < 100 µs. The $V_{DS(TRAN)}$ rating (800V) allows for repetitive events that are <100ns, with 80% derating required (for example repetitive leakage inductance spikes).
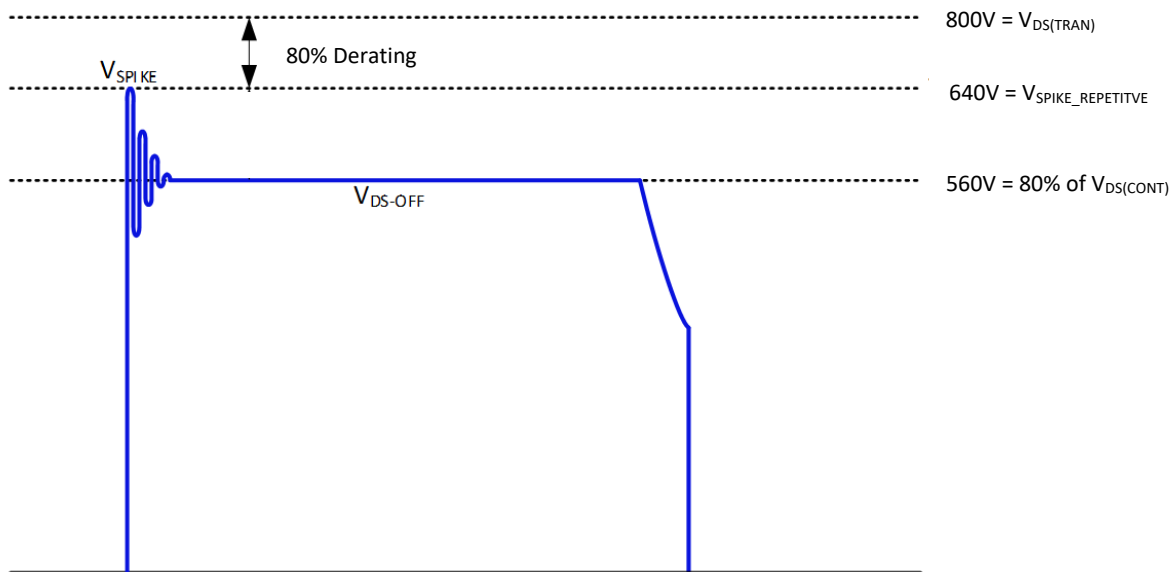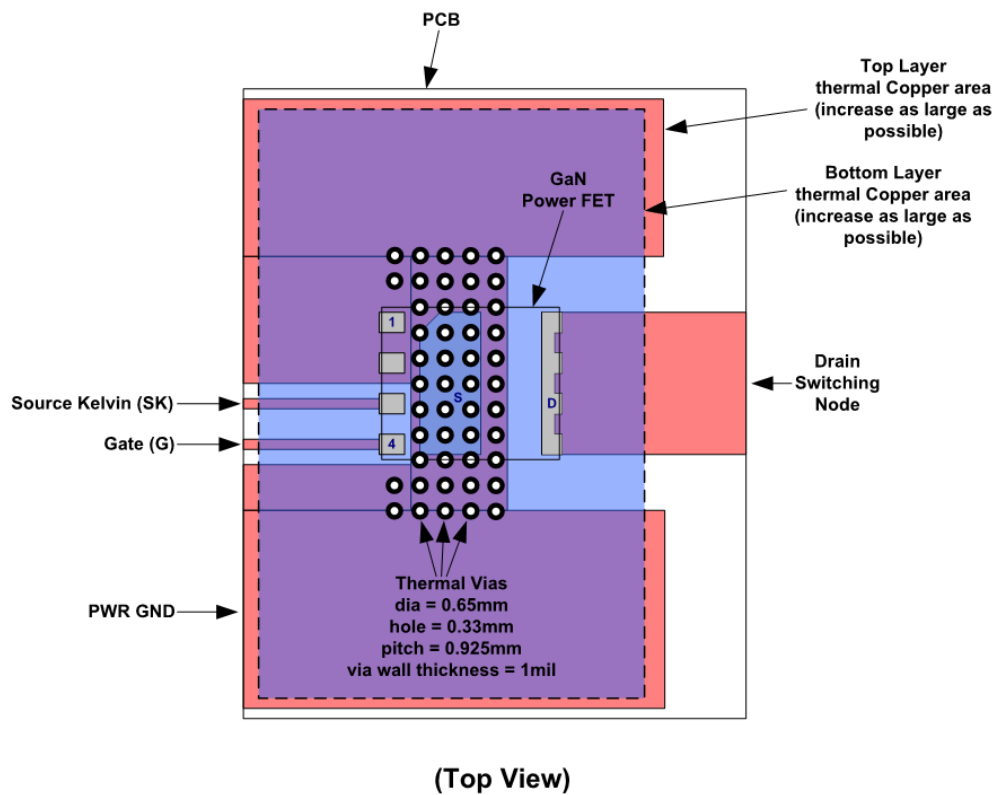

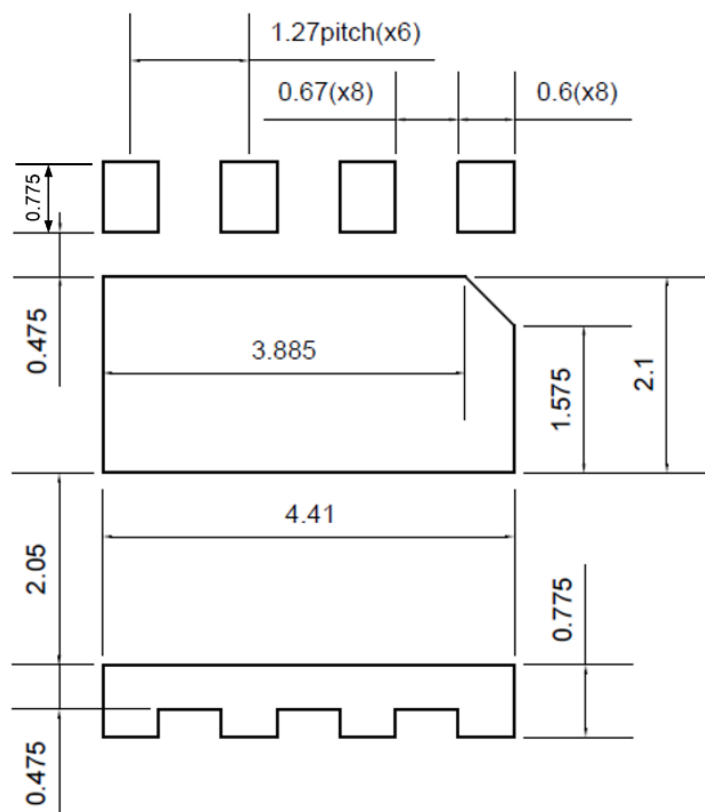Fig. 16. QR flyback drain-to-source voltage stress diagram

8. PCB Layout Guidelines

For best electrical and thermal results, the following PCB layout guidelines must be followed:
1) Route all connections on single layer. This allows for large thermal copper areas on other layers.
2) Place large copper areas on and around Source pad.
3) Place many thermal vias inside Source pad and inside source copper areas.
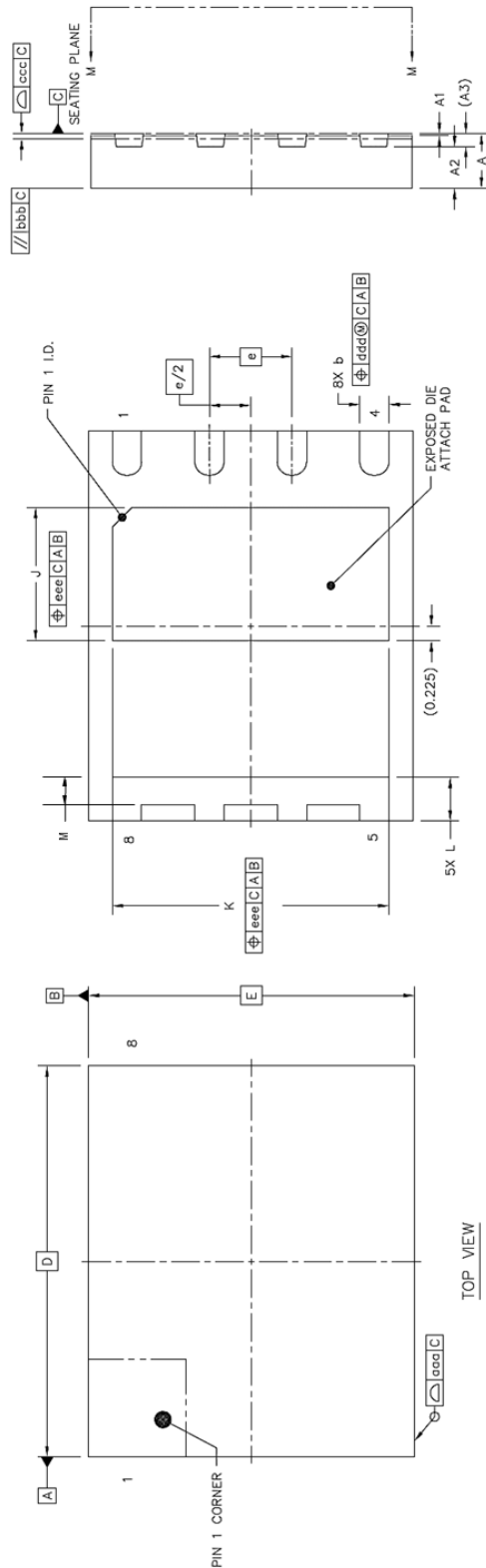4) Place large as possible copper areas on all other layers (bottom, top, mid1, mid2).

(Top View)

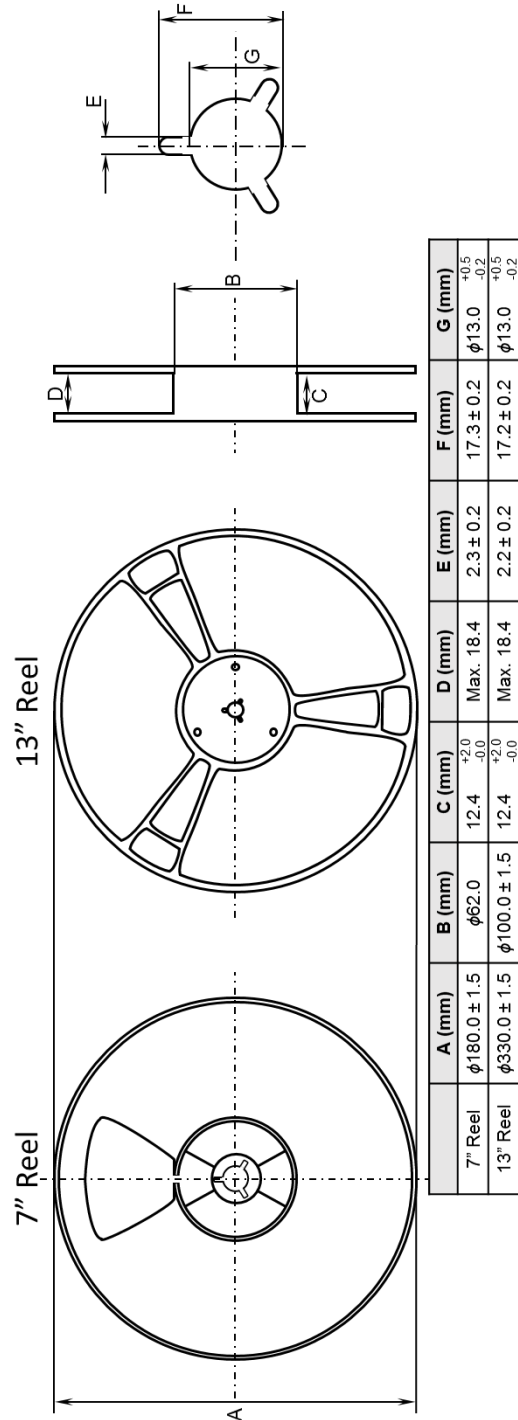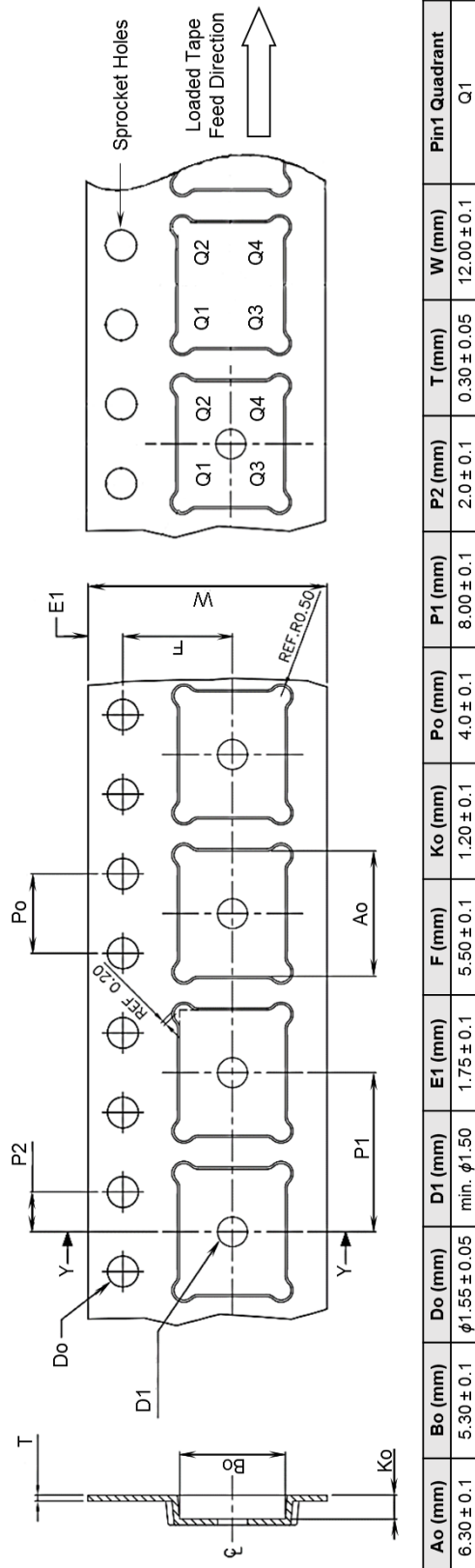## 9. Recommended PCB Land Pattern

Top View

All dimensions are in mm

10. QFN Package Outline

SYMBOL			MIN	NOM	MAX	
A			0.8	0.85	0.9	TOTAL THICKNESS
A1			0	0.035	0.05	STAND OFF
A3			---	0.65	---	MOLD THICKNESS
A3				0.203 REF		L/F THICKNESS
B			0.4	0.45	0.5	LEAD WIDTH
D	X			6 BSC		BODY SIZE
E	Y			5 BSC		
e				1.27 BSC		LEAD PITCH

SYMBOL		MIN	NOM	MAX	
J	X	1.95	2.05	2.15	EP SIZE
K	Y	4.16	4.26	4.36	
L		0.625	0.675	0.725	LEAD LENGTH
M			0.43		MERGED LEAD LENGTH
aaa			0.1		PACKAGE EDGE TOLERANCE
bbb			0.1		MOLD FLATNESS
ccc			0.08		COPLANARITY
ddd			0.1		LEAD OFFSET
eee			0.1		EXPOSED PAD OFFSET

11. Tape and Reel Dimensions

Ao (mm)	Bo (mm)	Do (mm)	D1 (mm)	E1 (mm)	F (mm)	Ko (mm)	Po (mm)	P1 (mm)	P2 (mm)	T (mm)	W (mm)	Pin1 Quadrant
6.30±0.1	5.30±0.1	φ1.55±0.05	min. φ1.50	1.75±0.1	5.50±0.1	1.20±0.1	4.0±0.1	8.00±0.1	2.0±0.1	0.30±0.05	12.00±0.1	Q1

	A (mm)	B (mm)	C (mm)	D (mm)	E (mm)	F (mm)	G (mm)
7" Reel	φ180.0±1.5	φ62.0	12.4 +2.0 -0.0	Max. 18.4	2.3±0.2	17.3±0.2	φ13.0 +0.5 -0.2
13" Reel	φ330.0±1.5	φ100.0±1.5	12.4 +2.0 -0.0	Max. 18.4	2.2±0.2	17.2±0.2	φ13.0 +0.5 -0.2

12. Ordering Information

Part Number	Operating Temperature Grade	Storage Temperature Range	Package	MSL Rating	Packing (Tape & Reel)
NV6012C-RA	-55 °C to +150 °C T_{CASE}	-55 °C to +150 °C T_{CASE}	5 x 6 mm QFN	3	1,000 : 7" Reel
NV6012C	-55 °C to +150 °C T_{CASE}	-55 °C to +150 °C T_{CASE}	5 x 6 mm QFN	3	5,000 : 13" Reel

13. Revision History

Date	Status	Notes
Jul. 13, 2023	PRELIMINARY	First publication
Dec. 11, 2023	FINAL	Datasheet updated with final graphs and content
Jan. 15, 2023	FINAL	Updated Abs Max section, updated VDS considerations section
June 5, 2024	FINAL	Updated VDScont, electrical data, characteristic graphs, VDS considerations

Additional Information

Navitas Semiconductor Ltd., 22 Fitzwilliam Square South, Saint Peter's, Dublin, D02 FH68, Republic of Ireland.

Contact info@navitassemi.com