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AK4940

24-bit Mono CODEC with Analog Direct Path

1. General Description

The AK4940 is an audio CODEC with gain amplifier for microphone and analog direct path. It is ideal for data communication modules (DCM). The AK4940 is available in small 24-pin QFN (4 mm × 4 mm, 0.5 mm pitch) package.

2. Features

□ **ADC: 24-bit Monaural ADC (with Microphone Gain Amplifier)**
- **Sampling Frequency: fs = 8kHz to 48kHz**
- **Analog Gain Amplifier for Microphones (-6 to 27dB, 3dB step)**
- **Analog Input Selector**
- **Differential Input/ Single-ended Input/ Pseudo Differential Input**
- **ADC Characteristics:**
  S/(N+D):80dB, S/N:90dB (fs=48kHz, Differential Input, MIC Gain=0dB)
- **Digital Volume (+24 to -103dB, 0.5dB Step, Mute)**
- **Digital HPF for DC Offset Cancelling**
- **Two Kinds of Digital Filters: Sharp Roll-Off Filter, Voice Filter**

□ **DAC: 24-bit Monaural DAC (with Line Amplifier)**
- **Sampling Frequency: fs=8kHz to 48kHz**
- **Differential Output/ Pseudo Differential Output x2, Single-ended Output x1**
- **DAC Characteristics:**
  S/(N+D): 80dB, S/N: 90dB (fs=48kHz, Single-ended Output)
- **Digital Volume (+12 to -115dB, 0.5dB Step, Mute)**
- **Digital Filter: Sharp Roll-Off Filter**

□ **Analog Direct Path**
- **Switch Resistance: 300Ω (max.)**
- **Signal Amplitude 3.0Vpp (max.)**

□ **Audio Serial Interface:**
- **Data Code: MSB First, 2's complement**
- **ADC: MSB justified / LSB justified / I²S / PCM Long Format / PCM Short Format**
- **DAC: MSB justified / LSB justified / I²S / PCM Long Format / PCM Short Format**

□ **Slave Operation**
□ **PLL (Reference Clock BICK)**
□ **µP Interface: I²C-bus (400kHz, Fast Mode)**
□ **Power Supply:**
- **Analog** **AVDD: 3.0 to 3.6V (typ. 3.3V)**
- **Digital I/F** **TVDD: 1.7 to 3.6V (typ. 3.3V)**

□ **Operation Temperature Range: -40°C to 105°C**
□ **Package: 24-pin QFN (4mm x 4mm, 0.5mm pitch)**

3. Table of Contents

4. Block Diagram

■ Block Diagram

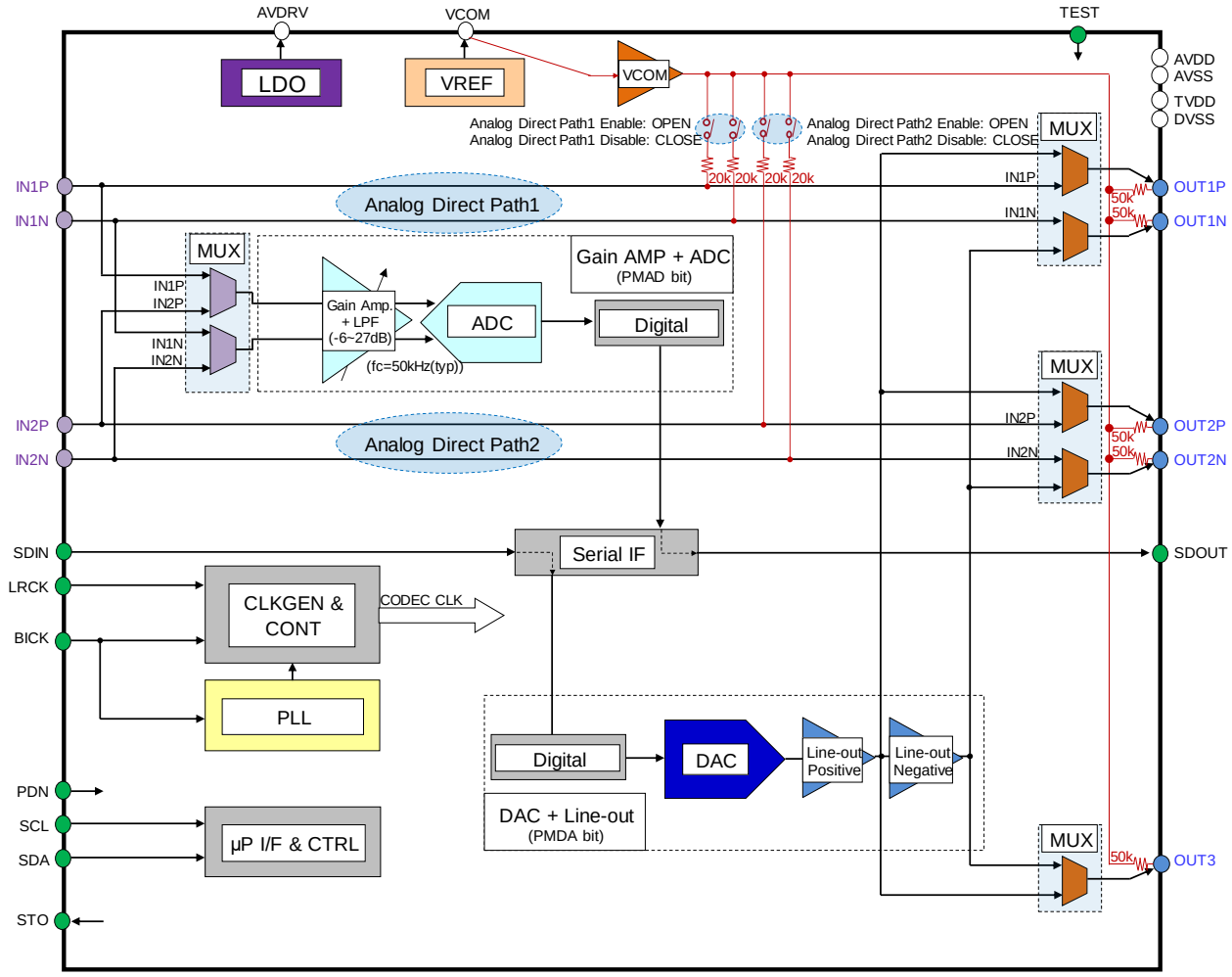


Figure 1. Block Diagram

■ Block Functions

Block	Function
VREF	Generate reference voltage VCOM (50% AVDD typ.).
LDO	Generate 1.2V (typ.) power supply for internal digital circuits.
VCOM Amp.	Supply reference voltage to internal analog circuits.
MUX	Select an analog signal from multiple analog signals.
Analog Direct Path1/2	Connect analog input pin to analog output pin.
Gain AMP + ADC	Amplify analog input signal and Convert to digital data.
DAC + Line-out	Convert digital input data to analog signal and output it.
PLL	Multiply input BICK and generate internal master clock.
CLKGEN & CONT	Generate clocks for ADC block and DAC block operation.
µP I/F & CTRL	I^2C interface and control register for register settings
Serial IF	Audio serial data input/output interface

5. Pin Configurations and Functions

■ Pin Configurations

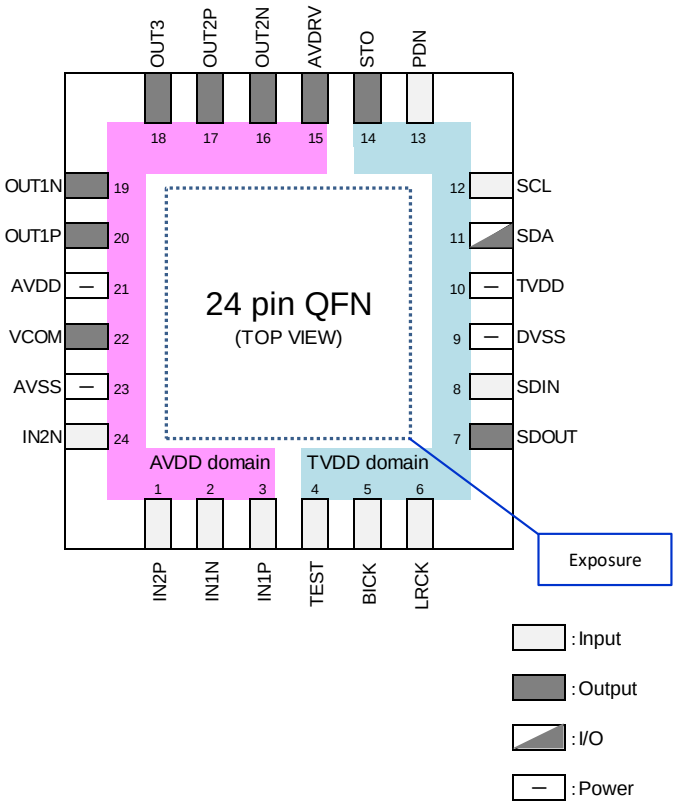


Figure 2. Pin Configuration

■ Pin Functions

No.	Pin Name	I/O	Functions	Power-down Status
1	IN2P	I	Analog Input Channel 2 Positive Differential: Analog Positive Signal Single-ended, Pseudo-differential: Analog Signal	Hi-Z
2	IN1N	I	Analog Input Channel 1 Negative Differential: Analog Negative Signal Single-ended: Connect a 10μF capacitor between this pin and AVSS. Pseudo-differential: Connect a 10μF capacitor between this pin and signal ground.	Hi-Z
3	IN1P	I	Analog Input Channel 1 Positive Differential: Analog Positive Signal Single-ended, Pseudo-differential: Analog Signal	Hi-Z
4	TEST	I	TEST Mode Control Connect to DVSS. This pin has 25kΩ pull-down resister.	Hi-Z
5	BICK	I	Serial Bit Clock Input	Hi-Z
6	LRCK	I	LR Channel Select Clock Input	Hi-Z
7	SDOUT	O	Audio Serial Data Output	Pulled-down by 50kΩ
8	SDIN	I	Audio Serial Data Input	Hi-Z
9	DVSS	-	Digital Ground	-
10	TVDD	-	Digital I/O Power Supply, 1.7 - 3.6V	-
11	SDA	I/O	I^2C Bus Data	Hi-Z
12	SCL	I	I^2C Bus Clock Input	Hi-Z
13	PDN	I	Power Down "L": Power Down, "H": Normal Operation	Hi-Z
14	STO	O	Internal Status Output	Pulled-down by 50kΩ
15	AVDRV	O	LDO Output Connect a 2.2μF (±30%) capacitor between this pin and DVSS. This pin must not be connected to external circuit. This capacitor must be low ESR (Ex. Ceramic Capacitor). The 2.2μF (±30%) includes the bias effect and the fluctuation with temperature.	Pulled-down by 110Ω
16	OUT2N	O	Analog Output Channel 2 Negative Analog Direct Path: IN2N Signal DAC Line Output: Inverted Signal or VCOM	Hi-Z
17	OUT2P	O	Analog Output Channel 2 Positive Analog Direct Path: IN2P Signal DAC Line Output: Non-Inverted Signal	Hi-Z
18	OUT3	O	DAC Line Output (Single-ended)	Hi-Z
19	OUT1N	O	Analog Output Channel 1 Negative Analog Direct Path: IN1N Signal DAC Line Output: Inverted Signal or VCOM	Hi-Z
20	OUT1P	O	Analog Output Channel 1 Positive Analog Direct Path: IN1P Signal DAC Line Output: Non-Inverted Signal	Hi-Z
21	AVDD	-	Analog Power Supply, LDO Power Supply, 3.0 - 3.6V	-

No.	Pin Name	I/O	Functions	Power-down Status
22	VCOM	O	Analog Block Common Voltage Output Connect 2.2μF (±30%) capacitor between this pin and AVSS. This pin must not be connected to external circuit. This capacitor must be low ESR. (Ex. Ceramic Capacitor) The 2.2μF (±30%) includes the bias effect and the fluctuation with temperature.	Pulled-down by 500Ω
23	AVSS	-	Analog Ground	-
24	IN2N	I	Analog Input Channel 2 Negative Differential: Analog Negative Signal Single-ended: Connect a 10μF capacitor between this pin and AVSS. Pseudo-differential: Connect a 10μF capacitor between this pin and signal ground.	Hi-Z
-	Exposed Pad	-	Solder to AVSS ground plane.	-

■ Handing of Unused Pin

Unused I/O pins must be connected appropriately.

Table 1. Handing of Unused Pins

Classification	Pin Name	Setting
Analog	IN2P, IN1N, IN1P, OUT2N, OUT2P, OUT3, OUT1N, OUT1P, IN2N	Open
Digital	STO, SDOUT	Open
	LRCK, BICK, SDIN, TEST	Connect to DVSS

6. Absolute Maximum Ratings

(AVSS=DVSS=0V; Note 1)

Parameter	Symbol	Min.	Max.	Unit
Power Supply Voltage				
Analog	AVDD	–0.3	4.3	V
Digital(I/F)	TVDD	–0.3	4.3	V
Difference (AVSS, DVSS) (Note 1)	ΔGND	–0.3	0.3	V
Input Current (Except power supply pins)	IIN	—	±10	mA
Analog Input Voltage (Note 2)	VINA	–0.3	(AVDD+0.3) or 4.3	V
Digital Input Voltage (Note 3)	VIND	–0.3	(TVDD+0.3) or 4.3	V
Ambient Temperature	Ta	–40	105	°C
Storage Temperature	Tstg	–65	150	°C

Note 1. All voltages are with respect to ground. AVSS and DVSS must be connected to the same analog ground plane.

Note 2. IN1P, IN1N, IN2P, IN2N pins.
The maximum analog input voltage is lower value between (AVDD+0.3V) and 4.3V.

Note 3. PDN, LRCK, BICK, SDIN, SDA(I), SCL pins
The maximum digital input voltage is lower value between (TVDD+0.3V) and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(AVSS=DVSS=0V; Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply					
Analog	AVDD	3.0	3.3	3.6	V
Digital(I/F)	TVDD	1.7	3.3	3.6	V
Difference	AVDD – TVDD	–0.3	-	3.6	V

Note 4. The AK4940 must be powered up when the PDN pin = “L”. The power up sequence between AVDD and TVDD is not critical. Set the PDN pin to “H” after all powers are supplied and stabilized.

Note 5. Do not turn off the power supply of the AK4940 with the power supply of the surrounding device turned on. When using the I^2C interface, pull-up resistors of SDA and SCL pins should be connected to TVDD or less voltage.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

8. Analog Characteristics

■ Gain Amplifier

(Ta=25°C; AVDD=TVDD=3.3V; AVSS=DVSS=0V)

	Parameter		Min.	Typ.	Max.	Unit
Gain Amp.	Input Impedance (Differential) IN1P, IN1N, IN2P, IN2N pins		14	20	26	kΩ
	Input Impedance (Single-ended, Pseudo Differential) IN1P, IN2P pins IN1N, IN2N pins		 16 900	 24 1300	 31 1700	 kΩ kΩ
	Gain	MGN[3:0]bits=0h (0000)	–7.5	–6	–4.5	dB
		MGN [3:0]bits=1h (0001)	–4.5	–3	–1.5	
		MGN [3:0]bits=2h (0010)	–1.5	0	1.5	
		MGN [3:0]bits=3h (0011)	1.5	3	4.5	
		MGN [3:0]bits=4h (0100)	4.5	6	7.5	
		MGN [3:0]bits=5h (0101)	7.5	9	10.5	
		MGN [3:0]bits=6h (0110)	10.5	12	13.5	
		MGN [3:0]bits=7h (0111)	13.5	15	16.5	
		MGN [3:0]bits=8h (1000)	16.5	18	19.5	
		MGN [3:0]bits=9h (1001)	19.5	21	22.5	
		MGN [3:0]bits=Ah (1010)	22.5	24	25.5	
		MGN [3:0]bits=Bh (1011)	25.5	27	28.5	
		MGN [3:0]bits= Others	Not Available			

■ Gain Amplifier + ADC

(Ta=25°C; AVDD=TVDD=3.3V; AVSS=DVSS=0V; Signal Frequency=1kHz; 24bit Data; BICK=64fs; fs=48kHz; Measurement Frequency BW=20Hz ~ 20kHz; Amp Gain=0dB)

	Parameter		Min.	Typ.	Max.	Unit
Gain AMP + ADC	Resolution		-	-	24	bit
	Differential Input					
	Input Full-scale Voltage (Note 6)	Sharp Roll-off Filter (VOAD bit="0")	±2.0	±2.2	±2.4	Vpp
		Voice Filter (VOAD bit="1")	±2.07	±2.28	±2.48	Vpp
	S/(N+D)	–1dBFS	72	80	-	dB
	Dynamic Range	–60dBFS, A-weighted	82	90	-	dB
	S/N	A-weighted	82	90	-	dB
	PSRR	(Note 7)	-	50	-	dB
	CMRR	(Note 8)	60	80	-	dB
	Single-ended Input, Pseudo Differential Input					
	Input Full-scale Voltage (Note 6)	Sharp Roll-off Filter (VOAD bit="0")	2.0	2.2	2.4	Vpp
		Voice Filter (VOAD bit="1")	2.07	2.28	2.48	Vpp
	S/(N+D)	–1dBFS	72	80	-	dB
	Dynamic Range	–60dBFS, A-weighted	82	90	-	dB
	S/N	A-weighted	82	90	-	dB
	PSRR	(Note 7)	-	50	-	dB
	CMRR	(Note 9)	55	75	-	dB

Note 6. Full-scale voltage is proportional to AVDD.

Note 7. PSRR is referred to AVDD and TVDD with 1kHz, 100 mVpp sine wave.

Note 8. CMRR is referred to INnP and INnN (n= 1, 2) with 1kHz, 100 mVpp in-pahse sine wave. These are relative values to the output level when inputting 1kHz, 100mVpp sine wave.

Note 9. Pseudo differential Input. CMRR is referred to INnP and INnN (n= 1, 2) with 1kHz, 100 mVpp sine wave. These are relative values to the output level when inputting 1kHz, 100mVpp sine wave.

■ DAC + Lineout

(Ta=25°C; AVDD=TVDD=3.3V; AVSS=DVSS=0V; Signal Frequency=1kHz; 24bit Data; BICK=64fs; fs=48kHz; Measurement Frequency BW=20Hz ~ 20kHz)

	Parameter		Min.	Typ.	Max.	Unit
DAC + Line-out	Resolution		-	-	24	bit
	Output Full-scale Voltage (Note 10)	Differential (Note 11)	±2.55	±2.76	±3.11	Vpp
		Single Ended, Pseudo Differential (Note 12)	2.55	2.76	3.11	Vpp
	S/(N+D)	0dBFS	72	80	-	dB
	Dynamic Range	–60dBFS, A-weighted	82	90	-	dB
	S/N	A-weighted	82	90		dB
	Channel Gain Mismatch (Note 13)		-	0.0	0.5	dB
	Load Resistance (Note 14)		10	-	-	kΩ
	Load Capacitance		-	-	30	pF
	PSRR (Note 7)		-	50	-	dB

Note 7. PSRR is referred to AVDD and TVDD with 1kHz, 100 mVpp sine wave.
Note 10. Full-scale voltage is proportional to AVDD.
Note 11. Output voltage between OUTxP pin and OUTxN pin (x = 1, 2) in differential output mode (OUTNSEL bit = “0”).
Note 12. Output voltage at the OUT1P, OUT1N, OUT2P, OUT2N and OUT3 pins in single-ended ouptut mode or pseudo diferential output mode (OUTNSEL bit = “1”).
Note 13. Channel gain mismatch between the OUT1P pin and OUT1N pin, the OUT2P pin and OUT2N pin when 0dBF is output..
Note 14. against AC load

■ Analog Direct Path

(Ta=25°C; AVDD=TVDD=3.0~3.6V; AVSS=DVSS=0V; Signal Frequency=1kHz; Measurement Frequency BW=20Hz ~ 20kHz)

	Parameter	Min.	Typ.	Max.	Unit
Analog Switch	Input PIN to Output PIN				
	Pin to Pin Impedance	-	-	300	Ω
	Signal Amplitude (Note 15)	-	-	3.0	Vpp
	Load Resistance (Note 14)	10	-	-	kΩ

Note 15. AC signal amplitude after reducing DC signal via Input capacitor.

■ Consumption Current

(Ta=25°C; AVDD: Typ.=3.3V, Max.=3.6V; TVDD: Typ.=3.3V, Max.=3.6V; AVSS=TVSS=0V; fs=48kHz, ADC ON; DAC ON; Line-out ON; C_L=20pF(Digital Output); R_L=10kΩ(Line Output))

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Current Normal Operation, PDN Pin= “H”	AVDD	-	11.4	20	mA
	TVDD	-	1	2	mA
Power Supply Current Power Down State, PDN Pin= “L”	AVDD	-	1	10	μA
	TVDD	-	1	10	μA

Note 16. Consumption current depends on operation frequency.

9. Digital Filter Characteristics

■ ADC

(Ta= -40~105°C; AVDD=3.0~3.6V; TVDD=1.7~3.6V; AVSS=DVSS=0V)

Sharp Roll-Off Filter (VOAD bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband (Note 17)	+0.14dB/−0.12dB	PB	0	-	20.7	kHz
	−3.0dB	PB	-	22.8	-	kHz
Stopband (Note 17)		SB	28.4	-	-	kHz
Stopband Attenuation		SA	65	-	-	dB
Group Delay Distortion : 0Hz~20kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 18)		GD	-	16.5	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response (Note 17)	−3.0dB	FR	-	3.7	-	Hz

Voice Filter (VOAD bit = "1")

fs=16kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
VOICE						
Passband (Note 17)	0.5dB/−0.5dB	PB	0	-	6.3	kHz
	−3.0dB		-	6.9	-	kHz
Stopband (Note 17)		SB	8.0	-	-	kHz
Stopband Attenuation		SA	59.5	-	-	dB
Group Delay Distortion : 0Hz~8kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 18)		GD	-	18.1	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response (Note 17)	−3.0dB	FR	-	1.24	-	Hz

Note 17. Frequencies of Passband, Stopband and frequency response of HPF scale with fs (system sampling rate). HPF characteristics are not included to Passband and Stopband.

Note 18. The calculated delay time caused by digital filtering. This time is from the input of analog signal to the output of MSB at the SDTO pin.

■ DAC

(Ta= −40~105°C; AVDD = 3.0~3.6V; TVDD =1.7~3.6V; AVSS = DVSS = 0V)

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband (Note 19)	±0.05dB	PB	0	-	21.7	kHz
	−6.0dB	PB	-	24	-	kHz
Passband Ripple		PR	-		±0.05	dB
Stopband (Note 19)		SB	26.2	-	-	kHz
Stopband Attenuation (Note 20, Note 22)		SA	64	-	-	dB
Group Delay (Note 21)		GD	-	24	-	1/fs
Digital Filter + SCF + SMF (Note 20)						
Frequency Response : 0 ~ 20.0kHz		-	-	±0.5	-	dB

Note 19. Passband and stopband frequencies scale with fs (system sampling rate).
PB max. = 0.4535×fs, SB min. = 0.546×fs

Note 20. The output level when inputting a 1kHz, 0dB sine wave is defined as 0dB.

Note 21. This time is from the input of impulse data to the output of analog peak signal.

Note 22. from 0kHz to fs

10. DC Characteristics

(Ta=−40~105°C; AVDD = 3.0~3.6V; TVDD =1.7~3.6V; AVSS= DVSS = 0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Normal Pin (Except for SBDATA and SBCLK Pins)						
High Level Input Voltage 1 (Note 23)		VIH1	75%TVDD	-	-	V
Low Level Input Voltage 1 (Note 23)		VIL1	-	-	25%TVDD	V
High Level Input Voltage 2 (Note 24)		VIH2	70%TVDD	-	-	V
Low Level Input Voltage 2 (Note 24)		VIL2	-	-	30%TVDD	V
High Level Output Voltage Iout= −100μA (Note 25)		VOH1	TVDD−0.3	-	-	V
Low Level Output Voltage Iout=100μA (Note 25)		VOL1	-	-	0.3	V
SDA	TVDD≥2.0V (Iout=3mA)	VOL2	-	-	0.4	V
Low Level Output Voltage	TVDD<2.0V (Iout=3mA)	VOL2	-	-	20%TVDD	V
Input Leakage Current (Note 26)		Iin	-	-	±10	μA

Note 23. PDN, SDIN, BICK, LRCK and TEST pins

Note 24. SCL and SDA pins

Note 25. SDOUT and STO pins

Note 26. PDN, SDIN, BICK, LRCK, SCL and SDA (I) pins

11. Switching Characteristics

■ System Clock

(Ta=–40~105°C; AVDD = 3.0~3.6V; TVDD = 1.7~3.6V; AVSS = DVSS = 0V; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
LRCK Input Timing					
Frequency	fs	7.9	-	49	kHz
Duty (I^2S, MSB Justified, LSB Justified)	dLRCK		50		%
Pulse Width High (PCM Short Frame)	tLRCKH	1/fBCLK	-	-	ns
Pulse Width High (PCM Long Frame)	tLRCKL	1/fBCLK	-	-	ns
BICK Input Timing					
Frequency (Note 27)	fBCLK	0.23	3.072	3.136	MHz
Pulse Width Low	tBCLKL	128	-	-	ns
Pulse Width High	tBCLKH	128	-	-	ns

Note 27. fBCLK must be higher than 2fs×(IO Data Length).

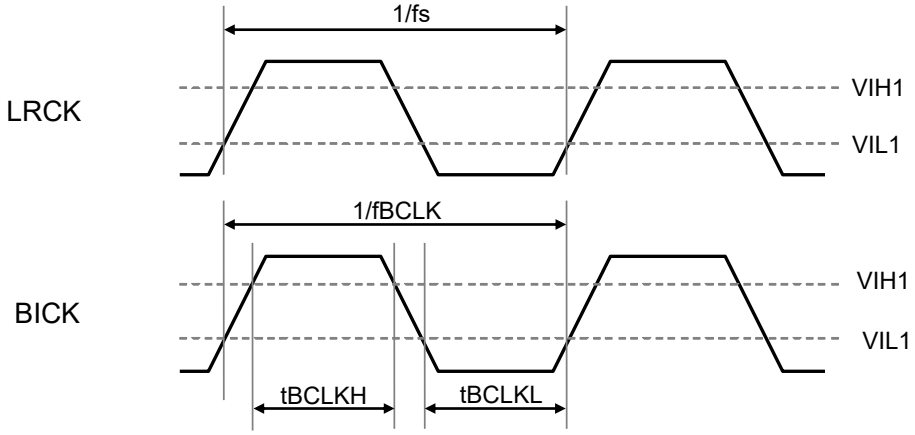


Figure 3. System Clock Timing

■ Audio Serial Inteface

(Ta=–40~105°C; AVDD = 3.0~3.6V; TVDD = 1.7~3.6V; AVSS = DVSS = 0V; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
BICK"↑" to LRCK Edge (Note 28)	tBLRD	10	-	-	ns
LRCK Edge to BICK"↑" (Note 28)	tLRBD	10	-	-	ns
SDTI Setup Time	tBSIDS	10	-	-	ns
SDTI Hold Time	tBSIDH	5	-	-	ns
LRCK Edge to SDTO (Except I^2S)	tLRD	0	-	20	ns
BICK"↓" to SDTO (Note 29)	tBSOD	0	-	20	ns

Note 28. When the polarity of BCLKx is inverted, delay time is counted from BCLKx "↓".
Note 29. When the polarity of BCLKx is inverted, delay time is counted from BCLKx "↑".

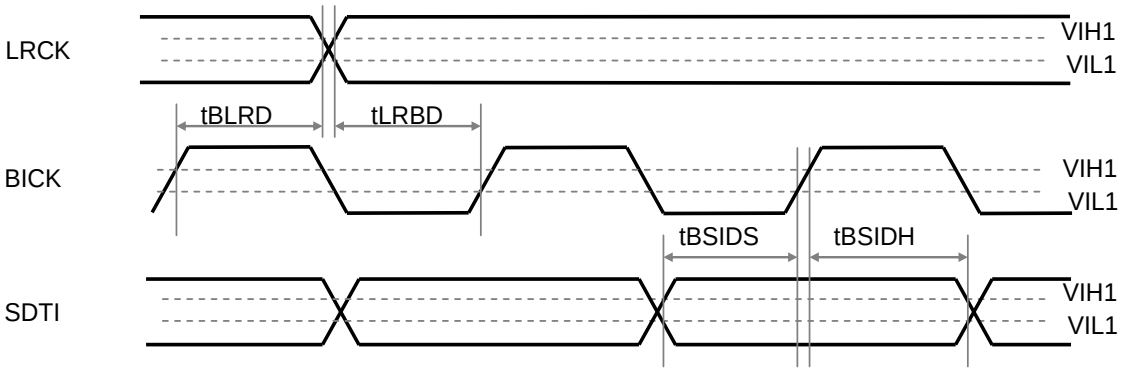


Figure 4. Audio Serial Interface Input Timing

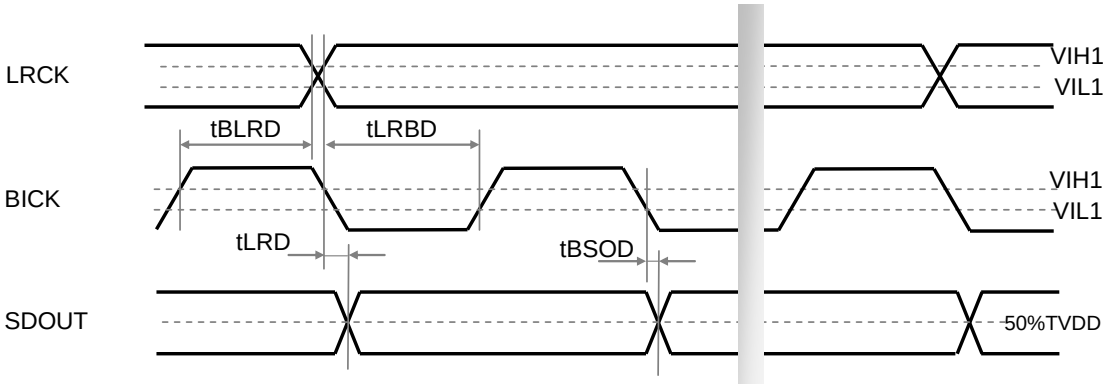


Figure 5. Audio Serial Interface Output Timing

■ Reset

(Ta=–40~105°C; AVDD = 3.0~3.6V; TVDD =1.7~3.6V; AVSS= DVSS = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
PDN Pulse Width (Note 30)	tRST	600	-	-	ns

Note 30. The PDN pin must be “L” when power up the AK4940.

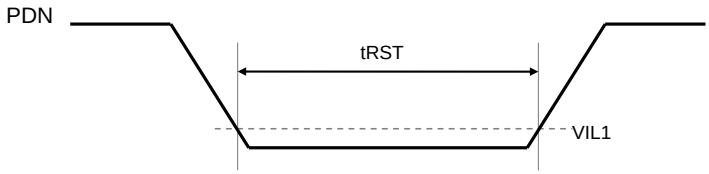


Figure 6. Reset Timing

■ I²C Interface

(Ta=−40~105°C; AVDD = 3.0~3.6V; TVDD =1.7~3.6V; AVSS= DVSS = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF

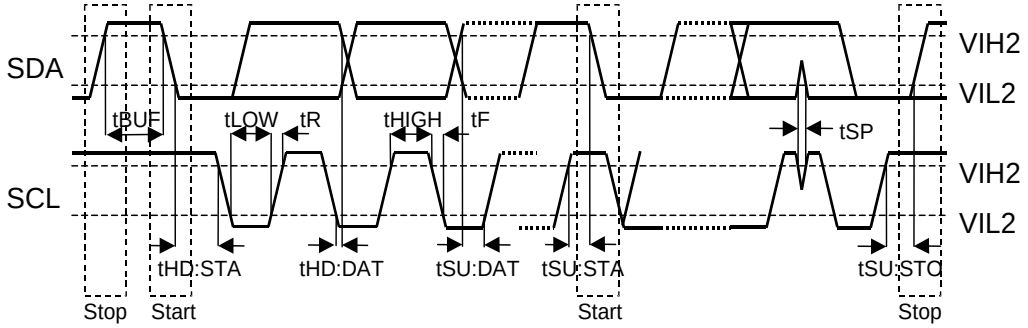


Figure 7. I²C BUS Interface Timing

12. Functional Description

■ System Clock

The AK4940 operates with external clocks that are input to the BICK pin and the LRCK pin. BICK and LRCK are defined as system clocks.

LRCK Input

A clock for sampling frequency (fs) is input to the LRCK pin. Set DFS[2:0] bits according to the fs clock.

BICK Input

A clock for data bit frequency is input to the BICK pin. Set BITFS[1:0] bits according to the BICK frequency. BICK clock must have stable frequency. Do not use a clock with two or more frequencies mixed.

Internal Master Clock PLL

The AK4940 integrates PLL and generates internal master clock from the input clock of the BICK pin. PLL multiple number is determined by DFS[2:0] bits that are for sampling frequency setting and BITFS[1:0] bits that are for BICK frequency setting.

Table 2. PLL Reference Clock (BICK) Frequency

		BICK Frequency			
		BITFS[1:0]			
		00 (default)	01	10	11
DFS[2:0]	fs	64fs	48fs	32fs	N/A
000 (default)	7.35kHz	470.4kHz	352.8kHz	235.2kHz	---
	8kHz	512kHz	384kHz	256kHz	---
001	11.025kHz	705.6kHz	NA (Note 31)	352.8kHz	---
	12kHz	768kHz	NA (Note 31)	384kHz	---
010	14.7kHz	940.8kHz	705.6kHz	470.4kHz	---
	16kHz	1024kHz	768kHz	512kHz	---
011	22.05kHz	1.4112MHz	1.0584MHz	705.6kHz	---
	24kHz	1.536MHz	1.152MHz	768kHz	---
100	29.4kHz	1.8816MHz	1.4112MHz	940.8kHz	---
	32kHz	2.048MHz	1.536MHz	1.024MHz	---
101	44.1kH	2.8224MHz	2.1168MHz	1.4112MHz	---
	48kHz	3.072MHz	2.304MHz	1.536MHz	---
110, 111	N/A	---	---	---	---

(N/A: Not Available)

Note 31. When BICK is 48fs, sampling frequency cannot be set 12kHz or 11.025kHz.

The PLL generates a 147.456 MHz or 135.4752 MHz internal master clock (PLLMCLK) by multiplying BICK.

Table 3. Internal Master Clock

Internal Master Clock (PLLMCLK) Frequency	48kHz base	44.1kHz base
	147.456MHz	135.4752MHz

■ Audio Serial Interface Format

The serial data code of ADC and DAC is MSB first, 2's compliment. Data format can be selected from MSB justified, LSB justified, I²S compatible and PCM.

Table 4. Audio Serial Interface Format Setting

LRIF [1:0]bits	DOFAD [1:0]bits	DIFDA [1:0]bits	BITFS [1:0]bits	Format	
Format Type	ADC Data Length & Position	DAC Data Length & Position	BICK Frequency	Data and LRCK	BICK Frequency
00	00	00	00	MSB Justified 24-bit	64fs
	01	01	00	LSB Justified 24-bit	64fs
			01	LSB Justified 24-bit	48fs
	10	10	00	LSB Justified 20-bit	64fs
			01	LSB Justified 20-bit	48fs
	11	11	00	LSB Justified 16-bit	64fs
			01	LSB Justified 16-bit	48fs
			10	LSB Justified 16-bit	32fs
01	00	00	00	I²S Compatible 24-bit	64fs
			01	I²S Compatible 24-bit	48fs
		11	10	I²S Compatible 16-bit	32fs
10	00	00	00	PCM Short Frame 24-bit	64fs
11	00	00	00	PCM Long Frame 24-bit	64fs
Others				N/A	N/A

BICK edge direction at LRCK starting edge can be set by the BCKP pin.

Table 5. BICK Edge Direction at LRCK Start Edge

BCKP bit	BICK Edge Direction	
0	Falling	(default)
1	Rising	

Serial Interface Format Examples

MSB Justified 24bit, BICK=64fs

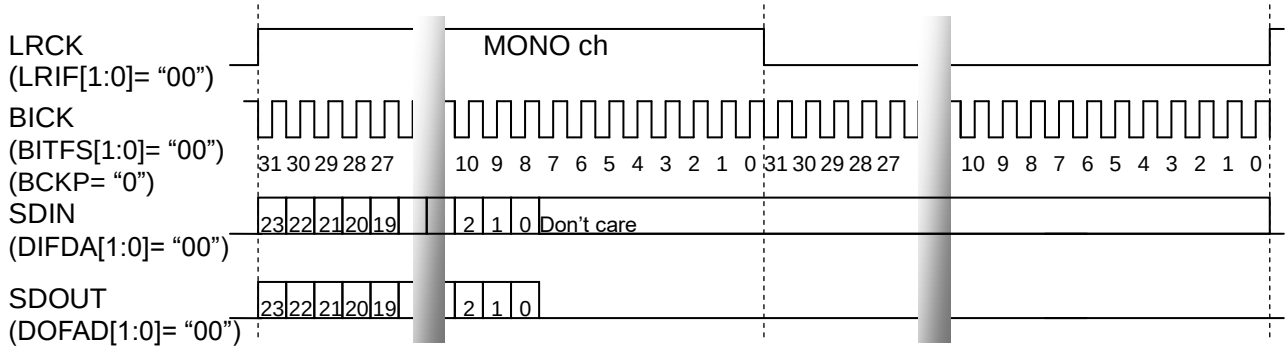


Figure 8. MSB Justified 24bit, BICK=64fs

LSB Justified 24bit/20bit/16bit, BICK=64fs

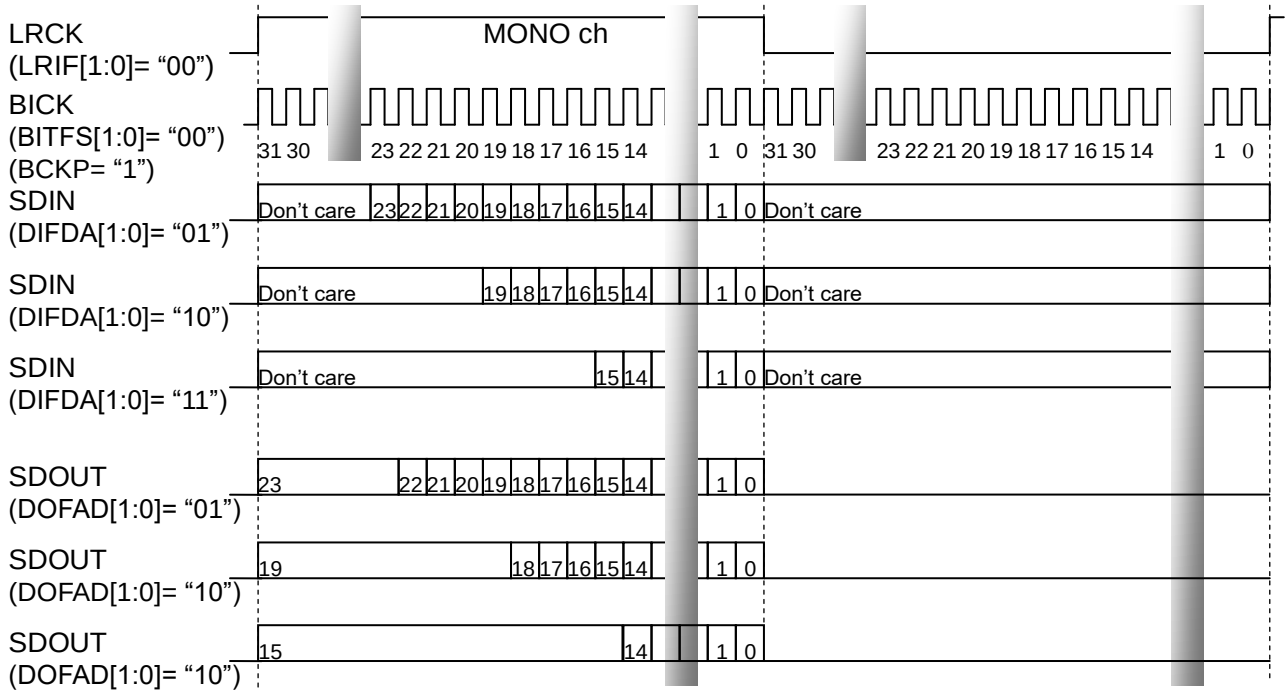


Figure 9. LSB Justified 24bit/20bit/16bit, BICK=64fs

LSB Justified 24bit/20bit/16bit, BICK=48fs

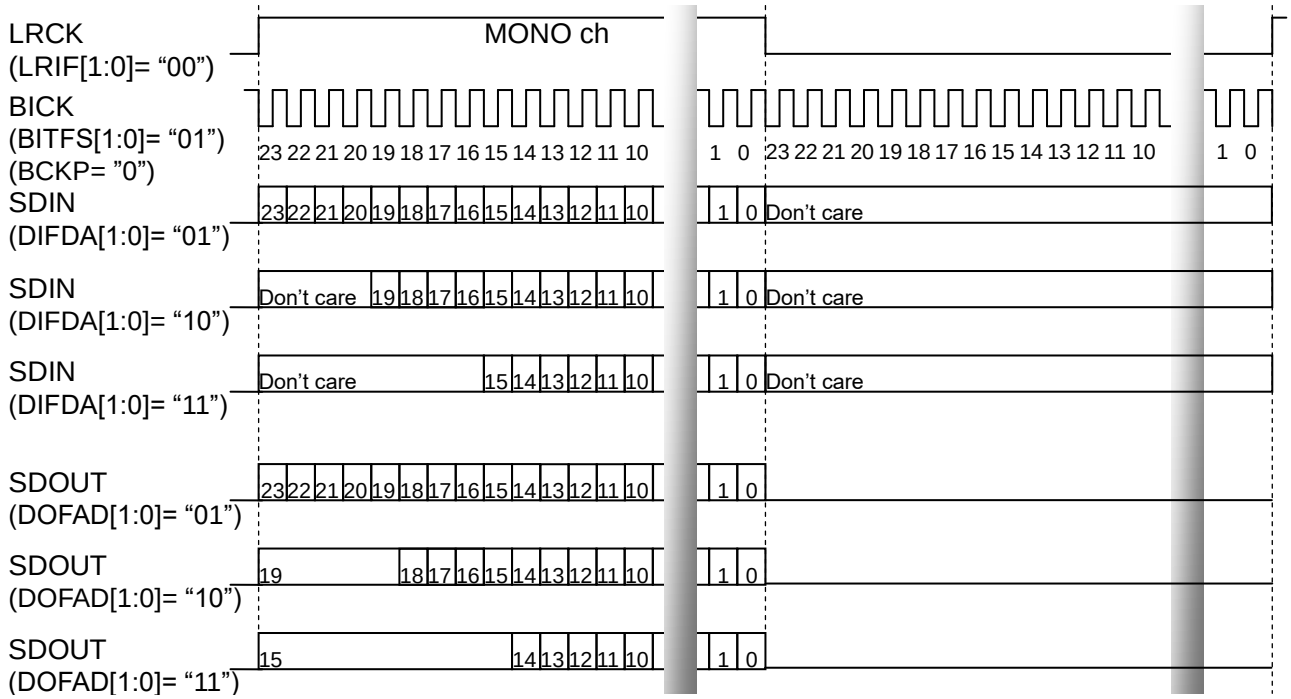


Figure 10. LSB Justified 24bit/20bit/16bit, BICK=48fs

LSB Justified 16bit, BICK=32fs

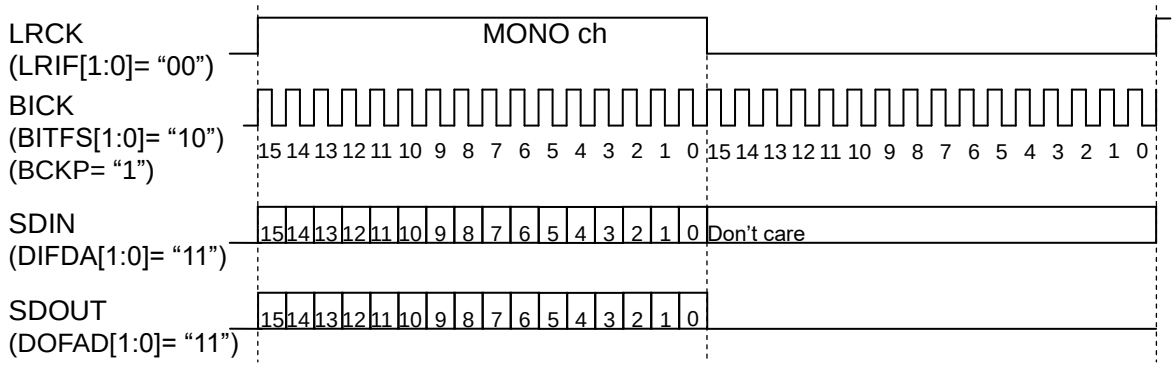


Figure 11. LSB Justified 16bit, BICK=32fs

I²S Compatible 24bit, BICK=64fs

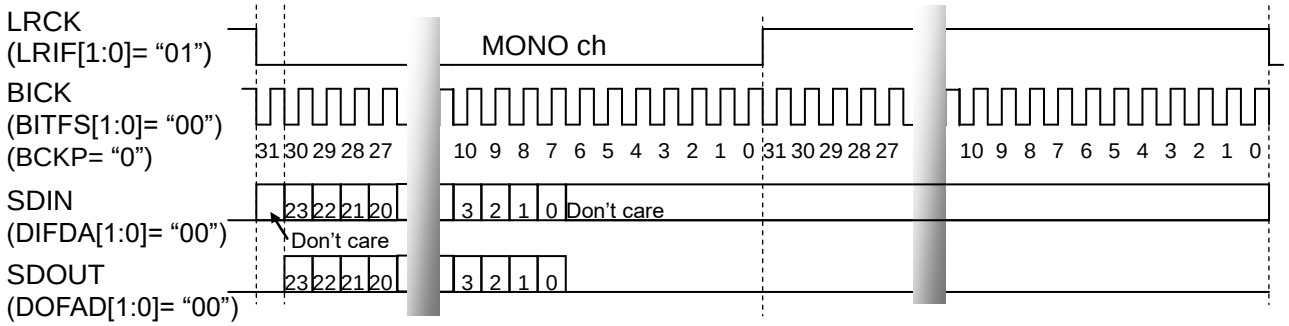


Figure 12. I²S Compatible 24bit, BICK=64fs

I²S Compatible 24bit, BICK=48fs

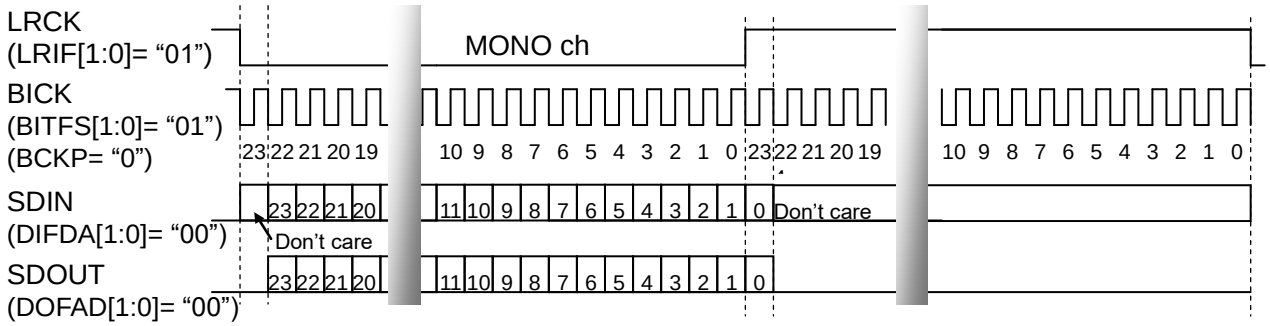


Figure 13. I²S Compatible 24bit, BICK=48fs

I²S Compatible 16bit, BICK=32fs

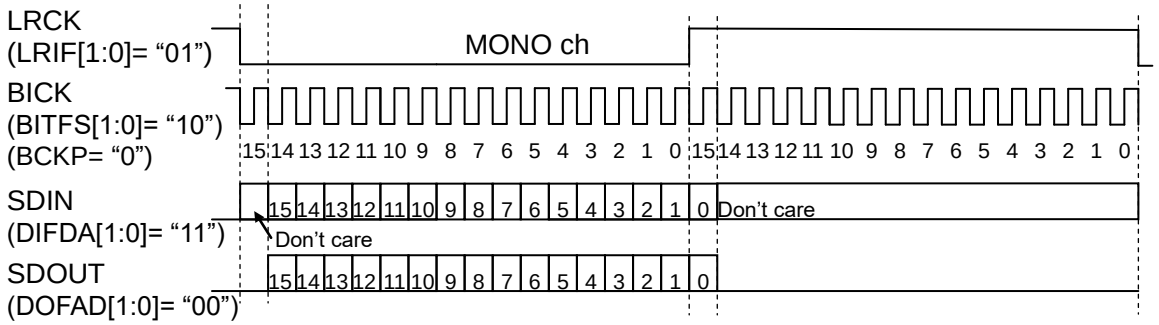


Figure 14. I²S Compatible 16bit, BICK=32fs

PCM Short Frame 24bit, BICK=64fs

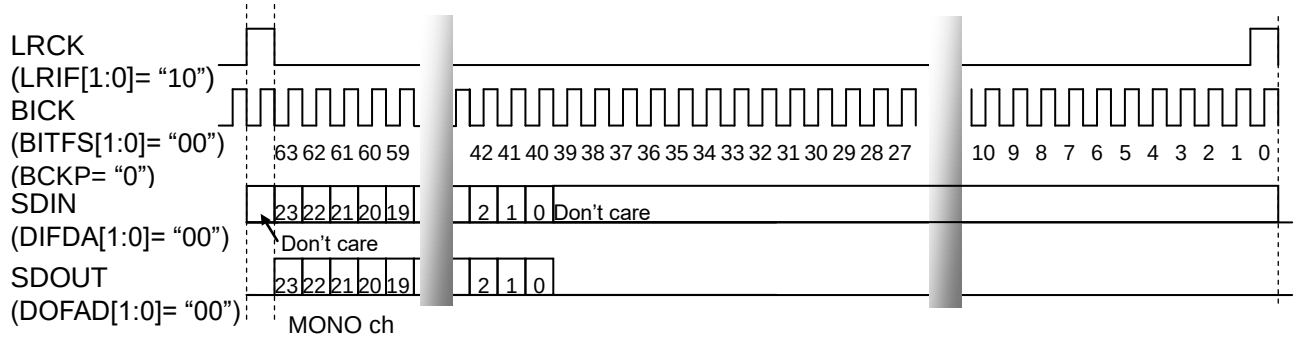


Figure 15. PCM Short Frame 24bit, BICK=64fs

PCM Long Frame 24bit, BICK=64fs

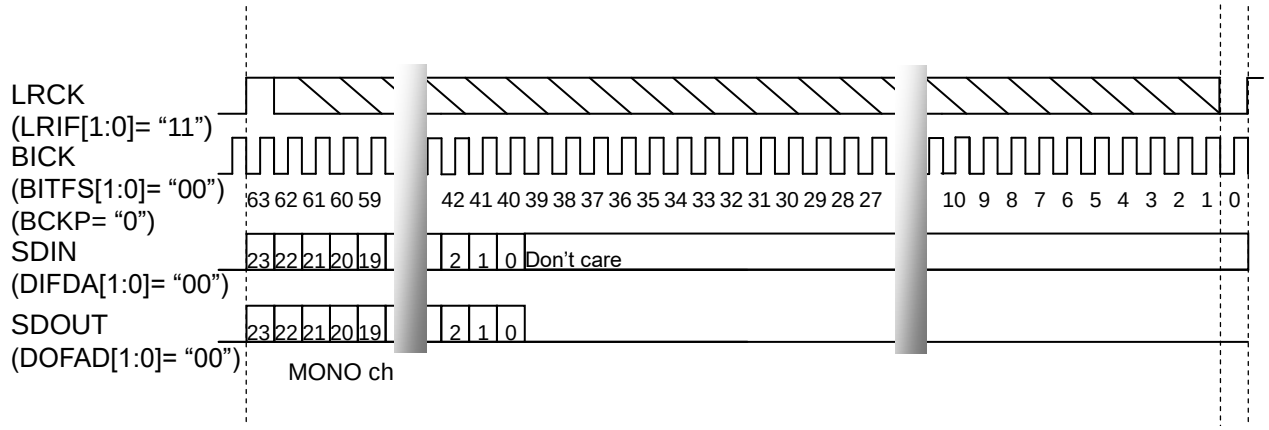


Figure 16. PCM Long Frame 24bit, BICK=64fs

■ LDO (Regulator for Internal Digital Circuits)

The AK4940 has a regulator (LDO) for driving internal digital circuits. Connect a 2.2μF (±30%) capacitor between the AVDRV pin and the DVSS pin for stabilization of the output voltage. Use a capacitor that has low ESL less than 100 nH and ESR less than 100 mΩ. In general, a ceramic capacitor has low ESL and low ESR. The value of 2.2μF (±30%) includes bias and temperature characteristics. The LDO starts operation by releasing power-down mode (PDN pin = “H”), and control register settings can be made after 1ms from the power-down release.
The AK4940 has an overcurrent protection circuit to avoid abnormal heat of the device that is caused by a short of the AVDRV pin to VSS, and an overvoltage protection circuit to protect the device from exceeded voltage when the voltage to the AVDRV pin gets too high. When these protection circuits perform, internal circuits are powered down and the STO pin outputs “L”. In this case, the AVDRV pin is pulled down by 110Ω (typ.). The internal circuit will not return to a normal operation until being reset by the PDN pin after removing the problems.

■ Power-down and Reset

Power-down, Reset Statuses and Power Management

Power-down and power-down release of the AK4940 are controlled by the PDN pin. Bringing the PDN pin to “L” power downs the AK4940. When the PDN pin is “L”, control register settings are fixed to their default values.
Power-down is released by setting the PDN pin to “H” and control registers can be accessed. After power-down is released, reset of the AK4940 and the power management of each block is controlled by registers such as CKRESETN bit (Clock Reset), CRESETN bit (CODEC Reset) and power management bits (PMAD, PMDA).
There are three states for the AK4940 other than normal operation: Power-down, Clock Reset and CODEC Reset. The power-down state means the status that the PDN pin is “L”. In this state, all blocks of the AK4940 stop operation.
The clock reset state means the status that the PDN pin is “H”, CKRESETN bit is “0” and CRESETN bit is “0”. In this state, the ADC, DAC, PLL circuits and internal clocks are stopped however LDO and VREF circuits are in operation.
The CODEC reset state means the status that the PDN pin is “H”, CKRESETN bit is “1” and CRESETN bit “0”. In this state, PLL and internal clocks are in operation but ADC and DAC are stopped. In this case, line-out amplifier outputs VCOM voltage. The AK4940 starts normal operation by setting the PDN pin = “H”, CKRESETN bit = “1” and CRESETN bit = “1”. In normal operation mode, ADC and DAC blocks can be controlled by PMAD and PMDA bits. ADC/DAC block is in operation when PMAD/PMDA bit = “1” and is stopped when PMAD/PMDA bit = “0”. The default value of PMAD and PMDA bits are “0”.

Table 6. Device State (x: Don’t Care)

State	Setting					Status			
	PDN pin	CKRESETN bit	CRESETN bit	PMAD bit	PMDA bit	PLL	ADC, Gain Amp.	DAC, Line-out Amp.	
Power Down	L	x	x	x	x	Down	Down	Down	
Clock Reset	H	0	0	x	x	Down	Down	Down	
CODEC Reset	H	1	0	x	x	Up	Down	Down	(Note 32)
CODEC Reset	H	1	1	0	0	Up	Down	Down	
DAC Reset	H	1	1	1	0	Up	Up	Down	
ADC Reset	H	1	1	0	1	Up	Down	Up	
Normal Operation	H	1	1	1	1	Up	Up	Up	

Note 32. A stable clock should be supplied before releasing clock reset (CKRESETN bit = “0” → “1”).

Power-down Release

The analog reference voltage source and LDO for internal digital circuit driving are powered-up by bringing the PDN pin to “H” from “L” after an interval of 600ns or more when AVDD and TVDD are powered up. Control register settings should be made with an interval of 1ms or longer after setting the PDN pin = “H”.

Clock Reset

After power-down mode is released (PDN pin = “H”), the default value of CKRESETN bit is “0” and the AK4940 is in clock reset state. All blocks except the analog reference voltage source and internal digital circuit driving LDO are in power-save mode. Even the internal PLL for master clock generation is powered down.

Necessary system clocks should be input before the clock reset is released. The internal PLL starts operation and the master clock is generated when clock reset is released (CKRESETN bit = “0” → “1”) (Figure 18). The AK4940 will be in normal operation by releasing power-down mode of the blocks by setting each power-management bit.

Do not stop system clocks except during clock reset (CKRESETN bit = “0”) or in power-down mode (PDN pin = “L”). The PLL and the internal clocks are stopped by this clock reset and the clock change can be done safely. Change register settings and system clock frequencies during clock reset or power-down mode. After system clock is stabilized, the PLL starts operation by releasing clock reset (CKRESETN bit = “1”).

Clock operated blocks (ADC, DAC) must be powered down before executing clock reset. These blocks can be powered down simultaneously by setting CRESETN bit to “0” from “1” (PMAD and PMDA bits settings are not necessary). Set CRESETN bit to “1” from “0” with an interval of 10ms (min.) for stabilization of PLL after clock reset is released.

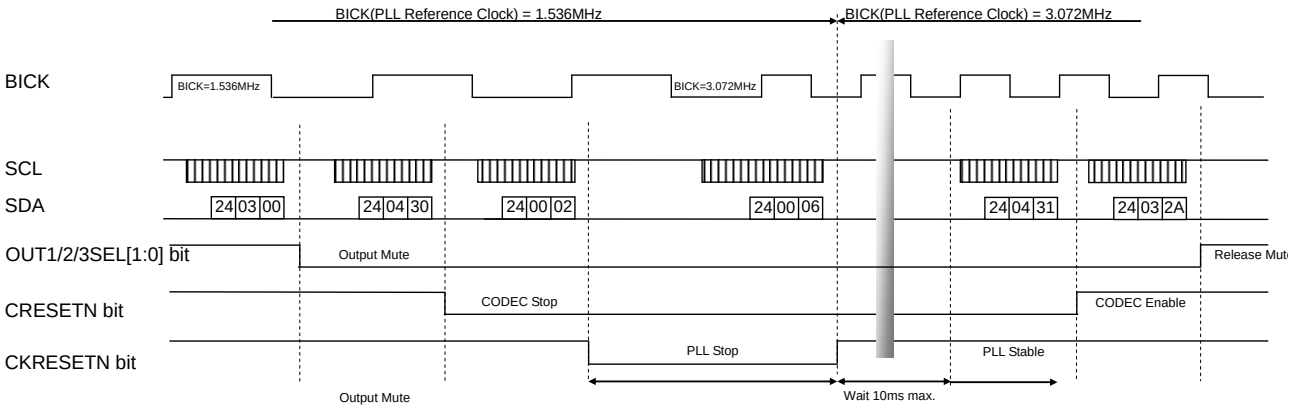


Figure 17. Clock Mode Switching Sequence

■ Power-up Sequence

The AK4940 should be powered up when the PDN pin = “L” (power-down state). Internal reference voltage source and internal digital circuits are powered up by setting the PDN pin to “H” after all power supplies are fed. In this time, control registers are initialized. Control register settings should be made with an interval of 1ms or more after the PDN pin = “H”.

The PLL starts operation by a clock reset release (CKRESETN bit = “0” → “1”) and generates the internal master clock after setting control registers. Therefore, necessary system clocks must be input before a clock reset release. The system clocks must not be stopped except during clock reset and power-down mode (PDN pin = “L”). Set analog output selector after releasing CODEC reset (CRESETN bit = “0” → “1”).

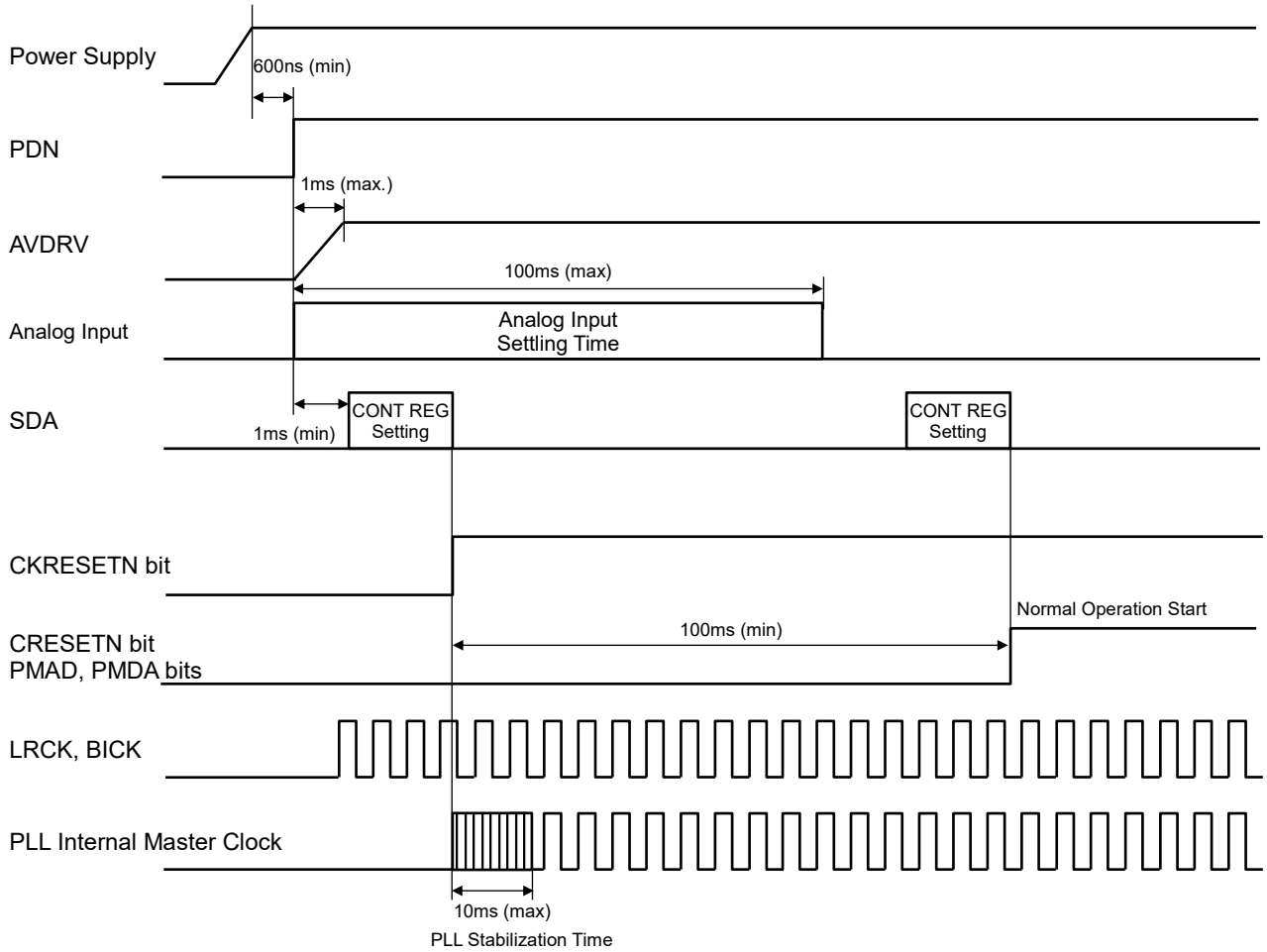


Figure 18. Power Up Sequence

■ STO Pin (Status Output)

The STO pin is an internal status output pin. It outputs “L” if the PDN pin = “L” (power-down mode) after the AK4940 is powered up. The internal LDO is powered up and the STO pin outputs “H” by releasing the power-down. The STO pin outputs “L” and internal circuits stop operation when overcurrent or overvoltage protection circuit for LDO is worked. Once the STO pin output become “L”, it will be kept until the AK4940 is reset by the PDN pin.

■ Analog Output Block

Start-up Time of Analog Output

Analog output pins (OUT1P/N, OUT2P/N, OUT3 pins) are connected to VCOM voltage via 2kΩ (typ.) resistors when setting the PDN pin to "H" from "L". The charging time constant will be 2ms if the external capacitors at analog output pins are 1μF. Wait time about 100ms is necessary to charge external capacitors sufficiently before switching output selectors (OUT1SEL, OUT2SEL and OUT3SEL bits). If the wait time is not enough, click noise may occur when switching output selector since the output pin voltage goes off from VCOM voltage.

Analog Output Selector

Output signal from the analog output pins can be selected by OUT1SEL[1:0] bits, OUT2SEL[1:0] bits, OUT3SEL[1:0] bits and OUTNSEL bit.

Table 7. Analog Output Signal Select

OUT1SEL [1:0] bits	OUTNSEL bit	Mode	OUT1P pin	OUT1N pin
00 (default)	X	VCOM	VCOM Output Impedance 2kΩ (Typ.)	VCOM Output Impedance 2kΩ (Typ.)
01	X	Analog Direct Path1	Connected to IN1P pin Path Impedance 300Ω (Max.)	Connected to IN1N pin Path Impedance 300Ω (Max.)
10	0	DAC Differential Output	DAC Lineout (+) Output Impedance 300Ω (Max.)	DAC Lineout (-) Output Impedance 300Ω (Max.)
10	1	DAC Single-ended or Pseudo Differential Output	DAC Lineout (+) Output Impedance 300Ω (Max.)	VCOM Output Impedance 300Ω (Max.)
11	X	N/A	N/A	N/A

(a) OUTP1, OUTN1 Signal Select

OUT1SEL [1:0] bits	OUTNSEL bit	Mode	OUT2P pin	OUT2N pin
00 (default)	X	VCOM	VCOM Output Impedance 2kΩ (Typ.)	VCOM Output Impedance 2kΩ (Typ.)
01	X	Analog Direct Path2	Connected to IN2P pin Path Impedance 300Ω (Max.)	Connected to IN2N pin Path Impedance 300Ω (Max.)
10	0	DAC Differential Output	DAC Lineout (+) Output Impedance 300Ω (Max.)	DAC Lineout (-) Output Impedance 300Ω (Max.)
10	1	DAC Single-ended or Pseudo Differential Output	DAC Lineout (+) Output Impedance 300Ω (Max.)	VCOM Output Impedance 300Ω (Max.)
11	X	N/A	N/A	N/A

(b) OUTP2, OUTN2 Signal Select

OUT3SEL [1:0] bits	OUTNSEL bit	Mode	OUT3 pin
00 (default)	X	VCOM	VCOM Output Impedance 2kΩ (Typ.)
01	X	DAC Single-ended Output	DAC Lineout (+) Output Impedance 300Ω (Max.)
10	0	DAC Single-ended Output	DAC Lineout (-) Output Impedance 300Ω (Max.)
10	1	VCOM	VCOM Output Impedance 300Ω (Max.)
11	X	N/A	N/A

(c) OUT3 Signal Select

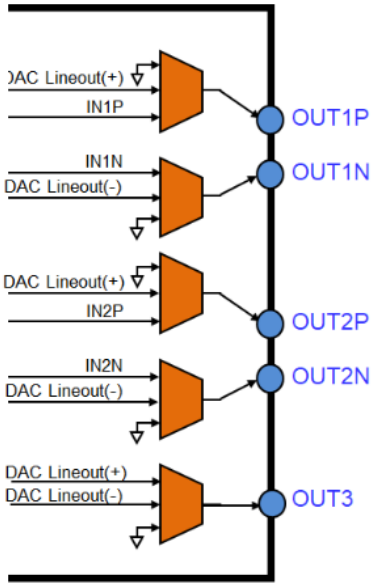


Figure 19. Analog Output Selector

■ Analog Input Block

Analog Direct Path

The AK4940 has two analog direct paths. The IN1P/N pin is connected to the OUT1P/N pin via analog direct path1 by setting OUT1SEL[1:0] bits = “01”. The IN2P/N pin is connected to the OUT2P/N pin via analog direct path2 by setting OUT2SEL[1:0] bits = “01”. Analog signal that is input via DC cut capacitor is converted to a signal that refers VCOM voltage (typ. AVDD/2) and output. The resistance between the input and the output pins is 300Ω (max.). The VCOM voltage is input to the analog direct path via a 50 kΩ (typ.) resistor. This 50 kΩ impedance will be load resistance to microphone signal output circuit.

Microphone Gain Amplifier

The AK4940 integrates a gain amplifier at input stage of ADC. The gain amplifier can be set by MGN[3:0] bits. Input impedance of the gain amplifier is 20kΩ (typ.). At maximum, 3.0 Vpp input signal is accepted. The amplifier should be adjusted not to exceed the input full scale of the ADC.

Table 8. Gain Setting

MGN [3:0] bits	Input Gain	
0000	–6dB	
0001	–3dB	
0010	0dB	(default)
0011	3dB	
0100	6dB	
0101	9dB	
0110	12dB	
0111	15dB	
1000	18dB	
1001	21dB	
1010	24dB	
1011	27dB	
Others	N/A	

Start-up Time of Analog Input

The IN1N and IN2N pins are connected to VCOM voltage via 0.8 kΩ (typ.) resistance when CRESETN bit = “0” or PMAD bit = “0”. When CRESETN bit = “1” and PMAD bit = “1”, one of the IN1N pin or IN2N pin that is not selected by ADCSEL bit is connected to VCOM voltage via 0.8 kΩ (typ.) resistance.

External capacitors at the IN1P/N or IN2P/N pins are charged by VCOM voltage when the AK4940 enters clock reset state by setting the PDN pin = “H”. Resistance between the IN1N, IN2N pin and VCOM is 0.8 kΩ (typ.). The time constant of charging will be 20ms if the values of external capacitors at analog output pins are 1μF. CODEC reset should be released (CRESTEN bit = “1”), and input mode and ADC input selection registers should be set after wait time about 100ms to charge external capacitors sufficiently. If the wait time is not enough, click noise may occur when switching output selector or when ADC operation starts since the reference voltage of input pin goes off from VCOM voltage.

ADC Input Selection

Analog signal input mode can be selected from differential input, single-ended input and pseudo differential input modes by setting ADDIFFN bit. Input channels are selected by ADCSEL bit.

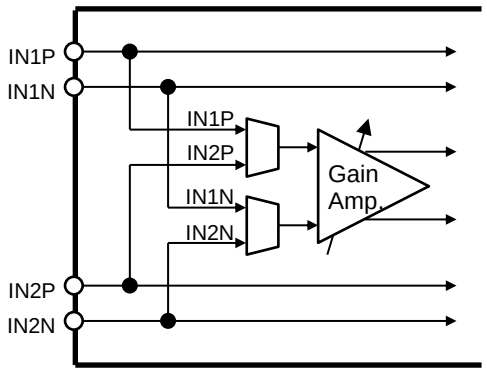


Figure 20. Analog Input Selector

Table 9. ADC Input Setting

ADDIFFN bit	Input Mode	
0	Differential	(default)
1	Single-End, Pseudo-Differential	

ADCSEL bit	Input Pin	
0	IN1P, IN1N	(default)
1	IN2P, IN2N	

■ ADC

ADC Initialization Cycle

ADC initialization cycle starts when ADC reset is released by PMAD bit or CRESETN bit. The output data of the SDOUT pin is 2's complement during initialization cycle. Initialization cycle will finish in 1059/fs and the AK4940 starts outputting A/D data.

ADC Block High Pass Filter

A digital high pass filter (HPF) for DC offset cancelling is integrated in ADC block. The cutoff frequency of the HPF is 3.7Hz (typ.) when fs = 48kHz. It is proportional to fs.

ADC Digital Filter

ADC block has two kinds of digital filters and they can be selected by VOAD bit.

Table 10. ADC Digital Filter Select

VOAD bit	Digital Filter	
0	Sharp Roll-Off Filter	(default)
1	Voice Filter	

ADC Block Digital Volume

Digital volume control (256 level, 0.5dB) is available at the output block of the ADC.

Table 11. VOLAD[7:0] bits vs ADC Digital Volume Level

code	dB	code	dB	code	dB	code	dB	Code	dB	code	dB	code	dB	code	dB
00h	24.0	20h	8.0	40h	-8.0	60h	-24.0	80h	-40.0	A0h	-56.0	C0h	-72.0	E0h	-88.0
01h	23.5	21h	7.5	41h	-8.5	61h	-24.5	81h	-40.5	A1h	-56.5	C1h	-72.5	E1h	-88.5
02h	23.0	22h	7.0	42h	-9.0	62h	-25.0	82h	-41.0	A2h	-57.0	C2h	-73.0	E2h	-89.0
03h	22.5	23h	6.5	43h	-9.5	63h	-25.5	83h	-41.5	A3h	-57.5	C3h	-73.5	E3h	-89.5
04h	22.0	24h	6.0	44h	-10.0	64h	-26.0	84h	-42.0	A4h	-58.0	C4h	-74.0	E4h	-90.0
05h	21.5	25h	5.5	45h	-10.5	65h	-26.5	85h	-42.5	A5h	-58.5	C5h	-74.5	E5h	-90.5
06h	21.0	26h	5.0	46h	-11.0	66h	-27.0	86h	-43.0	A6h	-59.0	C6h	-75.0	E6h	-91.0
07h	20.5	27h	4.5	47h	-11.5	67h	-27.5	87h	-43.5	A7h	-59.5	C7h	-75.5	E7h	-91.5
08h	20.0	28h	4.0	48h	-12.0	68h	-28.0	88h	-44.0	A8h	-60.0	C8h	-76.0	E8h	-92.0
09h	19.5	29h	3.5	49h	-12.5	69h	-28.5	89h	-44.5	A9h	-60.5	C9h	-76.5	E9h	-92.5
0Ah	19.0	2Ah	3.0	4Ah	-13.0	6Ah	-29.0	8Ah	-45.0	AAh	-61.0	CAh	-77.0	EAh	-93.0
0Bh	18.5	2Bh	2.5	4Bh	-13.5	6Bh	-29.5	8Bh	-45.5	ABh	-61.5	CBh	-77.5	EBh	-93.5
0Ch	18.0	2Ch	2.0	4Ch	-14.0	6Ch	-30.0	8Ch	-46.0	ACh	-62.0	CCh	-78.0	ECh	-94.0
0Dh	17.5	2Dh	1.5	4Dh	-14.5	6Dh	-30.5	8Dh	-46.5	ADh	-62.5	CDh	-78.5	EDh	-94.5
0Eh	17.0	2Eh	1.0	4Eh	-15.0	6Eh	-31.0	8Eh	-47.0	AEh	-63.0	CEh	-79.0	EEh	-95.0
0Fh	16.5	2Fh	0.5	4Fh	-15.5	6Fh	-31.5	8Fh	-47.5	AFh	-63.5	CFh	-79.5	EFh	-95.5
10h	16.0	30h	0.0	50h	-16.0	70h	-32.0	90h	-48.0	B0h	-64.0	D0h	-80.0	F0h	-96.0
11h	15.5	31h	-0.5	51h	-16.5	71h	-32.5	91h	-48.5	B1h	-64.5	D1h	-80.5	F1h	-96.5
12h	15.0	32h	-1.0	52h	-17.0	72h	-33.0	92h	-49.0	B2h	-65.0	D2h	-81.0	F2h	-97.0
13h	14.5	33h	-1.5	53h	-17.5	73h	-33.5	93h	-49.5	B3h	-65.5	D3h	-81.5	F3h	-97.5
14h	14.0	34h	-2.0	54h	-18.0	74h	-34.0	94h	-50.0	B4h	-66.0	D4h	-82.0	F4h	-98.0
15h	13.5	35h	-2.5	55h	-18.5	75h	-34.5	95h	-50.5	B5h	-66.5	D5h	-82.5	F5h	-98.5
16h	13.0	36h	-3.0	56h	-19.0	76h	-35.0	96h	-51.0	B6h	-67.0	D6h	-83.0	F6h	-99.0
17h	12.5	37h	-3.5	57h	-19.5	77h	-35.5	97h	-51.5	B7h	-67.5	D7h	-83.5	F7h	-99.5
18h	12.0	38h	-4.0	58h	-20.0	78h	-36.0	98h	-52.0	B8h	-68.0	D8h	-84.0	F8h	-100.0
19h	11.5	39h	-4.5	59h	-20.5	79h	-36.5	99h	-52.5	B9h	-68.5	D9h	-84.5	F9h	-100.5
1Ah	11.0	3Ah	-5.0	5Ah	-21.0	7Ah	-37.0	9Ah	-53.0	BAh	-69.0	DAh	-85.0	FAh	-101.0
1Bh	10.5	3Bh	-5.5	5Bh	-21.5	7Bh	-37.5	9Bh	-53.5	BBh	-69.5	DBh	-85.5	FBh	-101.5
1Ch	10.0	3Ch	-.6.0	5Ch	-22.0	7Ch	-38.0	9Ch	-54.0	BCh	-70.0	DCh	-86.0	FCh	-102.0
1Dh	9.5	3Dh	-6.5	5Dh	-22.5	7Dh	-38.5	9Dh	-54.5	BDh	-70.5	DDh	-86.5	FDh	-102.5
1Eh	9.0	3Eh	-7.0	5Eh	-23.0	7Eh	-39.0	9Eh	-55.0	BEh	-71.0	DEh	-87.0	FEh	-103.0
1Fh	8.5	3Fh	-7.5	5Fh	-23.5	7Fh	-39.5	9Fh	-55.5	BFh	-71.5	DFh	-87.5	FFh	Mute

Default: 30h (0dB)

When changing output levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions. Digital volume transition speed is controlled by ATSPAD bit.

Table 12. ADC Digital Volume Transition Speed

ATSPAD bit	Transition Time per Step	
0	4/fs	(default)
1	16/fs	

It takes 1020/fs (21.3ms@fs=48kHz) from 00h (24dB) to FFh (Mute) when ATSPAD bit = “0”.

Table 13. ADC Volume Transition Time between 00h and FFh

ATSPAD bit	00h ↔ FFh Transition Time				
	LRCK Cycle	fs=48kHz	fs=44.1kHz	fs=8kHz	
0	1020/fs	21.3ms	23.1ms	127.5ms	(default)
1	4080/fs	85.0ms	92.5ms	510.0ms	

ADC Soft Mute

The ADC block has a digital soft mute function. The output signal is attenuated to -∞ in "(FFh − VOLAD[7:0] bits) x ATT transition time" from the current ADC digital volume setting level by setting ADMUTE bit to "1". When the ADMUTE bit is set to "0" again, the mute is cancelled and the output attenuation level gradually changes to VOLAD[7:0] bits setting level in "FFh − VOLAD[7:0] bits x ATT transition time". If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and the volume level returns to original volume setting level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

The attenuation level transition takes 828/fs from 0dB to -∞ and from -∞ to 0dB. Soft mute function is available when the ADC block is in operation. Volume level will be at −∞ dB when the ADC is reset by setting PMAD bit = "0". It returns to the VOLAD[7:0] bits setting level when ADC operation is started.

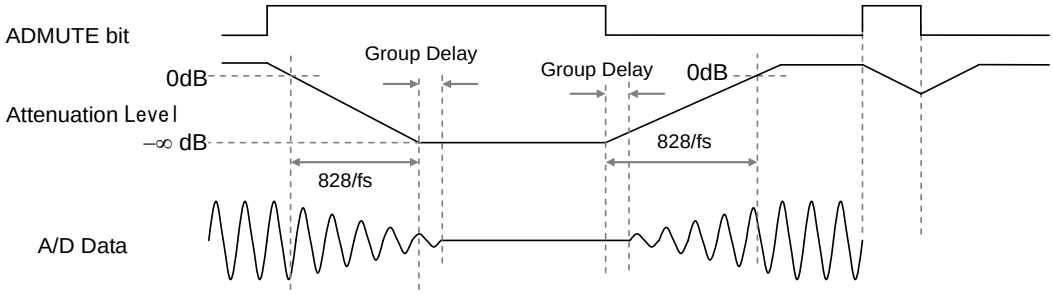


Figure 21. ADC Soft Mute

ADC Input Selector

The input selector should be changed after enabling soft mute function to avoid the switching noise of the input selector.

e.g.) Volume Level -3dB (36h), Transition Time for 1 code = 4/fs, fs=48kHz

(1) Enable Soft Mute	ADMUTE bit = "0" → "1"
(2) Wait until the volume become −∞dB	(FFh−36h) × 4/fs = (255−54) × 4 / (48×10^3) = 16.75ms
(3) Switch Selector	ADSEL bits = "0" → "1"
(4) Wait Stable Input of ADC	200ms min.
(5) Disable Soft Mute Function	ADMUTE bit = "1" → "0"

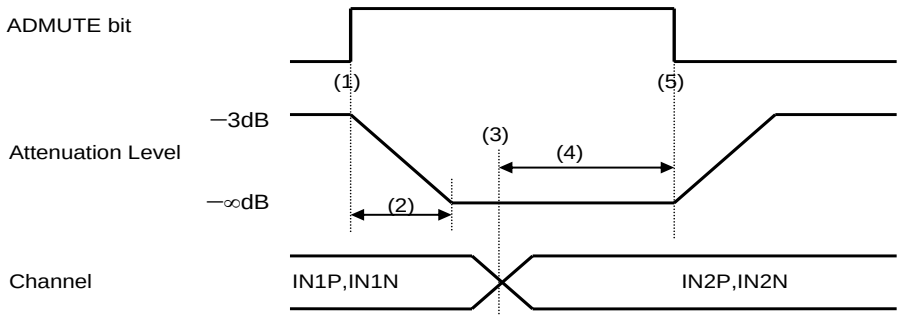


Figure 22. ADC Input Selector Switching Sequence Example

■ DAC

The DAC output is output from the OUT1P, OUT1N, OUT2P, OUT2N and OUT3 pins via line-out amplifiers. The OUT1N and the OUT2N pins are inverted output. Differential output is available by using the OUT1N and the OUT2N pins with the OUT1P and the OUT2P pins, respectively.

DAC Block Digital Volume

The AK4940 has digital volume control at DAC input block. (256 levels, 0.5 steps).

Table 14. VOLDA[7:0] bits vs DAC Digital Volume Level

code	dB	code	dB	code	dB	code	dB	code	dB	code	dB	code	DB	code	dB
00h	12.0	20h	-4.0	40h	-20.0	60h	-36.0	80h	-52.0	A0h	-68.0	C0h	-84.0	E0h	-100.0
01h	11.5	21h	-4.5	41h	-20.5	61h	-36.5	81h	-52.5	A1h	-68.5	C1h	-84.5	E1h	-100.5
02h	11.0	22h	-5.0	42h	-21.0	62h	-37.0	82h	-53.0	A2h	-69.0	C2h	-85.0	E2h	-101.0
03h	10.5	23h	-5.5	43h	-21.5	63h	-37.5	83h	-53.5	A3h	-69.5	C3h	-85.5	E3h	-101.5
04h	10.0	24h	-.6.0	44h	-22.0	64h	-38.0	84h	-54.0	A4h	-70.0	C4h	-86.0	E4h	-102.0
05h	9.5	25h	-6.5	45h	-22.5	65h	-38.5	85h	-54.5	A5h	-70.5	C5h	-86.5	E5h	-102.5
06h	9.0	26h	-7.0	46h	-23.0	66h	-39.0	86h	-55.0	A6h	-71.0	C6h	-87.0	E6h	-103.0
07h	8.5	27h	-7.5	47h	-23.5	67h	-39.5	87h	-55.5	A7h	-71.5	C7h	-87.5	E7h	-103.5
08h	8.0	28h	-8.0	48h	-24.0	68h	-40.0	88h	-56.0	A8h	-72.0	C8h	-88.0	E8h	-104.0
09h	7.5	29h	-8.5	49h	-24.5	69h	-40.5	89h	-56.5	A9h	-72.5	C9h	-88.5	E9h	-104.5
0Ah	7.0	2Ah	-9.0	4Ah	-25.0	6Ah	-41.0	8Ah	-57.0	AAh	-73.0	CAh	-89.0	EAh	-105.0
0Bh	6.5	2Bh	-9.5	4Bh	-25.5	6Bh	-41.5	8Bh	-57.5	ABh	-73.5	CBh	-89.5	EBh	-105.5
0Ch	6.0	2Ch	-10.0	4Ch	-26.0	6Ch	-42.0	8Ch	-58.0	ACh	-74.0	CCh	-90.0	ECh	-106.0
0Dh	5.5	2Dh	-10.5	4Dh	-26.5	6Dh	-42.5	8Dh	-58.5	ADh	-74.5	CDh	-90.5	EDh	-106.5
0Eh	5.0	2Eh	-11.0	4Eh	-27.0	6Eh	-43.0	8Eh	-59.0	AEh	-75.0	CEh	-91.0	EEh	-107.0
0Fh	4.5	2Fh	-11.5	4Fh	-27.5	6Fh	-43.5	8Fh	-59.5	AFh	-75.5	CFh	-91.5	EFh	-107.5
10h	4.0	30h	-12.0	50h	-28.0	70h	-44.0	90h	-60.0	B0h	-76.0	D0h	-92.0	F0h	-108.0
11h	3.5	31h	-12.5	51h	-28.5	71h	-44.5	91h	-60.5	B1h	-76.5	D1h	-92.5	F1h	-108.5
12h	3.0	32h	-13.0	52h	-29.0	72h	-45.0	92h	-61.0	B2h	-77.0	D2h	-93.0	F2h	-109.0
13h	2.5	33h	-13.5	53h	-29.5	73h	-45.5	93h	-61.5	B3h	-77.5	D3h	-93.5	F3h	-109.5
14h	2.0	34h	-14.0	54h	-30.0	74h	-46.0	94h	-62.0	B4h	-78.0	D4h	-94.0	F4h	-110.0
15h	1.5	35h	-14.5	55h	-30.5	75h	-46.5	95h	-62.5	B5h	-78.5	D5h	-94.5	F5h	-110.5
16h	1.0	36h	-15.0	56h	-31.0	76h	-47.0	96h	-63.0	B6h	-79.0	D6h	-95.0	F6h	-111.0
17h	0.5	37h	-15.5	57h	-31.5	77h	-47.5	97h	-63.5	B7h	-79.5	D7h	-95.5	F7h	-111.5
18h	0.0	38h	-16.0	58h	-32.0	78h	-48.0	98h	-64.0	B8h	-80.0	D8h	-96.0	F8h	-112.0
19h	-0.5	39h	-16.5	59h	-32.5	79h	-48.5	99h	-64.5	B9h	-80.5	D9h	-96.5	F9h	-112.5
1Ah	-1.0	3Ah	-17.0	5Ah	-33.0	7Ah	-49.0	9Ah	-65.0	BAh	-81.0	DAh	-97.0	FAh	-113.0
1Bh	-1.5	3Bh	-17.5	5Bh	-33.5	7Bh	-49.5	9Bh	-65.5	BBh	-81.5	DBh	-97.5	FBh	-113.5
1Ch	-2.0	3Ch	-18.0	5Ch	-34.0	7Ch	-50.0	9Ch	-66.0	BCh	-82.0	DCh	-98.0	FCh	-114.0
1Dh	-2.5	3Dh	-18.5	5Dh	-34.5	7Dh	-50.5	9Dh	-66.5	BDh	-82.5	DDh	-98.5	FDh	-114.5
1Eh	-3.0	3Eh	-19.0	5Eh	-35.0	7Eh	-51.0	9Eh	-67.0	BEh	-83.0	DEh	-99.0	FEh	-115.0
1Fh	-3.5	3Fh	-19.5	5Fh	-35.5	7Fh	-51.5	9Fh	-67.5	BFh	-83.5	DFh	-99.5	FFh	Mute

Default: 18h (0dB)

When changing output levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions. The transition time between set values is selected by ATSPDA bit.

Table 15. DAC Digital Volume Transition Speed

ATSPDA	Transition Time per Step	
0	4/fs	(default)
1	16/fs	

When ATSPDA bit = “0”, it takes 1020/fs (21.3ms@fs=48kHz) from 00H (0dB) to FFH (MUTE).

Table 16. DAC Volume Transition Time between 00h and FFh

ATSPDA bit	00h ↔ FFh Transition Time				
	LRCK Cycle	fs=48kHz	fs=44.1kHz	fs=8kHz	
0	1020/fs	21.3ms	23.1ms	127.5ms	(default)
1	4080/fs	85.0ms	92.5ms	510.0ms	

DAC Soft Mute

The DAC block has a digital soft mute function. The output signal is attenuated to -∞ in “(FFh – VOLDA[7:0] bits) x ATT transition time” from the current DAC digital volume setting level by setting DAMUTE bit to “1”. When the DAMUTE bit is set to “0” again, the mute is cancelled and the output attenuation level gradually changes to VOLDA[7:0] bits setting level in “(FFh – VOLDA[7:0] bits) x ATT transition time”. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and the volume level returns to original volume setting level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

The attenuation level transition takes 924/fs from 0dB to -∞ and from -∞ to 0dB. Soft mute function is available when the DAC is in operation.

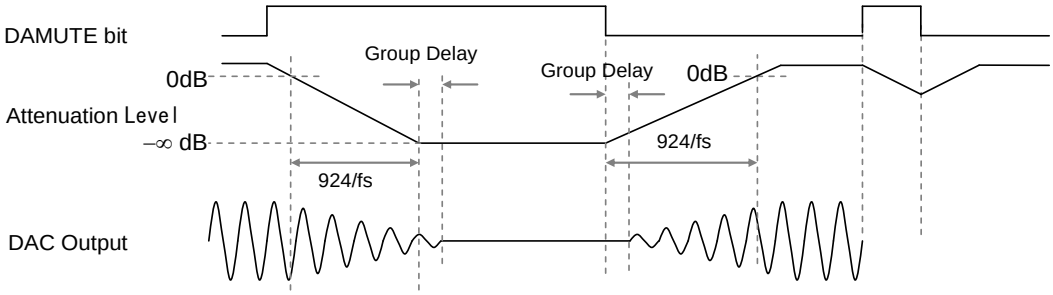


Figure 23. DAC Soft Mute Operation

If changing the system clock, set OUT1SEL[1:0] bits, OUT2SEL[1:0] bits, and OUT3SEL[1:0] bits to “00b” to mute the analog outputs. A click noise that occurs when resuming DAC operation after changing system clocks can be avoided.

DAC Output Polarity Invert

It is possible to invert the DAC output polarity by INV bit.

Table 17. DAC Output Polarity

INV bit	Output Polarity	
0	Non-Invert	(default)
1	Invert	

■ I²C-bus Interface

Access to the AK4940 registers and RAM can be controlled by an I²C bus. The AK4940 supports fast-mode I²C-bus (max: 400kHz) and fast-mode plus (max: 1MHz). The AK4940 does not support High Speed mode (max: 3.4MHz).

WRITE Operations

Figure 24 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 30). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as “0010010”. The next bit is CAD0 (device address bit). This bit identifies the specific device on the bus. If the slave address matches that of the AK4940, the AK4940 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 30). A R/W bit value of “1” indicates that the read operation is to be executed, and “0” indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4940 and the format is MSB first. (Figure 26). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 27). The AK4940 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 30).

The AK4940 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4940 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “09H” prior to generating a stop condition, the address counter will “roll over” to “00H” and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 32) except for the START and STOP conditions.

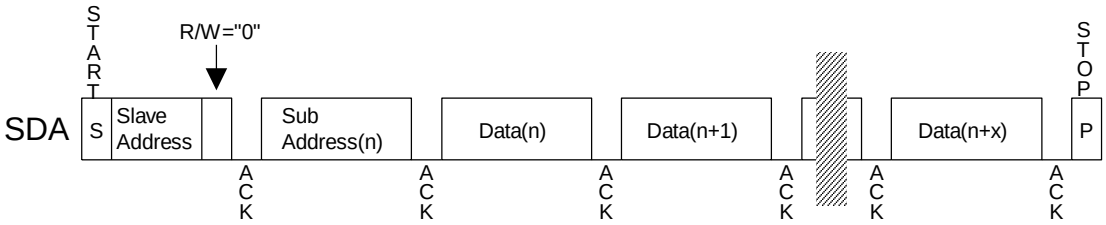


Figure 24. Data Transfer Sequence at the I²C-Bus

0	0	1	0	0	1	0	R/W

Figure 25. The First Byte

0	A6	A5	A4	A3	A2	A1	A0

Figure 26. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 27. Byte Structure after The Second Byte

READ Operations

Set the R/W bit = “1” for the READ operation of the AK4940. After transmission of data, the master can read the next address’s data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “09H” prior to generating stop condition, the address counter will “roll over” to “00H” and the data of “00H” will be read out.

The AK4940 supports two basic read operations: Current Address Read and Random Address Read.

(1) Current Address Read
The AK4940 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next CURRENT READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4940 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4940 ceases the transmission.

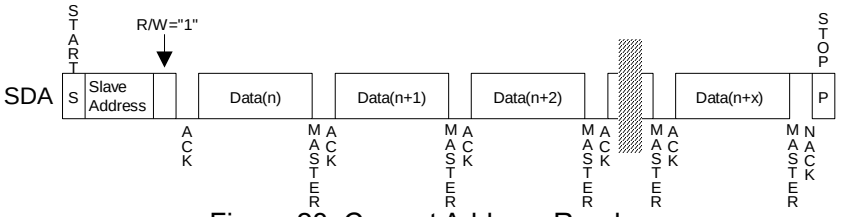


Figure 28. Current Address Read

(2) Random Address Read
The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit “1”, the master must first perform a “dummy” write operation. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit “1”. The AK4940 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4940 ceases the transmission.

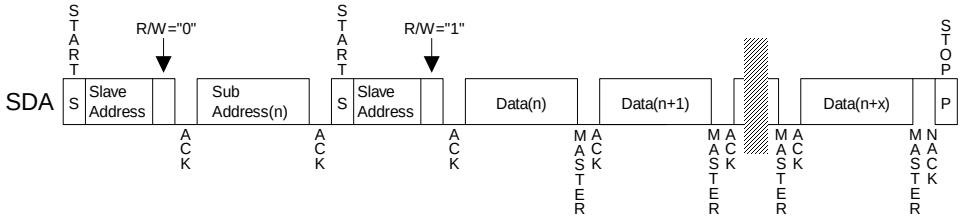


Figure 29. Random Address Read

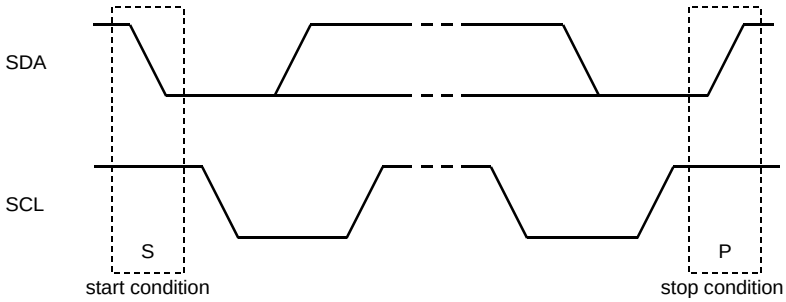


Figure 30. START and STOP Conditions

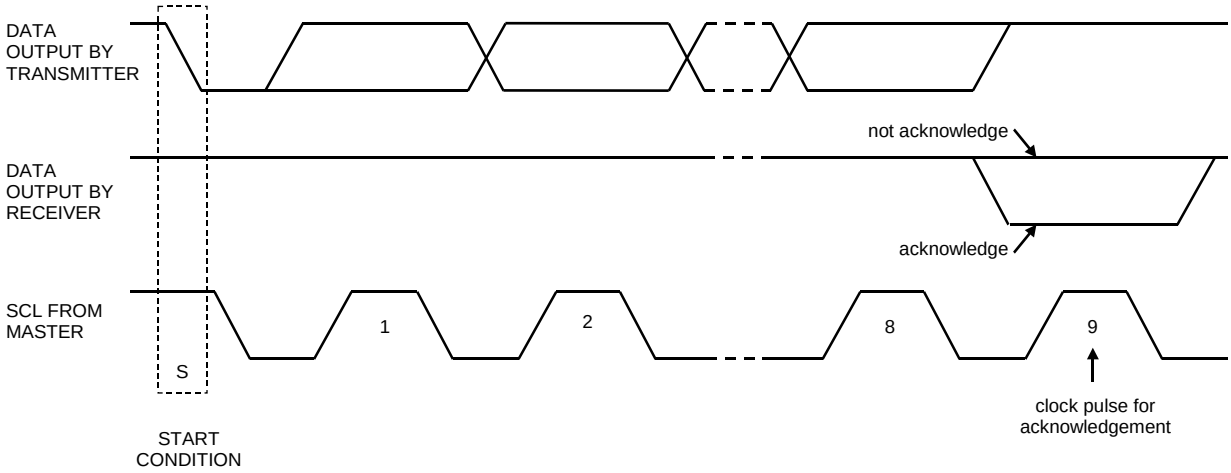


Figure 31. Acknowledge on the I²C-Bus

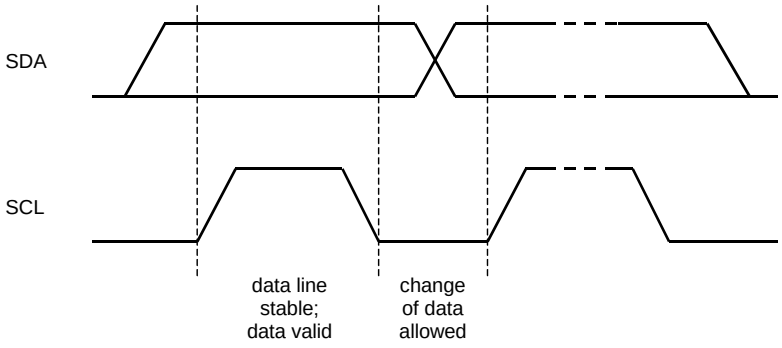


Figure 32. Bit Transfer on the I²C-Bus

Limitation in use of I2C Interface

The SDA and SCL pins have protection diodes against TVDD. Do not turn off the power of the AK4940 whenever the power supplies of other devices of the same system are turned on. Devices on the same I²C bus will not be able to communicate when TVDD = 0V since the SDA and SDL pins is connected to 0V via diodes. Pull-up resistors of SDA and SCL pins should be connected to TVDD or less voltage.

■ Register Map

Control registers can be initialized by setting the PDN pin = “L”.
Do not write "1" into bits described as 0.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Clock Management	0	0	0	0	CKRESETN	DFS2	DFS1	DFS0	00h
01h	Audio I/F Setting	LRIF1	LRIF0	DOFAD1	DOFAD0	DIFDA1	DIFDA0	BITFS1	BITFS0	00h
02h	ADC Control	BCKP	0	0	0	0	0	0	VOAD	00h
03h	Line Out Control	OUTNSEL	INV	OUT3SEL1	OUT3SEL0	OUT2SEL1	OUT2SEL0	OUT1SEL1	OUT1SEL0	00h
04h	Power Management	0	0	PMAD	PMDA	ADCSEL	ADDIFFN	0	CRESETN	00h
05h	Input Gain	0	0	0	0	MGN3	MGN2	MGN1	MGN0	02h
06h	ADC Digital Volume	VOLAD7	VOLAD6	VOLAD5	VOLAD4	VOLAD3	VOLAD2	VOLAD1	VOLAD0	30h
07h	DAC Digital Volume	VOLDA7	VOLDA6	VOLDA5	VOLDA4	VOLDA3	VOLDA2	VOLDA1	VOLDA0	18h
08h	Soft Mute Control	0	0	ADMUTE	ATSPAD	0	0	DAMUTE	ATSPDA	00h
09h	Reserved	0	0	0	0	0	0	0	0	00h

■ Register Definitions

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
00h	Clock Management	0	0	0	0	CKRESETN	DFS2	DFS1	DFS0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

CKRESETN: Clock Reset
0: Clock Reset (default)
1: Clock Reset Release

DFS[2:0]: Sampling Frequency Select

DFS[2:0]	fs		
	48kHz system	44.1kHz system	
000	8kHz	7.35kHz	(default)
001	12kHz	11.025kHz	
010	16kHz	14.7kHz	
011	24kHz	22.05kHz	
100	32kHz	29.4kHz	
101	48kHz	44.1kHz	
11x	N/A	N/A	

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
01h	Audio I/F Setting	LRIF1	LRIF0	DOFAD1	DOFAD0	DIFDA1	DIFDA0	BITFS1	BITFS0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LRIF[1:0]: Format Type Selection (Table 4)

DOFAD[1:0]: ADC Data Length and Data Position Selection (Table 4)

DIFDA[1:0]: DAC Data Length and Data Position Selection (Table 4)

BITFS[1:0]: BICK Frequency Selection (Table 4)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
02h	ADC Control	BCKP	0	0	0	0	0	0	VOAD
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

BCKP: BICK Edge Direction on LRCK Start Edge
- 0: Falling Edge (default)
- 1: Rising Edge

VOAD: ADC Digital Filter Selection
- 0: Sharp Roll-Off (default)
- 1: Voice

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
03h	Line Out Control	OUTNSEL	INV	OUT3SEL1	OUT3SEL0	OUT2SEL1	OUT2SEL0	OUT1SEL1	OUT1SEL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

OUTNSEL: DAC Lineout(-) Signal Selection (Table 7 (a), (b), (c))

INV: DAC Output Polarity Selection
- 0: Non-Invert (default)
- 1: Invert

OUT3SEL[1:0]: OUT3 pin Output Selection (Table 7 (c))

OUT2SEL[1:0]: OUTP2/OUTN2 pins Output Selection (Table 7 (b))

OUT1SEL[1:0]: OUTP1/OUTN1 pins Output Selection (Table 7 (a))

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
04h	Power Management	0	0	PMAD	PMDA	ADCSEL	ADDIFFN	0	CRESETN
R/W		RW	RW	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMAD: ADC Operation Selection
0: Reset State (default)
1: Normal Operation

PMDA: DAC Operation Selection
0: Reset State (default)
1: Normal Operation

ADCSEL: ADC Input Channel Selection
0: INP1, INN1 (default)
1: INP2, INN2

ADDIFFN: ADC Input Method Selection
0: Differential (default)
1: Single-ended, Pseudo-differential

CRESETN: ADC &DAC Reset
0: Reset (default)
1: Normal Operation

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
05h	Input Gain	0	0	0	0	MGN3	MGN2	MGN1	MGN0
R/W		R	R	R	R	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	1	0

MGN[3:0]: Input Block Amplifier Gain Setting (Table 8)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
06h	ADC Digital Volume	VOLAD7	VOLAD6	VOLAD5	VOLAD4	VOLAD3	VOLAD2	VOLAD1	VOLAD0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	0	0	0	0

VOLAD[7:0]: ADC Block Digital Volume Setting (Table 11)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
07h	DAC Digital Volume	VOLDA7	VOLDA6	VOLDA	VOLDA4	VOLDA3	VOLDA2	VOLDA1	VOLDA0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	1	0	0	0

VOLDA[7:0]: DAC Block Digital Volume Setting (Table 14)

Addr	Name	D7	D6	D5	D4	D3	D2	D1	D0
08h	Soft Mute Control	0	0	ADMUTE	ATSPAD	0	0	DAMUTE	ATSPDA
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

ADMUTE: ADC Block Soft Mute Control
0: Release Mute (default)
1: Start Mute

ATSPAD: ADC Block Soft Mute Transition Speed Selection
0: 4/fs (default)
1: 16/fs

DAMUTE: DAC Block Soft Mute Control
0: Release Mute (default)
1: Start Mute

ATSPDA: DAC Block Soft Mute Transition Speed Selection
0: 4/fs (default)
1: 16/fs

13. Recommended External Circuits

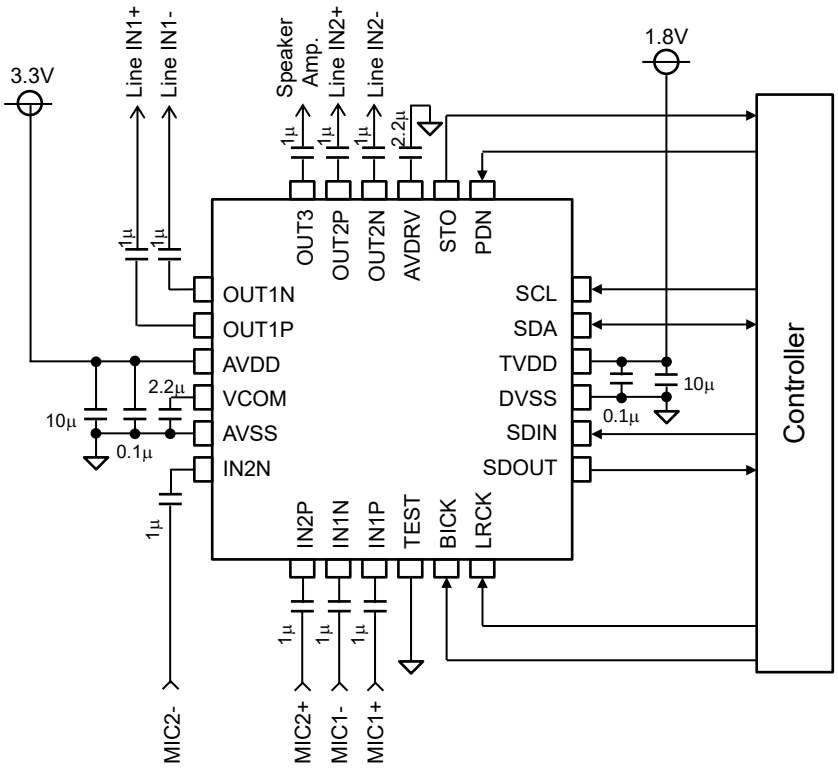


Figure 33. Differential Input 2ch, Differential Output 2ch, Single-ended Output 1ch

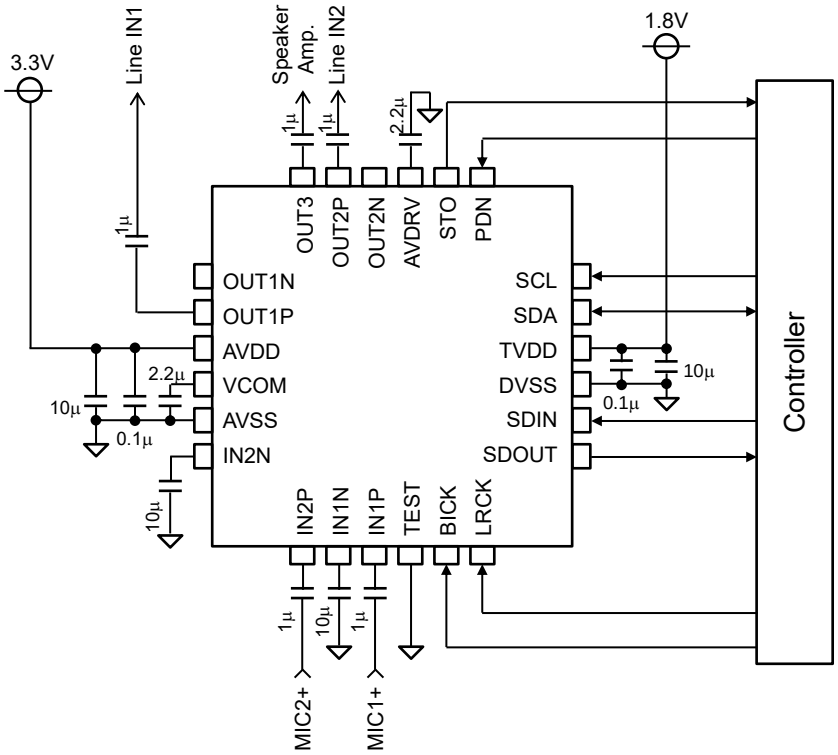


Figure 34. Single-ended Input 2ch, Single-ended Output 3ch

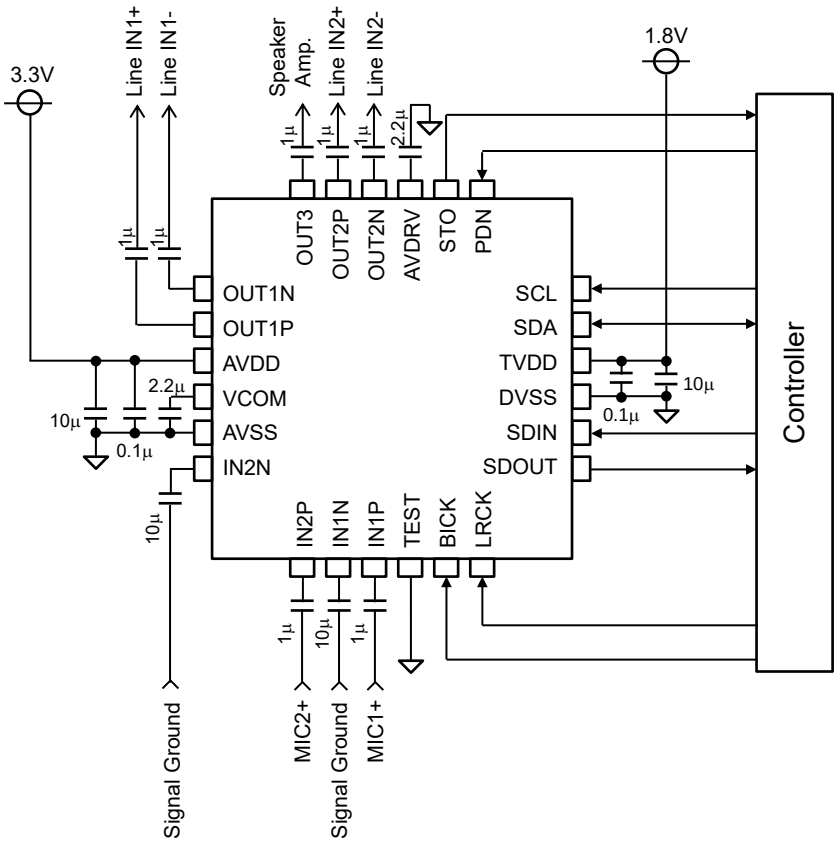


Figure 35. Pseudo-Differential Input 2ch, Pseudo-Differential Output 2ch, Single-ended Output 1ch

1. Ground

AVSS and DVSS should be connected to the same ground. Decoupling capacitors, particularly capacitors of small capacity, should be placed at positions as close as possible to the AK4940.

2. Reference Voltage

VCOM is a common voltage of this chip and the VCOM pin outputs AVDD/2. A 2.2μF capacitor should be connected between the VCOM pin and AVSS. Do not connect the VCOM pin to any external devices except the 2.2μF capacitor. Digital signal lines, especially clock signal line should be kept away as far as possible from this pin in order to avoid unwanted coupling into the AK4940.

3. Analog Input

The internal operating point level at the analog input pins of the AK4940 is VCOM voltage (AVDD/2). Concerning the internal operating point formation circuit, each input pin has impedance of 20kΩ (typ.) for the IN1P, and IN2P pins and 0.8 kΩ (typ.) for the IN1N and IN2N pins. After power-down is released, each analog input pin that is connected to an AC coupling capacitor becomes the same level as VCOM voltage by the impedance and required start-up time (time-constant).

The AK4940 samples the analog inputs at 512kHz when fs=8kHz. Digital filters remove noise around from 5kHz to 512kHz. The AK4940 includes a low-pass filter (fc=50kHz). This filter attenuates noises around 509.5kHz ~ 512kHz, which are not removed by the digital filters. Therefore no external low-pass filter is needed in front of the ADC since most of audio signals do not have a large noise around 509.5kHz. However, an external low-pass filter should be connected before the ADC for a signal which has large out-of-band noise such as D/A converted audio signals. Digital output code is 2‘s complement. DC offset is cancelled by the internal HPF.

The analog power supply to the AK4940 is +3.3V typical. A voltage more than AVDD + 0.3V or less than AVSS - 0.3V, and a current more than 10mA must not be applied to analog input pins. Excessive current will damage the internal protection circuit and will cause latch-up, destroying the IC. Accordingly, if the external analog circuit voltage is ±15V, the analog input pins must be protected from signals which are equal or larger than absolute maximum ratings.

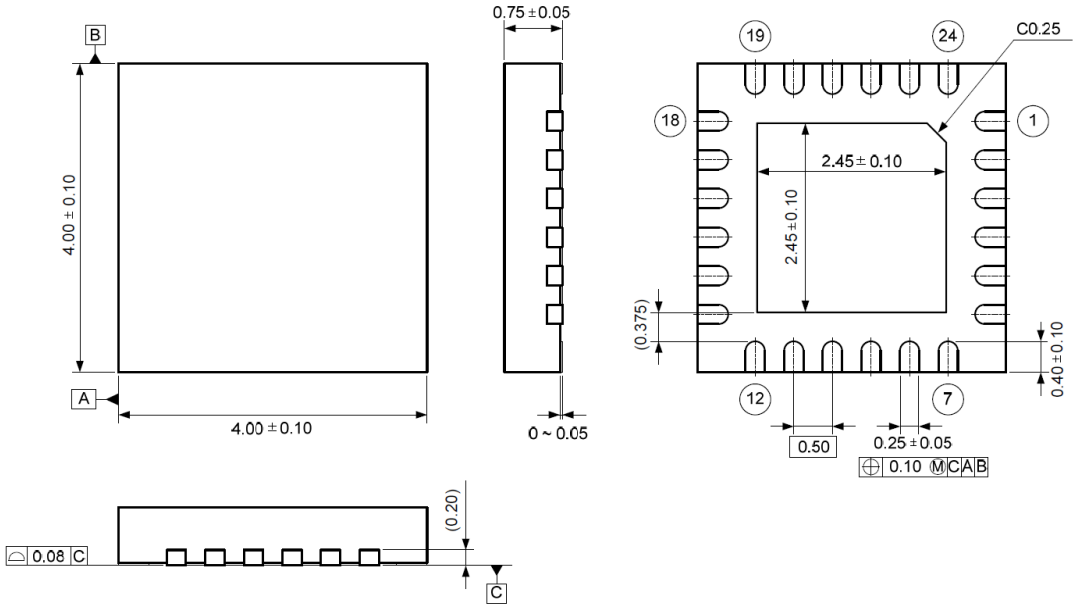
4. Analog Output

The analog output corresponds to both single-ended and differential outputs; it can be controlled by register setting. The digital input data format is two’s compliment. Positive full-scale output corresponds to 7FFFFFh (@24bit) input code, negative full-scale is 800000h (@24bit) and VCOM voltage ideally is 000000h (@24bit). The out-of-band noise (shaping noise) generated by the internal delta-sigma modulator is attenuated by an internal filter.

14. Package

■ Outline Dimensions

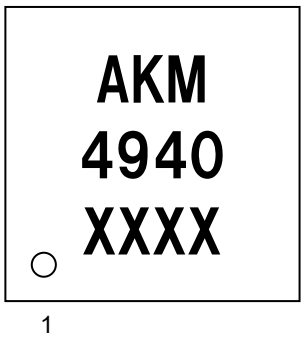
24-pin QFN (Unit: mm)



■ Material and Lead Finish

Package molding compound:	Epoxy resin
Lead frame materials:	Cu
Pin surface treatment:	Solder (Pb free) plate

■ Marking



1) Pin #1 indication
2) Date Code : XXXX (4 digits)
3) Marketing Code : 4940
4) AKM Logo: AKM

15. Ordering Guide

AK4940VN	−40 ~ +105°C	24-pin QFN (0.5mm pitch)
AKD4940	Evaluation Board for the AK4940	

16. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
18/06/21	00	First Edition		
19/01/18	01	Error Correction	7	Recommended Operating Conditions Note 4. “AVDD must be powered up before or at the same time of TVDD.” → “The power up sequence between AVDD and TVDD is not critical.”
		Error Correction	24	STO Pin (Status Output) “Once the STO pin output become “H”, …” → “Once the STO pin output become “L”, …

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