



# AK4331

## Low-Power Advanced 32-bit DAC with HP/SRC

## 1. General Description

The AK4331 is an advanced 32-bit high sound quality stereo audio DAC with a built-in ground-referenced headphone amplifier. The AK4331 has four types of 32-bit digital filters for better sound quality, achieving low distortion characteristics and wide dynamic range. The AK4331 also has a jitter cleaner with a built-in SRC and a X'tal. The AK4331 is available in a 36-pin CSP package, utilizing less board space than competitive offerings.

## 2. Features

1. High Sound Quality Low Power Advanced 32-bit Stereo DAC
  - 4 types of Digital Filter for Sound Color Selection
  - Short Delay Sharp Roll-off, GD = 5.5 / fs
  - Short Delay Slow Roll-off, GD = 4.5 / fs
  - Sharp Roll-off
  - Slow Roll-off
2. Ground-referenced Class-G Stereo Headphone Amplifier
  - Output Power: 70 mW @ 8Ω
  - THD+N: -100 dB
  - S/N: 109 dB
  - Output Noise Level: -114 dBV (Analog Volume = -10 dB)
  - Analog Volume: +4 to -10 dB, 2 dB Step
  - Ground Loop Noise Cancellation
3. Low Power Consumption: 4.4 mW (Play back, fs = 48 kHz, External Slave Mode)  
5.0 mW (Play back, fs = 48 kHz, PLL Slave Mode)
4. Headphone Amplifier Output Pins Comply with IEC61000-4-2 ESD Protection
  - ±8 kV Contact Discharge
5. Digital Audio interface
  - Master / Slave Mode
  - Sampling Frequency (Slave Mode / Master Mode):  
8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 64 k, 88.2 k, 96 k, 128 k,  
176.4 k, 192 kHz
  - Interface Format: 32/24/16-bit I<sup>2</sup>S/MSB justified
6. Asynchronous Sample Rate Converter
  - Up sample: up to ×6.02
7. Stereo Digital Microphone Interface
8. Power Management
9. PLL
10. Jitter Cleaner with a built-in SRC and X'tal Oscillator
11. μP Interface: I<sup>2</sup>C-bus (400 kHz)
12. Operation Temperature Range: Ta = -40 to 85 °C
13. Power Supply:
  - AVDD (DAC, PLL): 1.7 to 1.9 V
  - CVDD (Headphone Amplifier, Charge Pump): 1.7 to 1.9 V
  - LVDD (LDO2 for Digital Core): 1.7 to 1.9 V (built-in LDO)
  - TVDD (Digital Interface): 1.65 to 3.6 V
14. Pin Compatible and Register Backward Compatible with the AK4375A
15. Package: 36-pin CSP (2.533 × 2.371 mm, 0.4 mm pitch)

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#### 4. Block Diagram and Functions

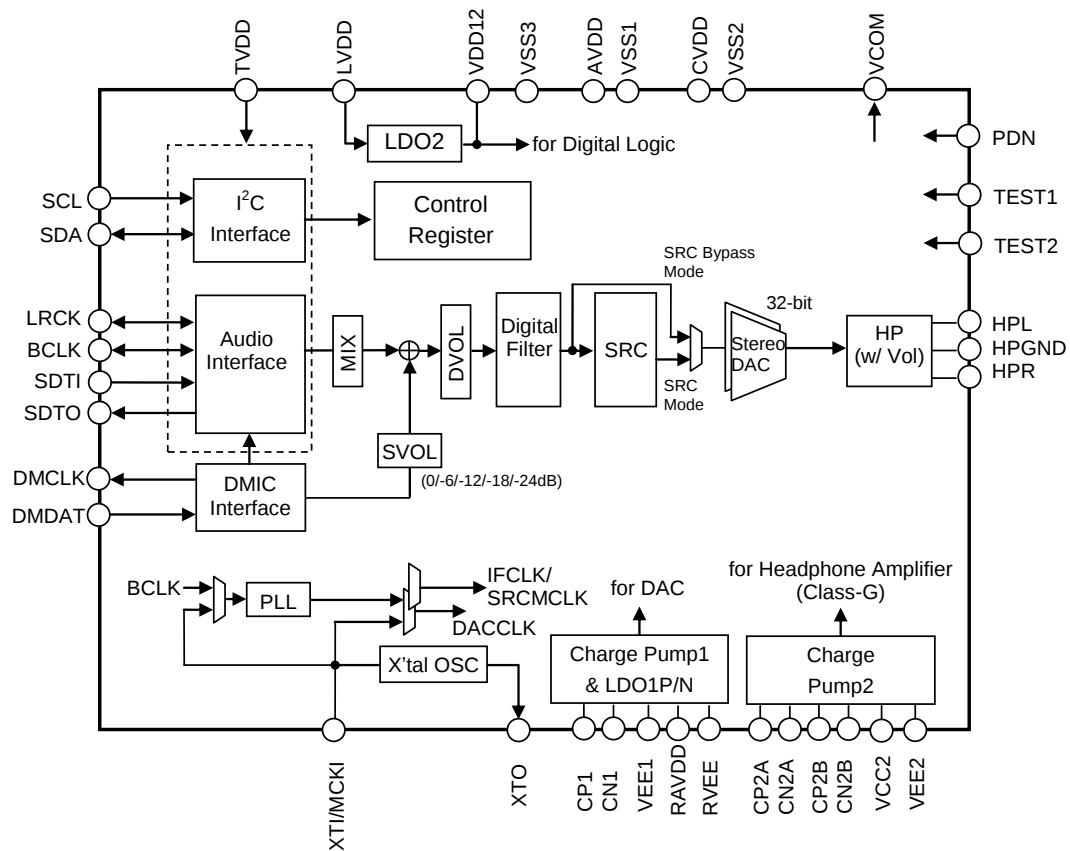
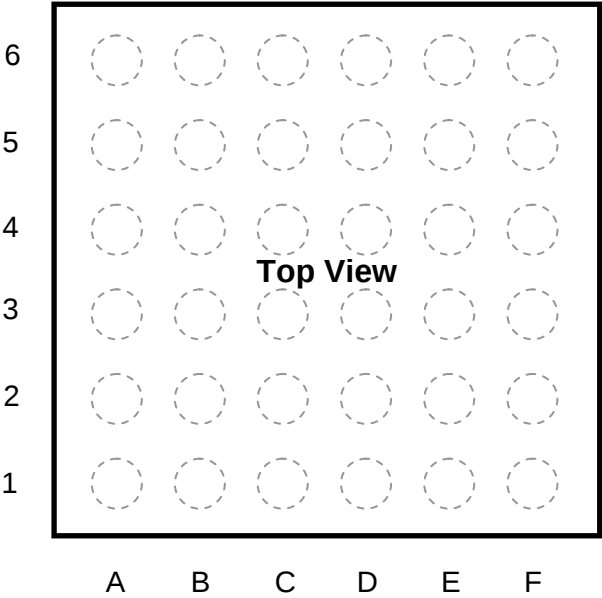


Figure 1. AK4331 Block Diagram

**5. Pin Configurations and Functions**

**5-1. Pin Configurations**

**36-pin CSP**



|   |              |       |       |       |      |       |
|---|--------------|-------|-------|-------|------|-------|
| 6 | VDD12        | LVDD  | CN1   | CP1   | CVDD | CN2B  |
| 5 | VSS3         | SDTI  | VEE1  | VSS2  | CP2B | CN2A  |
| 4 | TVDD         | LRCK  | SDA   | SCL   | CP2A | VEE2  |
| 3 | MCKI<br>/XTI | BCLK  | PDN   | TEST1 | VCC2 | HPR   |
| 2 | XTO          | DMDAT | TEST2 | VSS1  | HPL  | HPGND |
| 1 | SDTO         | DMCLK | RVEE  | RAVDD | AVDD | VCOM  |
|   | A            | B     | C     | D     | E    | F     |

**Top View**

## 5-2. Pin Function Difference with AK4375A

| Pin No. | AK4375A  |                                                                     | AK4331   |                                                                                                                       |
|---------|----------|---------------------------------------------------------------------|----------|-----------------------------------------------------------------------------------------------------------------------|
|         | Pin Name | Function                                                            | Pin Name | Function                                                                                                              |
| A1      | XTI      | X'tal Oscillator Input Pin<br>Left floating when not in use.        | SDTO     | Audio Serial Data Output Pin<br>Left floating when not in use.                                                        |
| A3      | MCKI     | External Master Clock Input Pin<br>Connect to VSS3 when not in use. | MCKI/XTI | External Master Clock Input / X'tal Oscillator Input Pin<br>Connect to VSS3 and set PMOSC bit to "0" when not in use. |
| B1      | TESTO    | Test Output Pin<br>Left floating when not in use.                   | DMCLK    | Digital MIC Clock Output Pin<br>Left floating when not in use.                                                        |
| B2      | LDO2E    | LDO2 Enable pin<br>This pin must be tied "H".                       | DMDAT    | Digital MIC Data Input Pin<br>Connect to VSS1 or AVDD when not in use.                                                |
| C2      | VSS4     | Ground4 pin<br>This pin must be tied "L".                           | TEST2    | Test Input pin<br>This pin must be tied "L".                                                                          |

### 5-3. Pin Functions

| No.                 | Pin Name | I/O | Function                                                                                                                  | Protection Diode | Power Domain |
|---------------------|----------|-----|---------------------------------------------------------------------------------------------------------------------------|------------------|--------------|
| <b>Power Supply</b> |          |     |                                                                                                                           |                  |              |
| E1                  | AVDD     | -   | Analog Power Supply Pin                                                                                                   | -                | AVDD         |
| D2                  | VSS1     | -   | Ground 1 Pin                                                                                                              | -                | -            |
| E6                  | CVDD     | -   | Headphone Amplifier / Charge Pump Power Supply Pin                                                                        | -                | CVDD         |
| D5                  | VSS2     | -   | Ground 2 Pin                                                                                                              | -                | -            |
| B6                  | LVDD     | -   | Digital Core & LDO2 Power Supply Pin                                                                                      | -                | LVDD         |
| A5                  | VSS3     | -   | Ground 3 Pin                                                                                                              | -                | -            |
| A4                  | TVDD     | -   | Digital Interface Power Supply Pin                                                                                        | -                | TVDD         |
| F1                  | VCOM     | O   | Common Voltage Output Pin<br>Connect a 2.2 $\mu\text{F}$ $\pm 50\%$ capacitor between this pin and the VSS1 pin. (Note 2) | AVDD / VSS1      | -            |
| A6                  | VDD12    | -   | LDO2 (1.2 V) Output Power Supply Pin (Note 1)<br>Connect a capacitor between this pin to the VSS3 pin. (Note 2)           | LVDD / VSS3      | LVDD         |

Note 1. Capacitor value connected to the VDD12 pin should be selected from 2.2  $\mu\text{F}$   $\pm 50\%$  to 4.7 $\mu\text{F}$   $\pm 50\%$ .

Note 2. Do not connect a load to the VCOM pin and the VDD12 pin.

| No.                          | Pin Name | I/O | Function                                                                                                                                                                                          | Protection Diode | Power Domain |
|------------------------------|----------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|--------------|
| <b>Charge Pump &amp; LDO</b> |          |     |                                                                                                                                                                                                   |                  |              |
| D6                           | CP1      | O   | Positive Charge Pump Capacitor Terminal 1 Pin<br>Connect a 2.2 $\mu\text{F}$ $\pm 50\%$ capacitor between this pin and the CN1 pin.                                                               | CVDD / VSS2      | CVDD         |
| C6                           | CN1      | I   | Negative Charge Pump Capacitor Terminal 1 Pin<br>Connect a 2.2 $\mu\text{F}$ $\pm 50\%$ capacitor between this pin and the CP1 pin.                                                               | CVDD             | CVDD         |
| C5                           | VEE1     | O   | Charge Pump Circuit Negative Voltage ( $-\text{CVDD}$ ) Output 1 Pin<br>Connect a 2.2 $\mu\text{F}$ $\pm 50\%$ capacitor between this pin and the VSS2 pin. (Note 3)                              | CVDD / VSS2      | -            |
| D1                           | RAVDD    | O   | LDO1P (1.5 V) Output Pin (Note 4)<br>Connect a capacitor between this pin and the VSS1 pin. (Note 3)                                                                                              | AVDD / VSS1      | -            |
| C1                           | RVEE     | O   | LDO1N ( $-1.5$ V) Output Pin (Note 4)<br>Connect a capacitor between this pin and the VSS1 pin. (Note 3)                                                                                          | AVDD / VSS1      | -            |
| E3                           | VCC2     | O   | Charge Pump Circuit Positive Voltage ( $\text{CVDD}$ or $1/2 \times \text{CVDD}$ ) Output Pin<br>Connect a 2.2 $\mu\text{F}$ $\pm 50\%$ capacitor between this pin and the VSS2 pin. (Note 3)     | CVDD / VSS2      | CVDD         |
| E4                           | CP2A     | O   | Positive Charge Pump Capacitor Terminal 2A Pin<br>Connect a 2.2 $\mu\text{F}$ $\pm 50\%$ capacitor between this pin and the CN2A pin.                                                             | CVDD / VSS2      | CVDD         |
| F5                           | CN2A     | I   | Negative Charge Pump Capacitor Terminal 2A Pin<br>Connect a 2.2 $\mu\text{F}$ $\pm 50\%$ capacitor between this pin and the CP2A pin.                                                             | CVDD             | CVDD         |
| E5                           | CP2B     | O   | Positive Charge Pump Capacitor Terminal 2B Pin<br>Connect a 2.2 $\mu\text{F}$ $\pm 50\%$ capacitor between this pin and the CN2B pin.                                                             | CVDD / VSS2      | CVDD         |
| F6                           | CN2B     | I   | Negative Charge Pump Capacitor Terminal 2B Pin<br>Connect a 2.2 $\mu\text{F}$ $\pm 50\%$ capacitor between this pin and the CP2B pin.                                                             | CVDD             | CVDD         |
| F4                           | VEE2     | O   | Charge Pump Circuit Negative Voltage ( $-\text{CVDD}$ or $-1/2 \times \text{CVDD}$ ) Output 2 Pin<br>Connect a 2.2 $\mu\text{F}$ $\pm 50\%$ capacitor between this pin and the VSS2 pin. (Note 3) | CVDD / VSS2      | -            |

Note 3. Do not connect a load to the VEE1 pin, VCC2 pin, VEE2 pin, RAVDD pin and the RVEE pin.

Note 4. Capacitor value connected to the RAVDD pin and the RVEE pin should be selected from 1.0  $\mu\text{F}$   $\pm 50\%$  to 4.7  $\mu\text{F}$   $\pm 50\%$ .

| No.                          | Pin Name | I/O | Function                                               | Protection Diode | Power Domain |
|------------------------------|----------|-----|--------------------------------------------------------|------------------|--------------|
| <b>Control Interface</b>     |          |     |                                                        |                  |              |
| D4                           | SCL      | I   | I <sup>2</sup> C Serial Data Clock Pin                 | TVDD / VSS3      | TVDD         |
| C4                           | SDA      | I/O | I <sup>2</sup> C Serial Data Input/Output Pin          | TVDD / VSS3      | TVDD         |
| <b>Audio Interface</b>       |          |     |                                                        |                  |              |
| A3                           | MCKI     | I   | External Master Clock Input Pin<br>(PMOSC bit = "0")   | TVDD / VSS3      | TVDD         |
|                              | XTI      | I   | X'tal Oscillator Input Pin<br>(PMOSC bit = "1")        |                  |              |
| A1                           | SDTO     | O   | Audio Serial Data Output Pin                           | TVDD / VSS3      | TVDD         |
| A2                           | XTO      | O   | X'tal Oscillator Output Pin                            | TVDD / VSS3      | TVDD         |
| B3                           | BCLK     | I/O | Audio Serial Data Clock Pin                            | TVDD / VSS3      | TVDD         |
| B4                           | LRCK     | I/O | Frame Sync Clock Pin                                   | TVDD / VSS3      | TVDD         |
| B5                           | SDTI     | I   | Audio Serial Data Input Pin                            | TVDD / VSS3      | TVDD         |
| <b>Analog Output</b>         |          |     |                                                        |                  |              |
| E2                           | HPL      | O   | Lch Headphone Amplifier Output Pin                     | CVDD / VEE2      | CVDD / VEE2  |
| F3                           | HPR      | O   | Rch Headphone Amplifier Output Pin                     | CVDD / VEE2      | CVDD / VEE2  |
| F2                           | HPGND    | I   | Headphone Amplifier Ground Loop Noise Cancellation Pin | -                | -            |
| <b>Digital MIC Interface</b> |          |     |                                                        |                  |              |
| B1                           | DMCLK    | O   | Digital MIC Clock Output Pin                           | AVDD / VSS1      | AVDD         |
| B2                           | DMDAT    | I   | Digital MIC Data Input Pin                             | AVDD / VSS1      | AVDD         |
| <b>Others</b>                |          |     |                                                        |                  |              |
| C3                           | PDN      | I   | Power down Pin<br>"L": Power-Down, "H": Power-Up       | TVDD / VSS3      | TVDD         |
| D3                           | TEST1    | I   | Test Input 1 Pin<br>It must be tied "L".               | TVDD / VSS3      | TVDD         |
| C2                           | TEST2    | I   | Test Input 2 Pin<br>It must be tied "L".               | TVDD / VSS3      | TVDD         |

Note 5. The SCL pin, SDA pin, MCKI/XTI pin, BCLK pin, LRCK pin, SDTI pin, HPGND pin, DMDAT pin, PDN pin, TEST1 pin and the TEST2 pin must not be allowed to float.

**5-4. Handing of Unused Pins**

Unused I/O pins must be connected appropriately.

| Classification | Pin Name               | Setting                 |
|----------------|------------------------|-------------------------|
| Analog         | HPL, HPR               | Open                    |
| Digital        | MCKI/XTI, TEST1, TEST2 | Connect to VSS3         |
|                | DMCLK, SDTO, XTO       | Open                    |
|                | DMDAT                  | Connect to VSS1 or AVDD |

## 6. Absolute Maximum Ratings

(VSS1 = VSS2 = VSS3 = 0 V; [Note 7](#), [Note 8](#))

| Parameter                                           | Symbol | Min. | Max.               | Unit |
|-----------------------------------------------------|--------|------|--------------------|------|
| Power Supplies:                                     |        |      |                    |      |
| Analog                                              | AVDD   | -0.3 | 4.3                | V    |
| Headphone Amplifier / Charge Pump                   | CVDD   | -0.3 | 4.3                | V    |
| LDO2 for Digital Core                               | LVDD   | -0.3 | 4.3                | V    |
| Digital Interface                                   | TVDD   | -0.3 | 4.3                | V    |
| Input Current, Any Pin Except Supplies              | IIN    | -    | ±10                | mA   |
| Digital Input Voltage 1 ( <a href="#">Note 9</a> )  | VIND1  | -0.3 | AVDD+0.3<br>or 4.3 | V    |
| Digital Input Voltage 2 ( <a href="#">Note 10</a> ) | VIND2  | -0.3 | TVDD+0.3<br>or 4.3 | V    |
| Ambient Temperature (powered applied)               | Ta     | -40  | 85                 | °C   |
| Storage Temperature                                 | Tstg   | -65  | 150                | °C   |

Note 6. Charge pump 1 & 2 are not in operation. In the case that charge pump 1 & 2 are in operation, the maximum values of AVDD and CVDD become 2.15 V.

Note 7. All voltages with respect to ground.

**Note 8. VSS1, VSS2 and VSS3 must be connected to the same analog plane.**

Note 9. DMDAT pin

The maximum value of input voltage is lower value between (AVDD+0.3) V and 4.3 V.

Note 10. MCKI/XTI, BCLK, LRCK, SDTI, SCL, SDA, PDN, TEST1, TEST2 pins

The maximum value of input voltage is lower value between (TVDD+0.3) V and 4.3 V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal Operation is not guaranteed at these extremes.

## 7. Recommended Operating Conditions

(VSS1 = VSS2 = VSS3 = 0 V; [Note 11](#))

| Parameter                         | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------------------|--------|------|------|------|------|
| Power Supplies:                   |        |      |      |      |      |
| Analog                            | AVDD   | 1.7  | 1.8  | 1.9  | V    |
| Headphone Amplifier / Charge Pump | CVDD   | 1.7  | 1.8  | 1.9  | V    |
| LDO2 for Digital Core             | LVDD   | 1.7  | 1.8  | 1.9  | V    |
| Digital Interface                 | TVDD   | 1.65 | 1.8  | 3.6  | V    |

Note 11. All voltages with respect to ground.

Note 12. Each power up/down sequence is shown below.

<Power-Up>

1. PDN pin = "L"
2. TVDD, AVDD, LVDD and CVDD are powered up.  
(AVDD must be powered up before or at the same time of CVDD. The power-up sequence of TVDD and LVDD is not critical.)
3. The PDN pin is allowed to be "H" after all power supplies are applied and settled.

<Power-down>

1. PDN pin = "L"
2. TVDD, AVDD, LVDD and CVDD are powered down.  
(CVDD must be powered down before or at the same time of AVDD. The power-down sequence of TVDD and LVDD is not critical.)

## 8. Electrical Characteristics

### 8-1. DAC Analog Characteristics

( $T_a = 25^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = TVDD = 1.8\text{ V}$ ;  $VSS1 = VSS2 = VSS3 = \text{HPGND} = 0\text{ V}$ ; Signal Frequency = 1 kHz; 24-bit Data;  $f_s = 48\text{ kHz}$ ,  $\text{BCLK} = 64\text{fs}$ ; Measurement Bandwidth = 20 Hz to 20 kHz,  $\text{OVL/R} = 0\text{ dB}$ ,  $R_L = 32\Omega$ , SELDAIN bit = "0"; unless otherwise specified)

| Parameter                                                                                                                   | Min.                        | Typ.    | Max.       | Unit   |          |
|-----------------------------------------------------------------------------------------------------------------------------|-----------------------------|---------|------------|--------|----------|
| Stereo DAC Characteristics:                                                                                                 |                             |         |            |        |          |
| Resolution                                                                                                                  | -                           | -       | 32         | Bits   |          |
| Headphone Amplifier Characteristics: DAC (Stereo) → HPL/HPR pins                                                            |                             |         |            |        |          |
| Output Power                                                                                                                |                             |         |            |        |          |
| 0 dBFS, R <sub>L</sub> = 32Ω, HPG = 0 dB                                                                                    | -                           | 25      | -          | mW     |          |
| 0 dBFS, R <sub>L</sub> = 32Ω, HPG = -4 dB                                                                                   | -                           | 10      | -          | mW     |          |
| R <sub>L</sub> = 16Ω, HPG = 0 dB, THD+N < -60 dB                                                                            | -                           | 45      | -          | mW     |          |
| R <sub>L</sub> = 8Ω, HPG = +2 dB, THD+N < -20 dB                                                                            | -                           | 70      | -          | mW     |          |
| Output Level (0 dBFS, R <sub>L</sub> = 32Ω, HPG = -4 dB) (Note 13)                                                          | 0.52                        | 0.57    | 0.61       | Vrms   |          |
| THD+N                                                                                                                       |                             |         |            |        |          |
| 0 dBFS, R <sub>L</sub> = 32Ω, HPG = -4 dB<br>(Po = 10 mW)                                                                   | fs = 48 kHz<br>BW = 20 kHz  | -       | -100       | -90    | dB       |
|                                                                                                                             | fs = 96 kHz<br>BW = 40 kHz  | -       | -97        | -      | dB       |
|                                                                                                                             | fs = 192 kHz<br>BW = 40 kHz | -       | -97        | -      | dB       |
| -60 dBFS, R <sub>L</sub> = 32Ω, HPG = -4 dB                                                                                 | fs = 48 kHz<br>BW = 20 kHz  | -       | -44        | -      | dB       |
|                                                                                                                             | fs = 96 kHz<br>BW = 40 kHz  | -       | -40        | -      | dB       |
|                                                                                                                             | fs = 192 kHz<br>BW = 40 kHz | -       | -40        | -      | dB       |
| Dynamic Range<br>-60 dBFS, A-weighted, HPG = -4 dB                                                                          |                             | -       | 107        | -      | dB       |
| S/N (A-weighted)<br>Po = 25 mW, HPG = 0 dB (Data = 0 dBFS / “0” Data)<br>Po = 10 mW, HPG = -4 dB (Data = 0 dBFS / “0” Data) |                             | -<br>99 | 109<br>107 | -<br>- | dB<br>dB |
| Output Noise Level<br>(A-weighted, HPG = -10 dB)                                                                            |                             | -       | -114       | -106   | dBV      |

Note 13. Output level is proportional to  $AVDD$ . Typ.  $0.57\text{ Vrms} \times AVDD / 1.8\text{ V}$  @headphone amplifier gain = -4 dB.

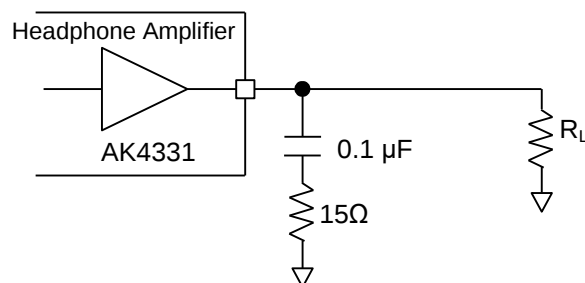


Figure 2. External Circuit for Headphone Amplifier

| Parameter                                                                                          | Min.               | Typ. | Max.  | Unit |
|----------------------------------------------------------------------------------------------------|--------------------|------|-------|------|
| Interchannel Isolation<br>0 dBFS, HPG = -4 dB (Po = 10 mW)<br>External Impedance = 0.09Ω (Note 14) | 80                 | 100  | -     | dB   |
| Interchannel Gain Mismatch                                                                         | -                  | 0    | 0.8   | dB   |
| Load Resistance                                                                                    | 7.2                | 32   | -     | Ω    |
| Load Capacitance                                                                                   | -                  | -    | 500   | pF   |
| Load Inductance                                                                                    | -                  | -    | 0.375 | μH   |
| PSRR (HPG = -4 dB) (Note 15)                                                                       |                    |      |       |      |
| 217 Hz                                                                                             | -                  | 85   | -     | dB   |
| 1 kHz                                                                                              | -                  | 85   | -     | dB   |
| DC-offset (Note 16)                                                                                |                    |      |       |      |
| HPG = 0 dB                                                                                         | -0.15              | 0    | +0.15 | mV   |
| HPG = All gain                                                                                     | -0.2               | 0    | +0.2  | mV   |
| <b>Headphone Output Volume Characteristics:</b>                                                    |                    |      |       |      |
| Gain Setting                                                                                       | -10                | -    | +4    | dB   |
| Step Width                                                                                         | Gain: +4 to -10 dB |      | 1     | 2    |
|                                                                                                    |                    |      | 3     | dB   |

Note 14. Impedance between the HPGND pin and the system ground.

Note 15. PSRR is referred to all power supplies with 100 mVpp sine wave.

Note 16. When there is no gain change and temperature drift after headphone amplifier is powered up.

| Parameter                                              | Value | Unit |
|--------------------------------------------------------|-------|------|
| ESD Immunity<br>IEC61000-4-2 Level4, Contact (Note 17) | ±8    | kV   |

Note 17. It is measured at the HPL and HPR pins on an evaluation board (AKD4331-SA Rev.1).

### 8-2. PLL Characteristics

(Ta = -40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; unless otherwise specified)

| Parameter                  | Min.                 | Typ. | Max.    | Unit |
|----------------------------|----------------------|------|---------|------|
| <b>PLL Characteristics</b> |                      |      |         |      |
| Reference Clock (Note 15)  | 76.8                 | -    | 768     | kHz  |
| PLLCLK Frequency (Note 15) | 44.1 kHz × 256fs × 2 | -    | 22.5792 | MHz  |
|                            | 48.0 kHz × 256fs × 2 | -    | 24.576  | MHz  |
| Lock Time                  | -                    | -    | 2       | msec |

### 8-3. Charge Pump & LDO Circuit Power-Up Time

(Ta = -40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; unless otherwise specified)

| Parameter                        | Capacitor   | Min. | Typ. | Max. | Unit |
|----------------------------------|-------------|------|------|------|------|
| <b>Block Power-Up Time</b>       |             |      |      |      |      |
| CP1 (Note 18)                    | -           | -    | -    | 6.5  | msec |
| CP2 (Class-G) (Note 18, Note 19) | -           | -    | -    | 4.5  | msec |
| LDO1P (Note 20)                  | 1 μF @RAVDD | -    | -    | 0.5  | msec |
| LDO1N (Note 20)                  | 1 μF @RVEE  | -    | -    | 0.5  | msec |
| LDO2 (Note 18)                   | -           | -    | -    | 1    | msec |

Note 18. Power-up time is a fixed value that is not affected by a capacitor.

Note 19. Power-up time is a value to  $-1/2 \times CVDD$ , since CP2 starts with 1/2VDD Mode as part of Class-G operation.

Note 20. Power-up time is proportional to a capacitor value. For instance, if a 2.2 μF capacitor is connected to the RAVDD pin, LDO1P power-up time is 1.1 msec at maximum.

#### 8-4. Power Supply Current

(Ta = 25°C; AVDD = CVDD = LVDD = TVDD = 1.8 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; unless otherwise specified)

| Parameter                                                 | Min. | Typ. | Max. | Unit |
|-----------------------------------------------------------|------|------|------|------|
| <b>Power Supply Current:</b>                              |      |      |      |      |
| Power Up (PDN pin = "H", All Circuits Power-Up) (Note 21) |      |      |      |      |
| AVDD + CVDD + LVDD + TVDD                                 | -    | 4.1  | 6.1  | mA   |
| Power Down (PDN pin = "L") (Note 22)                      |      |      |      |      |
| AVDD + CVDD + LVDD + TVDD                                 | -    | 0    | 10   | μA   |

Note 21. fso/fsi = 48 kHz/48 kHz, MCKI = 256fs, BCLK = 64fs; No data input, RL = 32Ω, DAC, Headphone Amplifier, PLL & X'tal & SRC & DMIC Power-Up

Note 22. The DMDAT pin is fixed to AVDD or VSS1 and other digital input pins are fixed to TVDD or VSS3.

#### 8-5. Power Consumptions for Each Operation Mode

(Ta = 25°C; AVDD = CVDD = LVDD = TVDD = 1.8 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; SRC Bypass Mode, MCKI = 256fs, BCLK = 64fs; No data input, RL = 32Ω, X'tal & DMIC OFF)

Table 1. Power Consumption (Typ.) for Each Operation Mode

| Mode                                                              | Typical Current [mA] |      |      |      | Total Power [mW] |
|-------------------------------------------------------------------|----------------------|------|------|------|------------------|
|                                                                   | AVDD                 | CVDD | LVDD | TVDD |                  |
| DAC → Headphone (fs = 48 kHz), External Slave Mode                | 0.79                 | 1.37 | 0.27 | 0.01 | 4.4              |
| DAC → Headphone (fs = 96 kHz), External Slave Mode                | 0.87                 | 1.69 | 0.36 | 0.01 | 5.3              |
| DAC → Headphone (fs = 192 kHz), External Slave Mode, MCKI = 128fs | 0.87                 | 1.69 | 0.44 | 0.01 | 5.4              |
| DAC → Headphone (fs = 48 kHz), External Slave Mode, DMIC enable   | 0.79                 | 1.37 | 0.69 | 0.01 | 5.1              |
| DAC → Headphone (fs = 96 kHz), External Slave Mode, DMIC enable   | 0.87                 | 1.69 | 1.16 | 0.01 | 6.7              |
| DAC → Headphone (fs = 48 kHz), PLL Slave Mode                     | 1.06                 | 1.37 | 0.31 | 0.01 | 5.0              |
| DAC → Headphone (fs = 96 kHz), PLL Slave Mode                     | 1.14                 | 1.69 | 0.41 | 0.01 | 5.9              |
| DAC → Headphone (fs = 192 kHz), PLL Slave Mode                    | 1.14                 | 1.69 | 0.49 | 0.01 | 6.0              |

#### 8-6. SRC Characteristics

(Ta = -40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = 0 V; unless otherwise specified)

| Parameter                                  | Symbol  | Min. | Typ. | Max. | Unit |
|--------------------------------------------|---------|------|------|------|------|
| Resolution                                 |         | -    | -    | 32   | Bits |
| Input Sample Rate                          | FSI     | 8    | -    | 192  | kHz  |
| Output Sample Rate                         | FSO     | 8    | -    | 192  | kHz  |
| Ratio between Input and Output Sample Rate | FSO/FSI | 0.98 | -    | 6.02 | -    |

## 8-7. DAC Sharp Roll-Off Filter Characteristics (SRC Bypass Mode)

### 8-7-1. Sharp Roll-Off Filter (SRC Bypass Mode, $f_s = 48$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 48$  kHz; DASD bit = "0", DASL bit = "0", SELDAIN bit = "0", DADFSEL bit = "0")

| Parameter                                                       | Symbol                        | Min. | Typ.   | Max.       | Unit       |
|-----------------------------------------------------------------|-------------------------------|------|--------|------------|------------|
| <b>DAC Digital Filter (LPF):</b>                                |                               |      |        |            |            |
| Passband<br>(Note 23)                                           | –0.006 to +0.23 dB<br>–6.0 dB | PB   | 0<br>– | –<br>24.02 | kHz<br>kHz |
| Stopband (Note 23)                                              |                               | SB   | 26.2   | –          | kHz        |
| Passband Ripple                                                 |                               | PR   | –0.006 | –          | dB         |
| Stopband Attenuation (Note 24)                                  |                               | SA   | 69.8   | –          | dB         |
| Group Delay (Note 25)                                           |                               | GD   | –      | 25.8       | 1/fs       |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                               |      |        |            |            |
| Frequency Response: 0 to 20.0 kHz                               |                               | FR   | –0.12  | –          | dB         |

Note 23. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.467 \times f_s$  (@–0.006/+0.23 dB), SB =  $0.5465 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 24. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 25. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

### 8-7-2. Sharp Roll-Off Filter (SRC Bypass Mode, $f_s = 96$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 96$  kHz; DASD bit = "0", DASL bit = "0", SELDAIN bit = "0", DADFSEL bit = "0")

| Parameter                                                       | Symbol                        | Min. | Typ.   | Max.       | Unit       |
|-----------------------------------------------------------------|-------------------------------|------|--------|------------|------------|
| <b>DAC Digital Filter (LPF):</b>                                |                               |      |        |            |            |
| Passband<br>(Note 26)                                           | –0.003 to +0.24 dB<br>–6.0 dB | PB   | 0<br>– | –<br>48.04 | kHz<br>kHz |
| Stopband (Note 26)                                              |                               | SB   | 52.5   | –          | kHz        |
| Passband Ripple                                                 |                               | PR   | –0.003 | –          | dB         |
| Stopband Attenuation (Note 27)                                  |                               | SA   | 69.8   | –          | dB         |
| Group Delay (Note 28)                                           |                               | GD   | –      | 25.8       | 1/fs       |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                               |      |        |            |            |
| Frequency Response: 0 to 40.0 kHz                               |                               | FR   | –1.69  | –          | dB         |

Note 26. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.4672 \times f_s$  (@–0.003/+0.24 dB), SB =  $0.547 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 27. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 28. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

**8-7-3. Sharp Roll-Off Filter (SRC Bypass Mode,  $f_s = 192$  kHz)**

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 192$  kHz; DASD bit = "0", DASL bit = "0", SELDAIN bit = "0", DADFSEL bit = "0")

| Parameter                                                       | Symbol                        | Min. | Typ.   | Max.       | Unit                     |
|-----------------------------------------------------------------|-------------------------------|------|--------|------------|--------------------------|
| <b>DAC Digital Filter (LPF):</b>                                |                               |      |        |            |                          |
| Passband<br>(Note 29)                                           | -0.002 to +0.24 dB<br>-6.0 dB | PB   | 0<br>- | -<br>96.08 | 89.74<br>-<br>kHz<br>kHz |
| Stopband (Note 29)                                              |                               | SB   | 104.9  | -          | -<br>kHz                 |
| Passband Ripple                                                 |                               | PR   | -0.002 | -          | +0.24<br>dB              |
| Stopband Attenuation (Note 30)                                  |                               | SA   | 69.8   | -          | -<br>dB                  |
| Group Delay (Note 31)                                           |                               | GD   | -      | 25.8       | -<br>1/ $f_s$            |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                               |      |        |            |                          |
| Frequency Response: 0 to 80.0 kHz                               |                               | FR   | -8.23  | -          | +0.35<br>dB              |

Note 29. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.4674 \times f_s$  (@-0.002/+0.24 dB), SB =  $0.5465 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 30. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 31. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/ $f_s$ ].

## 8-8. DAC Slow Roll-Off Filter Characteristics (SRC Bypass Mode)

### 8-8-1. Slow Roll-Off Filter (SRC Bypass Mode, $f_s = 48$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 48$  kHz; DASD bit = "0", DASL bit = "1", SELDAIN bit = "0", DADFSEL bit = "0")

| Parameter                                                       | Symbol                              | Min. | Typ.    | Max.       | Unit       |
|-----------------------------------------------------------------|-------------------------------------|------|---------|------------|------------|
| <b>DAC Digital Filter (LPF):</b>                                |                                     |      |         |            |            |
| Passband<br>(Note 32)                                           | $-0.07$ to $+0.005$ dB<br>$-3.0$ dB | PB   | 0<br>-  | -<br>20.15 | kHz<br>kHz |
| Stopband (Note 32)                                              |                                     | SB   | 42.59   | -          | kHz        |
| Passband Ripple                                                 |                                     | PR   | $-0.07$ | -          | dB         |
| Stopband Attenuation (Note 33)                                  |                                     | SA   | 72.8    | -          | dB         |
| Group Delay (Note 34)                                           |                                     | GD   | -       | 25.8       | 1/fs       |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                                     |      |         |            |            |
| Frequency Response: 0 to 20.0 kHz                               |                                     | FR   | $-3.21$ | -          | dB         |

Note 32. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.1769 \times f_s$  (@ $-0.07/+0.005$  dB), SB =  $0.887 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 33. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 34. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within  $\pm 1$  [1/fs].

### 8-8-2. Slow Roll-Off Filter (SRC Bypass Mode, $f_s = 96$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 96$  kHz; DASD bit = "0", DASL bit = "1", SELDAIN bit = "0", DADFSEL bit = "0")

| Parameter                                                       | Symbol                              | Min. | Typ.    | Max.      | Unit       |
|-----------------------------------------------------------------|-------------------------------------|------|---------|-----------|------------|
| <b>DAC Digital Filter (LPF):</b>                                |                                     |      |         |           |            |
| Passband<br>(Note 35)                                           | $-0.07$ to $+0.006$ dB<br>$-3.0$ dB | PB   | 0<br>-  | -<br>40.3 | kHz<br>kHz |
| Stopband (Note 35)                                              |                                     | SB   | 85.15   | -         | kHz        |
| Passband Ripple                                                 |                                     | PR   | $-0.07$ | -         | dB         |
| Stopband Attenuation (Note 36)                                  |                                     | SA   | 72.8    | -         | dB         |
| Group Delay (Note 37)                                           |                                     | GD   | -       | 25.8      | 1/fs       |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                                     |      |         |           |            |
| Frequency Response: 0 to 40.0 kHz                               |                                     | FR   | $-4.84$ | -         | dB         |

Note 35. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.1773 \times f_s$  (@ $-0.07/+0.006$  dB), SB =  $0.887 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 36. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 37. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within  $\pm 1$  [1/fs].

**8-8-3. Slow Roll-Off Filter (SRC Bypass Mode,  $f_s = 192$  kHz)**

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 192$  kHz;  $DASD$  bit = "0",  $DASL$  bit = "1",  $SELDAIN$  bit = "0",  $DADFSEL$  bit = "0")

| Parameter                                                       | Symbol                        | Min. | Typ.   | Max.       | Unit              |
|-----------------------------------------------------------------|-------------------------------|------|--------|------------|-------------------|
| <b>DAC Digital Filter (LPF):</b>                                |                               |      |        |            |                   |
| Passband<br>(Note 38)                                           | -0.07 to +0.006 dB<br>-3.0 dB | PB   | 0<br>- | -<br>80.65 | 34.17<br>-<br>kHz |
| Stopband (Note 38)                                              |                               | SB   | 170.3  | -          | -<br>kHz          |
| Passband Ripple                                                 |                               | PR   | -0.07  | -          | +0.006<br>dB      |
| Stopband Attenuation (Note 39)                                  |                               | SA   | 72.8   | -          | -<br>dB           |
| Group Delay (Note 40)                                           |                               | GD   | -      | 25.8       | -<br>1/ $f_s$     |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                               |      |        |            |                   |
| Frequency Response: 0 to 80.0 kHz                               |                               | FR   | -11.38 | -          | +0.35<br>dB       |

Note 38. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.178 \times f_s$  (@-0.07/+0.006 dB), SB =  $0.887 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 39. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 40. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/ $f_s$ ].

## 8-9. DAC Short Delay Sharp Roll-Off Filter Characteristics (SRC Bypass Mode)

### 8-9-1. Short Delay Sharp Roll-Off Filter (SRC Bypass Mode, $f_s = 48$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 48$  kHz; DASD bit = "1", DASL bit = "0", SELDAIN bit = "0", DADFSEL bit = "0")

| Parameter                                                       | Symbol                         | Min. | Typ.   | Max.       | Unit       |
|-----------------------------------------------------------------|--------------------------------|------|--------|------------|------------|
| <b>DAC Digital Filter (LPF):</b>                                |                                |      |        |            |            |
| Passband<br>(Note 41)                                           | –0.009 to +0.232 dB<br>–6.0 dB | PB   | 0<br>– | –<br>24.15 | kHz<br>kHz |
| Stopband (Note 41)                                              |                                | SB   | 26.23  | –          | kHz        |
| Passband Ripple                                                 |                                | PR   | –0.009 | –          | dB         |
| Stopband Attenuation (Note 42)                                  |                                | SA   | 69.8   | –          | dB         |
| Group Delay (Note 43)                                           |                                | GD   | –      | 5.5        | 1/fs       |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                                |      |        |            |            |
| Frequency Response: 0 to 20.0 kHz                               |                                | FR   | –0.12  | –          | dB         |

Note 41. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.4669 \times f_s$  (@–0.009/+0.232 dB), SB =  $0.5465 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 42. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 43. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

### 8-9-2. Short Delay Sharp Roll-Off Filter (SRC Bypass Mode, $f_s = 96$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 96$  kHz; DASD bit = "1", DASL bit = "0", SELDAIN bit = "0", DADFSEL bit = "0")

| Parameter                                                       | Symbol                         | Min. | Typ.   | Max.       | Unit       |
|-----------------------------------------------------------------|--------------------------------|------|--------|------------|------------|
| <b>DAC Digital Filter (LPF):</b>                                |                                |      |        |            |            |
| Passband<br>(Note 44)                                           | –0.004 to +0.238 dB<br>–6.0 dB | PB   | 0<br>– | –<br>48.32 | kHz<br>kHz |
| Stopband (Note 44)                                              |                                | SB   | 52.5   | –          | kHz        |
| Passband Ripple                                                 |                                | PR   | –0.004 | –          | dB         |
| Stopband Attenuation (Note 45)                                  |                                | SA   | 69.8   | –          | dB         |
| Group Delay (Note 46)                                           |                                | GD   | –      | 5.5        | 1/fs       |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                                |      |        |            |            |
| Frequency Response: 0 to 40.0 kHz                               |                                | FR   | –1.69  | –          | dB         |

Note 44. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.4669 \times f_s$  (@–0.004/+0.238 dB), SB =  $0.5465 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 45. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 46. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

**8-9-3. Short Delay Sharp Roll-Off Filter (SRC Bypass Mode, fs = 192 kHz)**

(Ta = -40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 192 kHz; DASD bit = "1", DASL bit = "0", SELDAIN bit = "0", DADFSEL bit = "0")

| Parameter                                                |                     | Symbol | Min.   | Typ.  | Max.   | Unit |
|----------------------------------------------------------|---------------------|--------|--------|-------|--------|------|
| DAC Digital Filter (LPF):                                |                     |        |        |       |        |      |
| Passband<br>(Note 47)                                    | −0.002 to +0.247 dB | PB     | 0      | -     | 89.68  | kHz  |
|                                                          | −6.0 dB             |        | -      | 96.64 | -      | kHz  |
| Stopband (Note 47)                                       |                     | SB     | 104.9  | -     | -      | kHz  |
| Passband Ripple                                          |                     | PR     | −0.002 | -     | +0.247 | dB   |
| Stopband Attenuation (Note 48)                           |                     | SA     | 69.8   | -     | -      | dB   |
| Group Delay (Note 49)                                    |                     | GD     | -      | 5.5   | -      | 1/fs |
| DAC Digital Filter (LPF) + DACANA (Headphone Amplifier): |                     |        |        |       |        |      |
| Frequency Response: 0 to 80.0 kHz                        |                     | FR     | −8.23  | -     | +0.36  | dB   |

Note 47. The passband and stopband frequencies scale with fs (system sampling rate).

PB =  $0.4671 \times fs$  (@ -0.002/+0.247 dB), SB =  $0.5465 \times fs$ . Each frequency response refers to that of 1 kHz.

Note 48. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 49. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

## 8-10. DAC Short Delay Slow Roll-Off Filter Characteristics (SRC Bypass Mode)

### 8-10-1. Short Delay Slow Roll-Off Filter (SRC Bypass Mode, $f_s = 48$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 48$  kHz; DASD bit = "1", DASL bit = "1", SELDAIN bit = "0", DADFSEL bit = "0")

| Parameter                                                       | Symbol                        | Min. | Typ.   | Max.       | Unit       |
|-----------------------------------------------------------------|-------------------------------|------|--------|------------|------------|
| <b>DAC Digital Filter (LPF):</b>                                |                               |      |        |            |            |
| Passband<br>(Note 50)                                           | –0.07 to +0.025 dB<br>–3.0 dB | PB   | 0<br>– | –<br>20.57 | kHz<br>kHz |
| Stopband (Note 50)                                              |                               | SB   | 42.98  | –          | kHz        |
| Passband Ripple                                                 |                               | PR   | –0.07  | –          | dB         |
| Stopband Attenuation (Note 51)                                  |                               | SA   | 75.1   | –          | dB         |
| Group Delay (Note 52)                                           |                               | GD   | –      | 4.5        | 1/fs       |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                               |      |        |            |            |
| Frequency Response: 0 to 20.0 kHz                               |                               | FR   | –2.96  | –          | dB         |

Note 50. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.2045 \times f_s$  (@–0.07/+0.025 dB), SB =  $0.8955 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 51. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 52. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/ $f_s$ ].

### 8-10-2. Short Delay Slow Roll-Off Filter (SRC Bypass Mode, $f_s = 96$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 96$  kHz; DASD bit = "1", DASL bit = "1", SELDAIN bit = "0", DADFSEL bit = "0")

| Parameter                                                       | Symbol                        | Min. | Typ.   | Max.       | Unit       |
|-----------------------------------------------------------------|-------------------------------|------|--------|------------|------------|
| <b>DAC Digital Filter (LPF):</b>                                |                               |      |        |            |            |
| Passband<br>(Note 53)                                           | –0.07 to +0.027 dB<br>–3.0 dB | PB   | 0<br>– | –<br>41.16 | kHz<br>kHz |
| Stopband (Note 53)                                              |                               | SB   | 85.97  | –          | kHz        |
| Passband Ripple                                                 |                               | PR   | –0.07  | –          | dB         |
| Stopband Attenuation (Note 54)                                  |                               | SA   | 75.1   | –          | dB         |
| Group Delay (Note 55)                                           |                               | GD   | –      | 4.5        | 1/fs       |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                               |      |        |            |            |
| Frequency Response: 0 to 40.0 kHz                               |                               | FR   | –4.59  | –          | dB         |

Note 53. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.2052 \times f_s$  (@–0.07/+0.027 dB), SB =  $0.8955 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 54. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 55. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/ $f_s$ ].

**8-10-3. Short Delay Slow Roll-Off Filter (SRC Bypass Mode,  $f_s = 192$  kHz)**

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 192$  kHz; DASD bit = "1", DASL bit = "1", SELDAIN bit = "0", DADFSEL bit = "0")

| Parameter                                                |                               | Symbol | Min.   | Typ.       | Max.       | Unit       |
|----------------------------------------------------------|-------------------------------|--------|--------|------------|------------|------------|
| DAC Digital Filter (LPF):                                |                               |        |        |            |            |            |
| Passband<br>(Note 56)                                    | −0.07 to +0.028 dB<br>−3.0 dB | PB     | 0<br>- | -<br>82.37 | 39.54<br>- | kHz<br>kHz |
| Stopband (Note 56)                                       |                               | SB     | 172    | -          | -          | kHz        |
| Passband Ripple                                          |                               | PR     | −0.07  | -          | +0.028     | dB         |
| Stopband Attenuation (Note 57)                           |                               | SA     | 75.1   | -          | -          | dB         |
| Group Delay (Note 58)                                    |                               | GD     | -      | 4.5        | -          | 1/fs       |
| DAC Digital Filter (LPF) + DACANA (Headphone Amplifier): |                               |        |        |            |            |            |
| Frequency Response: 0 to 80.0 kHz                        |                               | FR     | −11.13 | -          | +0.35      | dB         |

Note 56. The passband and stopband frequencies scale with  $f_s$  (system sampling rate)

PB =  $0.2059 \times f_s$  (@-0.07/+0.028 dB), SB =  $0.8958 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 57. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 58. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/ $f_s$ ].

## 8-11. DAC Sharp Roll-Off Filter Characteristics (SRC Mode)

### 8-11-1. Sharp Roll-Off Filter (SRC Mode, $f_s = 48$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 48$  kHz; DASD bit = "0", DASL bit = "0", SELDAIN bit = "1", DADFSEL bit = "1")

| Parameter                                                       | Symbol                               | Min. | Typ.     | Max.       | Unit       |
|-----------------------------------------------------------------|--------------------------------------|------|----------|------------|------------|
| <b>DAC Digital Filter (LPF):</b>                                |                                      |      |          |            |            |
| Passband<br>(Note 59)                                           | $-0.004$ to $+0.199$ dB<br>$-6.0$ dB | PB   | 0<br>-   | -<br>24.00 | kHz<br>kHz |
| Stopband (Note 59)                                              |                                      | SB   | 26.21    | -          | kHz        |
| Passband Ripple                                                 |                                      | PR   | $-0.004$ | -          | dB         |
| Stopband Attenuation (Note 60)                                  |                                      | SA   | 70.4     | -          | dB         |
| Group Delay (Note 61)                                           |                                      | GD   | -        | 27.6       | 1/fs       |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                                      |      |          |            |            |
| Frequency Response: 0 to 20.0 kHz                               |                                      | FR   | $-0.12$  | -          | dB         |

Note 59. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.4642 \times f_s$  (@ $-0.004/+0.199$  dB), SB =  $0.546 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 60. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 61. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within  $\pm 1$  [1/fs].

### 8-11-2. Sharp Roll-Off Filter (SRC Mode, $f_s = 96$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 96$  kHz; DASD bit = "0", DASL bit = "0", SELDAIN bit = "1", DADFSEL bit = "1")

| Parameter                                                       | Symbol                               | Min. | Typ.     | Max.       | Unit       |
|-----------------------------------------------------------------|--------------------------------------|------|----------|------------|------------|
| <b>DAC Digital Filter (LPF):</b>                                |                                      |      |          |            |            |
| Passband<br>(Note 62)                                           | $-0.001$ to $+0.202$ dB<br>$-6.0$ dB | PB   | 0<br>-   | -<br>48.01 | kHz<br>kHz |
| Stopband (Note 62)                                              |                                      | SB   | 52.45    | -          | kHz        |
| Passband Ripple                                                 |                                      | PR   | $-0.001$ | -          | dB         |
| Stopband Attenuation (Note 63)                                  |                                      | SA   | 70.2     | -          | dB         |
| Group Delay (Note 64)                                           |                                      | GD   | -        | 27.6       | 1/fs       |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                                      |      |          |            |            |
| Frequency Response: 0 to 40.0 kHz                               |                                      | FR   | $-1.72$  | -          | dB         |

Note 62. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.4644 \times f_s$  (@ $-0.001/+0.202$  dB), SB =  $0.5464 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 63. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 64. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within  $\pm 1$  [1/fs].

**8-11-3. Sharp Roll-Off Filter (SRC Mode, fs = 192 kHz)**

(Ta = -40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 192 kHz; DASD bit = "0", DASL bit = "0", SELDAIN bit = "1", DADFSEL bit = "1")

| Parameter                                                       | Symbol                        | Min. | Typ.   | Max.       | Unit                     |
|-----------------------------------------------------------------|-------------------------------|------|--------|------------|--------------------------|
| <b>DAC Digital Filter (LPF):</b>                                |                               |      |        |            |                          |
| Passband<br>(Note 65)                                           | 0.000 to +0.210 dB<br>-6.0 dB | PB   | 0<br>- | -<br>96.02 | 89.22<br>-<br>kHz<br>kHz |
| Stopband (Note 65)                                              |                               | SB   | 104.92 | -          | -<br>kHz                 |
| Passband Ripple                                                 |                               | PR   | 0.000  | -          | +0.210<br>dB             |
| Stopband Attenuation (Note 66)                                  |                               | SA   | 70.1   | -          | -<br>dB                  |
| Group Delay (Note 67)                                           |                               | GD   | -      | 27.6       | -<br>1/fs                |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                               |      |        |            |                          |
| Frequency Response: 0 to 80.0 kHz                               |                               | FR   | -8.27  | -          | +0.35<br>dB              |

Note 65. The passband and stopband frequencies scale with fs (system sampling rate).

PB =  $0.4647 \times fs$  (@0.000/+0.210 dB), SB =  $0.5465 \times fs$ . Each frequency response refers to that of 1 kHz.

Note 66. The bandwidth of the stopband attenuation value is from stopband to fs (system sampling rate).

Note 67. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/fs].

## 8-12. DAC Slow Roll-Off Filter Characteristics (SRC Mode)

### 8-12-1. Slow Roll-Off Filter (SRC Mode, $f_s = 48$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 48$  kHz; DASD bit = "0", DASL bit = "1", SELDAIN bit = "1", DADFSEL bit = "1")

| Parameter                                                       | Symbol                        | Min. | Typ.   | Max.       | Unit        |
|-----------------------------------------------------------------|-------------------------------|------|--------|------------|-------------|
| <b>DAC Digital Filter (LPF):</b>                                |                               |      |        |            |             |
| Passband<br>(Note 68)                                           | –0.07 to +0.011 dB<br>–3.0 dB | PB   | 0<br>– | –<br>20.06 | 8.91<br>kHz |
| Stopband (Note 68)                                              |                               | SB   | 42.57  | –          | –           |
| Passband Ripple                                                 |                               | PR   | –0.07  | –          | +0.011      |
| Stopband Attenuation (Note 69)                                  |                               | SA   | 73.9   | –          | –           |
| Group Delay (Note 70)                                           |                               | GD   | –      | 27.6       | –           |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                               |      |        |            |             |
| Frequency Response: 0 to 20.0 kHz                               |                               | FR   | –3.21  | –          | +0.03       |

Note 68. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.1856 \times f_s$  (@–0.07/+0.011 dB), SB =  $0.887 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 69. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 70. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/ $f_s$ ].

### 8-12-2. Slow Roll-Off Filter (SRC Mode, $f_s = 96$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 96$  kHz; DASD bit = "0", DASL bit = "1", SELDAIN bit = "1", DADFSEL bit = "1")

| Parameter                                                       | Symbol                        | Min. | Typ.   | Max.       | Unit         |
|-----------------------------------------------------------------|-------------------------------|------|--------|------------|--------------|
| <b>DAC Digital Filter (LPF):</b>                                |                               |      |        |            |              |
| Passband<br>(Note 71)                                           | –0.07 to +0.012 dB<br>–3.0 dB | PB   | 0<br>– | –<br>40.15 | 17.88<br>kHz |
| Stopband (Note 71)                                              |                               | SB   | 85.15  | –          | –            |
| Passband Ripple                                                 |                               | PR   | –0.07  | –          | +0.012       |
| Stopband Attenuation (Note 72)                                  |                               | SA   | 73.9   | –          | –            |
| Group Delay (Note 73)                                           |                               | GD   | –      | 27.6       | –            |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                               |      |        |            |              |
| Frequency Response: 0 to 40.0 kHz                               |                               | FR   | –4.87  | –          | +0.10        |

Note 71. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.1863 \times f_s$  (@–0.07/+0.012 dB), SB =  $0.887 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 72. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 73. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/ $f_s$ ].

**8-12-3. Slow Roll-Off Filter (SRC Mode,  $f_s = 192$  kHz)**

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 192$  kHz; DASD bit = "0", DASL bit = "1", SELDAIN bit = "1", DADFSEL bit = "1")

| Parameter                                                       | Symbol                        | Min. | Typ.   | Max.       | Unit              |
|-----------------------------------------------------------------|-------------------------------|------|--------|------------|-------------------|
| <b>DAC Digital Filter (LPF):</b>                                |                               |      |        |            |                   |
| Passband<br>(Note 74)                                           | -0.07 to +0.013 dB<br>-3.0 dB | PB   | 0<br>- | -<br>80.34 | 35.89<br>-<br>kHz |
| Stopband (Note 74)                                              |                               | SB   | 170.30 | -          | -<br>kHz          |
| Passband Ripple                                                 |                               | PR   | -0.07  | -          | +0.013<br>dB      |
| Stopband Attenuation (Note 75)                                  |                               | SA   | 73.9   | -          | -<br>dB           |
| Group Delay (Note 76)                                           |                               | GD   | -      | 27.6       | -<br>1/ $f_s$     |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                               |      |        |            |                   |
| Frequency Response: 0 to 80.0 kHz                               |                               | FR   | -11.42 | -          | +0.35<br>dB       |

Note 74. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.1869 \times f_s$  (@-0.07/+0.013 dB), SB =  $0.887 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 75. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 76. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/ $f_s$ ].

### 8-13. DAC Short Delay Sharp Roll-Off Filter Characteristics (SRC Mode)

#### 8-13-1. Short Delay Sharp Roll-Off Filter (SRC Mode, $f_s = 48$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 48$  kHz; DASD bit = "1", DASL bit = "0", SELDAIN bit = "1", DADFSEL bit = "1")

| Parameter                                                       | Symbol                               | Min. | Typ.     | Max.       | Unit       |
|-----------------------------------------------------------------|--------------------------------------|------|----------|------------|------------|
| <b>DAC Digital Filter (LPF):</b>                                |                                      |      |          |            |            |
| Passband<br>(Note 77)                                           | $-0.004$ to $+0.198$ dB<br>$-6.0$ dB | PB   | 0<br>-   | -<br>24.00 | kHz<br>kHz |
| Stopband (Note 77)                                              |                                      | SB   | 26.21    | -          | kHz        |
| Passband Ripple                                                 |                                      | PR   | $-0.004$ | -          | dB         |
| Stopband Attenuation (Note 78)                                  |                                      | SA   | 70.4     | -          | dB         |
| Group Delay (Note 79)                                           |                                      | GD   | -        | 7.3        | 1/ $f_s$   |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                                      |      |          |            |            |
| Frequency Response: 0 to 20.0 kHz                               |                                      | FR   | $-0.12$  | -          | dB         |

Note 77. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.4642 \times f_s$  (@ $-0.004/+0.198$  dB), SB =  $0.546 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 78. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 79. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within  $\pm 1$  [1/ $f_s$ ].

#### 8-13-2. Short Delay Sharp Roll-Off Filter (SRC Mode, $f_s = 96$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 96$  kHz; DASD bit = "1", DASL bit = "0", SELDAIN bit = "1", DADFSEL bit = "1")

| Parameter                                                       | Symbol                               | Min. | Typ.     | Max.       | Unit       |
|-----------------------------------------------------------------|--------------------------------------|------|----------|------------|------------|
| <b>DAC Digital Filter (LPF):</b>                                |                                      |      |          |            |            |
| Passband<br>(Note 80)                                           | $-0.001$ to $+0.202$ dB<br>$-6.0$ dB | PB   | 0<br>-   | -<br>48.01 | kHz<br>kHz |
| Stopband (Note 80)                                              |                                      | SB   | 52.44    | -          | kHz        |
| Passband Ripple                                                 |                                      | PR   | $-0.001$ | -          | dB         |
| Stopband Attenuation (Note 81)                                  |                                      | SA   | 70.4     | -          | dB         |
| Group Delay (Note 81)                                           |                                      | GD   | -        | 7.3        | 1/ $f_s$   |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                                      |      |          |            |            |
| Frequency Response: 0 to 40.0 kHz                               |                                      | FR   | $-1.72$  | -          | dB         |

Note 80. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.4644 \times f_s$  (@ $-0.001/+0.202$  dB), SB =  $0.5463 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 81. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 82. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within  $\pm 1$  [1/ $f_s$ ].

**8-13-3. Short Delay Sharp Roll-Off Filter (SRC Mode,  $f_s = 192$  kHz)**

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 192$  kHz; DASD bit = "1", DASL bit = "0", SELDAIN bit = "1", DADFSEL bit = "1")

| Parameter                                                       | Symbol                        | Min. | Typ.   | Max.       | Unit                     |
|-----------------------------------------------------------------|-------------------------------|------|--------|------------|--------------------------|
| <b>DAC Digital Filter (LPF):</b>                                |                               |      |        |            |                          |
| Passband<br>(Note 83)                                           | 0.000 to +0.210 dB<br>-6.0 dB | PB   | 0<br>- | -<br>96.02 | 89.22<br>-<br>kHz<br>kHz |
| Stopband (Note 83)                                              |                               | SB   | 104.90 | -          | -<br>kHz                 |
| Passband Ripple                                                 |                               | PR   | 0.000  | -          | +0.210<br>dB             |
| Stopband Attenuation (Note 84)                                  |                               | SA   | 70.4   | -          | -<br>dB                  |
| Group Delay (Note 85)                                           |                               | GD   | -      | 7.3        | -<br>1/ $f_s$            |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                               |      |        |            |                          |
| Frequency Response: 0 to 80.0 kHz                               |                               | FR   | -8.27  | -          | +0.36<br>dB              |

Note 83. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.4647 \times f_s$  (@0.000/+0.210 dB), SB =  $0.5464 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 84. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 85. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within  $\pm 1$  [1/ $f_s$ ].

## 8-14. DAC Short Delay Slow Roll-Off Filter Characteristics (SRC Mode)

### 8-14-1. Short Delay Slow Roll-Off Filter (SRC Mode, $f_s = 48$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 48$  kHz; DASD bit = "1", DASL bit = "1", SELDAIN bit = "1", DADFSEL bit = "1")

| Parameter                                                       | Symbol                        | Min. | Typ.   | Max.       | Unit         |
|-----------------------------------------------------------------|-------------------------------|------|--------|------------|--------------|
| <b>DAC Digital Filter (LPF):</b>                                |                               |      |        |            |              |
| Passband<br>(Note 86)                                           | –0.07 to +0.036 dB<br>–3.0 dB | PB   | 0<br>– | –<br>20.48 | 10.19<br>kHz |
| Stopband (Note 86)                                              |                               | SB   | 42.98  | –          | –            |
| Passband Ripple                                                 |                               | PR   | –0.07  | –          | +0.036       |
| Stopband Attenuation (Note 87)                                  |                               | SA   | 76.3   | –          | –            |
| Group Delay (Note 88)                                           |                               | GD   | –      | 6.3        | –            |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                               |      |        |            |              |
| Frequency Response: 0 to 20.0 kHz                               |                               | FR   | –2.97  | –          | +0.04        |

Note 86. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.2123 \times f_s$  (@–0.07/+0.036 dB), SB =  $0.8954 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 87. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 88. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/ $f_s$ ].

### 8-14-2. Short Delay Slow Roll-Off Filter (SRC Mode, $f_s = 96$ kHz)

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 96$  kHz; DASD bit = "1", DASL bit = "1", SELDAIN bit = "1", DADFSEL bit = "1")

| Parameter                                                       | Symbol                        | Min. | Typ.   | Max.       | Unit         |
|-----------------------------------------------------------------|-------------------------------|------|--------|------------|--------------|
| <b>DAC Digital Filter (LPF):</b>                                |                               |      |        |            |              |
| Passband<br>(Note 89)                                           | –0.07 to +0.038 dB<br>–3.0 dB | PB   | 0<br>– | –<br>40.98 | 20.45<br>kHz |
| Stopband (Note 89)                                              |                               | SB   | 85.80  | –          | –            |
| Passband Ripple                                                 |                               | PR   | –0.07  | –          | +0.038       |
| Stopband Attenuation (Note 90)                                  |                               | SA   | 73.9   | –          | –            |
| Group Delay (Note 91)                                           |                               | GD   | –      | 6.3        | –            |
| <b>DAC Digital Filter (LPF) + DACANA (Headphone Amplifier):</b> |                               |      |        |            |              |
| Frequency Response: 0 to 40.0 kHz                               |                               | FR   | –4.63  | –          | +0.10        |

Note 89. The passband and stopband frequencies scale with  $f_s$  (system sampling rate).

PB =  $0.2130 \times f_s$  (@–0.07/+0.038 dB), SB =  $0.8938 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 90. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 91. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/ $f_s$ ].

**8-14-3. Short Delay Slow Roll-Off Filter (SRC Mode,  $f_s = 192$  kHz)**

( $T_a = -40$  to  $85^\circ\text{C}$ ;  $AVDD = CVDD = LVDD = 1.7$  to  $1.9$  V;  $TVDD = 1.65$  to  $3.6$  V;  $VSS1 = VSS2 = VSS3 = HPGND = 0$  V;  $f_s = 192$  kHz;  $DASD$  bit = "1",  $DASL$  bit = "1",  $SELD$ AIN bit = "1",  $DADFSEL$  bit = "1")

| Parameter                                                |                    | Symbol | Min.   | Typ.  | Max.   | Unit |
|----------------------------------------------------------|--------------------|--------|--------|-------|--------|------|
| DAC Digital Filter (LPF):                                |                    |        |        |       |        |      |
| Passband<br>(Note 92)                                    | −0.07 to +0.039 dB | PB     | 0      | -     | 41.05  | kHz  |
|                                                          | −3.0 dB            |        | -      | 82.02 | -      | kHz  |
| Stopband (Note 92)                                       |                    | SB     | 171.96 | -     | -      | kHz  |
| Passband Ripple                                          |                    | PR     | −0.07  | -     | +0.039 | dB   |
| Stopband Attenuation (Note 93)                           |                    | SA     | 76.2   | -     | -      | dB   |
| Group Delay (Note 94)                                    |                    | GD     | -      | 6.3   | -      | 1/fs |
| DAC Digital Filter (LPF) + DACANA (Headphone Amplifier): |                    |        |        |       |        |      |
| Frequency Response: 0 to 80.0 kHz                        |                    | FR     | −11.17 | -     | +0.35  | dB   |

Note 92. The passband and stopband frequencies scale with  $f_s$  (system sampling rate)

PB =  $0.2138 \times f_s$  (@-0.07/+0.039 dB), SB =  $0.8956 \times f_s$ . Each frequency response refers to that of 1 kHz.

Note 93. The bandwidth of the stopband attenuation value is from stopband to  $f_s$  (system sampling rate).

Note 94. The calculated delay time is resulting from digital filtering. This is the time from the input of MSB for L channel of SDTI to the output of an analog signal. The error of the delay at audio interface is within +1 [1/ $f_s$ ].

**8-15. Digital Microphone Filter Characteristics**

(Ta = -40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V; TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; fs = 48 kHz)

| Parameter                                     |                   | Symbol      | Min.  | Typ. | Max. | Unit      |
|-----------------------------------------------|-------------------|-------------|-------|------|------|-----------|
| Passband<br>(Note 95)                         | +0.18 to -0.09 dB | PB          | 0     | -    | 20.7 | kHz       |
|                                               | -0.87 dB          |             | -     | 21.6 | -    | kHz       |
|                                               | -3.0 dB           |             | -     | 22.8 | -    | kHz       |
| Stopband (Note 95)                            |                   | SB          | 28.4  | -    | -    | kHz       |
| Passband Ripple                               |                   | PR          | -0.09 | -    | 0.18 | dB        |
| Stopband Attenuation                          |                   | SA          | 65    | -    | -    | dB        |
| Group Delay Distortion                        |                   | $\Delta$ GD | -     | 0    | -    | $\mu$ sec |
| Group Delay (Ts = 1/fs) (Note 96)             |                   | GD          | -     | 12.5 | -    | 1/fs      |
| <b>Digital MIC HPF: HPFC[1:0] bits = "00"</b> |                   |             |       |      |      |           |
| Frequency Response<br>(Note 95)               | -3.0 dB           | FR          | -     | 29.8 | -    | Hz        |

Note 95. The passband and stopband frequencies scale with "fs" (system sampling rate). Each frequency response refers to that of 1 kHz.

Note 96. The calculated delay time is resulting from digital filtering. This is the time from the 16/24/32-bit data is set to input register to the output of SDTO digital data.

**8-16. DC Characteristics**

(Ta = -40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V, TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V, PMOSC bit = "0")

| Parameter                                                                    | Symbol | Min.       | Typ. | Max.    | Unit |
|------------------------------------------------------------------------------|--------|------------|------|---------|------|
| <b>I/O Pins (Note 97)</b>                                                    |        |            |      |         |      |
| High-Level Input Voltage<br>Except for DMDAT pin                             | VIH1   | 70%TVDD    | -    | -       | V    |
| DMDAT pin                                                                    | VIH2   | 65%AVDD    | -    | -       | V    |
| Low-Level Input Voltage<br>Except for DMDAT pin                              | VIL1   | -          | -    | 30%TVDD | V    |
| DMDAT pin                                                                    | VIL2   | -          | -    | 35%AVDD | V    |
| High-Level Output Voltage<br>Except for DMCLK pin (Iout = -200 µA)           | VOH1   | TVDD - 0.2 | -    | -       | V    |
| DMCLK pin (Iout = -80 µA)                                                    | VOH2   | AVDD - 0.4 | -    | -       | V    |
| Low-Level Output Voltage<br>Except for SDA pin, DMCLK pin<br>(Iout = 200 µA) | VOL1   | -          | -    | 0.2     | V    |
| DMCLK pin (Iout = 80 µA)                                                     | VOL2   | -          | -    | 0.4     | V    |
| SDA pin<br>2 V < TVDD ≤ 3.6 V (Iout = 3 mA)                                  | VOL3   | -          | -    | 0.4     | V    |
| 1.65 V ≤ TVDD ≤ 2 V (Iout = 2 mA)                                            | VOL3   | -          | -    | 20%TVDD | V    |
| Input Leakage Current (Note 98)                                              | Iin    | -5         | -    | +5      | µA   |

Note 97. MCKI/XTI, BCLK, LRCK, SDTI, SDTO, SCL, SDA, PDN, TEST1, TEST2, DMCLK, DMDAT pins.

Note 98. Except for MCKI/XTI pin.

### 8-17. Switching Characteristics

(Ta = -40 to 85°C; AVDD = CVDD = LVDD = 1.7 to 1.9 V, TVDD = 1.65 to 3.6 V; VSS1 = VSS2 = VSS3 = HPGND = 0 V; CL = 80 pF; unless otherwise specified)

| Parameter                                          | Symbol  | Min.       | Typ.     | Max.               | Unit |
|----------------------------------------------------|---------|------------|----------|--------------------|------|
| <b>MCKI</b>                                        |         |            |          |                    |      |
| Input Frequency                                    | fMCK    | 0.256      | -        | 24.576             | MHz  |
| Pulse Width Low                                    | tMCKL   | 0.4 / fMCK | -        | -                  | nsec |
| Pulse Width High                                   | tMCKH   | 0.4 / fMCK | -        | -                  | nsec |
| <b>X'tal Oscillator (XTI pin)</b>                  |         |            |          |                    |      |
| Input Frequency                                    | fMCK    | 11.2896    | -        | 24.576             | MHz  |
| <b>Audio Interface Timing</b>                      |         |            |          |                    |      |
| <b>Master Mode</b>                                 |         |            |          |                    |      |
| LRCK Output Timing                                 |         |            |          |                    |      |
| Frequency (When not use Digital MIC)<br>(Note 99)  | fs      | 8          | -        | 192                | kHz  |
| Frequency (When use Digital MIC)<br>(Note 100)     | fs      | 8          | -        | 96                 | kHz  |
| Duty                                               | LRDuty  | -          | 50       | -                  | %    |
| BCLK Output Timing                                 |         |            |          |                    |      |
| Period (BCKO bit = "0")                            | tBCK    | -          | 1/(64fs) | -                  | nsec |
| (BCKO bit = "1")                                   | tBCK    | -          | 1/(32fs) | -                  | nsec |
| Duty                                               | BCKDuty | -          | 50       | -                  | %    |
| BCLK "↓" to LRCK Edge                              | tBLR    | -20        | -        | 20                 | nsec |
| SDTI Setup Time                                    | tBDS    | 10         | -        | -                  | nsec |
| SDTI Hold Time                                     | tBDH    | 10         | -        | -                  | nsec |
| Delay time from BCLK Falling to SDTO               | tBOD    | -40        | -        | 40                 | nsec |
| <b>Slave Mode</b>                                  |         |            |          |                    |      |
| LRCK Input Timing                                  |         |            |          |                    |      |
| Frequency (When not use Digital MIC)<br>(Note 99)  | fs      | 8          | -        | 192                | kHz  |
| Frequency (When use Digital MIC)<br>(Note 100)     | fs      | 8          | -        | 96                 | kHz  |
| Duty                                               | LRDuty  | 45         | 50       | 55                 | %    |
| BCLK Input Timing                                  |         |            |          |                    |      |
| Frequency (When not use Digital MIC)<br>(Note 101) | fBCK    | 0.256      | -        | 12.288<br>or 512fs | MHz  |
| Frequency (When use Digital MIC)<br>(Note 102)     | fBCK    | 0.256      | -        | 6.144<br>or 512fs  | MHz  |
| Pulse Width Low                                    | tBCKL   | 0.4 / tBCK | -        | -                  | nsec |
| Pulse Width High                                   | tBCKH   | 0.4 / tBCK | -        | -                  | nsec |
| BCLK "↑" to LRCK Edge                              | tBLR    | 20         | -        | -                  | nsec |
| LRCK Edge to BCLK "↑"                              | tLRB    | 20         | -        | -                  | nsec |
| SDTI Setup Time                                    | tBDS    | 10         | -        | -                  | nsec |
| SDTI Hold Time                                     | tBDH    | 10         | -        | -                  | nsec |
| Delay time from BCLK Falling to SDTO               | tBOD    | -          | -        | 40                 | nsec |

Note 99. Supported sampling rate are 8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 64 k, 88.2 k, 96 k, 128 k, 176.4 k and 192 kHz.

Note 100. Supported sampling rate are 8 k, 11.025 k, 12 k, 16 k, 22.05 k, 24 k, 32 k, 44.1 k, 48 k, 64 k, 88.2 k and 96 kHz.

Note 101. The maximum value is lower frequency between "12.288 MHz" and "512fs".

Note 102. The maximum value is lower frequency between "6.144 MHz" and "512fs".

| Parameter                                                             | Symbol  | Min. | Typ.     | Max. | Unit |
|-----------------------------------------------------------------------|---------|------|----------|------|------|
| <b>Digital MIC Interface Timing: C<sub>L</sub> = 100 pF</b>           |         |      |          |      |      |
| DMCLK Output Timing                                                   |         |      |          |      |      |
| Period                                                                | tSCK    | -    | 1/(64fs) | -    | nsec |
| Rising Time                                                           | tSRise  | -    | -        | 10   | nsec |
| Falling Time                                                          | tSFall  | -    | -        | 10   | nsec |
| Duty Cycle                                                            | dSCK    | 45   | 50       | 55   | %    |
| Audio Interface Timing (DMCLK, DMDAT pins)                            |         |      |          |      |      |
| DMDAT Setup Time                                                      | tDMS    | 50   | -        | -    | nsec |
| DMDAT Hold Time                                                       | tDMH    | 0    | -        | -    | nsec |
| <b>Control Interface Timing (I<sup>2</sup>C-bus mode): (Note 103)</b> |         |      |          |      |      |
| SCL Clock Frequency                                                   | fSCL    | -    | -        | 400  | kHz  |
| Bus Free Time Between Transmissions                                   | tBUF    | 1.3  | -        | -    | μsec |
| Start Condition Hold Time (prior to first clock pulse)                | tHD:STA | 0.6  | -        | -    | μsec |
| Clock Low Time                                                        | tLOW    | 1.3  | -        | -    | μsec |
| Clock High Time                                                       | tHIGH   | 0.6  | -        | -    | μsec |
| Setup Time for Repeated Start Condition                               | tSU:STA | 0.6  | -        | -    | μsec |
| SDA Hold Time from SCL Falling (Note 104)                             | tHD:DAT | 0    | -        | -    | μsec |
| SDA Setup Time from SCL Rising                                        | tSU:DAT | 0.1  | -        | -    | μsec |
| Rise Time of Both SDA and SCL Lines                                   | tR      | -    | -        | 0.3  | μsec |
| Fall Time of Both SDA and SCL Lines                                   | tF      | -    | -        | 0.3  | μsec |
| Setup Time for Stop Condition                                         | tSU:STO | 0.6  | -        | -    | μsec |
| Capacitive Load on Bus                                                | Cb      | -    | -        | 400  | pF   |
| Pulse Width of Spike Noise Suppressed by Input Filter                 | tSP     | 0    | -        | 50   | nsec |
| <b>Power-Down &amp; Reset Timing</b>                                  |         |      |          |      |      |
| PDN Accept Pulse Width (Note 105)                                     | tPDN    | 1    | -        | -    | msec |
| PDN Reject Pulse Width (Note 105)                                     | tRPD    | -    | -        | 50   | nsec |
| PMDMx bit = "1" to SDTO Valid (Note 106)                              |         |      |          |      |      |
| ADRST[1:0] bits = "00"                                                | tPDV    | -    | 1059     | -    | 1/fs |
| ADRST[1:0] bits = "01"                                                | tPDV    | -    | 267      | -    | 1/fs |
| ADRST[1:0] bits = "10"                                                | tPDV    | -    | 2115     | -    | 1/fs |
| ADRST[1:0] bits = "11"                                                | tPDV    | -    | 531      | -    | 1/fs |

Note 103. I<sup>2</sup>C-bus is a registered trademark of NXP B.V.

Note 104. Data must be held long enough to bridge the 300 nsec-transition time of SCL.

Note 105. The AK4331 will be reset by bringing the PDN pin = "L". The PDN pin must held "L" for longer period than or equal to tPDN (Min.). The AK4331 will not be reset by the "L" pulse shorter than or equal to tRPD (Max.).

Note 106. This is the time from PMDMx bit = "1" to the output of SDTO digital data.

## 8-18. Timing Diagram (System Clock)

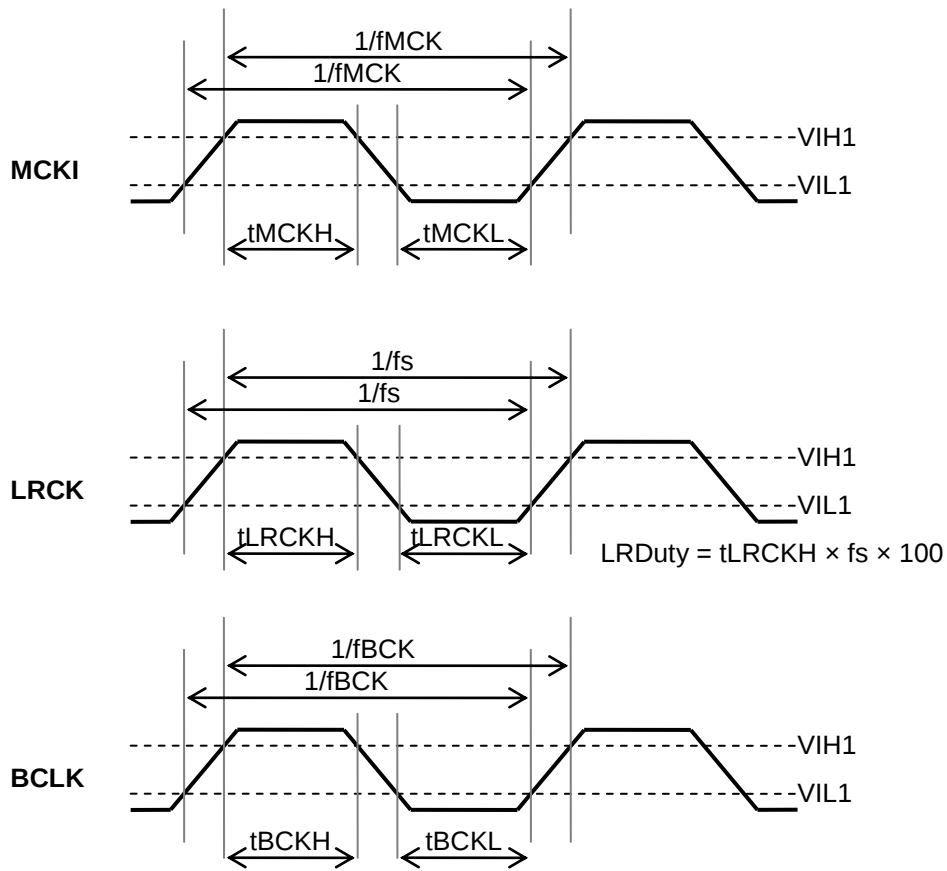


Figure 3. System Clock (Slave Mode)

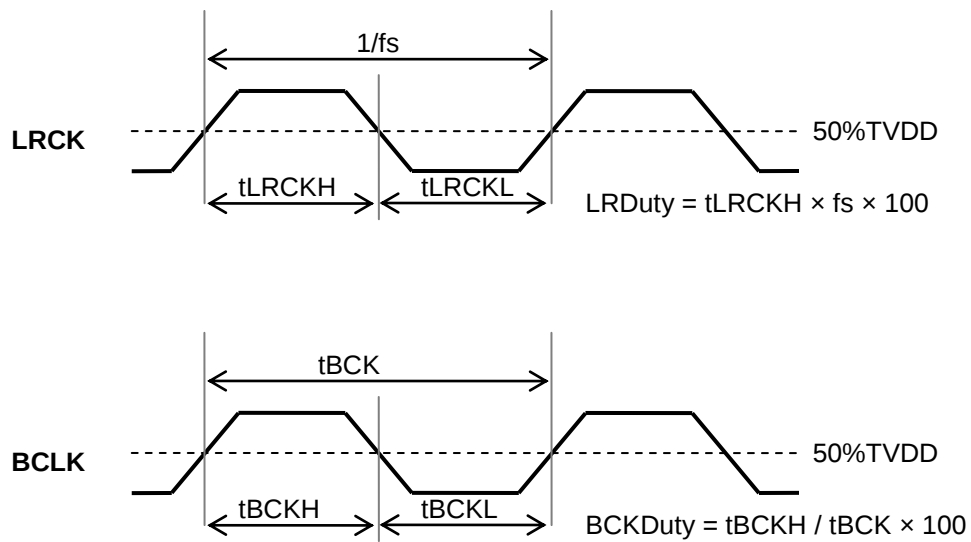


Figure 4. System Clock (Master Mode)

## 8-19. Timing Diagram (Serial Audio Interface)

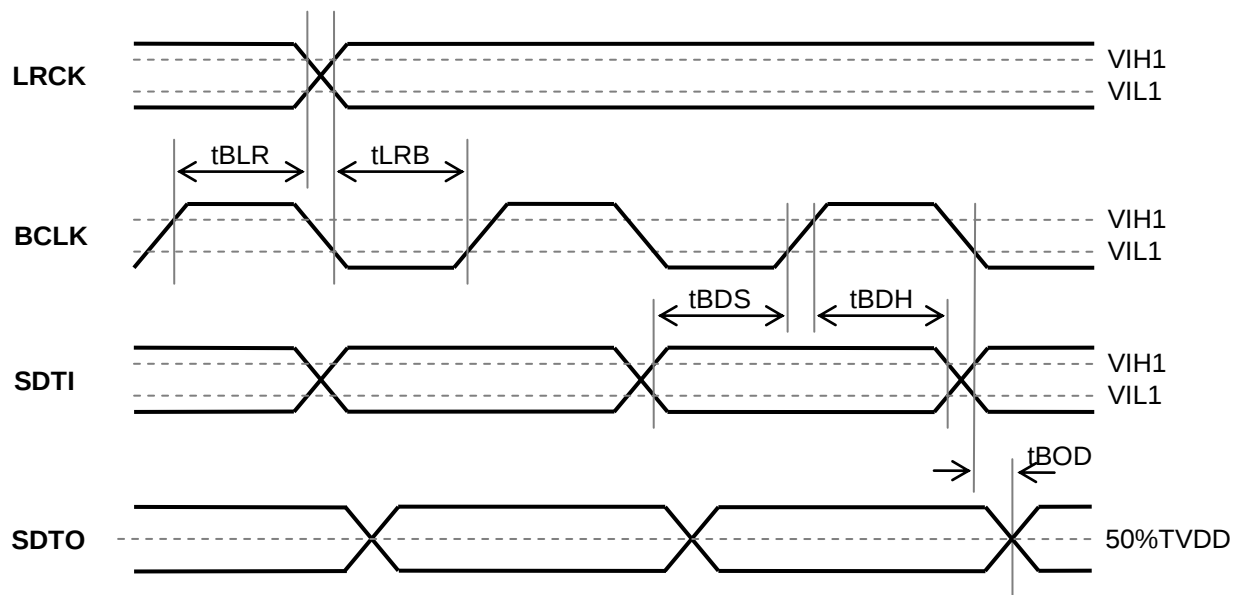


Figure 5. Serial Data Interface (Slave Mode)

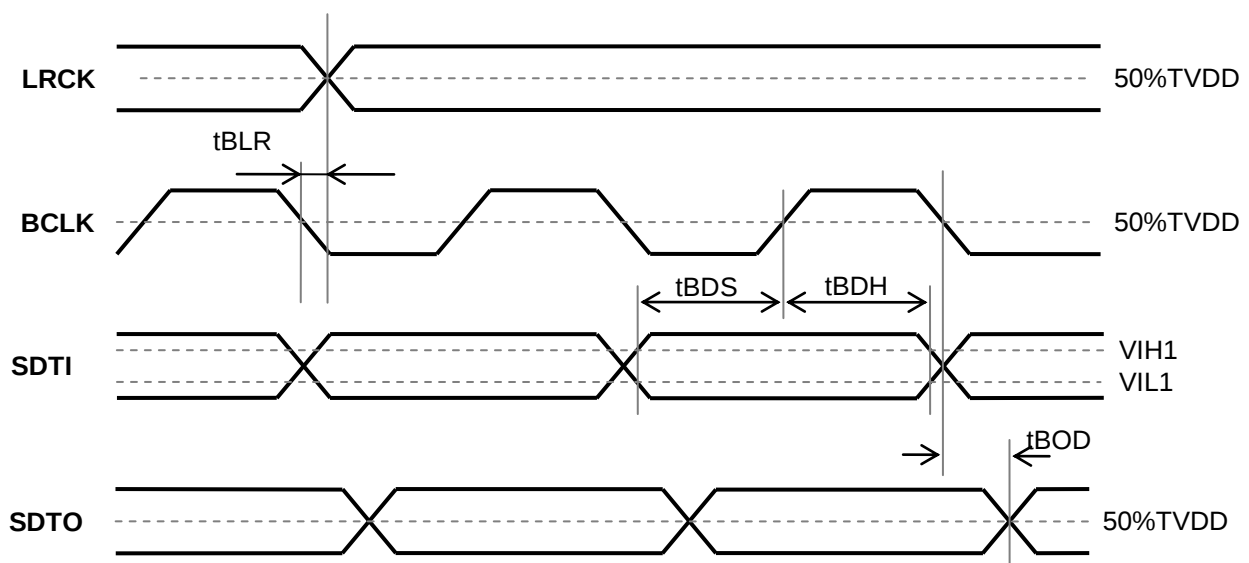


Figure 6. Serial Data Interface (Master Mode)

## 8-20. Timing Diagram (I<sup>2</sup>C-bus Interface)

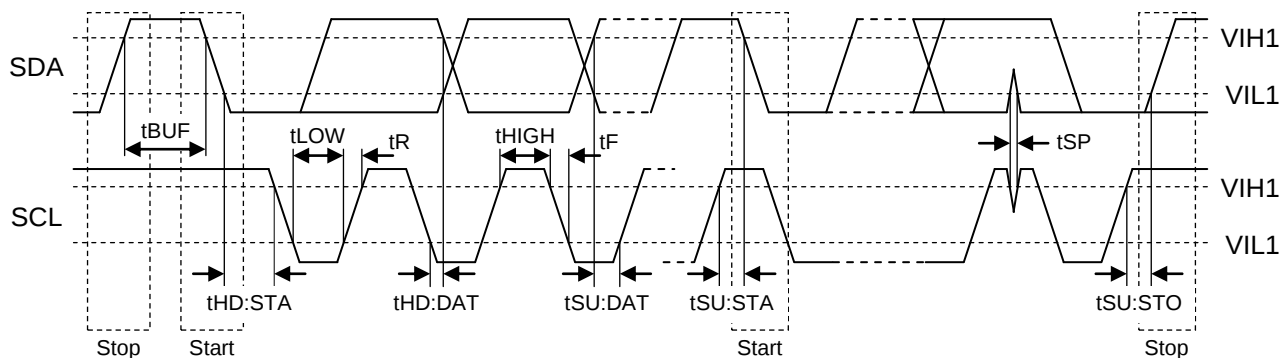


Figure 7. I<sup>2</sup>C-bus Mode Timing

## 8-21. Timing Diagram (Reset)

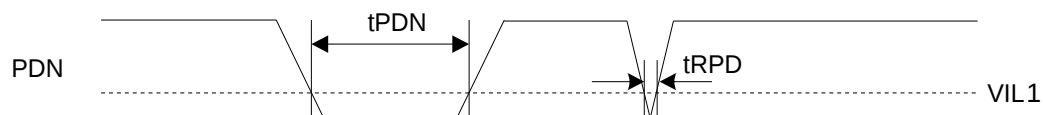


Figure 8. Power Down and Standby

## 8-22. Timing Diagram (Digital Microphone Interface)

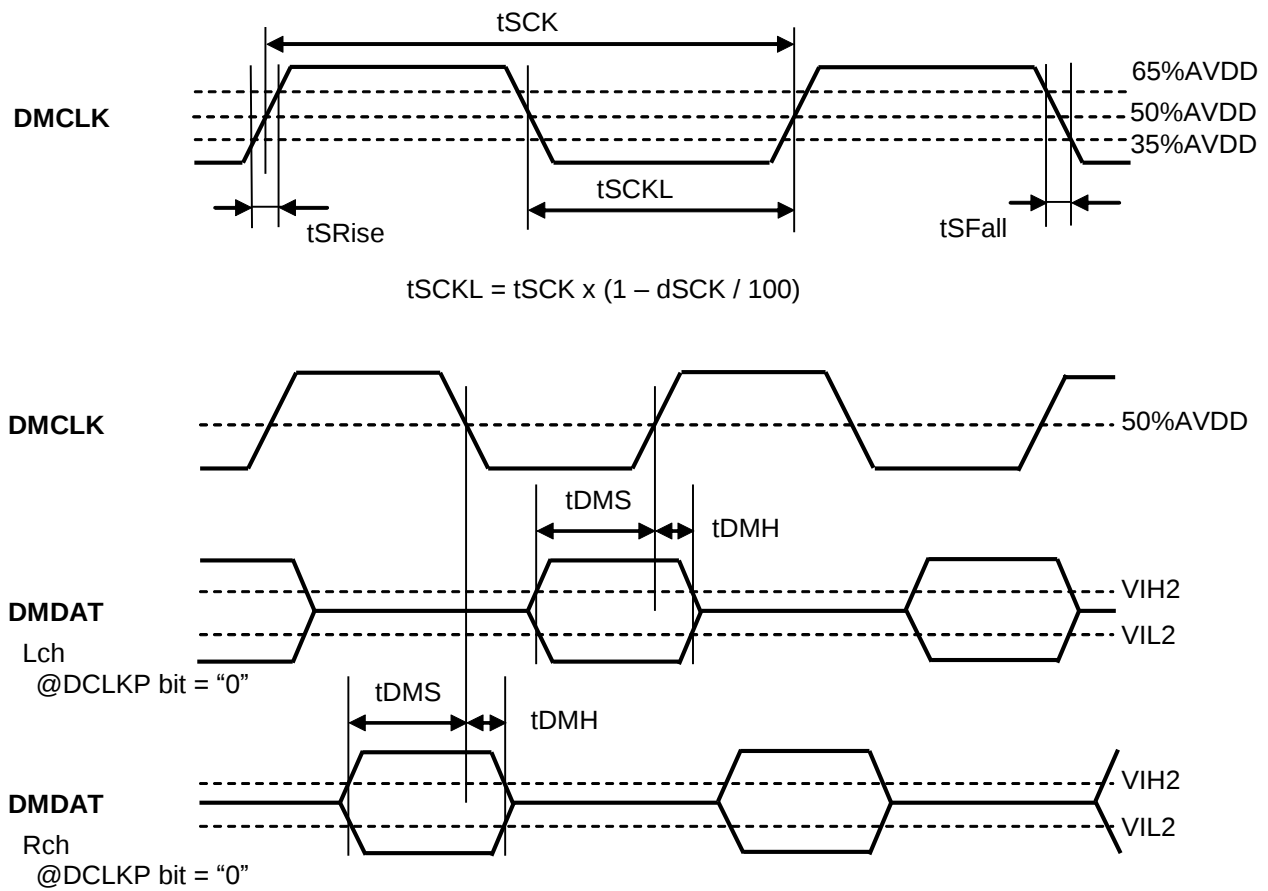


Figure 9. Digital Microphone Interface Timing

## 9. Functional Description

### 9-1. System Clock

The SRC, DAC, Headphone Amplifier and Audio Interface blocks are operated by a clock generated by PLL, an external MCKI or a clock generated by X'tal oscillator. The sampling frequency and master clock frequency are set by registers shown in [Table 2](#).

Table 2. Setting Registers for Master Clock Frequency and Sampling Frequency

| System Clock           | SRC Path Mode                                               |                                             |                                                              |
|------------------------|-------------------------------------------------------------|---------------------------------------------|--------------------------------------------------------------|
|                        | SRC Bypass Mode                                             | SRC Mode                                    |                                                              |
|                        |                                                             | FSI                                         | FSO                                                          |
| Master Clock Frequency | HPMD[1:0] bits, CM[1:0] bits<br>( <a href="#">Table 5</a> ) | CM[1:0] bits<br>( <a href="#">Table 7</a> ) | HPMD[1:0] bits, CM2[1:0] bits<br>( <a href="#">Table 9</a> ) |
| Sampling Frequency     | FS[4:0] bits<br>( <a href="#">Table 6</a> )                 | FS[4:0] bits<br>( <a href="#">Table 8</a> ) | FS2[4:0] bits<br>( <a href="#">Table 10</a> )                |

The AK4331 can be operated in both master and slave modes. Clock mode of the LRCK pin and the BCLK pin can be selected by MS bit. When using master mode, the LRCK pin and the BCLK pin should be pulled down or pulled up with an external resistor (about 100 kΩ) because both pins are floating state until MS bit becomes “1”.

Table 3. Master / Slave Mode Select

| MS bit | LRCK pin, BCLK pin |           |
|--------|--------------------|-----------|
| 0      | Slave Mode         | (default) |
| 1      | Master Mode        |           |

Master / slave mode switching is not allowed while the AK4331 is in normal operation. The SRC, DAC and headphone amplifier must be powered down and PMTIM bit must be “0” before master / slave mode is switched. Furthermore, PLL and charge pump must also be powered down in case that sampling frequency is changed or SRCMCLK / DACCLK is stopped.

#### <MS bit Setting Sequence Example>

1. SRC, DAC, Headphone Amplifier (PLL, Charge Pump) Power-Down
2. Clock Mode of ACPU Setting (In case clock mode of ACPU is master, switch to slave.)
3. MS bit Selection
4. Clock Mode of ACPU Setting (In case clock mode of ACPU is slave, switch to master.)
5. SRC, DAC, Headphone Amplifier (PLL, Charge Pump) Power-Up

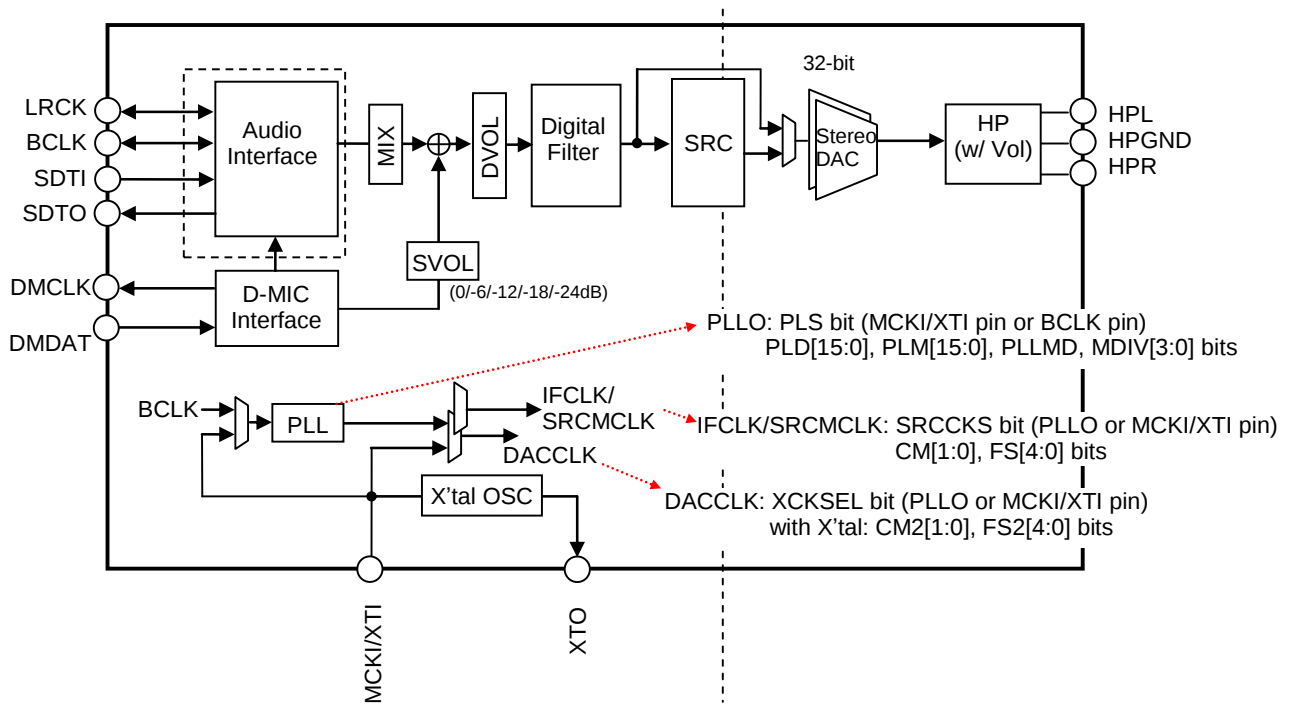


Figure 10. Internal configure diagram of AK4331

Table 4. Setting of Clock Select (x: Do not Care, S: Slave, M: Master)

| Mode | MS bit | PMOSC bit | PMPLL bit | PLS bit | PMSRC / SELDAIN bits | SRCCKS bit | XCKSEL bit | M/S | MCKI /XTI pin | LRCK BCLK pins | PLL Clock Source | SRC CLK  | DAC CLK |
|------|--------|-----------|-----------|---------|----------------------|------------|------------|-----|---------------|----------------|------------------|----------|---------|
| 1    | 0      | 0         | 0         | x       | 0                    | 1          | 1          | S   | MCLK          | In             | (PLL Disable)    | (Bypass) | MCKI    |
| 2    | 0      | 0         | 1         | 0       | 0                    | 0          | 0          | S   | MCLK          | In             | MCKI             | (Bypass) | PLLO    |
| 3    | 0      | 0         | 1         | 1       | 0                    | 0          | 0          | S   | VSS3          | In             | BCLK             | (Bypass) | PLLO    |
| 4    | 0      | 0         | 1         | 1       | 1                    | 0          | 0          | S   | VSS3          | In             | BCLK             | PLLO     | PLLO    |
| 5    | 0      | 1         | 1         | 1       | 1                    | 0          | 1          | S   | X'tal         | In             | BCLK             | PLLO     | XTI     |
| 6    | 0      | 1         | 0         | x       | 1                    | 1          | 1          | S   | X'tal         | In             | (PLL Disable)    | XTI      | XTI     |
| 7    | 1      | 0         | 0         | x       | 0                    | 1          | 1          | M   | MCLK          | Out            | (PLL Disable)    | (Bypass) | MCKI    |
| 8    | 1      | 0         | 1         | 0       | 0                    | 0          | 0          | M   | MCLK          | Out            | MCKI             | (Bypass) | PLLO    |
| 9    | 1      | 1         | 0         | x       | 0                    | 1          | 1          | M   | X'tal         | Out            | (PLL Disable)    | (Bypass) | XTI     |
| 10   | 1      | 1         | 1         | 0       | 0                    | 0          | 0          | M   | X'tal         | Out            | XTI              | (Bypass) | PLLO    |
| 11   | 1      | 0         | 0         | x       | 1                    | 1          | 1          | M   | MCLK          | Out            | (PLL Disable)    | MCKI     | MCKI    |
| 12   | 1      | 0         | 1         | 0       | 1                    | 0          | 0          | M   | MCLK          | Out            | MCKI             | PLLO     | PLLO    |
| 13   | 1      | 1         | 0         | x       | 1                    | 1          | 1          | M   | X'tal         | Out            | (PLL Disable)    | XTI      | XTI     |
| 14   | 1      | 1         | 1         | 0       | 1                    | 0          | 0          | M   | X'tal         | Out            | XTI              | PLLO     | PLLO    |

Note 107. Operation is only guaranteed with clock combinations in Table 4.

<Salve Mode: MS bit = "0">

1. SRC Bypass Mode (SELDAIN bit = "0")

DAC, Charge Pump, Headphone Amplifier: HPMD[1:0] bits, CM[1:0] bits, FS[4:0] bits

2. SRC Mode (SELDAIN bit = "1")

SRC (FSI): CM[1:0] bits, FS[4:0] bits

SRC (FSO), DAC, Charge Pump, Headphone Amplifier: HPMD[1:0] bits, CM2[1:0] bits, FS2[4:0] bits  
(DAC and Headphone Amplifier are operated by a X'tal)

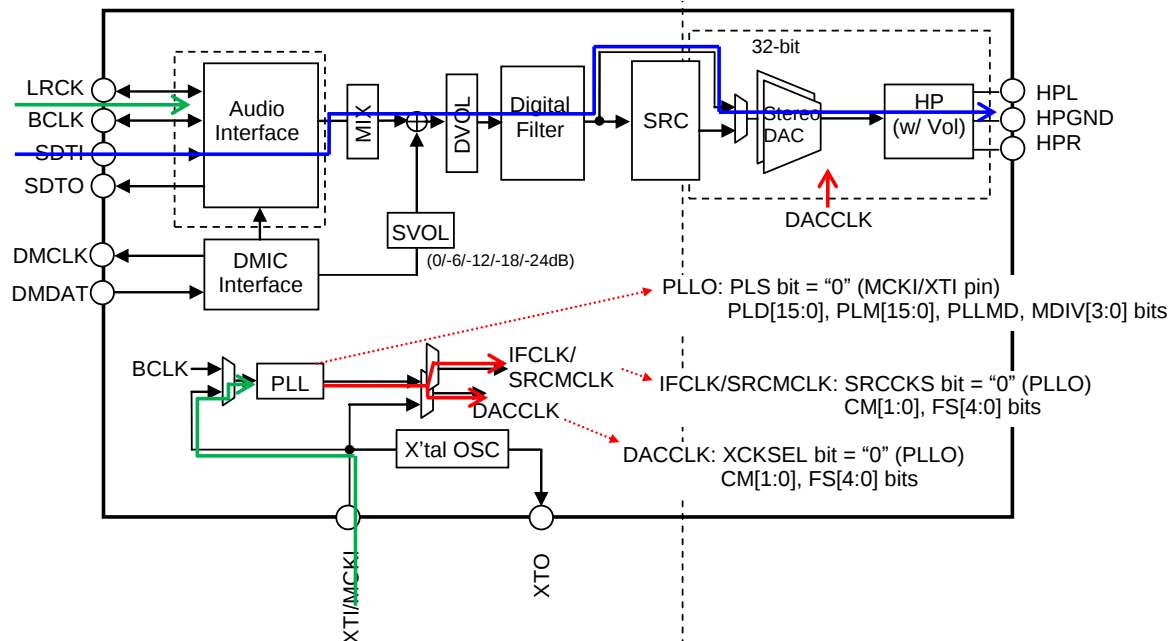


Figure 11. Example of Clock and Data Flow (Mode 2)

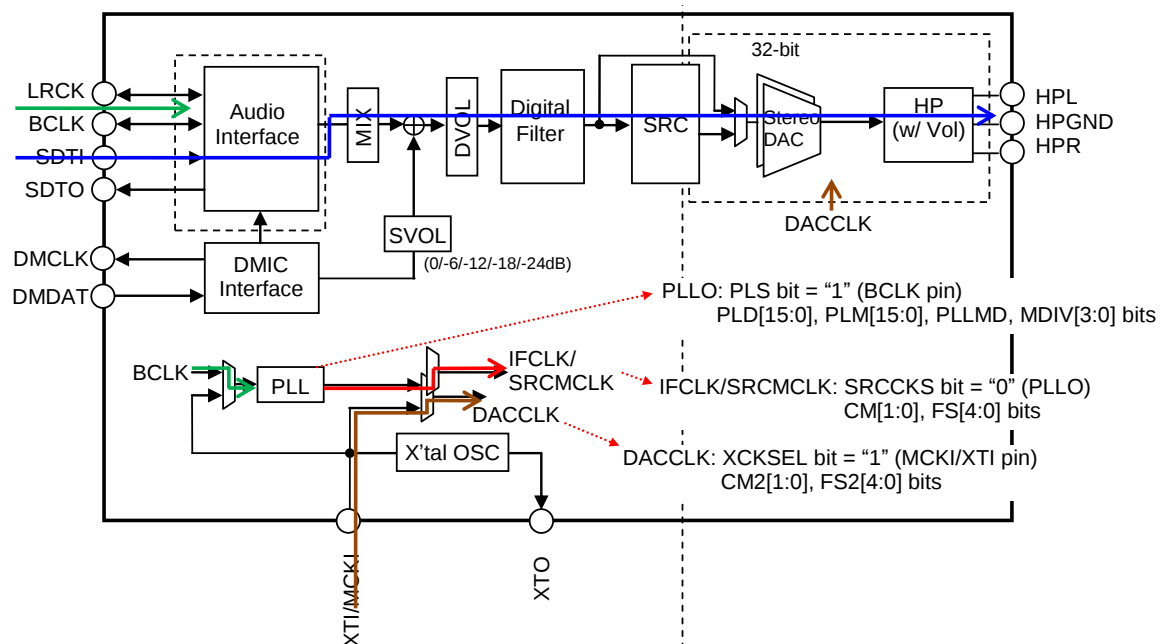


Figure 12. Example of Clock and Data Flow (Mode 5)

<Master Mode: MS bit = "1">

1. SRC Bypass Mode (SELDAIN bit = "0")

DAC, Charge Pump, Headphone Amplifier: HPMD[1:0] bits, CM[1:0] bits, FS[4:0] bits

2. SRC Mode (SELDAIN bit = "1")

SRC (FSI): CM[1:0] bits, FS[4:0] bits

SRC (FSO), DAC, Charge Pump, Headphone Amplifier: HPMD[1:0] bits, CM2[1:0] bits, FS2[4:0] bits  
(DAC and Headphone Amplifier are operated by a X'tal)

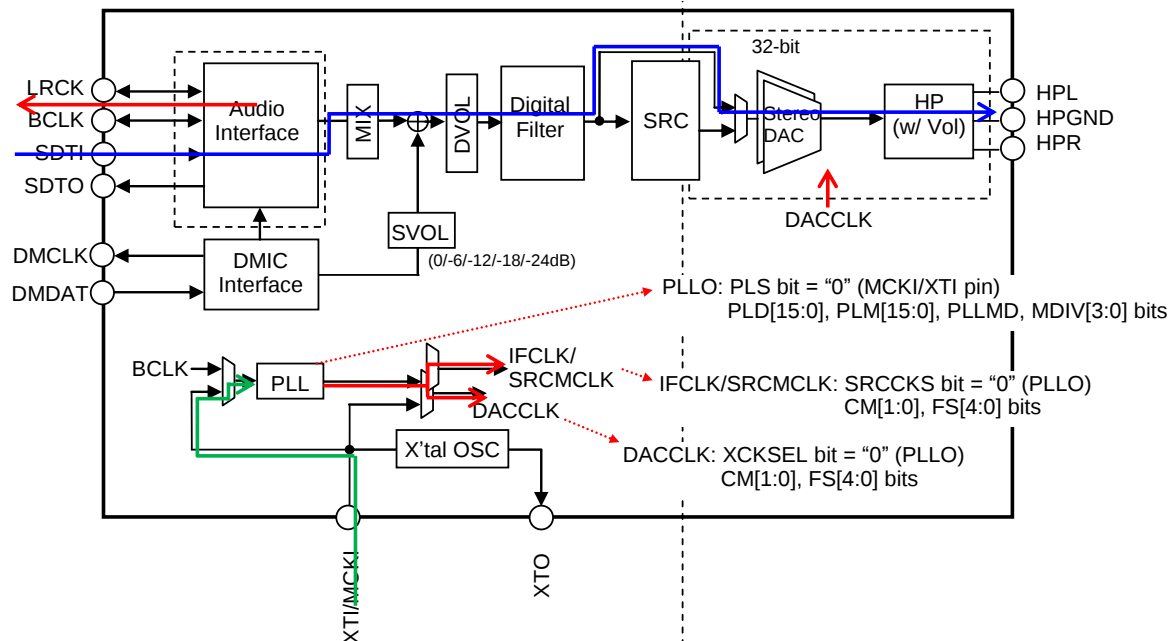


Figure 13. Example of Clock and Data Flow (Mode 8)

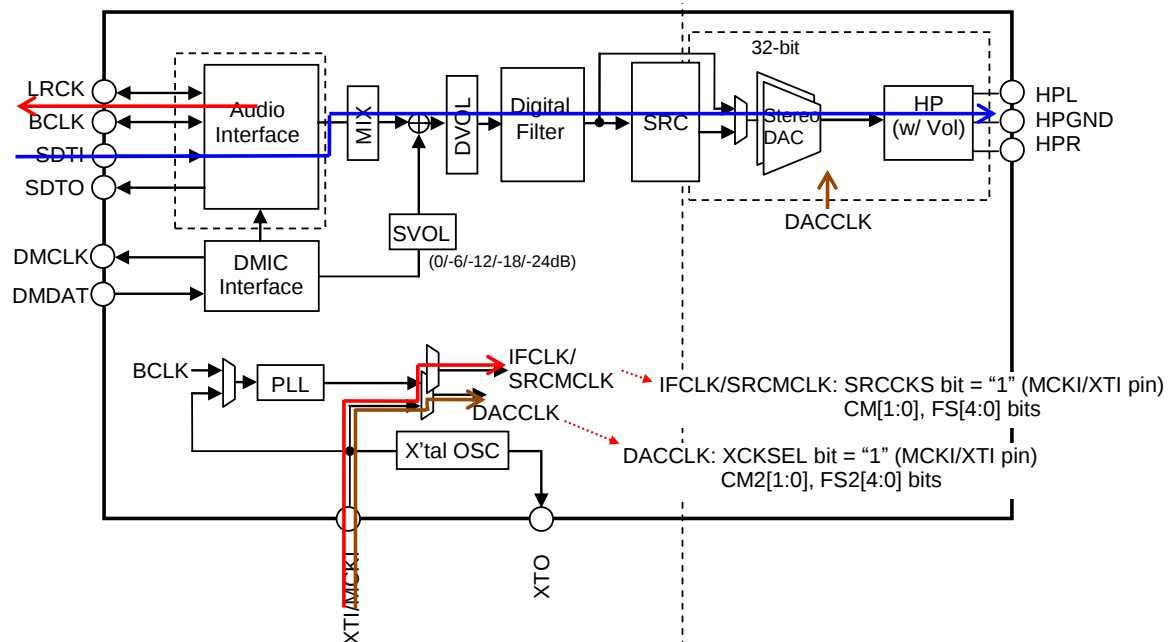


Figure 14. Example of Clock and Data Flow (Mode 11)

## &lt; Master Clock Frequency and Sampling Frequency Setting (SRC Bypass Mode) &gt;

Table 5. Setting of Master Clock Frequency (SRC Bypass Mode)

| HPMD1 bit | HPMD0 bit | CM1 bit | CM0 bit | Master Clock Frequency | Sampling Frequency Range |           |
|-----------|-----------|---------|---------|------------------------|--------------------------|-----------|
| 0         | 0         | 0       | 0       | 256fs                  | 8 to 48 kHz              | (default) |
| 1         | 1         | 0       | 0       | 256fs                  | 64 to 96 kHz             |           |
| 0         | 0         | 0       | 1       | 512fs                  | 8 to 48 kHz              |           |
| 0         | 0         | 1       | 0       | 1024fs                 | 8 to 24 kHz              |           |
| 1         | 1         | 1       | 1       | 128fs                  | 128 to 192 kHz           |           |

Table 6. Setting of Sampling Frequency (SRC Bypass Mode, N/A: Not available)

| FS4 bit | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency |           |
|---------|---------|---------|---------|---------|--------------------|-----------|
| 0       | 0       | 0       | 0       | 0       | 8 kHz              | (default) |
| 0       | 0       | 0       | 0       | 1       | 11.025 kHz         |           |
| 0       | 0       | 0       | 1       | 0       | 12 kHz             |           |
| 0       | 0       | 1       | 0       | 0       | 16 kHz             |           |
| 0       | 0       | 1       | 0       | 1       | 22.05 kHz          |           |
| 0       | 0       | 1       | 1       | 0       | 24 kHz             |           |
| 0       | 1       | 0       | 0       | 0       | 32 kHz             |           |
| 0       | 1       | 0       | 0       | 1       | 44.1 kHz           |           |
| 0       | 1       | 0       | 1       | 0       | 48 kHz             |           |
| 0       | 1       | 1       | 0       | 0       | 64 kHz             |           |
| 0       | 1       | 1       | 0       | 1       | 88.2 kHz           |           |
| 0       | 1       | 1       | 1       | 0       | 96 kHz             |           |
| 1       | 0       | 0       | 0       | 0       | 128 kHz            |           |
| 1       | 0       | 0       | 0       | 1       | 176.4 kHz          |           |
| 1       | 0       | 0       | 1       | 0       | 192 kHz            |           |
| Others  |         |         |         |         | N/A                |           |

\* Depending on setting of PLL's divider, the sampling frequency may differ.  
Please set PLD[15:0] and PLM[15:0] bits precisely.

## &lt; Master Clock Frequency and Sampling Frequency Setting (SRC Mode) &gt;

&lt;FSI&gt;

Table 7. Setting of Master Clock Frequency (SRC Mode: FSI)

| CM1 bit | CM0 bit | Master Clock Frequency | Sampling Frequency Range | (default) |
|---------|---------|------------------------|--------------------------|-----------|
| 0       | 0       | 256fs                  | 8 to 96 kHz              |           |
| 0       | 1       | 512fs                  | 8 to 48 kHz              |           |
| 1       | 0       | 1024fs                 | 8 to 24 kHz              |           |
| 1       | 1       | 128fs                  | 128 to 192 kHz           |           |

Table 8. Setting of Sampling Frequency (SRC Mode, N/A: Not available)

| FS4 bit | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency | (default) |
|---------|---------|---------|---------|---------|--------------------|-----------|
| 0       | 0       | 0       | 0       | 0       | 8 kHz              |           |
| 0       | 0       | 0       | 0       | 1       | 11.025 kHz         |           |
| 0       | 0       | 0       | 1       | 0       | 12 kHz             |           |
| 0       | 0       | 1       | 0       | 0       | 16 kHz             |           |
| 0       | 0       | 1       | 0       | 1       | 22.05 kHz          |           |
| 0       | 0       | 1       | 1       | 0       | 24 kHz             |           |
| 0       | 1       | 0       | 0       | 0       | 32 kHz             |           |
| 0       | 1       | 0       | 0       | 1       | 44.1 kHz           |           |
| 0       | 1       | 0       | 1       | 0       | 48 kHz             |           |
| 0       | 1       | 1       | 0       | 0       | 64 kHz             |           |
| 0       | 1       | 1       | 0       | 1       | 88.2 kHz           |           |
| 0       | 1       | 1       | 1       | 0       | 96 kHz             |           |
| 1       | 0       | 0       | 0       | 0       | 128 kHz            |           |
| 1       | 0       | 0       | 0       | 1       | 176.4 kHz          |           |
| 1       | 0       | 0       | 1       | 0       | 192 kHz            |           |
| Others  |         |         |         |         | N/A                |           |

\* Depending on setting of PLL's divider, the sampling frequency may differ.  
Please set PLD[15:0] and PLM[15:0] bits precisely.

&lt;FSO&gt;

Table 9. Setting of Master Clock Frequency (SRC Mode: FSO)

| HPMD1 bit | HPMD0 bit | CM21 bit | CM20 bit | Master Clock Frequency | Sampling Frequency Range |           |
|-----------|-----------|----------|----------|------------------------|--------------------------|-----------|
| 0         | 0         | 0        | 0        | 256fs                  | 8 to 48 kHz              | (default) |
| 1         | 1         | 0        | 0        | 256fs                  | 64 to 96 kHz             |           |
| 0         | 0         | 0        | 1        | 512fs                  | 8 to 48 kHz              |           |
| 0         | 0         | 1        | 0        | 1024fs                 | 8 to 24 kHz              |           |
| 1         | 1         | 1        | 1        | 128fs                  | 128 to 192 kHz           |           |

Table 10. Setting of Sampling Frequency (SRC Mode: FSO, N/A: Not available)

| FS24 bit | FS23 bit | FS22 bit | FS21 bit | FS20 bit | Sampling Frequency |           |
|----------|----------|----------|----------|----------|--------------------|-----------|
| 0        | 0        | 0        | 0        | 0        | 8 kHz              | (default) |
| 0        | 0        | 0        | 0        | 1        | 11.025 kHz         |           |
| 0        | 0        | 0        | 1        | 0        | 12 kHz             |           |
| 0        | 0        | 1        | 0        | 0        | 16 kHz             |           |
| 0        | 0        | 1        | 0        | 1        | 22.05 kHz          |           |
| 0        | 0        | 1        | 1        | 0        | 24 kHz             |           |
| 0        | 1        | 0        | 0        | 0        | 32 kHz             |           |
| 0        | 1        | 0        | 0        | 1        | 44.1 kHz           |           |
| 0        | 1        | 0        | 1        | 0        | 48 kHz             |           |
| 0        | 1        | 1        | 0        | 0        | 64 kHz             |           |
| 0        | 1        | 1        | 0        | 1        | 88.2 kHz           |           |
| 0        | 1        | 1        | 1        | 0        | 96 kHz             |           |
| 1        | 0        | 0        | 0        | 0        | 128 kHz            |           |
| 1        | 0        | 0        | 0        | 1        | 176.4 kHz          |           |
| 1        | 0        | 0        | 1        | 0        | 192 kHz            |           |
| Others   |          |          |          |          | N/A                |           |

\* Depending on setting of PLL's divider, the sampling frequency may differ.  
Please set PLD[15:0] and PLM[15:0] bits precisely.

## 9-2. Master Counter Synchronization Control

Internal master counter starts when setting PMTIM bit = "1". Phase difference can be controlled within 4/64fs by asserting PMTIM bit when using multiple AK4331's. In case of using PLL output (PLLO) as system clock, set PMTIM bit to "1" in 2 msec or more after setting PMPLL bit to "1". In case of using external clock as system clock, supply a stable clock and set PMTIM bit to "1". All power management bits except for PMOSC and PMPLL bits (PMCP1, PMCP2, PMLDO1P, PMLDO1N, PMSRC, PMSM, PMDA, PMHPL, PMHPR, PMDML and PMDMR bits) must be "0" when PMTIM bit = "0".

Table 11. Master Counter Power Control

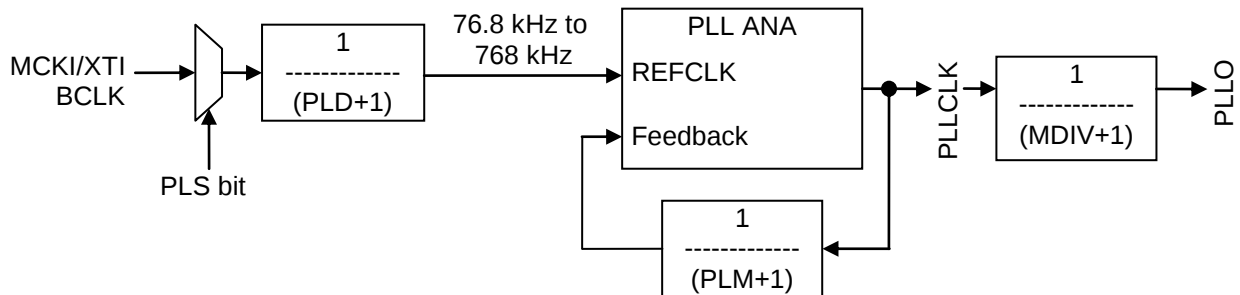
| PMTIM bit | Master Counter Status |           |
|-----------|-----------------------|-----------|
| 0         | Disable               | (default) |
| 1         | Enable                |           |

### 9-3. PLL

The PLL generates a PLLO which can be used as operation clock for the Digital Interface (IFCLK), the SRC (SRCMCLK) and the DAC (DACCLK). The oscillation frequency PLLCLK should be set in the range from 22.5792 to 24.576 MHz (Table 12 shows setting of 48 kHz, 44.1 kHz and 32 kHz base rates). Refer to Table 19 and Table 20 for PLL setting examples. Reference clock of PLL (REFCLK) should be set in the range from 76.8 kHz to 768 kHz.

Table 12. PLLCLK Setting

|        | 48 kHz base rate /<br>32 kHz base rate | 44.1 kHz base rate |
|--------|----------------------------------------|--------------------|
| PLLCLK | 24.576 MHz                             | 22.5792 MHz        |



$$\begin{aligned}\text{REFCLK} &= \text{PLL Source} / (\text{PLD}+1) \\ \text{PLLCLK} &= \text{REFCLK} \times (\text{PLM}+1) \\ \text{PLLO} &= \text{PLLCLK} / (\text{MDIV}+1)\end{aligned}$$

Figure 15. PLL Block Diagram

#### 9-3-1. Power Management (PMPLL)

PLL can be powered down by a control register setting.

Table 13. PLL Power Control

| PMPLL bit | PLL Status |           |
|-----------|------------|-----------|
| 0         | Power-Down | (default) |
| 1         | Power-Up   |           |

#### 9-3-2. Input Clock Select Function

The PLL has a function that selects the input clock. The clock source pin is selected by PLS bit. PLS bit must be set at PMTIM bit = "0".

Table 14. PLL Clock Source Select

| PLS bit | Clock Source |           |
|---------|--------------|-----------|
| 0       | MCKI/XTI pin | (default) |
| 1       | BCLK pin     |           |

### 9-3-3. PLL Reference Clock Divider

The PLL can set the dividing number of the reference clock in 16-bit. The input clock is used as PLL reference clock by dividing by (PLD + 1). PLD[15:0] bits must be set at PMTIM bit = "0".

Table 15. PLL Reference Clock Divider

| PLD[15:0] bits | Dividing Number | (default) |
|----------------|-----------------|-----------|
| 0000H          | 1               |           |
| 0001H to FFFFH | 1 / (PLD + 1)   |           |

Note 108. The reference clock divided by PLD should be set in the range from 76.8 kHz to 768 kHz.

### 9-3-4. PLL Feedback Clock Divider

The dividing number of feedback clock can be set freely in 16-bit. PLLCLK is divided by (PLM + 1) and used as PLL feedback clock. PLM[15:0] bits must be set at PMTIM bit = "0".

Table 16. PLL Feedback Clock Divider

| PLM[15:0] bits | Dividing Number | (default) |
|----------------|-----------------|-----------|
| 0000H          | Clock Stop      |           |
| 0001H to FFFFH | 1 / (PLM + 1)   |           |

### 9-3-5. PLL Internal Mode Setting

PLLMD bit controls PLL internal mode. Set PLLMD bit by referring to [Table 19](#) and [Table 20](#). PLLMD bit must be set at PMPLL bit = "0".

Table 17. PLL Internal Mode Setting

| PLLMD bit | Reference Clock | (default) |
|-----------|-----------------|-----------|
| 0         | ≥ 256 kHz       |           |
| 1         | < 256 kHz       |           |

### 9-3-6. PLLCLK Divider Setting

MDIV[3:0] bits control PLLCLK divider.  
MDIV[3:0] bits must be set at PMTIM bit = "0".

Table 18. PLLCLK Divider Setting

| MDIV[3:0] bits | Divide by               | (default) |
|----------------|-------------------------|-----------|
| 0H             | 1                       |           |
| 1H to FH       | $1 / (\text{MDIV} + 1)$ |           |

Note 109. When set each registers as following, divider value is set to 1.5 at MDIV[3:0] bits = 0H.

< SRC Bypass Mode (SELDAIN bit = "0"), SRCCKS bit = "0" and XCKSEL bit = "0" >

- CM[1:0] bits = "10", FS[4:0] bits = "00100" (1024fs, fs = 16 kHz)
- CM[1:0] bits = "01", FS[4:0] bits = "01000" (512fs, fs = 32 kHz)
- CM[1:0] bits = "00", FS[4:0] bits = "01100" (256fs, fs = 64 kHz)
- CM[1:0] bits = "11", FS[4:0] bits = "10000" (128fs, fs = 128 kHz)

< SRC Mode (SELDAIN bit = "1") and SRCCKS bit = "0" >

- CM[1:0] bits = "10", FS[4:0] bits = "00100" (1024fs, fs = 16 kHz)
- CM[1:0] bits = "01", FS[4:0] bits = "01000" (512fs, fs = 32 kHz)
- CM[1:0] bits = "00", FS[4:0] bits = "01100" (256fs, fs = 64 kHz)
- CM[1:0] bits = "11", FS[4:0] bits = "10000" (128fs, fs = 128 kHz)

< SRC Mode (SELDAIN bit = "1") and XCKSEL bit = "0" >

- CM2[1:0] bits = "10", FS2[4:0] bits = "00100" (1024fs, fs = 16 kHz)
- CM2[1:0] bits = "01", FS2[4:0] bits = "01000" (512fs, fs = 32 kHz)
- CM2[1:0] bits = "00", FS2[4:0] bits = "01100" (256fs, fs = 64 kHz)
- CM2[1:0] bits = "11", FS2[4:0] bits = "10000" (128fs, fs = 128 kHz)

## 9-3-7. PLL Setting Examples

Table 19. PLL Setting Example (PLL reference source: MCKI)

| CLKIN  |                   | PLL Condition |                |       |              |                |                      | Sampling<br>Frequency<br>[Hz] |
|--------|-------------------|---------------|----------------|-------|--------------|----------------|----------------------|-------------------------------|
| Source | Frequency<br>[Hz] | PLD+1         | REFCLK<br>[Hz] | PLM+1 | PLLMD<br>bit | PLLCLK<br>[Hz] | MDIV+1<br>(Note 110) |                               |
| MCKI   | 9,600,000         | 25            | 384,000        | 64    | 0            | 24,576,000     | 0                    | 48,000                        |
|        |                   |               |                |       |              |                |                      | 32,000                        |
|        | 19,200,000        | 25            | 768,000        | 32    | 0            | 24,576,000     | 0                    | 48,000                        |
|        |                   |               |                |       |              |                |                      | 32,000                        |
|        | 12,288,000        | 16            | 768,000        | 32    | 0            | 24,576,000     | 0                    | 48,000                        |
|        |                   |               |                |       |              |                |                      | 32,000                        |
|        | 24,576,000        | 32            | 768,000        | 32    | 0            | 24,576,000     | 0                    | 48,000                        |
|        |                   |               |                |       |              |                |                      | 32,000                        |
|        | 12,000,000        | 125           | 96,000         | 256   | 1            | 24,576,000     | 0                    | 48,000                        |
|        |                   |               |                |       |              |                |                      | 32,000                        |
|        | 24,000,000        | 125           | 192,000        | 128   | 1            | 24,576,000     | 0                    | 48,000                        |
|        |                   |               |                |       |              |                |                      | 32,000                        |
|        | 9,600,000         | 125           | 76,800         | 294   | 1            | 22,579,200     | 0                    | 44,100                        |
|        | 19,200,000        | 125           | 153,600        | 147   | 1            | 22,579,200     | 0                    | 44,100                        |
|        | 11,289,600        | 16            | 705,600        | 32    | 0            | 22,579,200     | 0                    | 44,100                        |
|        | 22,579,200        | 32            | 705,600        | 32    | 0            | 22,579,200     | 0                    | 44,100                        |

Note 110. At the case of CM[1:0] bits and CM2[1:0] bits are set to "01" (512fs).

Table 20. PLL Setting Example (PLL reference source: BCLK)

| CLKIN          |                   | PLL Condition |                |       |              |                |                      | Sampling<br>Frequency<br>[Hz] |
|----------------|-------------------|---------------|----------------|-------|--------------|----------------|----------------------|-------------------------------|
| Source         | Frequency<br>[Hz] | PLD+1         | REFCLK<br>[Hz] | PLM+1 | PLLMD<br>bit | PLLCLK<br>[Hz] | MDIV+1<br>(Note 110) |                               |
| BCLK<br>(32fs) | 256,000           | 1             | 256,000        | 96    | 0            | 24,576,000     | 5                    | 8,000                         |
|                | 352,800           | 1             | 352,800        | 64    | 0            | 22,579,200     | 3                    | 11,025                        |
|                | 512,000           | 1             | 512,000        | 48    | 0            | 24,576,000     | 2                    | 16,000                        |
|                | 705,600           | 1             | 705,600        | 32    | 0            | 22,579,200     | 1                    | 22,050                        |
|                | 768,000           | 1             | 768,000        | 32    | 0            | 24,576,000     | 1                    | 24,000                        |
|                | 1,024,000         | 2             | 512,000        | 48    | 0            | 24,576,000     | 0                    | 32,000                        |
|                | 1,411,200         | 2             | 705,600        | 32    | 0            | 22,579,200     | 0                    | 44,100                        |
|                | 1,536,000         | 2             | 768,000        | 32    | 0            | 24,576,000     | 0                    | 48,000                        |
| BCLK<br>(48fs) | 384,000           | 1             | 384,000        | 64    | 0            | 24,576,000     | 5                    | 8,000                         |
|                | 529,200           | 3             | 176,400        | 128   | 1            | 22,579,200     | 3                    | 11,025                        |
|                | 768,000           | 1             | 768,000        | 32    | 0            | 24,576,000     | 2                    | 16,000                        |
|                | 1,058,400         | 3             | 352,800        | 64    | 0            | 22,579,200     | 1                    | 22,050                        |
|                | 1,152,000         | 3             | 384,000        | 64    | 0            | 24,576,000     | 1                    | 24,000                        |
|                | 1,536,000         | 2             | 768,000        | 32    | 0            | 24,576,000     | 0                    | 32,000                        |
|                | 2,116,800         | 3             | 705,600        | 32    | 0            | 22,579,200     | 0                    | 44,100                        |
|                | 2,304,000         | 3             | 768,000        | 32    | 0            | 24,576,000     | 0                    | 48,000                        |
| BCLK<br>(64fs) | 512,000           | 1             | 512,000        | 48    | 0            | 24,576,000     | 5                    | 8,000                         |
|                | 705,600           | 1             | 705,600        | 32    | 0            | 22,579,200     | 3                    | 11,025                        |
|                | 1,024,000         | 2             | 512,000        | 48    | 0            | 24,576,000     | 2                    | 16,000                        |
|                | 1,411,200         | 2             | 705,600        | 32    | 0            | 22,579,200     | 1                    | 22,050                        |
|                | 1,536,000         | 2             | 768,000        | 32    | 0            | 24,576,000     | 1                    | 24,000                        |
|                | 2,048,000         | 4             | 512,000        | 48    | 0            | 24,576,000     | 0                    | 32,000                        |
|                | 2,822,400         | 4             | 705,600        | 32    | 0            | 22,579,200     | 0                    | 44,100                        |
|                | 3,072,000         | 4             | 768,000        | 32    | 0            | 24,576,000     | 0                    | 48,000                        |

## 9-4. Crystal Oscillator

The clock for the MCKI/XTI pin can be generated by two methods. PMOSC bit must be set to “1” when using a crystal oscillator.

### 1) X'tal Mode (PMOSC bit = “1”)

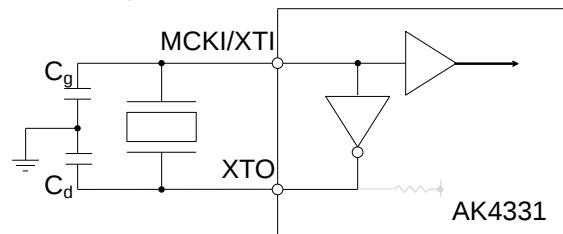


Figure 16. X'tal Mode

Note 111. The capacitor value is dependent on the crystal oscillator.

$C_d = C_g = 20.0 \text{ pF (Max.)}$ ,  $R_l$  (Equivalent Series Resistance) =  $80\Omega$  (Max.) @ 24.576 MHz

$C_d = C_g = 21.5 \text{ pF (Max.)}$ ,  $R_l$  (Equivalent Series Resistance) =  $60\Omega$  (Max.) @ 19.2 MHz

$C_d = C_g = 30.6 \text{ pF (Max.)}$ ,  $R_l$  (Equivalent Series Resistance) =  $200\Omega$  (Max.) @ 11.2896 MHz

### 2) External Clock Mode (PMOSC bit = “0”)

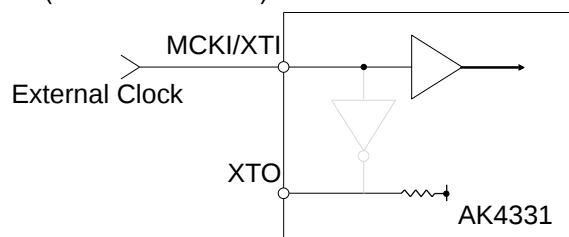


Figure 17. External Clock Mode

Note 112. Do not input a clock more than TVDD.

### 3) OFF Mode (Not Using the MCKI/XTI pin and the XTO pin (PMOSC bit = “0”))

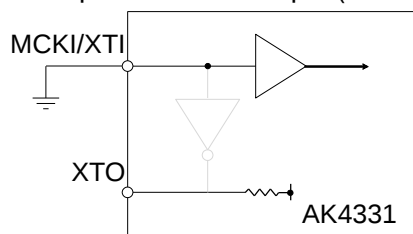


Figure 18. OFF Mode

## 9-5. Digital Microphone

### 1. Connection to Digital Microphone

The same power supply as AVDD must be provided to the digital microphone. The Figure 19 and Figure 20 show mono/stereo connection examples. The AK4331 provides DMCLK to a digital microphone by converting IFCLK to 64fs with a built-in decimation filter. Accordingly, the digital microphone generates 1-bit data by  $\Delta\Sigma$  Modulators and transmits to the DMDAT pin of the AK4331. PMDML/R bits control power-up/down of the digital block (Decimation Filter and HPF). The DCLKE bit controls ON/OFF of the output clock from the DMCLK pin. When the AK4331 is powered up (PDN pin = "H"), external pull-down resistor (R) should be connected to the DMDAT pin to avoid floating state.

**Note that the digital microphone sampling frequency is 96 kHz at maximum and interface does not support quad speed mode ( $f_s \geq 128$  kHz).**

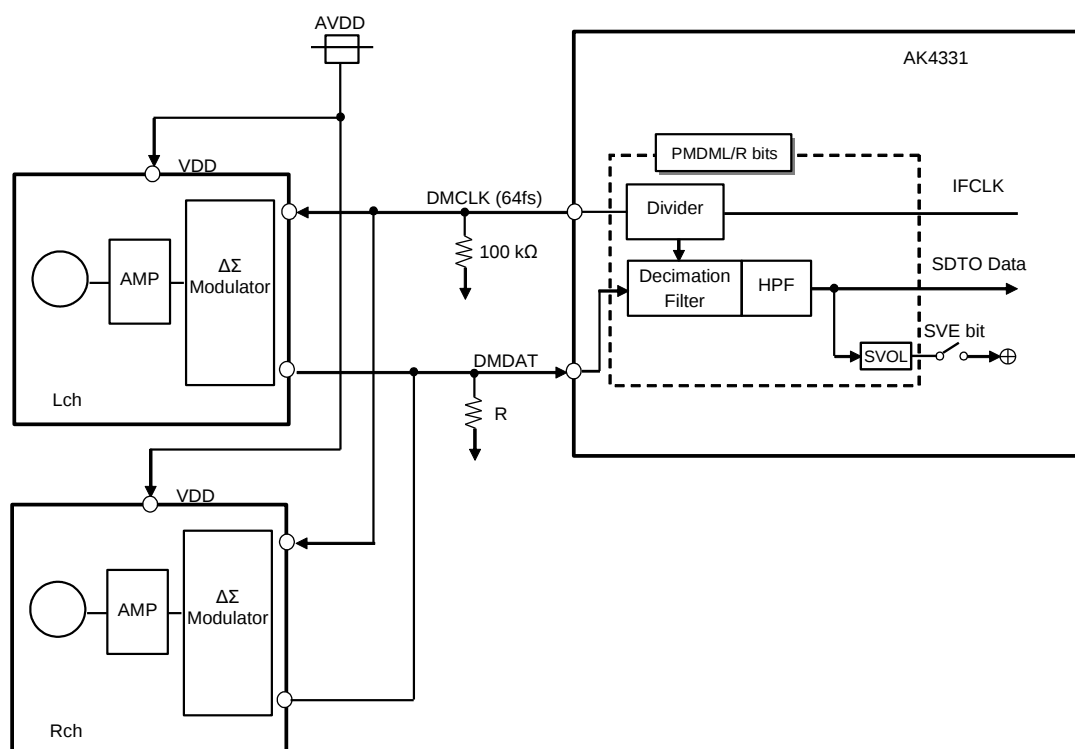


Figure 19. Connection Example of Stereo Digital Microphone

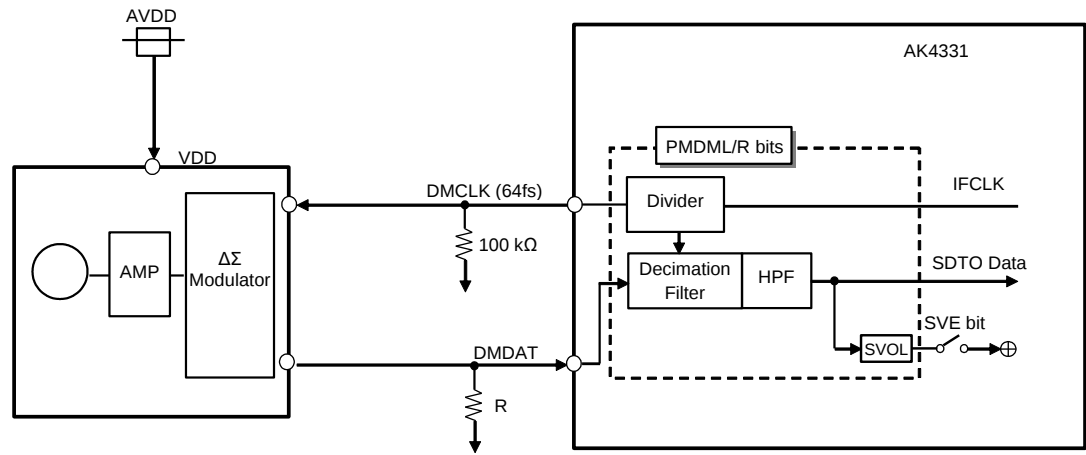


Figure 20. Connection Example of Mono Digital Microphone

2. Interface

The input data channel of the DMDAT pin is set by DCLKP bit. When DCLKP bit = “1”, L channel data is input to the Decimation Filter if DMCLK signal = “H”, R channel data is input if DMCLK signal = “L”. When DCLKP bit = “0”, R channel data is input to the Decimation Filter if DMCLK signal = “H”, L channel data is input if DMCLK signal = “L”. The DMCLK pin outputs “L” when DCLKE bit = “0”, and only supports 64fs. The output data through “the Decimation and Digital Filters” is the negative full-scale with the 0% 1’s density of 1-bit output data and positive full-scale with the 100% 1’s density of 1-bit output data. DCLKP bit must be set at PMDML/R bits = “0”.

Table 21. Data Input/Output Timing with Digital Microphone

| DCLKP bit | DMCLK pin = “H” | DMCLK pin = “L” | (default) |
|-----------|-----------------|-----------------|-----------|
| 0         | Rch             | Lch             |           |
| 1         | Lch             | Rch             |           |

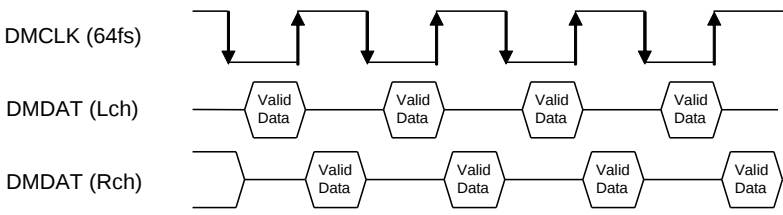


Figure 21. Data Input/Output Timing with Digital Microphone (DCLKP bit = “0”)

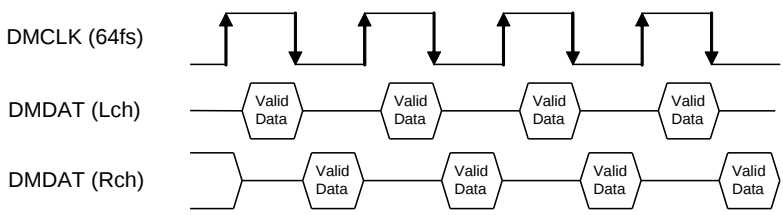


Figure 22. Data Input/Output Timing with Digital Microphone (DCLKP bit = “1”)

### 9-6. Digital Microphone HPF

A digital High Pass Filter (HPF) is integrated for DC offset cancellation of the digital microphone input. The cut-off frequencies are set by HPFC[1:0] bits (Table 22). It is proportional to the sampling frequency (fs) and default is 29.8 Hz (@fs = 48 kHz). HPFADN bit controls the ON/OFF of the HPF (Recommend HPF enable). HPFC[1:0] bits must be set at PMDML/R bits = "0".

Table 22. Digital Microphone HPF Cut-Off Frequency

| HPFC1 bit | HPFC0 bit | Cut-Off Frequency |             |             | (default) |
|-----------|-----------|-------------------|-------------|-------------|-----------|
|           |           | fs = 8 kHz        | fs = 48 kHz | fs = 96 kHz |           |
| 0         | 0         | 4.97 Hz           | 29.8 Hz     | 59.9 Hz     | (default) |
| 0         | 1         | 2.49 Hz           | 14.9 Hz     | 29.8 Hz     |           |
| 1         | 0         | 19.9 Hz           | 119.4 Hz    | 238.7 Hz    |           |
| 1         | 1         | 39.8 Hz           | 238.7 Hz    | 477.5 Hz    |           |

### 9-7. Digital Microphone Mono/Stereo Mode

PMDML and PMDMR bits set On/Off and mono/stereo operation of the digital microphone.

Table 23. Digital Microphone Mono/Stereo Select

| PMDMR bit | PMDML bit | SDTO Rch data         | SDTO Lch data         | (default) |
|-----------|-----------|-----------------------|-----------------------|-----------|
| 0         | 0         | All "0"               | All "0"               |           |
| 0         | 1         | DMIC Lch Input Signal | DMIC Lch Input Signal |           |
| 1         | 0         | DMIC Rch Input Signal | DMIC Rch Input Signal |           |
| 1         | 1         | DMIC Rch Input Signal | DMIC Lch Input Signal |           |

### 9-8. Digital Microphone Initialization Cycle

Initialization cycle of the digital microphone starts by setting PMDML and PMDMR bits to "1" from "0". The initialization cycle is set by ADRST[1:0] bits (Table 24). The outputs data of the DMDAT pin will become a data corresponds to analog input signal and settle after the initialization cycle is finished. ADRST[1:0] bits must be set at PMDML/R bits = "0".

Note 113. The initial data of the digital microphone has an offset that depends on the usage environment such as microphone, and the cut-off frequency of HPF. Set the initialization cycle longer or discard the initial data of the digital microphone if this offset causes a problem.

Table 24. Digital Microphone Initialization Cycle

| ADRST1 bit | ADRST0 bit | Digital MIC Initialization Cycle |            |             |             | (default) |
|------------|------------|----------------------------------|------------|-------------|-------------|-----------|
|            |            | Cycle                            | fs = 8 kHz | fs = 48 kHz | fs = 96 kHz |           |
| 0          | 0          | 1059/fs                          | 132.4 msec | 22 msec     | 11 msec     | (default) |
| 0          | 1          | 267/fs                           | 33.4 msec  | 5.6 msec    | 2.8 msec    |           |
| 1          | 0          | 2115/fs                          | 264.4 msec | 44.1 msec   | 22 msec     |           |
| 1          | 1          | 531/fs                           | 66.4 msec  | 11.1 msec   | 5.5 msec    |           |

### 9-9. Side Tone Digital Volume (SVOL)

The AK4331 has a side tone volume control (5 levels, 6 dB step, L/R channels common). The volume can be set by SV[2:0] bits and the attenuation range of the output data is from 0 to –24 dB. The volume is changed immediately by setting these bits. SVE bit can control whether adding a signal of the side tone block or not. SV[2:0] bits and SVE bit must be set when PMDML/R bits = “0”.

Table 25. Side Tone Control

| SVE bit | Side Tone Addition | (default) |
|---------|--------------------|-----------|
| 0       | Disable            |           |
| 1       | Enable             |           |

Table 26. Side Tone Volume Setting (N/A: Not available)

| SV[2:0] bits | Gain   | (default) |
|--------------|--------|-----------|
| 000          | 0 dB   |           |
| 001          | –6 dB  |           |
| 010          | –12 dB |           |
| 011          | –18 dB |           |
| 100          | –24 dB |           |
| Others       | N/A    |           |

## 9-10. DAC Digital Filter

DAC has four types of digital filter. The filter mode of DAC can be selected by DASD and DASL bits. The default setting is DASL = DASD bits = "0" (Sharp Roll-Off Filter). DASD bit and DASL bit must be set at PMSRC bit = "0" and PMDA bit = "0". And DADFSEL bit coordinate digital filter. In case of SRC Bypass Mode, DADFSEL bit must be set to "0". In case of SRC Mode, DADFSEL bit must be set to "1".

Table 27. DAC Digital Filter Setting (SRC Bypass Mode)

| DADFSEL bit | DASD bit | DASL bit | DAC Filter Mode Setting           |           |
|-------------|----------|----------|-----------------------------------|-----------|
| 0           | 0        | 0        | Sharp Roll-Off Filter             | (default) |
| 0           | 0        | 1        | Slow Roll-Off Filter              |           |
| 0           | 1        | 0        | Short Delay Sharp Roll-Off Filter |           |
| 0           | 1        | 1        | Short Delay Slow Roll-Off Filter  |           |

Table 28. DAC Digital Filter Setting (SRC Mode)

| DADFSEL bit | DASD bit | DASL bit | DAC Filter Mode Setting           |
|-------------|----------|----------|-----------------------------------|
| 1           | 0        | 0        | Sharp Roll-Off Filter             |
| 1           | 0        | 1        | Slow Roll-Off Filter              |
| 1           | 1        | 0        | Short Delay Sharp Roll-Off Filter |
| 1           | 1        | 1        | Short Delay Slow Roll-Off Filter  |

## 9-11. Digital Mixing

The AK4331 has digital mixing circuits for each L channel and R channel. They can mix the data digitally and convert the polarity. The inverted data by this polarity conversion is calculated in 2's complement format. MDACL/R bits, RDACL/R bits, LDACL/R bits and INVL/R bits must be set at PMSRC bits = "0" and PMDA bit = "0".

Table 29. DAC L/R Channel Input Signal Select

| MDACL bit<br>MDACR bit | RDACL bit<br>RDACR bit | LDACL bit<br>LDACR bit | DAC Lch Input Data<br>DAC Rch Input Data |           |
|------------------------|------------------------|------------------------|------------------------------------------|-----------|
| 0                      | 0                      | 0                      | MUTE                                     | (default) |
| 0                      | 0                      | 1                      | Lch                                      |           |
| 0                      | 1                      | 0                      | Rch                                      |           |
| 0                      | 1                      | 1                      | Lch + Rch                                |           |
| 1                      | 0                      | 0                      | MUTE                                     |           |
| 1                      | 0                      | 1                      | Lch / 2                                  |           |
| 1                      | 1                      | 0                      | Rch / 2                                  |           |
| 1                      | 1                      | 1                      | (Lch + Rch) / 2                          |           |

Table 30. DAC L/R Channel Input Signal Polarity Select

| INVL bit<br>INVR bit | Output Data |           |
|----------------------|-------------|-----------|
| 0                    | Normal      | (default) |
| 1                    | Inverting   |           |

## 9-12. Digital Volume

The AK4331 has a 32-level digital volume in front of DAC for each L and R channel. The volume is changed from +3 dB to –12 dB in 0.5 dB step including Mute. The volume change is executed immediately by setting registers.

When OVOLCN bit is “1”, the OVL[4:0] bits control L channel level and OVR[4:0] bits control R channel level. When OVOLCN bit = “0”, the OVL[4:0] bits control both L channel and R channel attenuation levels. In this case, the setting of OVR[4:0] bits is ignored. OVL/R[4:0] bits must be set at PMSRC bits = “0” and PMDA bit = “0”.

Table 31. Digital Volume Setting

| OVL[4:0] bits<br>OVR[4:0] bits | Volume (dB) |           |
|--------------------------------|-------------|-----------|
| 1FH                            | +3.0        |           |
| 1EH                            | +2.5        |           |
| 1DH                            | +2.0        |           |
| 1CH                            | +1.5        |           |
| 1BH                            | +1.0        |           |
| 1AH                            | +0.5        |           |
| 19H                            | 0.0         | (default) |
| 18H                            | –0.5        |           |
| 17H                            | –1.0        |           |
| 16H                            | –1.5        |           |
| 15H                            | –2.0        |           |
| 14H                            | –2.5        |           |
| 13H                            | –3.0        |           |
| 12H                            | –3.5        |           |
| 11H                            | –4.0        |           |
| 10H                            | –4.5        |           |
| 0FH                            | –5.0        |           |
| 0EH                            | –5.5        |           |
| 0DH                            | –6.0        |           |
| 0CH                            | –6.5        |           |
| 0BH                            | –7.0        |           |
| 0AH                            | –7.5        |           |
| 09H                            | –8.0        |           |
| 08H                            | –8.5        |           |
| 07H                            | –9.0        |           |
| 06H                            | –9.5        |           |
| 05H                            | –10.0       |           |
| 04H                            | –10.5       |           |
| 03H                            | –11.0       |           |
| 02H                            | –11.5       |           |
| 01H                            | –12.0       |           |
| 00H                            | MUTE        |           |

### 9-13. Headphone Amplifier Output (HPL/HPR pins)

Headphone amplifiers are operated by positive and negative power that is supplied from internal charge pump circuit. The VEE2 pin output the negative voltage generated by the internal charge pump circuit from CVDD. This charge pump circuit is switched between VDD mode and 1/2VDD mode by the output level of the headphone amplifiers. The headphone amplifier output is single-ended and centered on HPGND (0 V). Therefore, a capacitor for AC-coupling is not necessary. The minimum load resistance is 7.2Ω. The output power is 10 mW (@ 0 dBFS,  $R_L = 32\Omega$ ,  $AVDD = CVDD = 1.8\text{ V}$  and  $HPG = -4\text{ dB}$ ) and 25 mW (@ 0 dBFS,  $R_L = 32\Omega$ ,  $AVDD = CVDD = 1.8\text{ V}$  and  $HPG = 0\text{ dB}$ ). Ground loop noise cancelling function for headphone amplifier is available by connecting the HPGND pin to the ground of the jack.

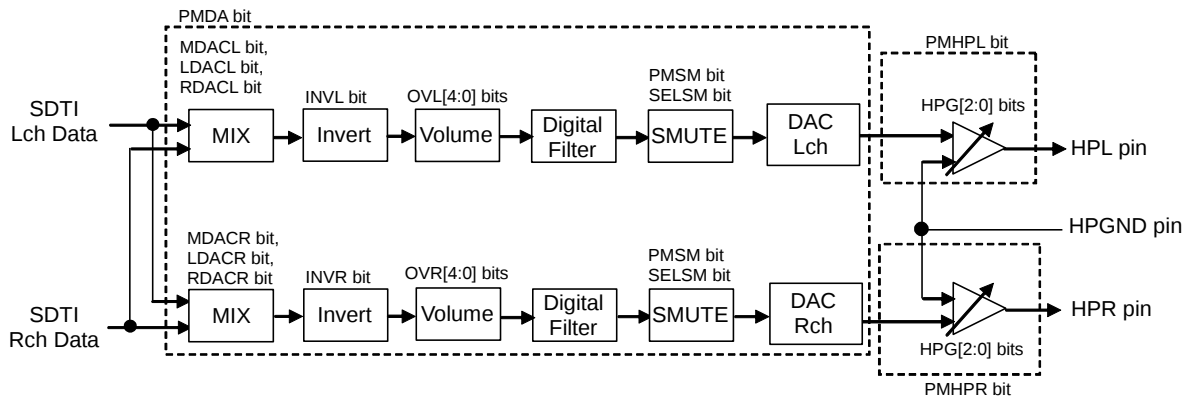


Figure 23. DAC & Headphone Amplifier Block Diagram (SRC Bypass Mode)

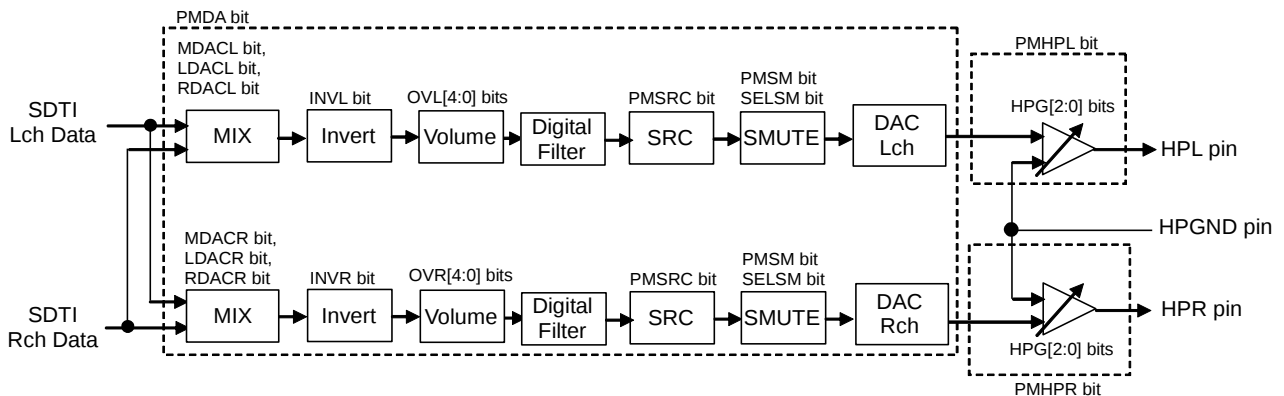


Figure 24. DAC & Headphone Amplifier Block Diagram (SRC Mode)

Table 32. Charge Pump Mode Setting (N/A: Not available)

| CPMODE1 bit | CPMODE0 bit | Mode                   | Operation Voltage   | (default) |
|-------------|-------------|------------------------|---------------------|-----------|
| 0           | 0           | Class-G Operation Mode | Automatic Switching |           |
| 0           | 1           | VDD Operation Mode     | $\pm VDD$           |           |
| 1           | 0           | 1/2VDD Operation Mode  | $\pm 1/2VDD$        |           |
| 1           | 1           | N/A                    | N/A                 |           |

**< Class-G Mode Switching Level >**

A switching threshold level of VDD and 1/2VDD modes can be set by LVDSSEL[1:0] bits. LVDSSEL[1:0] bits should be set before PMHPL bit or PMHPR bit is set to "1".

**LVDSSEL bits = "00" (default: Assuming connecting a 16Ω headphone)**

VDD → 1/2VDD: < 1.05 mW at both channels (@CVDD = 1.8 V,  $R_L$  = 16Ω)

1/2VDD → VDD: ≥ 1.05 mW at either channel (@CVDD = 1.8 V,  $R_L$  = 16Ω)

**LVDSSEL bits = "01" (Assuming connecting a 32Ω headphone or more)**

VDD → 1/2VDD: < 1.05 mW at both channels (@CVDD = 1.8 V,  $R_L$  = 32Ω)

1/2VDD → VDD: ≥ 1.05 mW at either channel (@CVDD = 1.8 V,  $R_L$  = 32Ω)

**LVDSSEL bits = "10" (Assuming connecting a 11Ω headphone)**

VDD → 1/2VDD: < 1.05 mW at both channels (@CVDD = 1.8 V,  $R_L$  = 11Ω)

1/2VDD → VDD: ≥ 1.05 mW at either channel (@CVDD = 1.8 V,  $R_L$  = 11Ω)

**LVDSSEL bits = "11" (Assuming connecting a 8Ω headphone)**

VDD → 1/2VDD: < 1.05 mW at both channels (@CVDD = 1.8 V,  $R_L$  = 8Ω)

1/2VDD → VDD: ≥ 1.05 mW at either channel (@CVDD = 1.8 V,  $R_L$  = 8Ω)

When the charge pump operation mode is changed to VDD mode from 1/2VDD mode, an internal counter for holding VDD mode starts (Table 33). The charge pump changes to 1/2VDD mode if the output signal level is lower than the switching level and 1/2VDD mode detection time that is set by LVDTM[2:0] bits is passed after VDD mode hold time is finished.

Table 33. VDD Mode Holding Period Setting (x: Do not Care)

| VDDTM[3:0]<br>bits | VDD Mode Holding Period |            |             |             |             | (default) |
|--------------------|-------------------------|------------|-------------|-------------|-------------|-----------|
|                    |                         | 8 kHz      | 48 kHz      | 96 kHz      | 192 kHz     |           |
| 0000               | 1024/fs                 | 128 msec   | 21.3 msec   | 10.7 msec   | 5.3 msec    | (default) |
| 0001               | 2048/fs                 | 256 msec   | 42.7 msec   | 21.3 msec   | 10.7 msec   |           |
| 0010               | 4096/fs                 | 512 msec   | 85.3 msec   | 42.7 msec   | 21.3 msec   |           |
| 0011               | 8192/fs                 | 1024 msec  | 170.7 msec  | 85.3 msec   | 42.7 msec   |           |
| 0100               | 16384/fs                | 2048 msec  | 341.3 msec  | 170.7 msec  | 85.3 msec   |           |
| 0101               | 32768/fs                | 4096 msec  | 682.7 msec  | 341.3 msec  | 170.7 msec  |           |
| 0110               | 65536/fs                | 8192 msec  | 1365.3 msec | 682.7 msec  | 341.3 msec  |           |
| 0111               | 131072/fs               | 16384 msec | 2730.7 msec | 1365.3 msec | 682.7 msec  |           |
| 1xxx               | 262144/fs               | 32768 msec | 5461.3 msec | 2730.7 msec | 1365.3 msec |           |

When the output voltage becomes less than class-G mode switching level, the internal detection counter for 1/2VDD mode which is set by LVDTM[2:0] bits starts. This counter is reset when the output voltage exceeds class-G mode switching level. The charge pump operation mode is changed to 1/2VDD from VDD if the detection counter of 1/2VDD mode is finished and also the VDD mode hold period is passed.

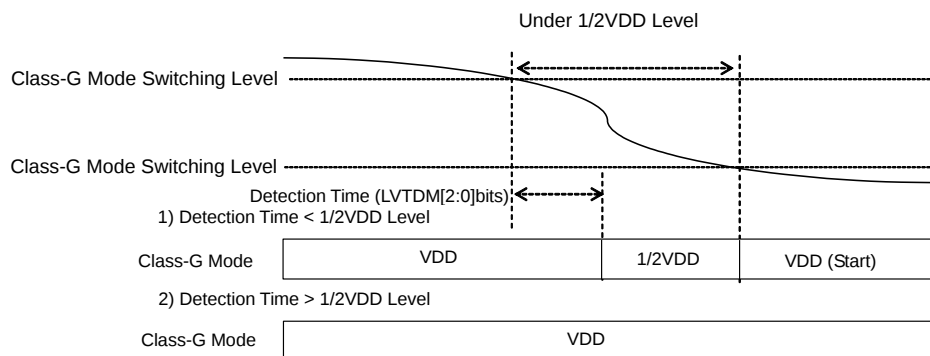


Figure 25. Transition to 1/2VDD Mode from VDD Mode

Table 34. 1/2VDD Detection Period (Minimum frequency that is not detected)

| LVDTM[2:0]<br>bits |         | 1/2VDD Mode Detection Time /<br>Minimum Frequency that is Not Detected |            |           |           |           |
|--------------------|---------|------------------------------------------------------------------------|------------|-----------|-----------|-----------|
|                    |         | 8 kHz                                                                  | 48 kHz     | 96 kHz    | 192 kHz   |           |
| 000                | 64/fs   | 8 msec                                                                 | 1.3 msec   | 0.67 msec | 0.33 msec | (default) |
|                    |         | 62.5 Hz                                                                | 375 Hz     | 750 Hz    | 1500 Hz   |           |
| 001                | 128/fs  | 16 msec                                                                | 2.7 msec   | 1.3 msec  | 0.67 msec |           |
|                    |         | 31.3 Hz                                                                | 187.5 Hz   | 375 Hz    | 750 Hz    |           |
| 010                | 256/fs  | 32 msec                                                                | 5.3 msec   | 2.7 msec  | 1.3 msec  |           |
|                    |         | 15.6 Hz                                                                | 93.8 Hz    | 187.5 Hz  | 375 Hz    |           |
| 011                | 512/fs  | 64 msec                                                                | 10.7 msec  | 5.3 msec  | 2.7 msec  |           |
|                    |         | 7.8 Hz                                                                 | 46.9 Hz    | 93.8 Hz   | 187.5 Hz  |           |
| 100                | 1024/fs | 128 msec                                                               | 21.3 msec  | 10.7 msec | 5.3 msec  |           |
|                    |         | 3.9 Hz                                                                 | 23.4 Hz    | 46.9 Hz   | 93.8 Hz   |           |
| 101                | 2048/fs | 256 msec                                                               | 42.7 msec  | 21.3 msec | 10.7 msec |           |
|                    |         | 2.0 Hz                                                                 | 11.7 Hz    | 23.4 Hz   | 46.9 Hz   |           |
| 110                | 4096/fs | 512 msec                                                               | 85.3 msec  | 42.7 msec | 21.3 msec |           |
|                    |         | 1.0 Hz                                                                 | 5.9 Hz     | 11.7 Hz   | 23.4 Hz   |           |
| 111                | 8192/fs | 1024 msec                                                              | 170.7 msec | 85.3 msec | 42.7 msec |           |
|                    |         | 0.5 Hz                                                                 | 2.8 Hz     | 5.9 Hz    | 11.7 Hz   |           |

### < Headphone Amplifier Volume Circuit >

The output level of the headphone amplifier can be controlled by HPG[2:0] bits. The volume setting is common for both L and R channels and ranges from +4 dB to -10 dB in 2 dB step (Table 35). When the volume is changed, zero cross detection is executed independently for L and R channels. Zero cross timeout period is set by HPTM[2:0] bits (Table 36).

The headphone amplifier volume should be changed with an interval of zero cross timeout period after setting HPG[2:0] bits once. If the volume is changed continuously without the interval, the gain setting at the next zero crossing point will be applied.

Table 35. Headphone Amplifier Volume Setting

| HPG[2:0] bits | Volume (dB) |
|---------------|-------------|
| 111           | +4          |
| 110           | +2          |
| 101           | 0           |
| 100           | -2          |
| 011           | -4          |
| 010           | -6          |
| 001           | -8          |
| 000           | -10         |

(default)

Table 36. Headphone Volume Zero Cross Timeout Setting (x: Do not care)

| HPTM[2:0]<br>bits | Zero Crossing Timeout Period |          |           |           |           |
|-------------------|------------------------------|----------|-----------|-----------|-----------|
|                   |                              | 8 kHz    | 48 kHz    | 96 kHz    | 192 kHz   |
| 000               | 128/fs                       | 16 msec  | 2.7 msec  | 1.3 msec  | 0.67 msec |
| 001               | 256/fs                       | 32 msec  | 5.3 msec  | 2.7 msec  | 1.3 msec  |
| 010               | 512/fs                       | 64 msec  | 10.7 msec | 5.3 msec  | 2.7 msec  |
| 011               | 1024/fs                      | 128 msec | 21.4 msec | 10.7 msec | 5.3 msec  |
| 1xx               | 2048/fs                      | 256 msec | 42.7 msec | 21.4 msec | 10.7 msec |

(default)

### < Headphone Amplifier External Circuit >

It is necessary to put an oscillation prevention circuit (0.1  $\mu$ F  $\pm$ 20% capacitor and 15 $\Omega$   $\pm$ 20% resistor) because there is a possibility that the headphone amplifier oscillates.

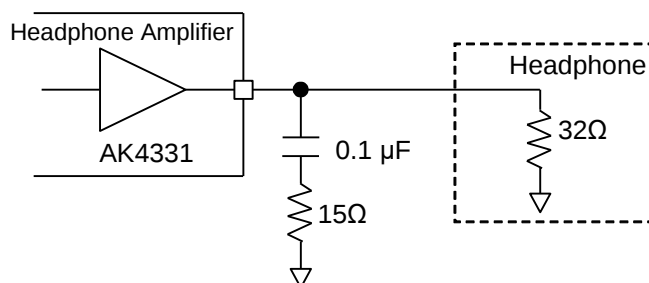


Figure 26. Example of Headphone Amplifier Oscillation Prevention Circuit

### < Power-Up/Down Sequence of Headphone Amplifier >

After releasing DAC power-down state by PMDA bit, the headphone amplifier should be powered up by PMHPL/R bits. A wait time from DAC power-up to headphone power-up is not necessary.

PMDA bit releases a power-down of the digital block of DAC, PMHPL or PMHPR bit powers up the analog block of the DAC and the headphone amplifier. Then, initialization cycle of the headphone amplifier is executed. The gain setting (HPG[2:0] bits) should be made before PMHPL bit or PMHPR bit is set to "1". Do not change the gain setting (HPG[2:0] bits) during the headphone initialization cycle. The gain setting can be changed after the headphone initialization cycle is finished. A wait time from the gain setting to PMHPL bit or PMHPR bit = "1" is not necessary.

When the AK4331 is powered down, the headphone amplifier should be powered down first. The DAC should be powered down next. A wait time from a headphone power-down to a DAC power-down is not necessary.

When the headphone amplifier is powered down, the HPL pin and the HPR pin are pulled down to HPGND via the internal pull-down register. The pulled-down resistor is 4Ω (Typ.) @ HPLHZ = HPRHZ bits = "0". The HPL pin and the HPR pin are also pulled down to HPGND via 95 kΩ (Typ.) if HPLHZ bit and HPRHZ bit are set to "1".

Table 37. Headphone Output Status (x: Do not Care)

| PMHPL bit<br>PMHPR bit | HPLHZ bit<br>HPRHZ bit | Headphone Amplifier Status |
|------------------------|------------------------|----------------------------|
| 0                      | 0                      | Pull-down by 4Ω (Typ.)     |
| 0                      | 1                      | Pull-down by 95 kΩ (Typ.)  |
| 1                      | x                      | Normal Operation           |

When the HPL pin and the HPR pin are connected to analog signal pins of an external device by Wire-OR, CP1, CP2, LDO1P and LDO1N should be powered up. Do not input a negative voltage to the HPL pin and the HPR pin when CP1, CP2, LDO1P and LDO1N are powered down.

To avoid pop noise, HPG[2:0] bits setting should be same at power-up and power-down of headphone.

The power-up time of headphone amplifier is shown in Table 38. The HPL and HPR pins output 0 V (HPGND) when the headphone amplifier is powered up. The power-down is executed immediately.

Table 38. Headphone Power-Up Time

| Sampling Frequency [kHz]       | Power-Up Time (Max) |
|--------------------------------|---------------------|
| 8/12/16/24/32/48/64/96/128/192 | 23.9 msec           |
| 11.025/22.05/44.1/88.2/176.4   | 25.9 msec           |

### < Over Current Protection Circuit >

If the headphone amplifier is in an overcurrent state, such as when output pins are shorted, the headphone amplifier limits the operation current. The headphone amplifier returns to a normal operation state if all causes are cleared.

## 9-14. Charge Pump & LDO Circuits

The charge pump circuits are operated by CVDD power supply voltage. CVDD is used to generate positive and negative voltage. The power-up/down sequence of charge pump and LDO circuits are as follows. CP1 should be powered up before LDO1P/N are powered up. CP2 should be powered up after LDO1P/N are powered up.

**Power-Up Sequence: CP1 → LDO1P, LDO1N → CP2**

**Power-Down Sequence: CP2 → LDO1P, LDO1N → CP1**

LDO1P and LDO1N have an overcurrent protection circuit. When overcurrent flows in a normal operation, the LDO1P and LDO1N circuits limit the operation current. If the overcurrent state is cleared, the overcurrent protection will be off and the LDO1P and LDO1N circuits will return to normal operation.

LDO2 has an overvoltage protection circuit. This overvoltage protection circuit powers the LDO2 down when the power supply becomes unstable by an instantaneous power failure, etc. during operation. The LDO2 circuit will not return to a normal operation until being reset by the PDN pin ("L" → "H") after removing the problems.

The charge pump and the LDO1 circuits, except for the LDO2, can be powered up again while they are in power-down state.

Table 39. Input/Output Voltage and Operation Block of the Charge Pump

| Charge Pump   | Power Management bit | Input Voltage | Output Voltage (Typ.) | Operation Block |
|---------------|----------------------|---------------|-----------------------|-----------------|
| CP1           | PMCP1                | CVDD          | −1.8 V                | LDO1N, DAC      |
| CP2 (Class-G) | PMCP2                | CVDD          | ±1.8 V / ±0.9 V       | Headphone       |

Table 40. Input/Output Voltage and Operation Block of the LDO

| LDO   | Power Management bit | Power Supply      | Output Voltage (Typ.) | Operation Block          |
|-------|----------------------|-------------------|-----------------------|--------------------------|
| LDO1P | PMLDO1P              | AVDD / VSS1       | +1.5 V                | VREF+ for DAC, Headphone |
| LDO1N | PMLDO1N              | VSS1 / CP1 Output | −1.5 V                | VREF− for DAC, Headphone |
| LDO2  | -                    | LVDD / VSS3       | +1.2 V                | Digital Core             |

### 9-15. Asynchronous Sampling Rate Converter (SRC)

The AK4331 has a stereo asynchronous SRC before the DAC block. The SRC supports an 8 kHz to 192 kHz audio source (FSI) and an 8 kHz to 192 kHz sampling rate output (FSO). Available sample rate ratio (FSO/FSI) is 0.98 to 6.02. PMSRC bit controls power up/down of the SRC.

Examples of supported sampling rate are shown below.

Table 41. Up-Sampling Examples

| FSO      | FSI      | FSO/FSI |
|----------|----------|---------|
| 192 kHz  | 48 kHz   | 4.00    |
| 96 kHz   | 48 kHz   | 2.00    |
| 48 kHz   | 48 kHz   | 1.00    |
| 48 kHz   | 44.1 kHz | 1.09    |
| 48 kHz   | 32 kHz   | 1.50    |
| 48 kHz   | 24 kHz   | 2.00    |
| 48 kHz   | 16 kHz   | 3.00    |
| 48 kHz   | 12 kHz   | 4.00    |
| 48 kHz   | 8 kHz    | 6.00    |
| 192 kHz  | 44.1 kHz | 4.35    |
| 44.1 kHz | 44.1 kHz | 1.00    |
| 44.1 kHz | 32 kHz   | 1.38    |
| 44.1 kHz | 24 kHz   | 1.84    |
| 44.1 kHz | 16 kHz   | 2.76    |
| 44.1 kHz | 12 kHz   | 3.68    |
| 44.1 kHz | 8 kHz    | 5.51    |
| 16 kHz   | 16 kHz   | 1.00    |
| 16 kHz   | 8 kHz    | 2.00    |
| 8 kHz    | 8 kHz    | 1.00    |

SRC input clock (SRCMCLK) is 128fs, 256fs, 512fs or 1024fs. SRCCKS bit selects SRC clock source between the MCKI/XTI pin and PLLO, and XCKSEL bit selects output clock for SRC (DACCLK) between the MCKI/XTI pin and PLLO. The SRC can be bypassed by setting SELDAIN bit = "0".

Table 42. SRC Power Management

| PMSRC bit | SRC Status |
|-----------|------------|
| 0         | Power-Down |
| 1         | Power-Up   |

(default)

Table 43. DAC and Charge Pump Clock Mode Setting

| XCKSEL bit | DAC and Charge Pump Clock Mode |
|------------|--------------------------------|
| 0          | PLLO                           |
| 1          | MCKI/XTI pin                   |

(default)

Table 44. SRC Clock Mode Setting

| SRCCKS bit | SRC Clock Mode |
|------------|----------------|
| 0          | PLLO           |
| 1          | MCKI/XTI pin   |

(default)

Note 114. SRCCKS bit and XCKSEL bit must be same value at SRC Bypass Mode (SELDAIN bit = "0").

**< Jitter Cleaner Function >**

The sound quality and characteristics may degrade if a clock with large jitter is input to the DAC from the host processor. The AK4331 maximizes DAC performance and the sound quality by the internal SRC with an external low jitter crystal oscillator. When the AK4331 is operated by a clock from the external crystal oscillator, the master clock is set by CM2[1:0] bits and the sampling frequency is set by FS2[4:0] bits.

**9-16. SRC Selector Function**

The DAC input data can be selected between the input data of the SDTI pin and the SRC output data by SELDAIN bit. SELDAIN bit must be set at PMSRC bit = “0”.

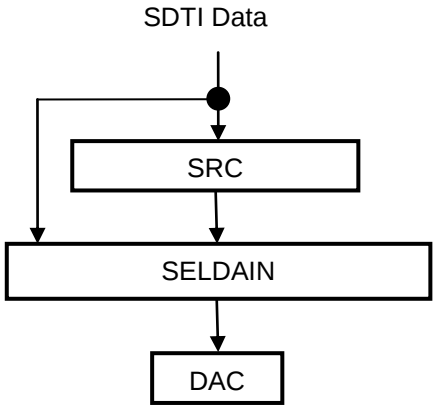


Figure 27. Input Selector for DAC

Table 45. DAC Data Path Setting

| SELDAIN bit | DAC             | (default) |
|-------------|-----------------|-----------|
| 0           | SRC Bypass Mode |           |
| 1           | SRC Mode        |           |

### 9-17. SRC Clock Change Sequence

When changing the system clock of SRC, the SRC should be reset by setting PMSRC bit to "0". The SRC output is "0" while PMSRC bit = "0". A data output becomes available within 20 msec from setting PMSRC bit to "1" (up to  $156/f_{so}$ , when the input clock is stabilized) after changing the system clock. Until then the SRC outputs "0". Set PMTIM bit to "1" and SRC settings should be finished before setting PMSRC bit to "1".

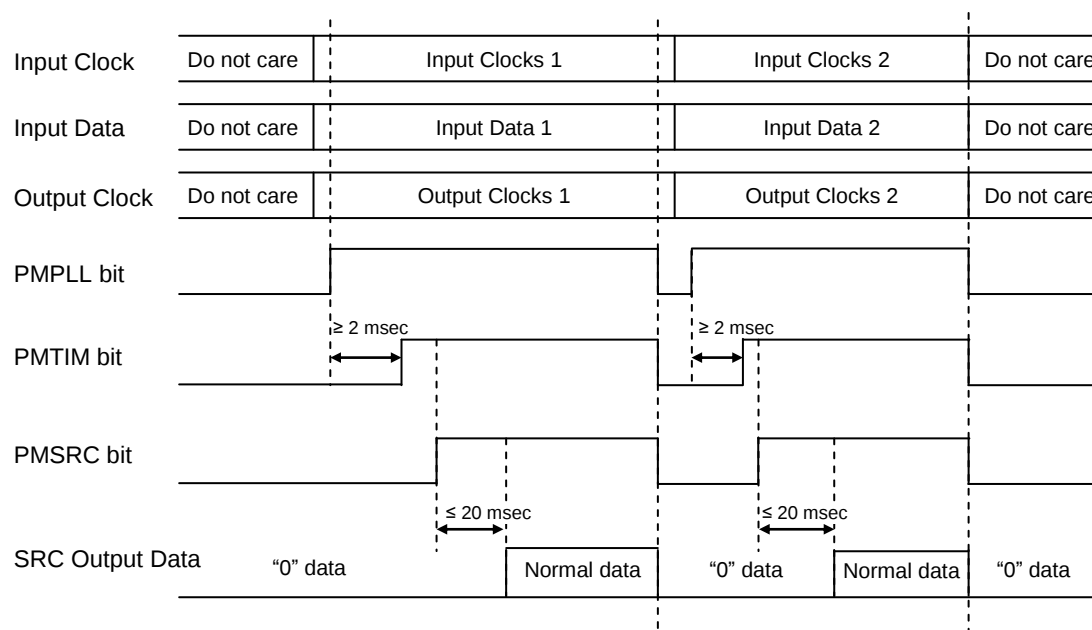


Figure 28. Sequence of Changing SRC System Clock

## 9-18. Soft Mute

AK4331 has a soft mute operation block. PMSM bit and SELSM bit must be set to “1” when using a soft mute block.

Table 46. Soft Mute Block Power Management (N/A: Not available)

| PMSM bit | SELSM bit | Soft Mute Block |           |
|----------|-----------|-----------------|-----------|
| 0        | 0         | Power-Down      | (default) |
| 1        | 1         | Power-Up        |           |
| Others   |           | N/A             |           |

### 1. Manual Mode

When SMUTE bit is changed to “1”, the output signal is attenuated to  $-\infty$  (“0”) in 1024/FSO cycle (SMT[1:0] bits = “00”). When the SMUTE bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to 0 dB in 1024/FSO cycle. If the soft mute is cancelled within 1024/FSO, the attenuation is discontinued and the attenuation level returns to 0 dB by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

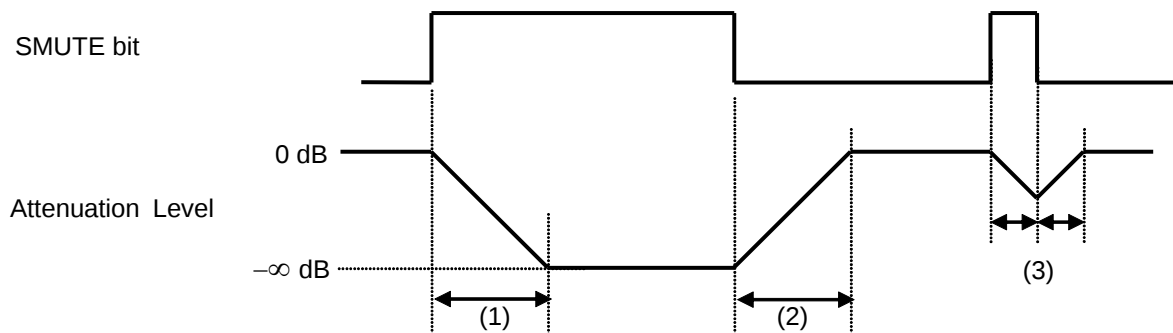


Figure 29. Soft Mute Manual Mode

- (1) SMUTE bit = “0” → “1”: The output signal is attenuated to  $-\infty$  (“0”) in 1024/FSO cycle (SMT[1:0] bits = “00”)
- (2) SMUTE bit = “1” → “0”: The attenuation level of the output signal returns to 0 dB from  $-\infty$  (“0”) in 1024/FSO cycle (SMT[1:0] bits = “00”)
- (3) If the soft mute is cancelled within 1024/FSO, the attenuation is discontinued and the attenuation level returns to 0 dB by the same cycle.

Table 47. Soft Mute Cycle Setting

| SMT1 bit | SMT0 bit | Period   | FSO = 48 kHz | FSO = 96 kHz | FSO = 192 kHz |           |
|----------|----------|----------|--------------|--------------|---------------|-----------|
| 0        | 0        | 1024/FSO | 21.3 msec    | 10.7 msec    | 5.3 msec      | (default) |
| 0        | 1        | 2048/FSO | 42.7 msec    | 21.3 msec    | 10.7 msec     |           |
| 1        | 0        | 4096/FSO | 85.3 msec    | 42.7 msec    | 21.3 msec     |           |
| 1        | 1        | 8192/FSO | 170.7 msec   | 85.3 msec    | 42.7 msec     |           |

## 2. Semi-Auto Mode

The AK4331 enters Semi-Auto mode by setting SAUTO bit to "1". In this mode, the soft mute is cancelled automatically in  $160/f_{so}$  after setting PMSM bit and SELSM bit to "1" and the AK4331 will be able to output the data. When power-down state is released (PMSM bit = SELSM bit = "0" → "1"), the soft mute function is ON if the SMUTE bit is "1".

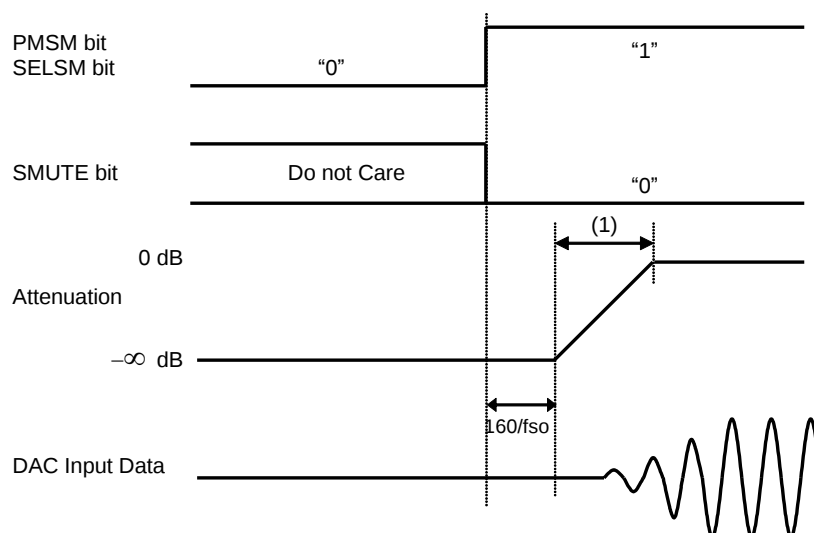


Figure 30. Soft Mute Semi-Auto Mode (SRC Bypass Mode)

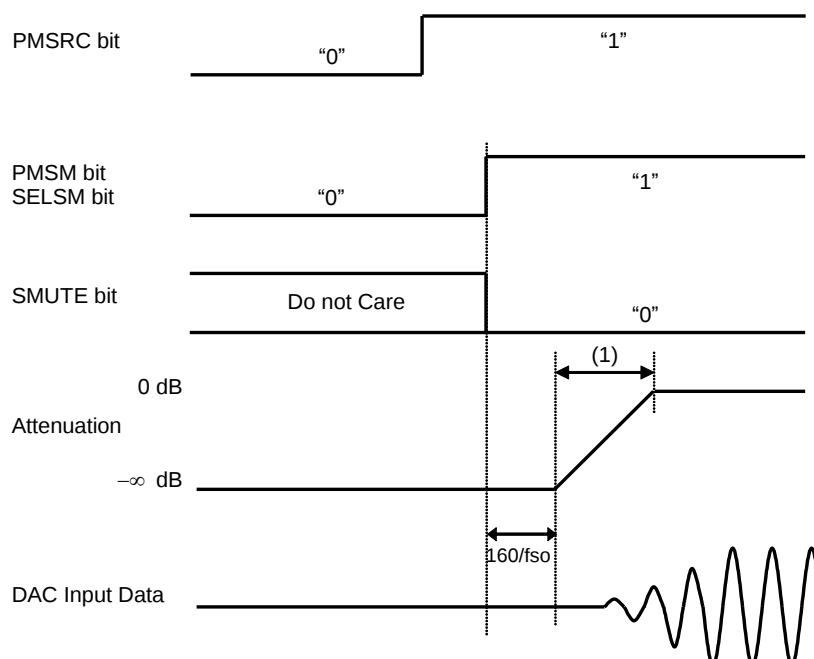


Figure 31. Soft Mute Semi-Auto Mode (SRC Mode)

(1) The attenuation level is returns to 0 dB in  $1024/f_{so}$  cycle (SMT[1:0] bits = "00").

## 9-19. Serial Audio Interface

The serial audio interface format is set by DIF bit and its data length is controlled by DL[1:0] bits. In case that the input data length is less than the value which set by DL[1:0] bits, unused lower bits are filled with "0". When using master mode, DL[1:0] bits is set in accordance with the setting of BCKO bit. DIF bit and DL[1:0] bits must be set at PMTIM bit = "0".

Table 48. Digital Audio Interface Format Setting

| DIF bit | Digital Interface Format    |           |
|---------|-----------------------------|-----------|
| 0       | I <sup>2</sup> S Compatible | (default) |
| 1       | MSB justified               |           |

Table 49. Data Length Setting (x: Do not Care, N/A: Not available)

| DL1 bit | DL0 bit | Data Length   | BCLK Frequency |                          |           |
|---------|---------|---------------|----------------|--------------------------|-----------|
|         |         |               | Slave Mode     | Master Mode              |           |
| 0       | 0       | 24-bit linear | ≥ 48fs         | N/A                      | (default) |
| 0       | 1       | 16-bit linear | ≥ 32fs         | 32fs<br>(BCKO bit = "1") |           |
| 1       | x       | 32-bit linear | ≥ 64fs         | 64fs<br>(BCKO bit = "0") |           |

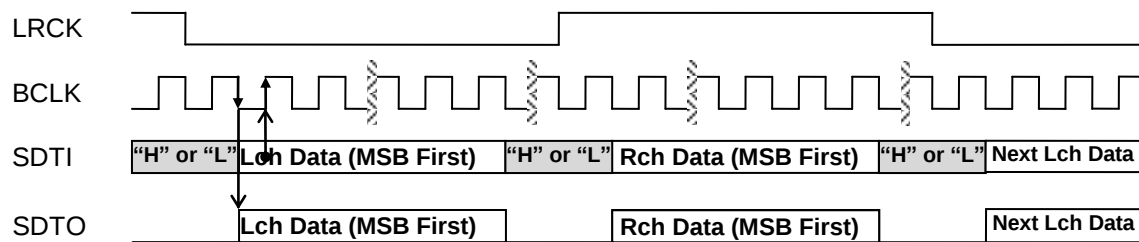


Figure 32. I<sup>2</sup>S Compatible Format (DIF bit = "0")

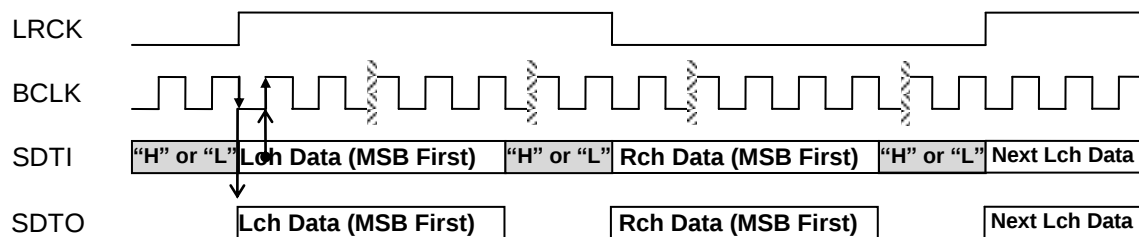


Figure 33. MSB justified format (DIF bit= "1")

## 9-20. Serial Control Interface (I<sup>2</sup>C-bus)

The AK4331 supports the fast-mode I<sup>2</sup>C-bus (Max: 400 kHz). Pull-up resistors at the SDA and SCL pins must be connected to (TVDD + 0.3) V or less voltage.

### 1. WRITE Operation

Figure 34 shows the data transfer sequence for the I<sup>2</sup>C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 40). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as “0010000”. If the slave address matches that of the AK4331, the AK4331 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 41). A R/W bit value of “1” indicates that the read operation is to be executed, and “0” indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4331. The format is MSB first 8 bits (Figure 36). The data after the second byte contains control data. The format is MSB first, 8 bits (Figure 37). The AK4331 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 40).

The AK4331 can perform more than one byte write operation per sequence at address from 00H to 17H. After receipt of the third byte the AK4331 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 17H prior to generating a stop condition, the address counter will “roll over” to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 42) except for the START and STOP conditions.

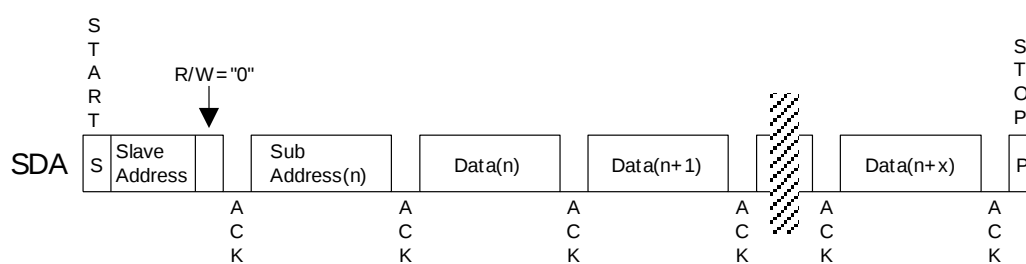


Figure 34. Data Transfer Sequence in I<sup>2</sup>C-bus Mode

|   |   |   |   |   |   |   |     |
|---|---|---|---|---|---|---|-----|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | R/W |
|---|---|---|---|---|---|---|-----|

Figure 35. The First Byte

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|----|----|----|----|----|----|----|----|

Figure 36. The Second Byte

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|

Figure 37. The Third Byte

## 2. READ Operation

Set the R/W bit = “1” for the READ operation of the AK4331. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 17H prior to generating stop condition, the address counter will “roll over” to 00H and the data of 00H will be read out.

The AK4331 supports two basic read operations: Current Address READ and Random Address READ.

### 2-1. Current Address READ

The AK4331 has an internal address counter that maintains the address of the last accessed word incremented by one. Therefore, if the last access (either a read or write) were to address “n”, the next Current READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK4331 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4331 ceases the transmission.

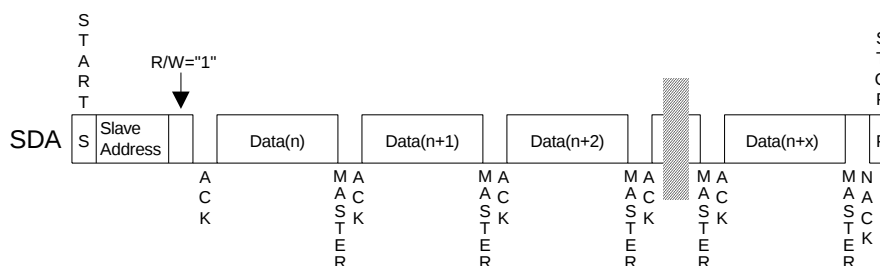


Figure 38. Current Address READ

## 2-2. Random Address READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4331 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge but generates a stop condition instead, the AK4331 ceases the transmission.

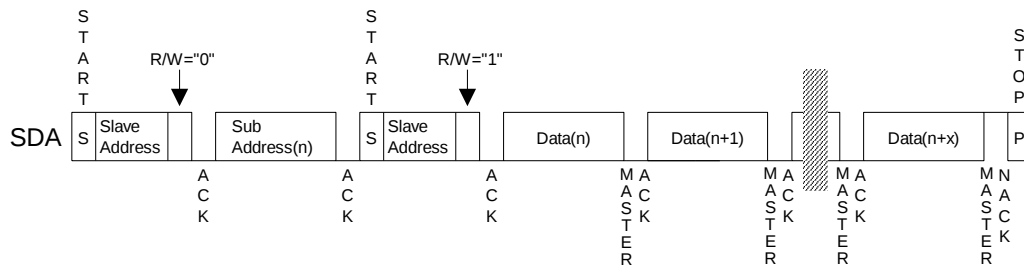


Figure 39. Random Address READ

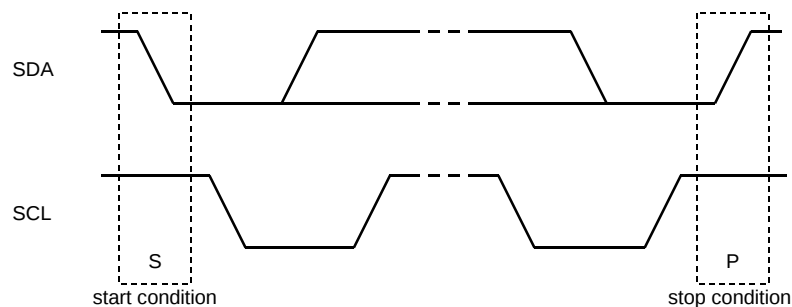


Figure 40. Start Condition and Stop Condition

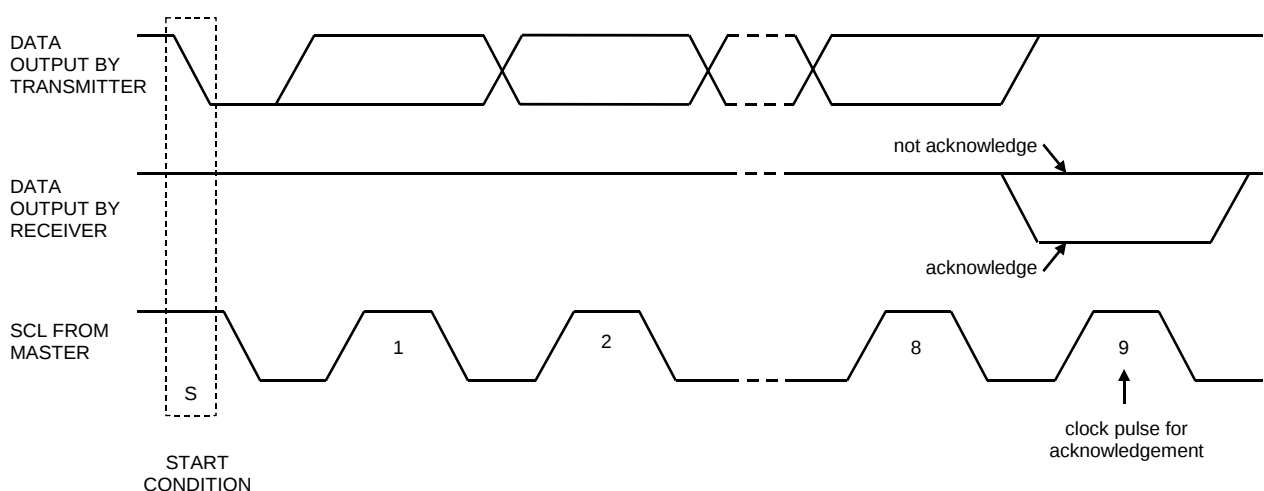
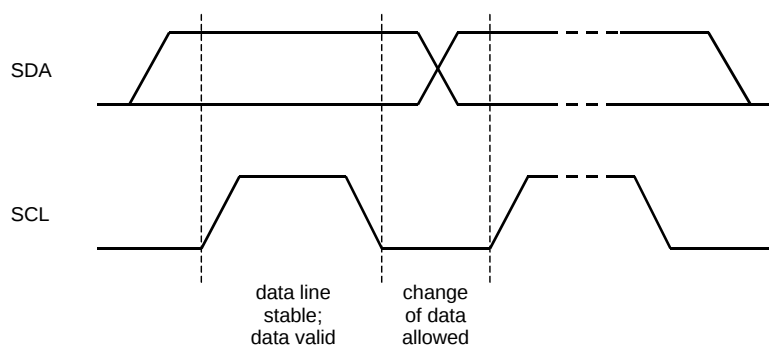


Figure 41. Acknowledge (I<sup>2</sup>C-bus)

Figure 42. Bit Transfer (I<sup>2</sup>C-bus)

## 9-21. Control Sequence

Figure 43 shows power-up sequence of DAC and headphone amplifier.

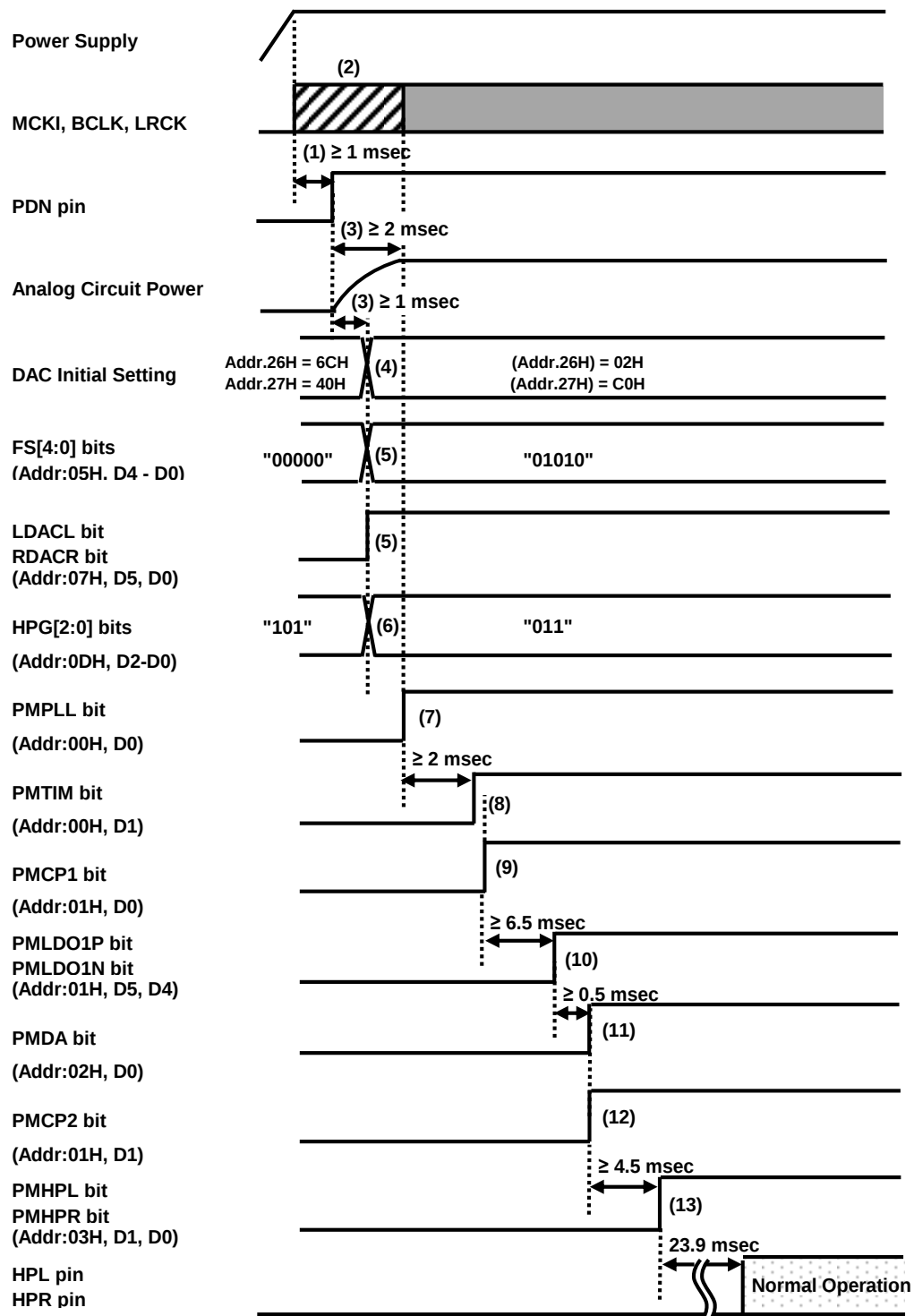


Figure 43. Power-Up Sequence Example of DAC and Headphone Amplifier

## &lt; Power-Up Sequence Example &gt;

- (1) Set the PDN pin from “L” to “H” after turning on all power supplies. In this case, 1 msec or more “L” time is needed for a certain reset.
- (2) After all power supplies are On, MCKI, BCLK and LRCK should be input before powering up PLL or CP1.
- (3) Set the PDN pin = “H” to release the power-down. Register access will be valid in 1 msec at maximum. However, a wait time of 2 msec is needed to access PMTIM bit and power management bits of the analog circuit (PMCP1 bit, PMCP2 bit, PMLDO1P bit, PMLDO1N bit, PMDA bit, PMHPL bit, PMHPR bit and PMPLL bit) until the analog circuit is powered up.
- (4) Set DAC initial settings. (Write 02H data into Address 26H and write C0H data into Address 27H)
- (5) Set sampling frequency (FS[4:0] bits) and the input signal path of the DAC.  
(LDACL bit = RDACR bit = “0” → “1”)
- (6) Set headphone amplifier volume by HPG[2:0] bits.
- (7) In case of using PLL, power-up PLL (PMPLL bit = “0” → “1”) and wait 2 msec for PLL output stabilization.
- (8) Start internal master counter. (PMTIM bit = “0” → “1”)  
PMCP1 bit, PMCP2 bit, PMLDO1P bit, PMLDO1N bit, PMDA bit, PMHPL bit and PMHPR bit must be powered up after PMTIM bit = “1”.
- (9) Power-up CP1 (PMCP1 bit = “0” → “1”) and wait 6.5 msec ([Note 115](#)) for CP1 output voltage stabilization.
- (10) Power-up LDO1P and LDO1N (PMLDO1P bit = PMLDO1N bit = “0” → “1”) and wait 0.5 msec ([Note 115](#)) for each LDO output voltage stabilization.
- (11) Power-up DAC (PMDA bit = “0” → “1”)
- (12) Power-up CP2 (PMCP2 bit = “0” → “1”) and wait 4.5 msec ([Note 115](#)) for CP2 output voltage stabilization.
- (13) Power-up headphone amplifier (PMHPL bit = PMHPR bit = “0” → “1”)  
The power-up time of headphone amplifier is 23.9 msec (@ fs = 48 kHz). The HPL pin and the HPR pin output 0 V until the headphone amplifier is powered up.

Note 115. Refer to “8-3. Charge Pump & LDO Circuit Power-Up Time”

Figure 44 shows power-down sequence of headphone amplifier and DAC.

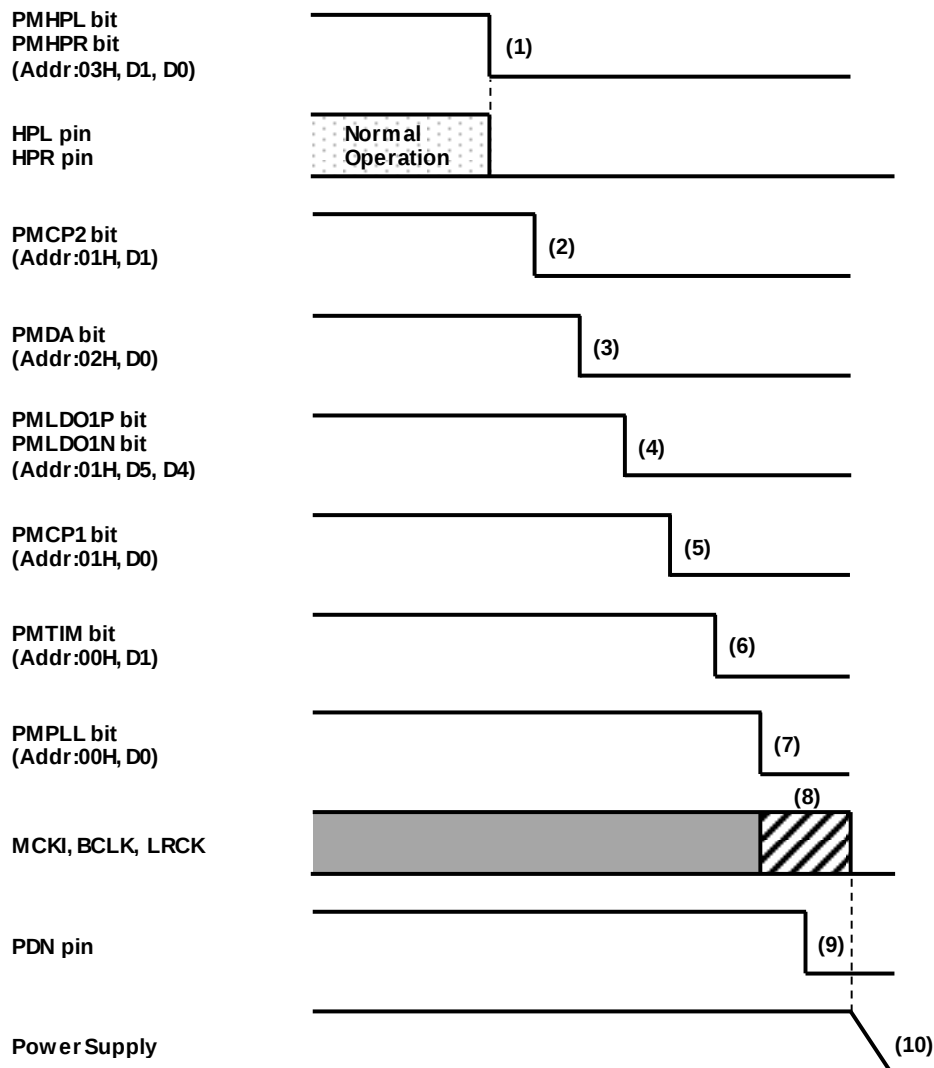


Figure 44. Power-Down Sequence Example of Headphone Amplifier and DAC

#### < Power-Down Sequence Example >

- (1) Power-down headphone amplifier (PMHPL bit = PMHPR bit = "1" → "0").  
When the headphone amplifier is powered down, the HPL pin and the HPR pin are pulled down to HPGND via the internal pull-down register.
- (2) Power-down CP2 (PMCP2 bit = "1" → "0").
- (3) Power-down DAC (PMDA bit = "1" → "0").
- (4) Power-down LDO1P, LDO1N (PMLDO1P bit = PMLDO1N bit = "1" → "0").
- (5) Power-down CP1 (PMCP1 bit = "1" → "0").
- (6) Stop internal master counter. (PMTIM bit = "1" → "0")  
PMCP1 bit, PMCP2 bit, PMLDO1P bit, PMLDO1N bit, PMDA bit, PMHPL bit and PMHPR bit must be powered off before PMTIM bit = "0".
- (7) In case of using PLL, power-down PLL. (PMPLL bit = "1" → "0")
- (8) Stop MCKI, BCLK and LRCK supply before turning off each of power supplies.
- (9) Set the PDN pin from "H" to "L".
- (10) Turn off each of power supplies.

## 9-22. Register Map

| Addr | Register Name            | D7            | D6         | D5         | D4       | D3          | D2        | D1         | D0     |
|------|--------------------------|---------------|------------|------------|----------|-------------|-----------|------------|--------|
| 00H  | Power Management 1       | 0             | 0          | 0          | PMOSC    | 0           | 0         | PMTIM      | PMPLL  |
| 01H  | Power Management 2       | 0             | 0          | PMLDO1N    | PMLDO1P  | 0           | 0         | PMCP2      | PMCP1  |
| 02H  | Power Management 3       | PMSRC         | 0          | PMSM       | SELSM    | 0           | 0         | 0          | PMDA   |
| 03H  | Power Management 4       | 0             | LVDTM[2:0] |            |          | CPMODE[1:0] |           | PMHPR      | PMHP1  |
| 04H  | Output Mode Setting      | LVDSEL[1:0]   |            | VDDTM[3:0] |          |             |           | HPRHZ      | HPLHZ  |
| 05H  | Clock Mode Select        | 0             | CM[1:0]    |            | FS[4:0]  |             |           |            |        |
| 06H  | Digital Filter Select    | DASD          | DASL       | DADFSEL    | 0        | 0           | 0         | 0          | 0      |
| 07H  | DAC Mono Mixing          | INVR          | MDACR      | RDACR      | LDACR    | INVL        | MDACL     | RDACL      | LDACL  |
| 08H  | SRC Clock Select         | 0             | CM2[1:0]   |            | FS2[4:0] |             |           |            |        |
| 09H  | Soft Mute Setting        | 0             | 0          | 0          | 0        | SMT[1:0]    |           | SAUTO      | SMUTE  |
| 0AH  | SRC Setting              | 0             | XCKSEL     | 0          | 0        | 0           | 0         | SELDIN     | 0      |
| 0BH  | Lch Output Volume        | OVOLCN        | 0          | 0          | OVL[4:0] |             |           |            |        |
| 0CH  | Rch Output Volume        | 0             | 0          | 0          | OVR[4:0] |             |           |            |        |
| 0DH  | HP Volume Control        | HPTM[2:0]     |            |            | 1        | 0           | HPG[2:0]  |            |        |
| 0EH  | PLL CLK Source Select    | 0             | 0          | 0          | PLLMD    | 0           | 0         | 0          | PLS    |
| 0FH  | PLL Ref CLK Divider 1    | PLD[15:8]     |            |            |          |             |           |            |        |
| 10H  | PLL Ref CLK Divider 2    | PLD[7:0]      |            |            |          |             |           |            |        |
| 11H  | PLL FB CLK Divider 1     | PLM[15:8]     |            |            |          |             |           |            |        |
| 12H  | PLL FB CLK Divider 2     | PLM[7:0]      |            |            |          |             |           |            |        |
| 13H  | SRC CLK Source Select    | 0             | 0          | 0          | 0        | 0           | 0         | 0          | SRCKS  |
| 14H  | PLLCLK Divider           | 0             | 0          | 0          | 0        | MDIV[3:0]   |           |            |        |
| 15H  | Audio Interface Format   | DEVICEID[2:0] |            |            | MS       | BCKO        | DIF       | DL[1:0]    |        |
| 16H  | Digital MIC              | PMDMR         | PMDML      | DCLKE      | DCLKP    | 0           | 0         | ADRST[1:0] |        |
| 17H  | Side Tone Volume Control | SV[2:0]       |            |            | SVE      | 0           | HPFC[1:0] |            | HPFADN |
| 26H  | DAC Adjustment 1         | T8            | T7         | T6         | T5       | T4          | T3        | T2         | T1     |
| 27H  | DAC Adjustment 2         | T16           | T15        | T14        | T13      | T12         | T11       | T10        | T9     |
| 29H  | Mode Control             | 0             | 0          | 0          | 0        | 0           | 0         | HPMD[1:0]  |        |

Note 116. PDN pin = "L" resets the registers to their default values.

Note 117. The bits defined as "0" must contain a "0" value.

Note 118. The bits defined as "1" must contain a "1" value.

Note 119. Writing access to 18H to 25H, 28H, 2AH to FFH is prohibited.

**9-23. Register Definitions**

| Addr | Register Name      | D7  | D6  | D5  | D4    | D3  | D2  | D1    | D0    |
|------|--------------------|-----|-----|-----|-------|-----|-----|-------|-------|
| 00H  | Power Management 1 | 0   | 0   | 0   | PMOSC | 0   | 0   | PMTIM | PMPLL |
|      | R/W                | R/W | R/W | R/W | R/W   | R/W | R/W | R/W   | R/W   |
|      | Default            | 0   | 0   | 0   | 0     | 0   | 0   | 0     | 0     |

PMPLL: PLL Power Management

0: Power-Down (default)

1: Power-Up

PMTIM: Synchronization Control Power Management

0: Disable (default)

1: Enable

PMOSC: Crystal Oscillator Power Management

0: Power-Down (default)

1: Power-Up

| Addr | Register Name      | D7  | D6  | D5      | D4      | D3  | D2  | D1    | D0    |
|------|--------------------|-----|-----|---------|---------|-----|-----|-------|-------|
| 01H  | Power Management 2 | 0   | 0   | PMLDO1N | PMLDO1P | 0   | 0   | PMCP2 | PMCP1 |
|      | R/W                | R/W | R/W | R/W     | R/W     | R/W | R/W | R/W   | R/W   |
|      | Default            | 0   | 0   | 0       | 0       | 0   | 0   | 0     | 0     |

PMCP1: Charge Pump 1 Power Management

0: Power-Down (default)

1: Power-Up

PMCP2: Charge Pump 2 Power Management

0: Power-Down (default)

1: Power-Up

PMLDO1P: LDO1P Power Management

0: Power-Down (default)

1: Power-Up

PMLDO1N: LDO1N Power Management

0: Power-Down (default)

1: Power-Up

| Addr | Register Name      | D7    | D6  | D5   | D4    | D3  | D2  | D1  | D0   |
|------|--------------------|-------|-----|------|-------|-----|-----|-----|------|
| 02H  | Power Management 3 | PMSRC | 0   | PMSM | SELSM | 0   | 0   | 0   | PMDA |
|      | R/W                | R/W   | R/W | R/W  | R/W   | R/W | R/W | R/W | R/W  |
|      | Default            | 0     | 0   | 0    | 0     | 0   | 0   | 0   | 0    |

PMDA: DAC Power Management

0: Power-Down (default)

1: Power-Up

PMSM, SELSM: Soft Mute Power Management ([Table 46](#))

“0, 0”: Power-Down (default)

“1, 1”: Power-Up

PMSRC: SRC Power Management

0: Power-Down (default)

1: Power-Up

| Addr | Register Name      | D7  | D6         | D5 | D4 | D3          | D2 | D1    | D0    |
|------|--------------------|-----|------------|----|----|-------------|----|-------|-------|
| 03H  | Power Management 4 | 0   | LVDTM[2:0] |    |    | CPMODE[1:0] |    | PMHPR | PMHPL |
|      | R/W                | R/W | R/W        |    |    | R/W         |    | R/W   | R/W   |
|      | Default            | 0   | 000        |    |    | 00          |    | 0     | 0     |

PMHPL/R: Headphone Amplifier L/R Channel Power Management

0: Power-Down (default)

1: Power-Up

CPMODE[1:0]: Charge Pump Mode Control ([Table 32](#))

Default: “00” (Automatic Switching Mode)

LVDTM[2:0]: Class-G 1/2VDD Mode Detection Time Setting ([Table 34](#))

Default: “000” (64/fs)

| Addr | Register Name       | D7           | D6 | D5         | D4 | D3 | D2 | D1    | D0    |
|------|---------------------|--------------|----|------------|----|----|----|-------|-------|
| 04H  | Output Mode Setting | LVDSSEL[1:0] |    | VDDTM[3:0] |    |    |    | HPRHZ | HPLHZ |
|      | R/W                 | R/W          |    | R/W        |    |    |    | R/W   | R/W   |
|      | Default             | 00           |    | 0000       |    |    |    | 0     | 0     |

HPRHZ/HPLHZ: GND Switch Setting for Headphone Amplifier Output

0: Pull-Down by 4Ω (Typ.) (default)

1: Pull-Down by 95 kΩ (Typ.)

VDDTM[3:0]: Class-G VDD Hold Time Setting ([Table 33](#))

Default: "0000" (1024/fs)

LVDSSEL[1:0]: Switching Threshold between VDD Mode and 1/2VDD Mode of CP2

00: VDD → 1/2VDD: < 1.05 mW at both channels (@CVDD = 1.8 V, R<sub>L</sub> = 16Ω)

1/2VDD → VDD: ≥ 1.05 mW at either channel (@CVDD = 1.8 V, R<sub>L</sub> = 16Ω)

(Default: Assuming when connecting a 16Ω Headphone)

01: VDD → 1/2VDD: < 1.05 mW at both channels (@CVDD = 1.8 V, R<sub>L</sub> = 32Ω)

1/2VDD → VDD: ≥ 1.05 mW at either channel (@CVDD = 1.8 V, R<sub>L</sub> = 32Ω)

(Assuming when connecting a 32Ω Headphone or more)

10: VDD → 1/2VDD: < 1.05 mW at both channels (@CVDD = 1.8 V, R<sub>L</sub> = 11Ω)

1/2VDD → VDD: ≥ 1.05 mW at either channel (@CVDD = 1.8 V, R<sub>L</sub> = 11Ω)

(Assuming when connecting a 11Ω Headphone)

11: VDD → 1/2VDD: < 1.05 mW at both channels (@CVDD = 1.8 V, R<sub>L</sub> = 8Ω)

1/2VDD → VDD: ≥ 1.05 mW at either channel (@CVDD = 1.8 V, R<sub>L</sub> = 8Ω)

(Assuming when connecting a 8Ω Headphone)

| Addr | Register Name     | D7  | D6      | D5 | D4      | D3 | D2 | D1 | D0 |
|------|-------------------|-----|---------|----|---------|----|----|----|----|
| 05H  | Clock Mode Select | 0   | CM[1:0] |    | FS[4:0] |    |    |    |    |
|      | R/W               | R/W | R/W     |    | R/W     |    |    |    |    |
|      | Default           | 0   | 00      |    | 00000   |    |    |    |    |

FS[4:0]: Sampling Frequency Setting ([Table 6](#) @SRC Bypass Mode, [Table 8](#) @SRC Mode)

Default: "00000" (fs = 8 kHz)

CM[1:0]: Master Clock Frequency Setting ([Table 5](#) @SRC Bypass Mode, [Table 7](#) @SRC Mode)

Default: "00" (256fs)

| Addr | Register Name         | D7   | D6   | D5      | D4  | D3  | D2  | D1  | D0  |
|------|-----------------------|------|------|---------|-----|-----|-----|-----|-----|
| 06H  | Digital Filter Select | DASD | DASL | DADFSEL | 0   | 0   | 0   | 0   | 0   |
|      | R/W                   | R/W  | R/W  | R/W     | R/W | R/W | R/W | R/W | R/W |
|      | Default               | 0    | 0    | 0       | 0   | 0   | 0   | 0   | 0   |

DADFSEL: Digital Filter Setting for DAC Compensation ([Table 27](#), [Table 28](#))

0: In case of SRC Bypass Mode (default)

1: In case of SRC Mode

DASD, DASL: DAC Digital Filter Mode Setting ([Table 27](#), [Table 28](#))

Default: "0, 0" (Sharp Roll-Off Filter)

| Addr | Register Name   | D7   | D6    | D5    | D4    | D3   | D2    | D1    | D0    |
|------|-----------------|------|-------|-------|-------|------|-------|-------|-------|
| 07H  | DAC Mono Mixing | INVR | MDACR | RDACR | LDACR | INVL | MDACL | RDACL | LDACL |
|      | R/W             | R/W  | R/W   | R/W   | R/W   | R/W  | R/W   | R/W   | R/W   |
|      | Default         | 0    | 0     | 0     | 0     | 0    | 0     | 0     | 0     |

MDACL, RDACL, LDACL: DAC L Channel Input Signal Select ([Table 29](#))

Default: "0, 0, 0" (MUTE)

MDACR, RDACR, LDACR: DAC R Channel Input Signal Select ([Table 29](#))

Default: "0, 0, 0" (MUTE)

INVL/R: DAC Input Signal Polarity Select

0: Normal (default)

1: Inverting

| Addr | Register Name    | D7  | D6       | D5 | D4       | D3 | D2 | D1 | D0 |
|------|------------------|-----|----------|----|----------|----|----|----|----|
| 08H  | SRC Clock Select | 0   | CM2[1:0] |    | FS2[4:0] |    |    |    |    |
|      | R/W              | R/W | R/W      |    | R/W      |    |    |    |    |
|      | Default          | 0   | 00       |    | 00000    |    |    |    |    |

FS2[4:0]: Sampling Frequency Setting for SRC Output ([Table 10](#))

Default: "00000" (fs = 8 kHz)

CM2[1:0]: Master Clock Frequency Setting for SRC Output ([Table 9](#))

Default: "00" (256fs)

| Addr | Register Name     | D7  | D6  | D5  | D4  | D3       | D2 | D1    | D0    |
|------|-------------------|-----|-----|-----|-----|----------|----|-------|-------|
| 09H  | Soft Mute Setting | 0   | 0   | 0   | 0   | SMT[1:0] |    | SAUTO | SMUTE |
|      | R/W               | R/W | R/W | R/W | R/W | R/W      |    | R/W   | R/W   |
|      | Default           | 0   | 0   | 0   | 0   | 00       |    | 0     | 0     |

SMUTE: Soft Mute Enable

0: Disable (default)

1: Enable

SAUTO: Semi-Auto Mode Enable

0: Disable (default)

1: Enable

SMT[1:0]: Soft Mute Cycle Setting ([Table 47](#))

Default: "00", 1024/FSO

| Addr | Register Name | D7  | D6     | D5  | D4  | D3  | D2  | D1      | D0  |
|------|---------------|-----|--------|-----|-----|-----|-----|---------|-----|
| 0AH  | SRC Setting   | 0   | XCKSEL | 0   | 0   | 0   | 0   | SELDAIN | 0   |
|      | R/W           | R/W | R/W    | R/W | R/W | R/W | R/W | R/W     | R/W |
|      | Default       | 0   | 0      | 0   | 0   | 0   | 0   | 0       | 0   |

SELDAIN: DAC Input Data Select ([Table 45](#))

Default: "0" (SDTI pin; SRC Bypass Mode)

XCKSEL: DAC and Charge Pump Operation Clock ([Table 43](#))

0: PLL0 (default)

1: MCKI/XTI pin

| Addr | Register Name     | D7     | D6  | D5  | D4       | D3 | D2 | D1 | D0 |
|------|-------------------|--------|-----|-----|----------|----|----|----|----|
| 0BH  | Lch Output Volume | OVOLCN | 0   | 0   | OVL[4:0] |    |    |    |    |
| 0CH  | Rch Output Volume | 0      | 0   | 0   | OVR[4:0] |    |    |    |    |
|      | R/W               | R/W    | R/W | R/W | R/W      |    |    |    |    |
|      | Default           | 0      | 0   | 0   | 19H      |    |    |    |    |

OVL[4:0]: DAC L Channel Digital Volume Control; +3 dB to –12 dB & Mute, 0.5 dB step ([Table 31](#))

OVR[4:0]: DAC R Channel Digital Volume Control; +3 dB to –12 dB & Mute, 0.5 dB step ([Table 31](#))

Default: 19H (0 dB)

OVOLCN: Digital Volume Control

0: Dependent (default)

1: Independent

OVL[4:0] bits control digital volume of both L and R channels when OVOLCN bit = "0". In this case, the value of OVL[4:0] bits will not be written to OVR[4:0] bits.

| Addr | Register Name     | D7        | D6 | D5 | D4  | D3  | D2       | D1 | D0 |
|------|-------------------|-----------|----|----|-----|-----|----------|----|----|
| 0DH  | HP Volume Control | HPTM[2:0] |    |    | 1   | 0   | HPG[2:0] |    |    |
|      | R/W               | R/W       |    |    | R/W | R/W | R/W      |    |    |
|      | Default           | 011       |    |    | 1   | 0   | 101      |    |    |

HPG[2:0]: Headphone Amplifier Analog Volume Control; +4 dB to –10 dB, 2 dB step ([Table 35](#))

Default: "101" (0 dB)

HPTM[2:0]: Zero Cross Time Output Period Setting for Analog Volume of Headphone Amplifier ([Table 36](#))

Default: "011" (1024/fs)

| Addr | Register Name         | D7  | D6  | D5  | D4    | D3  | D2  | D1  | D0  |
|------|-----------------------|-----|-----|-----|-------|-----|-----|-----|-----|
| 0EH  | PLL CLK Source Select | 0   | 0   | 0   | PLLMD | 0   | 0   | 0   | PLS |
|      | R/W                   | R/W | R/W | R/W | R/W   | R/W | R/W | R/W | R/W |
|      | Default               | 0   | 0   | 0   | 0     | 0   | 0   | 0   | 0   |

PLS: PLL Clock Source Select ([Table 14](#))

Default: "0" (MCKI/XTI pin)

PLLMD: PLL Internal Mode Setting ([Table 17](#))

Default: "0"

| Addr | Register Name         | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------------|-----------|----|----|----|----|----|----|----|
| 0FH  | PLL Ref CLK Divider 1 | PLD[15:8] |    |    |    |    |    |    |    |
| 10H  | PLL Ref CLK Divider 2 | PLD[7:0]  |    |    |    |    |    |    |    |
|      | R/W                   | R/W       |    |    |    |    |    |    |    |
|      | Default               | 0000H     |    |    |    |    |    |    |    |

PLD[15:0]: PLL Reference Clock Divider Setting ([Table 15](#))  
Default: 0000H

| Addr | Register Name        | D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------------|-----------|----|----|----|----|----|----|----|
| 11H  | PLL FB CLK Divider 1 | PLM[15:8] |    |    |    |    |    |    |    |
| 12H  | PLL FB CLK Divider 2 | PLM[7:0]  |    |    |    |    |    |    |    |
|      | R/W                  | R/W       |    |    |    |    |    |    |    |
|      | Default              | 0000H     |    |    |    |    |    |    |    |

PLM[15:0]: PLL Feedback Clock Divider Setting ([Table 16](#))  
Default: 0000H

| Addr | Register Name         | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0     |
|------|-----------------------|-----|-----|-----|-----|-----|-----|-----|--------|
| 13H  | SRC CLK Source Select | 0   | 0   | 0   | 0   | 0   | 0   | 0   | SRCKKS |
|      | R/W                   | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W    |
|      | Default               | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0      |

SRCKKS: SRC Clock Source Select ([Table 44](#))  
0: PLLO (default)  
1: MCKI/XTI pin

| Addr | Register Name  | D7  | D6  | D5  | D4  | D3        | D2 | D1 | D0 |
|------|----------------|-----|-----|-----|-----|-----------|----|----|----|
| 14H  | PLLCLK Divider | 0   | 0   | 0   | 0   | MDIV[3:0] |    |    |    |
|      | R/W            | R/W | R/W | R/W | R/W | R/W       |    |    |    |
|      | Default        | 0   | 0   | 0   | 0   | 0H        |    |    |    |

MDIV[3:0]: PLLCLK Divider Setting ([Table 18](#))  
Default: 0H (Divided by 1)

| Addr | Register Name          | D7            | D6 | D5 | D4  | D3   | D2  | D1      | D0 |
|------|------------------------|---------------|----|----|-----|------|-----|---------|----|
| 15H  | Audio Interface Format | DEVICEID[2:0] |    |    | MS  | BCKO | DIF | DL[1:0] |    |
|      | R/W                    | R             |    |    | R/W | R/W  | R/W | R/W     |    |
|      | Default                | 111           |    |    | 0   | 0    | 0   | 00      |    |

DL[1:0]: Data Length Setting ([Table 49](#))

Default: "00" (24-bit linear)

DIF: Digital Audio Interface Format Setting ([Table 48](#))

0: I<sup>2</sup>S Compatible (default)

1: MSB justified

BCKO: BCLK Output Frequency

0: 64fs (Default)

1: 32fs

MS: Master/Slave Mode Setting ([Table 3](#))

0: Slave Mode (default)

1: Master Mode

DEVICEID[2:0]: Device ID

Default: "111" (AK4375: "000", AK4375A: "001", AK4376/A: "010", AK4377: "011", AK4331: "111")

| Addr | Register Name | D7    | D6    | D5    | D4    | D3  | D2  | D1         | D0 |
|------|---------------|-------|-------|-------|-------|-----|-----|------------|----|
| 16H  | Digital MIC   | PMDMR | PMDML | DCLKE | DCLKP | 0   | 0   | ADRST[1:0] |    |
|      | R/W           | R/W   | R/W   | R/W   | R/W   | R/W | R/W | R/W        |    |
|      | Default       | 0     | 0     | 0     | 0     | 0   | 0   | 00         |    |

ADRST[1:0]: Digital Microphone Initialization Cycle Setting ([Table 24](#))

Default: "00" (1059/fs)

DCLKP: Data Latching Edge Select ([Table 21](#))

0: L channel data is latched on the DMCLK rising edge ("↑"). (default)

1: L channel data is latched on the DMCLK falling edge ("↓").

DCLKE: DMCLK pin Output Clock Control

0: "L" Output (default)

1: 64fs Output

PMDML/R: Input Signal Select with Digital Microphone Power Management ([Table 23](#))

0: Power-Down (default)

1: Power-Up

| Addr | Register Name            | D7      | D6 | D5 | D4  | D3  | D2        | D1 | D0     |
|------|--------------------------|---------|----|----|-----|-----|-----------|----|--------|
| 17H  | Side Tone Volume Control | SV[2:0] |    |    | SVE | 0   | HPFC[1:0] |    | HPFADN |
|      | R/W                      | R/W     |    |    | R/W | R/W | R/W       |    | R/W    |
|      | Default                  | 000     |    |    | 0   | 0   | 00        |    | 0      |

HPFADN: Digital Microphone HPF Control

0: On (default)

1: Off

HPFC[1:0]: Cut-off frequency of Digital Microphone HPF ([Table 22](#))

Default: "00" (29.8 Hz @fs = 48 kHz)

SVE: Side Tone Additional Control ([Table 25](#))

0: Disable (default)

1: Enable

SV[2:0]: Side Tone Volume Control; 0 dB to -24 dB, 6 dB step ([Table 26](#))

Default: "000" (0 dB)

| Addr | Register Name    | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 26H  | DAC Adjustment 1 | T8  | T7  | T6  | T5  | T4  | T3  | T2  | T1  |
|      | R/W              | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|      | Default          | 0   | 1   | 1   | 0   | 1   | 1   | 0   | 0   |

\* 02H data must be written to DAC Adjustment 1 (Addr. 26H) before analog blocks (CP1, CP2, LDO1, DAC, headphone amplifier and PLL) are powered up.

| Addr | Register Name    | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
|------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| 27H  | DAC Adjustment 2 | T16 | T15 | T14 | T13 | T12 | T11 | T10 | T9  |
|      | R/W              | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
|      | Default          | 0   | 1   | 0   | 0   | 0   | 0   | 0   | 0   |

\* C0H data must be written to DAC Adjustment 2 (Addr. 27H) before analog blocks (CP1, CP2, LDO1, DAC, headphone amplifier and PLL) are powered up.

| Addr | Register Name | D7  | D6  | D5  | D4  | D3  | D2  | D1        | D0 |
|------|---------------|-----|-----|-----|-----|-----|-----|-----------|----|
| 29H  | Mode Control  | 0   | 0   | 0   | 0   | 0   | 0   | HPMD[1:0] |    |
|      | R/W           | R/W | R/W | R/W | R/W | R/W | R/W | R/W       |    |
|      | Default       | 0   | 0   | 0   | 0   | 0   | 0   | 00        |    |

HPMD[1:0]: Headphone Amplifier Operation Mode Setting (N/A: Not available) ([Table 5](#), [Table 9](#))

00: In case of fs = 8 to 48 kHz (SRC Bypass Mode) / FSO = 8 to 48 kHz (SRC Mode) (default)

01: N/A

10: N/A

11: In case of fs = 64 to 192 kHz (SRC Bypass Mode) / FSO = 64 to 192 kHz (SRC Mode)

## 10. Recommended External Circuits

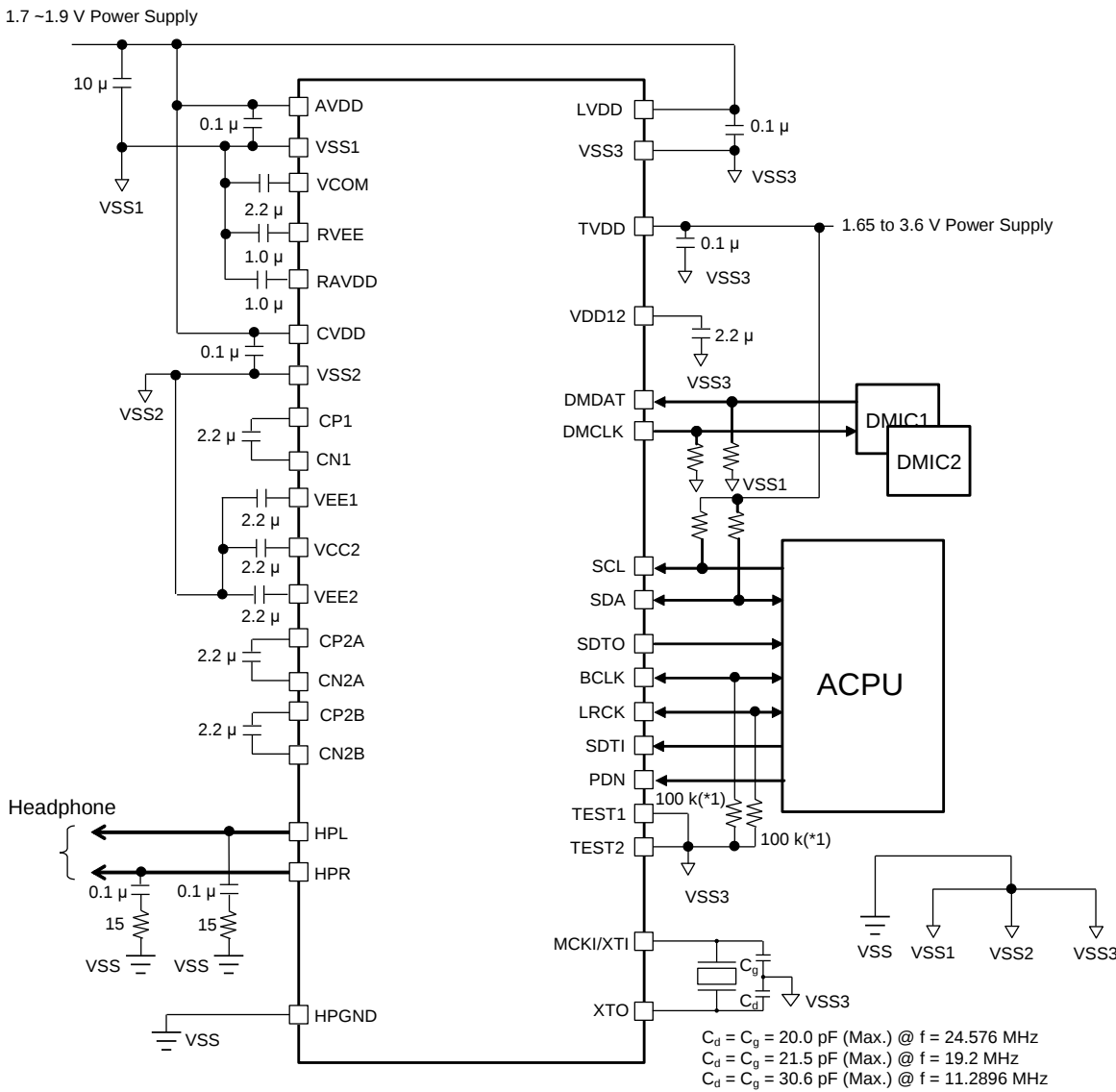


Figure 45. System Connection Diagram (When using X'tal Oscillator and Digital Microphone)

\*1: When the AK4331 is in master mode, a pull-down resistor (e.g. 100 kΩ) is needed.

## 1. Grounding and Power Supply Decoupling

The AK4331 requires careful attention to power supply and grounding arrangements. The PDN pin should be held “L” when power supplies are tuning on. AVDD should be powered up before or at the same time of CVDD. Power-up sequence of TVDD and LVDD is not critical. The PDN pin is allowed to be “H” after all power supplies are applied and settled. To power down the AK4331, set the PDN pin to “L” and power down CVDD before or at the same time of AVDD. Power-down sequence of LVDD and TVDD is not critical.

To avoid pop noise on analog output when power-up/down, the AK4331 should be operated along the following recommended power-up/down sequence.

### 1) Power-up

- The PDN pin should be held “L” when power supplies are turning on. The AK4331 can be reset by keeping the PDN pin “L” for 1 msec or longer after all power supplies are applied and settled. Then release the reset by setting the PDN pin to “H”.

### 2) Power-down

- Each of power supplies can be powered OFF after the PDN pin is set to “L”.

VSS1, VSS2 and VSS3 of the AK4331 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as close the power supply pins as possible. Especially, the small value ceramic capacitor is to be closest.

## 2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2  $\mu\text{F}$  ceramic capacitor attached between the VCOM pin eliminates the effects of high frequency noise. No load current is allowed to be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4331.

## 3. Charge Pump and LDO Circuits

Capacitors for CP1 block (connected between the CP1 pin and the CN1 pin, between the VEE1 pin and the VSS2 pin) and for CP2 block (connected between the CP2A pin and the CN2A pin, between the CP2B pin and the CN2B pin, between the VCC2 pin and the VSS2 pin, between the VEE2 pin and the VSS2 pin) should be low ESR 2.2  $\mu\text{F}$   $\pm 50\%$ .

Capacitors for LDO1P block (connected between the RAVDD pin and the VSS1 pin) and for LDO1N block (connected between the RVEE pin and the VSS1 pin) should be low ESR from 1.0  $\mu\text{F}$   $\pm 50\%$  to 4.7  $\mu\text{F}$   $\pm 50\%$ .

These capacitors must be connected as close as possible to the pins. No load current may be drawn from the Positive / Negative Power Output pin (VEE1, RAVDD, RVEE, VCC2 and VEE2 pins).

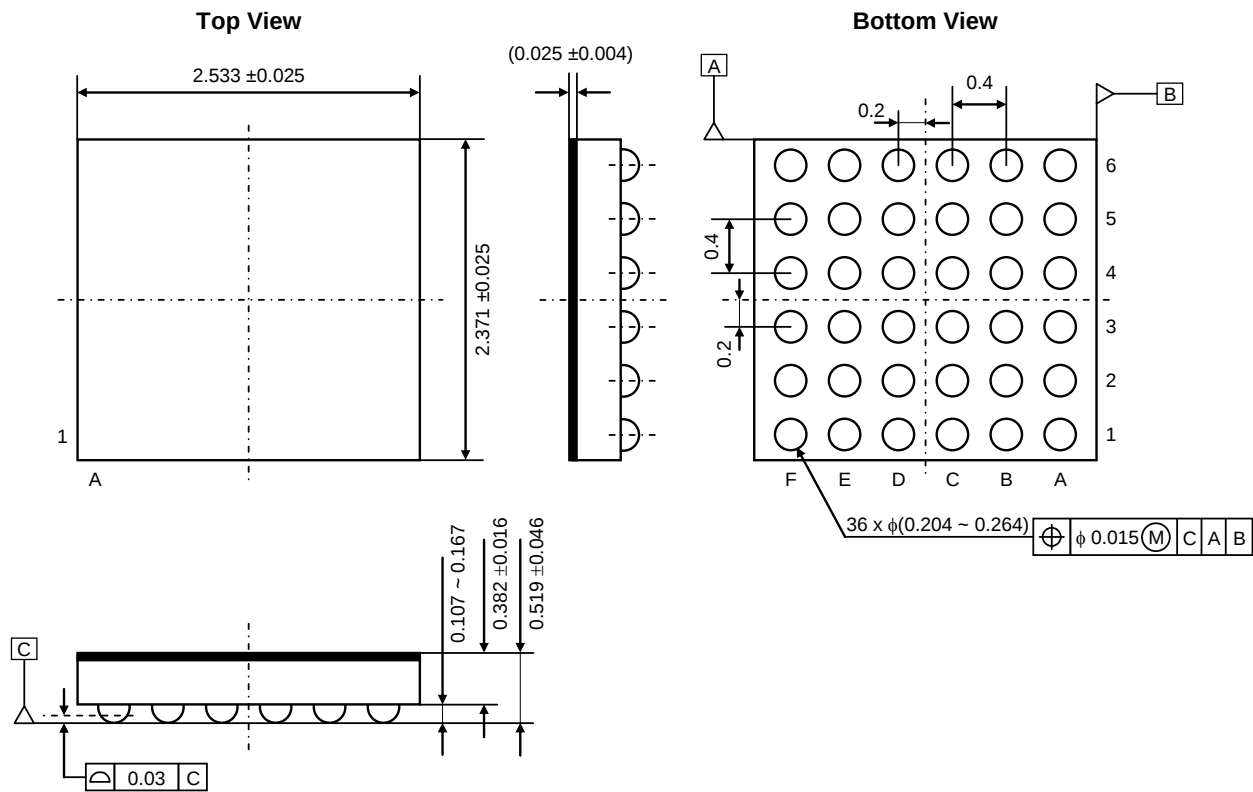
## 4. Analog Outputs

Headphone outputs are single-ended and centered at HPGND (0 V). They should be directly connected to a headphone without AC coupling.

## 11. Package

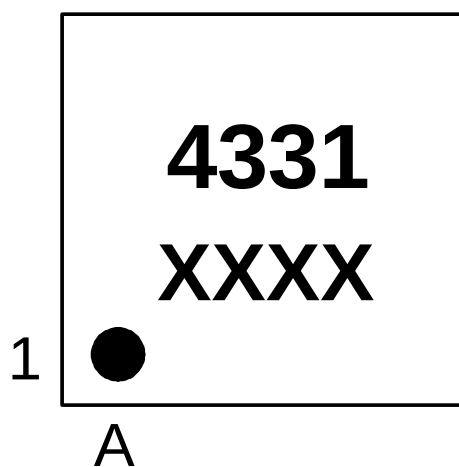
### 11-1. Outline Dimensions

#### 36-pin CSP (Unit: mm)



### 11-2. Material and Lead Finish

Package molding compound: Epoxy Resin, Halogen Free  
 Solder ball material: SnAgCu

**11-3. Marking**

XXXX: Date code (4 digits)  
Pin #A1 indication

**12. Ordering Guide**

|           |                             |                           |
|-----------|-----------------------------|---------------------------|
| AK4331ECB | −40 to 85°C                 | 36-pin CSP (0.4 mm pitch) |
| AKD4331   | Evaluation board for AK4331 |                           |

|                             |
|-----------------------------|
| <b>13. Revision History</b> |
|-----------------------------|

| Date (Y/M/D) | Revision | Reason        | Page | Contents |
|--------------|----------|---------------|------|----------|
| 18/07/12     | 00       | First Edition |      |          |

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