R1260S032A120-0300EV

60V Input / 80V Absolute Maximum Rating Synchronous Step-down DC/DC Controller Evaluation Board

No.EEV-511-S032A120-0300-250423

R1260S032A120-0300EV is the evaluation board for R1260 which has the below features, benefits and specifications.

OVERVIEW

The R1260S is a step-down DC/DC controller which can generate an output voltage of 1.0 V to 16.0 V by driving external high- / low-side NMOSFETs. By the adoption of a unique current mode PWM architecture without an external current sense resistor, this device can make up a stable DC/DC converter with high-efficiency even if adding low Ron MOSFETs and a low DCR inductor externally.

KEY BENEFITS

- 48 V power can be provided by a wide-ranging input voltage of 5 V to 60 V.
- High-accuracy feedback voltage: 0.8 V ±1.5% (−40°C ≤ Ta ≤ 105°C)
- High efficiency at light load (I_{OUT}=1mA) by VFM control (80% @V_{IN}=24V, 70% @V_{IN}=48V)

KEY SPECIFICATIONS

- Input Voltage Range: 5 V to 60 V
- Maximum Rating: 80 V
- Output Voltage: 12.0 V
- Feedback Voltage: 0.8 V ±1.5%
- Consumption Current at No Load: Typ.15μA (at VFM mode)
- Oscillator Frequency: 300kHz
  Adjustable Soft-start with an external capacitor: 600μs (without external capacitor)
- Minimum ON Time: Typ. 130 ns
- Minimum OFF Time: Typ.120 ns
- Selectable Output Voltage Controls: PWM/VFM Auto-switching mode / Forced PWM / PLL_PWM mode
- Operating Temperature Range: -40°C to 105°C
- Spread Spectrum Clock Generator (SSCG)*Option
- Power Good Output
- Undervoltage Detection (UVD), Overvoltage Detection (OVD)
- Undervoltage Lockout (UVLO)
- Thermal Shutdown: Tj = 160°C (Typ.)
- Overcurrent Protection: Hiccup-type
- Short-circuit Protection: LX to V_{IN} or GND
- Package: HSOP-18
- For more details on R1260 IC, please refer to
  https://www.nisshinbo-microdevices.co.jp/en/products/dc-dc-switching-regulator/spec/?product=r1260

PART NUMBER INFORMATION

Product Name	Package
R1260S032A120-0300	HSOP-18

03：Select the set output voltage range.

Set Output Voltage Range
8 V < V_{OUT} ≤ 16 V

2：Select the current limit threshold voltage.

Current limit threshold voltage (Typ.)	Reverse current limit threshold voltage (Typ.)
70mV	-35mV

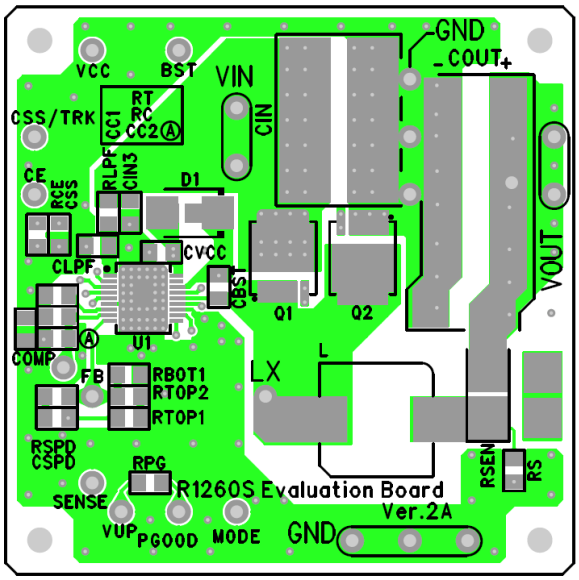
A：Select the combination of overcurrent protection and SSCG.

Overcurrent Protection	SSCG
Hiccup mode	Disable

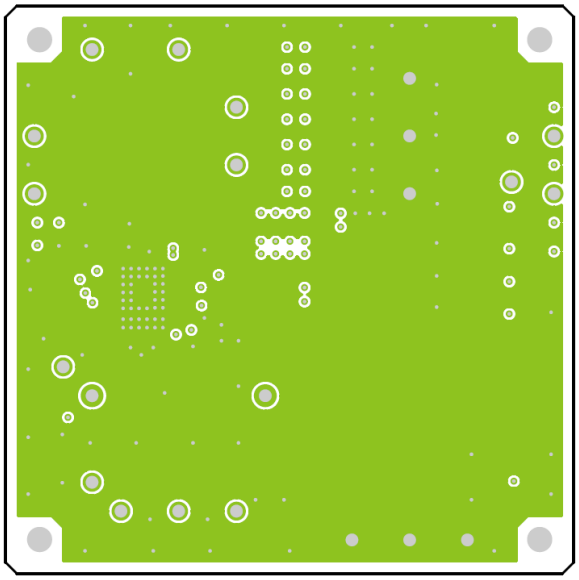
120：12V, Output Voltage

PCB LAYOUT

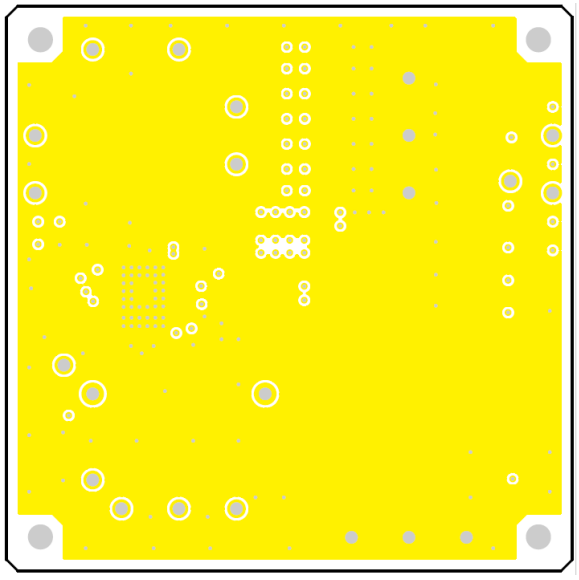
Evaluation board of R1260S (Package：HSOP-18)



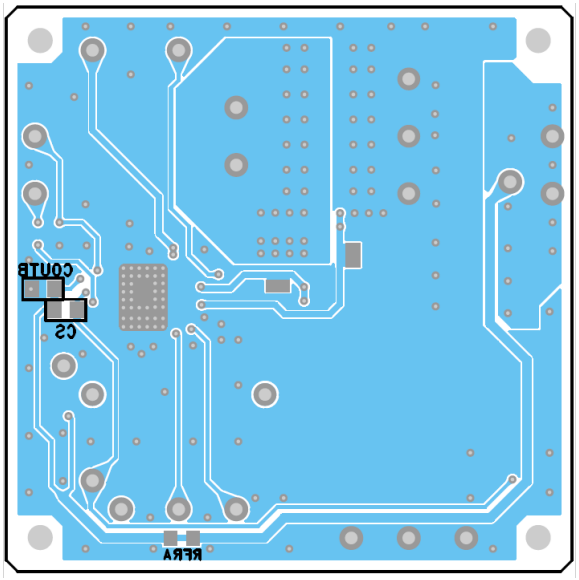
1st Layer (Top Layer)



2nd Layer

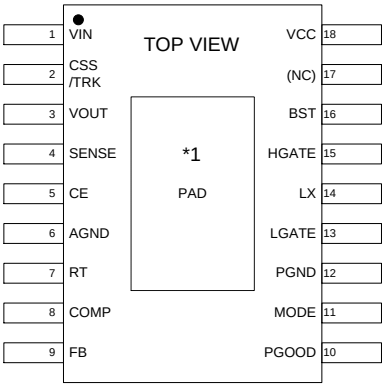


3rd Layer



4th Layer (Bottom Layer)

PIN DESCRIPTIONS



R1260S Pin Configuration

∗1 The tab on the bottom of the package must be electrically connected to GND (substrate level) when mounted on the board.

Pin Description

Pin No.	I/O	Pin Name	Description
1	I	VIN	Power Supply Input Pin. Apply input voltage between VIN pin and GND. Connect the input capacitor between the VIN pin and GND.
2	I	CSS/TRK	Soft-start and Tracking Control input pin. A capacitor to ground from this pin sets the ramp time to full output voltage. Without the capacitor, soft start time is Typ. 600us. Controlling this pin externally from 0V to 0.8V with a certain slope, the output voltage tracks the slope.
3	I	VOUT	Power Supply for Internal Circuit/Output Voltage Sense pin. Connect this pin to Output Voltage node. Connect a capacitor between this pin and GND.
4	I	SENSE	Sense pin for inductor current. By connecting a sense resistor between the VOUT pin and SENSE pin, the current value of the current limit and reverse current limit can be set.
5	I	CE	Chip enable pin. Forcing this pin above 1.3V enables the operation of the R1260. Forcing this pin below 1.1V stops switching operation of the R1260. Forcung this pin below 0.39V, all functions are disabled.
6	ー	AGND	Analog ground of the internal circuit. Connect this pin to the GND of PCB.
7	I	RT	Timing Resistor pin to Program the Oscillator Frequency. Connecting a resistor to ground from this pin sets the switching frequency. Switching frequency range is from 150kHz to 600kHz. R_{RT} [kΩ] = 34064 x f_{OSC} [kHz] ^ (-1.025)
8	O	COMP	Error amplifier phase compensation pin. Connect a resistor and a capacitor for phase compensation.
9	I	FB	Feedback input pin to the error amplifier. Receives the feedback voltage from a restive divider connected across the output.
10	O	PGOOD	Power-good output pin. NMOS open-drain logic output that is pulled to ground when the output voltage is not within the normal state. Refer to the “Power Good Function”. Pull-up voltage rating is 6V.
11	I	MODE	Mode Select and External Clock Synchronization Input pin. To select forced PWM mode, connect this pin to above designated “High”. Connecting this pin to a voltage between 0V and designated “Low” selects PWM/VFM auto-switching mode.
12	ー	PGND	Power ground. Connect this pin close to GND of PCB.
13	O	LGATE	Gate Drive pin for Bottom(low-side) Synchronous N-Channel MOSFET.

14	I	LX	Switch Node Connection to Inductor. This pin connects to the switch node between source of the high-side MOSFET and the drain of the low-side MOSFET, and the inductor.
15	O	HGATE	Gate Drive pin for Top(high-side) N-Channel MOSFET.
16	O	BST	Bootstrapped pin. A capacitor (C_{BST}) between the LX pin and the BST pin, and Schottky diode are tied between the VCC pin and the BST pin. Voltage between BST pin and Lx pin is controlled to Typ.5V.
17	—	NC	No connection. It is recommended to be left open to reduce the risk of adjacent pins' short.
18	O	VCC	Output pin of Internal 5V linear Regulator The control circuits of drive external NMOSFETs are powered from this voltage source. Must be decoupled to power ground with an output capacitor (C_{VCC}).

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Item	Ratings	Unit
V_{IN}	Input voltage	-0.3 to 80	V
V_{CE}	CE pin voltage	-0.3 to V_{IN}+0.3 ≤ 80	V
$V_{CSS/TRK}$	CSS/TRK pin voltage	-0.3 to 3	V
V_{OUT}	VOUTpin voltage	-0.3 to 20	V
V_{SENSE}	SENSE pin voltage	-0.3 to 20	V
V_{RT}	RT pin voltage	-0.3 to 3	V
V_{COMP}	COMP pin voltage	-0.3 to V_{CC} + 0.3 ≤ 6	V
V_{FB}	FB pin voltage	-0.3 to 2.85	V
$V_{SENSEOUT}$	Voltage between VOUT and SENSEpins	-0.3 to 0.3	V
V_{CC}	VCC pin votlage	-0.3 to 6	V
	Output current for VCC pin	Internally limited	mA
V_{BST}	BST pin voltage	LX-0.3 to LX+6	V
V_{HGATE}	HGATE pin voltage	LX-0.3 to BST	V
V_{LX}	LX pin voltage	-0.3 to V_{IN} +0.3 ≤ 80	V
V_{LGATE}	LGATE pin voltage	-0.3 to V_{CC} + 0.3 ≤ 6	V
V_{MODE}	MODE pin voltage	-0.3 to 6	V
V_{PGOOD}	PGOOD pin voltage	-0.3 to 6	V
P_D	Power Dissipation	Refer to Appendix *"POWER DISSIPATION"*	
Tj	Junction Temperature	−40 to 125	°C
Tstg	Storage Temperature Range	−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Item	Ratings	Unit
V_{IN}	Input Voltage	5.0 to 60	V
Ta	Operating Temperature Range	−40 to 105	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

V_{IN} = 48 V, V_{CE} = 5 V, unless otherwise specified.
The specifications surrounded by [ ] are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R1260Sxxyz Electrical Characteristics (Ta = 25°C)

Symbol	Item		Conditions	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage			1		16	V
V_{CC}	VCC Pin Voltage (VCC – AGND)		V_{FB} = 0.84 V	[4.85]	5.1	[5.3]	V
$I_{STANDBY}$	Standby Current		V_{IN} = 60 V, V_{CE} = 0 V		3	8.5	µA
I_{VIN1}	VIN Consumption Current 1 at Switching Stop in PWM Mode	R1260S032A	V_{FB} = 0.84 V, V_{MODE} = 5 V, V_{OUT} = V_{SENSE} = V_{LX} = 5 V		1.00	1.50	mA
I_{VIN2}	VIN Consumption Current 2 at Switching Stop in VFM mode	R1260S032A	V_{FB} = 0.84 V, V_{MODE} = 0 V V_{OUT} = V_{SENSE} = V_{LX} = 5 V		15	45	mA
V_{UVLO2}	UVLO Threshold Voltage		V_{CC} Rising	4.20	4.50	4.80	V
V_{UVLO1}			V_{CC} Falling	3.68	3.80	3.97	V
V_{FB}	FB Voltage Accuracy		Ta = 25°C	0.792	0.8	0.808	V
			-40°C ≤ Ta ≤ 105°C	[0.788]		[0.812]	
f_{OSC0}	Oscillation Frequency 0		RT = 200 kΩ	[135]	150	[165]	kHz
f_{OSC1}	Oscillation Frequency 1		RT = 47 kΩ	[540]	600	[660]	kHz
t_{OFF}	Minimum OFF Time		V_{IN} = 5 V, V_{OUT} = 5 V		120	[190]	ns
t_{ON}	Minimum ON Time				130	[170]	ns
f_{SYNC}	Synchronizing Frequency		f_{OSC} as reference	[f_{OSC} x0.5]		[f_{OSC} x1.5]	kHz
				[150]		[600]	
t_{SS1}	Soft-start Time 1		$V_{CSS/TRK}$ = OPEN	[0.25]	0.6	[1.35]	ms
t_{SS2}	Soft-start Time 2		C_{SS} = 4.7 nF	[1.6]	2.1	[2.8]	ms
I_{TSS}	Charge Current for Soft-start Pin		$V_{CSS/TRK}$ = 0 V	[1.8]	2	[2.2]	µA
V_{SSEND}	CSS/TRK pin Voltage at End of Soft-start			[V_{FB}]	V_{FB} +0.03	[V_{FB}+0.06]	V
R_{DIS_CSS}	Discharge Resistance for CSS/TRK Pin		V_{IN} = 4.5 V, V_{CE} = 0 V, $V_{CSS/TRK}$ = 3 V	[1.0]	3.0	[6.5]	kΩ
$R_{UPHGATE}$	On-resistance of Pull-up Transistor (HGATE Pin)		(BST – LX) = 5 V, I_{HGATE} = -100 mA		2.5	[5.7]	Ω
$R_{DOWNHGATE}$	On-resistance of Pull-down Transistor (HGATE Pin)		(BST – LX) = 5 V, I_{HGATE} = 100 mA		1.5	[5.0]	Ω
$R_{UPLGATE}$	On-resistance of Pull-up Transistor (LGATE Pin)		(VCC – PGND) = 5V, I_{LGATE} = -100mA		4.0	[7.2]	Ω
$R_{DOWNLGATE}$	On-resistance of Pull-down Transistor (LGATE Pin)		(VCC – PGND) = 5 V, I_{LGATE} = 100 mA		1.5	[4.7]	Ω

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

V_{IN} = 48 V, V_{CE} = 5 V, unless otherwise specified.

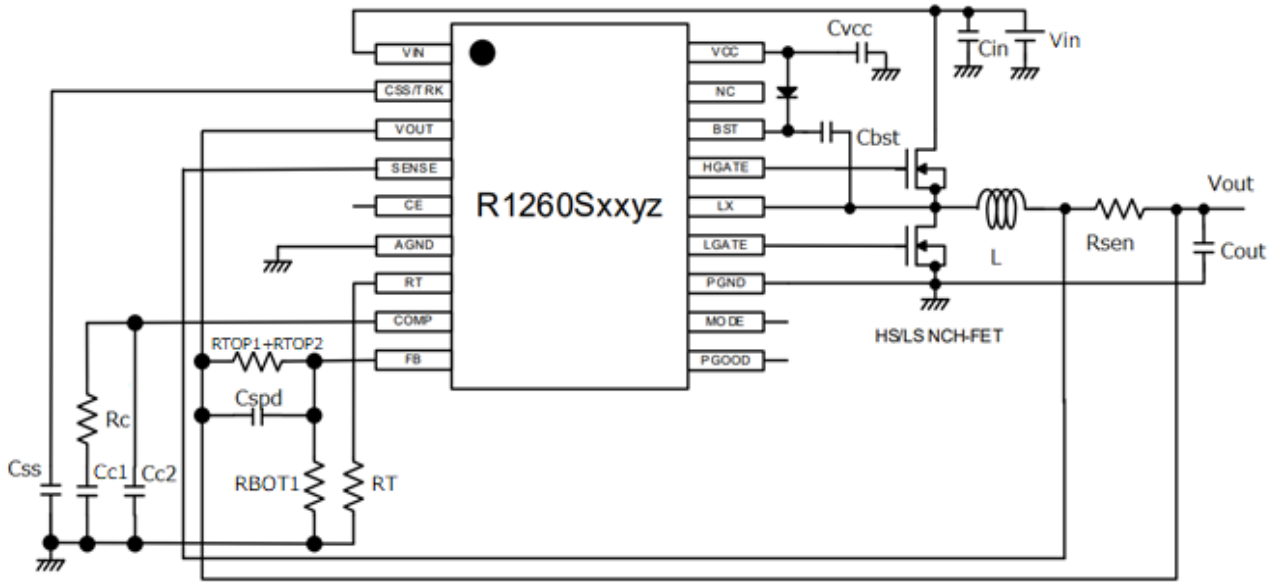
The specifications surrounded by ☐ are guaranteed by design engineering at -40°C ≤ Ta ≤ 105°C.

R1260Sxxyz Electrical Characteristics (Ta = 25°C)

Symbol	Item		Conditions	Min.	Typ.	Max.	Unit
V_{ILIMIT}	Current Limit Threshold Voltage (SENSE – VOUT)	R1260S032A		56	70	84	mV
$V_{IREVLIMIT}$	Reverse Current Sense Threshold (SENSE – VOUT)	R1260S032A	MODE = "High" or "CLK Input"	-49	-35	-22	mV
$V_{LXSHORTL}$	LX Short to GND Detector Threshold Voltage (VIN – LX)			0.80	1.0	1.2	V
$V_{LXSHORTH}$	LX Short to VCC Detector Threshold Voltage (LX – PGND)			0.32	0.40	0.44	V
V_{CEH}	CE Pin Input Voltage, high			1.3			V
V_{CEL}	CE Pin Input Voltage, low					1.1	V
I_{CEH}	CE Pin Input Current, high		V_{CE} = 60 V	-0.10		2.45	µA
I_{CEL}	CE Pin Input Current, low		V_{CE} = 0 V	-1.00	0	1.00	µA
I_{FBH}	FB Pin Input Current, high		V_{FB} = 2.85 V	-0.10		0.10	µA
I_{FBL}	FB Pin Input Current, low		V_{FB} = 0 V	-0.10		0.10	µA
V_{MODEH}	MODE Pin Input Voltage, high			1.33			V
V_{MODEL}	MODE Pin Input Voltage, low					0.74	V
I_{MODEH}	MODE Pin Input Voltage, high	R1260S032A	V_{MODE} = 5 V	3.0	5.3	9.6	µA
I_{MODEL}	MODE Pin Input Voltage, low		V_{MODE} = 0 V	-1.00	0	1.00	µA
$V_{PGOODOFF}$	PGOOD Pin Output Voltage, low		V_{IN} = 5.0 V, I_{PGOOD} = 1 mA		0.26	0.64	V
$I_{PGOODOFF}$	PGOOD Pin Leakage Current		V_{IN} = 60 V, V_{CE} = 0 V, V_{PGOOD} = 6 V	-0.10	0	0.10	µA
V_{FBOVD1}	FB Pin OVD Threshold Voltage		V_{FB} Rising	V_{FB} x1.070	V_{FB} x1.100	V_{FB} x1.135	V
V_{FBOVD2}			V_{FB} Falling	V_{FB} x1.044	V_{FB} x 1.070	V_{FB} x1.110	V
V_{FBUVD1}	FB Pin UVD Threshold Voltage		V_{FB} Falling	V_{FB} x0.865	V_{FB} x 0.900	V_{FB} x0.936	V
V_{FBUVD2}			V_{FB} Rising	V_{FB} x0.890	V_{FB} x 0.930	V_{FB} x0.970	V
gm (EA)	Trans Conductance Amplifier		V_{COMP} = 1.5 V	0.55	1.00	1.45	mS

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C).

TYPICAL APPLICATION CIRCUIT



R1260S Typical Application Circuit

Recommended values for components

Symbol	Value
CIN	22 µF * 3set
COUT	100 µF * 3set
CBST	0.22 µF
CVCC	2.2 µF
CSPD	OPEN
CC1	33 nF
CC2	220 pF
CSS	33 nF
L	6.8 µH
RSEN	5 mΩ
RTOP1	270 kΩ
RTOP2	39 kΩ
RBOT1	22 kΩ
RT	100 kΩ
RC	6.8 kΩ

TECHNICAL NOTES

The performance of power source circuits using this IC largely depends on peripheral circuits. When selecting the peripheral components, please consider the conditions of use. Do not allow each component, PCB pattern or the IC to exceed their respected rated values (voltage, current, and power) when designing the peripheral circuits.

- It is recommended to mount all the external components on the same layer as the IC on board. External components must be connected as close as possible to the ICs and make wiring as short as possible. Especially, the capacitor connected in between V_{IN} pin and GND pin must be wiring the shortest. If their impedance is high, internal voltage of the IC may shift by the switching current, and the operating may be unstable. Make the power supply and GND lines sufficient.

- Since the current loop of a switching regulator changes with each switching, the current changes significantly and high-frequency noise may be generated due to parasitic capacitance and inductance. Design the board layout so that the current loop length is as short as possible. Also, make sure that the current loops do not overlap the line from C_{OUT} to the subsequent load side to avoid the bad impact from the output voltage ripple.

- AGND and PGND for the controller must be wired to the GND line at the low impedance point of the same layer with C_{IN} and C_{OUT}. Reduce the impedance between the AGND and PGND of IC

- It is recommended that the C_{IN}, high-side, and low-side MOSFETs be placed on the same layer as the IC on PCB. If vias are used and placed on a different layer from the IC, the parasitic inductance of vias may affect the ringing of the LX pin voltage and increase noise.

- R_{TOP}, R_{BOT}, and C_{SPD} should be set close to the FB pin, but mount them away from the inductor, LX pin, and BST pin to avoid their noise.

- Place a capacitor (C_{BST}) as close as possible to the LX pin and the BST pin. If controlling slew rate for EMI, a resistor (R_{BST}) should be in series between the BST pin and the capacitor (C_{BST}), but not be in series to MOSFET for HGATE and LGATE pins. Because connecting the resistor in series to the MOSFET becomes a cause of a through-current.

- The tab on the bottom of the HSOP-18 package must be connected to GND when mounted on the board. To improve thermal dissipation on the multilayer board, set via to release the heat to the other layer in the connecting part of the tab on the bottom. Likewise, thermal dissipation for MOSFET is required.

- The MODE pin requires the "High" / "Low" voltages with the high stability when the forced PWM mode (MODE = “High”) or the VFM mode (MODE = “Low”) is enabled. If the voltage with the high stability cannot be applied, connection to the VCC pin as “High” level or the AGND pin as “Low” level is recommended. If connecting to the PGND pin as noisy, a malfunction may occur. Avoid the use of the MODE pin being “Open”.

- If V_{OUT} is a minus potential, the setup cannot occur.

- The power for the controller and for the high-side MOSFET must be used on the same power supply, since the internal slope compensation is applied as the power supply voltage of the high-side MOSFET is equal to the controller's. If applying the other power supply voltage, the controller will become unstable owing to the inappropriate slope compensation.

- The thermal shutdown function prevents the IC from danger in smoke or burn, but not to ensure the reliability of the IC or to keep it below the absolute maximum rating. In addition, it is not effective against the heat generated by abnormal condition such as latch-up and overvoltage forcing.

- Do not design with depending on the thermal shutdown function of this IC as the system protection. The thermal shutdown function is designed for this IC.

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