R1243K is the discontinued product.

NISSHINBO

R1243x Series

30 V Input 2 A Buck DC/DC Converter

No.EA-206-250715

OUTLINE

The R1243x is a CMOS-based step-down DC/DC converter with internal Nch high-side Tr. (0.175 Ω), which can provide the maximum 2 A output current. Internally, the R1243x consists of an oscillator, a PWM control circuit, a reference voltage unit, an error amplifier, phase compensation circuits, a slope circuit, a soft-start circuit, protection circuits, internal voltage regulators and a switch for bootstrap circuit. A step-down DC/DC converter can be configured by only adding an inductor, resistors, a diode and capacitors to the R1243x.
The R1243x is a current mode operating type DC/DC converter that does not require external current sense resistor. It has high-speed response time and is high efficiency and compatible with ceramic capacitors.
The oscillator frequency of the R1243x001A/B/E is fixed to 1000 kHz. The oscillator frequency of the R1243x001C/D is fixed 330 kHz.
The R1243x has a cycle-by-cycle peak current limit function, a short protection function, a thermal shutdown function and an UVLO as protection features. The R1243x001A/C/E has a latch protection with 2 ms delay time, the R1243x001B/D has a fold-back protection that keep operating during short condition with lower operating frequency and limiting the LX current. The R1243x has a built-in soft-start time (Typ. 0.4 ms). In addition to this, the soft-start time is adjustable by adding an external capacitor. The R1243x has the FLG pin, which mainly monitors the FB pin voltage and gives a flag output by the Nch open drain if the abnormal condition is detected.
The R1243x is offered in 8-pin HSOP-8E and 10-pin DFN(PL)2527-10 packages that can achieve high density mounting.

FEATURES

- Operating Voltage Range ..... 4.5 V to 30 V
- Standby Current ..... Max. 10 µA (V_{IN} = 30 V, CE = L)
- Supply Current..... Typ. 0.7 mA (V_{IN} = 30 V, V_{FB} = 1.0 V)
- Output Voltage Range ..... 0.8 V to 18 V, Adjustable with external resistors
- Feedback Voltage..... 0.5 V with 1.4% accuracy
- Output Current..... Max. 2 A(1)
- Peak Current Limiting ..... Typ. 3.8 A
- Internal Nch MOSFET Driver..... Typ. 175 mΩ
- Maximum Duty Cycle..... Min. 85%
- Oscillator Frequency..... R1243x001A/B/E: 1000 kHz, R1243x001C/D: 330 kHz
- Latch Type Protection..... R1243x001A/C: Typ. 2 ms, R1243x001E: 0.08 ms
- Fold-back Type Protection..... R1243x001B: 250 kHz, R1243x001D: 82.5 kH
- Internal Soft-start Time ..... Typ. 0.4 ms, TSS = Open
- External Soft-start Time..... Typ. 12 ms, C_{SS} = 0.1 µF
- Flag Output..... Typ. 0.25 ms, FLG “OFF” delay time
- UVLO Released Voltage..... Typ. 4.0 V
- Thermal Shutdown ..... Typ. 160° C, Hysteresis = 35° C
- Package ..... HSOP-8E, DFN(PL)2527-10

(1) This is an approximate value, because output current depends on conditions and external parts.

APPLICATIONS

- Digital Home Appliances
- Hand-held Communication Equipment: Cameras, VCRs, Camcorders
- Battery-powered Equipment
- Battery Charger

SELECTION GUIDE

The package type, the oscillator frequency (Fixed: 1000 kHz, 330 kHz) and the short-circuit protection type (Latch, Fold-back) are user-selectable options.

Selection Guide

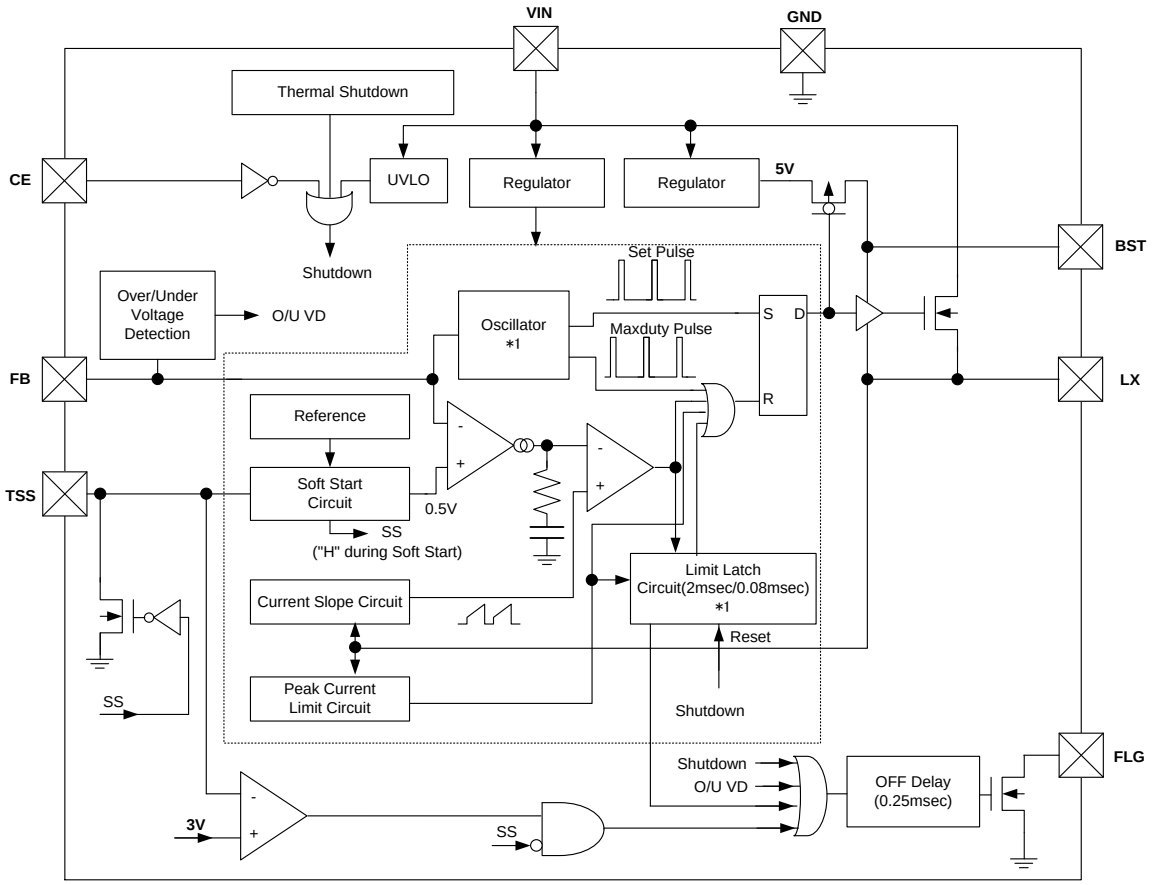
Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1243S001∗-E2-FE	HSOP-8E	1,000 pcs	Yes	Yes
R1243K001∗-TR	DFN(PL)2527-10	5,000 pcs	Yes	Yes

∗: Specify the oscillator frequency and the short-circuit protection type.

(A) Fixed Frequency: 1000 kHz, Latch Type (2 ms)
(B) Fixed Frequency: 1000 kHz, Fold-back Type
(C) Fixed Frequency: 330 kHz, Latch Type (2 ms)
(D) Fixed Frequency: 330 kHz, Fold-back Type
(E) Fixed Frequency: 1000 kHz, Latch Type (0.08 ms), only for HSOP-8E

R1243K is the discontinued product.

BLOCK DIAGRAM

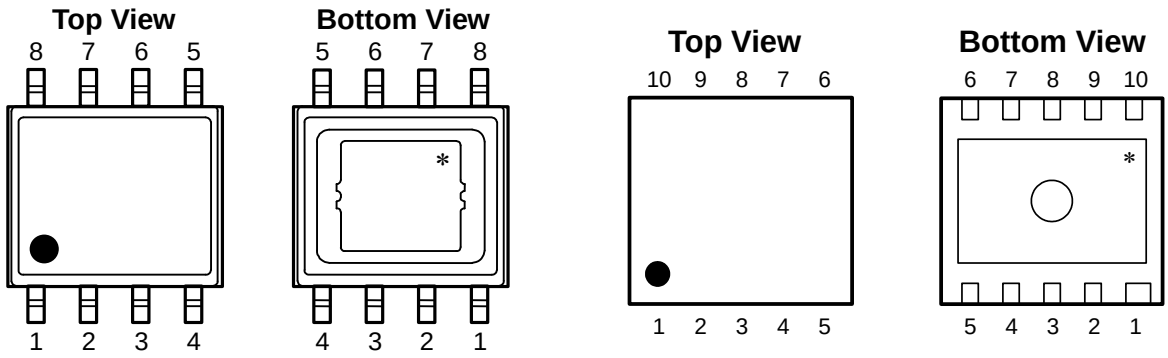


R1243x Block Diagram

*1

Version	Oscillator Frequency	Short-circuit Protection Type
A	1000 kHz	Latch Type (2 ms)
B	1000 kHz	Fold-back Type
C	330 kHz	Latch Type (2 ms)
D	330 kHz	Fold-back Type
E	1000 kHz	Latch Type (0.08 ms)

PIN DESCRIPTIONS



HSOP-8E Pin Configuration **DFN(PL)2527-10 Pin Configuration**

* The tab is substrate level (GND). It must be connected to the GND level.

R1243S001x Pin Description

Pin No	Symbol	Pin Description
1	BST	Bootstrap Pin
2	VIN	Power Supply Pin
3	LX	LX Switching Pin
4	GND	Ground Pin
5	FB	Feedback Pin
6	FLG	Flag Output Pin
7	CE	Chip Enable Pin, Active with “H”
8	TSS	Soft-start Pin

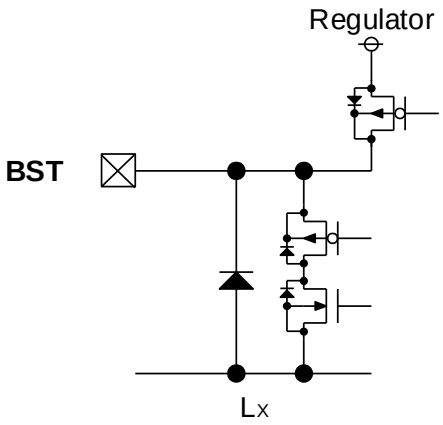
R1243K001x Pin Description

Pin No	Symbol	Pin Description
1	LX	LX Switching Pin
2	LX	LX Switching Pin
3	GND	Ground Pin
4	FB	Feedback Pin
5	FLG	Flag Output Pin(1)
6	CE	Chip Enable Pin, Active with “H”
7	TSS	Soft-start Pin
8	BST	Bootstrap Pin
9	VIN	Power Supply Pin
10	VIN	Power Supply Pin

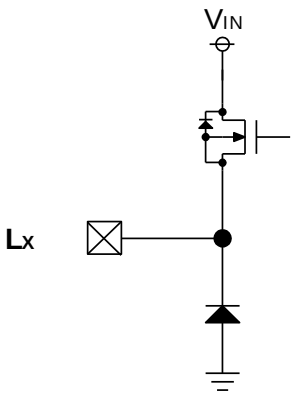
(1) The FLG pin should be connected to GND or should be left floating when it is not used.

INTERNAL EQUIVALENT CIRCUIT FOR EACH PIN

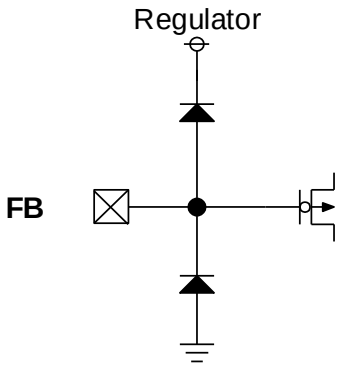
BST Pin



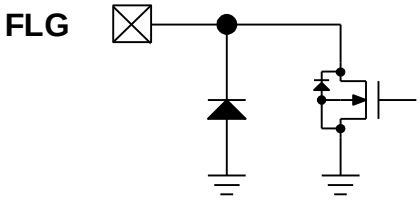
LX Pin



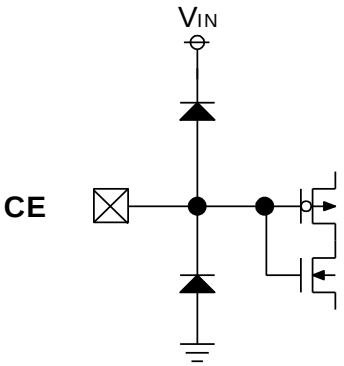
FB Pin



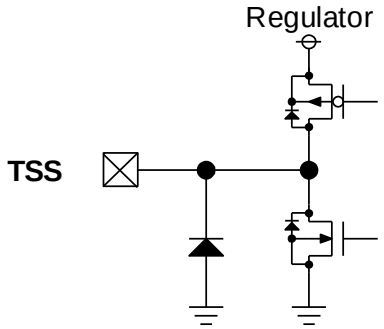
FLG Pin



CE Pin



TSS Pin



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings (GND = 0 V)

Symbol	Parameter	Rating			Unit
V_{IN}	Input Voltage	−0.3 V to 32 V			V
V_{BST}	Boost Pin Voltage	V_{LX} −0.3 V to V_{LX} + 6 V			V
V_{LX}	LX Pin Voltage	−0.3 V to V_{IN} + 0.3			V
V_{CE}	CE Pin Input Voltage	−0.3 V to V_{IN} + 0.3			V
V_{FB}	VFB Pin Voltage	−0.3 V to 6 V			V
V_{FLG}	FLG Pin Voltage	−0.3 V to 6 V			V
V_{TSS}	TSS Pin Voltage	−0.3 V to 6 V			V
P_D	Power Dissipation(1)	(HSOP-8E)	JEDEC STD. 51-7	2900	mW
		(DFN(PL)2527-10)	JEDEC STD. 51-7	2800	
Tj	Junction Temperature Range	−40 to 125			ºC
Tstg	Storage Temperature Range	−55 to 125			ºC

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the life time and safety for both device and system using the device in the field.
The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
V_{IN}	Operating Input Voltage	4.5 to 30	V
Ta	Operating Temperature Range	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

(1) Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, unless otherwise noted.

Electrical Characteristics (Ta = 25°C)

Symbol	Parameter	Test Conditions/Comments	Min.	Typ.	Max.	Unit
Istandby	Standby Current	V_{IN} = 30 V, V_{CE} = 0 V		0	10	µA
I_{SS}	Supply Current	V_{IN} = 30 V, V_{FB} = 1.0 V		0.7	1.0	mA
V_{UVLO1}	UVLO Detector Threshold	Falling	3.6	3.8	4.0	V
V_{UVLO2}	UVLO Released Voltage	Rising	3.8	4.0	4.2	V
$V_{UVLOHYS}$	UVLO Hysteresis	$V_{UVLO2} - V_{UVLO1}$		0.2		V
V_{FB}	Feedback Voltage		0.493	0.500	0.507	V
$\Delta V_{FB}/\Delta Ta$	Feedback Voltage Temperature Coefficient	−40ºC ≤ Ta ≤ 85ºC		±100		ppm /ºC
fosc	Oscillator Frequency (R1243x001A/B)		900	1000	1100	kHz
	Oscillator Frequency (R1243x001C/D)		290	330	370	kHz
f_{FLB}	Fold-back Frequency (R1243x001B/D)	V_{FB} < 0.35 V, fosc Ratio		25		%
Maxduty	Oscillator Maximum Duty Cycle	V_{IN} = 6 V	85	90	95	%
I_{TSS}	TSS Pin Current	V_{TSS} = 0 V		4.0		µA
t_{SS1}	Soft-start Time 1	TSS = open	0.2	0.4	0.8	ms
t_{SS2}	Soft-start Time 2	C_{SS} = 0.1 µF	6	12	18	ms
t_{DLY}	Latch Protection Delay Time (R1243x001A/C)	V_{IN} = 5.0 V		2.0		ms
	Latch Protection Delay Time (R1243x001E)			0.08		
I_{LXHOFF}	Highside Switch Leakage Current	V_{IN} = 30 V, V_{CE} = 0 V		0	10	µA
R_{LXH}	Highside Switch ON Resistance	$V_{BST} - V_{LX}$ = 4.5 V		175		mΩ
I_{LIMLXH}	Highside Switch Limited Current	$V_{BST} - V_{LX}$ = 4.5 V	2.8	3.8		A
V_{CEH}	CE “H” Input Voltage	V_{IN} = 30 V	1.4			V
V_{CEL}	CE “L” Input Voltage	V_{IN} = 30 V			0.4	V
I_{CEH}	CE “H” Input Current	V_{IN} = 30 V, V_{CE} = 30 V	−1.0	0	1.0	µA
I_{CEL}	CE “L” Input Current	V_{IN} = 30 V, V_{CE} = 0 V	−1.0	0	1.0	µA
I_{FBH}	FB “H” Input Current	V_{FB} = 2.0 V	−1.0	0	1.0	µA
I_{FBL}	FB “L” Input Current	V_{FB} = 0 V	−1.0	0	1.0	µA
T_{TSD}	Thermal Shutdown Detect Temperature	Hysteresis 35ºC		160		ºC
V_{FLGL}	FLG “L” Voltage	I_{FLG} = 1 mA			0.4	V
I_{FLGOFF}	FLG “OFF” Current	V_{FLG} = 5.5 V		0.0	1.0	µA
t_{FLGOFF}	FLG “OFF” Delay Time		0.05	0.25	0.60	ms
V_{OVD}	Overvoltage Detection Voltage	V_{FB}	0.55	0.60	0.65	V
V_{UVD}	Undervoltage Detection Voltage	V_{FB}	0.35	0.40	0.45	V

OPERATING DESCRIPTIONS

SOFT-START TIME ADJUSTMENT FUNCTION AND FLAG FUNCTION

Soft-Start Time Adjustment Function

The soft-start time (t_{SS}) of the R1243x is adjustable by adding the soft-start time adjusting capacitor (C_{SS}) to the TSS pin. The soft-start time can be set longer than the internal soft-start time (Typ. 0.4 ms).
For example, if the soft-start time adjusting capacitor (C_{SS}) is 0.1µF, the externally adjusted soft-start time will be 12 ms (Typ.). If there is no need of adjusting the soft-start time, leave the TSS pin as open so that the internal soft-start time (Typ. 0.4 ms) will be applied.

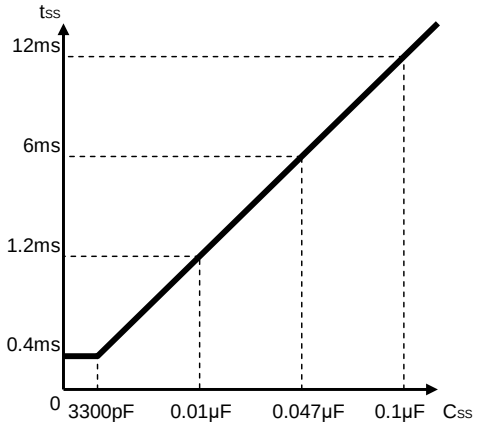


Fig. 1 C_{SS} vs. t_{SS} (Typ.)

Flag Function

The R1243x includes a flag output function using Nch open drain. If an abnormal state is detected, the flag output function turns the Nch transistor on and switches the FLG pin low. After recovering from the abnormal state, the flag output function turns the Nch transistor off and switches the FLG pin high after recovering from the low voltage detection (Typ. 0.4 V) and waiting for the delay time (Typ. 0.25 ms). The flag function detects the following conditions as abnormal states.

- CE = "L" (Shutdown)
- UVLO (Shutdown)
- Thermal Shutdown
- V_{FB} Overvoltage Detection (Typ. 0.6 V)
- V_{FB} Undervoltage Detection (Typ. 0.4 V)
- Active Latch Function (R1243x001A/C/E)
- Overvoltage Protection for TSS Pin after the Completion of Soft-start (Typ. 3 V)

The flag resistors (R_{FLG}) have to be between 10 kΩ to 100 kΩ. If the flag function is not used, the FLG pin has to be left open or connected to GND.

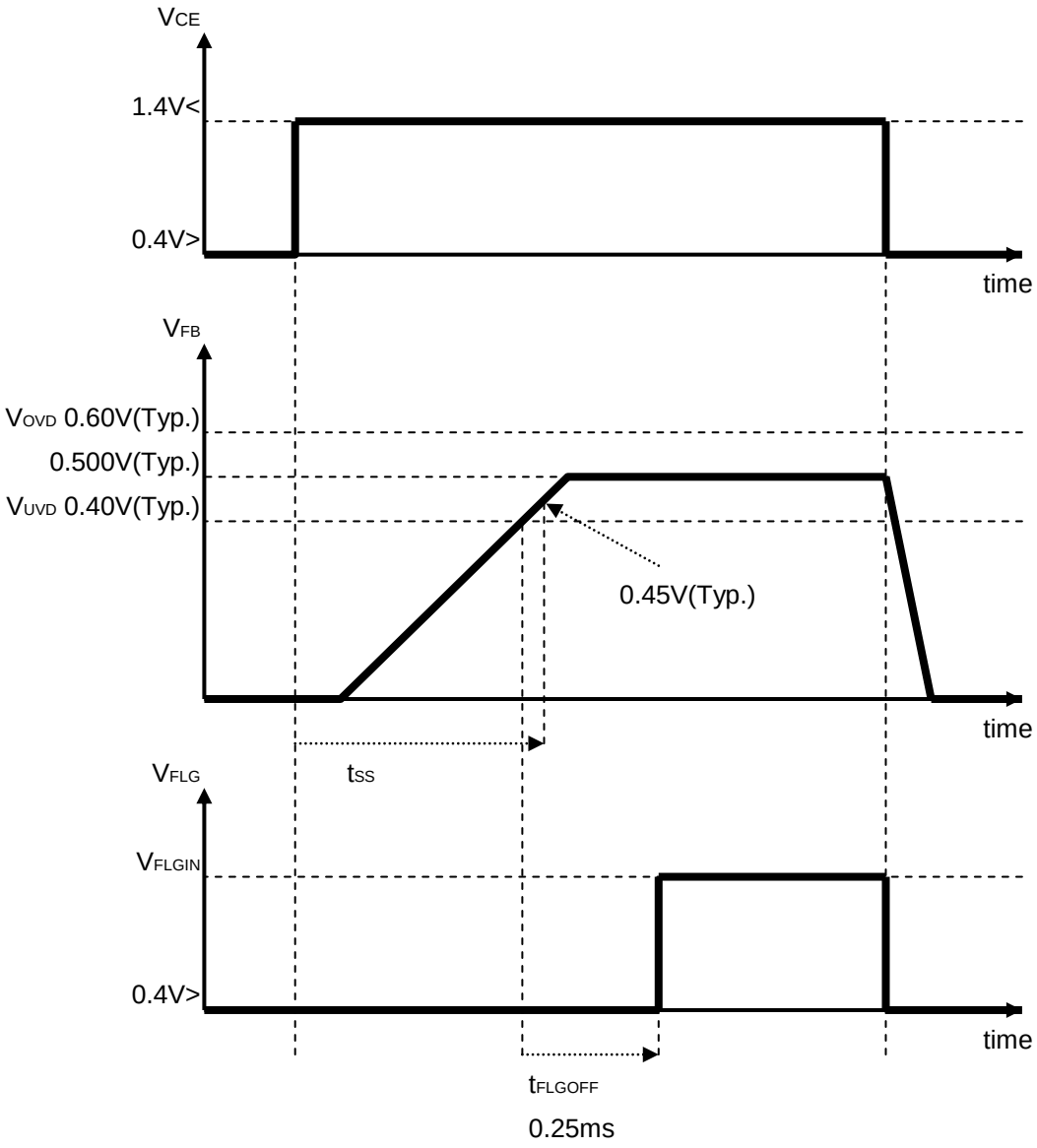
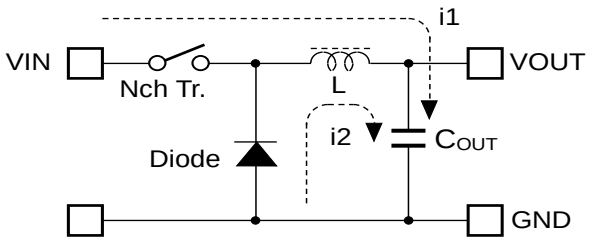


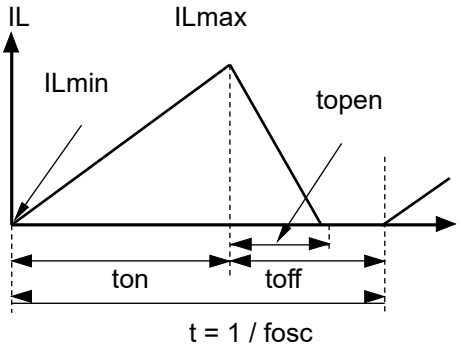
Fig. 2 Flag Function Sequence

OPERATION OF STEP-DOWN DC/DC CONVERTER AND OUTPUT CURRENT

The step-down DC/DC converter stores energy in the inductor (L) when the LX transistor turns on, and releases energy from L when the LX transistor turns off. This is why it can control with less energy loss and provide a lower output voltage (V_{OUT}) than the input voltage (V_{IN}). The operation of the step-down DC/DC converter is explained in the following figures.



Basic Circuit



Inductor Current flowing through Inductor

Step 1. The Nch transistor turns on and the inductor current (i1) flows, L is charged with energy. At this moment, i1 increases from the minimum inductor current (ILmin), which is 0 A, and reaches the maximum inductor current (ILmax) in proportion to the on-time period (ton) of the Nch transistor.

Step 2. When the Nch transistor turns off, L tries to maintain IL at ILmax, so L turns the diode on and the inductor current (i2) flows into L.

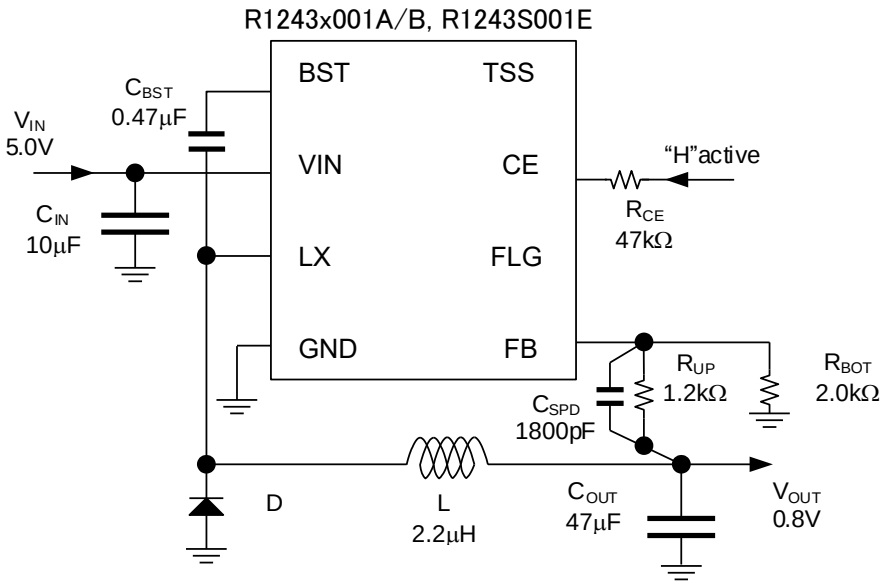
Step 3. i2 decreases gradually and reaches ILmin after the open-time period (topen) of the Nch transistor, and then the diode turns off. This is called discontinuous current mode.
As the output current (I_{OUT}) increases, the off-time period (toff) of the Nch transistor runs out before IL reaches ILmin. The next cycle starts, and the Nch transistor turns on and the diode turns off, which means IL starts increasing from ILmin. This is called continuous current mode.

In the case of PWM mode, V_{OUT} is maintained by controlling ton. During PWM mode, the oscillator frequency (fosc) is being maintained constant.

APPLICATION INFORMATION

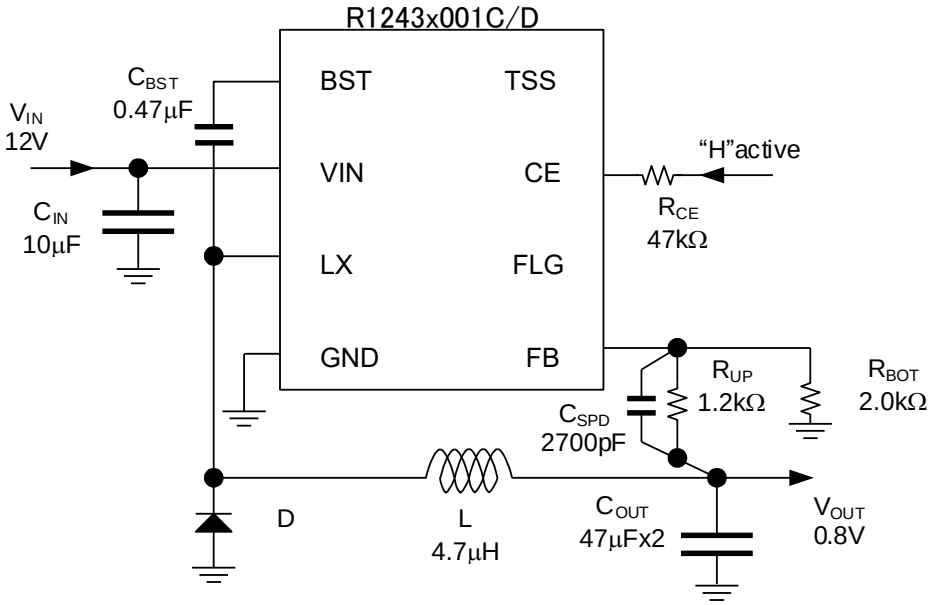
TYPICAL APPLICATION CIRCUIT

V_{OUT} = 0.8 V, t_{SS} = 0.4 ms



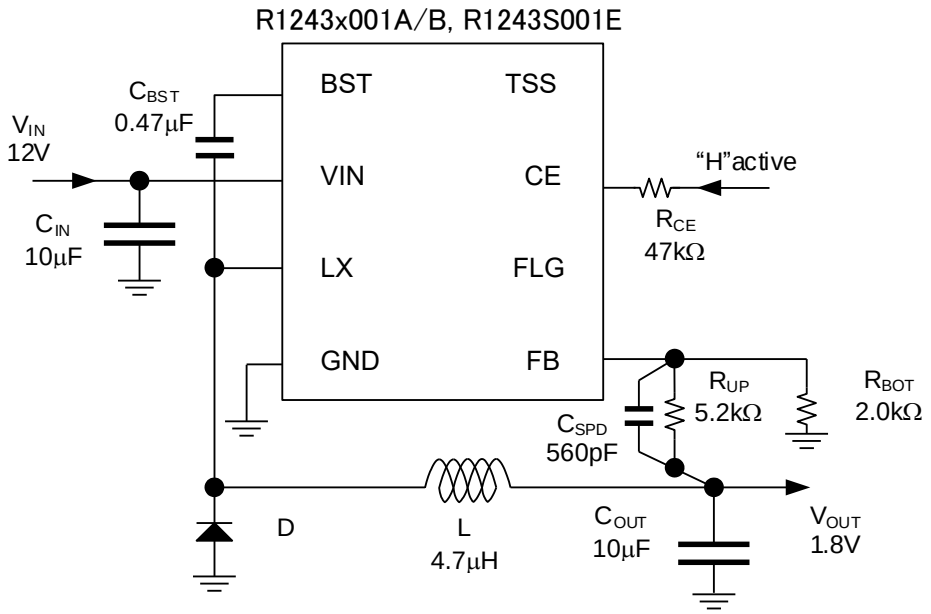
R1243x001A/B/E Typical Application

V_{OUT} = 0.8 V, t_{SS} = 0.4 ms



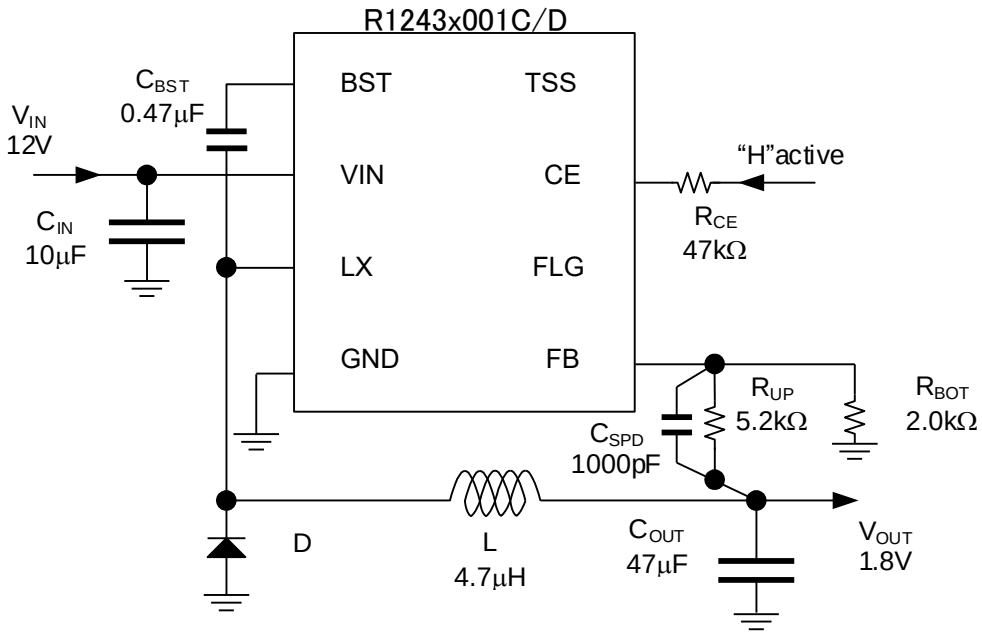
R1243x001C/D Typical Application

V_{OUT} = 1.8 V, t_{SS} = 0.4 ms



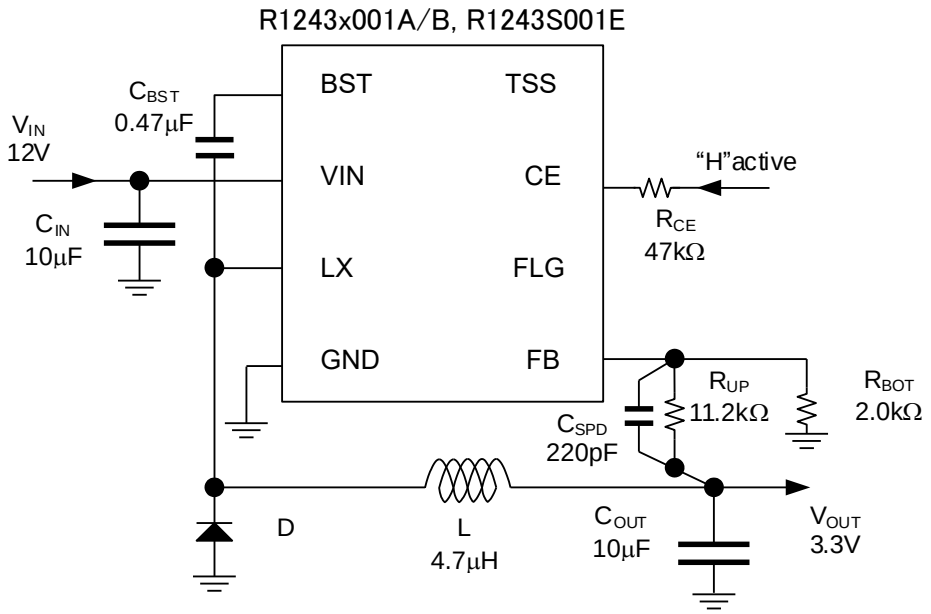
R1243x001A/B/E Typical Application

V_{OUT} = 1.8 V, t_{SS} = 0.4 ms



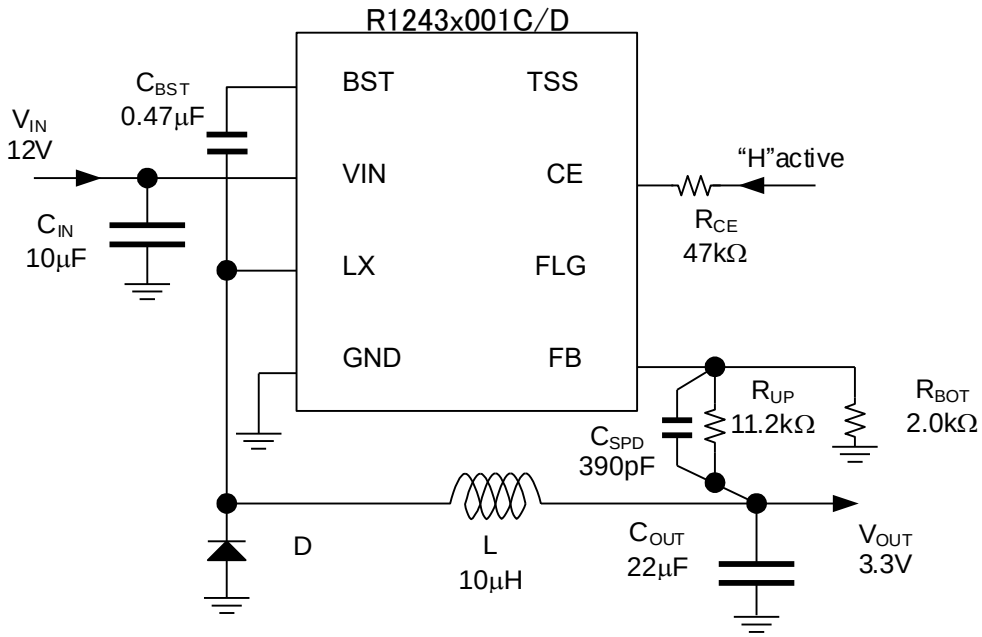
R1243x001C/D Typical Application

V_{OUT} = 3.3 V, t_{SS} = 0.4 ms



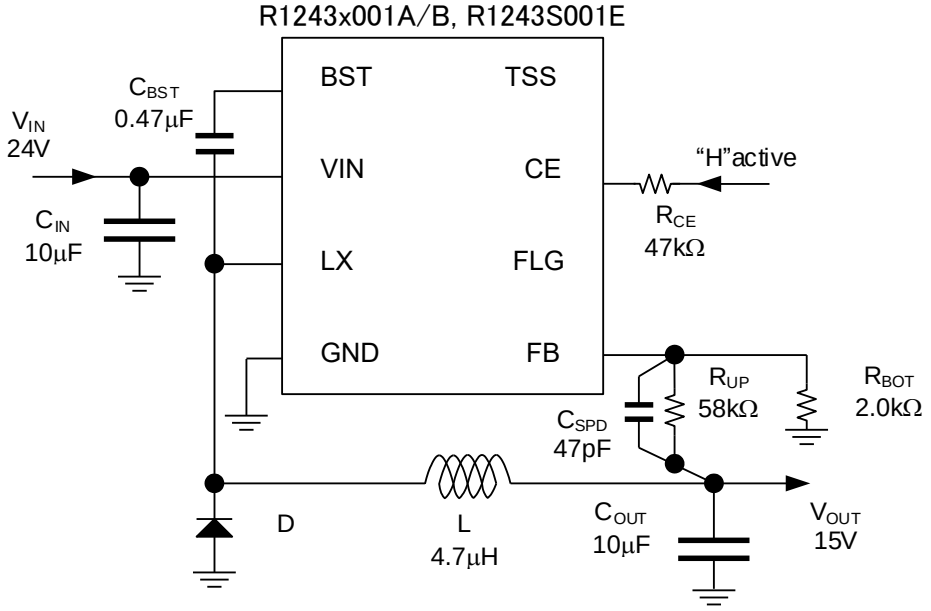
R1243x001A/B/E Typical Application

V_{OUT} = 3.3 V, t_{SS} = 0.4 ms



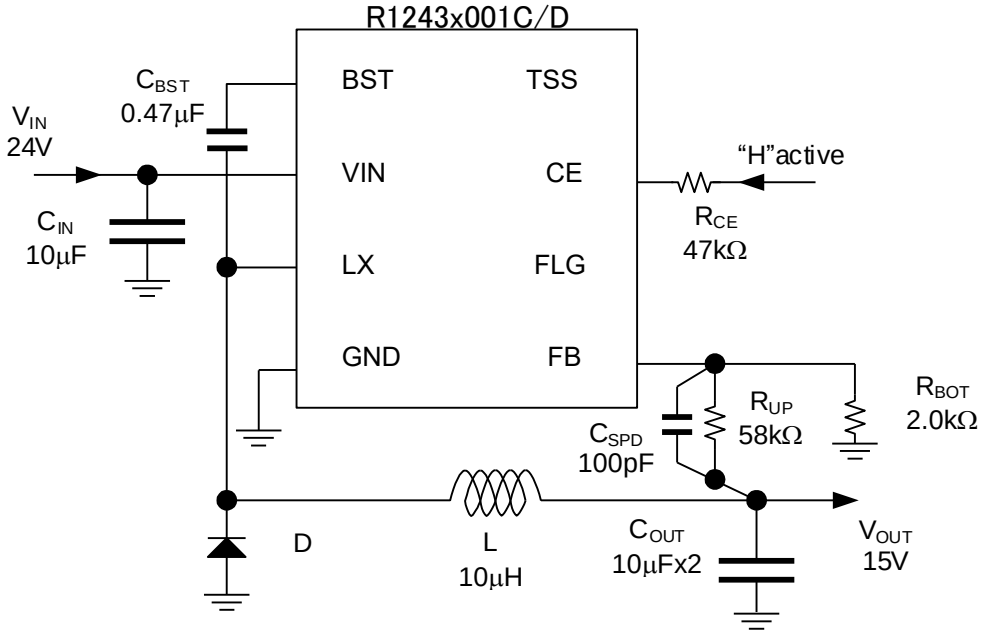
R1243x001C/D Typical Application

V_{OUT} = 15 V, t_{SS} = 0.4 ms



R1243x001A/B/E Typical Application

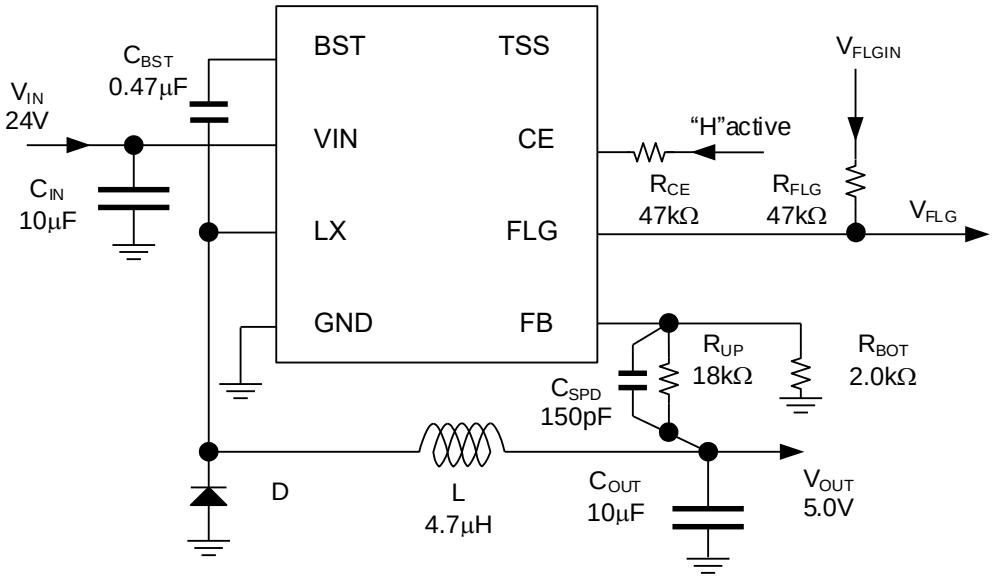
V_{OUT} = 15 V, t_{SS} = 0.4 ms



R1243x001C/D Typical Application

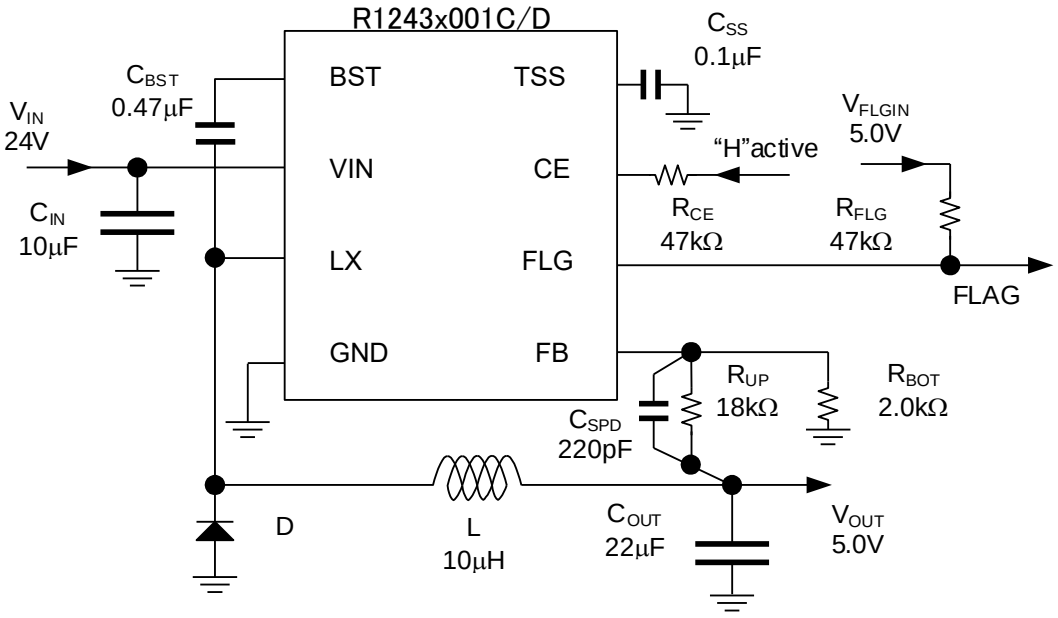
R1243K is the discontinued product.

V_{OUT} = 5.0 V, t_{SS} = 0.4 ms, Flag Function Using
R1243x001A/B, R1243S001E



R1243x001A/B/E Typical Application

V_{OUT} = 5.0 V, t_{SS} = 12 ms, Flag Function Using



R1243x001C/D Typical Application

The R1243x includes a flag output function using Nch open drain. If an abnormal state is detected, the flag output function turns the Nch transistor on and switches the FLG pin low. After recovering from the abnormal state, the flag output function turns the Nch transistor off and switches the FLG pin high after recovering from the low voltage detection (Typ. 0.4 V) and waiting for the delay time (Typ. 0.25 ms).

If V_{OUT} is used as V_{FLGIN}, the FLG pin high voltage (V_{FLGH}) will be same voltage level as V_{OUT} even before the completion of soft-start. When using the soft-start time adjustment in the sequential startup circuits, note that V_{FLGH} is dependent on V_{FLGIN} (connecting to V_{OUT} directly or using other voltage source).

- CE = "L" (Shutdown)
- UVLO (Shutdown)
- Thermal Shutdown
- VFB Overvoltage Detection (Typ. 0.6 V)
- VFB Undervoltage Detection (Typ. 0.4 V)
- Active Latch Function (R1243x001A/C/E)
- Overvoltage Protection for the TSS pin after the completion of soft-start (Typ. 3 V)

SEQUENTIAL START-UP

The figure below shows the example of sequential startup circuits using soft-start time adjustment and flag functions. Where: the input voltage is 12 V, the output voltage of the R1243x001A/B/E (DCDC1) is 5.0 V, the output voltage of the R1243x001A/B/E (DCDC2) is 3.3 V, the electrolytic capacitor for the 5.0 V output is 470 µF and the electrolytic capacitor for the 3.3 V output is 100 µF. The DCDC1 circuit starts up first followed by the DCDC2 circuit, so that the output voltage of DCDC1 will not drop below the output voltage of the DCDC2.

Soft-start Time and Charging Current

During the soft-start, the R1243x generates a charging current (I_{CHRG}) for a capacitor connected to V_{OUT} in addition to the output current (I_{OUT}) for supplying the output load. Therefore, I_{OUT} is given by:

$I_{OUT}' = I_{OUT} + I_{CHRG} = I_{OUT} + V_{OUT} \times (C_{OUT} + C_L) / t_{SS}$

I_{OUT2}' (DCDC1) and I_{OUT2}' (DCDC2) are given by:

DCDC1: $I_{OUT}' = I_{OUT} + V_{OUT} / (C_{OUT} + C_L) / t_{SS} = I_{OUT} + 5.0\ V \times (10\ \mu F + 470\ \mu F) / 26\ ms = I_{OUT} + 92\ mA$

DCDC2: $I_{OUT2}' = I_{OUT2} + V_{OUT2} / (C_{OUT2} + C_{L2}) / t_{SS} = I_{OUT} + 3.3\ V \times (10\ \mu F + 100\ \mu F) / 2.6\ ms = I_{OUT2} + 140\ mA$

The output current should not exceed 2.0 A even during soft-start.

Using the Output Voltage of DCDC1 as the FLG Pin Voltage of DCDC1

The R1243x includes a flag output function using Nch open drain. If an abnormal condition is detected, the flag output function turns the Nch transistor on and switches the FLG pin low. If an abnormal condition is not detected, the flag output function turns the Nch transistor off and switches the FLG pin high after recovering from the low voltage detection (Min. 0.35 V) and waiting for the delay time (Min. 0.05 ms). If V_{OUT} is used as V_{FLGIN}, the FLG pin high voltage (V_{FLGH}) will be same voltage level as V_{OUT} even before finishing the soft-start. After recovering from the low voltage detection, the lowest V_{FLGH} will be 70% of the set output voltage (V_{SET}).

Using the FLG Pin Voltage of DCDC1 as the CE Pin Input Voltage of DCDC2

The lowest CE pin low voltage (V_{CEL}) is 0.4 V, and the highest CE pin high voltage (V_{CEH}) is 1.4 V. The highest flag pin low voltage (V_{FLGL}) is 0.4 V and the lowest V_{FLGH} of DCDC1 is approximately 3.5 V, so the flag pin voltage (V_{FLG}) can be used as the CE pin input voltage (V_{CE}) of DCDC2.

Auto-discharge using the FLG Pin

The R1243x turns the Nch transistor on and switches the FLG pin low during shutdown. If the FLG pin is switched low, a FLG pin current (I_{FLG}) flows from V_{FLGIN} to the FLG pin resistor (R_{FLG}) and the Nch transistor. Therefore, using V_{OUT} as V_{FLGIN} can discharge the electric charges of a capacitor connected to V_{OUT} during shutdown.

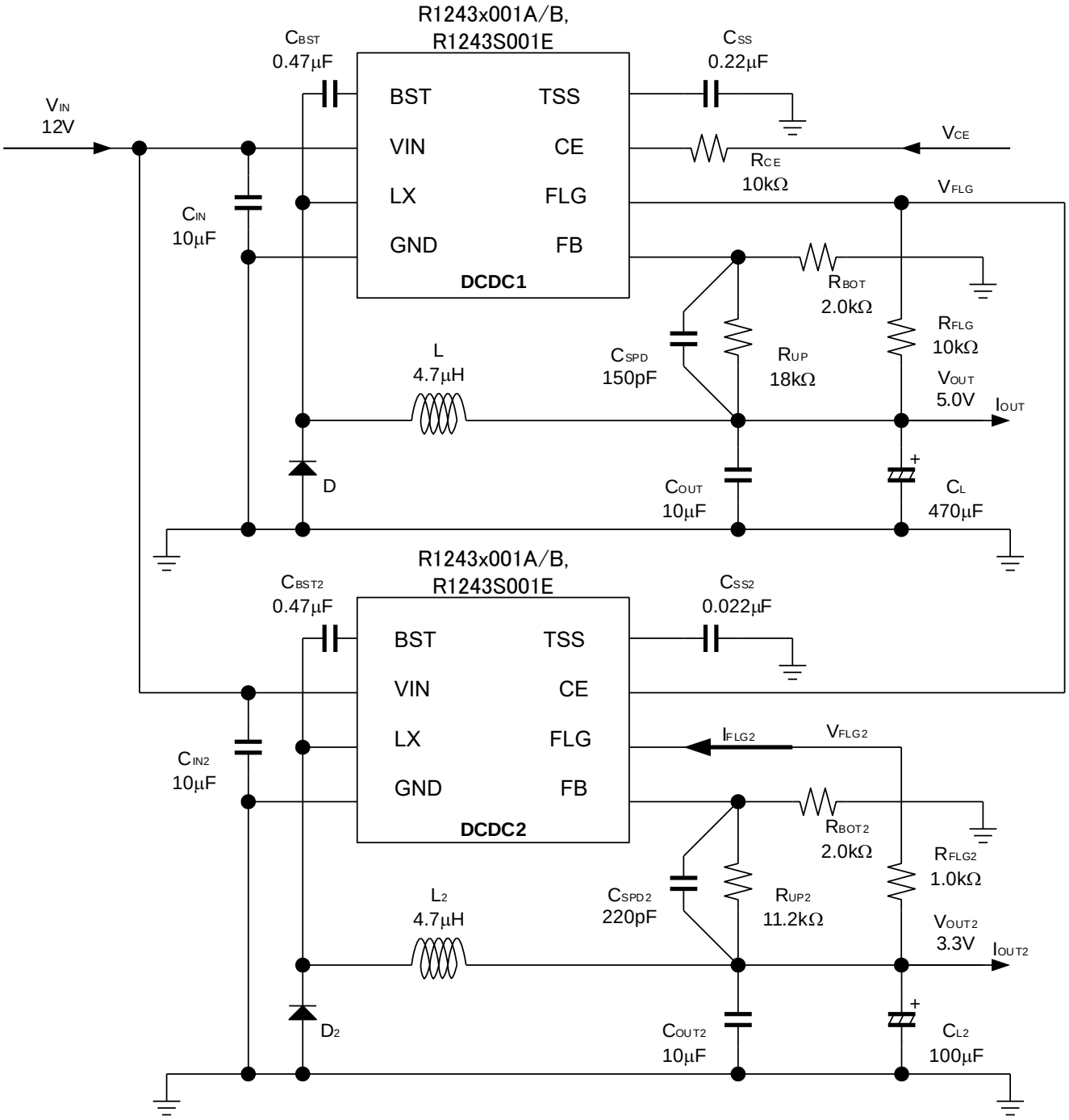
The highest I_{FLG} will be V_{FLGIN} divided by R_{FLG}. When determining the R_{FLG} value, ensure that the highest I_{FLG} will be 5 mA or less. Do not directly connect V_{OUT} to the FLG pin. I_{FLG} may become excessive and damage the device.

V_{FLGL} is regulated as I_{FLG} = 1 mA. If R_{FLG} is set higher than I_{FLG} = 1 mA, the highest V_{FLGL} of 0.4 V is not guaranteed, hence the flag function itself may be spoiled.

Typical Application Circuit with Start-up Sequencing

(DCDC1) R1243x001A/B/E: 1000 kHz, V_{IN} = 12 V, V_{OUT} = 5.0 V, t_{SS} = 26 ms (C_{SS} = 0.22 µF)

(DCDC2) R1243x001A/B/E: 1000 kHz, V_{IN} = 12 V, V_{OUT} = 3.3 V, t_{SS} = 2.6 ms (C_{SS} = 0.022 µF)



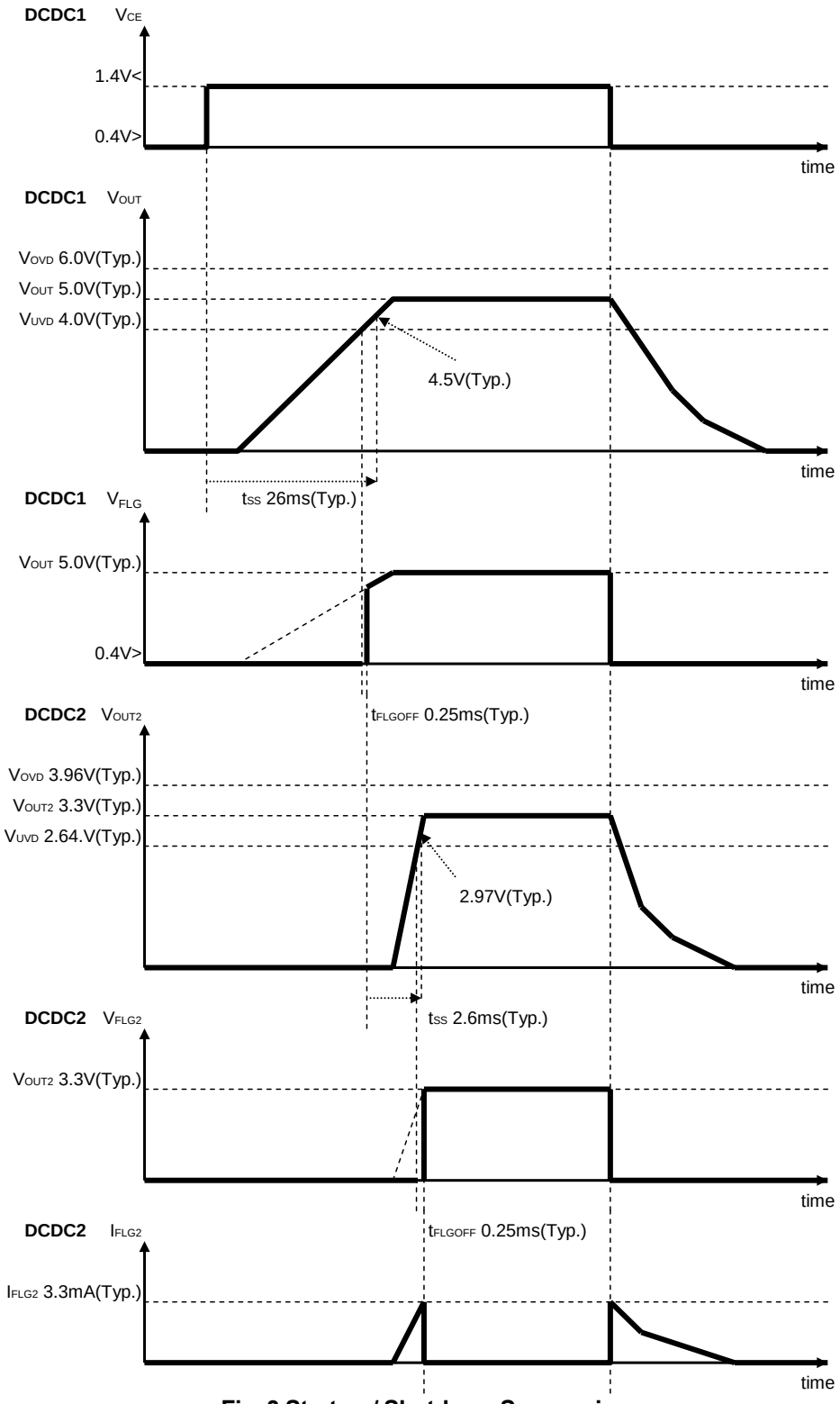


Fig. 3 Start-up/ Shutdown Sequencing

THE MINIMUM ON-TIME

The minimum On-Time of the R1243 Series is set at 150 ns (Typ.). The minimum On-Time (150 ns) is determined by considering the tolerable delay time and the necessary stability of the current sense circuits.

The R1243 Series has adopted the current control mode system, which does not require any sense resistor. By substituting the R_{ON} (Nch driver's on-resistance) value into the following equation, the I_{LX} (Inductor current) value can be obtained: $V_{IN} - V_{LX} = I_{LX} \times R_{ON}$. I_{LX} can be sensed only while the Nch driver is turned on (LX = High period). If the I_{LX} is sensed during the switching surge immediately after the Nch driver is turned on, the switching surge may cause the malfunction. To avoid the malfunction caused by the switching surge, disable the current sensing function of Nch driver for a while immediately after the Nch driver is turned on. While the current sensing function of the Nch driver is disabled, both the current control mode system and the limited current circuit cannot function normally.

Fig. 4 is a graph with the on time on the horizontal axis, and the limit current on the vertical. The graph shows that the delay time is occurred in the limited current circuit within 150 ns because the current sensing is not functioning normally. As a result, the detecting current is increased dramatically. The delay time occurred in the limited circuit current includes the circuit delay time occurred between the current sense circuit and the driver.

This could happen in the current control mode system as well. The current control mode system does not function normally under 150 ns but the operation becomes similar operation to the voltage control mode system that is low stable.

For the above reasons, the stability and the over-current limit accuracy of the R1243 Series degrades dramatically under 150 ns. In the case of setting the minimum on time equal or less than 150 ns, an adequate stability has to be ensured by the external parts and also the over current protection circuit has to be designed without depending on the current limit circuit of the IC.

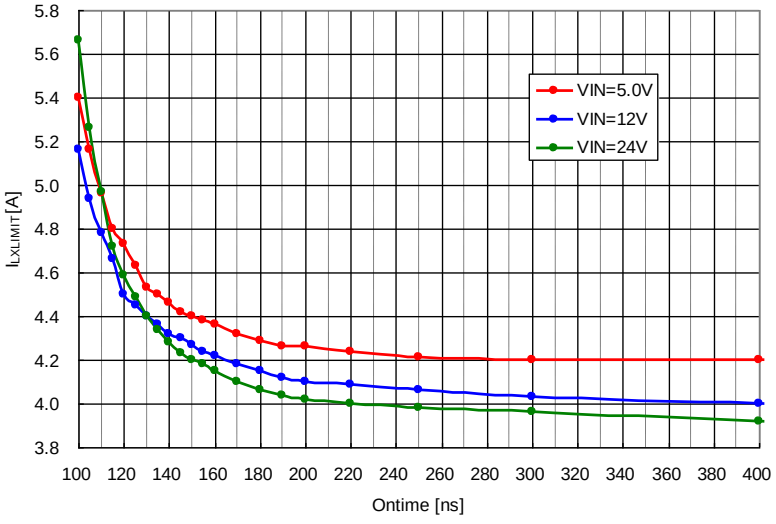


Fig. 4 On-time and Peak Current of Lx pin ($I_{LXLIMIT}$) at Current Limit Detection of Lx pin

OUTPUT CURRENT AND SELECTION OF EXTERNAL COMPONENTS

The following equations explain the relationship between output current and peripheral components.
I_{RP} is the ripple current P-P value, R_{ONH} is the ON resistance of Highside Tr., R_L is the DC resistance of inductor.

First, when Highside Tr. is “ON”, the following equation is satisfied.

$V_{IN} = V_{OUT} + (R_{ONH} + R_L) \times I_{OUT} + L \times I_{RP} / ton$ ..... Equation 1

Second, when Highside Tr. is "OFF" (Diode is "ON"), the following equation is satisfied.

$L \times I_{RP} / toff = V_F + V_{OUT} + R_L \times I_{OUT}$ ..... Equation 2

Put Equation 2 to Equation 1 to solve ON duty of Highside Tr. ($D_{ON} = ton / (toff + ton)$):

$D_{ON} = (V_{OUT} + V_F + R_L \times I_{OUT}) / (V_{IN} + V_F - R_{ONH} \times I_{OUT})$ ..... Equation 3

Ripple Current is given by:

$I_{RP} = (V_{IN} - V_{OUT} - R_{ONH} \times I_{OUT} - R_L \times I_{OUT}) \times D_{ON} / fosc / L$ ..... Equation 4

Peak current (ILmax) that flows through L, and LX Tr. is given by:

$ILmax = I_{OUT} + I_{RP} / 2$ ..... Equation 5

The valley current (ILmin) is given by:

$ILmin = I_{OUT} - I_{RP} / 2$ ..... Equation 6

If ILmin is smaller than 0 ($ILmin < 0$), the step-down DC/DC converter operate in discontinuous mode.

The step--down DC/DC converter operates in discontinuous mode when:

$I_{OUT} < I_{RP} / 2$ ..... Equation 7

It is important to consider ILmax and ILmin when making the input/output conditions or selecting the external components. The above explanation is based on the ideal operation of continuous mode.

Ripple Current and LX Current Limiting

The fluctuation in ripple current of inductor can be caused by various reasons. The R1243x has a LX current limiting that sets the upper limitation of the inductor current (LX peak current limit). Note that the LX peak current limit is not the average inductor current (same as output current value). The larger the ripple current is, the larger the LX peak current will be. The R1243x001B/D is using this characteristic in the fold-back current limiting. The fold-back current limiting maintains the LX peak current limiting and reduces the switching frequency to lower the average inductor current. To release the fold-back current limiting, the LX peak current of the R1243x001B (250 kHz) or the R1243x001D (82.5 kHz) should not go beyond the LX peak current limit. Fig. 5 shows the LX current limit sequencing.

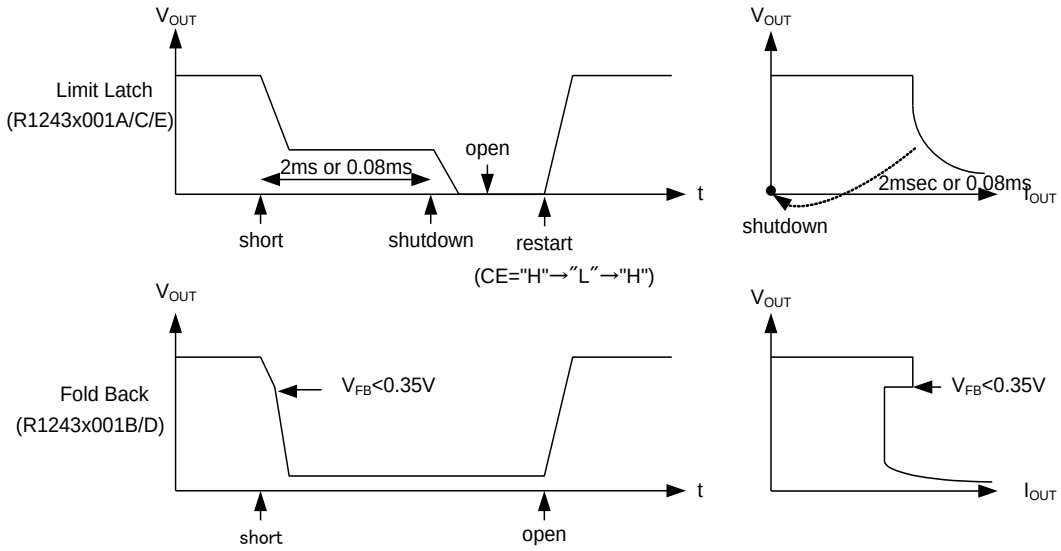


Fig. 5 LX Current Limit Sequencing

Latch Protection for the R1243x001A/C/E

After current limit detection, if a voltage drop continues more than a specified time, the R1243x001A/C/E enables a latch protection to turn off output. Note that if a power voltage rising is slow and the output voltage after soft-start is less than a set output voltage for more than a latch timer period. Refer to *TECHNICAL NOTES* for details.

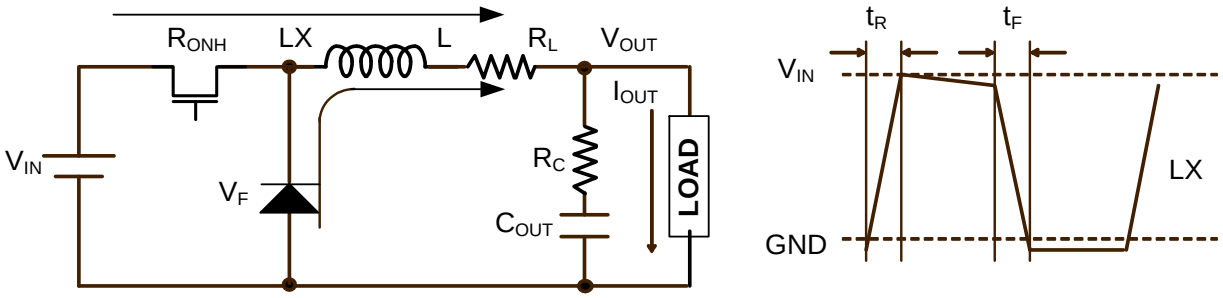
Fold-back Protection for the R1243x001B/D

The R1243x00B/D enables a fold-back protection after soft-start. The fold-back protection reduces the oscillator frequency to 1/4 if the output voltage drops to 70% (Typ.) or less of a set output voltage, which means the FB pin voltage is typically 0.35 V or less. If an oscillator frequency decreases, a ripple current increases. As shown in Equation 8, with LX current limiting, the average current decreases as the ripple current increases.

$I_{OUT} = I_{Lmax} - I_{RP} / 2$ ……Equation 8

Once the fold-back protection is enabled during heavy load, the R1243x may not be able to return to normal operation due to the increased ripple current. Note that if a power voltage rising is slow and the output voltage drops 70% (typ.) or less of a set output voltage after soft-start. Refer to *TECHNICAL NOTES* for details.

POWER LOSS AND EFFICIENCY



Nch High-side Tr. Turn-on Loss: $P_{ON} = R_{ONH} \times I_{OUT}^2 \times Onduty$

Nch High-side Tr. Switching Loss: $P_F = (t_R + t_F) / 2 \times V_{IN} \times I_{OUT} \times f_{OSC}$

Diode Loss: $P_{OFF} = V_F \times I_{OUT} \times Offduty$

Inductor Conduction Loss: $P_L = R_L \times I_{OUT}^2$

IC's Consumption Current Loss: $P_D = V_{IN} \times I_{SS}$

Inductor's Ripple Current Loss: $P_{PP} = 1 / 4 \times R_C \times I_{RP}^2$

Efficiency $\eta = (V_{OUT} \times I_{OUT}) / ((V_{OUT} \times I_{OUT}) + P_{ON} + P_F + P_{CL} + P_D + P_{PP}) \times 100\%$

P_{ON}, P_F and P_D are power losses in the ICs. These power losses are converted into heat inside the IC. Using the following equation, ensure that the junction temperature does not rise above 125°C:

$Tj = \theta ja \times (P_{ON} + P_F + P_D) + Ta < 125°C$

TECHNICAL NOTES ON SHUTDOWN USING INPUT VOLTAGE CONTROL

If the CE pin is enabled without switching the CE pin status, which means connecting the CE pin to the VIN pin, while a set output voltage (V_{SET}) is higher than the UVLO detection threshold (typ. 3.8 V), the input/output ratio may exceed the maximum duty ratio at shutdown. If the input/output ratio exceeds the maximum duty ratio, the output voltage drops and if the input/output ratio falls below the maximum duty ratio, the output voltage rises. These voltage fluctuations generate oscillating waveforms at shutdown.

As shown in Fig. 6, if the input voltage drops before the output voltage drops, a large reverse current may flow. To avoid this, ensure the input voltage is high enough before switching the CE pin status low, or otherwise add a discharge circuit.

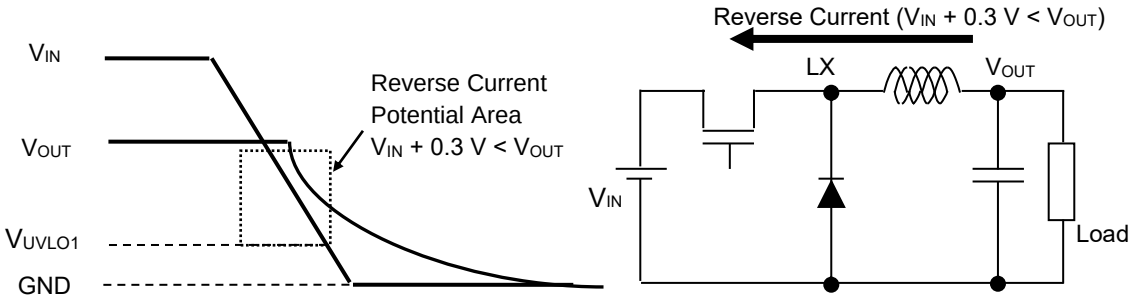


Fig. 6 Shutdown Using Input Voltage Control

TECHNICAL NOTES

- External components have to be connected as close as possible to the IC and have to be wired as short as possible. Especially, the capacitor connected between V_{IN} and GND pin must be wired the shortest. If the impedances of the power supply line and the GND line are high, the operation can be unstable due to the switching current, which fluctuates the power line of the inside the IC. The impedances of power supply line and GND line must be as low as possible. It is necessary to give careful consideration to the large current flowing into the power supply, GND, LX, V_{OUT} and inductor when designing their wirings. The wiring of output voltage setting resistance (R_{UP}) and the wiring of inductor must be separated from load wiring.
- The capacitors to be used in the R1243x must be low ESR ceramic capacitors. The C_{IN} capacitor between V_{IN} and GND should be equal or more than 10 μF. Please pay attention to the bias-dependent properties and the temperature variability characteristics of the ceramic capacitors.
- The internal phase compensation of this IC is designed within the recommended values of inductor and C_{OUT} ceramic capacitor. If the inductor value is small, the peak values of the switching current increase along with the load current. When the peak value of the switching current reaches to the current limit, the over current protection circuit may start to function.
- If the parasitic capacitance of the schottky diode is large, the operation may result in unstable because of the large switching current when the switch is turned on. Please use the schottky diode with 100 pF or less when the reverse voltage is 10 V. If the Schottky diode with large parasitic capacitance is used, excessive switching current may flow when the switch is turned on, which may cause the IC to become unstable. If the parasitic capacitance of the Schottky diode exceeds 100 pF or is unknown, confirm that there are no problems with the load regulation, the line regulation, or the load transient response characteristics before using it. If a diode with a small current rating and a large Vf is used, the LX terminal voltage may exceed the negative MAXIMUM rating when the V_{OUT} is shorted, depending on the configuration of the peripheral circuit, and the IC may be damaged. This depends on the short-circuit conditions, other peripheral components, and the board layout, but please be especially careful when using a diode with a Vf value of more than 0.7V at 4-5A.
- If the V_{OUT} Terminal is shorted under high input voltage conditions, the limit current value may become significantly larger. (Refer to "THE MINIMUM ON-TIME" page) In the case, we recommended the foldback protection version or a version with a frequency of 330KHz. Also, please take external measures for current protection such as using a fuse, as necessary.
- The output voltage (V_{OUT}) can be calculated by this equation: $V_{OUT} = V_{FB} \times (R_{UP} + R_{BOT}) / R_{BOT}$. By changing R_{UP} and R_{BOT}, the output voltage (V_{OUT}) is adjustable. If resistance values of R_{UP} and R_{BOT} are high, the impedance of the FB pins become high, and the IC becomes vulnerable to an influence of noise. R_{BOT} is recommended to be between 1.0 kΩ to 4.7 kΩ. If the operation become unstable due to the high impedance, it is important to consider lowering the impedance.
- In the IC, ESD protection diode is connected between CE pin and V_{IN} pin. If there is a possibility that the CE pin voltage becomes higher than the V_{IN} pin voltage, it is recommended to insert a 10 kΩ resistance or more in order to prevent the large current flowing from CE pin into V_{IN} pin.
- Connect the reverse side of the IC pad to GND. To improve the radiation of heat of the multiple-layered board, it is effective to make the via on the connection part of the reverse side of the IC pad to release the heat to multiple layers.
- The flag resistor (R_{FLG}) is recommended to be between 10 kΩ to 100 kΩ. If the flag function is not used, FLG pin has to be left open or connected to GND.

- If the soft-start time adjustment function is not used, TSS pin must be left open. In this case, soft-start time is set as 0.4 ms (Typ.).
- After the completion of the soft-start, latch function (R1243x001A/C/E) starts to function. The internal counter starts counting when the overcurrent protection circuits runs the current limit detection. When the internal counter counts up to 2 ms typically (R1243x001A/C) or up to 0.08 ms (R1243x001E), latch function turns off the output. The turned off output can be reset when CE pin is changed to "L", and also V_{IN} pin voltage became less than 3.8 V typically, which is UVLO detecting voltage. If the output voltage becomes more than the setting voltage (FB pin voltage is 0.50 V typically within the latch timer period, the counter restores the default. Therefore, the careful attention is required when the power-supply voltage's start-up is slow and the output voltage is not reached to the setting voltage within the latch timer period after the completion of the soft-start.
- After the completion of the soft-start, fold-back function (R1243x001B/D) starts to function. The fold-back function limits the oscillation frequencies into 1/4 when FB pin voltage becomes less than 0.35 V (Typ.). Therefore, the careful attention is required when the power-supply voltage's start-up is slow and the output voltage is not reached to the 70% (Typ.) of the setting voltage even for a short period of time after the completion of the soft-start.
- The quality of the power supply circuit using the R1243x largely depends on the external components. The careful attention is required for the external component parameters.
- The careful attention is required for the maximum ratings (voltage, current, and wattage) of the external components, board layout pattern and the IC.
- The table on the next page shows the recommended values for setting output voltage.

Table 1. R1243x Recommended Value for Each Output Voltage

R1243x001A/B/E: 1000 kHz

V_{IN}	V_{OUT}	L [µH]	C_{OUT} [µF]	C_{SPD}	C_{BST} [µF]	R_{BOT} [kΩ]
4.5 ≤ V_{IN} ≤ Max	0.8 ≤ V_{OUT} ≤ 1.2	2.2	47	*1	0.47	2.0
4.5 ≤ V_{IN} ≤ Max	1.2 ≤ V_{OUT} ≤ 1.8	2.2	22	*1	0.47	2.0
4.5 ≤ V_{IN} ≤ Max	1.8 ≤ V_{OUT} ≤ 2.5	4.7	10	*1	0.47	2.0
4.5 ≤ V_{IN} ≤ 6	2.5 ≤ V_{OUT} ≤ Maxduty	4.7	22	open	0.47	2.0
6 ≤ V_{IN} ≤ Max	2.5 ≤ V_{OUT} ≤ 5	4.7	10	*1	0.47	2.0
Min ≤ V_{IN} ≤ Max	5 ≤ V_{OUT} ≤ Maxduty	4.7	10	*1	0.47	2.0

R1243x001C/D: 330 kHz

V_{IN}	V_{OUT}	L [µH]	C_{OUT} [µF]	C_{SPD}	C_{BST} [µF]	R_{BOT} [kΩ]
4.5 ≤ V_{IN} ≤ 7.5	0.8 ≤ V_{OUT} ≤ 1.2	4.7	47×2	open	0.47	2.0
4.5 ≤ V_{IN} ≤ 7.5	1.2 ≤ V_{OUT} ≤ Maxduty	10	47×2	open	0.47	2.0
7.5 ≤ V_{IN} ≤ Max	0.8 ≤ V_{OUT} ≤ 1.2	4.7	47×2	*2	0.47	2.0
7.5 ≤ V_{IN} ≤ 12	1.2 ≤ V_{OUT} ≤ 2.5	10	47	*2	0.47	2.0
7.5 ≤ V_{IN} ≤ Max	1.2 ≤ V_{OUT} ≤ 2.5	4.7	47	*2	0.47	2.0
7.5 ≤ V_{IN} ≤ Max	2.5 ≤ V_{OUT} ≤ 5	10	22	*2	0.47	2.0
7.5 ≤ V_{IN} ≤ Max	5 ≤ V_{OUT} ≤ 18	10	10×2	*2	0.47	2.0

***1 R1243x001A/B/E: 1000 kHz**

V_{OUT} [V]	C_{SPD} [pF]	R_{UP} [kΩ]	R_{BOT} [kΩ]
0.8	1800	1.2	2.0
1	1200	2.0	2.0
1.2	1000	2.8	2.0
1.5	820	4.0	2.0
1.8	560	5.2	2.0
2.5	390	8.0	2.0
3.3	220	11.2	2.0
5	150	18.0	2.0
6	120	22.0	2.0
9	82	34.0	2.0
12	56	46.0	2.0
15	47	58.0	2.0
18	47	70.0	2.0

***2 R1243x001C/D: 330 kHz**

V_{OUT} [V]	C_{SPD} [pF]	R_{UP} [kΩ]	R_{BOT} [kΩ]
0.8	2700	1.2	2.0
1	2200	2.0	2.0
1.2	1500	2.8	2.0
1.5	1200	4.0	2.0
1.8	1000	5.2	2.0
2.5	560	8.0	2.0
3.3	390	11.2	2.0
5	220	18.0	2.0
6	180	22.0	2.0
9	150	34.0	2.0
12	100	46.0	2.0
15	100	58.0	2.0
18	100	70.0	2.0

Table 2. R1243x Recommended External Components

C_{IN}	V_{IN}	Cap.	Spec.	Part Name	Manufacturer
	≤ 12.5 V	10 µF	25 V	GRM31CR71E106K	Murata
	≤ 12.5 V	10 µF	25 V	CM316X5R106K25ABH	Kyocera
	All	10 µF	50 V	UMK325BJ106MM-P	Taiyo Yuden
	All	10 µF	50 V	CGA6P3X7S1H106K	TDK

C_{OUT}	V_{OUT}	Cap.	Spec.	Part Name	Manufacturer
	≤ 8 V	47 µF	16 V	GRM32EB31C476KE15	Murata
	≤ 5 V	22 µF	10 V	GRM31CR71A226M	Murata
	≤ 12.5 V	10 µF	25 V	GRM31CR71E106K	Murata
	≤ 8 V	22 µF	16 V	CM316X5R226K16AB	Kyocera
	≤ 12.5 V	22 µF	25 V	CM32X5R226M25AB	Kyocera
	≤ 12.5 V	10 µF	25 V	CM316X5R106K25ABH	Kyocera
	All	10 µF	50 V	UMK325BJ106MM-P	Taiyo Yuden
	All	10 µF	50 V	CGA6P3X7S1H106K	TDK

C_{BST}	V_{OUT}	Cap.	Spec.	Part Name	Manufacturer
	all	0.47 µF	16 V	EMK212BJ474KD-T	Taiyo Yuden
	all	0.47 µF	16 V	C1608JB1C474K	TDK

D	V_{IN}	Spec.	Part Name	Manufacturer
	≤ 15 V	15 V, 2A	SBS010M	SANYO
	≤ 15 V	15 V, 2A	SS20015M	SANYO
	all	40 V, 3A	CMS16	TOSHIBA

L	Ind.	Spec.	Part Name	Manufacturer
	2.2 µH	5.4 A	RLF7030T-2R2M5R4	TDK
	4.7 µH	3.4 A	RLF7030T-4R7M3R4	TDK
	10 µH	2.5 A	SLF10145T-100M2R5	TDK
	2.2 µH	2.7 A	NR6020T2R2N	Taiyo Yuden
	4.7 µH	2.6 A	NR6028T4R7M	Taiyo Yuden
	10 µH	2.5 A	NR6045T100M	Taiyo Yuden

TECHNICAL NOTES ON PCB LAYOUT PATTERN

1. The exposed pad on the bottom of the package enhances the thermal performance and is electrically connected to GND inside the package. It is recommended that the exposed pad be connected to the ground plane on the board with thermal vias if possible.

2. Connect shortest possible: “a wiring between the V_{IN} pin of input capacitor (C_{IN}) and the V_{IN} pin of IC” and “a wiring between the GND pin of input capacitor (C_{IN}) and the GND pin of IC”.
   Connect as short as possible: “a wiring among the Lx pin of IC, the Lx pin of diode, the GND pin of diode, and the GND pin of input capacitor (C_{IN})”.
   These are recommended to wire without intermediary of a through hole.

3. Wire the Lx pin short so that the parasitic capacitance would not be provided. It is recommended to implement without intermediary of a through hole.

4. Connect between the GND pin of C_{OUT} and the GND pin of diode as short as possible. It is recommended to wire without intermediary of a through hole.

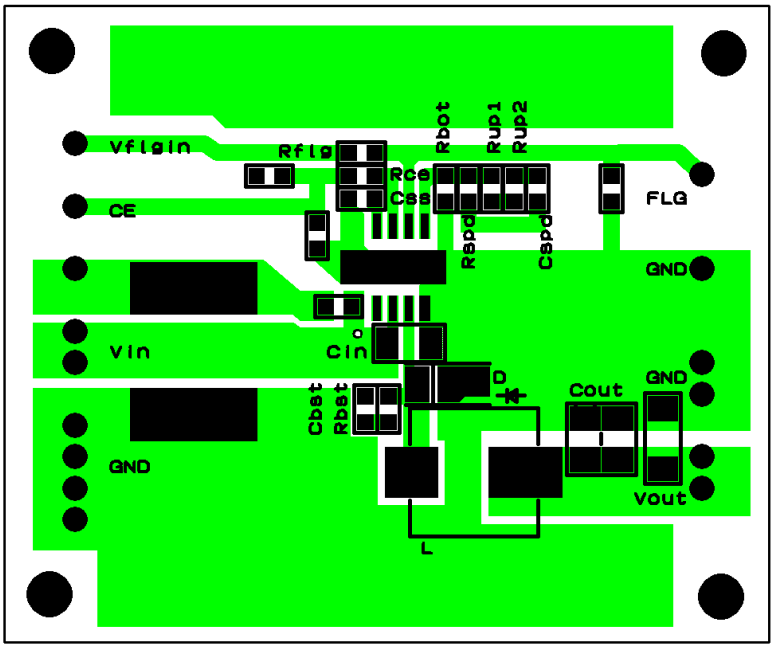
5. The FB pin side of R_{UP}, R_{BOT}, C_{SPD}, and R_{SPD} should be designed to keep a distance from inductor, BST pin, and Lx pin in order to avoid the high impedance and noise effect. These can be wired via through hole.

6. For V_{OUT} wiring to R_{UP}, the feed-back must be made as close as possible from the output capacitor (C_{OUT}). This can be wired via through hole.

7. For the GND wiring to the soft-start time adjusting capacitor (C_{SS}), avoid the current path of parts including input capacitors (C_{IN}) and diodes. This can be wired via through hole.

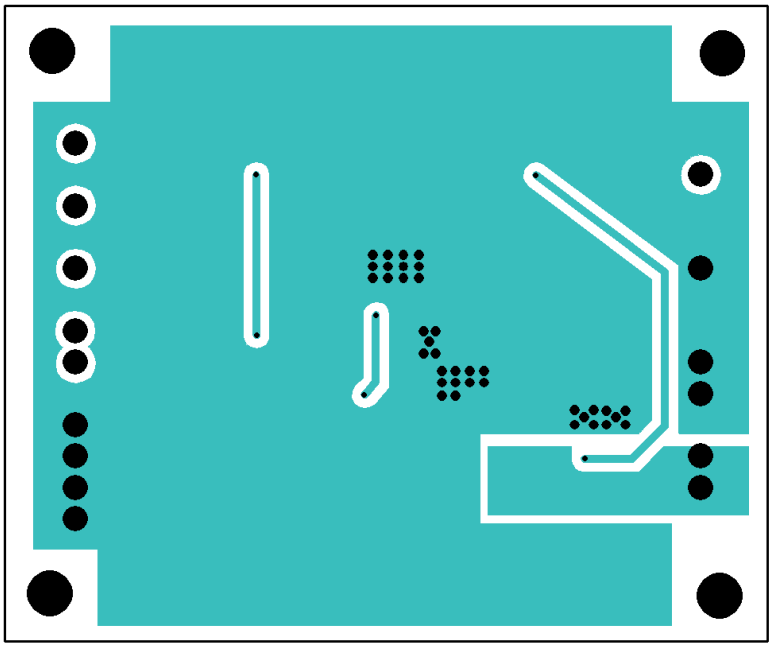
PCB LAYOUT

R1243S001x Evaluation Board TOP VIEW

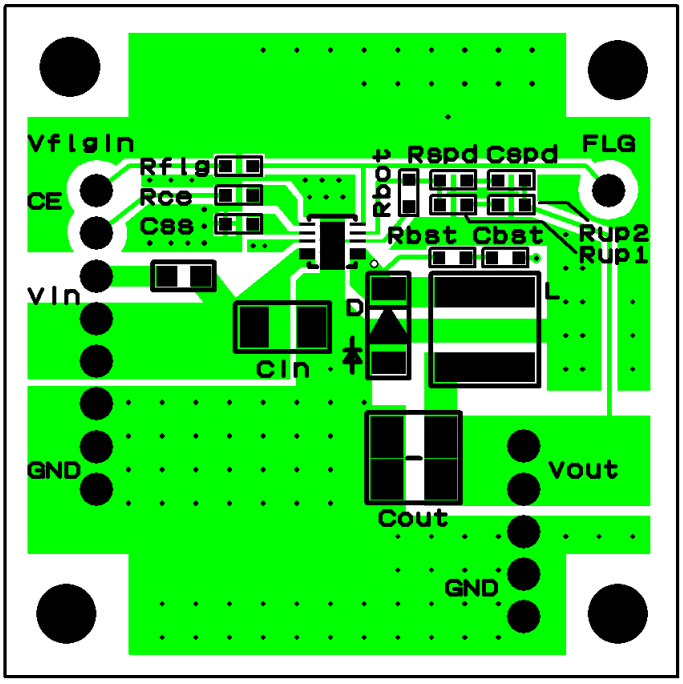


(The broad land of Lx section enables a connection with large inductors and diodes).

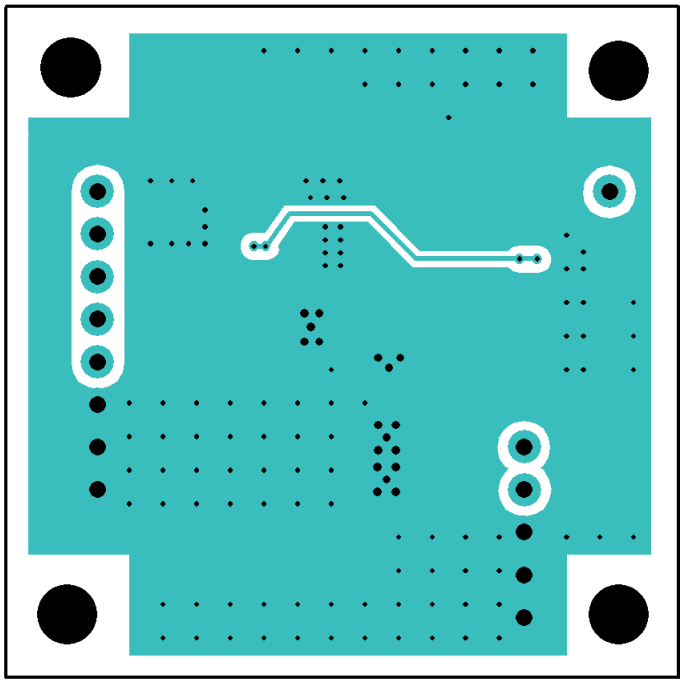
R1243S001x Evaluation Board TOP VIEW



R1243K001x Evaluation Board TOP VIEW



R1243K001x Evaluation Board TOP VIEW

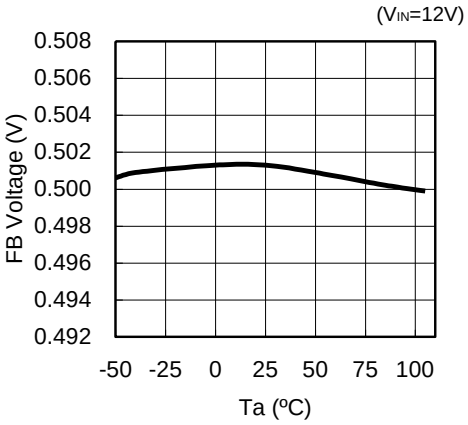


TYPICAL PERFORMANCE CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

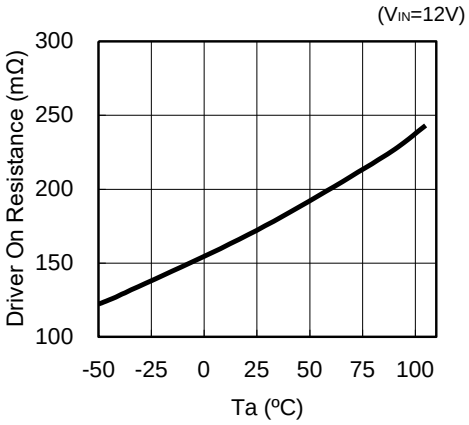
1) FB Voltage vs Temperature

R1243x001x



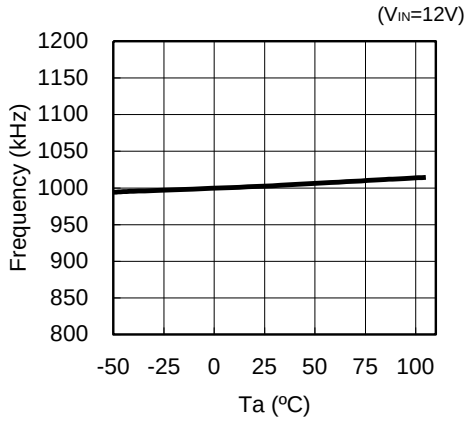
2) Driver On Resistance vs Temperature

R1243x001x



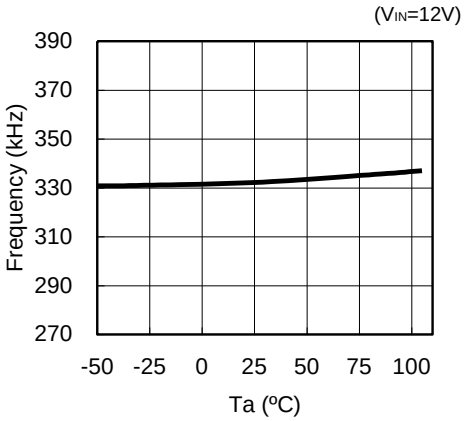
3) Oscillator Frequency vs Temperature

R1243x001A/R1243x001B, R1243S001E



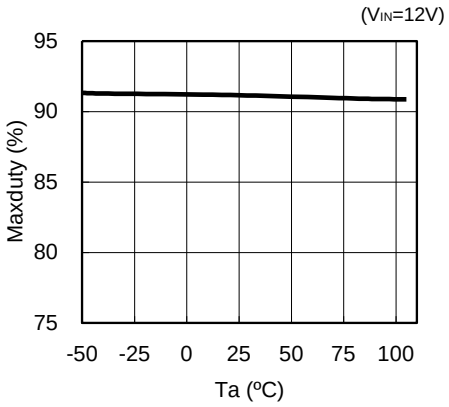
4) Oscillator Frequency vs Temperature

R1243x001C/R1243x001D



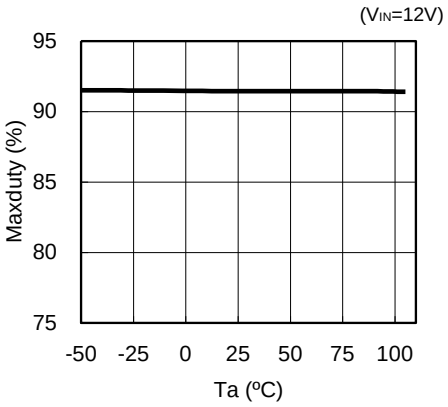
5) Maxduty vs Temperature

R1243x001A/R1243x001B, R1243S001E



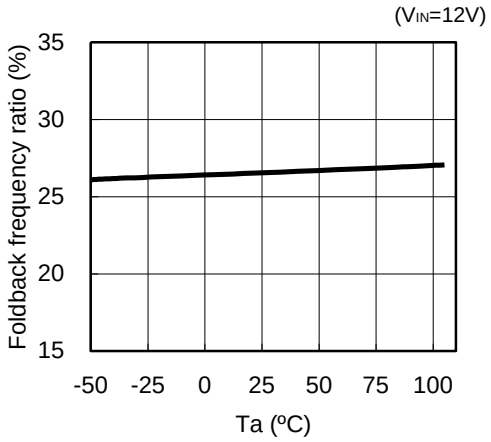
6) Maxduty vs Temperature

R1243x001C/R1243x001D



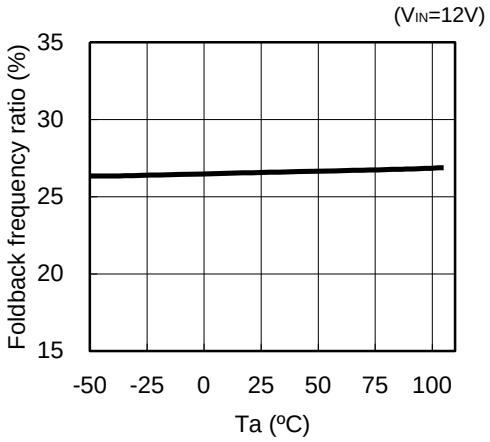
7) Fold-back Frequency vs Temperature

R1243x001A/R1243x001B



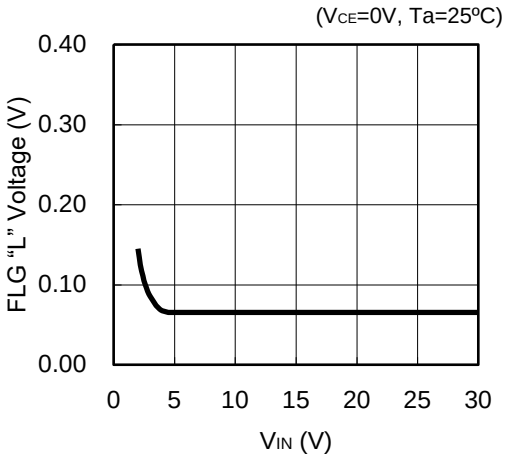
8) Fold-back Frequency vs Temperature

R1243x001C/R1243x001D



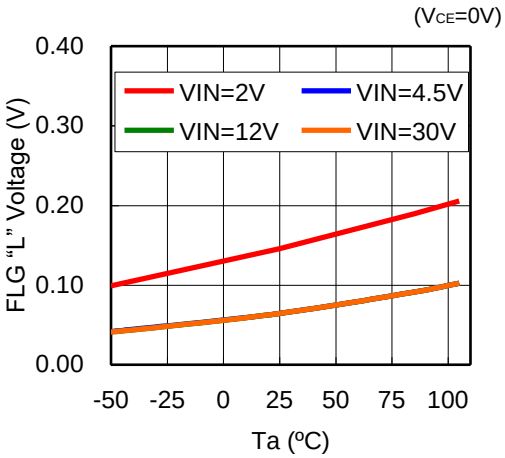
9) FLG Voltage "L" vs. Input Voltage

R1243x001x



10) FLG Voltage "L" vs. Temperature

R1243x001x

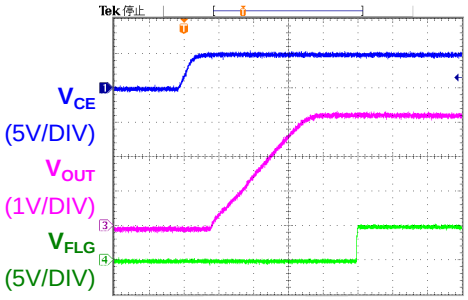


11) Soft-Start Waveform

R1243x001x

t_{SS} = 0.4 ms

($R1243S001A, V_{IN}$ = 12 V, V_{OUT} = 3.3 V, t_{SS} = open, V_{FLGIN} = 5.0 V, R_{OUT} = 3.3 Ω (I_{OUT} = 1.0 A), Ta = 25°C)

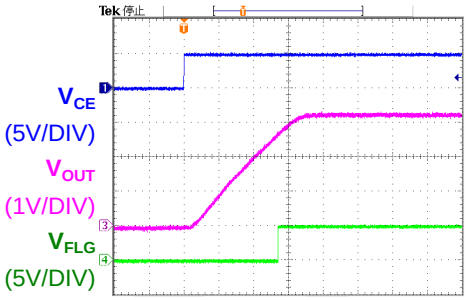


(100µs/DIV)

R1243x001x

t_{SS} = 12 ms

($R1243S001A, V_{IN}$ = 12 V, V_{OUT} = 3.3 V, C_{SS} = 0.1 µF, V_{FLGIN} = 5.0 V, R_{OUT} = 3.3 Ω (I_{OUT} = 1.0 A), Ta = 25°C)

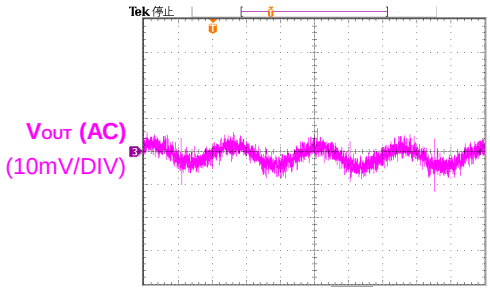


(4ms/DIV)

12) Output Voltage Waveform (AC)

R1243x001A/R1243x001B, R1243S001E

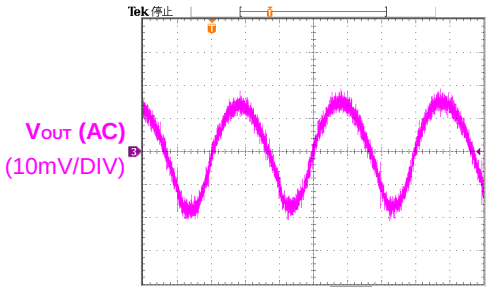
($R1243K001A, V_{IN}$ = 12 V, V_{OUT} = 3.3 V, L = 4.7 µH, C_{OUT} = 10 µF, R_{OUT} = 3.3 Ω (I_{OUT} = 1.0 A), Ta = 25°C)



(400ns/DIV)

R1243x001C/R1243x001D

($R1243K001D, V_{IN}$ = 12 V, V_{OUT} = 3.3 V, L = 10 µH, C_{OUT} = 22 µF, R_{OUT} = 3.3 Ω (I_{OUT} =1.0 A), Ta = 25°C)

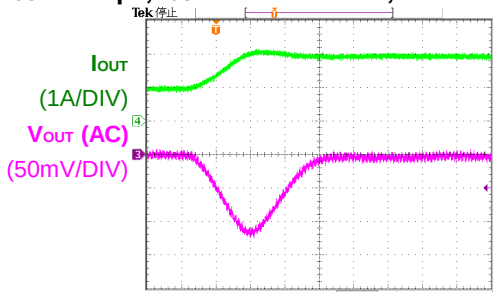


(1µs/DIV)

13) Output Voltage Waveform (AC), Load Transient Response

R1243x001A/R1243x001B, R1243S001E

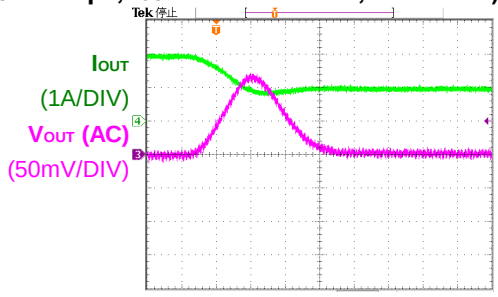
($R1243K001A, V_{IN}$ = 12 V, V_{OUT} = 3.3 V, L = 4.7 µH, C_{OUT} = 10 µF, I_{OUT} = 1.0 A→2.0 A, Ta = 25°C)



(10µs/DIV)

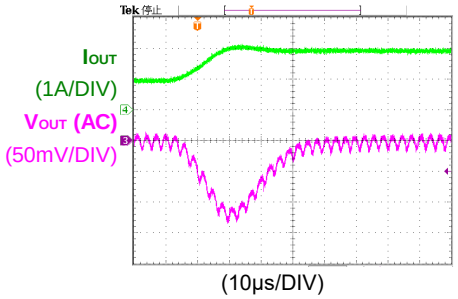
R1243x001C/R1243x001D

($R1243K001A, V_{IN}$ = 12 V, V_{OUT} = 3.3 V, L = 4.7 µH, C_{OUT} = 10 µF, I_{OUT} = 2.0 A→1.0 A, Ta = 25°C)

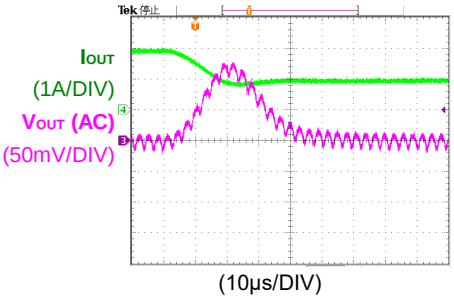


(10µs/DIV)

R1243x001C/R1243x001D
(I_{OUT} = 1.0 A→2.0 A)

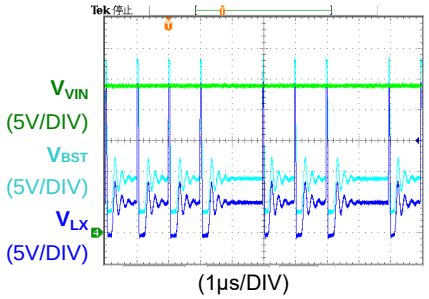


R1243x001C/R1243x001D
(I_{OUT} = 2.0 A→1.0 A)

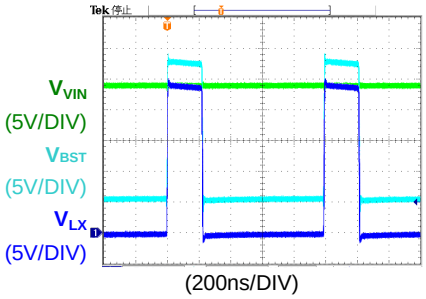


14) Switching Operation Waveform

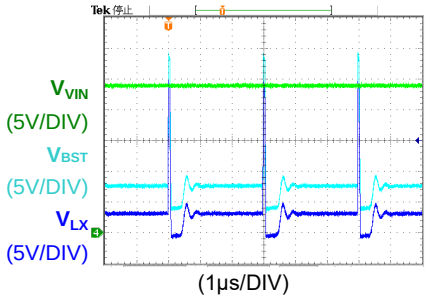
R1243x001A/R1243x001B, R1243S001E
(I_{OUT} = 0 mA)



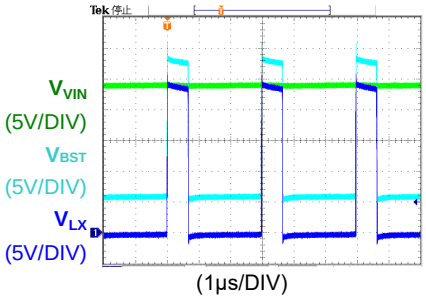
R1243x001A/R1243x001B, R1243S001E
(R_{OUT} = 5.0 Ω (I_{OUT} = 1.0 A))



R1243x001C/R1243x001D
(I_{OUT} = 0 mA)



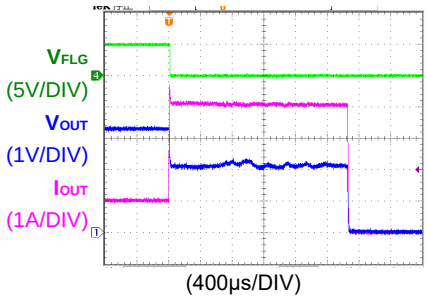
R1243x001C/R1243x001D
(R_{OUT} = 3.3 Ω (I_{OUT} = 1.0 A))



15) Limit-latch Operation Waveform

R1243x001A/R1243x001C

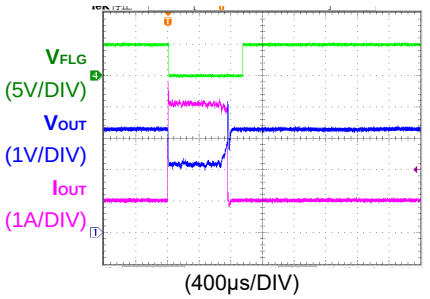
($R1243K001A, V_{IN}$ = 12 V, V_{OUT} = 3.3 V, L = 4.7 µH, C_{OUT} = 10 µF, R_{OUT} = 3.3 Ω→0.5 Ω, Ta = 25ºC)



16) Latch-type Limit Detection Release Waveform

R1243x001A/R1243x001C

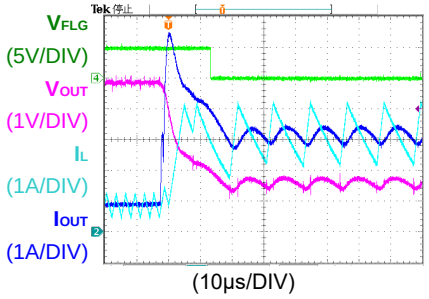
($R1243K001A, V_{IN}$ = 12 V, V_{OUT} = 3.3 V, L = 4.7 µH, C_{OUT} = 10 µF, R_{OUT} = 3.3 Ω→0.5 Ω→3.3 Ω, Ta = 25ºC)



17) Fold-back Operation Waveform

R1243x001B/R1243x001D

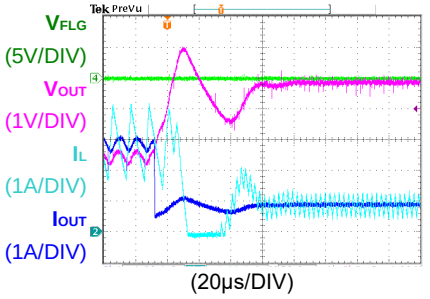
($R1243S001D, V_{IN}$ = 12 V, V_{OUT} = 5.0 V, L = 10 µH, C_{OUT} = 22 µF, R_{OUT} = 5.0 Ω→0.5 Ω, Ta = 25ºC)



18) Fold-back Release Waveform

R1243x001B/R1243x001D

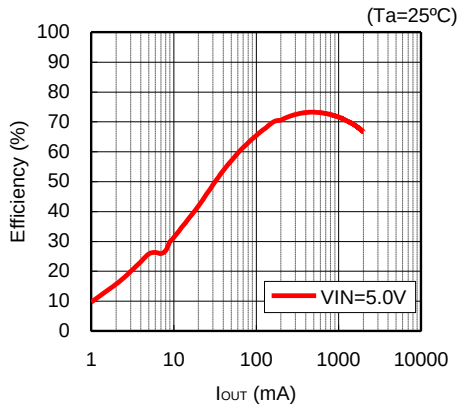
($R1243S001D, V_{IN}$ = 12 V, V_{OUT} = 5.0 V, L = 10 µH, C_{OUT} = 22 µF, R_{OUT} = 0.5 Ω→5.0 Ω, Ta = 25ºC)



19) Output Current vs. Efficiency

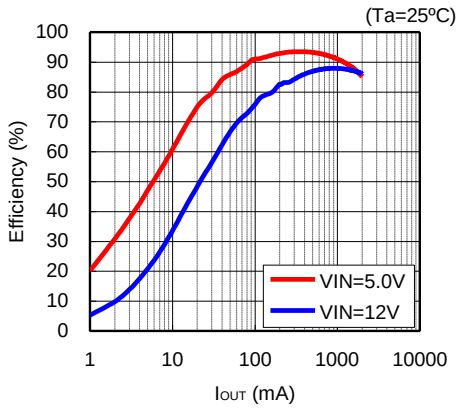
R1243x001A/R1243x001B, R1243S001E

V_{OUT} = 0.8 V



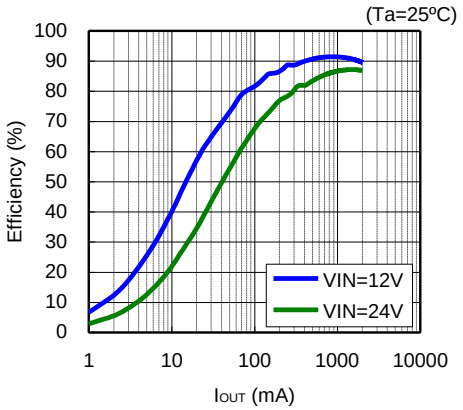
R1243x001A/R1243x001B, R1243S001E

V_{OUT} = 3.3 V



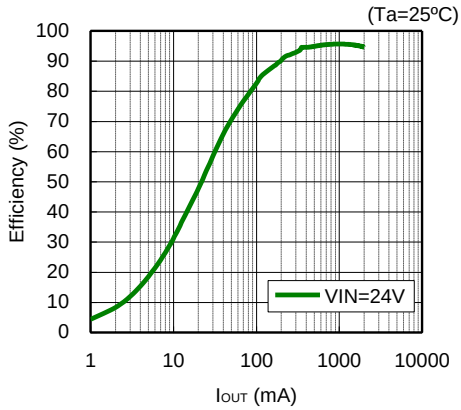
R1243x001A/R1243x001B, R1243S001E

V_{OUT} = 5.0 V



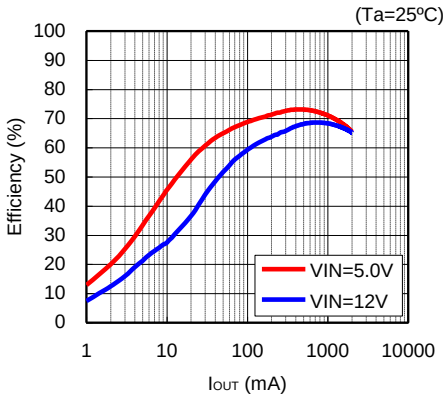
R1243x001A/R1243x001B, R1243S001E

V_{OUT} = 18 V



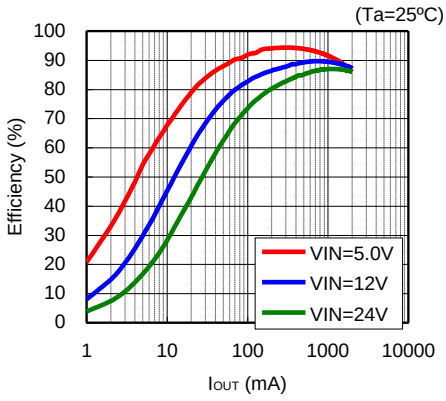
R1243x001C/R1243x001D

V_{OUT} = 0.8 V



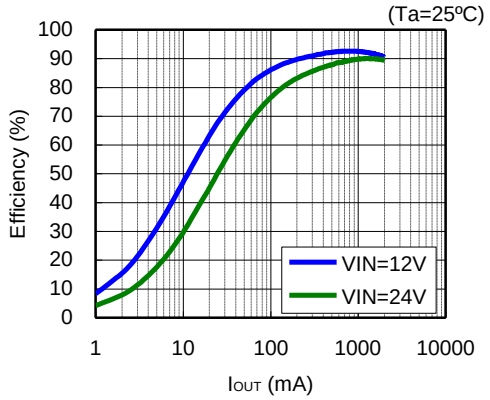
R1243x001C/R1243x001D

V_{OUT} = 3.3 V



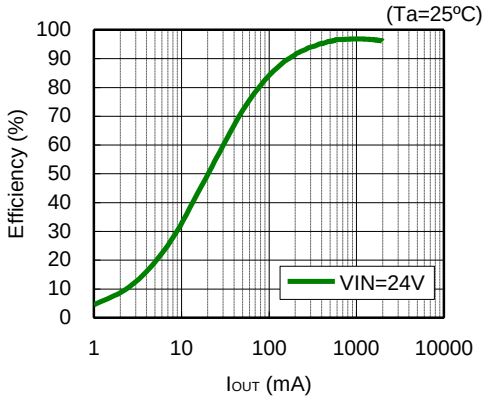
R1243x001C/R1243x001D

V_{OUT} = 5.0 V



R1243x001C/R1243x001D

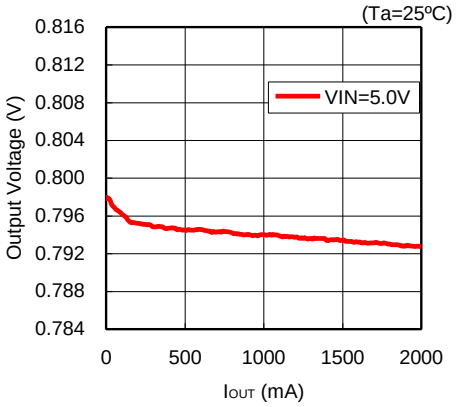
V_{OUT} = 18 V



20) Output Current vs. Output Voltage

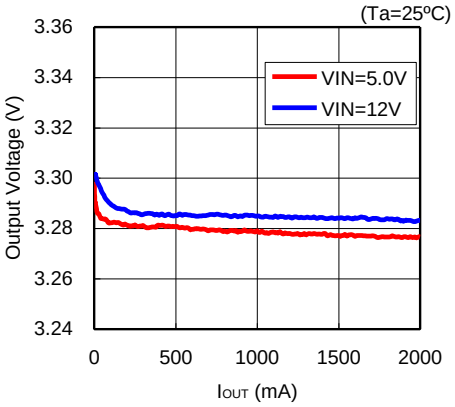
R1243x001A/R1243x001B, R1243S001E

V_{OUT} = 0.8 V



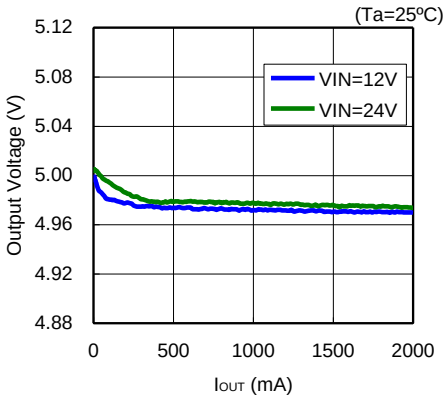
R1243x001A/R1243x001B, R1243S001E

V_{OUT} = 3.3 V



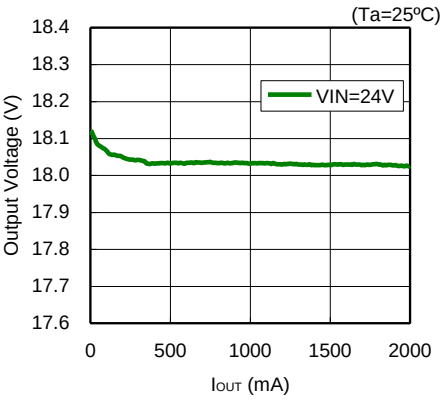
R1243x001A/R1243x001B, R1243S001E

V_{OUT} = 5.0 V



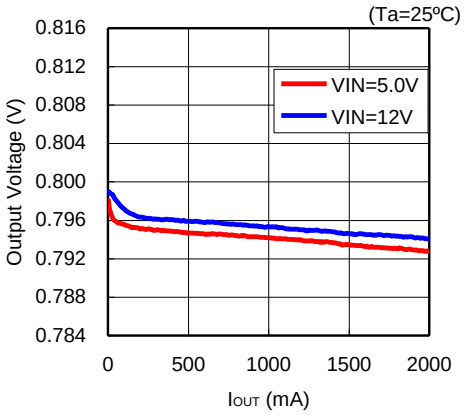
R1243x001A/R1243x001B, R1243S001E

V_{OUT} = 18 V



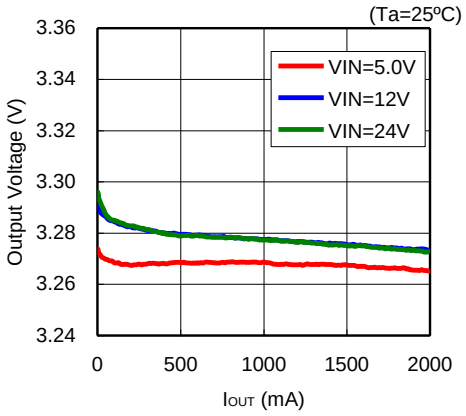
R1243x001C/R1243x001D

V_{OUT} = 0.8 V



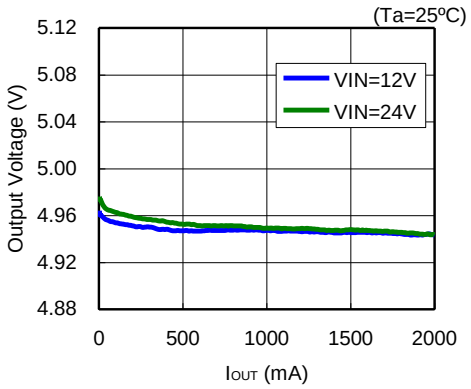
R1243x001C/R1243x001D

V_{OUT} = 3.3 V



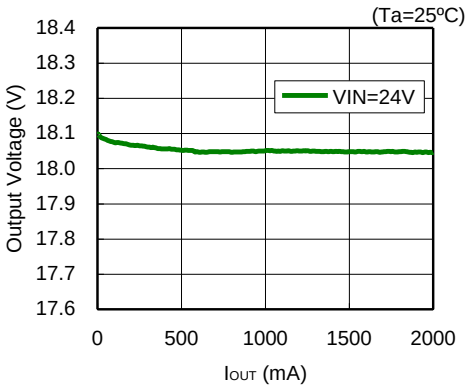
R1243x001C/R1243x001D

V_{OUT} = 5.0 V



R1243x001C/R1243x001D

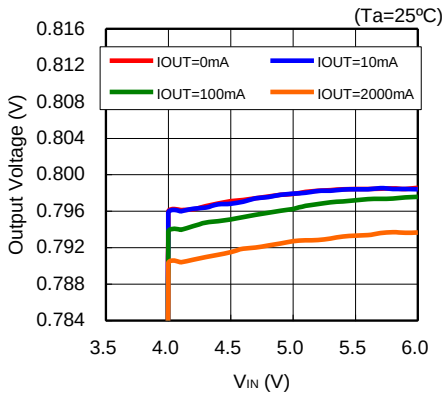
V_{OUT} = 18 V



21) Input Voltage vs. Output Voltage

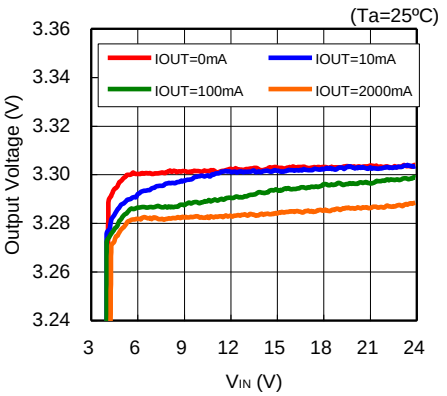
R1243x001A/R1243x001B, R1243S001E

V_{OUT} = 0.8 V



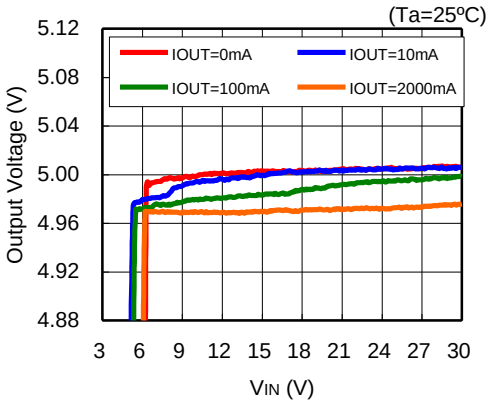
R1243x001A/R1243x001B, R1243S001E

V_{OUT} = 3.3 V



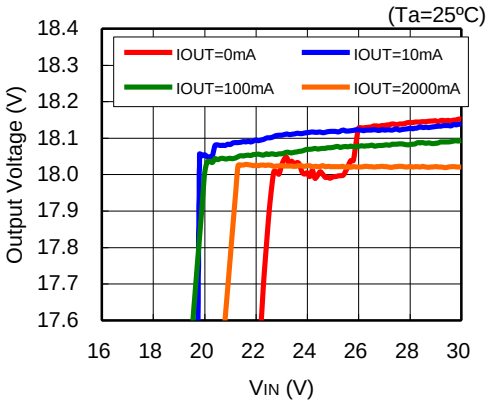
R1243x001A/R1243x001B, R1243S001E

V_{OUT} = 5.0 V



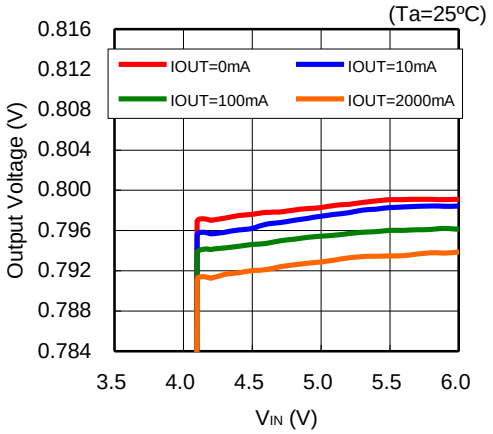
R1243x001A/R1243x001B, R1243S001E

V_{OUT} = 18 V



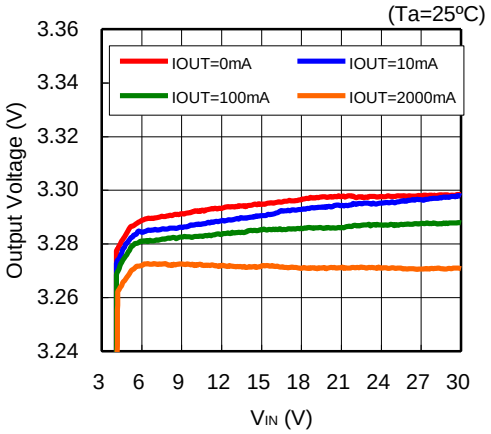
R1243x001C/R1243x001D

V_{OUT} = 0.8 V



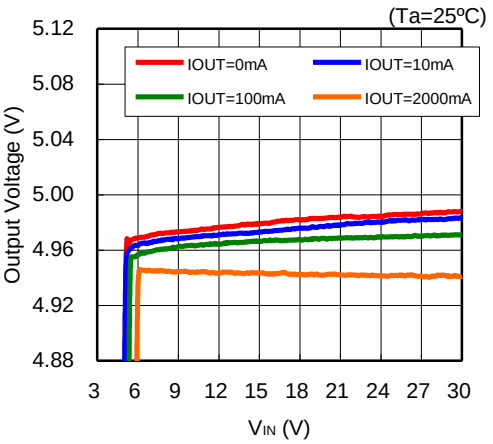
R1243x001C/R1243x001D

V_{OUT} = 3.3 V



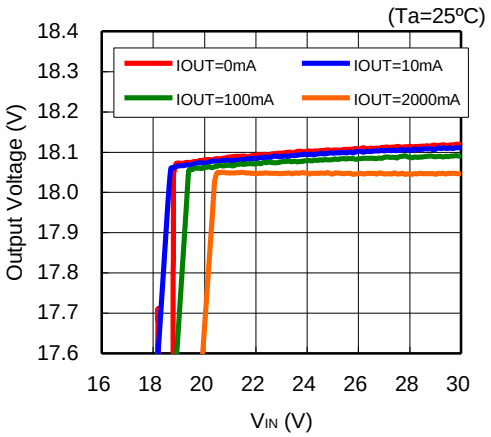
R1243x001C/R1243x001D

V_{OUT} = 5.0 V



R1243x001C/R1243x001D

V_{OUT} = 18 V



Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

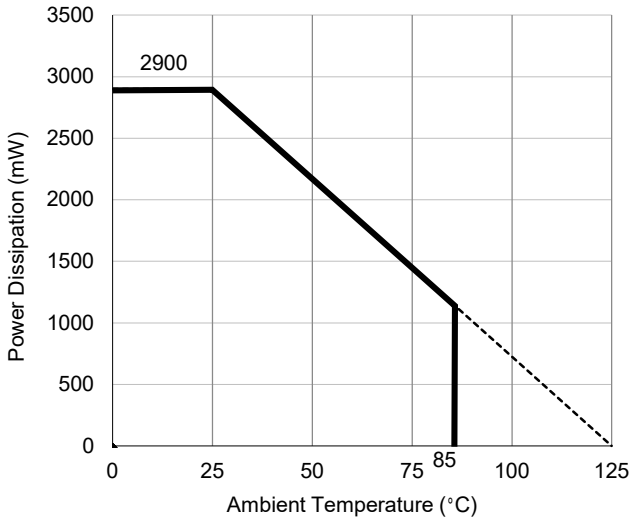
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 21 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

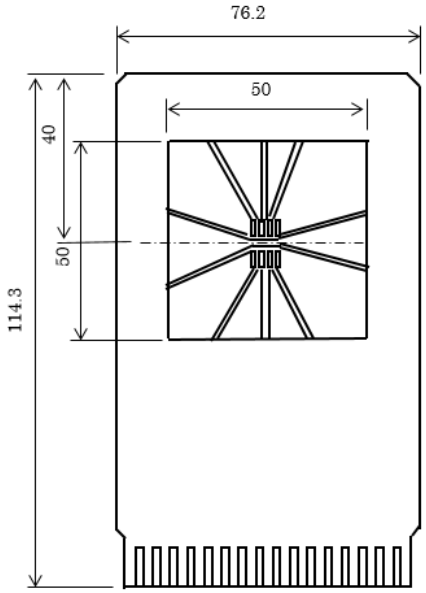
Item	Measurement Result
Power Dissipation	2900 mW
Thermal Resistance (θja)	θja = 34.5°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 10°C/W

θja: Junction-to–ambient thermal resistance.

ψjt: Junction–to-top of package thermal characterization parameter

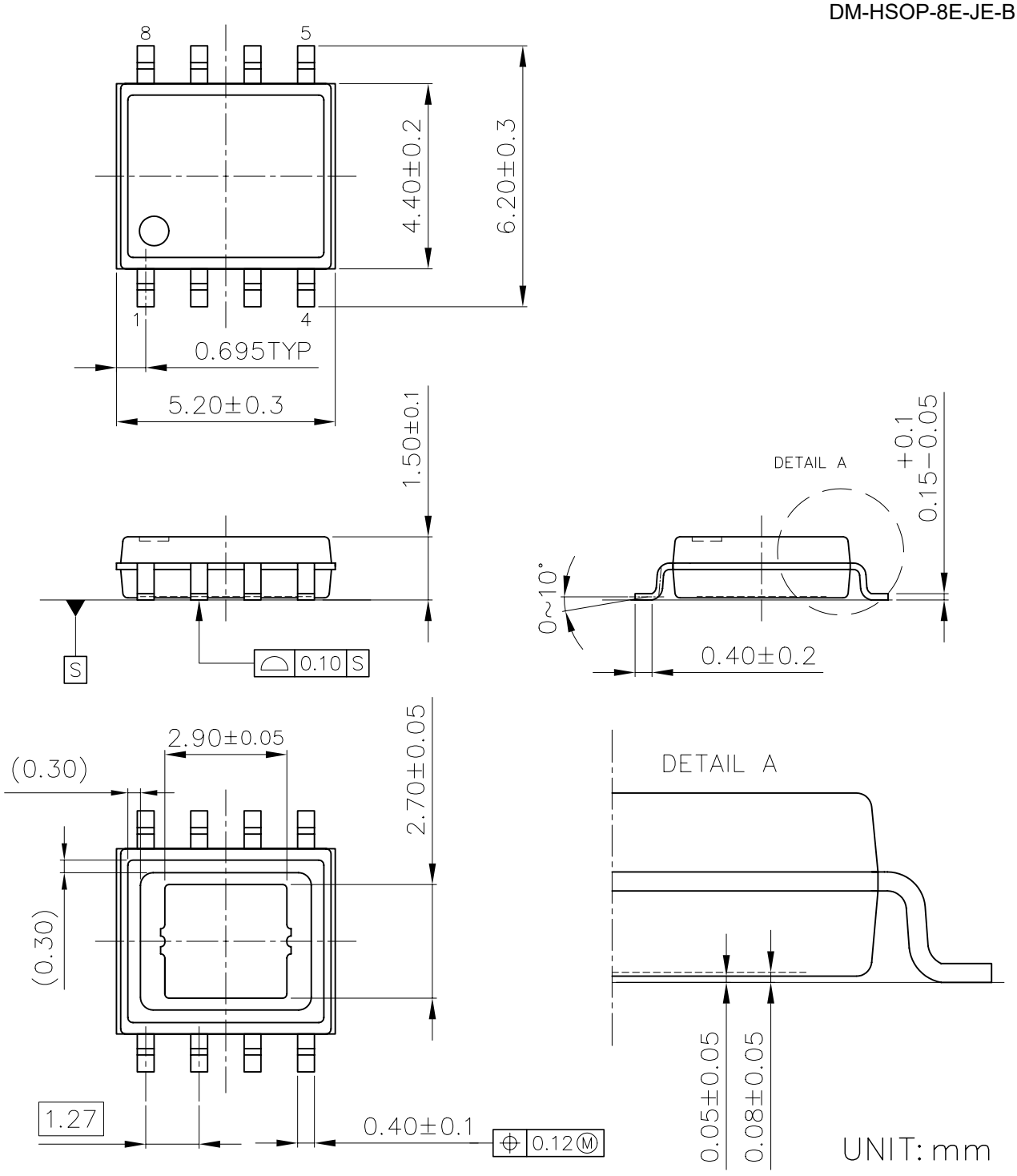


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

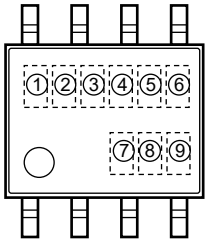
DM-HSOP-8E-JE-B



HSOP-8E Package Dimensions

R1243S SERIES MARK SPECIFICATION

- **HSOP-8E**



① to ⑥ : Product Code (Refer to Part Number vs. Product Code)

⑦ to ⑨ : Lot Number

- **Part Number vs. Product Code**

R1243Sxxxx Series

Part Number	Product Code					
	①	②	③	④	⑤	⑥
R1243S001A	R	S	0	0	2	A
R1243S001B	R	S	0	0	2	B
R1243S001C	R	S	0	0	2	C
R1243S001D	R	S	0	0	2	D
R1243S001E	R	S	0	0	2	E

Ver. A

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

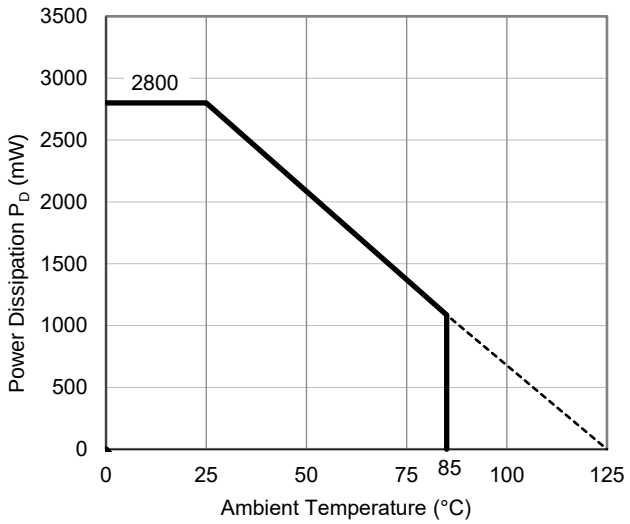
Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	ϕ 0.3 mm × 30 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

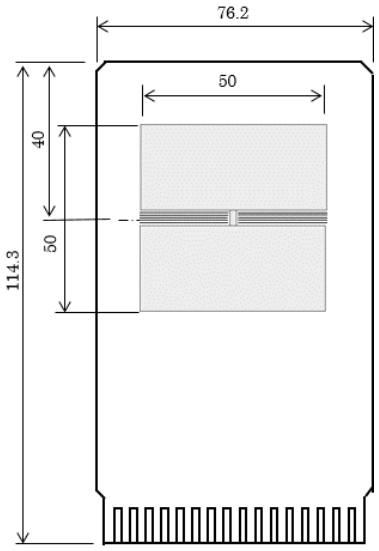
Item	Measurement Result
Power Dissipation	2800 mW
Thermal Resistance (θja)	θja = 35°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 10°C/W

θja: Junction-to-Ambient Thermal Resistance

ψjt: Junction-to-Top Thermal Characterization Parameter

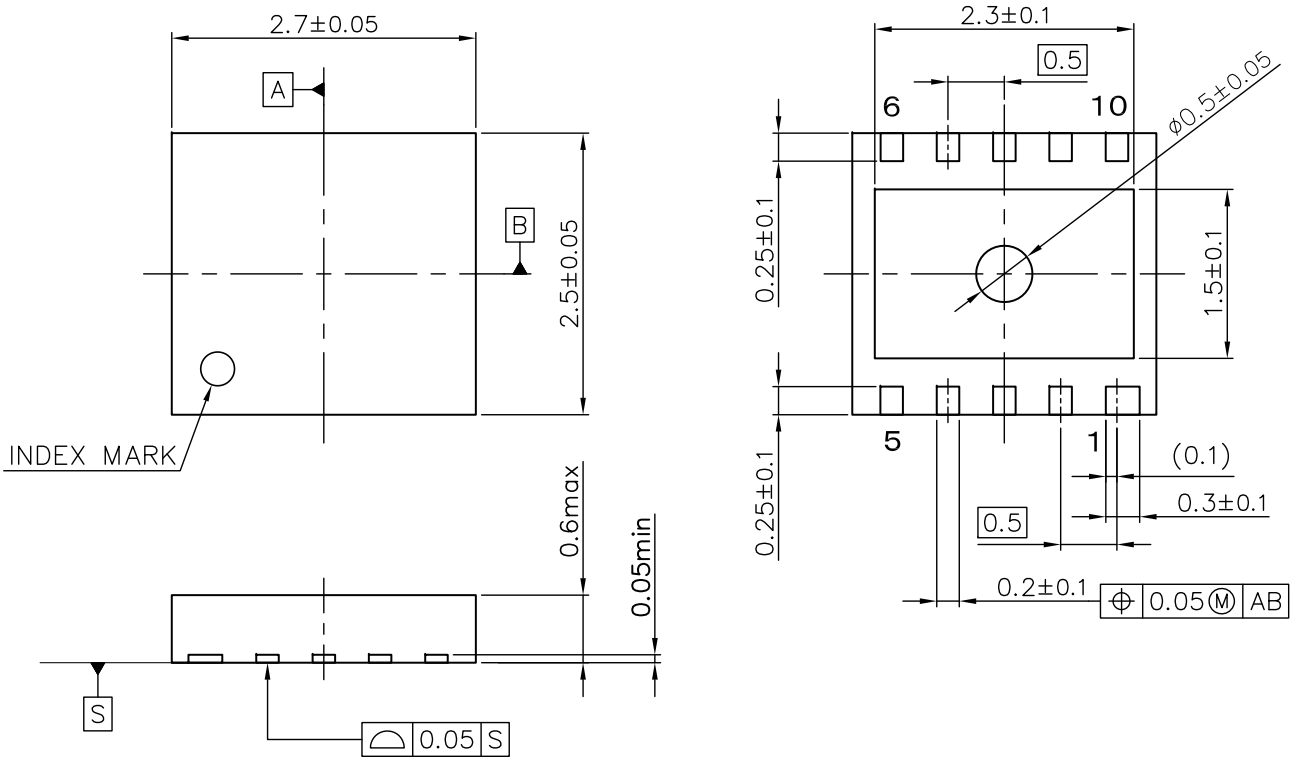


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

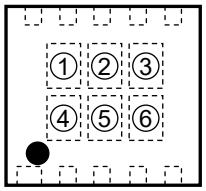
DM-DFN(PL)2527-10-JE-C



DFN(PL)2527-10 Package Dimensions (mm)

R1243K SERIES MARK SPECIFICATION

- **DFN(PL)2527-10**



① to ④ : Product Code (Refer to Part Number vs. Product Code)

⑤ , ⑥ : Lot Number

- **Part Number vs. Product Code**

R1243K Series

Part Number	Product Code			
	①	②	③	④
R1243K001A	C	T	0	1
R1243K001B	C	T	0	2
R1243K001C	C	T	0	3
R1243K001D	C	T	0	4
R1243K001E	C	T	0	5

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    - Various Safety Devices
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    In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.
    8-2. Quality Warranty Remedies
    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
    Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
    8-3. Remedies after Quality Warranty Period
    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
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