Nisshinbo Micro Devices Inc.

NB7120ZA

1-cell Li-ion Battery Protection IC for High-side FETS

FEATURES

- Supply Current
  Normal mode: Typ. 5.0μA / Max. 8.0 μA
  Standby mode: Max. 0.04 μA

- Detector Selectable Range and Accuracy
  Overcharge Detection Voltage (V_{DET1}):
  4.2 V to 4.6 V, ±10 mV
  Over-discharge Detection Voltage (V_{DET2}):
  2.0 V to 3.4 V, ±35 mV
  Discharge Overcurrent Detection Voltage (V_{DET3}):
  0.0080 V to 0.0800 V
  0.0080 V to 0.030 V: ±1.5 mV
  0.0301 V to 0.060V: ±5%
  0.0601 V to 0.0800 V: ±3 mV
  Charge Overcurrent Detection Voltage (V_{DET4}):
  –0.080 V to –0.008 V
  –0.008 V to –0.0325 V: ±1.5 mV
  –0.0326 V to –0.0600 V: ±5%
  –0.0601 V to –0.0800 V: ± 3mV
  Short Circuit Detection Voltage (V_{SHORT}):
  0.025 V to 0.125 V, ±2.5 mV

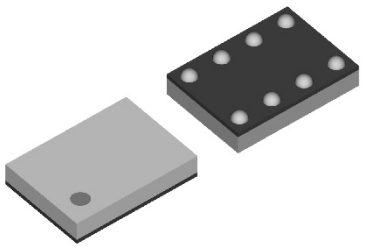
- 0 V Battery Charging: Inhibition
  0 V Battery Charging Inhibition Voltage (V_{NOCHG}):
  1.25 V to 2.00 V, ±50 mV
- Over-discharge Release Type: Latch
- Discharge Overcurrent Release Type selectable:
  Auto Release /Latch

APPLICATIONS

- Hearable / Wearable devices,
- Smart Phone,
- Handheld Data Terminals

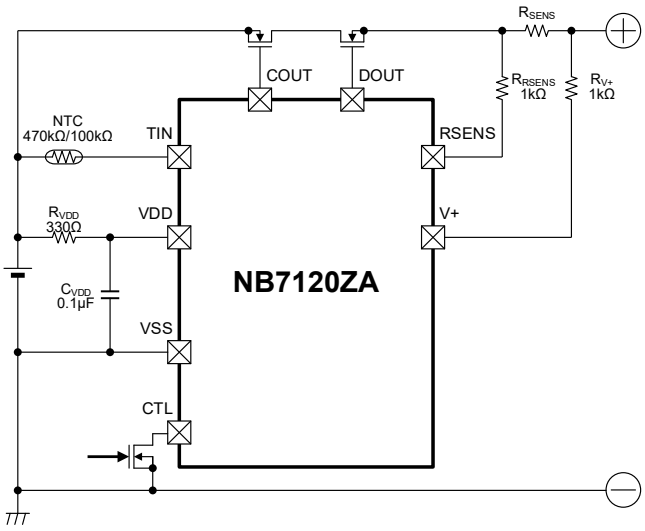
GENERAL DESCRIPTION

The NB7120ZA is one-cell Li-ion / Li-polymer rechargeable battery protection IC features high-accuracy over-charge/discharge, overcurrent and temperature protections for external high-side FETs and a sense resistor.
The NB7120ZA can detect over-charge/discharge and load overcurrent, further includes a short circuit protector for preventing large external short circuit current. It is possible to detect the temperature by connecting a thermistor.



WLCSP-8-P15
1.50 x 1.08 x 0.38 *1 [mm]
*1 Maximum thickness including balls

TYPICAL APPLICATION CIRCUIT



PRODUCT NAME INFORMATION

NB7120 ZA * * * E2 S**
aa bbb c d ee f

Description of configuration

Composition	Item	Description
aa	Package	Indicates the package code.
bbb	Specific Option	Indicates a three-digit number code that combined set voltages. Refer to the table of set voltages for details.
c		Indicates a delay time code. Refer to the table of delay times for details.
d		Indicates a function code. Refer to the table of functions for details.
ee	Packing	Indicates the taping direction. Refer to Packing Specification in the appendix Package Information for details.
f	Grade	Indicates the quality grade. S: Standard Refer to the table of grade for details.

Note: For mass-produced products, refer to the Appendix "Product Code List".

Table of set voltages (bbb)

Symbol	V_{DET1}	V_{DET2}	V_{DET3}	V_{DET4}	V_{SHORT}	V_{NOCHG}	$T_{DET1/2}$	$T_{REL1/2}$ *1	NTC
Range [V] / [°C] (Step)	4.2V to 4.6V (0.005)	2.0V to 3.4V (0.005)	0.0080V to 0.0800V (0.0001)	–0.0800V to –0.0080V (0.0001)	0.025V to 0.125V (0.001)	1.250V to 2.000V (0.05)	40°C to 85°C (5)	$T_{DET1/2}$ – [0 to 10] (5)	100 kΩ/ 470 kΩ

*1 Each set value of $T_{REL1/2}$ can be set to 0°C to 10°C (in steps of 5°C) lower than $T_{DET1/2}$.

Table of delay times (c)

Symbol	t_{VDET1}	t_{VREL1} *1	t_{VDET2}	t_{VREL2}	t_{VDET3}	t_{VREL3}	t_{VDET4} *1	t_{VREL4}	t_{VSHORT}	$t_{TDET1/2}$	$t_{TREL1/2}$	t_{TS}	t_{TNS}
Time [ms]	1024 / 2048 / 3072 / 4096	2 / 16	16 / 32 / 128	1.1	32 / 128 / 256 / 512 / 1024	1.1	8 / 16 / 16.5 / 32	1.1	0.28	128 / 512 / 1024 / 4096	128	10	90 / 528 / 1040
D	4096	16	32	1.1	32	1.1	16.5	1.1	0.28	4096	128	10	90.0
E	1024	16	128	1.1	256	1.1	8	1.1	0.28	1024	128	10	528
F	1024	2	128	1.1	256	1.1	8	1.1	0.28	1024	128	10	528

*1 The selectable value of t_{VDET4} depends on t_{VREL1}.
When t_{VREL1} = 2ms, delay times other than 16.5ms can be selected for t_{VDET4}.
When t_{VREL1} = 16ms, delay times other than 16ms can be selected for t_{VDET4}.

Table of functions (d)

Function	Overcharge Release	Over-discharge Release	Discharge Overcurrent Release	0 V Battery Charging	Charge Overcurrent Detection	Overcurrent Release Option (V_{REL3}, V_{REL4}) *1
Type / Condition	Latch	Latch	Auto Release Latch	Inhibition	Available Unavailable	Type1 / Type2
Z	Latch	Latch	Auto Release	Inhibition	Available	Type2

*1 Each set voltage of type1/2 is as follows:
Type1: V_{REL3} = V_{DD} x 0.84 / V_{DD} x 0.87 / V_{DD} x 0.90 (Min./Typ./Max.), V_{REL4} = –0.050 / 0.00 / 0.030 (Min./Typ./Max.)
Type2: V_{REL3} = V_{REL4} : V_{DD} - 0.18 / V_{DD} – 0.12 / V_{DD} – 0.06 (Min./Typ./Max.)

Table of grade (f)

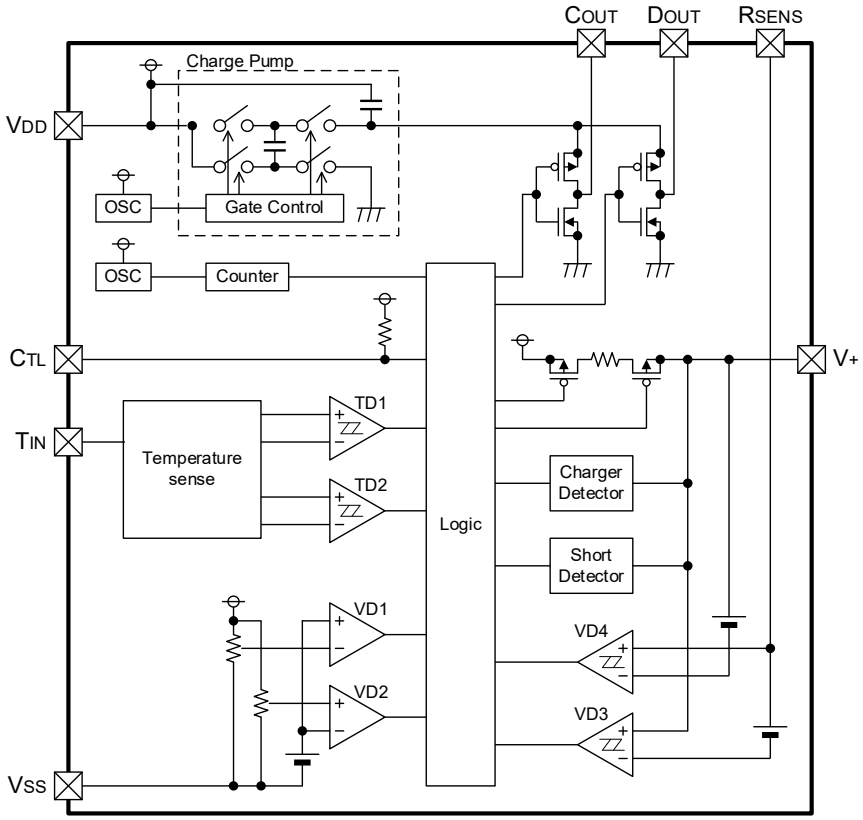
	Applications	Operating Temperature Range	Test Temperature
S	General–purpose and Consumer application	–40°C to 85°C	25°C

ORDER INFORMATION

For the mass-produced products, please refer to the Appendix “Product Code List”.

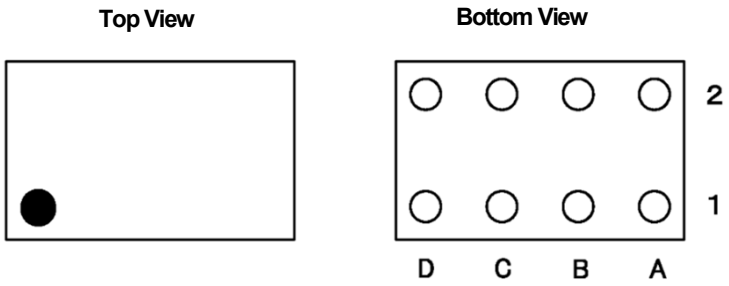
Product Name	Package	RoHS	Halogen-Free	Plating Composition	Weight [mg]	MOQ [pcs/reel]
NB7120ZA*****E2S	WLCSP-8-P15	Yes	Yes	Sn-3Ag-0.5Cu	1.0	5,000

BLOCK DIAGRAM



NB7120ZA Block Diagram

PIN DESCRIPTIONS



NB7120ZA (WLCSP-8-P15) Pin Configuration

Pin No.	Pin Name	I/O	Description
A1	VSS	-	Ground pin for the IC
B1	TIN	I	Temperature sensing input pin
C1	CTL	I	Forced standby control input pin
D1	RSENS	I	Current sensing input pin
A2	VDD	I	Power supply pin, the substrate level of the IC
B2	COUT	O	Charge control pin, CMOS output
C2	DOUT	O	Discharge control pin, CMOS output
D2	V+	I	Battery pack plus voltage input pin

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	V_{SS} – 0.3 to V_{SS} + 6.5	V
VP Pin Input Voltage	V+	V_{SS} – 0.3 to V_{SS} + 30	V
RSENS Pin Input Voltage	V_{RSENS}	V_{SS} – 0.3 to V_{SS} + 30	V
TIN Pin Input Voltage	V_{TIN}	V_{SS} – 0.3 to V_{SS} + 6.5	V
CTL Pin Input Voltage	V_{CTL}	V_{SS} – 0.3 to V_{SS} + 6.5	V
COUT Pin Output Voltage	V_{COUT}	V_{SS} – 0.3 to V_{DD} + 6.5	V
DOUT Pin Output Voltage	V_{DOUT}	V_{SS} – 0.3 to V_{DD} + 6.5	V
Power Dissipation	P_D	670	mW
Junction Temperature Range	Tj	–40 to 105	°C
Storage Temperature Range	Tstg	–55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION VOLTAGE

	Symbol	Rating	Unit
HBM (Human Body Model)	C = 100 pF, R = 1.5 kΩ	±2000	V
CDM (Charged Device Model)	Field Included CDM (FI-CDM)	±1000	V

ELECTROSTATIC DISCHARGE RATINGS

The electrostatic discharge test is done based on JEDEC JS001, JS002.

RECOMMENDED OPERATING CONDITIONS

	Symbol	Rating	Unit
Operating Input Voltage	V_{DD1}	1.5 to 5.0	V
Operating Temperature Range	Ta	–40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

ELECTRICAL CHARACTERISTICS

Voltages are defined as $V_{DD} - V_{SS}$, Ta = 25°C, unless otherwise specified in Conditions.

NB7120ZAxxxxx Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
0V Battery Charging Inhibition Voltage	V_{NOCHG}	V+ = V_{DD}	V_{NOCHG} – 0.050	V_{NOCHG}	V_{NOCHG} + 0.050	V	A
Overcharge Detection Voltage	V_{DET1}	R_{VDD} = 330Ω	V_{DET1} – 0.010	V_{DET1}	V_{DET1} + 0.010	V	A
Overcharge Release Voltage	V_{REL1}	R_{VDD} = 330Ω, V+ = V_{DD} – 0.3 V	V_{DET1} – 0.015	V_{DET1}	V_{DET1} + 0.010	V	W
Overcharge Detection Delay Time	t_{VDET1}	V_{DD} = 3.9 V → 4.6 V	t_{VDET1} × 0.80	t_{VDET1}	t_{VDET1} × 1.20	ms	B
Overcharge Release Delay Time	t_{VREL1}	V_{DD} = 3.9 V, V+ = 3.9 V → 2.9 V				ms	C
		t_{VREL1} = 2ms	1	2	3		
		t_{VREL1} = 16ms	t_{VREL1} × 0.80	t_{VREL1}	T_{VREL1} × 1.20		
Over-discharge Detection Voltage	V_{DET2}	Detect falling edge of V_{DD}	V_{DET2} – 0.035	V_{DET2}	V_{DET2} + 0.035	V	D
Over-Discharge Release Voltage	V_{REL2}	$V_+ = V_{DD}$, Detect rising edge of V_{DD}	V_{DET2} – 0.035	V_{DET2} + 0.008	V_{DET2} + 0.051	V	D
Over-discharge Detection Delay Time	t_{VDET2}	V_{DD} = 3.9 V → 2.0 V	t_{VDET2} × 0.80	t_{VDET2}	t_{VDET2} × 1.20	ms	E
Over-discharge Release Delay Time	t_{VREL2}	V_{DD} = 3.9 V, V+ = 0V → 3.9V	0.85	1.10	1.35	ms	E
Discharge Overcurrent Detection Voltage	V_{DET3}	Defined as V_{RSENS} – V+, V_{DD} = 3.9 V				V	F
		–0.0080 V to –0.0300 V	V_{DET3} – 0.0015	V_{DET3}	V_{DET3} + 0.0015		
		–0.0301 V to –0.0600 V	V_{DET3} × 0.95	V_{DET3}	V_{DET3} × 1.05		
		–0.0601 V to –0.0800 V	V_{DET3} – 0.003	V_{DET3}	V_{DET3} + 0.003		
Discharge Overcurrent Release Voltage	V_{REL3}	Defined as V+ – V_{SS}, Detect rising edge of V+				V	F
		Type 1	V_{DD} × 0.84	V_{DD} × 0.87	V_{DD} × 0.90		
		Type 2	V_{DD} – 0.180	V_{DD} – 0.120	V_{DD} – 0.060		
Discharge Overcurrent Detection Delay Time	t_{VDET3}	V_{DD} = V_{RSENS} = 3.9 V, V+ = 3.9 V → 3.9 V – V_{DET3} – 0.01 V	t_{VDET3} × 0.80	t_{VDET3}	t_{VDET3} × 1.20	ms	G
Discharge Overcurrent Release Delay Time	t_{VREL3}	V_{DD} = V_{RSENS} = 3.9 V, V+ = 0 V → 3.9 V	0.85	1.10	1.35	ms	G
Charge Overcurrent Detection Voltage	V_{DET4}	Defined as V_{RSENS} – V+, V_{DD} = 3.9 V, Detect rising edge of V+				V	F
		–0.0080 V to –0.0325 V	V_{DET4} – 0.0015	V_{DET4}	V_{DET4} + 0.0015		
		–0.0326 V to –0.0600 V	V_{DET4} × 0.95	V_{DET4}	V_{DET4} × 1.05		
		–0.0601 V to –0.0800 V	V_{DET4} – 0.003	V_{DET4}	V_{DET4} + 0.003		
Charge Overcurrent Release Voltage	V_{REL4}	V_{DD} = 3.9 V, Detect falling edge of V+				V	F
		Type1, Defined as V+ – V_{DD}	– 0.050	0.00	0.030		
		Type2, Defined as V+ – V_{SS}	V_{DD} – 0.180	V_{DD} – 0.120	V_{DD} – 0.060		

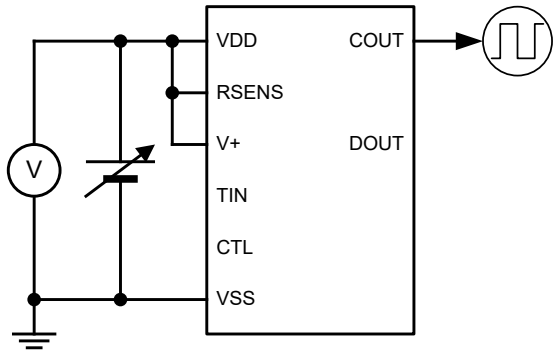
NB7120ZAxxxxx Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
Charge Overcurrent Detection Delay Time	t_{VDET4}	V_{DD} = V_{RSENS} = 3.9 V, V+ = 3.9 V → 3.9 V + V_{DET4} – 0.01 V	t_{VDET4} × 0.80	t_{VDET4}	t_{VDET4} × 1.20	ms	G
Charge Overcurrent Release Delay Time	t_{VREL4}	V_{DD} = V_{RSENS} = 3.9 V, V+ = 3.95 V → 2.9 V	0.85	1.10	1.35	ms	G
Short Circuit Detection Voltage	V_{SHORT}	Defined as V_{RSENS} – V+, V_{DD} = 3.9 V, Detect falling edge of V+	V_{SHORT} – 0.0025	V_{SHORT}	V_{SHORT} + 0.0025	V	F
Short Circuit Detection Delay Time	t_{SHORT}	V_{DD} = V_{RSENS} = 3.9 V, V+ = 3.9 V → 3.9 V – V_{SHORT} – 0.01 V	210	280	350	µs	G
Internal Resistance for Discharge Overcurrent Protection	R_{SHORT}	V_{DD} = 3.9 V, V+ = 2.9 V	15	45	70	kΩ	H
Charger Detection Voltage for Standby Release	V_{CHGDET}	Defined as V+ – V_{SS}, R_{V+} = 1kΩ, V_{DD} = 3.9 V	V_{DD} × 0.4	V_{DD} × 0.5	V_{DD} × 0.7	V	I
Charger Pump Output Voltage1	V_{BST1}	COUT / DOUT pin voltage, V_{DD} = 3.9 V, I_{COUT} = I_{DOUT} = 0µA	7.400	7.650	-	V	J
Charger Pump Output Voltage2	V_{BST2}	COUT / DOUT pin voltage, V_{DD} = 3.9 V, I_{COUT} = I_{DOUT} = 1µA	6.500	6.950	-	V	J
COUT Pin NMOS ON Voltage	V_{OL1}	I_{OL} = 10µA, V_{DD} = 4.7 V	-	0.030	0.100	V	K
DOUT Pin NMOS ON Voltage	V_{OL21}	I_{OL} = 10µA, V_{DD} = 1.9 V, V+ = V_{DD}	-	0.065	0.150	V	L
DOUT Pin NMOS ON Voltage 2 (at Standby Mode)	V_{OL22}	I_{OL} = 1µA, V_{DD} = 1.9 V, V+ = V_{SS} after t_{VDET2}	-	0.020	0.100	V	M
Supply Current	I_{DD}	V_{DD} = V+ = 3.9 V, I_{OUT} = 0µA	-	5.0	8.0	µA	N
Standby Current	$I_{STANDBY}$	V_{DD} = 1.9 V	-	-	0.04	µA	O
Detection Temperature 1 for External NTC	T_{DET1}	V_{DD} = 3.9 V, [NTC performance] Vender: muRata Part: NCP02WF474F05RH Resistance: 470kΩ±1%(25°C) Part: NCP03WF104F05RL Resistance: 100kΩ±1%(25°C) B-Constant: 4250K±1%	T_{DET1} – 3.0	T_{DET1}	T_{DET1} + 3.0	°C	P
Release Temperature 1 for External NTC	T_{REL1}		T_{REL1} – 3.0	T_{REL1}	T_{REL1} + 3.0	°C	P
Detection Temperature 2 for External NTC	T_{DET2}		T_{DET2} – 3.0	T_{DET2}	T_{DET2} + 3.0	°C	Q
Release Temperature 2 for External NTC	T_{REL2}		T_{REL2} – 3.0	T_{REL2}	T_{REL2} + 3.0	°C	Q
Delay Time for $T_{DET1/2}$	t_{TDET}	V_{DD} = 3.9 V	t_{TDET} × 0.80	t_{TDET}	t_{TDET} × 1.20	ms	R
Delay Time for $T_{REL1/2}$	t_{TREL}	V_{DD} = 3.9 V	102	128	154	ms	R
Temperature Sense Time	t_{TS}	V_{DD} = 3.9 V	8	10	12	ms	S
Temperature No-sense Time	t_{TNS}	V_{DD} = 3.9 V	t_{TNS} × 0.80	t_{TNS}	t_{TNS} × 1.20	ms	S
Internal Resistance for Temperature Sense	R_{TIN}	V_{DD} = V_{TIN} = 3.9 V, R_{TIN} = 3.9 / TIN current				kΩ	T
		NTC Resistance: 470kΩ	65	150	270		
		NTC Resistance: 100kΩ	14	35	65		
Delay Time Shortening Mode Voltage	V_{DS}	Defined as V+ – V_{SS}, V_{DD} = 3.9 V	V_{DD} + 1.4	-	V_{DD} + 2.2	V	U
Detection Threshold of Standby State	V_{RCDET}	Defined as V+ – V_{SS}, V_{DD} = 3.9 V	V_{DD} × 0.35	V_{DD} × 0.45	V_{DD} × 0.65	V	U
Detection Voltage for COUT / DOUT Boost Voltage	V_{BSTDET}	Defined as V_{COUT} – V_{SS} or V_{DOUT} – V_{SS}, V_{DD} = 3.9 V	V_{DD} + 0.8	V_{DD} + 1.3	V_{DD} + 1.6	V	V
CTL Pin Pullup Resistance	R_{CTL}	V_{DD} = 3.9 V	1.200	3.000	4.700	MΩ	X
CTL Pin Detection Voltage	V_{CTLDET}	V_{DD} = 3.9 V	V_{DD} – 1.6	V_{DD} – 1.0	V_{DD} – 0.5	V	X
CTL Pin Detection Delay Time	t_{VCTL}	t_{VCTL} = t_{VDET2}, V_{DD} = 3.9 V, V_{CTL} = 3.9 V → 0 V	t_{VDET2} × 0.80	t_{VDET2}	t_{VDET2} × 1.20	ms	X

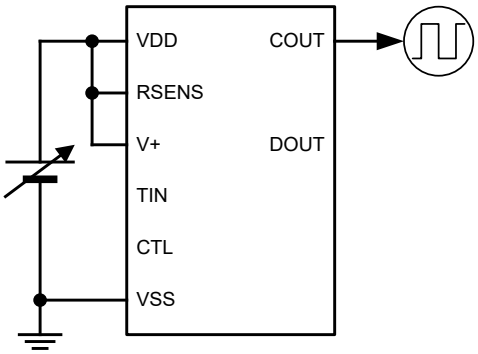
All test parameters listed in Electrical Characteristics are done under Ta = 25°C only.

Test Circuits

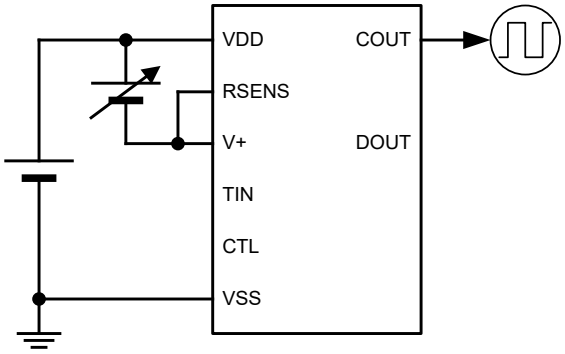
A



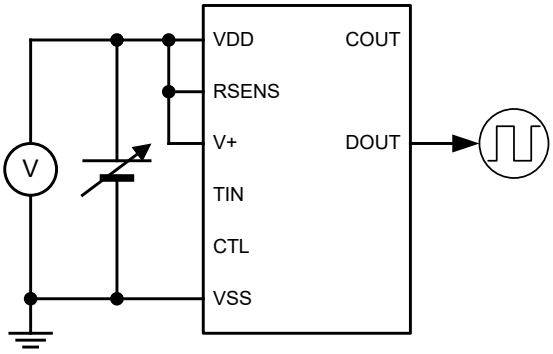
B



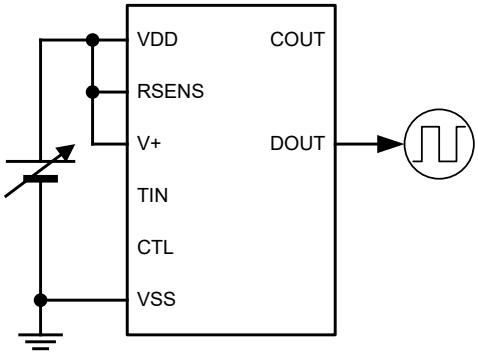
C



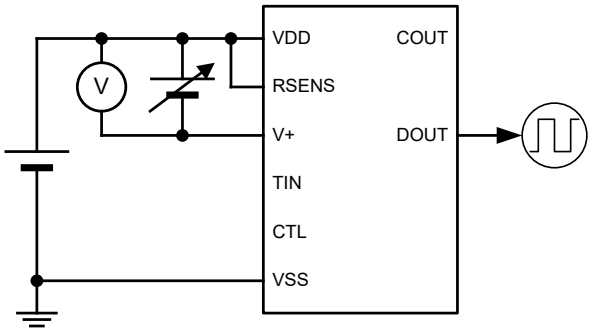
D



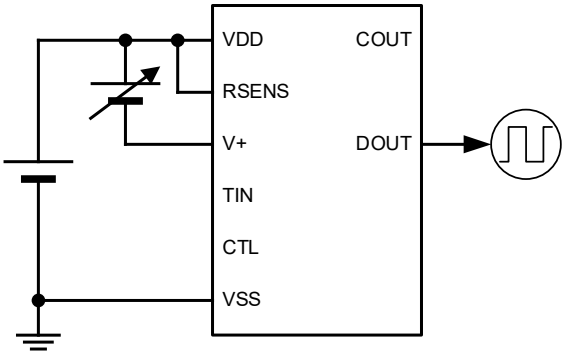
E



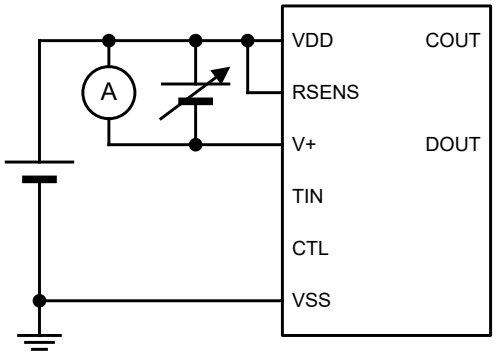
F



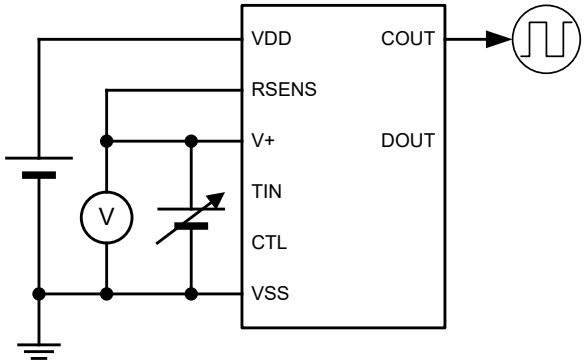
G



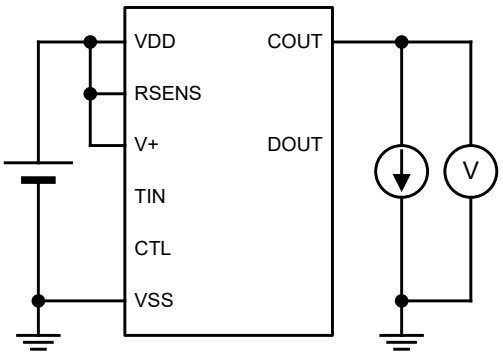
H



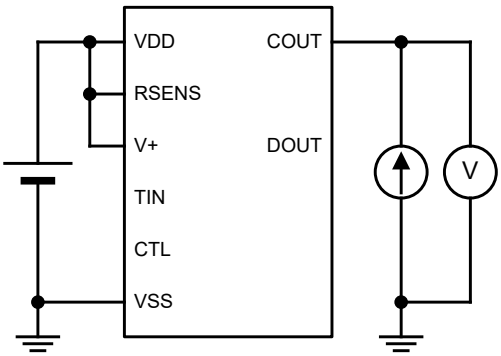
I


VDD
COUT
RSENS
V+
DOUT
TIN
CTL
VSS
V

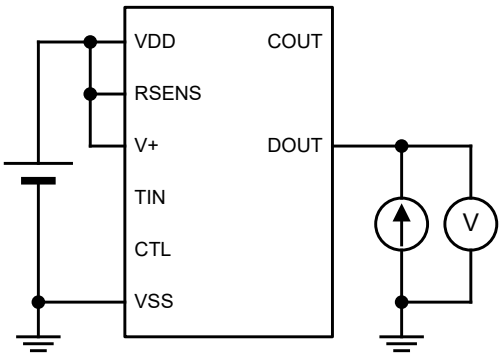
J


VDD
COUT
RSENS
V+
DOUT
TIN
CTL
VSS
V

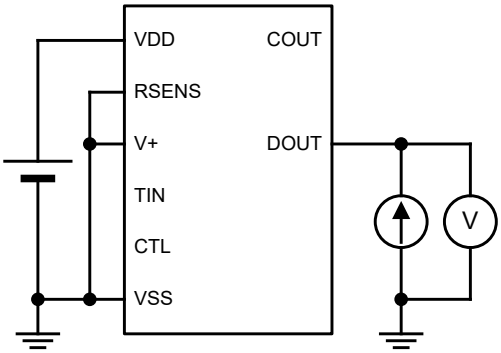
K


VDD
COUT
RSENS
V+
DOUT
TIN
CTL
VSS
V

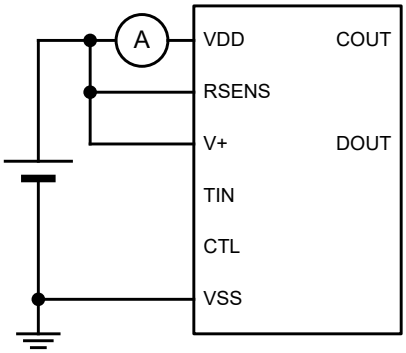
L


VDD
COUT
RSENS
V+
DOUT
TIN
CTL
VSS
V

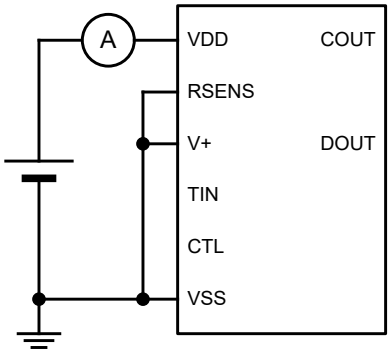
M


VDD
COUT
RSENS
V+
DOUT
TIN
CTL
VSS
V

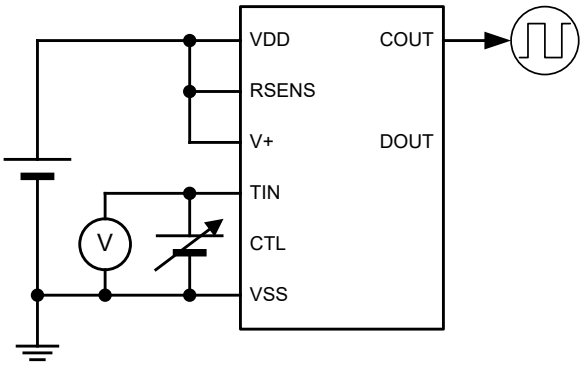
N


A
VDD
COUT
RSENS
V+
DOUT
TIN
CTL
VSS

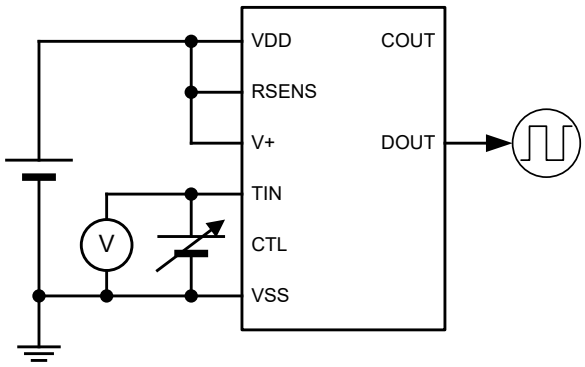
O


A
VDD
COUT
RSENS
V+
DOUT
TIN
CTL
VSS

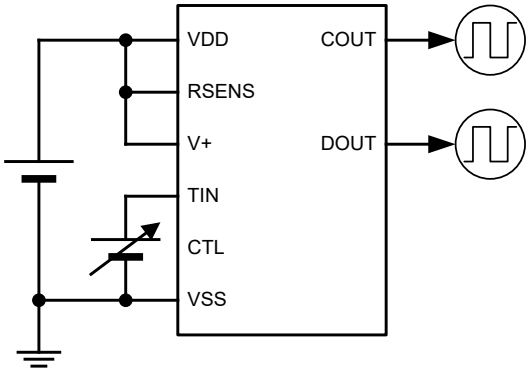
P


VDD
COUT
RSENS
V+
DOUT
TIN
CTL
VSS
V

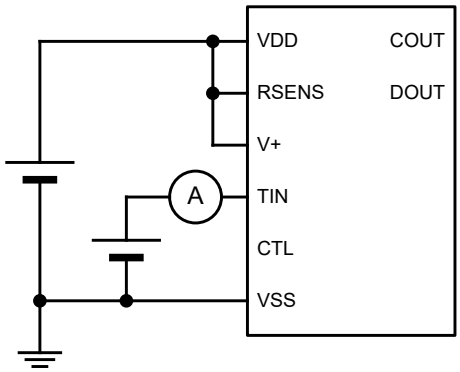
Q


VDD
COUT
RSENS
V+
DOUT
TIN
CTL
VSS
V

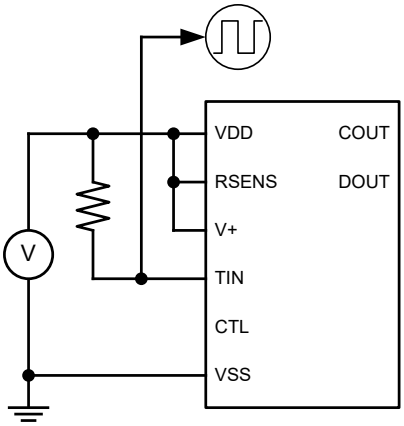
R


VDD
COUT
RSENS
V+
DOUT
TIN
CTL
VSS

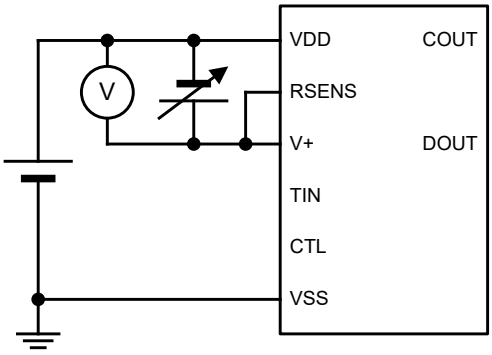
S


VDD
COUT
RSENS
DOUT
V+
A
TIN
CTL
VSS

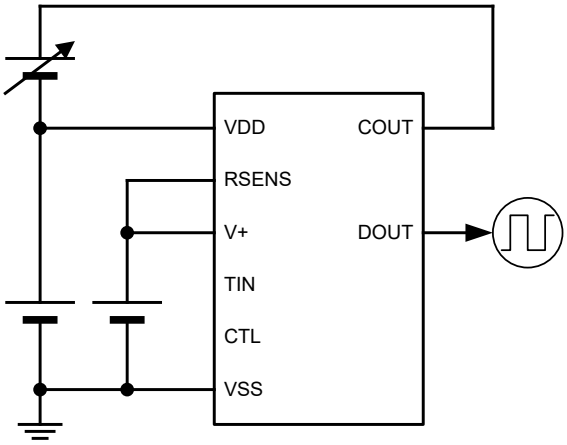
T


VDD
COUT
RSENS
DOUT
V+
V
TIN
CTL
VSS

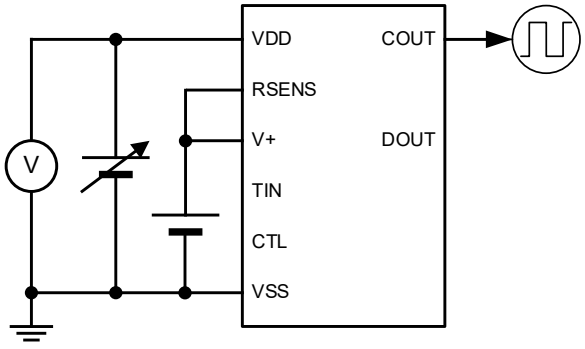
U


VDD
COUT
RSENS
V+
DOUT
V
TIN
CTL
VSS

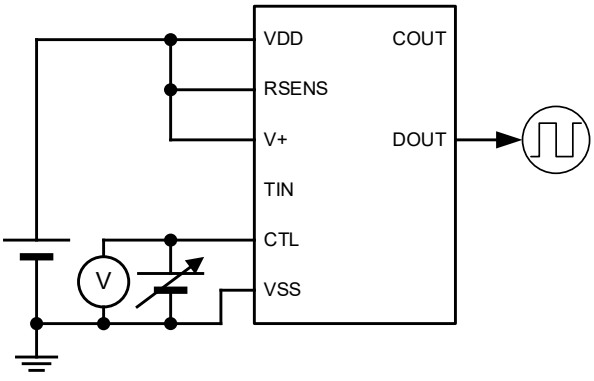
V


VDD
COUT
RSENS
V+
DOUT
TIN
CTL
VSS

W


VDD
COUT
RSENS
V+
DOUT
V
TIN
CTL
VSS

X


VDD
COUT
RSENS
V+
DOUT
TIN
CTL
V
VSS

THEORY OF OPERATION

Overcharge Protection

When the VDD pin voltage (V_{DD}) exceeds the overcharge detection voltage (V_{DET1}) for longer than the overcharge detection delay time (t_{VDET1}), this IC enters the overcharge state. In this state, the COUT pin becomes Low, and the charge control FET is turned off to stop charging.
The V+ pin voltage decreases by the Vf voltage at the internal parasitic diode compared to the VDD pin voltage (V_{DD}), as the discharge current flows via the parasitic diode even when the charge control FET is off.

A release from the overcharge state must meet the following pin condition and delay time.

Type	Pin Condition	Delay Time	Remarks
Latch	V+ < V_{REL4} and V_{DD} < V_{DET1}	t_{VREL1}	-

Over-discharge Protection

When the VDD pin voltage (V_{DD}) falls below the over-discharge detection voltage (V_{DET2}) for longer than the over-discharge detection delay time (t_{VDET2}), this IC enters the over-discharge state. In this state, the DOUT pin becomes Low, and the discharge control FET is turned off to stop discharging.
The V+ pin voltage increases by the Vf voltage at the internal parasitic diode compared to the VDD pin voltage (V_{DD}), as the charge current flows via the parasitic diode even when the discharge control FET is off.
In addition, when V+ is pulled down to V_{SS} level and falls below the V_{RCDET}, the IC enters the standby state.
In the standby state, the current consumption is reduced to a minimum.

A release from the over-discharge state must meet the following pin condition and delay time.

Type	Pin Condition	Delay Time	Remarks
Latch	V+ > V_{CHGDET} and V_{DD} > V_{DET2}	t_{VREL2}	The V+ pin is internally pulled down to VSS.

Discharge Overcurrent Protection

To monitor the discharge current, this IC measures the voltage difference at the sense resistor (R_{SENS}) connected between the RSENS and the V+ pins to detect the current value.
When the discharge current, converted by R_{SENS} for current-to-voltage conversion, exceeds the discharge overcurrent detection voltage (V_{DET3}) for longer than the discharge overcurrent detection delay time (t_{VDET3}), this IC enters the discharge overcurrent state. In this state, the DOUT pin becomes Low, and the discharge control FET is turned off to shut off the discharge current.

A release from the discharge overcurrent state must meet the following pin condition and delay time depending on the release type selected.

Type	Pin Condition	Delay Time	Remarks
Latch	V+ > V_{REL3}	t_{VREL3}	The V+ pin is internally pulled down to VSS.
Auto Release	V+ > V_{REL3}	t_{VREL3}	The V+ pin is internally pulled up to VDD.

Short Circuit Protection

To monitor the short circuit current, this IC measures the voltage difference at the sense resistor (R_{SENS}) connected between the RSENS and the V+ pins to detect the current value.
When the short circuit current converted to current-to-voltage at R_{SENS} exceeds the short circuit detection voltage (V_{SHORT}), this IC enters the short circuit state. In this state, the DOUT pin becomes Low, and the discharge control FET is turned off to shut off the short circuit current.
If the short circuit current falls below V_{SHORT} within the short circuit detection delay time (t_{SHORT}), the short circuit state can be prevented.

A release from the short circuit state must meet the same condition and delay time as the discharge overcurrent protection.

Charge Overcurrent Protection

To monitor the charge current, this IC measures the voltage difference at the sense resistor (R_{SENS}) connected between the RSENS and the V+ pins to detect the current value.
When the charge current converted to current-to-voltage at R_{SENS} falls below the charge overcurrent detection voltage (V_{DET4}) for longer than the charge overcurrent detection delay time (t_{VDET4}), this IC enters the charge overcurrent state. In this state, the COUT pin becomes Low, and the charge control FET is turned off to shut off the charge current.

A release from the charge overcurrent state must meet the following pin condition and delay time depending on the release type selected.

Type	Pin Condition	Delay Time	Remarks
Type1/2	V+ < V_{REL4}	t_{VREL4}	The V+ pin is internally pulled down to VSS.

0 V Battery Charging Inhibition

0 V Battery Charge Function “Inhibition”

When the battery is below the 0 V battery charging inhibition voltage (V_{NOCHG}), charging is prohibited even with the charger connected.

Temperature Protection

This IC monitors the voltage converted from the temperature detected by the external thermistor connected to the TIN pin through the temperature-to-voltage converter using the internal resistor (R_{TIN}).
The thermistor operates only for a period of 10ms (t_{TNS}) per cycle (t_{TS} + t_{TNS}) to save the supply current.
The COUT pin becomes Low when a temperature higher than the detection temperature 1 for external NTC (T_{DET1}) is detected and sustained for longer than the delay time for $T_{DET1/2}$ (t_{TDET}), and the external Nch MOSFET is turned off to stop charging. Similarly, the DOUT pin becomes Low when the temperature higher than the detection temperature 2 for external NTC (T_{DET2}) is detected and sustained for longer than t_{TDET}, and the external Nch MOSFET is turned off to stop discharging.
When the temperature falls below the release temperature 1 for external NTC (T_{REL1}) or the release temperature 2 for external NTC (T_{REL2}) for longer than the temperature delay time (t_{TREL}), the COUT or DOUT pin becomes High.

Type	Pin Condition	Delay Time	Remarks
Auto Release	Temp.<$T_{REL1/2}$	t_{TREL}	-

Delay Time Shortening

To reduce the delay time, the V+ pin voltage (V+) must be set higher than the delay time shortening mode voltage (V_{DS}) to enter test mode.
To enable this mode, both the COUT and DOUT pin voltages must become higher than the detection voltage for COUT / DOUT boost voltage (V_{BSTDET}) for a certain period, provided that this mode is not enabled when either the COUT or DOUT pin voltage falls below V_{BSTDET}.

This test mode offers several benefits, including the delay time shortening.

- The delay time for each output is reduced.
- The voltage booster circuit is turned off.
- Constant temperature monitoring (sampling cycle stop)
- V_{DET3}, V_{SHORT}, and V_{DET4} become invalid.

Forced Over-discharge Detection by CTL Pin

The IC can detect an over-discharge by driving the CTL pin pulled up to VDD via the internal resistor (R_{CTL}) to VSS. When the over-discharge is detected and V+ falls below V_{RCDET}, the IC enters standby state. This allows the IC to be forced into the standby by the CTL pin, without reducing the battery voltage.
In the standby state, the current consumption is reduced to a minimum.

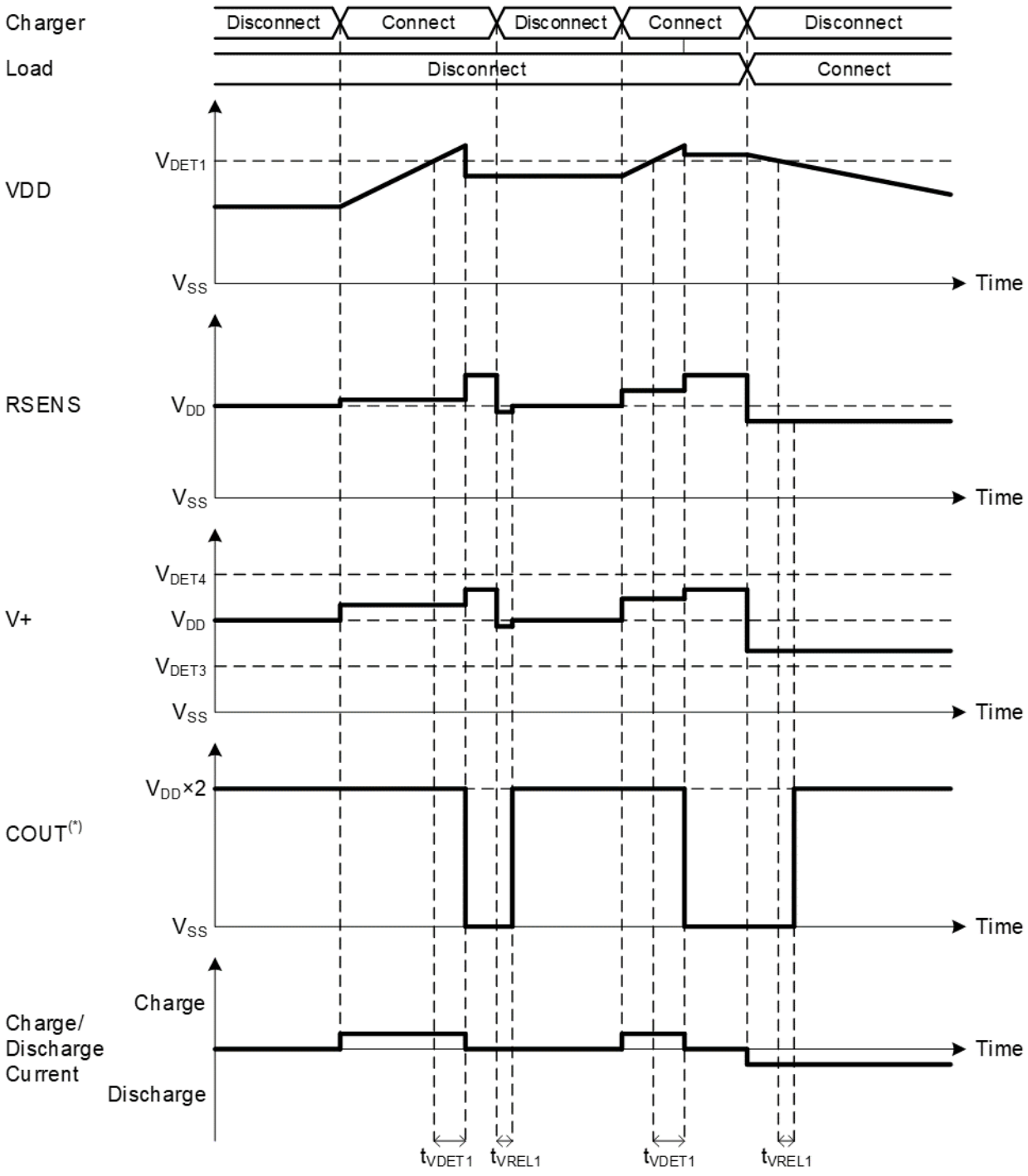
A release from the standby state must meet the following pin condition and delay time.

Pin Condition	Delay Time	Remarks
$V_{CTL} = V_{DD}$ and $V+ > V_{CHGDET}$	t_{VREL2}	-

Voltage Boost Function

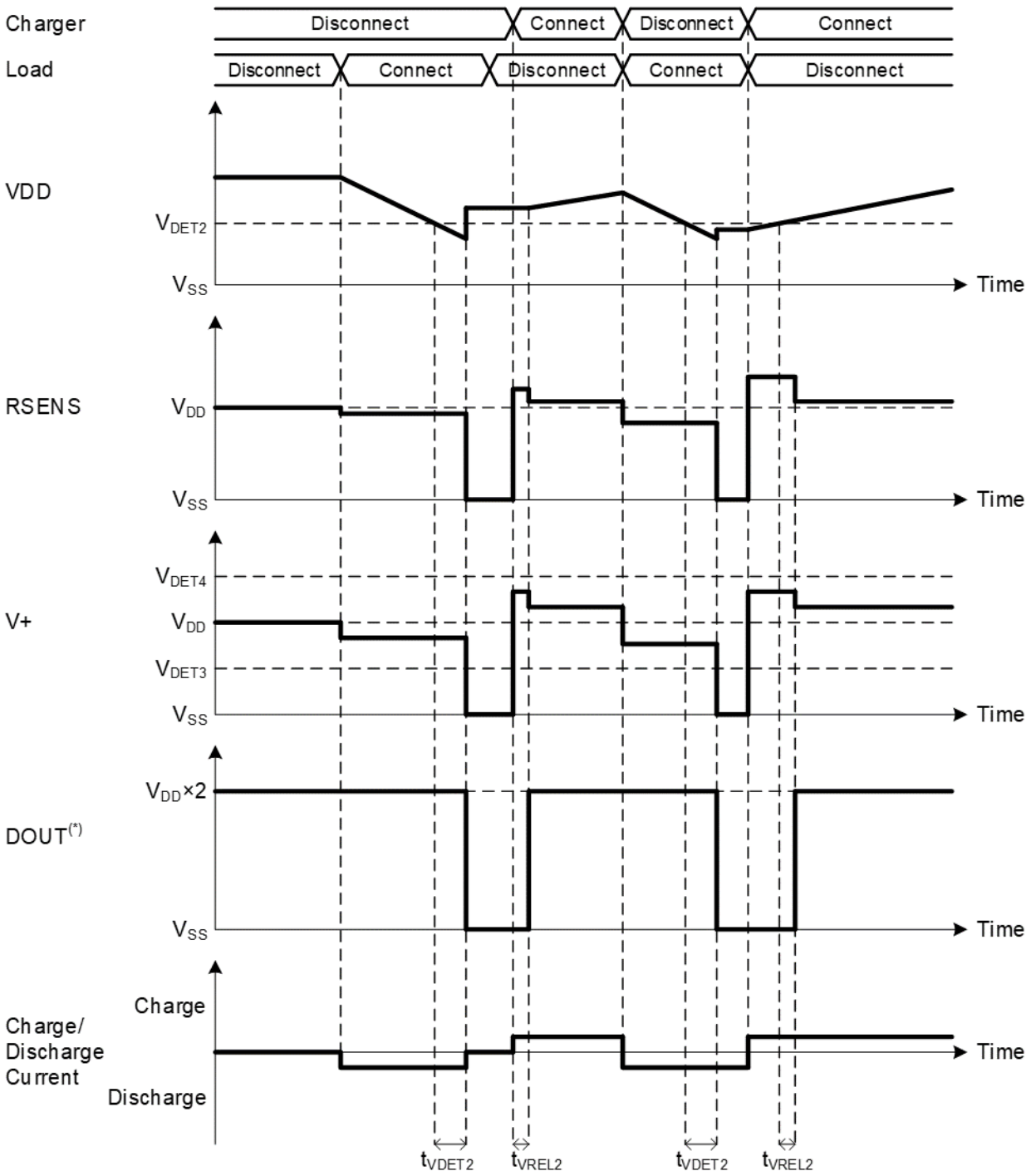
This IC features the internal charge pump that boosts the High level of the COUT and the DOUT pins to approximately twice the voltage of the VDD pin. The charge pump stops when the IC enters the standby mode.
The voltage boost on the COUT and DOUT pins can be detected by the detection voltage for COUT / DOUT boost voltage (V_{BSTDET}).

Timing Chart



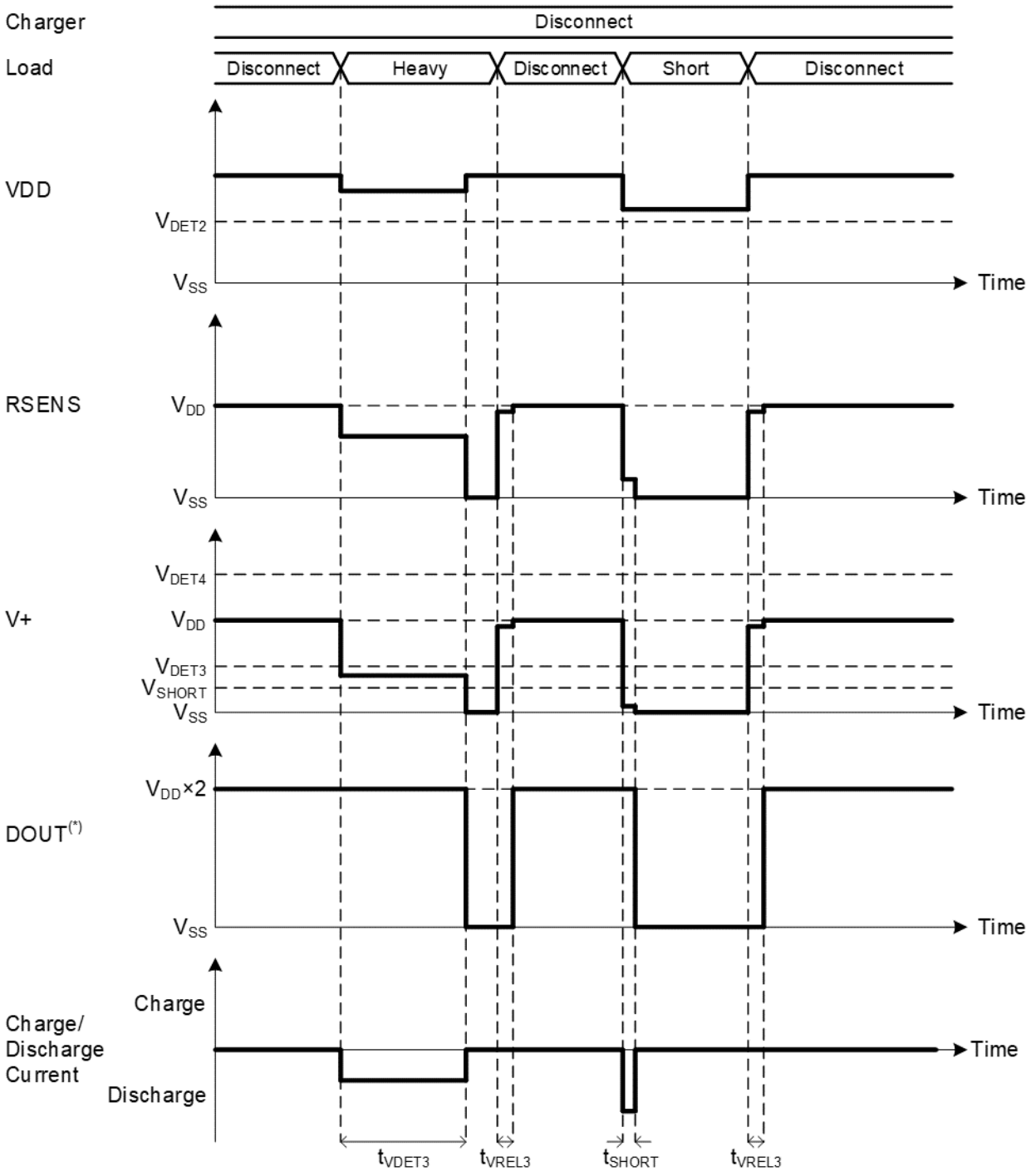
Overcharge Detector Timing Diagram

(*) The COUT pin output is an approximate value of VDD×2 but it is simplified to draw with a square wave in the diagram.



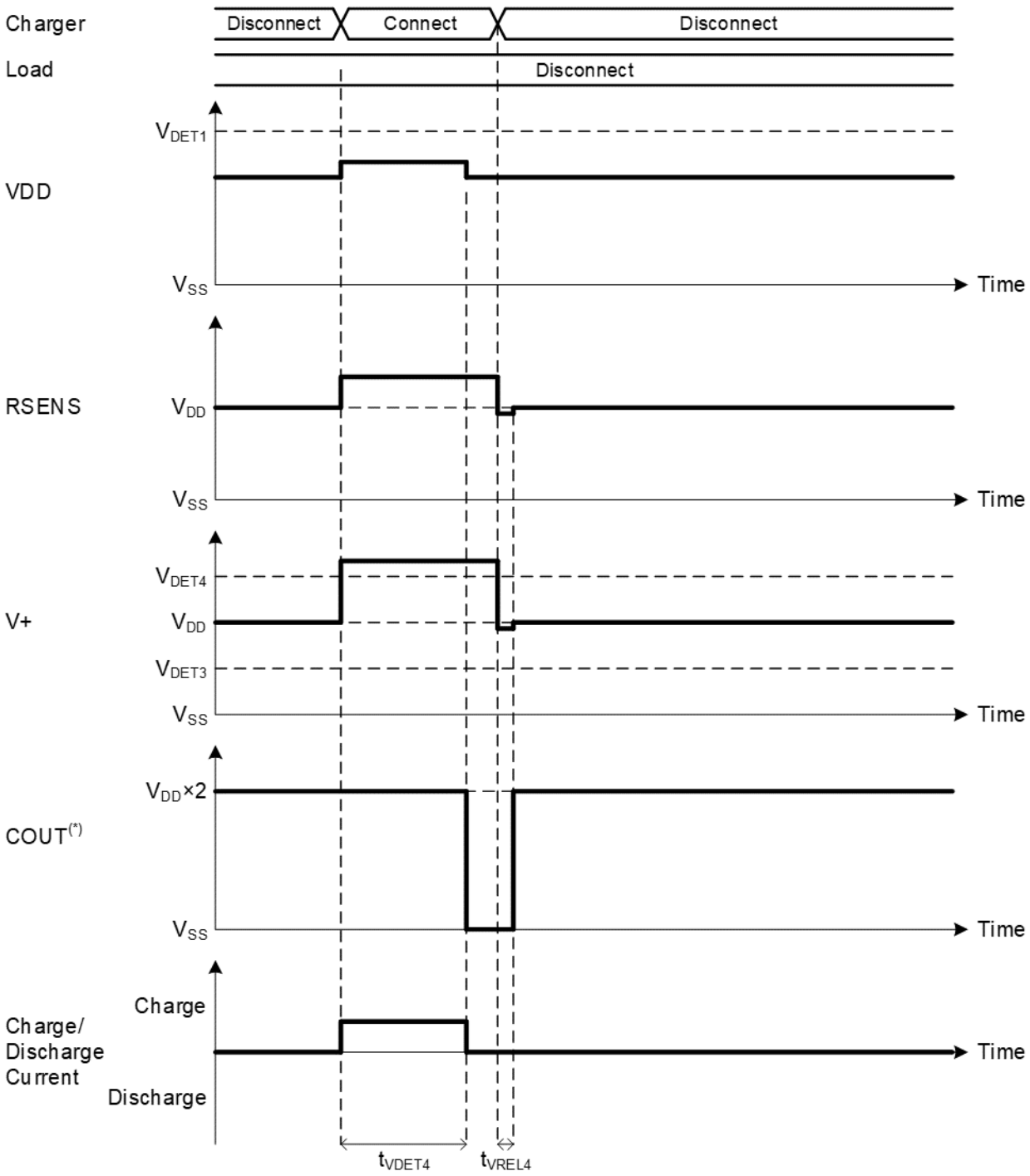
Over-discharge Detector Timing Diagram

(*) The DOUT pin output is an approximate value of VDD×2 but it is simplified to draw with a square wave in the diagram.



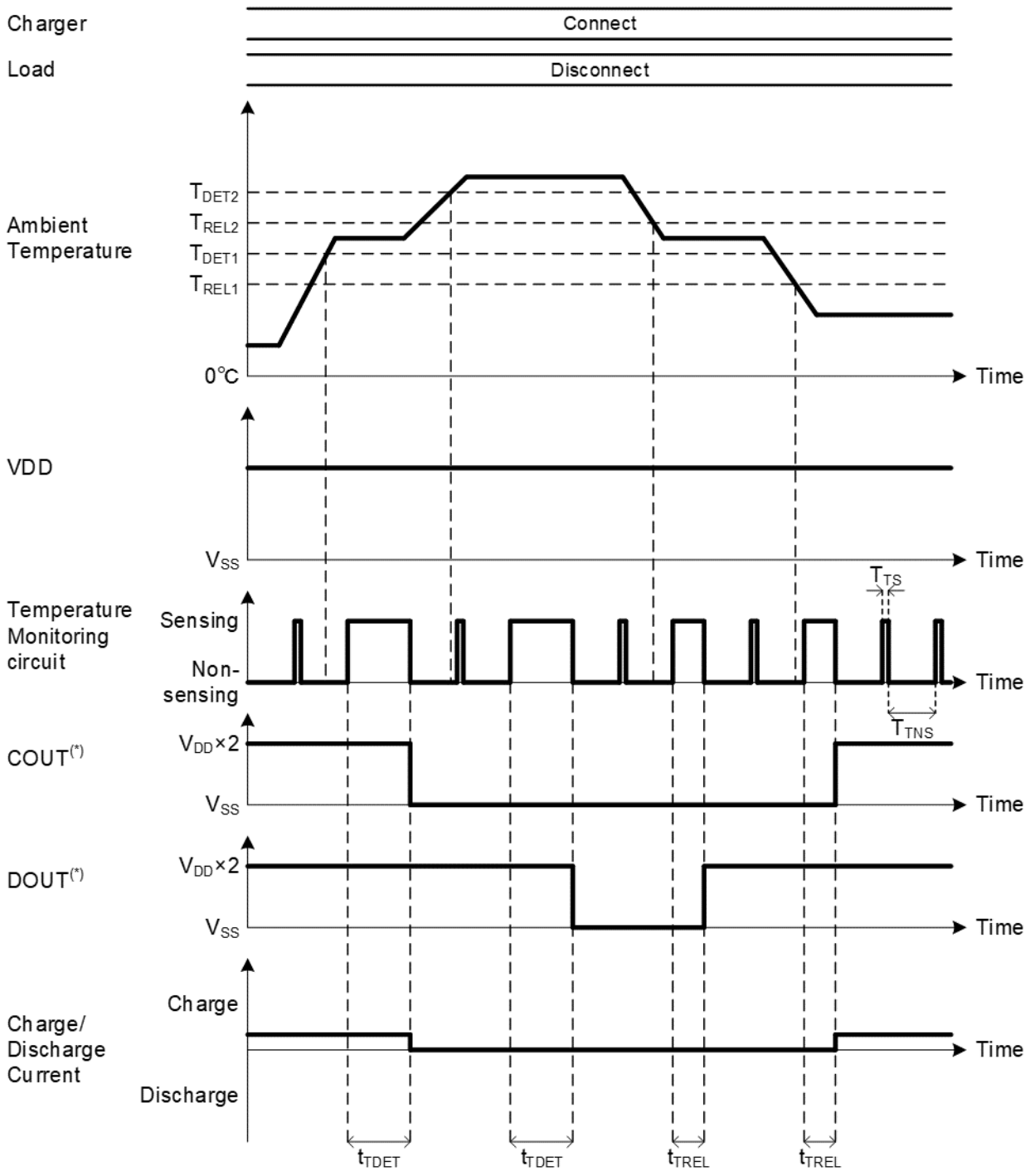
Discharge Overcurrent Detector (Auto Release Type) and Short Circuit Timing Diagram

(*) The DOUT pin output is an approximate value of VDD×2 but it is simplified to draw with a square wave in the diagram.



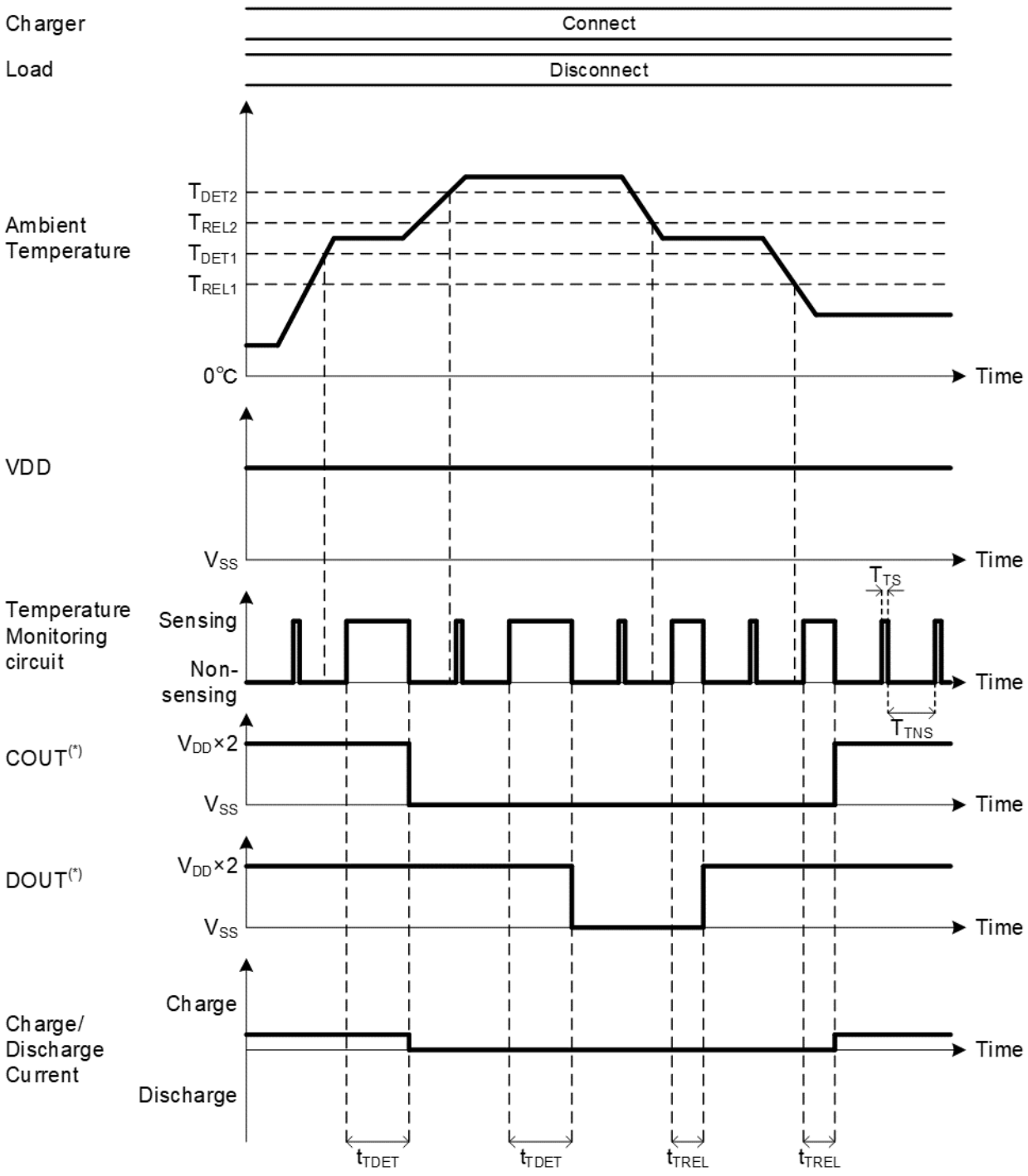
Charge Overcurrent Detector Timing Diagram

(*) The COUT pin output is an approximate value of VDD×2 but it is simplified to draw with a square wave in the diagram.



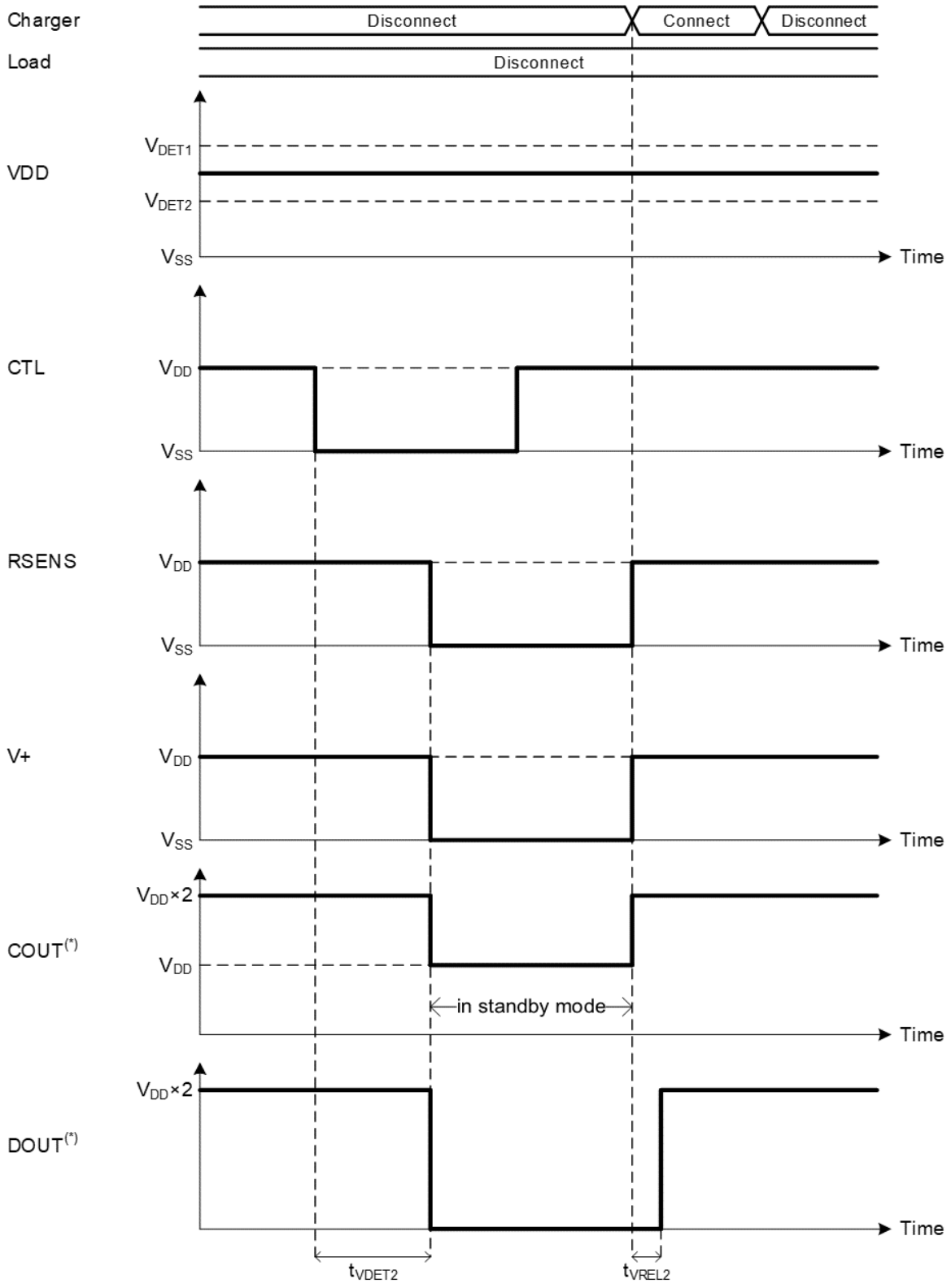
Temperature Protection with Charger Timing Diagram

(*) Each output of the COUT and the DOUT pins is an approximate value of VDD×2 but it is simplified to draw with a square wave in the diagram.



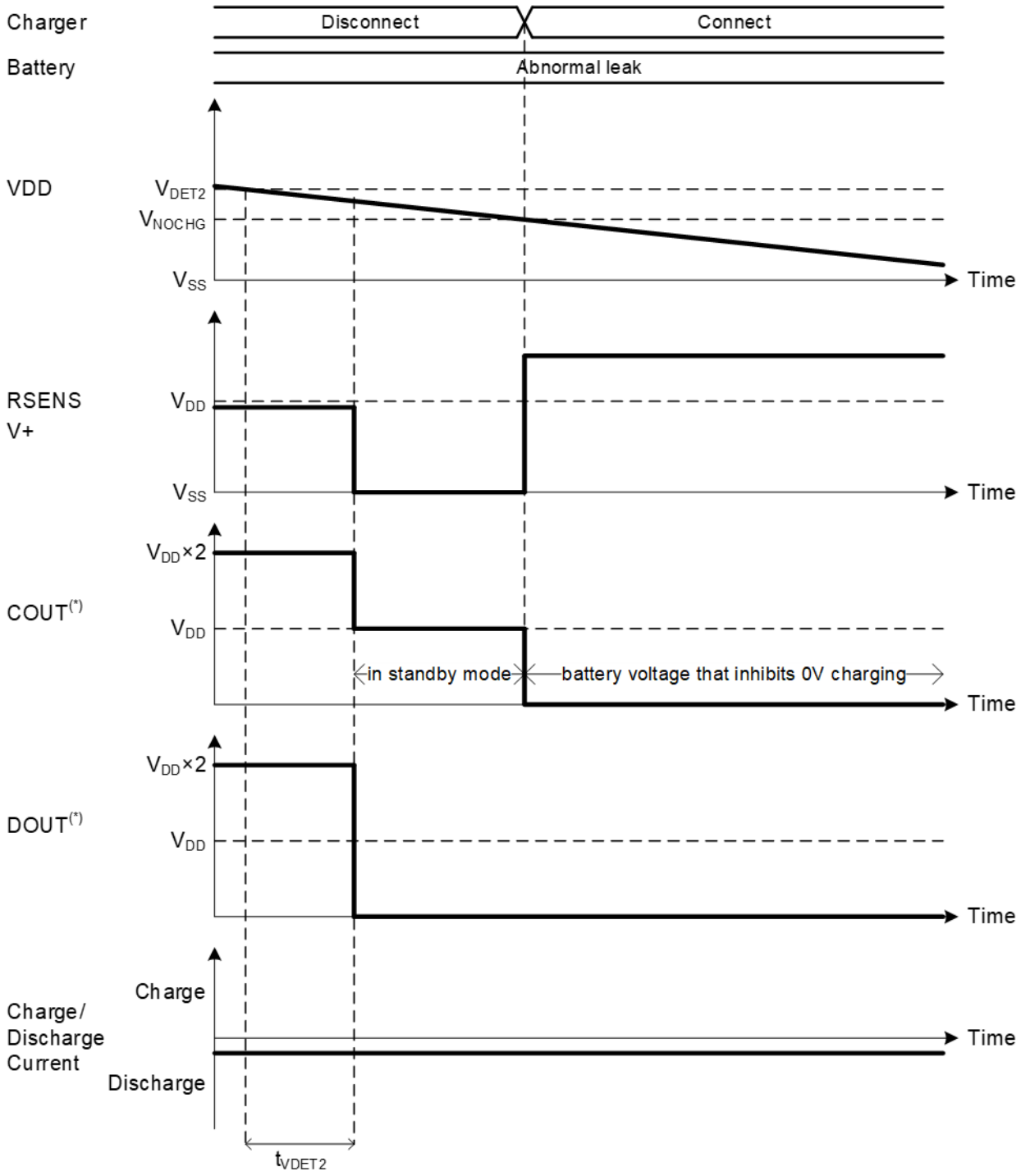
Temperature Protection with Load Timing Diagram

(*) Each output of the COUT and the DOUT pins is an approximate value of VDD×2 but it is simplified to draw with a square wave in the diagram.



Forced Over-discharge Detection by CTL Pin Timing Diagram

(*) Each output of the COUT and the DOUT pins is an approximate value of VDD×2 but it is simplified to draw with a square wave in the diagram.

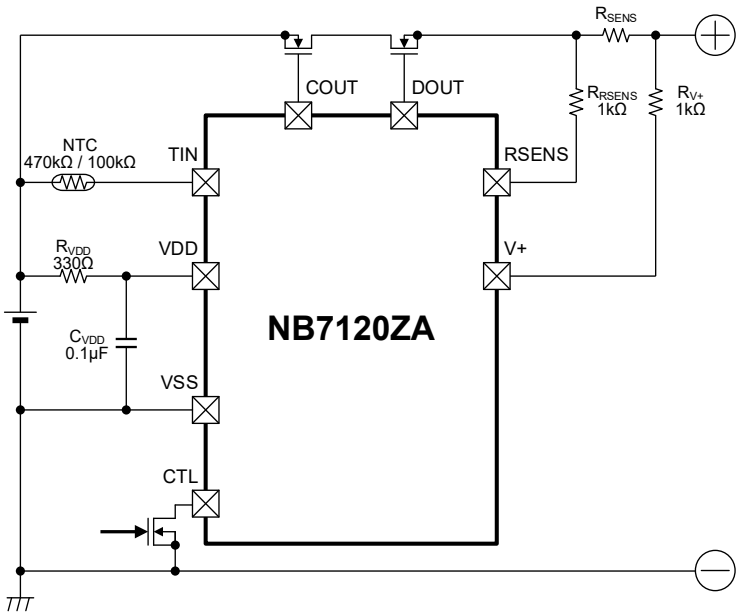


Maximum Operating Voltage at Charging Inhibition (V_{NOCHG}) Timing Diagram

(*) Each output of the COUT and the DOUT pins is an approximate value of VDD×2 but it is simplified to draw with a square wave in the diagram.

APPLICATION INFORMATION

Typical Application Circuit



NB7120ZA Typical Application Circuit

The voltage flucuation is stabilized by R_{VDD} and C_{VDD}. If R_{VDD} is too large, the detection voltage rises by the conduction current at detection. To stabilize the operation, it is recommended to use a resistor of 330Ω or less for R_{VDD} and a capacitor of 0.01µF to 1.00µF for C_{VDD}.

When the R_{SENS} of the resistor sensing the overcurrent is too large, the power loss also become large. If the R_{SENS} is inappropriate for the overcurrent, the power loss may exceed the allowable loss of the R_{SENS}. The appropriate R_{SENS} should be selected according to the cell specifications.

In addition, when a reverse charger is connected, the external resistors must meet the following requirements to suppress the current flowing from the pack+ side pin to the VDD pin.

Reverse Charge Current Path	Recommended Resistance Conditions
From RSENS pin to VSS pin	$R_{V+} = R_{RSENS} = 1k\Omega$ Note
From V+ pin to VSS pin	

Note: If R_{V+} is larger than the requirement, charger connection may not be recognized that is required to release from some abnormal detection sates.

The NTC thermistor with the following characteristics is required.

Vendor	muRata	
Part Number	NCP02WF474F05RH	NCP03WF104F05RL
Resistance	470kΩ±1% (25°C)	100kΩ±1% (25°C)
B-Constant	4250K ±1%	

This application circuit diagram is an example. The performance of the circuit depends on the PCB layout and external components. In the actual application, fully evaluation is required.

TECHNICAL NOTES

A peripheral component or the device mounted on PCB should not exceed a rated voltage, a rated current or a rated power. When designing a peripheral circuit, please be fully aware of the following points.

- Please evaluate the product at the PCB level before use, as some symptoms may remain that cannot be confirmed by the evaluation at the IC level.
- When using any coating or underfill to improve moisture resistance or joining strength, evaluate them adequately before using. In certain materials or coating conditions, corrosion by contained constituents, current leakage by moisture absorption, crack and delamination by physical stress can happen. If the curing temperature of the coating material or underfill material exceeds the absolute maximum rating, the electrical characteristics of this product may change.
- When performing X-ray inspection in mass production process and evaluation build stage such as the product functions and characteristics confirmation, please confirm X-ray irradiation does not exceed 1.5Gy (absorbed dose for air).

Nisshinbo Micro Devices Inc.

NB7120ZA CodeList

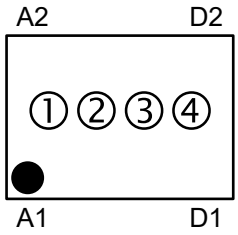
	Set Voltage [V] / Delay Time [ms]											Set Temperature [°C] / Delay Time [ms]					Optional Function							
	V_{DET1} t_{VDET1}	- t_{VREL1}	V_{DET2} t_{VDET2}	- t_{VREL2}	V_{DET3} t_{VDET3}	- t_{VREL3}	V_{DET4} t_{VDET4}	- t_{VREL4}	V_{SHORT} t_{SHORT}	V_{NOCHG} -	Unit	$T_{TDET1/2}$ $t_{TDET1/2}$	$T_{TREL1/2}$ $t_{TREL1/2}$	- t_{TS}	- t_{TNS}	Unit	Overcharge Release	Over-discharge Release	Discharge Overcurrent Release	0V Battery Charging	Charge Overcurrent Detection	Discharge Overcurrent Release	Overcurrent Release Option	NTC Thermistor [kΩ]
NB7120ZA601EZ	4.5	-	2.4	-	0.015	-	-0.012	-	0.04	1.5	V	75	65	-	-	°C	Latch	Latch	Auto Release	Inhibition	Available	RSENS	Type2	100
	1024	16	128	1.1	256	1.1	8	1.1	0.28	-	ms	1024	128	10	528	ms								
NB7120ZA601FZ	4.5	-	2.4	-	0.015	-	-0.012	-	0.04	1.5	V	75	65	-	-	°C	Latch	Latch	Auto Release	Inhibition	Available	RSENS	Type2	100
	1024	2	128	1.1	256	1.1	8	1.1	0.28	-	ms	1024	128	10	528	ms								
NB7120ZA602FZ	4.55	-	2.4	-	0.015	-	-0.01	-	0.04	1.5	V	75	65	-	-	°C	Latch	Latch	Auto Release	Inhibition	Available	RSENS	Type2	470
	1024	2	128	1.1	256	1.1	8	1.1	0.28	-	ms	1024	128	10	528	ms								
NB7120ZA603FZ	4.55	-	3.31	-	0.012	-	-0.01	-	0.032	1.5	V	75	65	-	-	°C	Latch	Latch	Auto Release	Inhibition	Available	RSENS	Type2	470
	1024	2	128	1.1	256	1.1	8	1.1	0.28	-	ms	1024	128	10	528	ms								
NB7120ZA604FZ	4.24	-	2.4	-	0.028	-	-0.028	-	0.07	1.6	V	70	65	-	-	°C	Latch	Latch	Auto Release	Inhibition	Available	RSENS	Type2	470
	1024	2	128	1.1	256	1.1	8	1.1	0.28	-	ms	1024	128	10	528	ms								
NB7120ZA605DZ	4.505	-	2.395	-	0.015	-	-0.009	-	0.04	1.55	V	75	65	-	-	°C	Latch	Latch	Auto Release	Inhibition	Available	RSENS	Type2	470
	4096	16	32	1.1	32	1.1	16.5	1.1	0.28	-	ms	4096	128	10	90	ms								
NB7120ZA606FZ	4.55	-	2.2	-	0.04	-	-0.035	-	0.075	1.5	V	75	65	-	-	°C	Latch	Latch	Auto Release	Inhibition	Available	RSENS	Type2	470
	1024	2	128	1.1	256	1.1	8	1.1	0.28	-	ms	1024	128	10	528	ms								
NB7120ZA607FZ	4.55	-	2.4	-	0.015	-	-0.012	-	0.04	1.5	V	75	65	-	-	°C	Latch	Latch	Auto Release	Inhibition	Available	RSENS	Type2	470
	1024	2	128	1.1	256	1.1	8	1.1	0.28	-	ms	1024	128	10	528	ms								
NB7120ZA608FZ	4.55	-	2.4	-	0.008	-	-0.008	-	0.025	1.5	V	75	65	-	-	°C	Latch	Latch	Auto Release	Inhibition	Available	RSENS	Type2	470
	1024	2	128	1.1	256	1.1	8	1.1	0.28	-	ms	1024	128	10	528	ms								

Please contact our sales representatives if required a product code other than the above combinations.

NB7120 ZA xxxxx E2 S

- ZA: Package Type (ZA: WLCSP)
- xxxxx: Specific code
- E2: Orientation in taping pocket
- S: Grade

PKG: WLCSP-8-P15



①②: Product code (See the table below)

③④: Lot No. (series) 00,01,...,09,0A,...,0Y,10,...,9Y,A0,A1,...,AY,C0,...,YY (except B,D,I,M,O,Q,S,W,Z)

NOTICE

There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used.
In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

Product Name	①②
NB7120ZA601EZ	K0
NB7120ZA601FZ	K5
NB7120ZA602FZ	K1
NB7120ZA603FZ	K2
NB7120ZA604FZ	K3
NB7120ZA605DZ	K4
NB7120ZA606FZ	K6
NB7120ZA607FZ	K7
NB7120ZA608FZ	K8

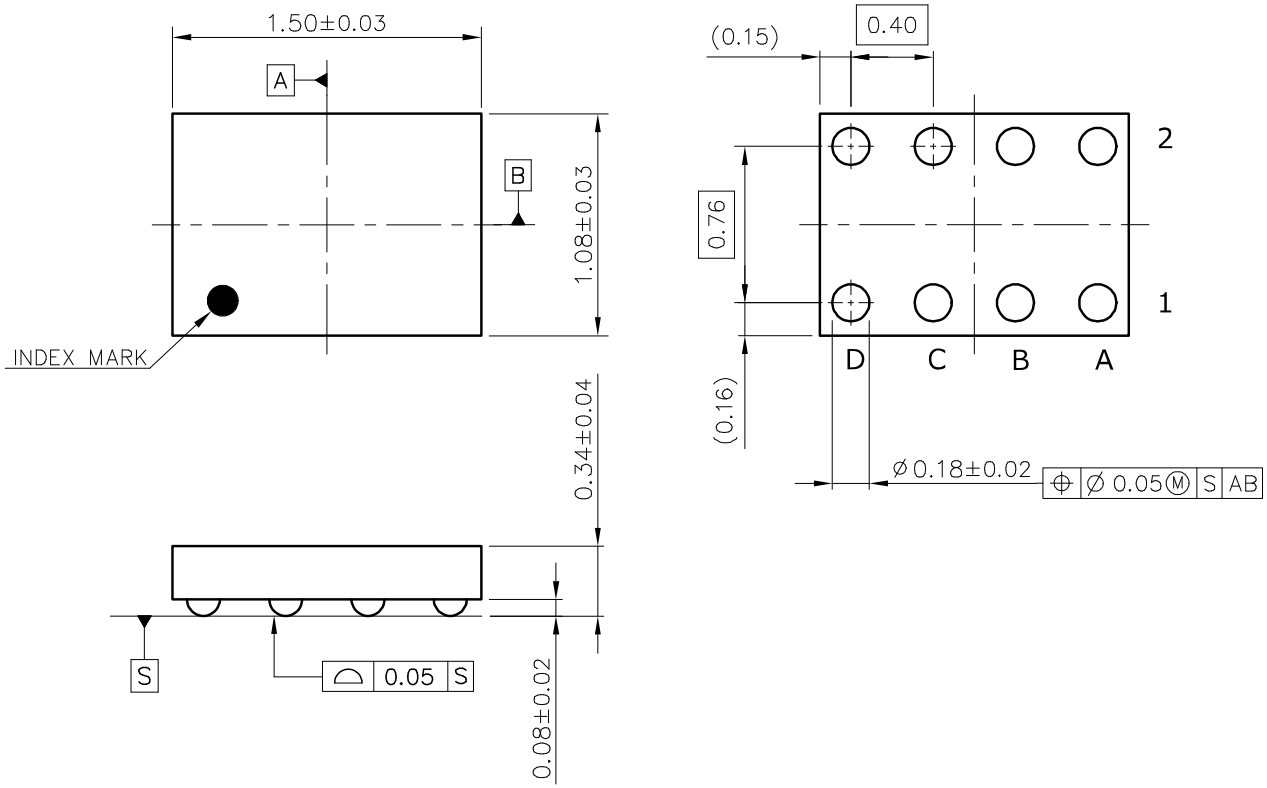
Nisshinbo Micro Devices Inc.

WLCSP-8-P15

PI-WLCSP-8-P15-E-B

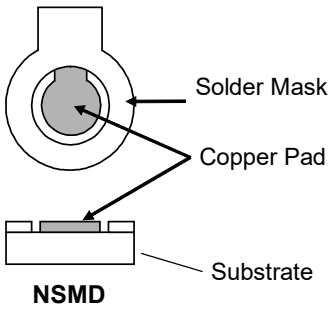
■ PACKAGE DIMENSIONS

UNIT: mm



■ EXAMPLE OF SOLDER PADS DIMENSIONS

Recommended Land Pattern



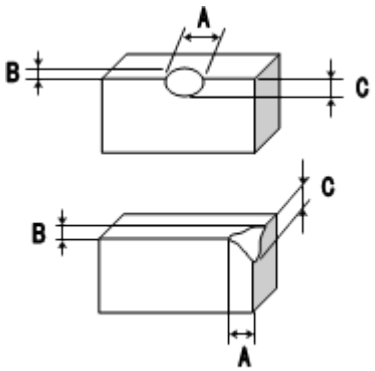
NSMD Pad Definition		
Pad definition	Copper Pad	Solder Mask Opening
NSMD (Non-Solder Mask defined)	0.18mm	MIN. 0.28mm

*) Pad Layout and size can modify by customers material, equipment and method.
*) Please adjust pad layout according to your conditions.
*) Recommended Stencil Aperture Size: ϕ0.26mm

Nisshinbo Micro Devices Inc.

WLCSP-8-P15

■ Visual Inspection Criteria

No.	Inspection Items	Inspection Criteria	Figures
1	Package chipping	A ≥ 0.2mm is rejected B ≥ 0.2mm is rejected C ≥ 0.2mm is rejected And, Package chipping to Si surface and to bump is rejected.	
2	Si surface chipping	A≥0.2mm is rejected B≥0.2mm is rejected C≥0.2mm is rejected But, even if A ≥ 0.2mm, B ≤ 0.1mm is acceptable.	
3	No bump	No bump is rejected.	
4	Marking miss	To reject incorrect marking, such as another product name marking or another lot No. marking.	
5	No marking	To reject no marking on the package.	
6	Reverse direction of marking	To reject reverse direction of marking character.	
7	Defective marking	To reject unreadable marking. (Microscope: X15/ White LED/ Viewed from vertical direction)	
8	Scratch	To reject unreadable marking character by scratch. (Microscope: X15/ White LED/ Viewed from vertical direction)	
9	Stain and Foreign material	To reject unreadable marking character by stain and foreign material. (Microscope: X15/ White LED/ Viewed from vertical direction)	

Nisshinbo Micro Devices Inc.

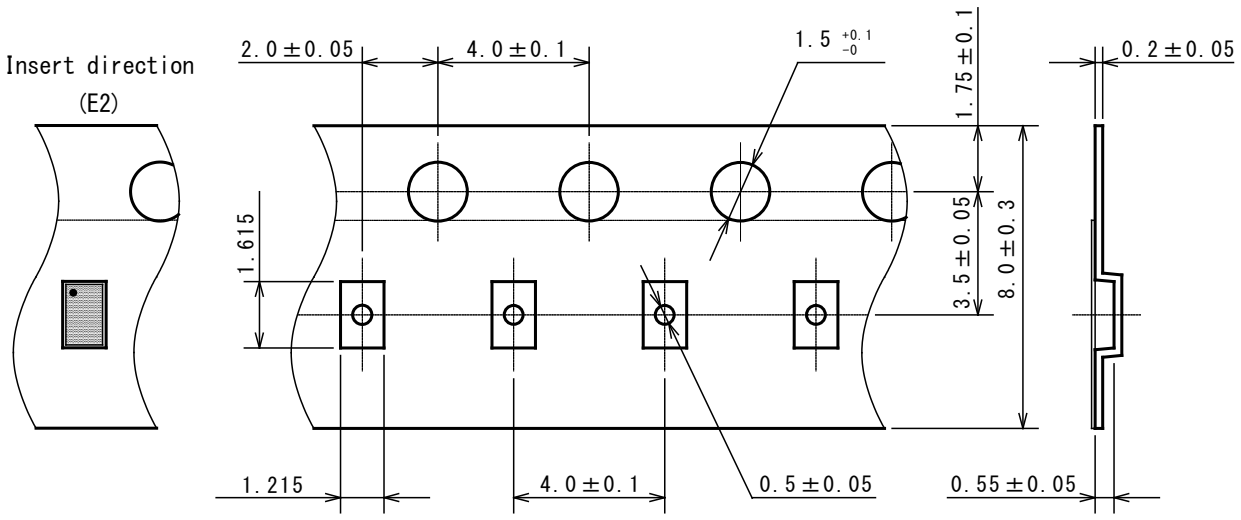
WLCSP-8-P15

PI-WLCSP-8-P15-E-B

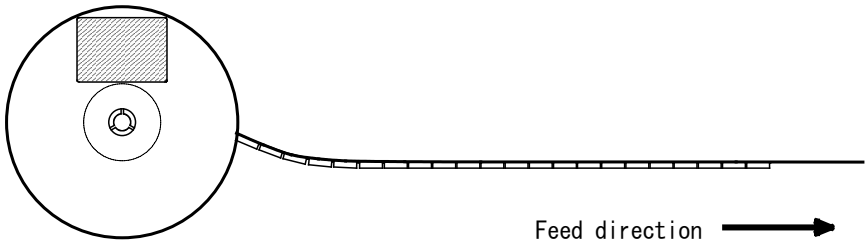
■ PACKING SPEC

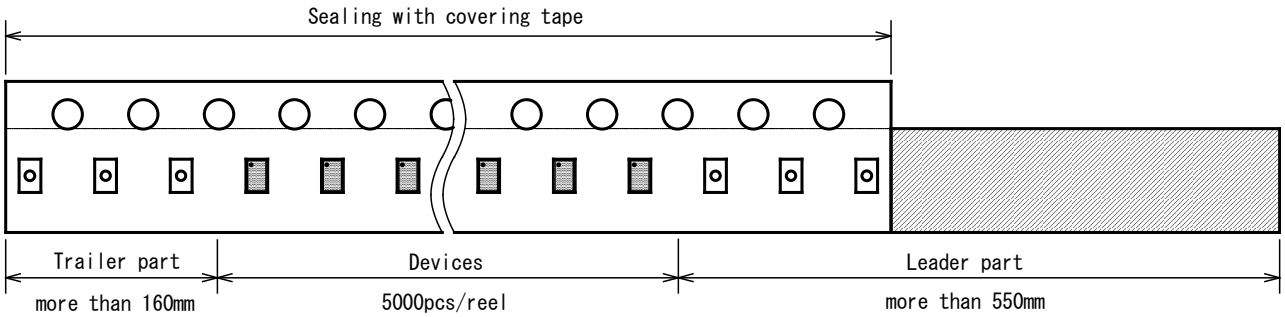
UNIT: mm

(1) Taping dimensions / Insert direction

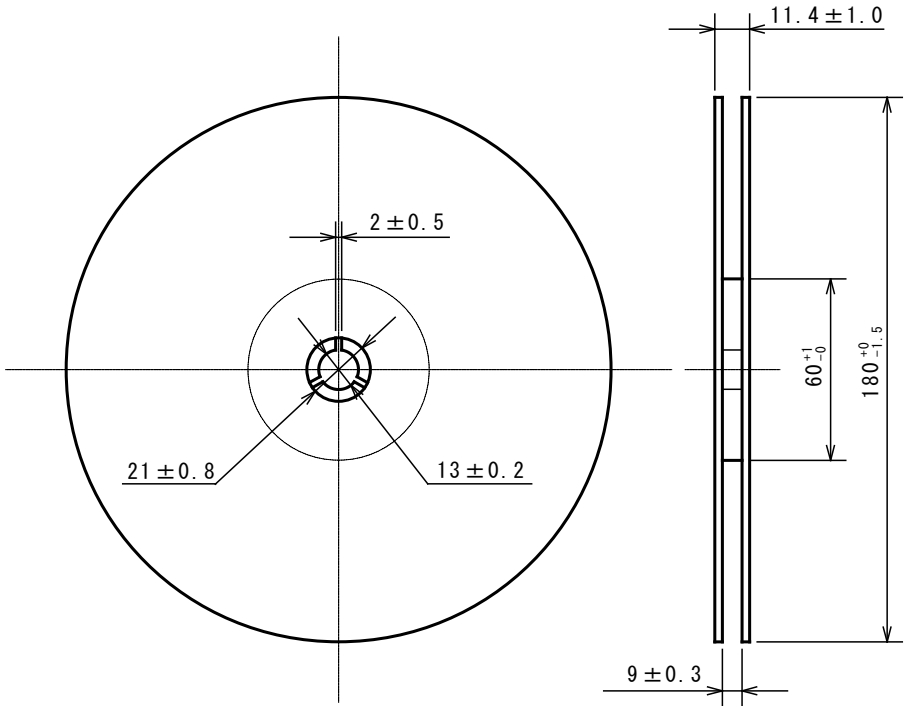


(2) Taping state





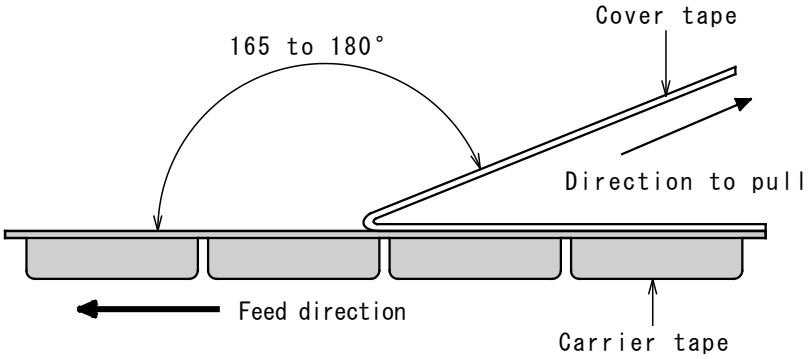
(3) Reel dimensions



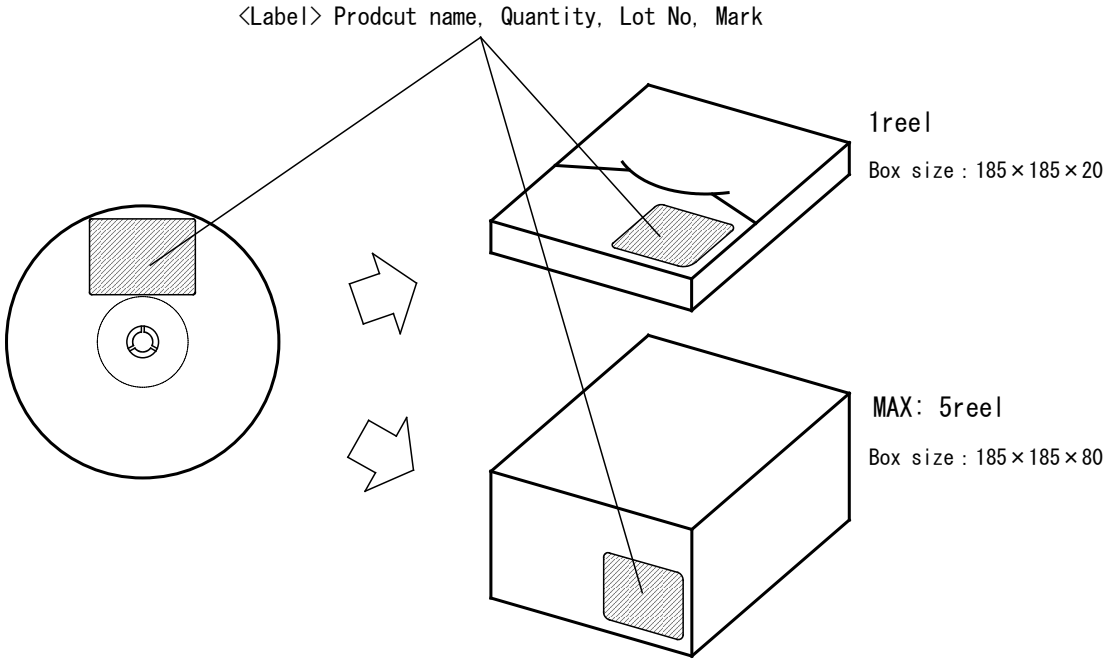
(4) Peeling strength

Peeling strength of cover tape

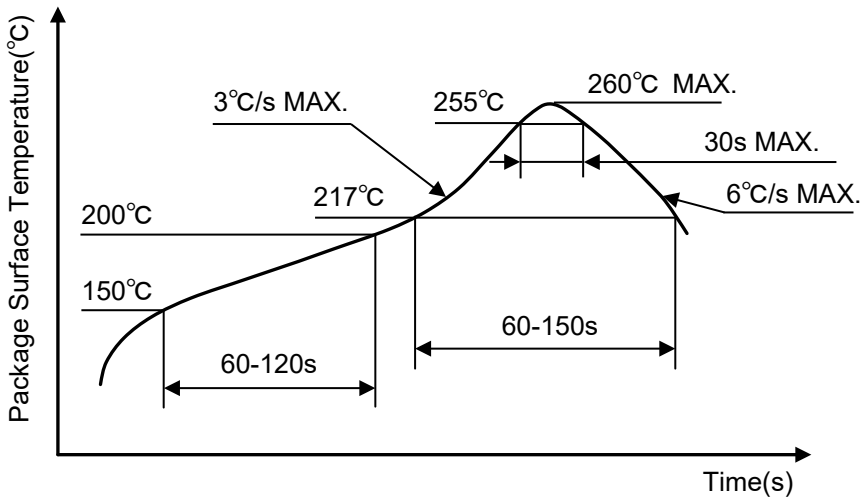
・Peeling angle	165 to 180° degrees to the taped surface.
・Peeling speed	300mm/min
・Peeling strength	0.1 to 1.0N



(5) Packing state



■ **HEAT-RESISTANCE PROFILES**



Reflow profile

REVISION HISTORY

Date	Version		Changes
March 25, 2024	1.0	-	First official datasheet release
October 30, 2024	1.1	a	Added the delay codes of E and F and the function code Z in *the PRODUCT NAME INFORMATION chapter*. Changed Typ. and Max. values of V_{REL2} as follows: Typ. V_{DET2}+0.008, Max.V_{DET2}+0.051; Corrected the accuracy of V_{SHORT} from ±0.025 to ±0.0025 in *the Electrical Characteristics chapter.* Added the NTC of 100kΩ in t*he Electrical Characteristics and the Application Information chapter*.
January 27, 2025			Added 601EZ,601FZ,602FZ,603FZ,604FZ, and 605DZ in the Product Code List.
April 3, 2025		b	Added 606FZ in the Product Code List and the Marking Specification.
June 17, 2025		c	Added 607FZ in the Product Code List and the Marking Specification.
November 10, 2025	1.2	a	Added 608FZ in the Product Code List and the Marking Specification. Updated the block diagram.

1. The products and the product specifications described in this document are subject to change or discontinuation of production without notice for reasons such as improvement. Therefore, before deciding to use the products, please refer to our sales representatives for the latest information thereon.
2. The materials in this document may not be copied or otherwise reproduced in whole or in part without the prior written consent of us.
3. This product and any technical information relating thereto are subject to complementary export controls (so-called KNOW controls) under the Foreign Exchange and Foreign Trade Law, and related politics ministerial ordinance of the law. (Note that the complementary export controls are inapplicable to any application-specific products, except rockets and pilotless aircraft, that are insusceptible to design or program changes.) Accordingly, when exporting or carrying abroad this product, follow the Foreign Exchange and Foreign Trade Control Law and its related regulations with respect to the complementary export controls.
4. The technical information described in this document shows typical characteristics and example application circuits for the products. The release of such information is not to be construed as a warranty of or a grant of license under our or any third party's intellectual property rights or any other rights.
5. The products listed in this document are intended and designed for use as general electronic components in standard applications (office equipment, telecommunication equipment, measuring instruments, consumer electronic products, amusement equipment etc.). Those customers intending to use a product in an application requiring extreme quality and reliability, for example, in a highly specific application where the failure or misoperation of the product could result in human injury or death should first contact us.
    - Aerospace Equipment
    - Equipment Used in the Deep Sea
    - Power Generator Control Equipment (nuclear, steam, hydraulic, etc.)
    - Life Maintenance Medical Equipment
    - Fire Alarms / Intruder Detectors
    - Vehicle Control Equipment (automotive, airplane, railroad, ship, etc.)
    - Various Safety Devices
    - Traffic control system
    - Combustion equipment

    In case your company desires to use this product for any applications other than general electronic equipment mentioned above, make sure to contact our company in advance. Note that the important requirements mentioned in this section are not applicable to cases where operation requirements such as application conditions are confirmed by our company in writing after consultation with your company.
6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order to prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire containment feature and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.
7. The products have been designed and tested to function within controlled environmental conditions. Do not use products under conditions that deviate from methods or applications specified in this datasheet. Failure to employ the products in the proper applications can lead to deterioration, destruction or failure of the products. We shall not be responsible for any bodily injury, fires or accident, property damage or any consequential damages resulting from misuse or misapplication of the products.
8. Quality Warranty
    8-1. Quality Warranty Period
    In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.
    8-2. Quality Warranty Remedies
    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
    Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
    8-3. Remedies after Quality Warranty Period
    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
9. Anti-radiation design is not implemented in the products described in this document.
10. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
11. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
12. Warning for handling Gallium and Arsenic (GaAs) products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.
13. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.

NISSHINBO

Nisshinbo Micro Devices Inc.

Official website
https://www.nisshinbo-microdevices.co.jp/en/

Purchase information
https://www.nisshinbo-microdevices.co.jp/en/buy/