Spread Spectrum Modulation (SSFM) Oscillator IC with External Synchronization for Switching Regulators

■ FEATURES

- Anti-phase outputs to reduce ripple current 0°, 180°
- External clock synchronization frequency 120 kHz to 2.4 MHz
- SSFM for improved EMI performance
- Frequency spreading ±4.4%
- Selectable modulation rate $f_{CLK}/2048$, $f_{CLK}/512$, $f_{CLK}/128$
- Operating voltage range 2.7 V to 5.5 V
- Standby function
- Package MSOP8

■ APPLICATIONS

- External synchronization signal of switching regulator

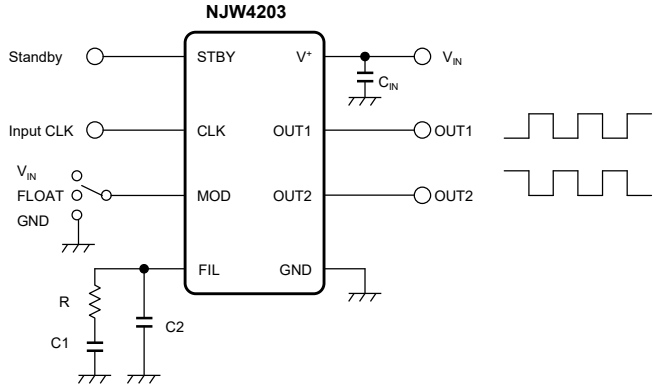
■ DESCRIPTION

The NJW4203 is an oscillator with spread spectrum frequency modulation (SSFM) that outputs two types of antiphase shifted by 0° or 180°. The SSFM reduces the peak noise level of EMI.

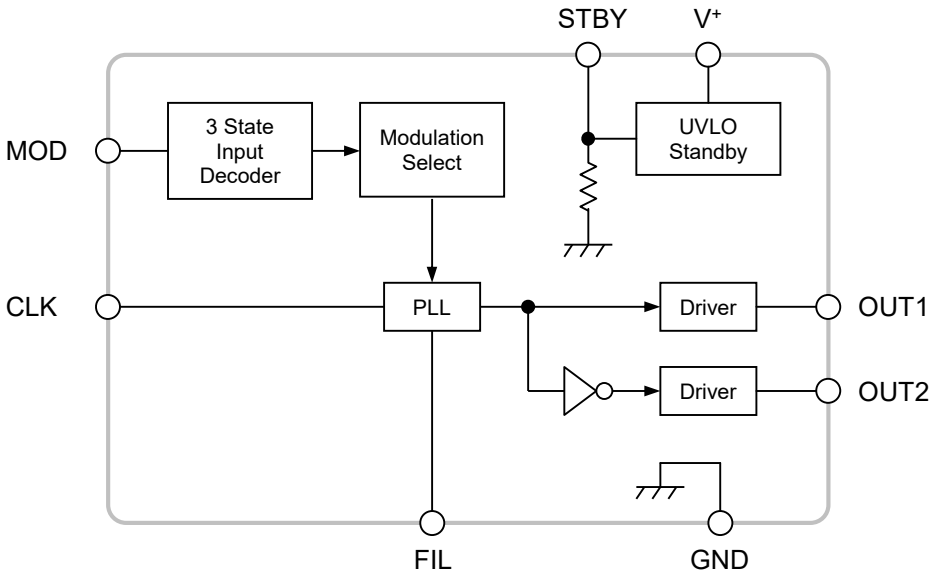
The output clock spreads the frequency at ±4.4% of the center frequency, and the modulation rate can be selected from $f_{CLK}/2048$, $f_{CLK}/512$, or $f_{CLK}/128$. In addition, a PLL control system improves the stability of the output clock.

The NJW4203 operates from 120 kHz to 2.4 MHz, and is suitable for the external synchronization signal application of the switching regulators.

■ TYPICAL APPLICATION

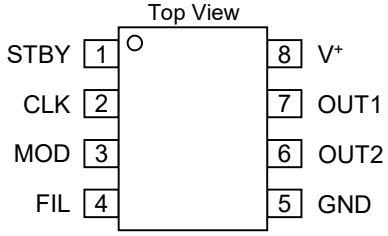


■ BLOCK DIAGRAM



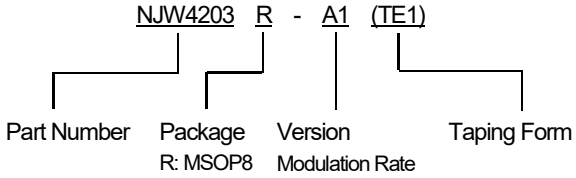
■ PIN CONFIGURATION

MSOP8
Top View



PIN NO.	NAME	FUNCTION
1	STBY	Standby pin controls the operation and stop of NJW4203. This pin is pulled down to GND with an internal resistor. The STBY pin operates at a high level and goes into standby mode at a low level or open.
2	CLK	Clock signal input pin. This pin operates at an oscillation frequency based with the signal by inputting a clock signal.
3	MOD	Modulation rate selection pin. This pin sets the level of spectrum spread frequency modulation. Pattern A: High level Pattern B: Open (Hi-Z) Pattern C: Low level
4	FIL	C, R connection pin for filter. Connect a resistor and a capacitor for PLL circuit filter.
5	GND	Ground pin
6	OUT2	Output pin of an oscillator. Push-pull output drives the load. Connect to the external synchronization input pin of a switching regulator.
7	OUT1	
8	V^+	Power supply pin. Place the input capacitor as close to the device as possible to reduce the power supply impedance.

■ PRODUCT NAME INFORMATION



■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJW4203R-A1 (TE1)	MSOP8	Yes	Yes	Sn-2Bi	4203A1	21	2000

■ PRODUCT CLASSIFICATION

PRODUCT NAME	VERSION	CLK INPUT FREQUENCY	FREQUENCY SPREADING	MODULATION RATE	PACKAGE
NJW4203R-A1	A1	120 kHz to 2.4 MHz	±4.4%	Pattern A: $f_{CLK}/2048$ Pattern B: $f_{CLK}/512$ Pattern C: $f_{CLK}/128$	MSOP8

Pattern A: MOD pin High
Pattern B: MOD pin Open
Pattern C: MOD pin Low

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+	−0.3 to 7	V
STBY Pin Voltage	V_{STBY}	−0.3 to 6	V
CLK Pin Voltage	V_{CLK}	−0.3 to 7	V
MOD Pin Voltage	V_{MOD}	−0.3 to V^++0.3	V
OUT1/2 Pin Voltage	$V_{OUT/2}$	−0.3 to V^++0.3	V
Power Dissipation (T_a = 25°C) MSOP8	P_D	2-Layer / 4-Layer 500 (1) / 660 (2)	mW
Junction Temperature	T_j	−40 to 150	°C
Storage Temperature	T_{stg}	−50 to 150	°C

(1) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).
(2) 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4), internal Cu area: 74.2 mm × 74.2 mm.

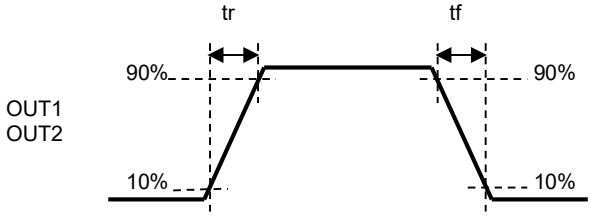
■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Operating Voltage	V^+	2.7 to 5.5	V
STBY Pin Voltage	V_{STBY}	0 to 5.5	V
CLK Pin Voltage	V_{CLK}	0 to 5.5	V
MOD Pin Voltage	V_{MOD}	0 to V^+	V
OUT1/2 Pin Voltage	$V_{OUT1/2}$	0 to V^+	V
External Input Frequency	f_{CLK}	120 to 2400	kHz
Operating Temperature	T_{opr}	−40 to 125	°C

■ **ELECTRICAL CHARACTERISTICS** V^+ = 5 V, T_a = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL CHARACTERISTICS						
Quiescent Current	I_{DD}	R_L = No load, V_{MOD} = Open	-	1.5	2.2	mA
Standby Current	I_{DD_STB}	V_{STBY} = GND	-	-	1	μA
UNDERVOLTAGE LOCKOUT (UVLO)						
ON Threshold Voltage	V_{T_ON}	V_{T_ON} = L → H	2.3	2.5	2.7	V
OFF Threshold Voltage	V_{T_OFF}	V_{T_OFF} = H → L	2.2	2.4	2.6	V
Hysteresis Voltage	V_{HYS}		50	100	-	mV
CLK INPUT						
CLK Pin High Threshold Voltage	V_{THH_CLK}	V_{CLK} = L → H	V^+−0.5	-	V^+	V
CLK Pin Low Threshold Voltage	V_{THL_CLK}	V_{CLK} = H → L	0	-	0.5	V
CLK Pin Input Bias Current	I_{CLK}	V_{CLK} = 5 V	-	-	70	μA
Frequency Spreading	f_{FS}	V_{MOD} = V^+, Open or GND, f_{CLK} = 500 kHz	-	±2.7	±4.4	%
OUTPUT						
Duty Cycle	D_{UTY}	f_{CLK} = 500 kHz	-	50	-	%
Output High Level ON-Resistance	R_{OH}	$I_{O1,2}$ = −4 mA	-	50	80	Ω
Output Low Level ON-Resistance	R_{OL}	$I_{O1,2}$ = +4 mA	-	60	100	Ω
Output Pin Leak Current	I_{LEAK}	V^+ = 5.5 V	−0.1	-	+0.1	μA
Output Rise Time	tr	C_{OUT} = 100 pF	-	20	-	ns
Output Fall time	tf	C_{OUT} = 100 pF	-	22	-	ns
MOD CONTROL						
MOD Pin High Threshold Voltage	V_{THH_MOD}	V_{MOD} = L → H	V^+−0.5	-	V^+	V
MOD Pin Low Threshold Voltage	V_{THL_MOD}	V_{MOD} = H → L	0	-	0.5	V
MOD Pin Impedance at Floating	Z_{FL_MOD}		20	-	-	kΩ
MOD Pin Input Bias Current	I_{MOD}	V_{MOD} = 5 V, 0 V	25	-	100	μA
STANDBY CONTROL						
STBY Pin High Threshold Voltage	V_{THH_STBY}	V_{STBY} = L → H	V^+−0.5	-	V^+	V
STBY Pin Low Threshold Voltage	V_{THL_SYBY}	V_{STBY} = H → L	0	-	0.5	V
STBY Pin Input Bias Current	I_{STBY}	V_{STBY} = 5 V	-	-	90	μA

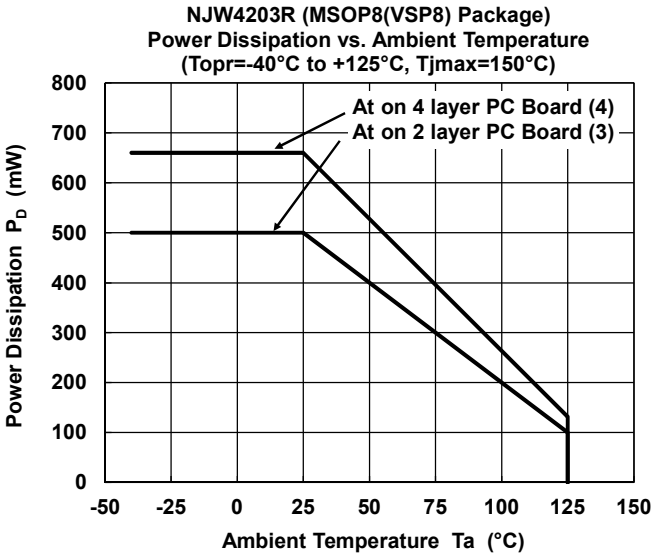
■ OUTPUT WAVEFORM



■ THERMAL CHARACTERISTICS

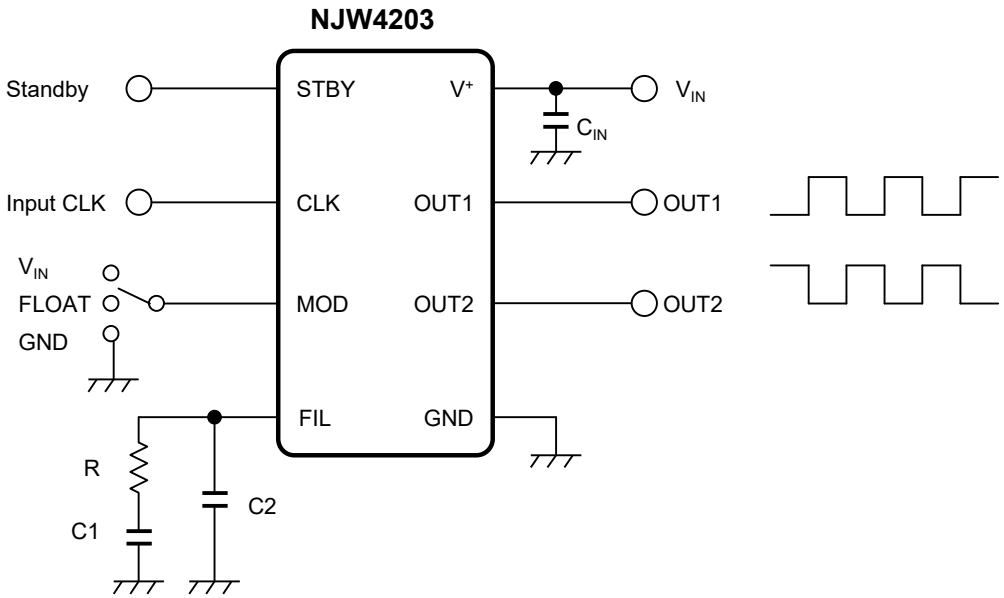
PARAMETER	SYMBOL	VALUE	UNIT
Junction-To-Ambient Thermal Resistance MSOP8	θ_{ja}	2-Layer / 4-Layer 252 (3) / 189 (4)	°C/W
Junction-To-Top of Package Characterization Parameter MSOP8	Ψ_{jt}	2-Layer / 4-Layer 62 (3) / 53 (4)	°C/W

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE



(3) 2-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 2-layer FR-4).
(4) 4-Layer: Mounted on glass epoxy board (76.2 mm × 114.3 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4), internal Cu area: 74.2 mm × 74.2 mm.

■ TYPICAL APPLICATION



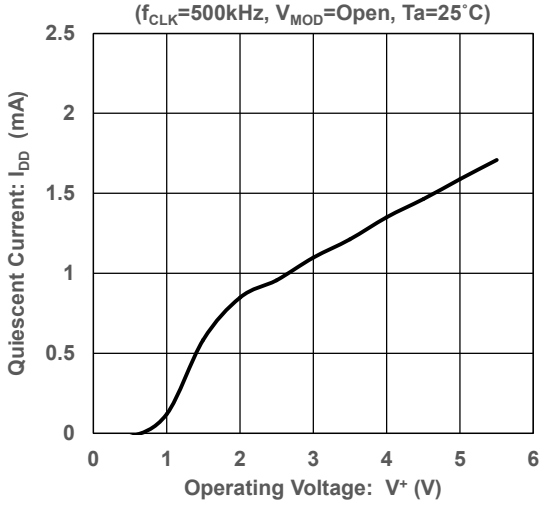
When using at V^+ = 5V, if f_{CLK} = 1.4MHz or higher and operating temperature -20°C or lower, the EMI effect may decrease due to spectrum characteristics. In that case, it is recommended to use at V^+ = 3.3V.

■ TRUTH TABLE

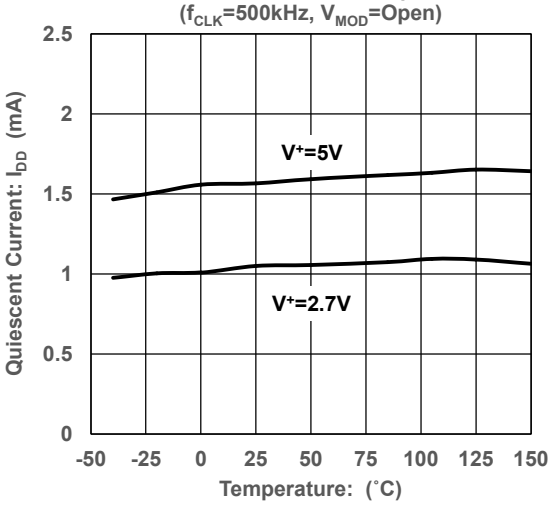
STBY PIN	IC STATUS	MOD PIN	OUT1	OUT2
Open	Standby	-	High-Z	High-Z
GND Short	Standby	-	High-Z	High-Z
High	Operating	High	Modulation Pattern A	Modulation Pattern A
High	Operating	Open	Modulation Pattern B	Modulation Pattern B
High	Operating	Low	Modulation Pattern C	Modulation Pattern C

■ TYPICAL CHARACTERISTICS

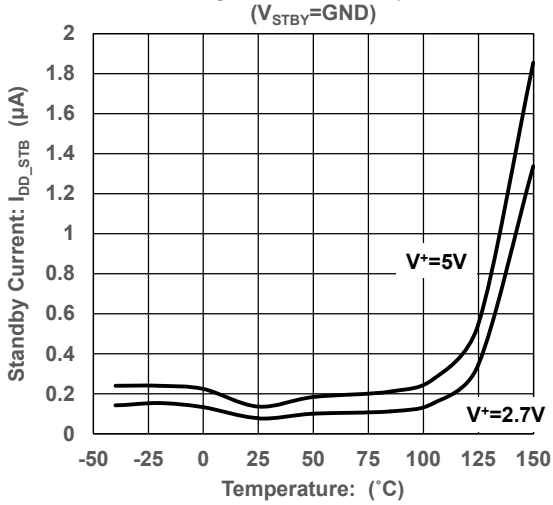
Quiescent Current vs. Operating Voltage
(f_{CLK}=500kHz, V_{MOD}=Open, Ta=25˚C)



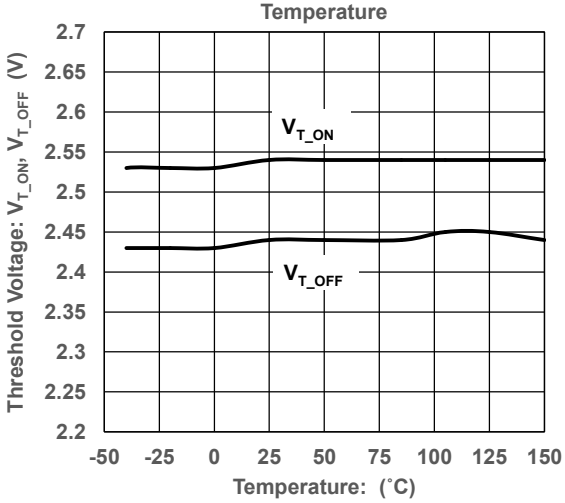
Quescent Current vs. Temperature
(f_{CLK}=500kHz, V_{MOD}=Open)



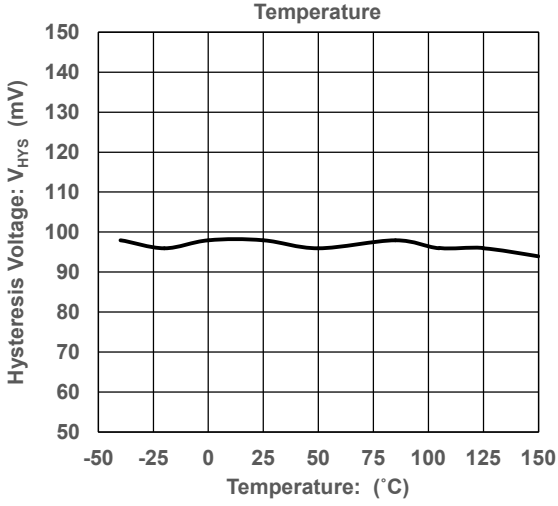
Standby Current vs. Temperature
(V_{STBY}=GND)



Under Voltage Lockout Threshold Voltage vs. Temperature

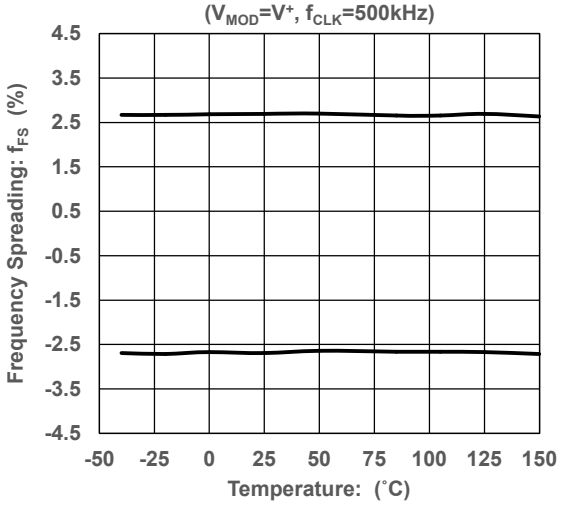


Under Voltage Lockout Hysteresis Voltage vs. Temperature

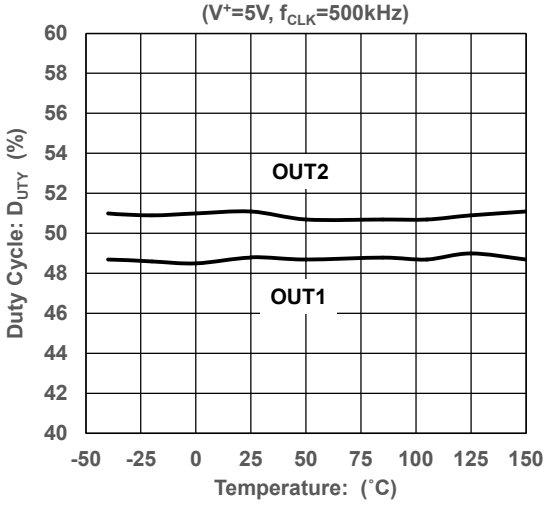


■ TYPICAL CHARACTERISTICS

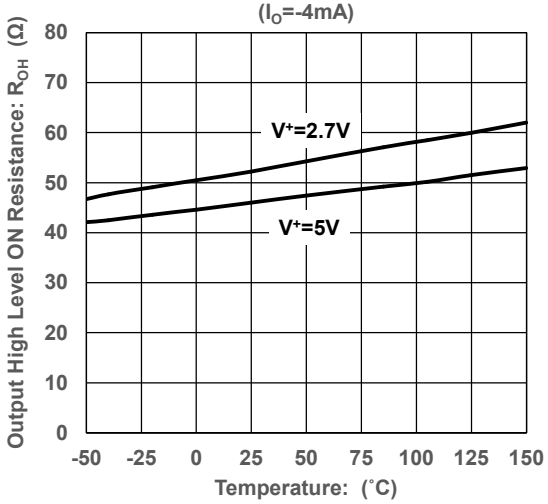
Frequency Spreading vs. Temperature
(V_{MOD}=V^+, f_{CLK}=500kHz)



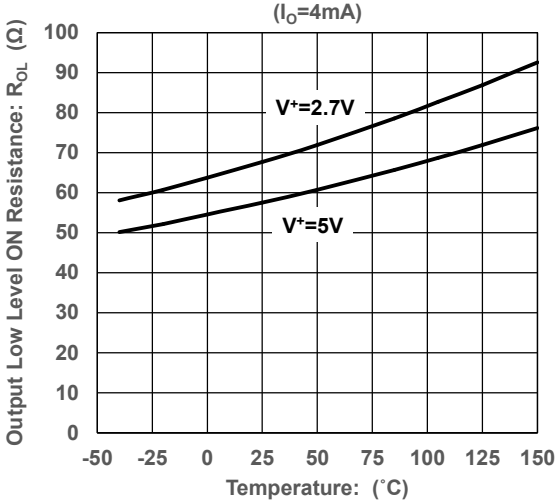
Duty Cycle vs. Temperature
(V^+=5V, f_{CLK}=500kHz)



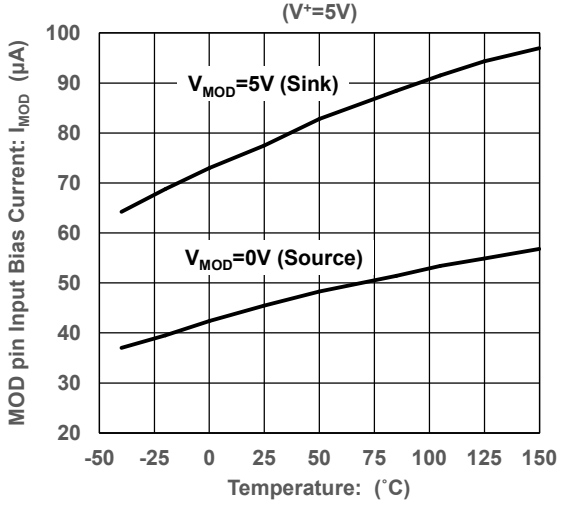
Output High Level ON Resistance vs. Temperature
(I_O=-4mA)



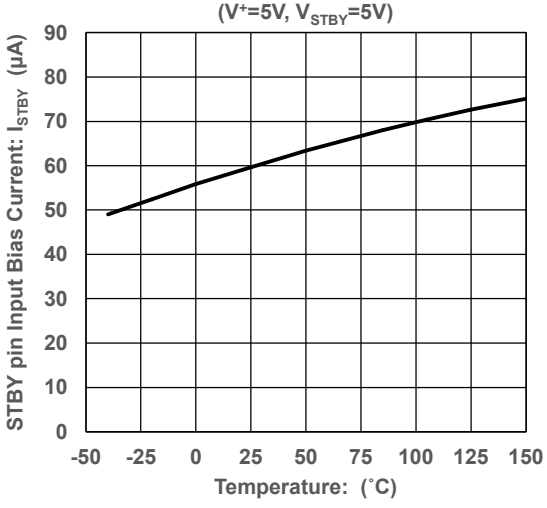
Output Low Level ON Resistance vs. Temperature
(I_O=4mA)



MOD pin Input Bias Current vs. Temperature
(V^+=5V)



STBY pin Input Bias Current vs. Temperature
(V^+=5V, V_{STBY}=5V)



■ APPLICATION NOTE

Functional description of each block

● Operation overview

NJW4203 is an oscillator IC with a spread spectrum function for switching regulators. Outputs a spread spectrum-modulated clock based on the input clock. The output clock spreads the frequency at ± 4.4% max. of the input frequency, and the modulation rate can be selected from f_{CLK} / 2048, f_{CLK} / 512, and f_{CLK} / 128. Frequency spreading profile is shown as Fig.1.

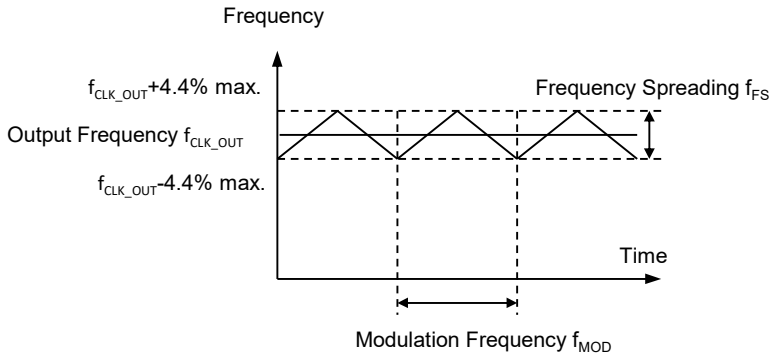


Fig.1. Frequency spread profile of output frequency

The modulation rate at the modulation frequency can be selected by the MOD pin. The MOD pin supports 3-state input, and the modulation rate is determined by the High level, Open, and Low level states. Electric potential is set inside the MOD pin by voltage dividing resistor. The internal configuration is shown as Fig.2.

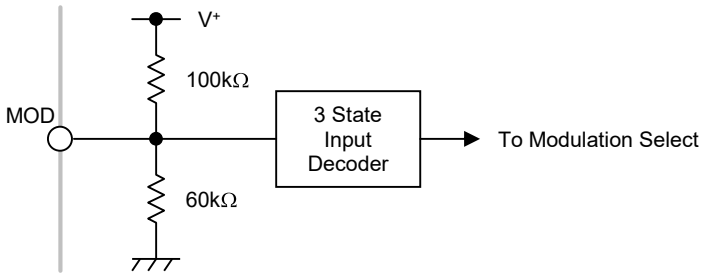


Fig.2. MOD pin internal configuration.

Functional description of each block

Table 1 shows the relationship between the MOD pin and the modulation rate, and Fig. 3 shows an example of the spectrum of the output frequency of the NJW4203.

Table 1 Relationship between version and modulation rate

MOD PIN	MODULATION RATE	MODULATION FREQUENCY CALCULATION EXAMPLE
High	Pattern A: f_{CLK}/2048	f_{CLK}=500kHz, f_{MOD}=244Hz
		f_{CLK}=2000kHz, f_{MOD}=977Hz
Open	Pattern B: f_{CLK}/512	f_{CLK}=500kHz, f_{MOD}=977Hz
		f_{CLK}=2000kHz, f_{MOD}=3.9kHz
Low	Pattern C: f_{CLK}/128	f_{CLK}=500kHz, f_{MOD}=3.9kHz
		f_{CLK}=2000kHz, f_{MOD}=15.6kHz

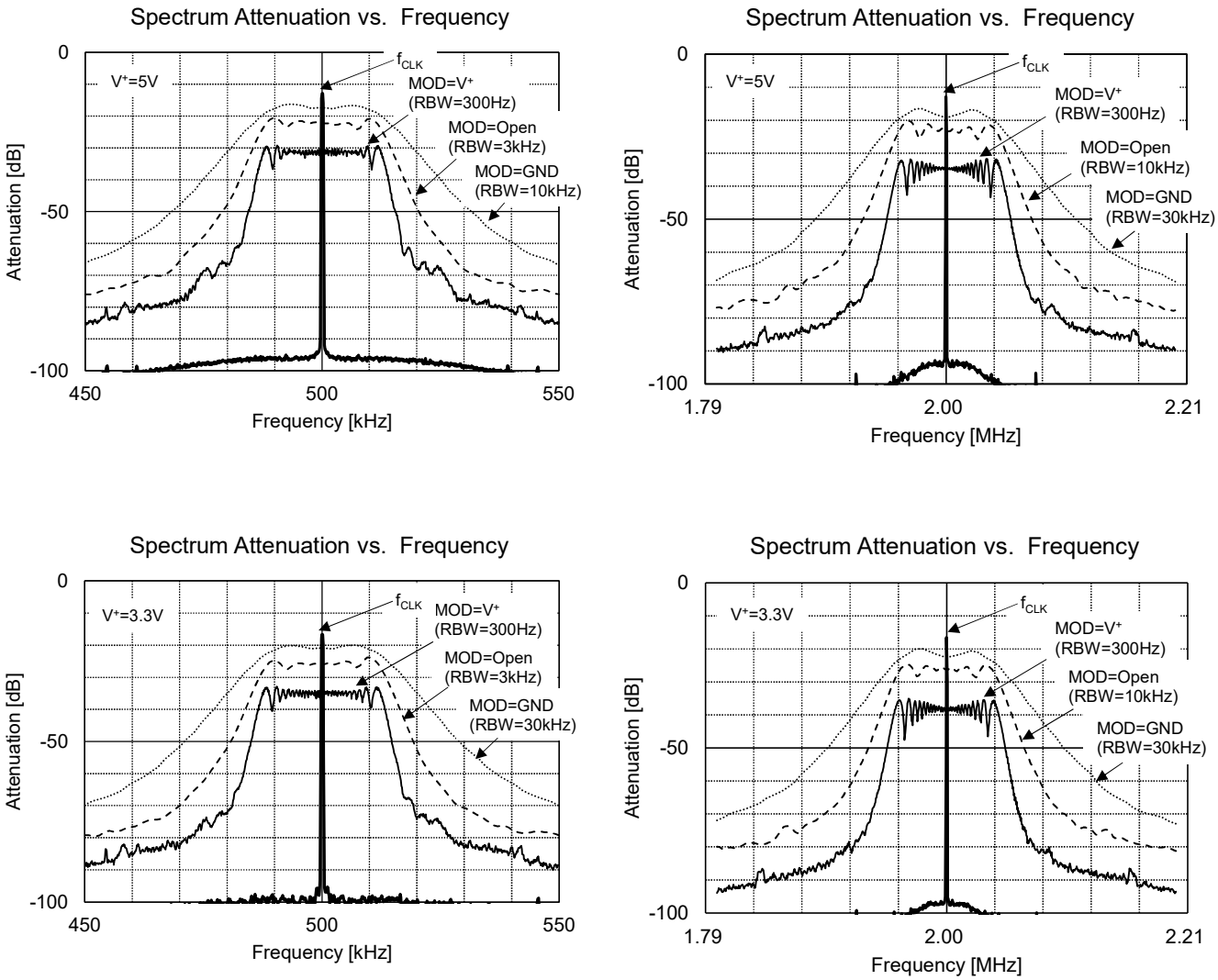


Fig.3. Example of output frequency spectrum characteristics of NJW4203

Functional description of each block

● **PLL circuit block**

The clock input to the CLK pin is converted to a spread-spectrum-modulated clock through the PLL circuit. The specifications of the clock input to the CLK pin are as follows.

Input frequency	120kHz to 2400kHz
Duty cycle	20% to 80%
Voltage amplitude	V^+−0.5Vor higher (High level)
	0.5V or less (Low level)

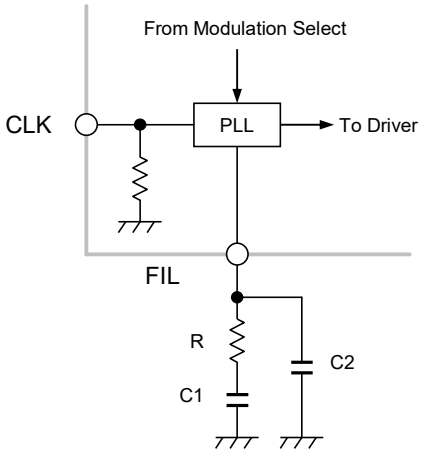


Fig.4 FIL pin configuration.

The PLL circuit filter is determined by the CR connected to the FIL pin. (Fig. 4).
Since the CR value differs depending on the input clock frequency, refer to the FIL setting example in Table 3. Since the FIL pin has high impedance, place the external CR near the IC and make the shortest wiring between the FIL pin and the GND pin.

Due to the responsiveness of the PLL circuit, it takes time for the output to stabilize after the clock signal is input.
When the NJW4203 starts up or returns from standby, the output clock is masked for a certain period of time in order to prevent unstable output transitions during startup. NJW4203 startup waveform is shown as Fig.5. The delay time from power-on to output start depends on the operating frequency. Table 3 shows the reference values for the output delay time.

Table 3. FIL setting example and maximum output delay time example.

INPUT FREQUENCY f_{CLK} (kHz)	RESISTOR R (kΩ)	CAPACITOR C1 (μF)	CAPACITOR C2 (μF)	MAXIMUM OUTPUT DELAY TIME (5) (ms)
120 to 200	22	0.22	0.022	250
200 to 250	16	0.22	0.022	150
250 to 350	10	0.22	0.022	120
350 to 700	5.6	0.22	0.022	100
700 to 1000	5.6	0.15	0.015	80
1000 to 2400	5.6	0.1	0.01	70

(5) Reference value

When using the variable range of the input frequency at 300kHz ↔ 400kHz, set it with a low frequency value.
In this case, set the R=10kΩ, C1=0.22μF and C2=0.022μF.

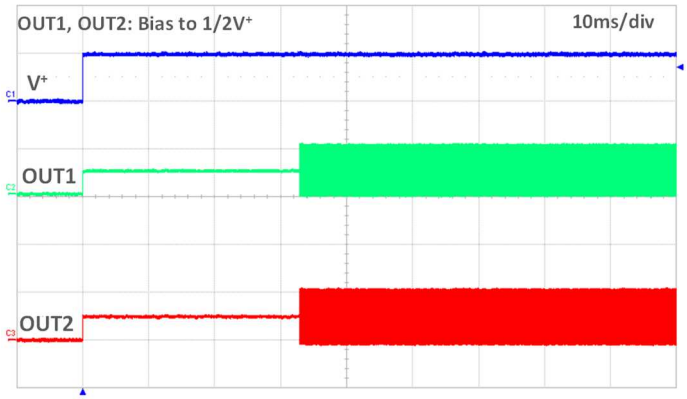


Fig.5. NJW4203 startup waveform
(V^+=5.0V, STBY=V^+, f_{CLK}=500kHz, Ta=25°C)

Functional description of each block

Table 4 shows the transition time when the input frequency is changed during the operation of NJW4203. If the input frequency change width is large, frequency overshoot may occur. To minimize overshoot, use (f_{CLK2} / f_{CLK1} -1) < 0.5 as a guideline for the input frequency change width. The larger the change width of the input frequency, the longer the transition time.

Table 4 Example of transition time when the input frequency is changed.

INPUT FREQUENCY f_{CLK} (kHz) $f_{CLK1} \leftrightarrow f_{CLK2}$	MAXIMUM TRANSITION TIME (6) (ms)
120 ↔ 180	650
200 ↔ 300	550
300 ↔ 400	450
400 ↔ 500	350
500 ↔ 600	300
2000 ↔ 2100	30
2300 ↔ 2400	30

(6) Reference value

If the input clock is lost during the operation of the NJW4203, the output is limited to prevent unstable output transition of the PLL circuit. The number of clocks output is 5 or 6 pulses, depending on the signal timing. Fig.6 shows an example of the waveform when the input clock disappears. If the clock is re-input within the specified period after the input clock is lost, the NJW4203 maintains the clock output.

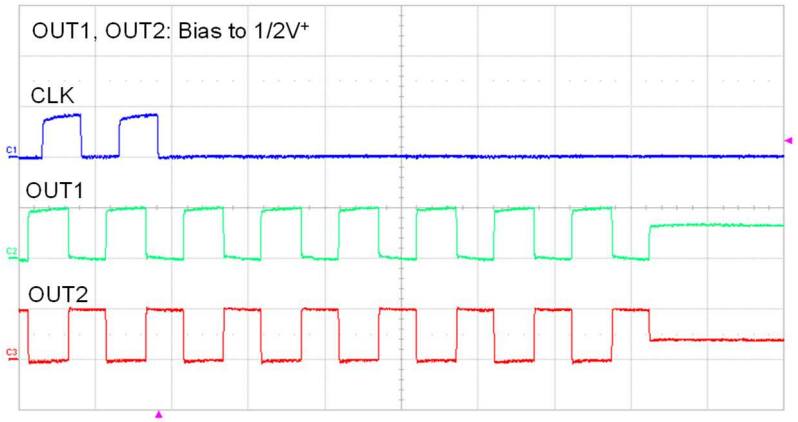


Fig.6 Waveform example when the input clock is lost

Functional description of each block

● **Output block (OUT1, OUT2)**

The output driver circuit is composed of a push-pull system and can drive the load directly. Connect to the external synchronous input pin of the switching regulator. Since the outputs of OUT1 and OUT2 are inverted, the anti-phase operation of the switching regulator can be easily configured. If one of the OUT pin is unused, open it.

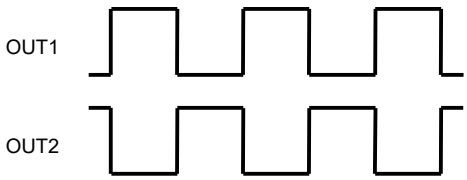


Fig.7. NJW4203 output waveform

● **Under voltage lockout (UVLO) block**

If the supply voltage is low, the UVLO circuit will stop the operation of the IC, and if the supply voltage is 2.5V typ. or higher, the UVLO circuit will be released and the IC will start operating. The detection voltage and release voltage of the UVLO circuit have a hysteresis width of 100 mV typ. in order to prevent UVLO release and detection chattering.

● **Standby function block**

By setting the STBY pin to 0.5V max. or less, the NJW4203 function is stopped and put into standby mode. The inside of the pin is pulled down by a resistor, and even when the STBY pin is open, it shifts to standby mode. When not using the standby function, connect the STBY pin to V^+.

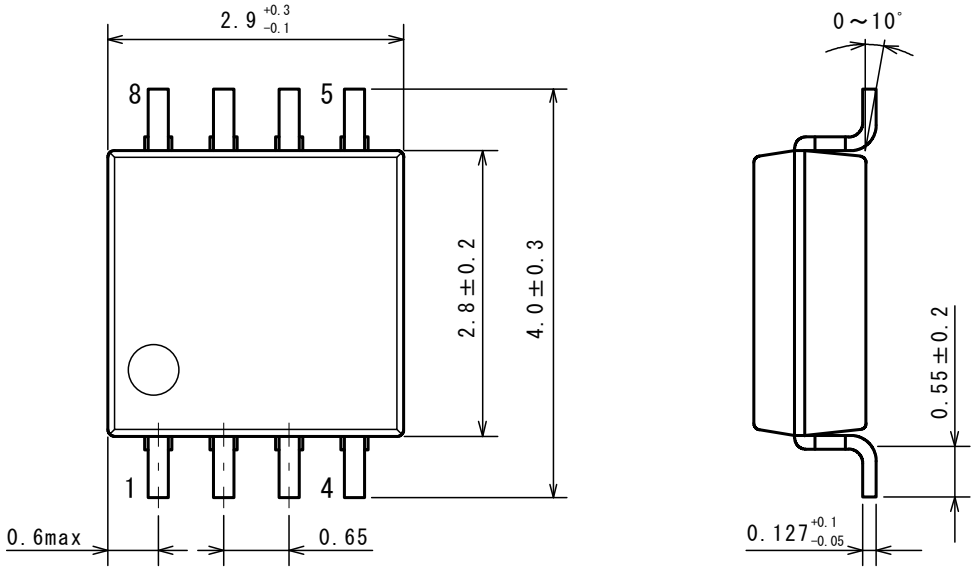
● **Power supply, GND (V^+, GND) block**

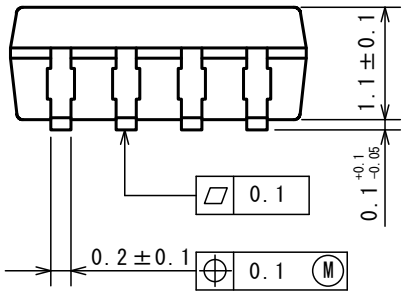
Along with the high-speed oscillation operation, a current corresponding to the frequency flows through the IC. If the impedance of the power supply line is high, the power supply will become unstable and the IC performance will not be fully exhibited. Insert a bypass capacitor of about 1μF near the V^+ pin and GND pin to lower the high frequency impedance.

MSOP8 MEET JEDEC MO-187-DA

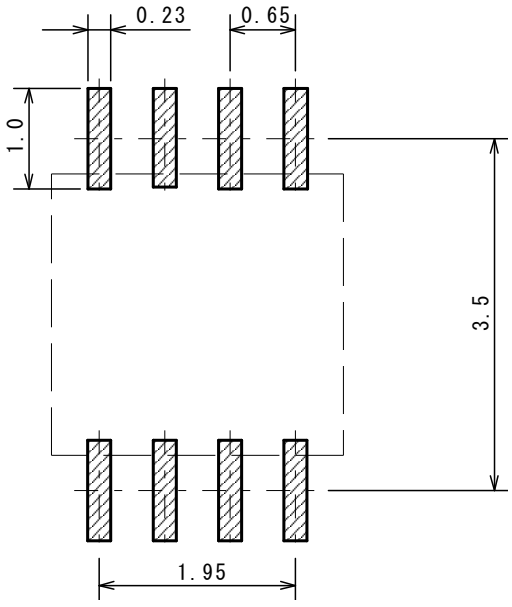
■ PACKAGE DIMENSIONS

Unit: mm





■ EXAMPLE OF SOLDER PADS DIMENSIONS

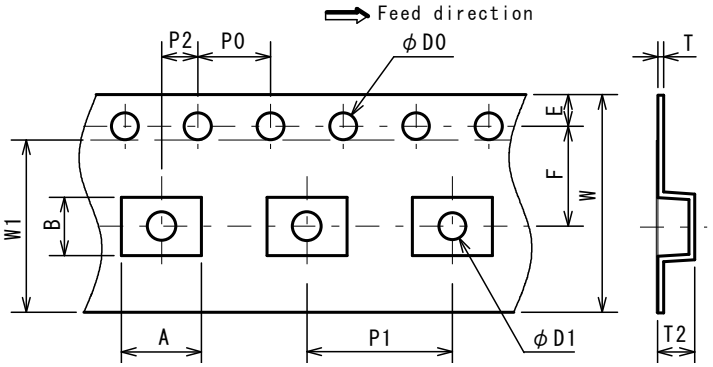


MSOP8 MEET JEDEC MO-187-DA

■ PACKING SPEC

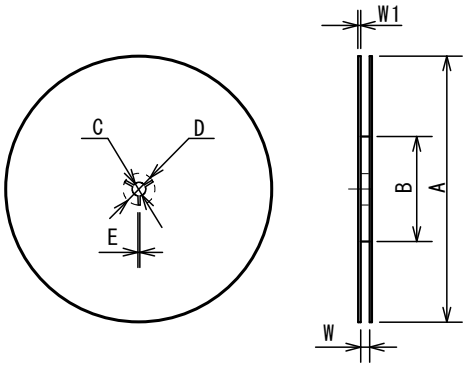
Unit: mm

TAPING DIMENSIONS



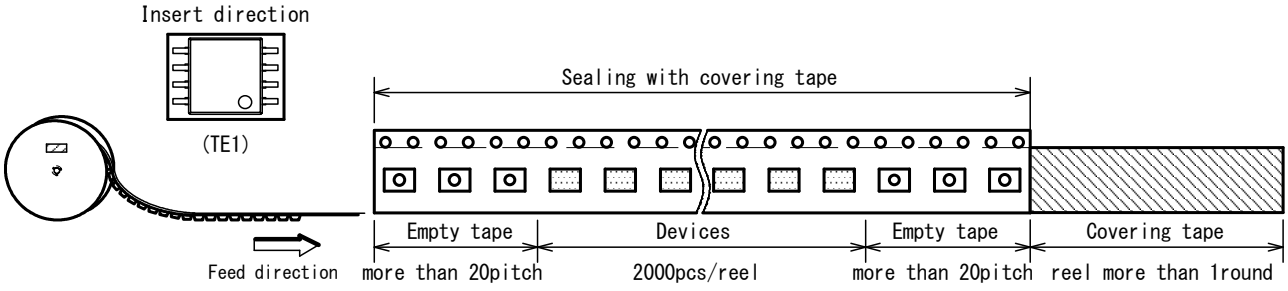
SYMBOL	DIMENSION	REMARKS
A	4.4	BOTTOM DIMENSION
B	3.2	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	$1.5^{+0.1}_{0}$	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
T	0.30±0.05	
T2	2.0 (MAX.)	
W	12.0±0.3	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

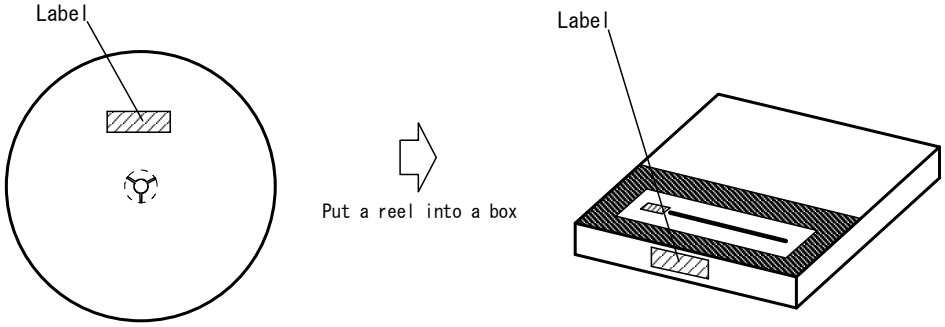


SYMBOL	DIMENSION
A	φ254±2
B	φ100±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	13.5±0.5
W1	2.0±0.2

TAPING STATE

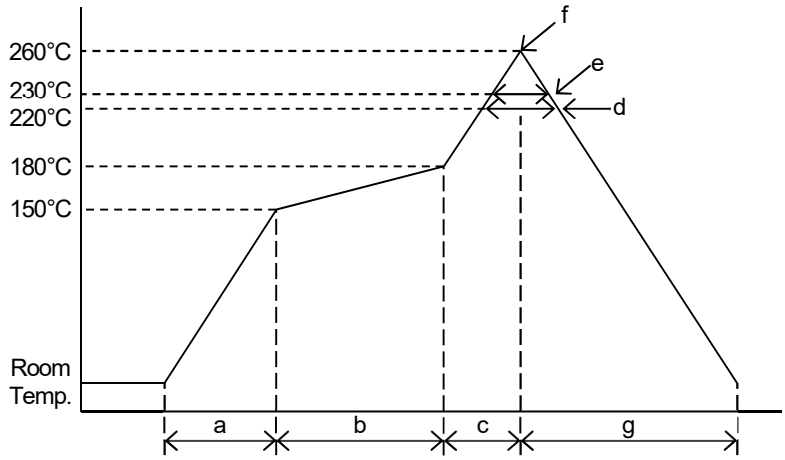


PACKING STATE



■ RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING PROFILE



a	Temperature ramping rate	1 to 4°C/s
b	Pre-heating temperature Pre-heating time	150 to 180°C 60 to 120s
c	Temperature ramp rate	1 to 4°C/s
d	220°C or higher time	shorter than 60s
e	230°C or higher time	shorter than 40s
f	Peak temperature	lower than 260°C
g	Temperature ramping rate	1 to 6°C/s

The temperature indicates at the surface of mold package.

■ REVISION HISTORY

DATE	REVISION	CHANGES
April 13, 2021	Ver.1.0	Initial release

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   - Equipment Used in the Deep Sea
   - Power Generator Control Equipment (Nuclear, steam, hydraulic, etc.)
   - Life Maintenance Medical Equipment
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   - Vehicle Control Equipment (Automobile, airplane, railroad, ship, etc.)
   - Various Safety Devices

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