NAU88L11

Ultra-Low Power Audio CODEC With ClassAB Power Amplifier

GENERAL DESCRIPTION

The NAU88L11 is a cost effective ultra-low power high performance MONO audio CODEC. It's suitable for wide range of applications including industrial or portable audio applications. This CODEC includes I2S/PCM interface, Analog/Digital microphone interface, integrated DSP functions, high quality DAC and ADC, and a Class-AB power amplifier. The advanced on-chip digital signal processing features include a dynamic range compressor (DRC) and programmable biquad filter. The NAU88L11 digital and analog voltage can be operated as low as 1.62V, with Speaker Driver voltage operated from 2.5 to 3.6V.

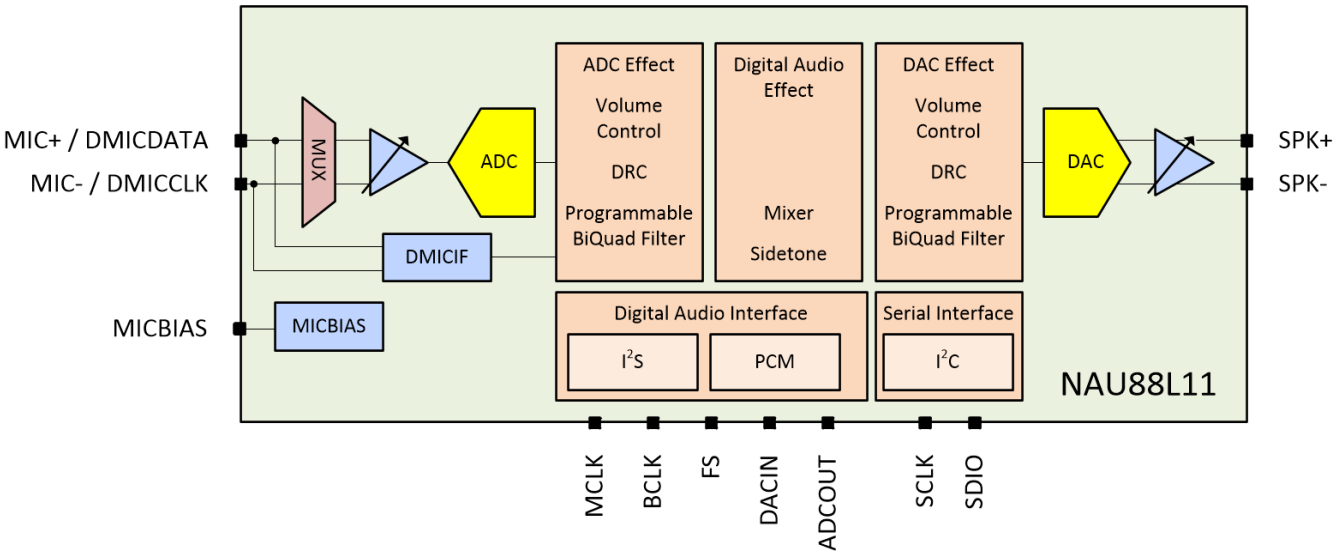
FEATURES

- DAC SNR(A-weighted): 105dB@1.8V, R_L= 8Ω, DAC gain=11dB, THD= -85dB
- ADC SNR(A-weighted): 103dB@1.8V, MIC gain=0dB,Fs=48kHz, THD =-93dB
- Low Noise Microphone PGA SNR: 100dB@+18dB gain, 256x OSR
- Digital I2S/PCM I/O port
- Mono differential analog microphone input, or mono digital microphone input
- Low noise Microphone bias: <10 uV_{RMS} noise between 20~20kHz;
- Class AB Power Amplifier: 350mW @ 8Ω, 1% THD+N
- Lineout Mode with Pop&Click Noise Suppression during startup
- Sampling rate from 8k to 96kHz
- Integrated DSP with specific functions:
  - Programmable Biquad filter
  - Dynamic Range Compressor (DRC)
- Package: 20 Pin QFN

Applications

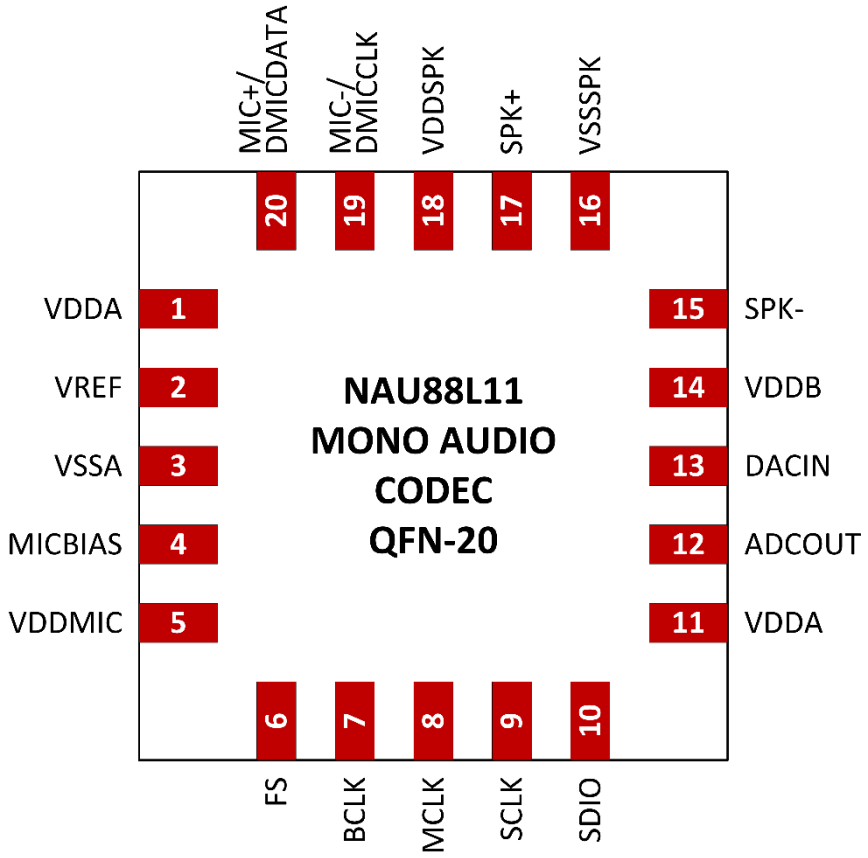
- Intercom
- Doorbell
- Portable Recording Device
- Wireless handsets /headsets
- Surveillance Camera
- Dash CAM
- Sports CAM
- Digital Still Cameras
- Speakerphone

Block Diagram



Pin Diagram :

QFN 20-pin (4mm x 4mm)



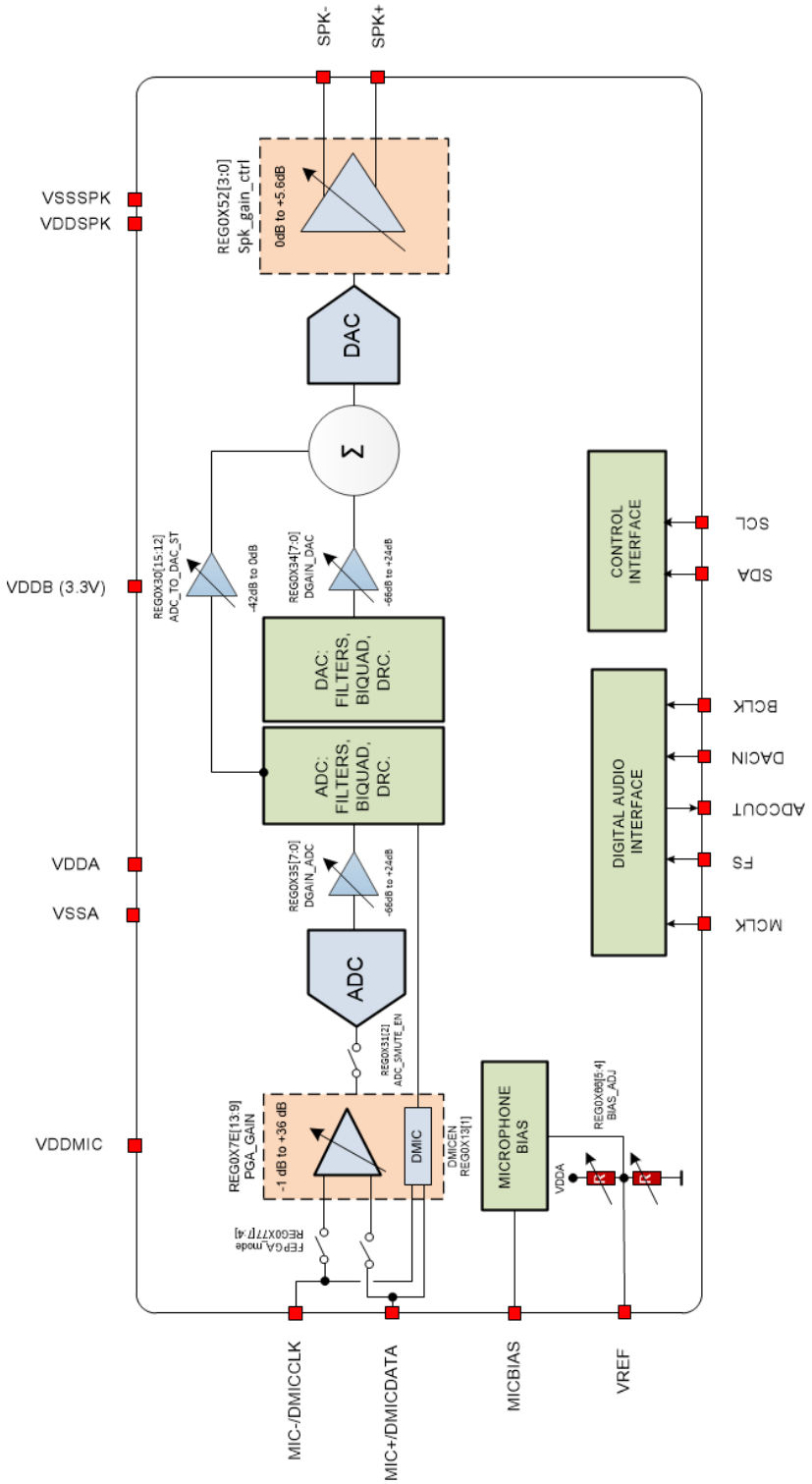
Pin Description

Pin #	Name	Type	Functionality
1	VDDA	Supply	1.8V Analog Supply
2	VREF	Analog I/O	Internal DAC & ADC voltage reference decoupling I/O
3	VSSA	Ground	Analog Ground
4	MICBIAS	Analog Output	Microphone Bias Output
5	VDDMIC	Supply	Microphone supply
6	FS	Digital I/O	Frame Sync input / output for I2S / PCM data
7	BCLK	Digital I/O	Serial data bit clock input / output for I2S / PCM data
8	MCLK	Digital Input	CODEC external Master clock source input
9	SCLK	Digital Input	Serial Data Clock for I2C
10	SDIO	Digital I/O	Serial Data for I2C
11	VDDA	Supply	1.8V Analog Supply
12	ADCOUT	Digital Output	Serial Audio data Output for I2S / PCM data
13	DACIN	Digital Input	Serial Audio data input for I2S / PCM data
14	VDDB	Supply	3.3V Digital I/O supply
15	SPK -	Analog Output	Speaker - channel output
16	VSSSPK	Ground	Speaker Driver Ground
17	SPK+	Analog Output	Speaker + channel output
18	VDDSPK	Supply	Speaker Driver Supply
19	MIC - / DMICCLK	Analog Input	Microphone - channel input / Digital Mic Clock pin
20	MIC + / DMICDATA	Analog Input	Microphone + channel input / Digittal Mic Data Pin

Notes:

1. Unused MIC input pins should be left as no-connection.
2. Digial Microphone should be power by MICBIAS, with setting to V_{DDA}

Functional Block Diagram



Electrical Characteristics

Conditions: V_{DDA}=1.8V, V_{DDB} = 3.3V; V_{DDSPK}= 3.6V, V_{DDMIC}= 3.6V.
R_L= 8 Ω, f = 1KHz, MCLK=12.88MHz, unless otherwise specified. Limits apply for T_A = 25°C

Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
I_{SB}	Standby Current	V_{DDA}	4	16	µA
		V_{DDB}	1	5	
		V_{DDMIC}	1	5	
I_Q	Quiescent Current	f_S = 48kHz, DAC On, SPK_DRV On, P_{OUT} = 0mW. R_L = 8Ω	20		mA
Speaker Driver (V_{DDSPK}= 3.6V, R_L = 8Ω, BTL)					
	Full-Scale output signal	V_{DDSPK}= 3.6V, R_L=8Ω	2.0		V_{RMS}
P_O	Output Power	DAC Gain = 0dB, THD+N = 1%	350		mW
THD+N	Total Harmonic Distortion + Noise	Po =350mW	-85		dB
SNR	Signal to Noise Ratio	VOUT = 2V_{RMS}, SPK_DRV Gain=4.4dB, DAC_Gain = 11dB, A-Weighted	105		dB
PSRR	Power Supply Rejection Ratio	Ripple on V_{DDA} = 200mVpp at 217Hz	80		dB
	Frequency Response	F = 20Hz ~ 20kHz	+0.1/-0.2		dB
ADC					
FS_{ADC}	ADC Full Scale Input Level	V_{DDA}= 1.8V	1		V_{RMS}
THD+N	Total Harmonic Distortion + Noise	MIC Input=0.8V_{RMS}, MIC GAIN=0dB, f=1KHz, fs = 48kHz, Differential Input	-90		dB
		MIC Input=0.8V_{RMS}, MIC GAIN=30dB, f=1KHz, fs=16kHz, Differential Input	-90		dB
SNR	Signal to Noise Ratio	A-Weighted, MIC Gain = 0dB, fs = 48kHz, Differential Input	102		dB
		A-Weighted, MIC Gain = 6 dB, fs = 48kHz, Differential Input	100		dB
PSRR	Power Supply Rejection Ratio	Ripple on V_{DDA} = 200mVpp at 217Hz MIC GAIN = 0dB Differential Input	70		dB
CMRR	Common Mode Rejection Ratio	Differential Input 100 mV_{RMS}, PGA gain = 20dB, frequency sweep 20Hz ~ 20KHz	65		dB
	Minimum Input Impedance		10		kOhm
	Frequency Response	f = 20Hz ~ 20kHz	+0.1/-0.2		dB
	Power Consumption	No Signal, ADC on f_s = 44.1kHz	7.9		mW
MICBIAS					
I_{OUT}	Output Current	Low Noise Mode		4	mA
e_{os}	Output Noise	Low Noise Mode, f = 20Hz ~ 20kHz MICBIAS=2.7V		10	uV_{RMS}

Digital I/O

Parameter	Symbol	Comments/Conditions		Min	Max	Units
Input LOW level	V_{IL}	V_{DDB} = 1.8V			0.33* V_{DDB}	V
		V_{DDB} = 3.3V			0.37* V_{DDB}	
Input HIGH level	V_{IH}	V_{DDB} = 1.8V		0.57* V_{DDB}		V
		V_{DDB} = 3.3V		0.63* V_{DDB}		
Output HIGH level	V_{OH}	I_{Load}= 1mA	V_{DDB} =1.8V	0.9* V_{DDB}		V
			V_{DDB} = 3.3V	0.95* V_{DDB}		
Output LOW level	V_{OL}	I_{Load}= 1mA	V_{DDB} = 1.8V		0.1* V_{DDB}	V
			V_{DDB} =3.3V		0.05* V_{DDB}	

Recommended Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Digital I/O Supply Range	V_{DDB}	1.62	3.3	3.6	V
1.8V Supply Range**	V_{DDA}	1.62	1.8	1.98	V
Speaker Drvier Supply Range	V_{DDSPK}	2.5	3.3	3.6	V
Microphone Bias Supply Voltage	V_{DDMIC}	3.0	3.3	3.6	V
Temperature Range	T_A	-40		+85	°C

****** Note: DMIC Supply power should connected to MICBIAS, and set same as V_{DDA}.

Absolute Maximum Ratings

Parameter	Min	Max	Units
Digital I/O Supply Range	-0.3	4.0	V
1.8V Supply Range	-0.3	2.2	V
Speaker Driver Supply Range	-0.3	4.0	V
Microphone Bias Supply Voltage	-0.3	4.0	V
Voltage Input Digital Range	V_{SSD} - 0.3	V_{DDA} + 0.3	V
Voltage Input Analog Range	V_{SSA} - 0.3	V_{DDA} + 0.3	V
Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

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1. General Description

NAU88L11 is an ultra-low power, highly integrated CODEC, which features mono audio DAC, and mono audio ADC, that supports Analog and Digital Microphone Input. NAU88L11 includes DSP functions including DRCs (Dynamic Range Compression) and programmable biquad filters. The NAU88L11 supports a full range of audio formats including Left-justified, I^2S, and multiple PCM formats. The NAU88L11 device is controlled through 2-wire digital control interface. The NAU88L11 digital and analog voltage can be operated as low as 1.62V, with Speaker Driver voltage operated from 2.5 to 3.6V. Mic bias votlage supply is upgraded to support voltages up to 3.6V.

1.1 Analog and Digital Inputs

The NAU88L11 provides an analog input to acquire and process audio signals from a microphone with high fidelity and flexibility. The mono input path that can be used to capture signals from single-ended or a differential source. The channel has a fully differential programmable gain amplifier (PGA). The outputs of the PGA connect to the ADC.

The NAU88L11 also has an input for a digital microphone. The NAU88L11 provides a DMICCLK, (the clock signal) for the digital microphones. Note that the analog and the digital microphone inputs cannot be used simultaneously.

1.2 Analog Output

NAU88L11 has a Class AB speaker driver that is fed by the high quality DAC. The speaker driver has a gain control from 0dB to +5.6dB and Mute. The Speaker driver output can also be used as lineout.The speaker driver is capable of delivering 350mW into 8Ω with 1% THD+N.

1.3 ADC, DAC and Digital Signal Processing

The NAU88L11 has a high quality ADC and DAC. These are high performance 24-bit sigma-delta converters, which are suitable for a very wide range of applications.
The ADC and DAC have functions that individually support digital mixing and routing. The ADC and DAC blocks also support advanced digital signal processing subsystems that enable a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is done with 24-bit precision to minimize processing artifacts and maximize the audio dynamic range supported by the NAU88L11.

The ADC and DAC digital signal process can support two-point dynamic range compressors (DRCs), programmable biquad filters configurable for low pass filters, high pass filters, Notch filter, Bell, low shelf, and high shelf filters with various gain, Q, and frequency controls. Two-point DRCs can be programmed to limit the maximum output level and/or boost a low output level. The biquad filters can be configured as high pass filters intended for DC-blocking or low frequency noise reduction, such as reducing unwanted ambient noise or “wind noise” on a microphone input.

1.4 Digital Interfaces

Command and control of the device is accomplished by using the I^2C interface.

The digital audio I/O data streams transfer separately from command and control using either I^2S or PCM audio data protocols These simple but highly flexible interface protocols are compatible with most commonly used serial data protocols, host drivers, and industry standard I^2S and PCM devices.

2. Power Supply

This NAU88L11 has been designed to operate reliably using a wide range of power supply conditions and power-on/power-off sequences. Because of this, there are no special requirements for the sequence or rate at which the various power supply pins change. Any supply can rise or fall at any time without harming the device. However, pops and clicks may result from some coditions. For Lineout mode, optimum handling of hardware and software power-on and power-off sequences are described in more detail in the Lineout configuation section.

2.1 Power on and off reset

The NAU88L11 includes a power on reset circuit on chip. The circuit resets the internal logic control at V_{DDA} supply power up and this reset function is automatically generated internally when power supplies are too low for reliable operation. The reset threshold is approximately 0.55Vdc and 1.0Vdc for V_{DDA}. It should be noted that these values are much lower than the required voltage for normal operation of the chip.

The reset is held on while the power levels for both V_{DDA} are below their respective thresholds. Once the power levels rise above their thresholds, the reset is released. Once the reset is released, the registers are ready to be written to. It is also important to note that all the registers should be kept in their reset state for at least 6µs.

An additional internal RC filter based circuit is added which helps the circuit respond for fast ramp rates (~10µs) and generate the desired reset period width (~10µs at typical corner). This filter is also used to eliminate supply glitches which can generate a false reset condition, typically 50ns.

For reliable operation, it is recommended to write **SOFTWARE_RST**, REG 0x00 upon power up. This will reset all registers to the known default state. Note that when V_{DDA} is below the power on reset threshold, then the digital IO pins will go into a tri-state condition.

Note that when V_{DDA} are below the power on reset threshold, then the digital IO pins will go into a tri-state condition.

3. Input Path Detailed Descriptions

NAU88L11 is design with a low noise, high common mode rejection ratio analog microphone differential input. The microphone input MIC+/- are followed by -1dB to 36dB PGA gain stage that has a fixed 12kOhm input impedance.

The input is maintained at a DC bias of approximately ½ of the V_{DDA} supply voltage. Connections to the input should be AC-coupled by means of external DC blocking capacitors suitable for the device application.

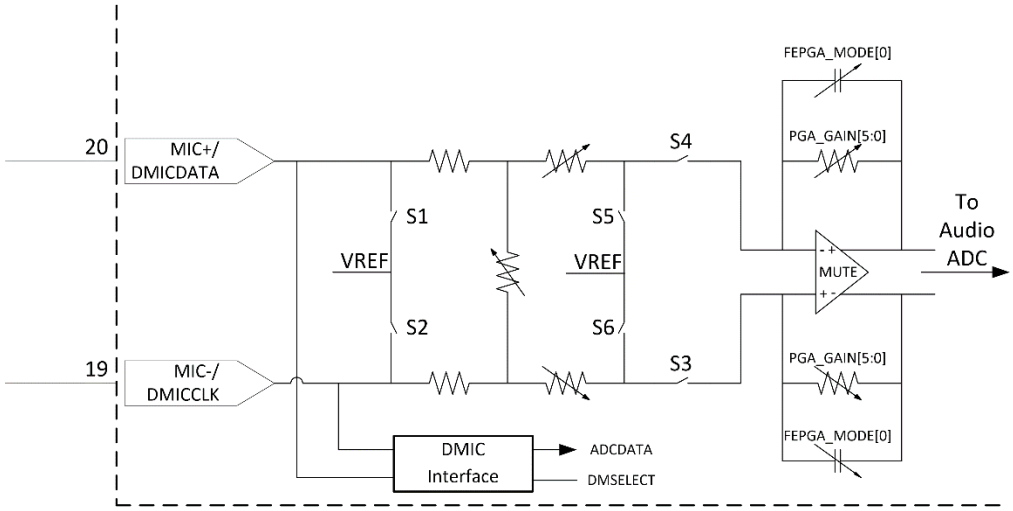
The differential microphone input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary such as in portable digital devices.

A differential input is also very useful to reduce ground noise in systems in which there are ground voltage differences between different chips and components. When properly implemented, the differential input architecture offers an improved power-supply rejection ratio (PSRR) and higher ground noise immunity.

3.1 Analog Microphone Inputs

The analog microphone input is routed to a Front End Programmable Gain Amplifier(FEPGA). The input stage can be configured in different modes by using **FEPGA_MODE**. The FEPGA gain can be varied from -1dB to 36dB in 1dB steps. The gain stage has a fixed 12kΩ input impedance and can be individually enabled or disabled using the powerup control signal, **PUPL**, REG 0x7F[15].

As shown below:
The input path control is done through S1~S6. Related Register and configuration is provided in blow input block diagram.



S1	BOOST.DISHCHRG FEPGA.ACDC_CTRL[0]	S5	FEPGA_MODE[3]	S4	FEPGA_MODE[1]
S2	BOOST.DISHCHRG FEPGA.ACDC_CTRL[1]	S6	FEPGA_MODE[3]	S3	FEPGA_MODE[1]

Figure 1: Microphone Input Block Diagram with Registers

3.2 Digital Microphone Input

The MIC- and MIC+ pins can be used for the digital microphone input. MIC- is the clock for the digital microphone and the MIC+ is the data in. DMIC supply voltage must be provided by MICBIAS, and set the same as V_{DDA}.

3.3 VREF

The NAU88L11 includes a mid-supply reference circuit that produces a voltage close to $V_{DDA}/2$. This "VREF" pin should be decoupled to VSS through an external bypass capacitor. Because V_{REF} is used as a reference voltage inside the NAU88L11, a large capacitance is required to achieve good power supply rejection at low frequency. Typically, a value of 4.7µF should be used. The V_{REF} voltage can be enabled by setting **VMIDEN**, REG 0x66[6] and the output impedance can be set using **VMIDSEL.**

VMIDSEL	VREF Resistor Selection	VREF Impedance
00	Open, no resistor selected	Open, no impedance installed
01	50kOhm	25kOhm
10	250kOhm	125kOhm
11	5kOhm	2.5kOhm

Table 1: VREF Impedance Selection

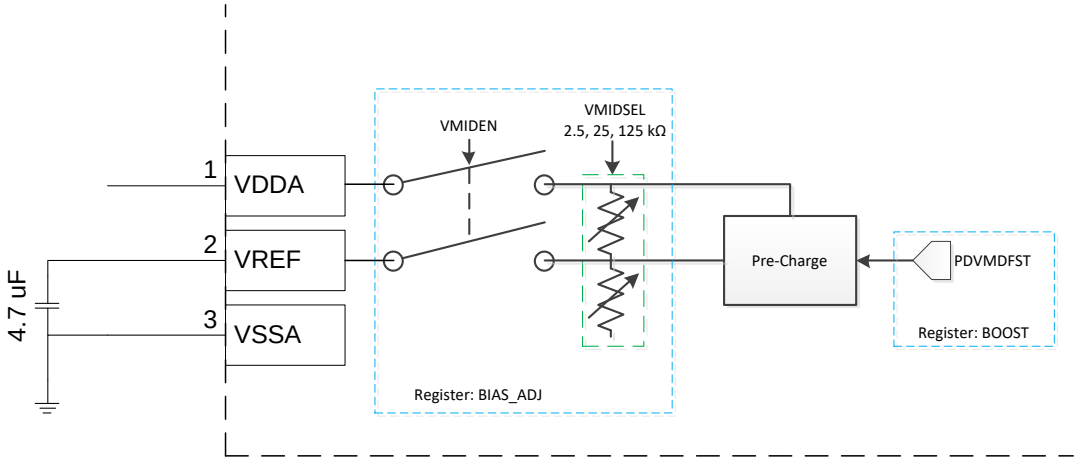


Figure 2: VREF Circuitry

3.4 MIC Bias

The NAU88L11 provides a MICBIAS pin to power an electret type microphone. The MICBIAS pin is the low impedance output of the MIC Bias LDO. An external 2kΩ resistor has to be used if the analog microphone is biased by this pin. This pin can be enabled by using **POWERUP**, REG 0x74[8] and the level can be set by using **MICBIASLVL1**,REG 0x74[2:0].

MICBIAS has three modes of operation selected by **MB_LPMODE**, REG 0x74[4:3]. It can be operated as low noise mode, low power mode or ultra low power mode. See electrical characteristics for expected operating values. Ultra Low Power Mode can be used for Voice wakeup applications. Low power mode is ideally suited for digital MIC applications.

3.5 MIC detect

The MIC detect is used to detect whether a microphone is connected to the MICBIAS output. The detection is made internally to the MICBIAS block by determining current draw from the MICBIAS pin. The status of the Mic detect can be read from **IRQ_STATUS.MICDET**. Mic detection is triggered when MICBIAS voltage drops 25mV below MICBIAS1 value set by **MICBIASLVL1**.

3.6 Key Detect

Key detect is used to detect when a key is pressed on the microphone (e.g. to answer/end a call). In this mode, the MICBIAS output is shunted through an external 2kΩ resistor to GND and a key detect inturupt status is set in **IRQ_STATUS.KEYDET ,**REG 0x10[11]. Key detection is triggered at 85mV reference to GND.

4. ADC Digital Block

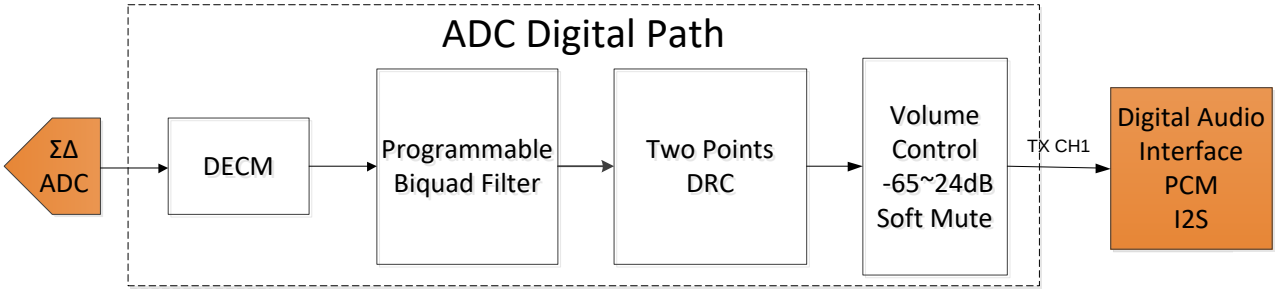


Figure 2 ADC Digital Path

The ADC digital block takes the output of the 24-bit Analog-to-Digital converter and performs signal processing aimed at producing a high quality audio sample stream to the audio path digital interface. The above figure shows the functional blocks associated with the ADC digital path.

This block can be enabled by using **ENA_CTRL.ADCEN**, REG 0x01[12]. Oversampling is used to improve noise and distortion performance without affecting the final audio sample rate. The **ADC_RATE**, REG 0x2B[1:0]can be used to set the ADC OSR and **SMPL_RATE**, REG 0x2B[7:5] should be set to the value closest to the actual sample rate. The polarity of the ADC output signal can be controlled independently. This data management feature can help minimize subsequent audio processing that may be otherwise required, as the data is passed through stages in the system.

The full-scale input level is proportional to V_{DDA}. For example, with a 1.8V supply voltage, the full-scale level is $1.0V_{RMS}$.

4.1 ADC Dynamic Range Compressors (DRC)

The ADC in the digital signal path is design with a a two-point dynamic range compressor (DRC) for advanced signal processing. The DRC can be programmed to limit the maximum output level and/or boost a low output level signal. The DRC function consists of level estimation and static curve control.

4.1.1 Level Estimation

The NAU88L11 uses Peak level estimation that depends on the attack and decay time settings, which can be programmable by register settings as in below table.

Bits	DRC_PK_COEF1_ADC	DRC_PK_COEF2_ADC
0000	Ts	63*Ts
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts

Table 2: ADC Level Estimation - Attack and Decay Time Register Settings

Please note that Ts is the sampling time given by 1/(Sampling Frequency)

4.1.2 Static Curve

The DRC static curve supports up to five programmable sections as below figure.

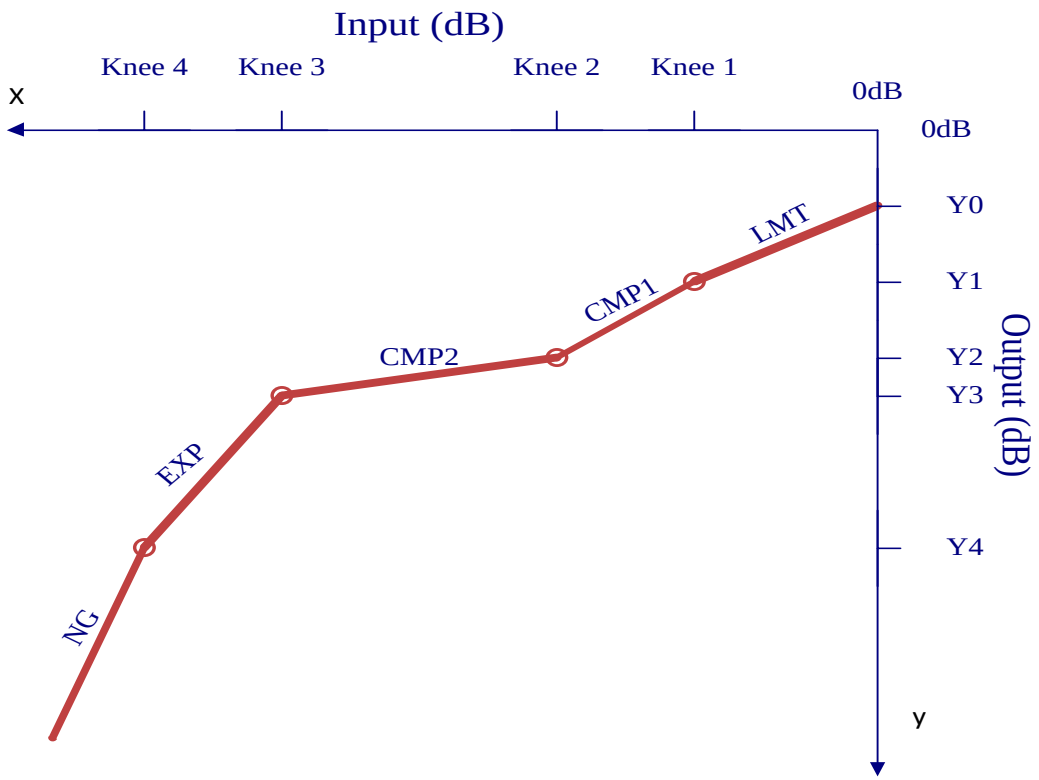


Figure 3 DRC Static Characteristic

Each section on the characteristic (labeled NG, EXP, CMP2, CMP1, and LMT) can be controlled by setting the slope and knee point values, in their respective registers.

The table below provides the corresponding register locations.

Static Curve Section	Slope	Knee Point
LMT	0, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1	
CMP1	0, 1/2, 1/4, 1/8, 1/16, 1	0 to -31dB with -1dB step
CMP2	0, 1/2, 1/4, 1/8, 1/16, 1	0 to -63dB with -1dB step
EXP	1, 2, 4	-18 to -81dB with -1dB step
NG	1, 2, 4, 8 s	-35 to -98dB with -1dB step

Table 3: ADC DRC Static Curve control registers

The output Y values can be determined based on the slopes and knee points selected. Y1 is always equal to Knee 1, as an initial and default condition.

Y1 = Knee 1
Y0 = Y1 - (Knee 1) * (LMT Slope)
Y2 = (Knee 2 - Knee 1) * (CMP1 Slope) + Y1
Y3 = (Knee 3 - Knee 2) * (CMP2 Slope) + Y2
Y4 = (Knee 4 - Knee 3) * (EXP Slope) + Y3

The attack time and decay time is programmable as shown in the Table 4. And the smooth knee filter can be also enabled by register setting.

Application Notes:

- The Y axis distance adjusting along curve cannot exceed 36dB.
- Smooth Knee filter function can be enabled by using **DRC_SMTH_ENA_ADC, REG 0x36[7].**
- The attack time can be set using **DRC_ATK_ADC,REG 0x39[7:4].**
- The decay time can be set using **DRC_DCY_ADC, REG 0x39[3:0]**

Bits	DRC_ATK_ADC	DRC_DCY_ADC
0000	Ts	63*Ts
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4905*Ts
0111	255*Ts	8191*Ts
1000	511*Ts	16383*Ts
1001	1023*Ts	32757*Ts
1010	2047*Ts	65535*Ts
1011	4095*Ts	
1100	8191*Ts	

Table 4: ADC Attack and Decay Time Register Settings

4.2 ADC Digital Volume Control

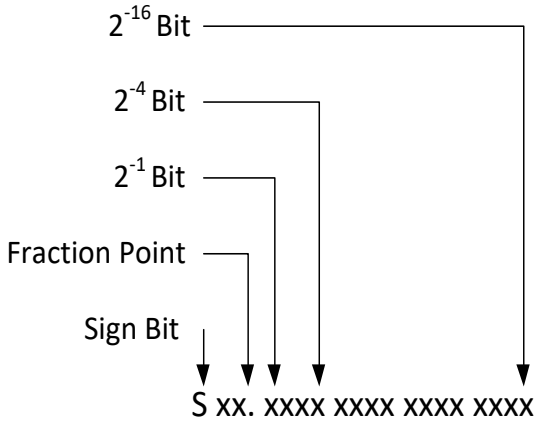
The digital volume control feature allows adjustment of the audio volume coming from ADC using a two-stage volume control. This allows the gain to be adjusted from -66dB to +24dB in 0.5dB steps. Also included is a mute value that will reduce the output signal of the ADCs to zero To adjust the channel volume controls, use register: **DGAIN_ADC, REG 0x35[7:0].**

4.3 ADC Programmable Biquad Filter

The NAU88L11 has 2 dedicated digital biquad filters. One for the ADC path, and another for the DAC path. The biquad filter is a second-order recursive linear filter with two poles and two zeros. Its transfer function is the Z-domain consists of two quadratic functions:

$$H(z) = \frac{B_0 + B_1 Z^{-1} + B_2 Z^{-2}}{1 + A_1 Z^{-1} + A_2 Z^{-2}}$$

The coefficients A_1, A_2, B_0, B_1, B_2 are represented in the 3.16 format described below



Each Biquad Coefficient has 19 bits in total, as formatted below

- S is the sign bit (1 bit),
- xx are integers (2bits)
- 16 fractional bits (16 bits)

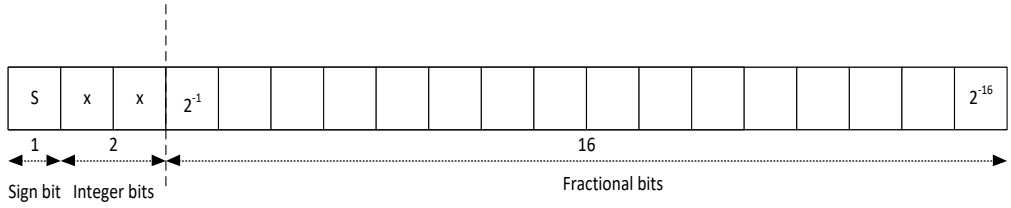


Figure 5: Number format description for biquad filters coefficients.

Application Notes:

- Biquad filter coefficients for the ADC with 3.16 format for A1, A2, B0, B1, and B3 are located in below registers.
  - **BIQ0_COF2.BIQ_A1_H** and **BIQ0_COF1.BIQ_A1_L**
  - **BIQ0_COF4.BIQ_A2_H** and **BIQ0_COF3.BIQ_A2_L**
  - **BIQ0_COF6.BIQ_B0_H** and **BIQ0_COF5.BIQ_B0_L**
  - **BIQ0_COF8.BIQ_B1_H** and **BIQ0_COF7.BIQ_B1_L**
  - **BIQ0_COF10.BIQ_B2_H** and **BIQ0_COF9.BIQ_B2_L**

- To program the biquad filter in the ADC path, write **BIQ0_COF1** to **BIQ0_COF10** for coefficients.

- To turn on the biquad filter in the ADC path, write '1' to **BIQ0_COF10.BIQ0_EN**.

4.4 Additional ADC Application Notes

- **CLK_ADC_PL**, REG 0x03[10] sets the ADC clock polarity
- **CLK_ADC_SRC**, REG 0x03[7:6] can reduce the clock speed
- **ADC_TX_SEL**, REG 0x1B[3:2] allows ADC data be placed in selected time slots to output on the I^2S interface
- It is recommended to match **ADC_RATE**, REG 0x2B[1:0] with **CLK_ADC_SRC** according to the table below

ADC_RATE	CLK_ADC_SRC
00(OSR=32)	11(CODEC 1/8)
01(OSR=64)	10(CODEC1/4)
10(OSR=128)	01(CODEC 1/2)
11(OSR=256)	00(CODEC CLK)

Table 5: ADC_RATE and CLK_ADC_SRC Pairs

5. DAC Digital Block

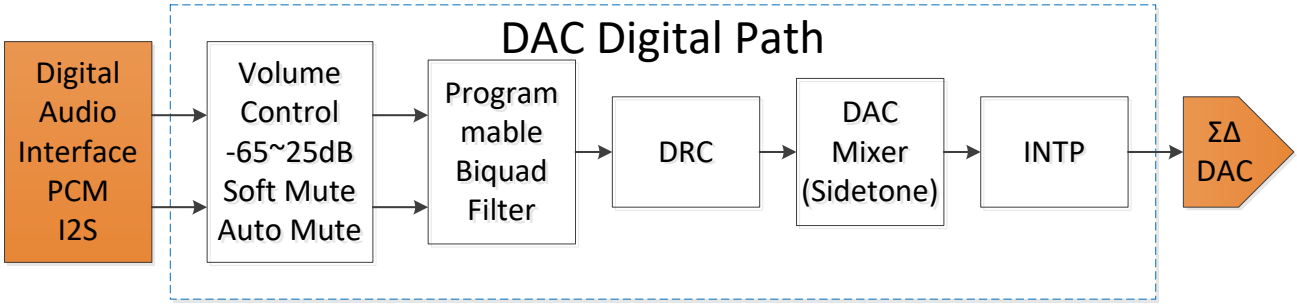


Figure 4 DAC Digital Path

The DAC digital block uses 24-bit signal processing to generate analog audio with a 16-bit digital sample stream input. This block consists of a sigma-delta modulator, programmable biquad filter, and a DRC. The full-scale output level is proportional to V_{DDA}. For example, with a 1.8V supply voltage, the full-scale level is 1.0 V_{RMS}. The oversampling feature of the DAC can be changed from 32x to 256x for improved audio performance at higher power consumption. The DAC output signal polarity can be changed using register setting. This can help minimize any audio processing that may be required as the data is passed from other stages of the system. The DAC channel is enabled by **DACEN**, REG 0x01[13]

5.1 DAC Digital Volume Control, Mute and Channel selection

The DAC has a digital volume controls that allow the user to adjust the gain from –66dB to +24dB in 0.5dB steps**. DGAIN_DAC**, REG 0x34[7:0]. Also included is a mute setting that will reduce the path gain to a minimum, control is through register **DGAIN_DAC**. When using full scale input or **DGAIN_DAC** above 0dB, it is recommended for best performance to set the DAC control bit, **DAC_CTRL1.CICCLP_OFF** as 0, and set **DAC_CTRL1.CIC_GAIN_ADJ** for optimal output amplitude.

5.2 DAC Soft Mute

The soft mute function works for both the DAC and the ADC and gradually attenuates the volume of the signal to zero. The soft mute ramps the DAC digital volume down to zero when enabled by register **SMUTE_EN**, REG0X31[9]. When disabled, the volume increases to the specified volume level. This soft mute feature provides for pop and click reduction in DAC signal path when the chip powers up.ADC soft mute features is controlled by **ADC_SMUTE_EN**.

5.3 DAC Auto Mute

This feature is implemented for DAC in NAU88L11. In the automatic mode, first the signal **AMUTE_EN,** REG 0x31[11] needs to be enabled. When 1024 consecutive zeros samples are detected, the analog mute signal is asserted and its status is written to **ANALOG_MUTE**, REG 0x59[10]. As soon as the first non-zero sample is detected,analog mute signal is de-asserted. If at any time there is a non-zero sample value, the DAC will be unmuted,and the 1024 count will be reinitialized to zero.

5.4 DAC Programmable Biquad Filter

Application Notes:

- Biquad filter coefficients for the DAC with 3.16 format for A1, A2, B0, B1, and B3 are located in below registers.
  - **BIQ1_COF2.BIQ_A1_H** and **BIQ1_COF1.BIQ_A1_L**
  - **BIQ1_COF4.BIQ_A2_H** and **BIQ1_COF3.BIQ_A2_L**
  - **BIQ1_COF6.BIQ_B0_H** and **BIQ1_COF5.BIQ_B0_L**
  - **BIQ1_COF8.BIQ_B1_H** and **BIQ1_COF7.BIQ_B1_L**
  - **BIQ1_COF10.BIQ_B2_H** and **BIQ1_COF9.BIQ_B2_L**

- To program the biquad filter in the DAC path, write **BIQ1_COF1** to **BIQ1_COF10** for coefficients.

To turn on the biquad filter in the DAC path, write ‘1’ to **BIQ1_COF10.BIQ1_EN**.

5.5 DAC Dynamic Range Control (DRC)

The DAC DRC functions in the same way as the ADC DRC explained in Section 4.1. However, different control registers are used.

5.5.1 Level Estimation

The Table 6 shows the attack and decay times for the peak level estimation. And, the time constant Ts is the the sampling time given by 1/(Sampling Frequency).

BITS	DRC_PK_COEF1_ADC	DRC_PK_COEF2_ADC
0000	Ts	63*Ts
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts

Table 6: DAC Level Estimation Attack and Decay Time Register Settings

5.5.2 Static Curve

The DRC static curve supports five programmable sections, and slope and knee points can be configured as shown in the Table 7.

Static Curve Section	Slope	Knee Point
LMT	0, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1	
CMP1	0, 1/2, 1/4, 1/8, 1/16, 1	0 to -31dB with -1dB step
CMP2	0, 1/2, 1/4, 1/8, 1/16, 1	0 to -63dB with -1dB step
EXP	1, 2, 4, 8	-18 to -81dB with -1dB step
NG	1, 2, 4, 8	-35 to -98dB with -1dB step

Table 7: DAC DRC Static Curve Control Registers

The Table 8 shows the attack and decay time for DRC. And, it needs to be carefully used combination with cross talk function because DRC is the last blocks in the path after mixer. Small cross-talk signal might be filtered out by DRC. The smooth knee function can be also enabled by register setting.

BITS	DRC_ATK_DAC	DRC_DCY_DAC
0000	Ts	63*Ts
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts
1000	511*Ts	16383*Ts
1001	1023*Ts	32757*Ts
1010	2047*Ts	65535*Ts
1011	4095*Ts	
1100	8191*Ts	

Table 8: DAC Static Curve Attack and Delay Time Register Settings

Application Notes:

- Smooth Knee function can be enabled by **DRC_SMTH_ENA_DAC, REG 0x3A[7].**
- The attack time can be set using **DRC_ATK_DAC, REG 0x3D[7:4].**
- The decay time can be set using **DRC_DCY_DAC, REG 0x3D[3:0]**.
- DRC needs to be carefully used combination with cross talk function because DRC is the last blocks in the path after mixer. Small cross-talk signal might be filtered out by DRC.

5.6 DAC Path with Sidetone

The ADC input channel and I2S channel are capable of being mixed into the output of the DAC. The figure below shows a block diagram of how this works along with the related registers

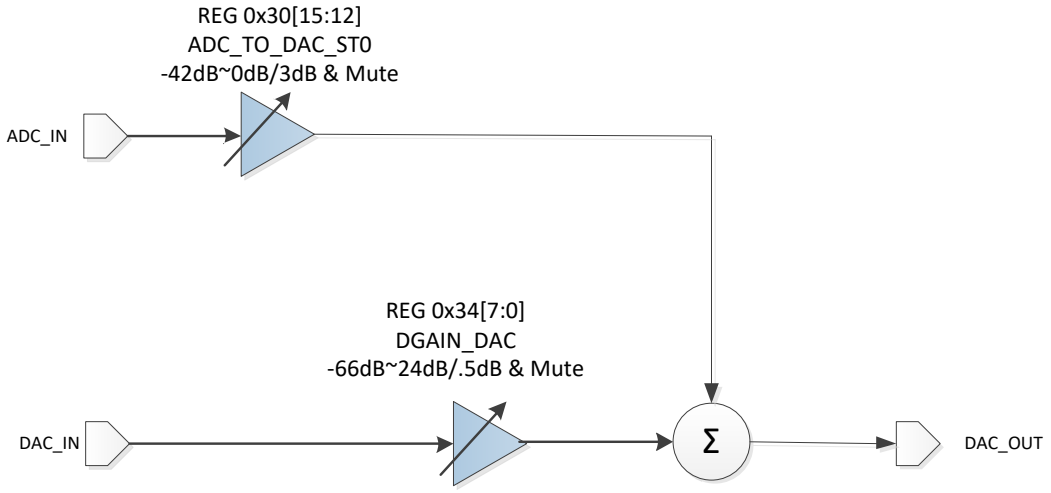


Figure 5 DAC Path Digital Mixer with Sidetone

DAC channel sidetone calculation:
DAC Mixer = DAC Data * DGAIN_DAC + ADC Data * ADC_TO_DAC_ST0

5.7 Speaker Output

The NAU88L11 features a differential speaker output (SPKOUT+ and SPKOUT-). The speaker amplifier is designed to drive a load differentially; a configuration referred to as Bridge-Tied Load (BTL). The gain of the speaker driver can be controlled in steps of 0.4dB from 0 to 5.6dB using **SPK_GAIN_CNTRL,** REG 0x52[3:0].

The differential speaker outputs can drive a single 8Ω speaker or two headphone loads of 16Ω or 32Ω or a line output. Driving the load differentially doubles the output voltage. The output of the speaker can be manipulated by changing attenuation and the volume (loudness of the output signal).

The output stage is powered by the speaker supply, VDDSPK, which are capable of driving up to 2.0V_{RMS} signals (equivalent to 4V_{RMS} into a BTL speaker). The speaker outputs can be controlled and can be muted individually. The output pins are at reference DC level when the output is muted.

5.8 Lineout Configuratioin

The Class AB amplifier includes a control circuit used in Lineout mode to precharge the amplifier output to the common mode voltage VCM (default 1.65V @ 3.3V). The precharge control smoothly charges the amplifier output towards VCM with negligible pop noise. Below is the code sequence to enable the precharge control and charge the output to VCM level with minimum pop noise.

Step	REG	Value	Comments
1	0076	2000	[13] = 1 to keep slow rising V_{REF}
2	002C	0072	[7:4] = 0x7 to turn on CIC and set CIC_GAIN_ADJ = x7, OSR128
	DELAY		//600ms by I^2C dummy write
3	0073	1108	[12] = 1 to enable DAC, [8] = 1 to enable DAC clock, [3:2] = 2'b10 to select DAC V_{REF} = 1.61V
4	0066	0062	[6] = 1 to enable VMID, [5:4]= 1,0 VMID tie-off selection options
5	0076	3000	[13] = 1 to keep slow rising V_{REF}; [12] = 1 for global bias enable
6	0051	0220	[9:6] VCM = 1.65V, [5] = 1 to enable VCM buffer, [4] = 0 to enable precharge, [3:2] = 2'b00 R-bias
7	DELAY		//600ms by I^2C dummy write
8	0001	3FC2	enable DAC, ADC in digital domain
9	0008	8000	[15] = 1 to power up the V_{REF} buffer
10	0052	00A0	[5] = 1 to power up the main speaker driver, [3:0] = 0 for gain
11	0051	220	[4] = 1 to disable precharge

Table 9 Lineout configuration for minimizing pop/click noise

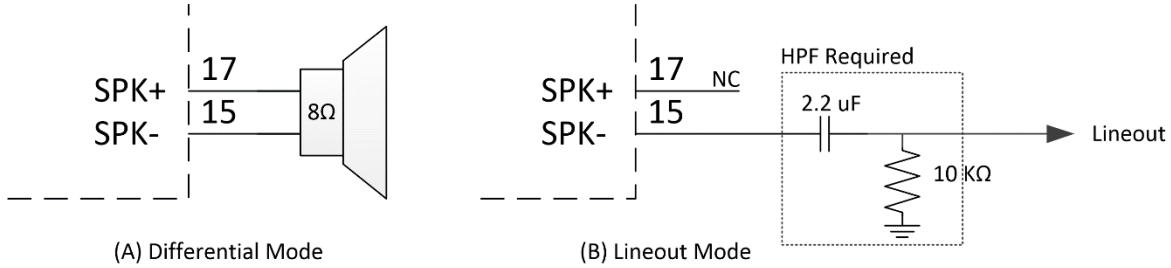


Figure 8:Load diagram

With the above sequence,the rise time is a function of C_{ext} and can be approximated by the equation $t_{rise} = 1 + 27*10^4*C_{ext}$ (example: for C_{ext}=2.2uF, R_L=10k, the rise time is ~ 1.6 secs).

5.9 Speaker Driver Short Circuit Protection

The short circuit protection is enabled by default with **DISABLE_SHRT_DET**, REG 0x76[6] set to 0.

When a ground short is detected, the chip starts limiting the short circuit current locally in the output driver. If FS clock is running and there is a short present, the **APR_EMERGENCY_SHUTDOWN** will be generated and the output driver will be in shut-down mode. If FS is not running, then the output driver will stay in the limiting mode when there is a short. A short to VDD will also activate the limiting-mode protection and may trigger an interrupt flag. INT will only be generated if MCLK is running.

When a short is detected, a short_detect signal is generated and sent to the APR digital block. After T1(2.FS) cycles, the apr_em_shutdown is generated and turns off the output driver. Then a counter is started and the driver is kept in the power-down mode for T2(2048.FS) cycles. The counter time is a function of FS clock frequency which is from 8KHz (min) to 96kHz (max). At the end of time T2, if a short is still present, the operation will restart the timer and the cycle is repeated. The user can read the **APR_EMRG_SHTDWN,** REG 0x10[9], short detect interrupt flag status bit. After reading, the interrupt flag the status can be cleared by writing to register **INT_CLR_KEY_STATUS[9]**.

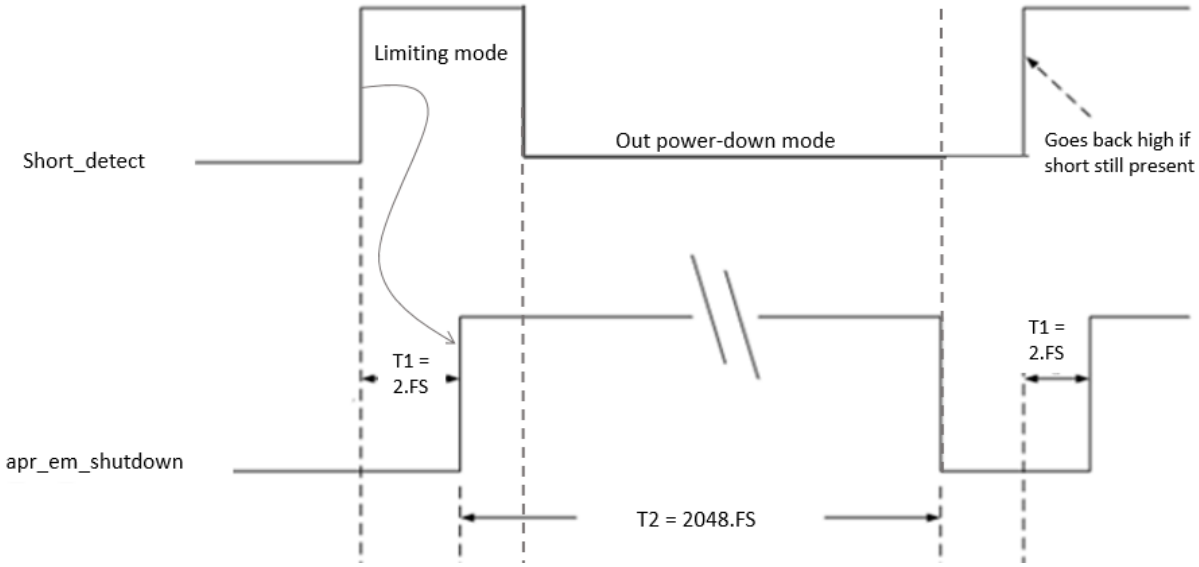


Figure 6 Speaker driver short-circuit protection timing

5.10 Companding

Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates using non-linear algorithms. The NAU88L11 supports the two main telecommunications companding standards on both transmit and receive sides: A-law and μ-law. The A-law algorithm is primarily used in European communication systems and the μ-law algorithm is primarily used by North America, Japan, and Australia.

Companding converts 14 bits (μ-law) or 13 bits (A-law) to 8 bits using non-linear quantization resulting in 1 sign bit, 3 exponent bits and 4 mantissa bits. When the companding mode is enabled, 8 bit word operation must be enabled.

Below two subsections contain the compression equations set by the ITU-T G.711 standard and implemented in the NAU88L11.

Both NAU88L11 ADC, DAC path supports companding format control.

- ADC: **I2S_PCM_CTRL1. ADCCM0**
- DAC: **I2S_PCM_CTRL1.DACCM0**

5.10.1 μ-law

$$F(x) = \frac{\ln(1+\mu \times |x|)}{\ln(1+\mu)}, \qquad -1 < x < 1$$

$$\mu = 255$$

5.10.2 A-law

$$F(x) = \frac{A \times |x|}{(1+\ln(A))}, \qquad 0 < x < \frac{1}{A}$$

$$F(x) = \frac{(1+\ln(A \times |x|)}{(1+\ln(A))}, \qquad \frac{1}{A} \le x \le 1$$

$$A = 87.6$$

6. Power Up and Start Sequence

The power up sequence to bring up the analog blocks smoothly is illustrated below and involves three different time segments (T1 – T3). The power supply ramp rate depends on a number of factors such as the power source drive strength, board parasitics and the decopling capacitor size on the supply line. Typically, a power supply ramp time can be as fast as 5mS or as slow as 200mS.

During time T1, the power supply ramps-up. The internal PORB reset is generated when V_{DDA} is lower than 1.1V for reliable maintenance of internal logic circuits. While PORB signal is low, it clears internal digital flops. Most of the flops will be cleared to '0' while some flops can be set to '1' during the PORB pulse depending on the required default state of the register.

After time T1, wait another time 1mS so that the power supply is stable before writing to the registers. During time T2, the chip is in stand-by mode and all registers are in a default state. In stand-by, the chip only consumes leakage current and all analog blocks are turned-off. At time T3, the user can start to write data into the registers via the I2C serial bus to setup the chip for their application.

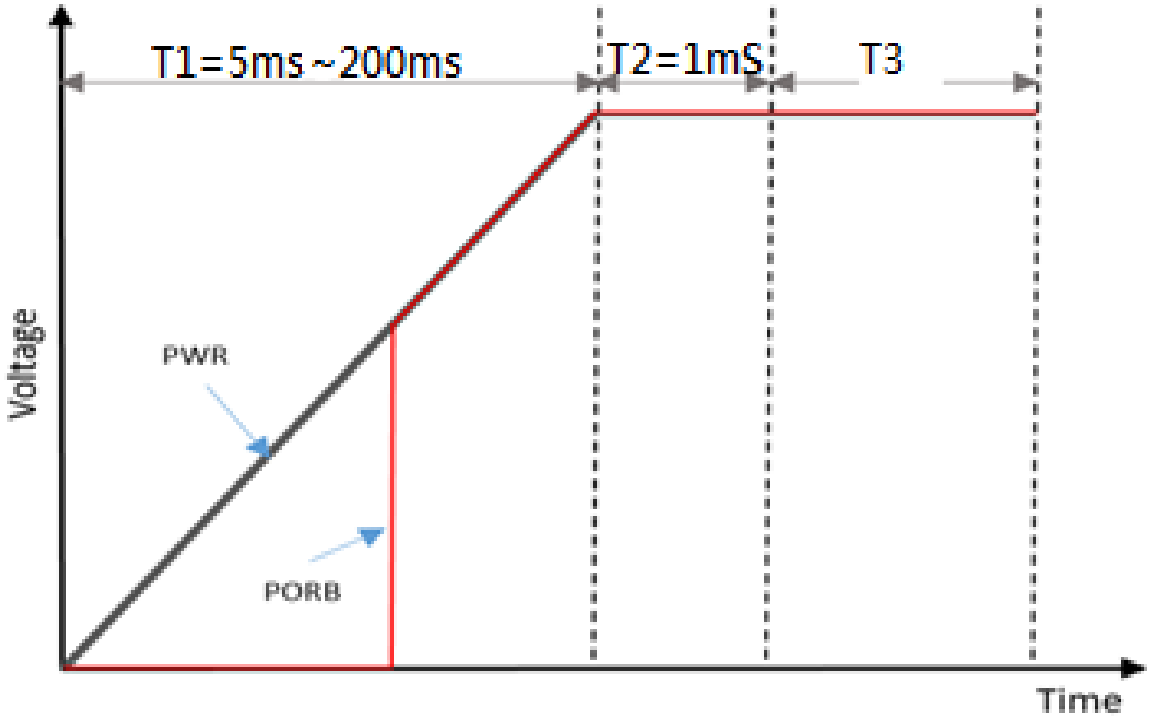


Figure 7 Power Up Sequence

6.1 Basic Register Sequence

The following register sequence in the table below is a general guide to help setup the NAU88L11. This can be done after time T3 shown in Figure above following the power up sequence.

Below sequence is based on MCLK = 12.288MHz, FS=48KHz, with MIC enabled to ADC, Sidetone to DAC/SPK, and I2S to DAC/SPK features enabled.

Function	Register Name	REG	Value	Config Comment	Default Setting
Power Up					
Power Setting	**SOFTWARE_RST**	0x00	0x0000	Software Reset	0x0000
MCU		delay 10ms			
ADC Path	**MUTE_CTRL**	0x31	0x0200	**SMUTE_EN** =1 (ADC soft-mute)	0x0000
DAC Path	**DAC_CTRL1**	0x2C	0x0072	**CIC_GAIN_ADJ** = 3b'111 (fine tuning DAC output glich)	0x0082
ADC/DAC Path					
DAC Path	**VCM_BUF**	0x51	0x0230	**PDB_VCMBUF** = 1 (VCM buffer Power Up) **VOUT_PRECHG_ DISABLE** = 1 (Output VCM precharge disable)	0x0210
DAC Path	**SPK_DRV**	0x52	0x00AB	**PUP_MAIN_DRV** = 1 (main speaker driver Power Up) **SPK_GAIN_CNTRL** = 4b'1011 (SPK 4-bit gain = 4.4dB)	0x0080
ADC Path	**BIAS_ADJ**	0x66	0x0060	**VMIDEN**=1 (VMID enable) **VMIDSEL**=2b'10 (VMID 125k ohm)	0x0000
DAC Path	**SPARE_ ANALOG1**	0x69	0x0020	**THD_BOOST** = 1 (thd_boost path enable)	0x0000
ADC Path	**ANALOG_ ADC_2**	0x72	0x0140	**PDNOT** = 1 (ADC Power Up)	0x0100
DAC Path	**DAC**	0x73	0x1108	**DAC_EN** = 1 (DAC enable) **CLK_DAC_EN** = 1 (DAC clock enable)	0x0008
ADC Path	**MIC_BIAS**	0x74	0x0104	**POWERUP** = 1 (MICBIAS Power Up)	0x0004
Power Setting	**BOOST**	0x76	0x3040	**STG2_SEL** = 1 (PGA in class A mode) **PDVMDFST** = 1 (VMID Pre-charge disable) **BIASEN** = 1 (Global Analog Bias enable)	0x0040
ADC Path	**PGA_GAIN**	0x7E	0x0B00	**PGA_GAIN** = 6b'001011 (PGA gain 10dB)	0x0000
ADC Path	**POWER_ UP_ CONTROL**	0x7F	0x8000	**PUPL** = 1 (PGA Power Up)	0x0000

Function	Register Name	REG	Value	Config Comment	Default Setting
Audio System Control System					
Power Setting	**ENA_CTRL**	0x01	0x3FC6	**DACEN** = 1 (DAC enable) **ADCEN** = 1 (ADC enable) **DCLK_ADC_EN** = 1 (ADC clock enable) **DCLK_DAC_EN** = 1 (DAC clock enable) **CLK_BIST_EN** = 1 (BIST clock Enable) **CLK_I2S_EN** = 1 (I2S clock enable) **CLK_DRC_EN** = 1 (DRC clock enable) **MCLK_RNG_SEL** = 3b'000 (15.74MHz or lower frequency) **SYSCLK_SEL** = 0 (SYSCLK = 1*MCLK)	0x03FE
Clock Setting	**CLK_DIVIDER**	0X03	0x0050	**CLK_ADC_SRC** = 2b'01 **(**Scaling for ADC clock from MCLK_INT – div by 1) **CLK_DAC_SRC** = 2b'01 (Scaling for DAC clock from MCLK_INT – div by 1) **MCLK_DIV** = **3b'000** (Scaling for MCLK_INT from SYSCLK_SRC – div by 1)	0x0050
ADC Path	**ADC_DGAIN_CTRL**	0x30	0xF000	**ADC_TO_DAC_ST0** = 4b'1111 (ADC to DAC Sidetone = 0dB)	0x0000
ADC Path	**MUTE_CTRL**	0x31	0x0000	**SMUTE_EN** =0 (ADC soft-unmute)	0x0000

Table 10 Reference Setup Sequence

6.2 Clock Detection

The NAU88L11 includes a Clock Detection circuit that can be used to enable and disable the audio path, based on an initialized audio path setting. If MCLK is detected on the input, a status flag in **MCLK_DET_INT**, REG 0x10[5] will be set, when MCLKDETECT signal going active, as described by the block diagram below.

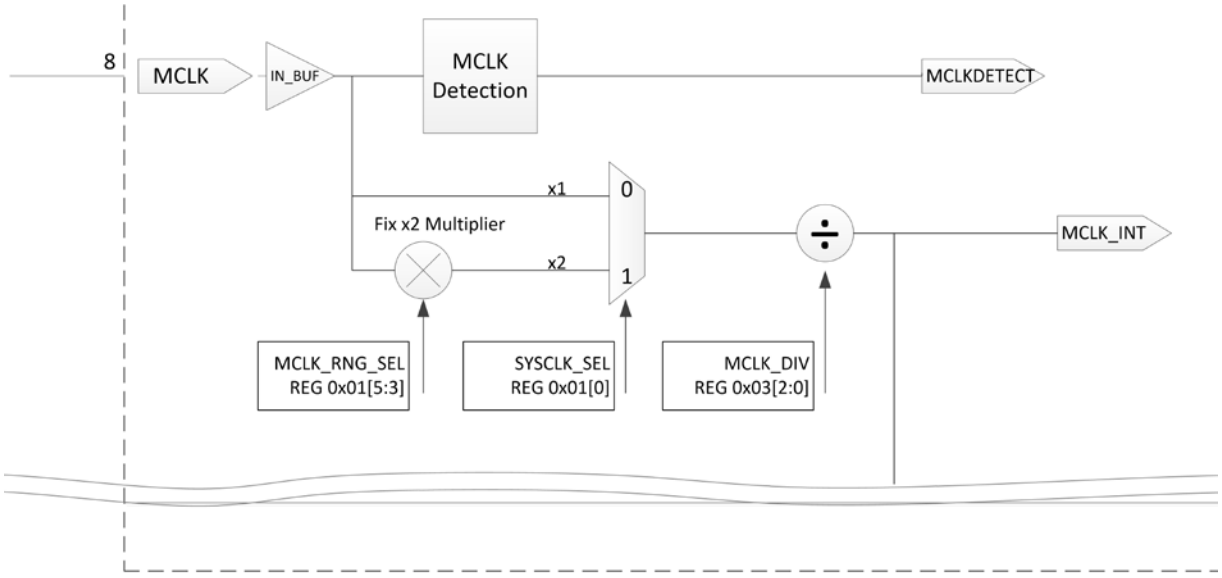


Figure 8 NAU88L11 Clock Detection

For MCLK/FS input pin in slave mode, the range of input frequency are defined here.

Input Signal	Pin Name	Min	Max	Unit
Frame Synch	FS	8	96	kHz
Master Clock	MCLK	2.048	24.576	MHz

Table 11 Range of MCLK/FS for Slave Mode

System design should be checked that MCLK/FS adhere to the frequency range, then follow the later section to pick out the correct setting, and supported combinations.

From MCLK input pin, the MCLK signal can be routed for two path, controlled by **SYSCLK_SEL**, REG 0x01[0]. Aside from the direct path (x1), the multipler path applies a fix multiplier to double the MCLK frequency. In order to adjust for 50% duty cycle, **MCLK_RNG_SEL**, REG 0x01[5:3] is a required frequency range setting while the multipler path is selected. The MCLK input frequency range is divided into three band, from 2.048MHz~ 15.74MHz, 15.74MHz ~ 21.6MHz, 21.6MHz to 24.576MH by setting **MCLK_RNG_SEL.**

6.3 MCLK / FS Clock Setting in Slave Mode

For slave mode, the NAU88L11 can accept exteral clocks from MCLK/FS input pin. Based on the MCLK and FS input with internal logic to derive MCLK_INT, and CLK_DAC, CLK_ADC for related internal ADC/DAC, DSP, Digital Audio Interface and other internal subsystems.

The figure below provides the full clock distribution diagram, and the key registers are liste here:

- MCLK_DIV, REG 0x03[2:0]
- CLK)CODEC_SRC, REG 0x03[13]
- CLK_ADC_SRC, REG 0x03[7:6]
- CLK_DAC_SRC, REG 0x03[5:4]

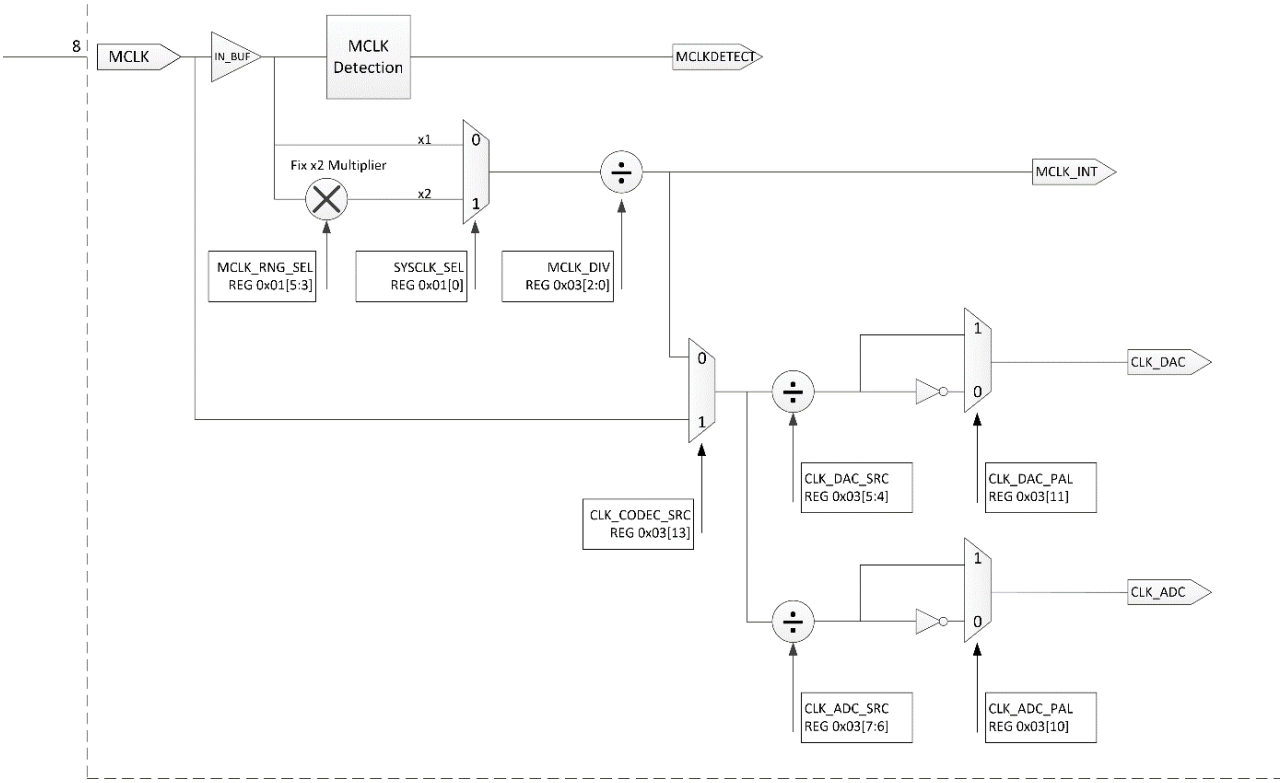


Figure 9 NAU88L11 MCLK and Clock Distribution

The NAU88L11 Clock distribution and subsystem is design to minize design effort with simplified setting. The relationship of MCLK/FS input frequency combianations will be described in details below.

The MCLK/FS input frequency range is described in previous section where MCLK input frequency should be between 2.048MHz ~ 24.567MHz. And, FS should be between 8KHz ~ 96KHz.

The internal clock distribution of NAU88L11 is designed support 3 MCLK_INT/FS ratios, which are 256, 400, 500. Please note MCLK_INT refers to the internal MCLK frequency after MCLK Divider. This means the MCLK/FS input frequency combation should consider the Multiplier/direct path selected by **SYSCLK_SEL**, and also the **MCLK_DIV** divider.

Below table are the key criterion for MCLK/FS input frequencies supported organized by the MCLK_INT/FS Ratio into 3 group.

Group1: MCLK_INT/FS Ratio of 256	
SYSCLK_SEL set x1 path	
Target FS	8/16/24 ..44.1/96KHz
MCLK	Target FS * **MCLK_DIV***256
Register Related	**MCLK_DIV**, **SYSCLK_SEL**
SYSCLK_SEL set x2 path	
Target FS	8/16/24 ..44.1/96KHz
MCLK	Target FS * MCLK_DIV*256/2
Register Related	**MCLK_DIV**, **MCLKSEL**, **SYSCLK_SEL**
Group2: MCLK_INT/FS Ratio of 400	
SYSCLK_SEL set x1 path	
Target FS	8/16/24 ..44.1/96KHz
MCLK	Target FS * **MCLK_DIV***400
Register Related	**MCLK_DIV**, **SYSCLK_SEL** **CLK_ADC_SRC, CLK_DAC_SRC** must set as 1/4
SYSCLK_SEL set x2 path	
Target FS	8/16/24 ..44.1/96KHz
MCLK	Target FS * **MCLK_DIV***400/2
Register Related	**MCLK_DIV**, **MCLKSEL**, **SYSCLK_SEL** **CLK_ADC_SRC, CLK_DAC_SRC** must set as 1/4
Group 3: MCLK_INT/FS Ratio of 500	
SYSCLK_SEL x1/x2	
Notes	• Support list is provided in appendix • No need to set **CLK_DAC_SRC, CLK_DAC_SRC** is fixed
Register Related	**MCLK_DIV**, **MCLKSEL**, **SYSCLK_SEL**

Table 12 Criterion for supported MCLK/FS for slave mode

Following above table, one more limit is added, which is from generating CLK_ADC, CLK_DAC, which should be less than or equal to 6.144MHz.

- CLK_DAC = MCLK_INT * **CLK_DAC_SRC**
- CLK_ADC = MCLK_INT * **CLK_ADC_SRC**

Following the above 3 group of criterion to pick out the correct MCLK/FS combinations is essential for system design. A full list of supported MCLK/FS combinations and related settings can be found in the apptediex section for Group 1~3.

6.4 ADC/DAC Oversampling Rate

ADC/DAC Oversample rate setting is used in the NAU88L11 ADC/DAC blocks beyond the CLK_DAC, CLK_ADC signal described in previous clock distribution figure.

The the conditions to set **OSR_ADC_RATE**, **OSR_DAC_RATE** for MCLK_INT/FS ratio of 256 is listed below.

- CLK_ADC = **OSR_ADC_RATE** * FS (<=6.144MHz)
- CLK_DAC = **OSR_DAC_RATE** * FS (<=6.144MHz)

For MCLK_INT/FS ratios of 400/500, oversample rate is fixed as 100, therefore no need to set **OSR_ADC_RATE/OSR_DAC_RATE**

Example 1:

MCLK=24.576MHz, FS=96KHz

- The Ratio here is picked as 24.576MHz = 256 * 96KHz
  - **SYSCLK_SEL** can be set either x1 or x2 path
  - For x1 path, **MCLK_DIV** is set as divid by 1, MCLK_INT=24.576MHz
  - For x2 path, **MCLK_DIV** is set as divid by 2, MCLK_INT=24.575MHz
- Based on CLK_ADC = MCLK_INT * **CLK_ADC_SRC** (<=6.144MHz)
  - Avialble **OSR_ADC_RATE** option for each **CLK_ADC_SRC** are listed below in Green for each CLK_ADC
  - For CLK_ADC as 6.144MHz, the ORS_ADC_RATE should be set as 64, so the clock would match as below table in green
  - For CLK_ADC as 3.072 MHz, the ORS_ADC_RATE should be set as 32, so the clock would match as below table in green

		CLK_ADC=MCLK_INT*CLK_ADC_SRC (<=6.144MHz)			
		24.576	12.288	6.144	3.072
FS*OSR (<=6.144MHz)	32	-	-	3.072	3.072
	64	-	-	6.144	6.144
	128	-	-	12.288	12.288
	256	-	-	24.576	24.576

Example 2:

MCLK=19.2MHz, FS=32KHz

- The Ratio here is picked as MCLK_INT 12.8MHz = 400 * 32KHz
  - **SYSCLK_SEL** is set as x2 path
  - For x2 path, **MCLK_DIV** is set as divid by 3, MCLK_INT=12.8MHz
- With MCLK_INT/FS Ratio of 400.
  - **CLK_ADC_SRC/CLK_DAC_SRC** must be set as divid by 4.
  - No need to set **OSR_ADC_RATE/OSR_DAC_RATE**

7. Control Interfaces

The NAU88L11 includes a serial control bus that provides access to all the device control registers, it may be configured as a 2-wire interface that conforms to industry standard implementations of the I^{2}C serial bus protocol.

7.1 2-Wire-Serial Control Mode (I^{2}C Style Interface)

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and any device receiving data as the receiver (or slave). The NAU88L11 can function only as a slave when in the 2-wire interface configuration.

7.2 2-Wire Protocol Convention

All 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH. All 2-Wire interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

An acknowledge (ACK), is a software convention used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.

Following a START condition, the master must output a device address byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W=1, this indicates the master is initiating a read operation from the slave device, and when R/W=0, the master is initiating a write operation to the slave device. If the device address matches the address of the slave device, the slave will output an ACK during the period when the master allows for the ACK signal.

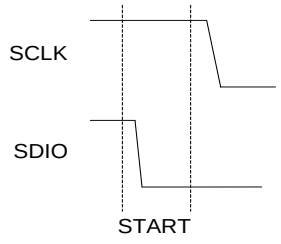


Figure 10 Valid START Condition

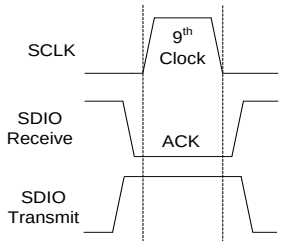


Figure 11 Valid Acknowledge

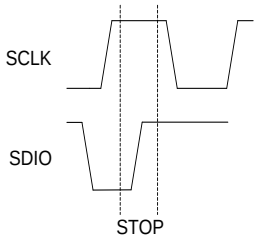


Figure 12 Valid STOP Condition

Please Note:

- Sometimes, I^{2}C needs to use level shifter between different supplies domains. During Acknowledge as below figure, receiver side (CODEC) will pull low, and transmit side (MCU) is disable and pull high by pull high resistor. Because NAU88L11 SDIO can sink 2mA by default setting (maximum up to 8mA,) shown as below **Error! Reference source not found.**, R_{PU1} and R_{PU2} need to be select

such that total current V_{DDB}/R_{PU1}+ VDD_MCU/R_{PU2} during Acknowledge should not be too large to exceed SDIO sinking capability.

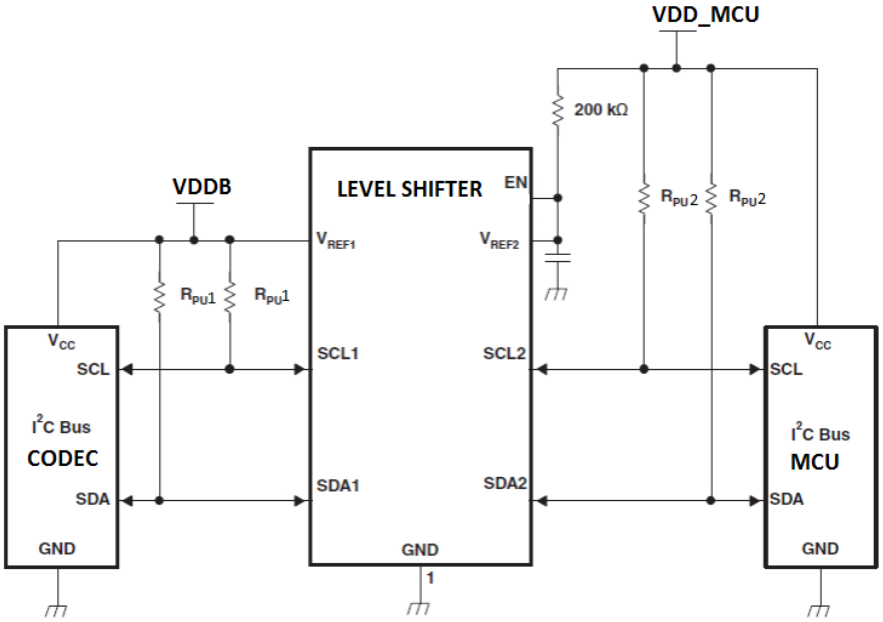


Figure 13 Typical I2C level shifter circuit

7.3 2-Wire Write Operation

A Write operation consists of a three-byte instruction followed by one or more Data Bytes. A Write operation requires a START condition, followed by a valid device address byte with R/W=0, a valid control address byte, data byte(s), and a STOP condition. The Device Address of the NAU88L11 is fixed to 0x1B. If the Device Address matches this value, the NAU88L11 will respond with the expected ACK signaling as it accepts the data being transmitted to it.

0	0	1	1	0	1	1	R/W	Device Address Byte
A15	A14	A13	A12	A11	A10	A9	A8	Control Address Bytes
A7	A6	A5	A4	A3	A2	A1	A0	
D15	D14	D13	D12	D11	D10	D9	D8	Data Bytes
D7	D6	D5	D4	D3	D2	D1	D0	

Figure 14 Slave Address Byte, Control Address Byte, and Data Byte

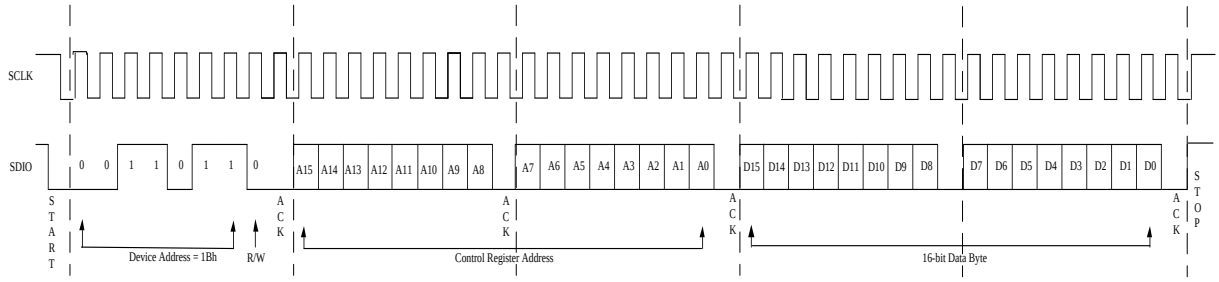


Figure 15 2-Wire Write Sequence

7.4 2-Wire Read Operation

A Read operation consists of a three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, device address byte with the R/W bit set to “0”, and a Control Register Address byte. This indicates to the slave device which of its control registers is to be accessed.

If the device address matches this value, the NAU88L11 will respond with the expected ACK signaling as it accepts the Control Register Address being transmitted into it. After this, the master transmits a second START condition, and a second instantiation of the same device address, but now with R/W=1.

After again recognizing its device address, the NAU88L11 transmits an ACK, followed by a two byte value containing the 16 bits of data from the selected control register inside the NAU88L11.

During this phase, the master generates the ACK signaling with each byte transferred from the NAU88L11. If there is no STOP signal from the master, the NAU88L11 will internally auto-increment the target Control Register Address and then output the two data bytes for this next register in the sequence.

This process will continue as long as the master continues to issue ACK signaling. If the Control Register Address being indexed inside the NAU88L11 reaches the value 0xFFFF (hexadecimal) and the value for this register is output, the index will roll over to 0x0000. The data bytes will continue to be output until the master terminates the read operation by issuing a STOP condition.

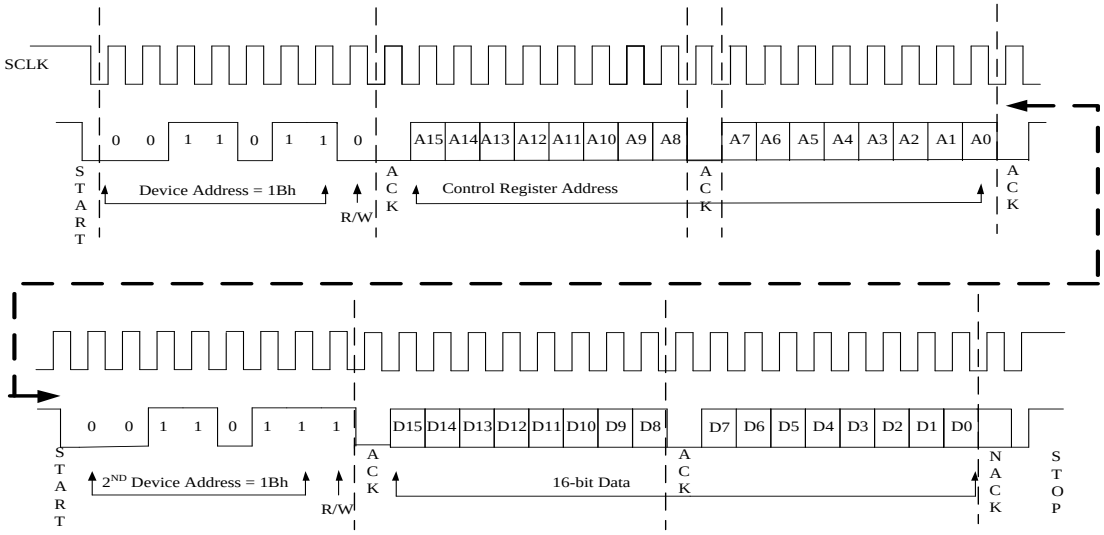


Figure 16 Two-wire Read Sequence

7.5 Digital Serial Interface Timing

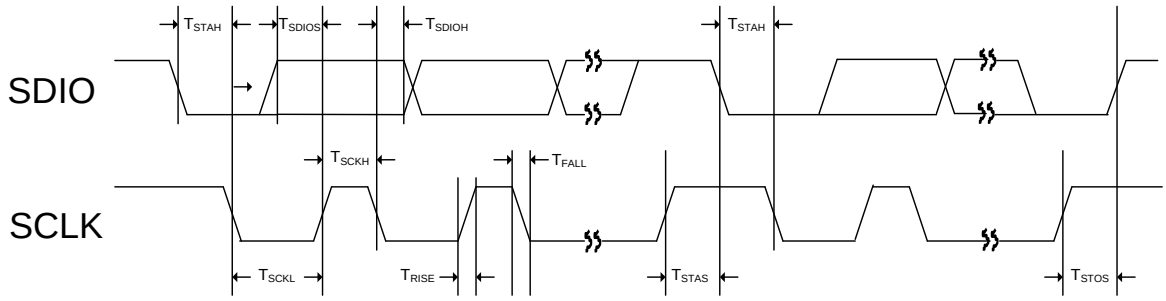


Figure 17 Two-wire Control Mode Timing

Symbol	Description	min	typ	max	unit
T_{STAH}	SDIO falling edge to SCLK falling edge hold timing in START / Repeat START condition	600	-	-	ns
T_{STAS}	SCLK rising edge to SDIO falling edge setup timing in Repeat START condition	600	-	-	ns
T_{STOS}	SCLK rising edge to SDIO rising edge setup timing in STOP condition	600	-	-	ns
T_{SCKH}	SCLK High Pulse Width	600	-	-	ns
T_{SCKL}	SCLK Low Pulse Width	1,300	-	-	ns
T_{RISE}	Rise Time for all 2-wire Mode Signals	-	-	300	ns
T_{FALL}	Fall Time for all 2-wire Mode Signals	-	-	300	ns
T_{SDIOS}	SDIO to SCLK Rising Edge DATA Setup Time	100	-	-	ns
T_{SDIOH}	SCLK falling Edge to SDIO DATA Hold Time	0	-	600	ns

Table 13 2-Wire Serial Interface Timing

7.6 Software Reset

The NAU88L11 and all of its control registers can be reset to “default”, initial conditions by writing any value to REG 0x00 using the two-wire interface mode.

7.7 I²C Addresses

The NAU88L11 has 7 bits assigned to the device for I²C address, the eighth bit of the command byte is a R/W bit. The 7 I²C address bits are hard coded by metal layer internal to the device. The default set for read and write is shown below:

	Bit<6>	Bit<5>	Bit<4>	Bit<3>	Bit<2>	Bit<1>	Bit<0>	R/W
Read Address	0	0	1	1	0	1	1	1
Write Address	0	0	1	1	0	1	1	0

Table 14 I²C Adress Table

8. Digital Audio Interfaces

The NAU88L11 can be configured as either the master or the slave, by setting register **MS0,** in REG 0x1D[3], to 1 for master mode and to 0 for slave mode. Slave mode is the default if this bit is not written. In master mode, NAU88L11 outputs both Frame Sync (FS) and the audio data bit clock (BCLK) and has full control of the data transfer. In the slave mode, an external controller supplies BCLK and FS. Data is latched on the rising edge of BCLK; SDO clocks out ADC data, while SDI clocks in data for the DACs.

When not transmitting data, SDO pulls LOW in the default state. Depending on the application, the output can be configured to pull up or pull down. When the time slot function is enabled (see below), there are additional output state modes including controlled tristate capability. NAU88L11 supports five audio formats; left justified, I2S, PCMA, PCMB, and PCM Time Slot. Below table shows digital audio interface modes

PCM Mode	**I2S_PCM_CTRL1.AIFMT0** REG 0x1C[1:0]	**I2S_PCM_CTRL1.LRP0** REG 0x1C[6]	**I2S_PCM_CTRL2.PCM_TS_EN0** REG 0x1D[10]
Left Justified	01	0	0
I^2S	10	0	0
PCMA	11	0	0
PCMB	11	1	0
PCM Time Slot	11	Don't care	1

Table 15 Digital Audio Interface Support Modes

8.1 Right-Justified Audio Data

In right-justified mode, the LSB is clocked on the last BCLK rising edge before FS transitions. When FS is HIGH, channel_0 data is transmitted and when FS is LOW, channel_1 data is transmitted. This can be seen in the image below.

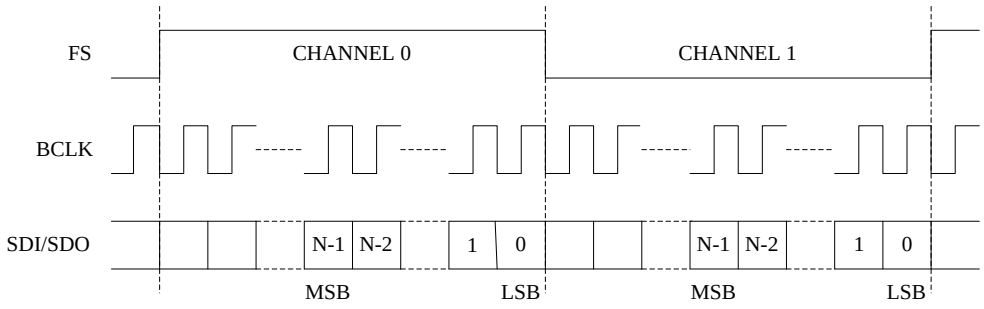


Figure 18 Right-Justified Audio Interface

8.2 Left-Justified Audio Data

In left-justified mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, channel_0 data is transmitted and when FS is LOW, channel_1 data is transmitted. This can be seen in the figure below.

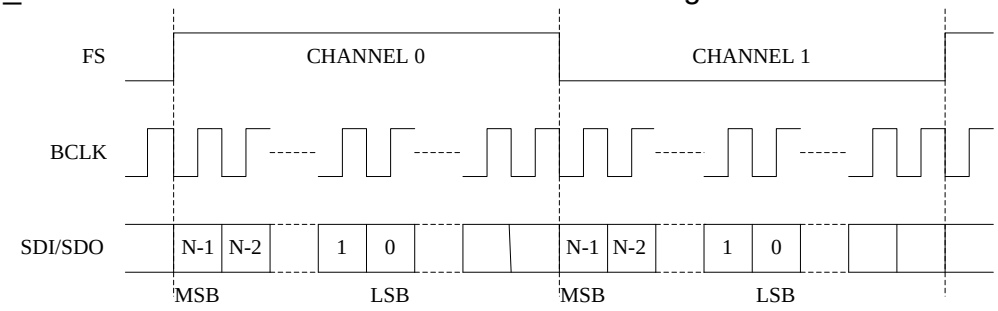


Figure 19 Left-Justified Audio Interface

8.3 I2S Audio Data

In I^{2}S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, left channel data is transmitted and when FS is HIGH, right channel data is transmitted. This can be seen in the figure below.

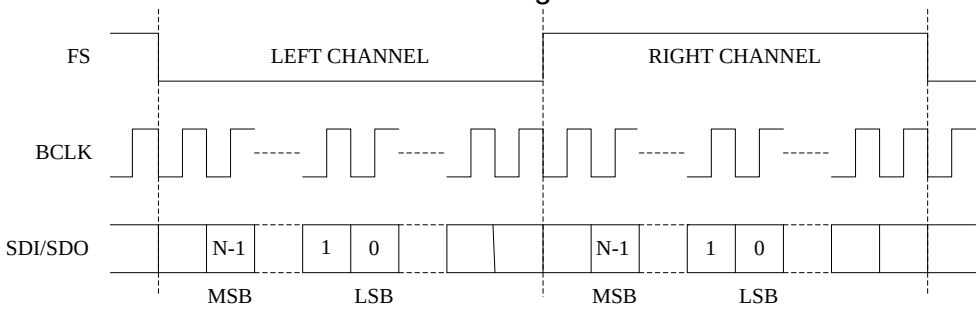


Figure 20 I2S Audio Interface

8.4 PCMA Audio Data

In the PCM A mode, channel 0 data is transmitted first followed immediately by channel 1 data. The channel 0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and channel 1 MSB is clocked on the next BCLK after the left channel LSB. This can be seen in the figure below.

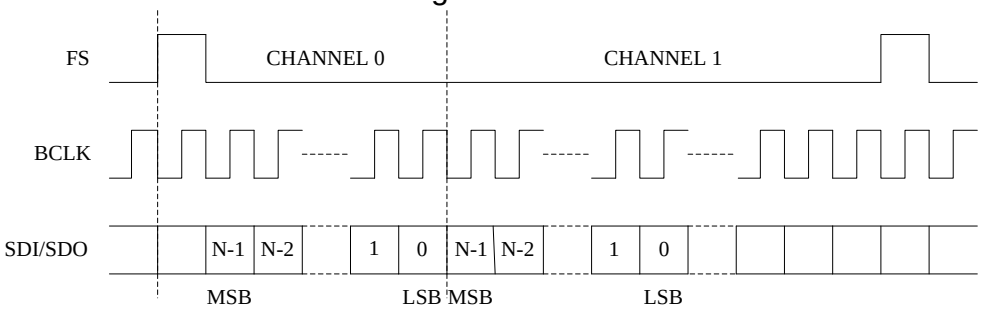


Figure 21 PCMA Audio Interface

8.5 PCMB Audio Data

In the PCMB mode, channel_0 data is transmitted first followed immediately by channel_1 data. Channel 0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and channel_1 MSB is clocked on the next BCLK after channel_0 LSB. This can be seen in the figure below.

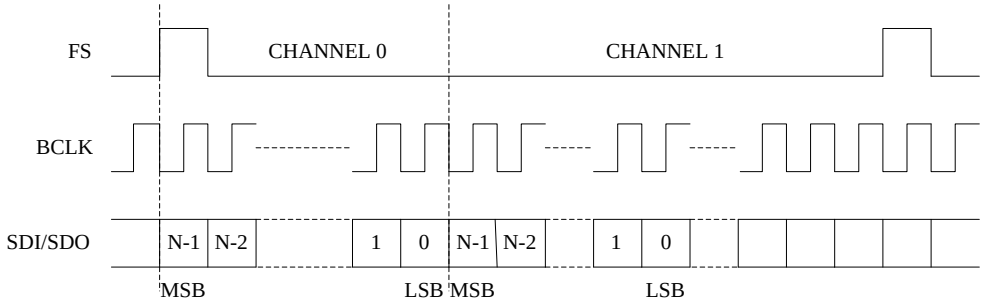


Figure 22 PCMB Audio Interface

8.6 PCM Time Slot Audio Data

The PCM time slot mode is used to allocate different time slots for ADC and DAC data. This can be useful when multiple NAU88L11 chips or other devices are sharing the same audio bus. This will allow each chip audio to be delayed around each other without interference.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS), however, in the PCM time slot mode; the audio data can be delayed by left / right channel PCM time slot start value in the registers.
These delays can be seen before the MSB in the figure below.

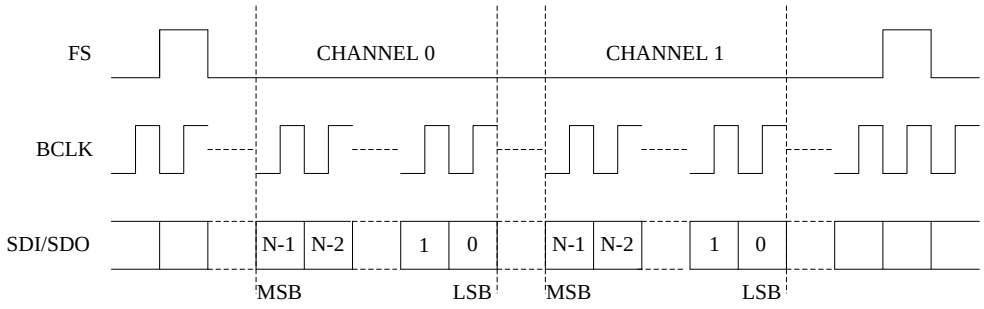


Figure 23 PCM Time Slot Audio Interface

The PMC time slot mode can be also used to swap channel 0 and channel 1 audio or cause both channels to use the same data. When using the NAU88L11 with other driver chips, the SDO pin can be set to pull up or pull down or high impedance during no transmission. Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots with reduced risk of bus driver contention.

8.7 TDM I2S Audio Data

In I²S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, channel_0 then channel_2 data is transmitted and when FS is HIGH, channel_1 then channel_3 data is transmitted. This is shown in the figure below.

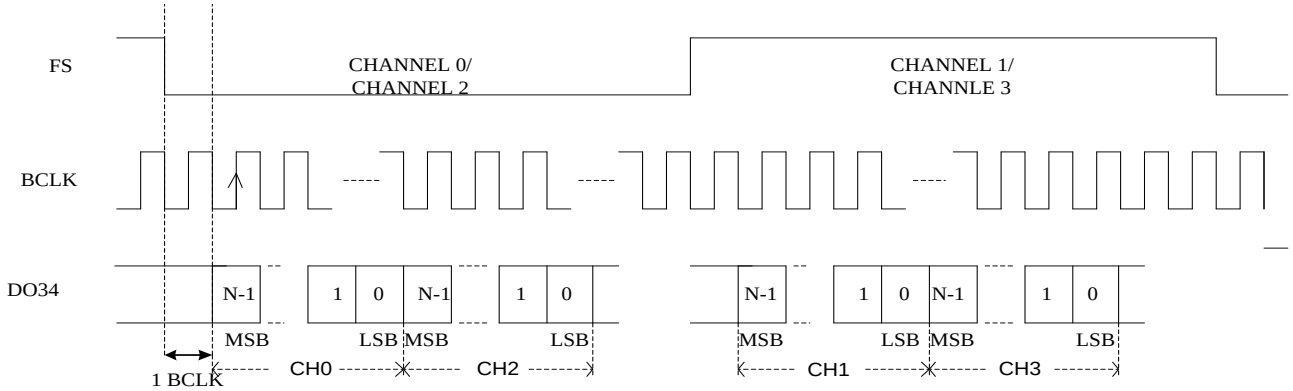


Figure 24 TDM I2S Audio Format

8.8 TDM PCMA Audio Data

In the PCMA mode, channel_0 data is transmitted first followed sequentially by channel_1, 2, and 3 immediately after. The channel_0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in the figure below.

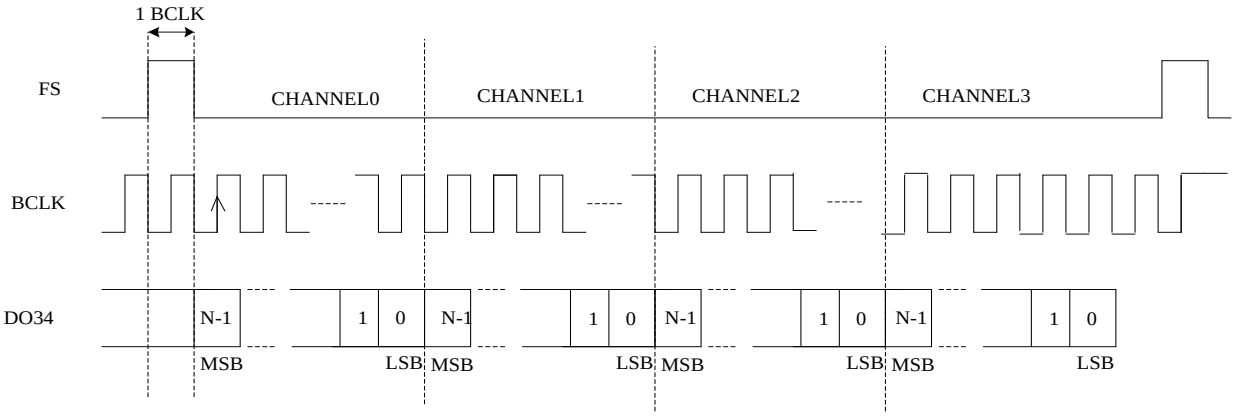


Figure 25 TDM PCMA Audio Format

8.9 TDM PCMB Audio Data

In TDM PCMB mode, channel_0 data is transmitted first followed immediately by channel_1 data. The channel_0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and channel_1 MSB is clocked on the next SCLK after channel_0 LSB.

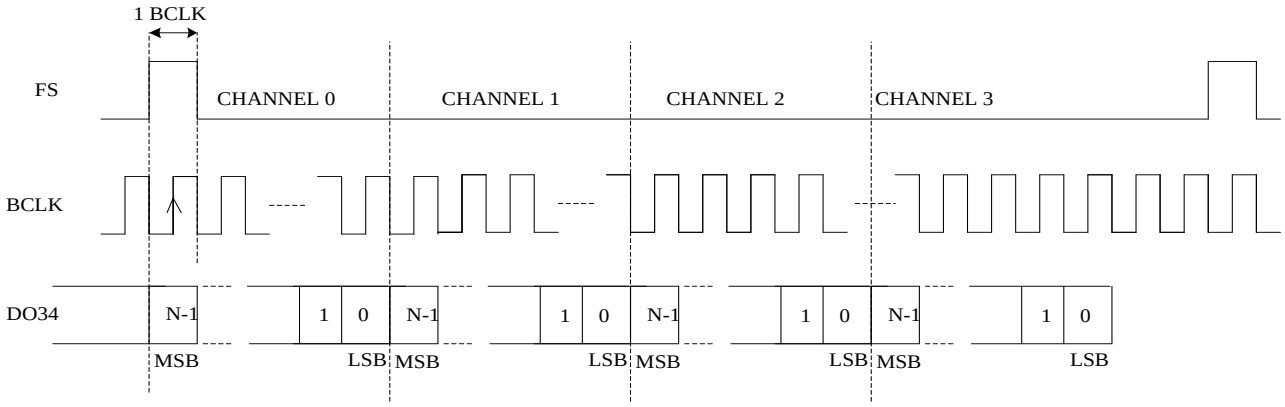


Figure 26 TDM PCMB Audio Format

8.10 TDM PCM Offset Audio Data

The PCM offset mode is used to delay the time at which DAC data is clocked. This increases the flexibility of the NAU88L11 to be used in a wide range of system designs. One key application of this feature is to enable multiple NAU88L11 or other devices to share the audio data bus, thus enabling more than four channels of audio. This feature may also be used to swap channel data, or to cause multiple channels to use the same data.

Normally, the DAC data are clocked immediately after the Frame Sync (FS). In this mode audio data is delayed by a delay count specified in the device control registers. The channel 0 MSB is clocked on the BCLK rising edge defined by the delay count set in .This can be seen in the figure below.

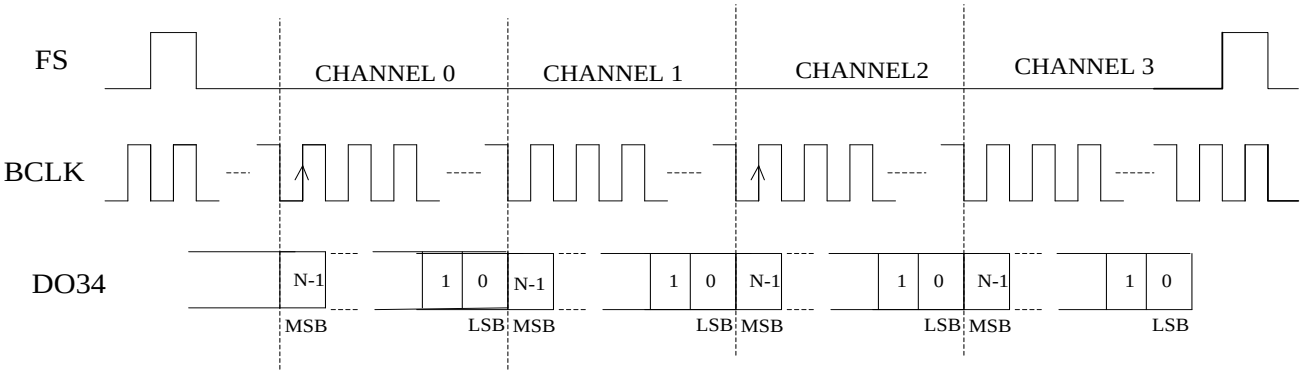


Figure 27 TDM PCM Offset Audio Format

8.11 Digital Audio Interface Timing Diagrams

8.11.1 Digital Audio Interface Slave Mode

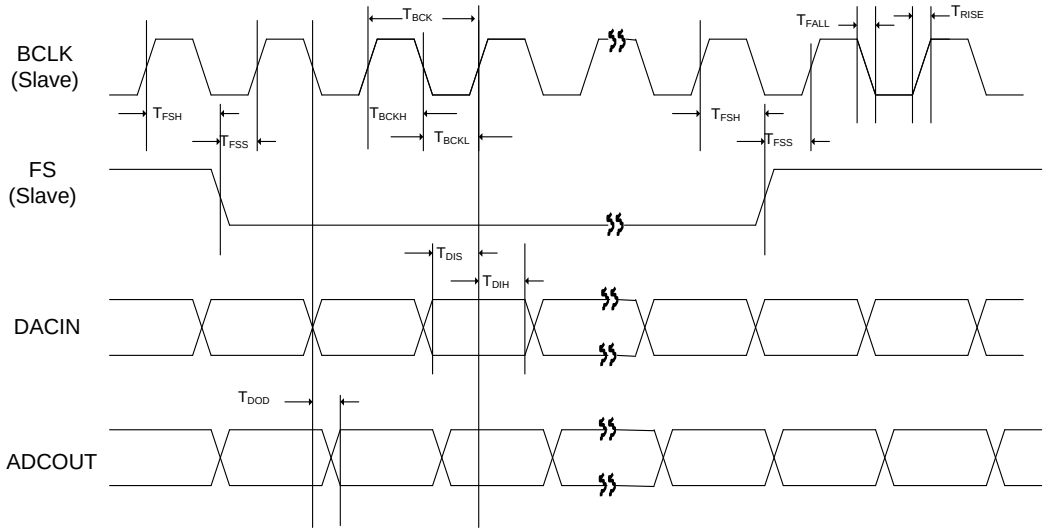


Figure 28 Audio Inteface Mode Slave Timing

Symbol	Description	min	typ	max	unit
T_{BCK}	BCLK Cycle Time in Slave Mode	50	-	-	ns
T_{BCKH}	BCLK High Pulse Width in Slave Mode	20	-	-	ns
T_{BCKL}	BCLK Low Pulse Width in Slave Mode	20	-	-	ns
T_{FSS}	FS to BCLK Rising Edge Setup Time in Slave Mode	20	-	-	ns
T_{FSH}	BCLK Rising Edge to FS Hold Time in Slave Mode	20	-	-	ns
T_{RISE}	Rise Time for All Audio Interface Signals	-	-	$0.135T_{BCK}$	ns
T_{FALL}	Fall Time for All Audio Interface Signals	-	-	$0.135T_{BCK}$	ns
T_{DIS}	DACIN to BCLK Rising Edge Setup Time	15	-	-	ns
T_{DIH}	BCLK Rising Edge to DACIN Hold Time	15	-	-	ns
T_{DOD}	BCLK Falling Edge to ADCOUT Delay Time	-	-	10	ns

Table 16 Audio Interface Slave Mode Timing Parameters

9. Control and Status Registers

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
0	SOFTWARE_RST	RESET_N_SOFT_PRE																	Reset the signal once write to the register.
1	ENA_CTRL	CMLCK_ENB																	PGA Common Mode Lock; '0'=enabled, '1'=disabled
		CLK_DAC_INV																	DAC clock inversion in analog domain 1 = Enable 0 = Disable
		DACEN																	DAC Enable (digital path) 1 = ON 0 = OFF
		ADCEN																	ADC Enable (digital path) 1 = ON 0 = OFF
		DCLK_ADC_EN																	ADC Clock Enable 1 = ON 0 = OFF
		DCLK_DAC_EN																	DAC Clock Enable 1 = ON 0 = OFF
		CLK_BIST_EN																	BIST Clock Enable 1 = ON 0 = OFF
		CLK_I2S_EN																	I2S Clock Enable 1 = ON 0 = OFF
		CLK_DRC_EN																	DRC Clock Enable 1 = ON 0 = OFF
		MCLK_RNG_SEL																	MCLK Pin input frequency range select [000] =15.74MHz or lower frequency [100] = 15.74-21.6MHz [111] = 21.6 - 24.576 MHz
		SYSCLK_SEL																	Master clock sources selection 0=MCLK (default path) 1= 2 * MCLK (clock multiplier path) MCLKSEL 0x01[5:3] setting required.
		Default	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	**0x03FE**
3	CLK_DIVIDER	CLK_CODEC_SRC																	ADC clock and DAC clock source selection 1 = from MCLK 0 = from internal MCLK
		CLK_DAC_PL																	Invert DAC Clock Polarity in digital domain 1= Invert 0= No change
		CLK_ADC_PL																	Invert ADC Clock Polarity 1= Invert 0= No change
		CLK_ADC_SRC																	Scaling for ADC clock from CLK_CODEC_SRC 00 = 1 01 = 1/2 10 = 1/4 11 = 1/8
		CLK_DAC_SRC																	Scaling for DAC clock from CLK_CODEC_SRC 00 = 1 01 = 1/2 10 = 1/4 11 = 1/8

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
3	CLK_DIVIDER	MCLK_DIV																	Scaling for MCLK from SYSCLK_SEL Output 000: div by 1 001: div by 1 and inverted 010: div by 2 011: div by 3 100: div by 4 110: div by 6
		Default	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	**0x0050**
8		PDB_DAC																	DAC V_{REF} buffer power 0 = power-down 1=power-up
																			Reserved
		Default	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x4000**
F	INTERRUPT_MASK	APR_EMRGENCY_ SHTDWN1_INTP_MASK																	APR Emergency Shutdown Interrupt mask 1 = Mask the interrupt 0 = Unmask
		KEY_RELEASE_INTP_ MASK																	Key Release Interrupt mask 1 = Mask the interrupt 0 = Unmask
		KEY_INTP_MASK																	Key Pressed Interrupt mask 1 = Mask the interrupt 0 = Unmask
		MCLKDET_INTP_MASK																	Missing MCLK Detection Interrupt mask 1 = Mask the interrupt 0 = Unmask
		MIC_DET_INTP_MASK																	MIC Detection Interrupt mask 1 = Mask the interrupt 0 = Unmask
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
10	IRQ_STATUS	POWERUP																	Mirror 0x74[8], for use with polling 0 = Power down MICBIAS1 1 = Power on MICBIAS1
		KEYDET																	KEY DETECT Status Bit (unlatched)
		MICDET																	MIC Detect Status Bit (unlatched)
		APR_EMRG_SHTDWN																	APR Emergency Short Circuit Shutdown IRQ
		KEY_RELEASE_INT																	Key Release for Key Detection IRQ Status
		KEY_PRESS_INT																	Key Press for Key Detection IRQ Status
		MCLK_DET_INT																	Missing MCLK Detection IRQ Status
		MIC_DET_INT																	MIC Detection IRQ Status
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**Read Only**
11	INT_CLR_ KEY_STATUS	INT_CLR_KEY_STATUS																	Write Operation to Clear IRQ Status Write [15:0] to clear related IRQ_STATUS [15:0] Write 1s to bits that you want to clear
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**Read/Write**

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
12	INTERRUPT_DIS_CTRL (Write mode)	APR_EMRG_ SHTDWN _INT_DIS																	APR Emergency Short Circuit Shutdown Interrupt Disable Control 1 = Disable 0 = Enable
		KEY_INT_DIS																	Key Interrupt Disable Control 1 = Disable 0 = Enable
		MCLKDET_INT_DIS																	Missing MCLK Detection Interrupt Disable Control 1 = Disable 0 = Enable
		MIC_DET_INT_DIS																	MIC Detection/Headset Configuration interrupt disable control 1 = Disable 0 = Enable
		Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	**0xFFFF**
13	DMIC_CTRL	DMIC_DS																	DMIC Driving Strength 1 = High drive current; 0 = Low drive current
		DMIC_SLEW <2:0>																	DMIC Pin Slew Rate Selection
		CLK_DMIC_SRC																	DMIC Clock Speed Selection: 00 = ADC Clock 01 = ADC Clock / 2 10 = ADC Clock / 4 11 = ADC Clock / 8
		DMICEN																	Digital Microphone Mode Enable 1 = Enabled 0 = Disabled
		Default	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	**0x0F00**
1B	TDM_CTRL	TDM																	TDM Enable 1 = Enable 0 = Disable
		PCM_OFFSET_MODE_ CTRL																	PCM Offset Control in TDM 1 = Enable 0 = Disable
		ADCPHS0																	ADC audio channel data left-right ordering (I2S) or Channel 0 and Channel 1 (PCM) 0 = left ADC data in left phase of LRP 1 = left ADC data in right phase of LRP (left-right reversed)
		DACPHS0																	DAC channel audio data left-right ordering (I2S) or Channel 0 and Channel 1 (PCM) 0 = left DAC data in left phase of LRP 1 = left DAC data in right phase of LRP (left-right reversed)
		DAC_SEL																	DAC left channel source under TDM mode I2S: 000: from Slot 0 001: from Slot 1 010: from Slot 2 011: from Slot 3 100: Reserved 101: Reserved 110: Reserved 111: Reserved PCM: 000: from slot 0 001: from slot 1 010: from slot 2 011: from slot 3 100: from slot 4 101: from slot 5 110: from slot 6 111: from slot 7

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
1B	TDM_CTRL	ADC_TX_SEL																	ADC left channel source under TDM mode I2S: 000: from Slot 0 001: from Slot 1 010 : from Slot 2 011: from Slot 3 100: Reserved 101: Reserved 110: Reserved 111: Reserved PCMA: 000: from slot 0 001: from slot 1 010: from slot 2 011: from slot 3 100: from slot 4 101: from slot 5 110: from slot 6 111: from slot 7
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
1C	I2S_PCM_CTRL1	DACCM0																	DAC companding mode control 00 = Off (normal linear operation) 01 = Reserved 10 = U-law companding 11 = A-law companding
		ADCCM0																	ADC companding mode control 00 = Off (normal linear operation) 01 = Reserved 10 = U-law companding 11 = A-law companding
		ADDAP0																	DAC audio data input option to route directly from ADC data stream 0 = No pass through, normal operation 1 = ADC output data stream routed to DAC input data path
		CMB8_0																	8-bit word enable for companding mode of operation 0 = Normal operation (no companding) 1 = 8-bit operation for companding mode
		UA_OFFSET																	uLaw offset 0 = 1's complement 1 = 2's complement
		BCP0																	Bit clock phase inversion option for BCLK 0 = Normal phase 1 = Input logic sense inverted
		LRP0																	PCMA and PCMB left/right word order control 0 = Right Justified/Left Justified/I2S/PCMA mode 1 = PCMB Mode Enable: MSB is valid on 1st rising edge of BCLK after rising edge of FS
		WLEN0																	Port Word length (24-bits default) of audio data stream 00 = 16-bit word length 01 = 20-bit word length 10 = 24-bit word length 11 = 32-bit word length
		AIFMT0																	Port Audio interface data format 01 = Left justified 10 = Standard I2S format (Default) 11 = PCMA or PCMB audio data format option
		Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	**0x000A**

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
1D	I2S_PCM_CTRL2	I2S_TRI																	I2S tri state 0 = Normal mode 1 = Output high Z
		I2S_DRV																	I2S driving enable 0 = Normal mode 1 = Always out
		LRC_DIV																	LRC divide coefficient setting 00 = 1/256 01 = 1/128 10 = 1/64 11 = 1/32
		PCM_TS_EN0																	0 = Only PCM_A_MODE or PCM_B_MODE (STEREO Only) can be used when PCM Mode is selected 1 = Time slot function enable for PCM mode
		TRI0																	Without TDM mode 0 = Drive the full Clock of LSB 1 = Tri-State the 2nd half of LSB
		PCM8BIT0																	0 = Use **I2S_PCM_CTRL1.WEN0** to select Word Length 1 = PCM Select 8-bit word length
		PCM_TS_SEL																	Reserved to 0
		ADCDAT0_PE																	ADCDAT IO Pull Enable 1 = Enable 0 = Disable
		ADCDAT0_PS																	ADCDAT IO Pull Up/Down Enable 1 = Pull Up 0 = Pull Down
		ADCDAT0_OE																	0 = ADCDAT is not always out (when no data out, ADCOUT pin becomes high) 1 = ADCDAT always out
		MS0																	Master/Slave Mode Enable 0 = Slave Mode 1 = Master Mode
		BCLKDIV																	BCLK DIVIDE Setting from MCLK frequency 000 = 1 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 1/32
		Default	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	**0x8010**
1E	LEFT_TIME_SLOT	FS_ERR_CMP_SEL																	Triggers short frame sync signal if frame sync is less than 00 = 252 x MCLK_INT 01 = 253 x MCLK_INT 10 = 254 x MCLK_INT 11 = 255 x MCLK_INT
		DIS_FS_SHORT_DET																	Short Gram Sync detection logic Enable 0 = Enable 1 = Disable
		TSLOT_L0																	Left channel PCM time slot start value Or PCM TDM Offset Mode Slot start value
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
21	BIQ0_ COF1	BIQ0_A1_L																	Program ADC BIQ_A1 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
22	BIQ0_ COF2	BIQ0_A1_H																	Program ADC BIQ_A1 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
23	BIQ0_ COF3	BIQ0_A2_L																	Program ADC BIQ_A2 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
24	BIQ0_COF4	BIQ0_A2_H																	Program ADC BIQ_A2 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
25	BIQ0_ COF5	BIQ0_B0_L																	Program ADC BIQ_B0 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
26	BIQ0_ COF6	BIQ0_B0_H																	Program ADC BIQ_B0 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
27	BIQ0_ COF7	BIQ0_B1_L																	Program ADC BIQ_B1 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
28	BIQ0_COF8	BIQ0_B1_H																	Program ADC BIQ_B1 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
29	BIQ0_ COF9	BIQ0_B2_L																	Program ADC BIQ_B2 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
2A	BIQ0_COF10	BIQ0_EN																	BIQ ADC Path Enable 1 = Enable 0 = Disable
		BIQ0_B2_H																	Program ADC BIQ_B2 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
2B	ADC_RATE	ADC SRC																	In Non-DMIC Mode: 0 = Latch Analog data input to the Channel Filter In DMIC Mode: 0 = Left Channel in Rising Edge 1 = Left Channel in Falling Edge
		SMPL_RATE																	Generating 2.048MKHz based on SRs 000 = 48k SR(default) 001 = 32k SR 110 = 96k SR
		GAINCMP																	Reserved, always set to zero
		OSR_ADC_RATE																	ADC SINC Down selection 00 = Down 32 01 = Down 64 10 = Down 128 11 = Down 256
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	**0x0002**
2C	DAC_CTRL1	CICCLP_OFF																	**Recommended setting is 0**
		CIC_GAIN_ADJ																	For fine tuning the DAC output for glitch & noise, Please set 0x7 value for best performance
		OSR_DAC_RATE																	DAC oversample rate selection *000 = 64* 001 = 256 *010 = 128* 100 = 32
		Default	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	**0x0082**

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
2D	DAC_CTRL2	Reserved																	Reserved to 0
		SDMOD_DITHER																	Number of bits of dithering on SD modulator. Each level increments dithering by 1 bit 0000 = No dithering 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 0111 = 7 1000 = 8 1001 = 9 1010 = 10 1011 = 11 1100 = 12 1101 = 13 1110 = 14 1111 = 15
		Reserved																	Reserved to 0
		Reserved																	Reserved to 0
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
30	ADC_DGAIN_CTR	ADC_TO_DAC_ST0																	ADC to DAC CH0 Sidetone selection. Step size is 3dB 0000 = mute 0001 = -42dB ▼ 1110 = -3dB 1111 = 0dB
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
31	MUTE_CTRL																		Reserved
		DAC_SLOW_UM																	DAC Slow Soft Unmute Enable 1 = Enable (512 MCLK per step soft unmute) 0 = Disable (16 MCLK per step soft unmute)
		DAC_ZC_EN																	DAC Zero Crossing Enable 1 = Enable 0 = Disable
		AMUTE_EN																	Auto mute enable Generate null output to analog circuitry when 1024 consecutive zeros are detected. De-assert as soon as first non-zero sample is detected.
		AMUTE_CTRL																	Auto mute control 1 = DAC channels must have 1024 consecutive zero samples 0 = DAC channel must have 0 values for 1024 samples before AMUTE turns on
		SMUTE_EN																	Soft mute enable 1 = Gradually lower DAC volume to zero 0 = Gradually increase DAC volume to volume register setting
		ADC_ZC_EN																	ADC Zero Crossing Enable 1 = Enable 0 = Disable
		ADC_SMUTE_EN																	ADC Soft Mute Enable 1 = Enable 0 = Disable
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
34																			Reserved
		DGAIN_DAC																	DAC Volume control. Expressed as a gain or attenuation in 0.5db steps Note: Digital DAC input (I2S_DACIN) needs to meet the criteria: $Effective\ DAC\ input \leq 0\ dB$, where $Effective\ DAC\ input = DACIN[dBFS] + DAC_Vol[dB]$ Setting effective DAC input greater than 0dB is not recommended. 0xFF = +24dB 0xFE = +24.5dB ▼ 0xCD = 0dB ▼ 0x4B = -66dB 0x4A = Reserved ▼ 0x0F = Reserved 0x0E = Mute 0x00 = Mute
		Default	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1	**0xCFCF**
35	ADC_DGAIN_CTRL1																		Reserved
		DGAIN_ADC																	ADC Volume control. Expressed as a gain or attenuation in 0.5db steps 0xFF = +24dB 0xFE = +23.5dB ▼ 0xCF = 0dB ▼ 0x4B = -66dB 0x4A = Reserved ▼ 0x0F = Reserved 0x0E = Mute 0x00 = Mute
		Default	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1	**0xCFCF**
36	ADC_DRC_KNEE_IP12	DRC_ENA_ADC																	ADC channel DRC enable 1 = Enable 0 = Disable
		DRC_KNEE2_IP_ADC																	ADC DRC Knee point 2 setting, increments in -1dB steps 0x00 = 0dB 0x01 = -1dB ▼ 0x3E = -62dB 0x3F = -63dB
		DRC_SMTH_ENA_ADC																	1= ADC Smooth filter enable

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
36	ADC_DRC_KNEE_IP12	DRC_KNEE1_IP_ADC																	ADC DRC Knee point 1 setting, increments in -1dB steps 0x00 = 0dB 0x01 = -1dB ▼ 0x1E = -30dB 0x1F = -31dB
		Default	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1	0	**0x1486**
37	ADC_DRC_KNEE_IP34	DRC_KNEE4_IP_ADC																	ADC DRC Knee point 4 setting, increments in -1dB steps 0x00 = -35dB 0x01 = -36dB ▼ 0x3E = -97dB 0x3F = -98dB
		DRC_KNEE3_IP_ADC																	ADC DRC Knee point 3 setting, increments in -1dB steps 0x00 = -18dB 0x01 = -19dB ▼ 0x3E = -80dB 0x3F = -81dB
		Default	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	**0x0F12**
38	ADC_DRC_SLOPES	DRC_NG_SLP_ADC																	ADC DRC Noise Gate Slope 00 = 1:1 01 = 2:1 10 = 4:1 (default) 11 = 8:1
		DRC_EXP_SLP_ADC																	ADC DRC Expansion Slope 00 = 1:1 01 = 2:1 10 = 4:1 (default) 11 = Reserved
		DRC_CMP2_SLP_ADC																	ADC DRC Compressor Slope (lower region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = Reserved 111 = 1 (default)
		DRC_CMP1_SLP_ADC																	ADC DRC Compressor Slope (higher region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = Reserved 111 = 1 (default)
		DRC_LMT_SLP_ADC																	ADC DRC Limiter Slope 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101 = 1:32 110 = 1:64 111 = 1 (default)
		Default	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	**0x25FF**

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
39	ADC_DRC_ATKDCY	DRC_PK_COEF1_ADC																	ADC DRC Peak detection attack time Ts = 1/SMPL_RATE 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1xxx reserved
		DRC_PK_COEF2_ADC																	ADC DRC Peak detection release time Ts = 1/SMPL_RATE 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts 1xxx reserved
		DRC_ATK_ADC																	ADC DRC Attack time Ts = 1/SMPL_RATE 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1000 = 511*Ts 1001 = 1023*Ts 1010 = 2047*Ts 1011 = 4095*Ts 1100 = 8191*Ts
		DRC_DCY_ADC																	ADC DRC Decay time Ts = 1/SMPL_RATE 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 =4095*Ts 0111 = 8191*Ts 1000 = 16383*Ts 1001 = 32757*Ts 1010 = 65535*Ts
		Default	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	1	**0x3457**
3A	DAC_DRC_KNEE_IP12	DRC_ENA_DAC																	DAC channel DRC enable 1 = Enable. 0 = Disable
		DRC_KNEE2_IP_DAC																	DRC DAC Knee point 2 setting, increments in -1dB/step 0x00 = 0dB 0x01 = -1dB ▼ 0x3E = -62dB 0x3F = -63dB
		DRC_SMTH_ENA_DAC																	DRC DAC Smooth filter enable 1 = Enable. 0 = Disable
		DRC_KNEE1_IP_DAC																	DRC DAC Knee point 1 setting, increments in -1dB steps 0x00 = 0dB 0x01 = -1dB ▼ 0x1E = -30dB 0x1F = -31dB
		Default	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1	0	**0x1486**

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
3B	DAC_DRC_KNEE_IP34	DRC_KNEE4_IP_DAC																	DRC DAC Knee point 4 setting, increments in -1dB steps 0x00 = -35dB 0x01 = -36dB ▼ 0x3E = -97dB 0x3F = -98dB
		DRC_KNEE3_IP_DAC																	DRC DAC Knee point 3 setting, increments in -1dB steps 0x00 = -18dB 0x01 = -19dB ▼ 0x3E = -80dB 0x3F = -81dB
		Default	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	**0x0F12**
3C	DAC_DRC_SLOPES	DRC_NG_SLP_DAC																	DAC Noise Gate Slope 00 = 1:1 01 = 2:1 10 = 4:1 (default) 11 = 8:1
		DRC_EXP_SLP_DAC																	DAC DRC Expansion Slope 00 = 1:1 01 = 2:1 10 = 4:1 (default) 11 = 8:1
		DRC_CMP2_SLP_DAC																	DAC Compressor Slope (lower region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = Reserved 111 = 1 (default)
		DRC_CMP1_SLP_DAC																	DAC Compressor Slope (higher region) 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = Reserved 111 = 1 (default)
		DRC_LMT_SLP_DAC																	DAC Limiter Slope 000 = 0 001 = 1:2 (default) 010 = 1:4 011 = 1:8 100 = 1:16 101 = 1:32 110 = 1:64 111 = 1
		Default	0	0	1	0	0	1	0	1	1	1	1	1	1	0	0	1	**0x25F9**
3D	DAC_DRC_ATKDCY	DRC_PK_COEF1_DAC																	DAC Peak detection attack time Ts = 1/SMPL_RATE 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1xxx reserved
		DRC_PK_COEF2_DAC																	DAC Peak detection release time Ts = 1/SMPL_RATE 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts 1xxx reserved

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
3D	DAC_DRC_ATKDCY	DRC_ATK_DAC																	DAC Attack time Ts = 1/SMPL_RATE 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1000 = 511*Ts 1001 = 1023*Ts 1010 = 2047*Ts 1011 = 4095*Ts 1100 = 8191*Ts
		DRC_DCY_DAC																	DAC Decay time Ts = 1/SMPL_RATE 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts 1000 = 16383*Ts 1001 =32757*Ts 1010 = 65535*Ts
		Default	0	0	1	1	0	1	0	0	0	1	0	1	0	1	1	1	**0x3457**
41	BIQ1_ COF1	BIQ1_A1_L																	Program DAC BIQ_A1 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
42	BIQ1_ COF2	BIQ1_A1_H																	Program DAC BIQ_A1 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
43	BIQ1_ COF3	BIQ1_A2_L																	Program DAC BIQ_A2 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
44	BIQ1_COF4	BIQ1_A2_H																	Program DAC BIQ_A2 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
45	BIQ1_ COF5	BIQ1_B0_L																	Program DAC BIQ_B0 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
46	BIQ1_ COF6	BIQ1_B0_H																	Program DAC BIQ_B0 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
47	BIQ1_ COF7	BIQ1_B1_L																	Program DAC BIQ_B1 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
48	BIQ1_COF8	BIQ1_B1_H																	Program DAC BIQ_B1 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
49	BIQ1_ COF9	BIQ1_B2_L																	Program DAC BIQ_B2 parameter Bit[15:0]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
4A	BIQ1_COF10	BIQ1_EN																	BIQ DAC Path Enable 1 = Enable 0 = Disable
		BIQ1_B2_H																	Program DAC BIQ_B2 parameter Bit[18:16]
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
4C	IMM_MODE_CTRL	Reserved																	Reserved to zero
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**

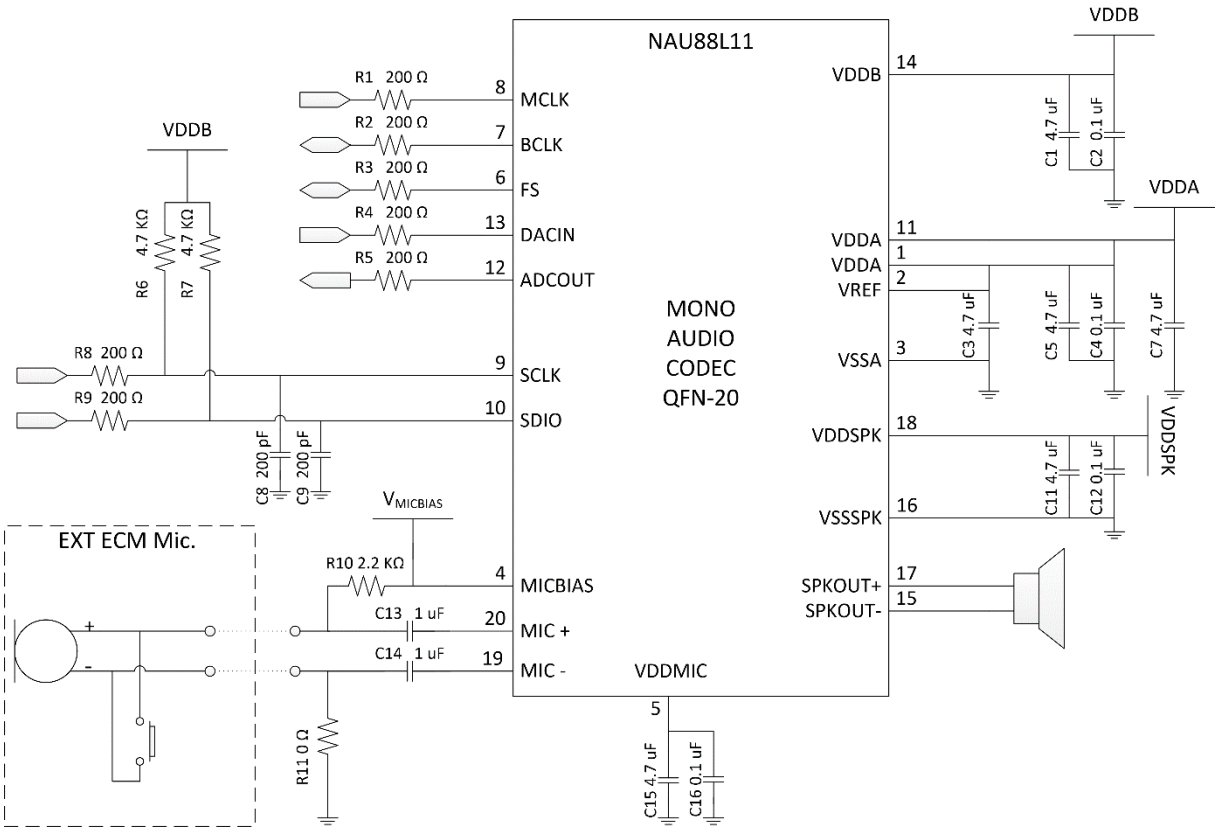
REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
51	VCM_BUF	VCM_GAIN_CTRL <3:0>																	VCM buffer gain control; default = 1000 for 1.65V
		PDB_VCMBUF																	VCM buffer enable control 0 = power down 1 = power up
		VOUT_PRECHG_DISABLE																	Output VCM pre-charge 0 = Enable 1= Disable (default)
		PRECHG_IB_CTRL <1:0>																	VCM pre-charge tail R-bias control Default = 00 for R =75k ; decrement 5K/step
		Default	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	**0x0210**
52	SPK_DRV	MUTE_SPK																	Mute speaker driver 0= Disable 1= Enable
		MDRV_IB_SEL <1:0>																	Class AB amplifier Bias Current 01 = 0.5uA (00 = no current) 10 = 1.0uA (default) 11 = 1.5uA
		PUP_MAIN_DRV																	Power Up main speaker driver 1 = Power up 0 = Power down
		SPK_GAIN_CNTRL																	SPK 4-bit gain control from 0 to 5.6 dB with a gain resolution of ~ 0.4 dB per step. 0000 = 0 0001 = 0.4dB ▼ 1110 = 5.2dB 1111 = 5.6dB
		Default	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	**0x0080**
53	SPG_AMP_OFFSETDEC	CAL_SGN																	Class AB offset trim sign
		EN_CAL																	Enable Class AB amplifier offset trim
		OFFSET_CAL0																	Class AB amplifier input 3bit offset trim
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
55	MISC_CTRL	RAM_TEST_START																	Ram Test Control 1 = Enable 0 = Disable
		D2A_LOOP																	1: Use DAC Filter Input as ADC decimation filter output
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
58	I2C_DEVICE_ID	I2C_DEVICE_ID[14:8]																	I2C Device ID read in [0x1B]
		Silicon Revision ID																	Silicon revision bits
		Default	X	0	0	1	1	0	1	1	1	1	X	X	X	X	X	X	**Read Only**
59	SARDOUT_RAM_ STATUS	RATM_TEST_FINISH																	1 = Test is finished 0 = Test is not complete
		RAM_TEST_FAIL																	1 = Test is failed 0 = Test is passed
		ANALOG_MUTE																	Analog mute status flag for DAC auto mute Asserted when 1024 consecutive zeros samples are detected
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**Read Only**

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
66	BIAS_ADJ	MUTE																	Mute PGA 1 = Enable 0 = Disable
		TESTDAC																	DAC test
		Reserved																	Reserved to 0
		VMIDEN																	VMID enable 1 = Enable 0 = Disable
		VMIDSEL																	VMID tie-off selection options 00 = Open (default) 01 = 25k Ohm 10 = 125k Ohm 11 = 2.5k Ohm
		Reserved																	Reserved
		Reserved																	Reserved
		BIASADJ																	PGA Master bias current power options 00 = normal operation (default) 01 = 9% reduced bias current from default 10 = 17% reduced bias current from default 11 = 11% increased bias current from default
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
69	SPARE_ANALOG1	PULL_SPKR_DWN																	Pull down Class AB outputs to GND; 0 = Disable 1 = Enable
		PRECHG_CURR_BOOST																	Increase precharge slew rate 2x for Cout=4.7uF 0 = Disable 1= Enable
		PRECHG_TURBO_BOOST																	Increase precharge slew rate 4x for Cout=4.7uF 0 = Disable 1 = Enable
		THD_BOOST																	Signal to boost THD. 0 = Disable (default) 1 = Enable
		TESTDACIN<1:0>																	DAC test signal 00 = GND 01 = HIGH 10 = LOW 11 = GND
		CAP<1:0>																	DAC Reference Decoupling Capacitor
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
6B		MUTE_N																	MUTE MICN Input to PGA when set to '1'
		MUTE_P																	MUTE MICP Input to PGA when set to '1'
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
71	ANALOG_ADC_1	Reserved																	Reserved
		TRIM_MIC<2:0>																	Mic detect threshold Trim threshold resolution = 10uA/bit default = 000, Imic_det = 35uA
		TRIM_BUTTON<2:0>																	Key detect threshold Trim threshold resolution = 100uA/bit default = 000, Ikey_det = 500uA
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
72	ANALOG_ADC_2	Reserved																	Reserved

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
72	ANALOG_ADC_2	Reserved																	Reserved
		ADC_UP																	PGA bias current increase enable for driving the ADC at high sample rates 1 = Enable 0 = Disable
		BIAS																	Change bias currents in ADC 00 = Nominal 01 = Double 10 = Half 11 = Quarter
		VREFSEL																	ADC Reference voltage 00 = 1.8V 01 = 1.54V 10 = 1.65V 11 = 1.77V
		Reserved																	Reserved '0'
		PDNOT																	ADC(analog path): 0=power down; 1 = Power on
		Default	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	**0x0100**
73	DAC	DAC_EN																	DAC enable (analog path) 1 = Enable 0 = Disable
		CLK_DAC_EN																	DAC CLOCK enable (analog path) 1 = Enable 0 = Disable
		FC_CTR																	DAC Smoothing Filter on Output enable 1 = Enable 0 = Disable
		CLK_DAC_DELAY																	DAC clock delay setting (analog path)
		DACVREFSEL<1:0>																	DAC Reference voltage 00 = 1.8V 01 = 1.56V 10 =1.61V(default) 11 = 1.75V
		Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	**0x0008**
74	MIC_BIAS	POWERUP																	(Mirror in register 10) 0 = Power down MICBIAS1 1 = Power on MICBIAS1
		MB_LPMODE<1:0>																	00 = Low noise mode (default) 01 = Low power mode
		MICBIASLVL1																	Set output level for MICBIAS1 000 = V_{DDA} 001 = 1.1 x V_{DDA} 010 = 1.2 x V_{DDA} 011 = 1.3 x V_{DDA} 100 = 1.4 x V_{DDA} 101 = 1.53 x V_{DDA}
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	**0x0004**
76	BOOST	CLR_APR_EMRGENCY_SHTDWN																	Clear Headset short circuit shut down IRQ 1 = Reset (momentary) 0 = Default
		STG2_SEL																	PGA in class A mode of operation enables instead of class AB 1 = Enable; 0 = Disable (default)
		PDVMDFST																	VMID Pre-charge disable 1 = Disable 0 = Enable
		BIASEN																	Global Analog Bias enable 1 = Enable 0 = Disable

REG	Function	Name	Bit [15..12]				Bit [11..8]				Bit [7..4]				Bit [3..0]				Description
76	BOOST	DISCHRG																	Charges inputs to VREF based on ACDC_CTRL 1 = Enable 0 = Disable
		RST_SHRT_IRQ																	Reset the IRQ short-det register after 100ms
		DISABLE_SHRT_DET																	Disable Automatic short-circuit detection 1 = disable short circuit detection (default) 0 = enable short circuit detection
		Default	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	**0x40**
77	FEPGA	ACDC_CTRL																	DC state control for Input pins. Action takes effect when DISCHRG=1 ACDC_CTRL[0] charges MICP to VREF ACDC_CTRL[1] charges MICN to VREF 1 = Enable 0 = Disable
		CMLCK_ADJ																	PGA Common Mode Threshold lock adjust. Recommended to leave this as default.
		IB_LOOP_CTR																	PGA: Current Trim Recommended to leave this as default.
		IBCTR_CODE																	PGA: Current Trim Recommended to leave this as default.
		PGA_MODE																	PGA mode selection; MODE[0] = Anti-aliasing filter adjust MODE[1] = Disconnects MICP & MICN MODE[2] = No function MODE[3] = Shorts the inputs and terminates with 12kOhm differentially 1 = Enable 0 = Disable
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
7E	PGA_GAIN	PGA_GAIN																	PGA gain, increments in 1dB steps 000000 = -1dB 000001 = 0dB ▼ 100100 = 35dB 100101 = 36dB
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
7F	POWER_UP_CONTROL	PUPL																	PUP - Power Up PGA 1 = Enable 0 = Disable
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
82	GENERAL_STATUS																		Reserved
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**Read Only**

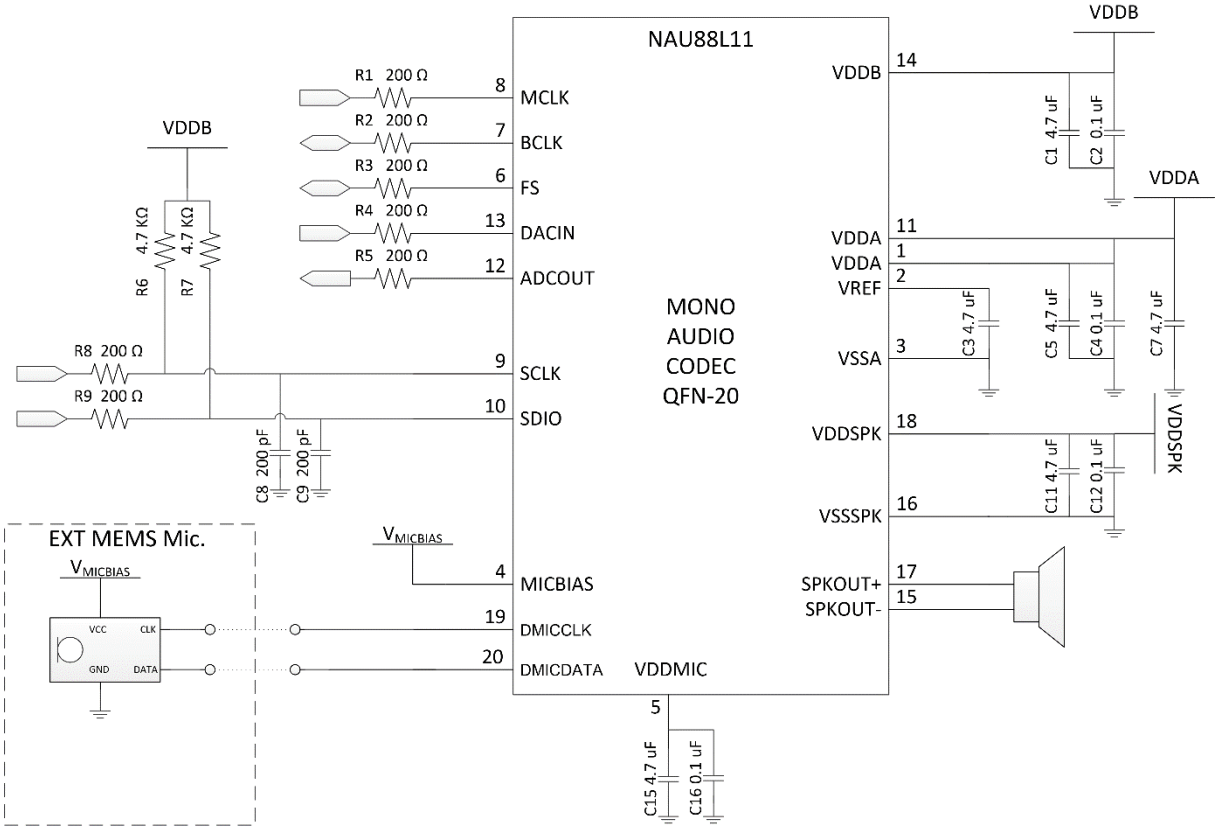
10. Typical Application Diagram with Analog Microphone



Notes:

1. All non-polar capacitors are assumed to be low ESR type parts, such as with MLC construction or similar. If capacitors are not low ESR,
   additional 0.1uF and/or 0.01uF capacitors may be necessary in parallel with the bulk 4.7uF capacitors on the supply rails. (C1, C3, C5, C7, C11, 4.7uF must be added. Optional C2, C4, C12 depends on Low ESR Cap used.)
2. Unused MIC input pins should be left as no-connection.
3. Damping Resistor R1~R5, the resistance may vary by different PCB.
4. I2C Low pass filter cut-off frequency should be 8MHz to 33MHz
5. For ECM Microphone type, MIC- should be routed to a quiet ground reference near the VREF capacitor. Customer may omit the 0ohm placed in schematic, but should not route this pin through Thermal pad, but route directly to the VREF Cap.
6. VDDA on Pin 11 must have a separate capacitor to ground. (C7 must be added)

10.1 Typical Application Diagram with Digital Microphone

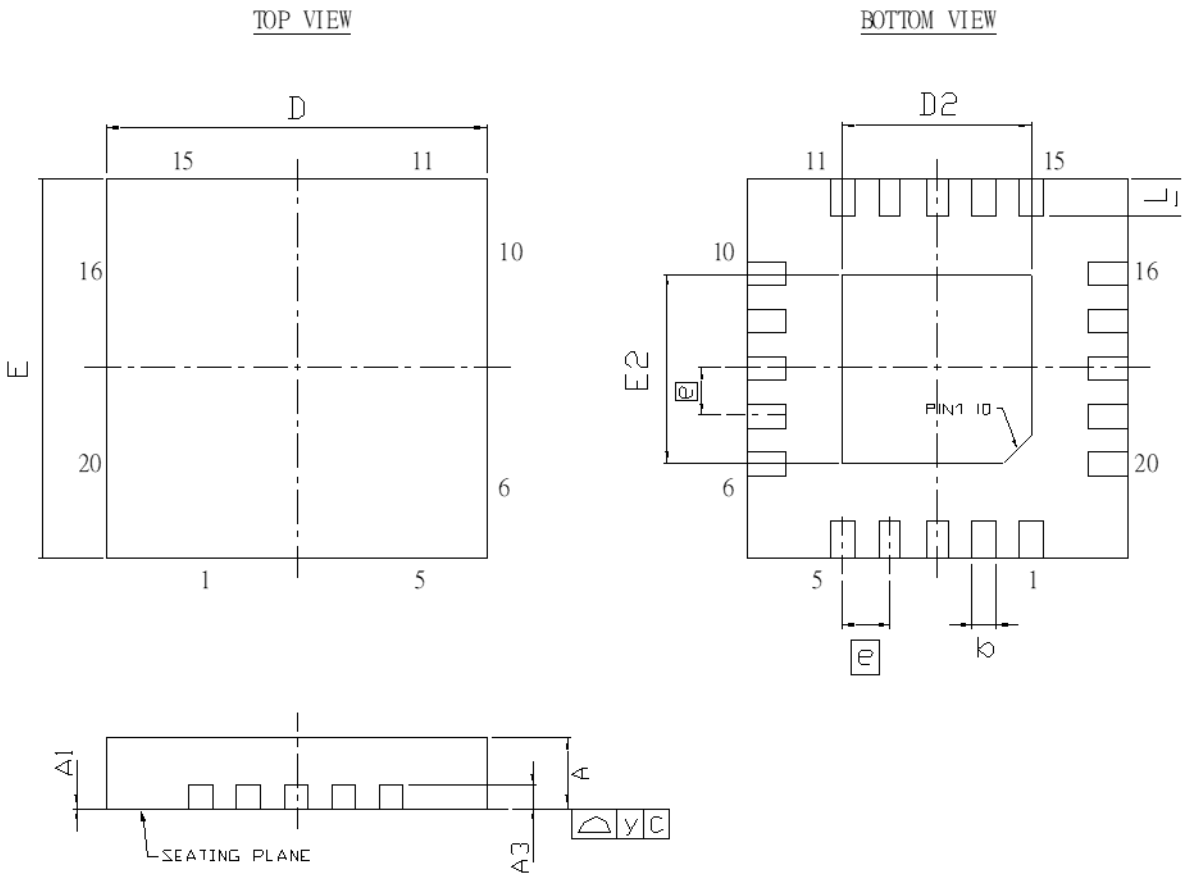


Notes:

1. All non-polar capacitors are assumed to be low ESR type parts, such as with MLC construction or similar. If capacitors are not low ESR,
   additional 0.1uF and/or 0.01uF capacitors may be necessary in parallel with the bulk 4.7uF capacitors on the supply rails. (C1, C3, C5, C7, C11, 4.7uF must be added. Optional C2, C4, C12 depends on Low ESR Cap used.)
2. Digital Microphone power should be connected to MICBIAS, and set same voltage as VDDA
3. Damping Resistor R1~R5, the resistance may vary by different PCB.
4. I2C Low pass filter cut-off frequency should be 8MHz to 33MHz
5. VDDA on Pin 11 must have a separate capacitor to ground. (C7 must be added)

11. Package Information

20-lead plastic QFN20; 4X4mm2, 0.5mm lead pitch



Controlling Dimension :Millimeters

SYMBOL	DIMENSION (MM)			DIMENSION (Inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.02756	0.02953	0.03150
A1	0	0.02	0.05	0	0.0079	0.00197
A3	0.203 REF			0.0079 REF		
b	0.18	0.25	0.30	0.00709	0.00984	0.01181
D	3.90	4.00	4.10	0.1535	0.1575	0.1614
D2	1.90	2.00	2.10	0.0748	0.0787	0.0827
E	3.90	4.00	4.10	0.1535	0.1575	0.1614
E2	1.90	2.00	2.10	0.0748	0.0787	0.0827
e	0.50 BSC			0.01969 BSC		
L	0.30	0.40	0.50	0.01181	0.01574	0.01969
y	0.08			0.00315		

Note.D2,E2 by die size difference .

12. Ordering Information

Part Number	Dimension	Package	Package Material
NAU88L11YG	4x4 mm	QFN-20	Green

NAU88L11 _ _

Package Material:

G = Pb-free Package

Package Type:

Y = 20-Pin QFN Package

13. Appendix

13.1 MCLK/FS Table: Group 1 MCLK_INT/FS ratio of 256

MCLK (MHz)	FS (KHz)	SYSCLK_SEL REG0x1[0]	MCLKSEL REG0x1[5:3]	MCLK_DIV REG0x3[2:0]	MCLK_INT (MHz)
2.048	8	0	-	1	2.048
4.096	16	0	-	1	4.096
6.144	24	0	-	1	6.144
8.192	32	0	-	1	8.192
11.2896	44.1	0	-	1	11.2896
12.288	48	0	-	1	12.288
22.5792	88.2	0	-	1	22.5792
24.576	96	0	-	1	24.576
4.096	8	0	-	2	2.048
8.192	16	0	-	2	4.096
12.288	24	0	-	2	6.144
16.384	32	0	-	2	8.192
22.5792	44.1	0	-	2	11.2896
24.576	48	0	-	2	12.288
6.144	8	0	-	3	2.048
12.288	16	0	-	3	4.096
18.432	24	0	-	3	6.144
24.576	32	0	-	3	8.192
8.192	8	0	-	4	2.048
16.384	16	0	-	4	4.096
24.576	24	0	-	4	6.144
12.288	8	0	-	6	2.048
24.576	16	0	-	6	4.096
2.048	16	1	b'000	1	4.096
3.072	24	1	b'000	1	6.144
4.096	32	1	b'000	1	8.192
5.6448	44.1	1	b'000	1	11.2896
6.144	48	1	b'000	1	12.288
11.2896	88.2	1	b'000	1	22.5792
12.288	96	1	b'000	1	24.576
2.048	8	1	b'000	2	2.048
4.096	16	1	b'000	2	4.096
6.144	24	1	b'000	2	6.144
8.192	32	1	b'000	2	8.192
11.2896	44.1	1	b'000	2	11.2896
12.288	48	1	b'000	2	12.288
22.5792	88.2	1	b'111	2	22.5792

MCLK (MHz)	FS (KHz)	SYSCLK_SEL REG0x1[0]	MCLKSEL REG0x1[5:3]	MCLK_DIV REG0x3[2:0]	MCLK_INT (MHz)
24.576	96	1	b'111	2	24.576
3.072	8	1	b'000	3	2.048
6.144	16	1	b'000	3	4.096
9.216	24	1	b'000	3	6.144
12.288	32	1	b'000	3	8.192
16.9344	44.1	1	b'100	3	11.2896
18.432	48	1	b'100	3	12.288
4.096	8	1	b'000	4	2.048
8.192	16	1	b'000	4	4.096
12.288	24	1	b'000	4	6.144
16.384	32	1	b'100	4	8.192
22.5792	44.1	1	b'111	4	11.2896
24.576	48	1	b'111	4	12.288
6.144	8	1	b'000	6	2.048
12.288	16	1	b'000	6	4.096
18.432	24	1	b'100	6	6.144
24.576	32	1	b'111	6	8.192

13.2 MCLK/FS Table: Group 1 MCLK_INT/FS ratio of 400

MCLK (MHz)	FS (KHz)	SYSCLK_SEL REG0x1[0]	MCLKSEL REG0x1[5:3]	MCLK_DIV REG0x3[2:0]	MCLK_INT (MHz)
3.2	8	0	-	1	3.2
6.4	16	0	-	1	6.4
9.6	24	0	-	1	9.6
12.8	32	0	-	1	12.8
17.64	44.1	0	-	1	17.64
19.2	48	0	-	1	19.2
6.4	8	0	-	2	3.2
12.8	16	0	-	2	6.4
19.2	24	0	-	2	9.6
9.6	8	0	-	3	3.2
19.2	16	0	-	3	6.4
12.8	8	0	-	4	3.2
19.2	8	0	-	6	3.2
3.2	16	1	b'000	1	6.4
4.8	24	1	b'000	1	9.6
6.4	32	1	b'000	1	12.8
8.82	44.1	1	b'000	1	17.64

9.6	48	1	b'000	1	19.2
3.2	8	1	b'000	2	3.2
6.4	16	1	b'000	2	6.4
9.6	24	1	b'000	2	9.6
12.8	32	1	b'000	2	12.8
17.64	44.1	1	b'100	2	17.64
19.2	48	1	b'100	2	19.2
4.8	8	1	b'000	3	3.2
9.6	16	1	b'000	3	6.4
14.4	24	1	b'000	3	9.6
19.2	32	1	b'100	3	12.8
6.4	8	1	b'000	4	3.2
12.8	16	1	b'000	4	6.4
19.2	24	1	b'100	4	9.6
9.6	8	1	b'000	6	3.2
19.2	16	1	b'100	6	6.4

13.3 MCLK/FS Table: Group 1 MCLK_INT/FS ratio of 500

MCLK (MHz)	FS (KHz)	SYSCLK_SEL REG0x1[0]	MCLKSEL REG0x1[5:3]	MCLK_DIV REG0x3[2:0]	MCLK_INT (MHz)
4	8	0	-	1	4
8	16	0	-	1	8
12	24	0	-	1	12
16	32	0	-	1	16
22.05	44.1	0	-	1	22.05
24	48	0	-	1	24
4	16	1	b'000	1	8
6	24	1	b'000	1	12
8	32	1	b'000	1	16
11.025	44.1	1	b'000	1	22.05
12	48	1	b'000	1	24

14. Revision History

Version			DESCRIPTION
#	Date	Page(s)	
1.4	Feb 19, 2021	All	Initial released version
1.5	Mar 3, 2021	2, 37,38	Fix Type Error

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