Data Sheet

ACPL-K34T

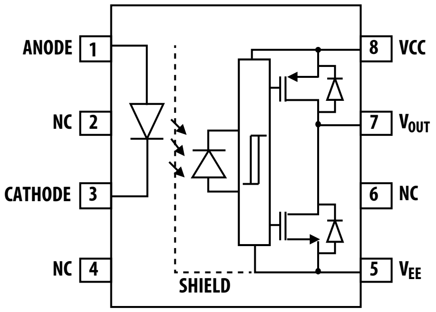
Automotive 2.5A Peak High Output Current MOSFET Gate Drive Optocoupler with Rail-to-Rail Output Voltage in Stretched SO-8 Package

Overview

The Broadcom® ACPL-K34T 2.5A Automotive R²Coupler Gate Drive Optocoupler contains an AlGaAs LED, which is optically coupled to an integrated circuit with a power output stage. The ACPL-K34T features fast propagation delay and tight timing skew, so it is ideally designed for driving power MOSFETs used in AC-DC and DC-DC converters. The high operating voltage range of the output stage provides the drive voltages required by gate-controlled devices. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct driving power MOSFETs at high frequency for high-efficiency conversion.

Broadcom R²Coupler isolation products provide reinforced insulation and reliability that deliver safe signal isolation critical in automotive and high-temperature industrial applications.

Figure 1: ACPL-K34T Functional Diagram



LED	$V_{CC} - V_{EE}$	V_{OUT}
OFF	0 to 20V	LOW
ON	<VUVLO–	LOW
ON	>VUVLO+	HIGH

Features

- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive temperature range: –40°C to +125°C
- Peak output current: 2.0A min.
- Rail-to-rail output voltage
- Propagation delay: 110 ns max.
- Dead time distortion: +50 ns/–40 ns
- LED current input drive with hysteresis
- Common mode rejection (CMR): 50 kV/µs min. at V_{CM} = 1500V
- Low supply current allow bootstrap half-bridge topology: I_{CC} = 3.9 mA max.
- Under-voltage lockout (UVLO) protection with hysteresis for power MOSFET
- Wide operating V_{CC} range: 10V to 20V
- Safety approvals:
  - UL recognized 5000 V_{RMS} for 1 minute
  - CSA
  - IEC/EN/DIN EN 60747-5-5 V_{IORM} = 1140 V_{PEAK}

Applications

- Hybrid power train DC/DC converter
- EV/PHEV charger
- Automotive isolated MOSFET gate drive
- AC and brushless DC motor drives

CAUTION! Take normal static precautions in the handling and assembly of this component to prevent damage, degradation, or both that might be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

Ordering Information

Part Number	Option (RoHS Compliant)	Package	Surface Mount	Tape and Reel	UL 5000 V_{RMS} / 1 Minute Rating	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-K34T	-000E	Stretched SO-8	X		X		80 per tube
	-060E		X		X	X	80 per tube
	-500E		X	X	X		1000 per reel
	-560E		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

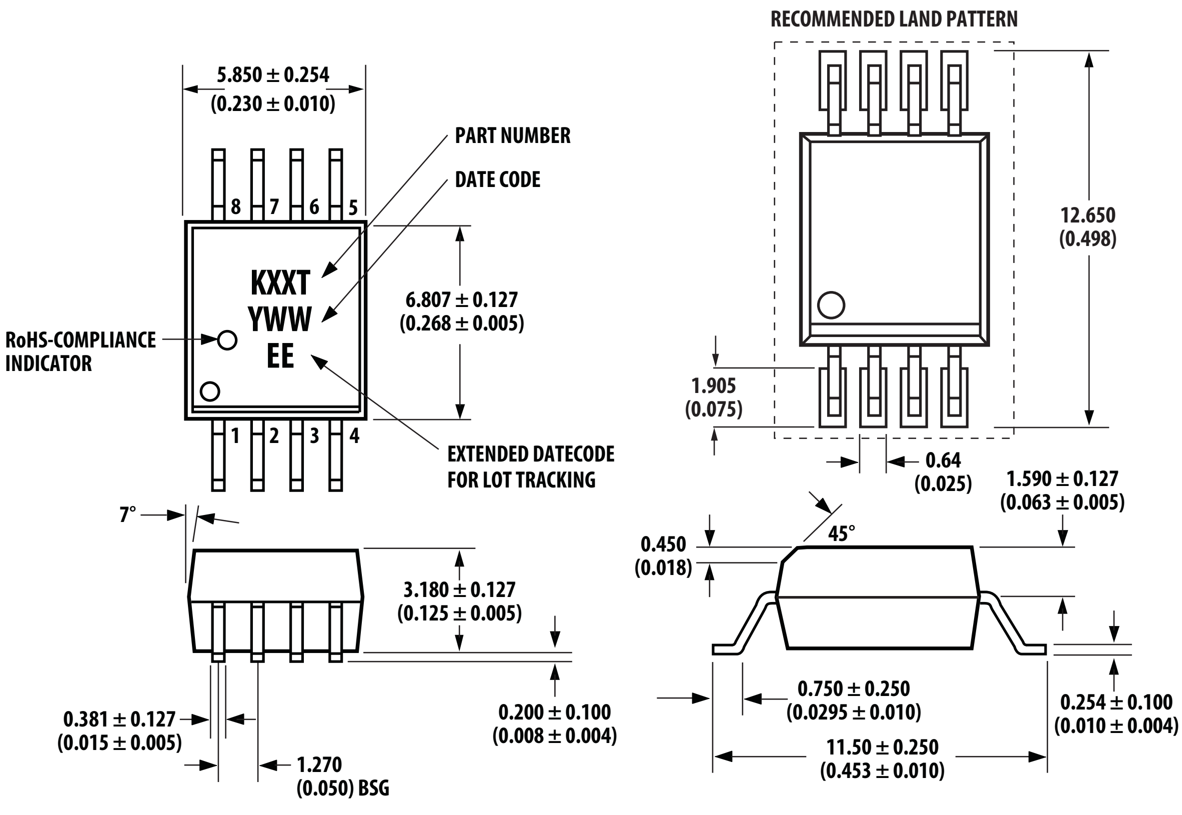
Example:

ACPL-K34T-560E to order product of SSO-8 surface-mount package in tape-and-reel packaging with IEC/EN/DIN EN 60747-5-5 safety approval in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Package Outline Drawings (Stretched SO-8)

Figure 2: ACPL-K34T Stretched SO-8 Package Outline Drawing



NOTE:

- Dimensions are in millimeters (inches).
- Lead coplanarity = 0.1 mm (0.004 inches).
- Floating lead protrusion = 0.25 mm (10 mils) maximum.

Recommended PB-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

NOTE: Non-halide flux should be used.

Regulatory Information

The ACPL-K34T is approved by the following organizations:

UL	UL 1577, component recognition program up to V_{ISO} = 5 kV_{RMS}.
CSA	CSA Component Acceptance Notice #5.
IEC/EN/DIN EN 60747-5-5	IEC 60747-5-5 EN 60747-5-5 DIN EN 60747-5-5

IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics (Option 060 and 560 Only)

Description	Symbol	Option 060 and 560	Unit
Insulation Classification per DIN VDE 0110/1.89, Table 1 For Rated Mains Voltage ≤ 600 V_{RMS} For Rated Mains Voltage ≤ 1000 V_{RMS}		 I – IV I – III	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1140	V_{PEAK}
Input to Output Test Voltage, Method b V_{IORM} × 1.875 = V_{PR}, 100% Production Test with t_m = 1 second, Partial Discharge < 5 pC	V_{PR}	2137	V_{PEAK}
Input to Output Test Voltage, Method a V_{IORM} × 1.6 = V_{PR}, Type and Sample Test, t_m = 10 seconds, Partial Discharge < 5 pC	V_{PR}	1824	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 seconds)	V_{IOTM}	8000	V_{PEAK}
Safety-Limiting Values – Maximum values allowed in the event of a failure. See Figure 6. Case Temperature Input Current Output Power	 T_S $I_{S,INPUT}$ $P_{S,OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	> 10^9	Ω

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Unit	Conditions
Minimum External Air Gap (Clearance)	L(101)	8	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight-line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1.
Isolation Group (DIN VDE0109)	IIIa			Material Group (DIN VDE 0109).

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	–55	150	°C	
Operating Temperature	T_A	–40	125	°C	
IC Junction Temperature	T_J	—	150	°C	a
Average Input Current	$I_{F(AVG)}$	—	20	mA	
Peak Input Current (50% duty cycle, < 1 ms pulse width)	$I_{F(PEAK)}$	—	40	mA	
Peak Transient Input Current (<1 µs pulse width, 300 pps)	$I_{F(TRAN)}$	—	1	A	
Reverse Input Voltage	V_R	—	6	V	
High Peak Output Current	$I_{OH(PEAK)}$	—	2.5	A	b
Low Peak Output Current	$I_{OL(PEAK)}$	—	2.5	A	b
Total Output Supply Voltage	$(V_{CC} – V_{EE})$	0	25	V	
Output Voltage	$V_{O(PEAK)}$	–0.5	V_{CC}	V	
Output IC Power Dissipation	P_O	—	500	mW	c
Total Power Dissipation	P_T	—	550	mW	a

a. Total power dissipation is derated linearly above 110°C free-air temperature at a rate of 13 mW/°C. The maximum LED and IC junction temperature should not exceed 150°C

b. Maximum pulse width = 100 ns. Duty cycle = 2%.

c. Derate linearly above 110°C free-air temperature at a rate of 13 mW/°C. See Figure 3.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Operating Temperature	T_A	–40	125	°C	
Output Supply Voltage	$(V_{CC} – V_{EE})$	10	20	V	
Input Current (ON)	$I_{F(ON)}$	7	13	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	–5.5	0.8	V	

Electrical Specifications

Unless otherwise specified, all minimum and maximum specifications are at recommended operating conditions. All typical values at T_A = 25°C, $V_{CC} – V_{EE}$ = 10V, V_{EE} = Ground.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
High Level Peak Output Current	I_{OH}	—	–3.5	–2.0	A	$V_{CC} – V_O$ = 10V	4	
Low Level Peak Output Current	I_{OL}	2.0	4.4	—	A	$V_O – V_{EE}$ = 10V	5	
High Output Transistor RDS(ON)	$R_{DS,OH}$	—	2.2	4.0	Ω	I_{OH} = –2.0A		a
Low Output Transistor RDS(ON)	$R_{DS,OL}$	—	1.0	2.0	Ω	I_{OL} = 2.0A		a
High Level Output Voltage	V_{OH}	V_{CC} – 0.4	V_{CC} – 0.2	—	V	I_F = 10 mA, I_O = –100 mA		b, c
Low Level Output Voltage	V_{OL}	—	0.1	0.25	V	I_O = 100 mA		
High Level Supply Current	I_{CCH}	—	2.5	3.9	mA	I_F = 10 mA	6	
Low Level Supply Current	I_{CCL}	—	2.5	3.9	mA	V_F = 0V	7	
Threshold Input Current Low to High	I_{FLH}	—	1.5	4.9	mA	V_O > 5V	8	
Threshold Input Voltage High to Low	V_{FHL}	0.8	—	—	V			
Input Forward Voltage	V_F	1.25	1.5	1.85	V	I_F = 10 mA	8	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$	—	–1.5	—	mV/°C			
Input Reverse Breakdown Voltage	BV_R	6	—	—	V	I_R = 100 µA		
Input Capacitance	C_{IN}	—	90	—	pF	f = 1 MHz, V_F = 0V		
UVLO Threshold	V_{UVLO+}	8.1	8.6	9.1	V	V_O > 5 V, I_F = 10 mA	9	
	$V_{UVLO–}$	7.1	7.6	8.1			9	
UVLO Hysteresis	$UVLO_{HYS}$	0.5	1.0	—	V			

a. Output is source at –2.0A or 2.0A with a maximum pulse width of 10 µs.

b. In this test, V_{OH} is measured with a DC load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.

c. Maximum pulse width = 1 ms.

Switching Specifications

Unless otherwise specified, all minimum and maximum specifications are at recommended operating conditions. All typical values at T_A = 25°C, $V_{CC} - V_{EE}$ = 10V, V_{EE} = Ground.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	30	60	110	ns	V_{CC} = 10V R_G = 4.7Ω, C_L = 10 nF, f = 200 kHz, Duty Cycle = 50% V_{in} = 4.5V – 5.5V, R_{in} = 350Ω	10, 13, 15	a
Propagation Delay Time to Low Output Level	t_{PHL}	30	60	110	ns		11, 13, 15	
Pulse Width Distortion ($t_{PHL} - t_{PLH}$)	PWD	–40	0	40	ns		12	b
Dead Time Distortion Caused by Any Two Parts ($t_{PLH} - t_{PHL}$)	DTD	–40	—	50	ns			c
Rise Time	t_R	—	10	30	ns	V_{CC} = 10V, C_L = 1 nF, f = 200 kHz, Duty Cycle = 50% V_{in} = 4.5V to 5.5V, R_{in} = 350Ω	14, 15	
Fall Time	t_F	—	10	30	ns			
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	50	>75	—	kV/µs	T_A = 25°C, V_{CC} = 20V, V_{CM} = 1500V, with split resistors	16	d, e
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	50	>75	—	kV/µs			d, f

a. This load condition approximates the gate load of a 600V/50A power MOSFET.

b. Pulse width distortion (PWD) is defined as $t_{PHL} - t_{PLH}$ for any given device.

c. Dead time distortion (DTD) is defined as $t_{PLH} - t_{PHL}$ between any two parts under the same test condition. A negative DTD reduces original system dead time, while a positive DTD increases original system dead time.

d. Pin 2 and pin 4 must be connected to LED common.

e. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output will remain in the high state (that is, V_O > 10V).

f. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to ensure that the output will remain in a low state (that is, V_O < 1.0V).

Package Characteristics

Unless otherwise specified, all minimum and maximum specifications are at recommended operating conditions. All typical values at $T_A = 25°C$.

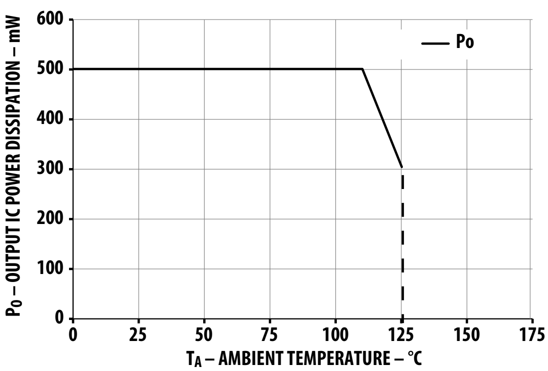
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Input-Output Momentary Withstand Voltage[a]	V_{ISO}	5000	—	—	V_{RMS}	RH < 50%, t = 1 min. $T_A = 25°C$	b, c
Input-Output Resistance	R_{I-O}	—	10^{14}	—	Ω	$V_{I-O} = 500\ V_{DC}$	c
Input-Output Capacitance	C_{I-O}	—	0.6	—	pF	f = 1 MHz	

a. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Broadcom Application Note 1074, *Optocoupler Input-Output Endurance Voltage*.

b. In accordance with UL1577, each optocoupler is proof-tested by applying an insulation test voltage ≥ 6000 V_{RMS} for 1 second.

c. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.

Figure 3: Output IC Power Dissipation Derating Chart



Typical Performance Plots

Figure 4: I_{OH} vs. (V_{CC} – V_{OH})

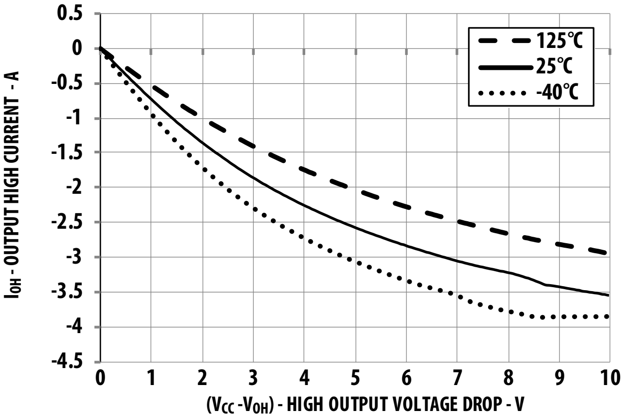


Figure 5: I_{OL} vs. V_{OL}

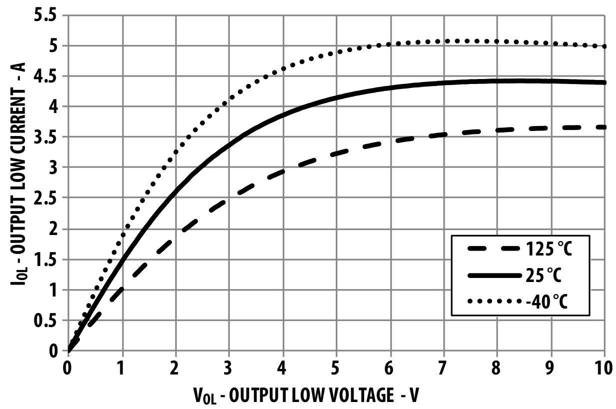


Figure 6: I_{CCH} vs. Temperature

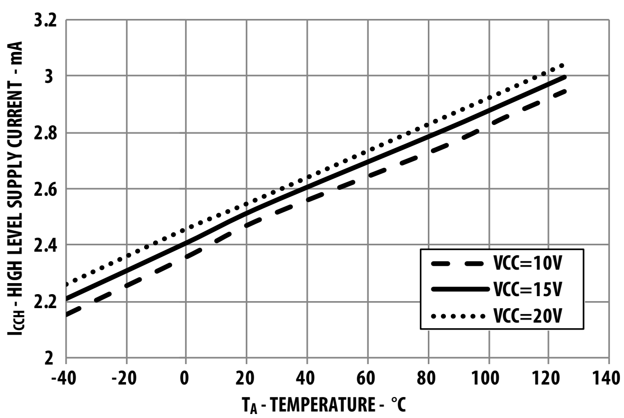


Figure 7: I_{CCL} vs. Temperature

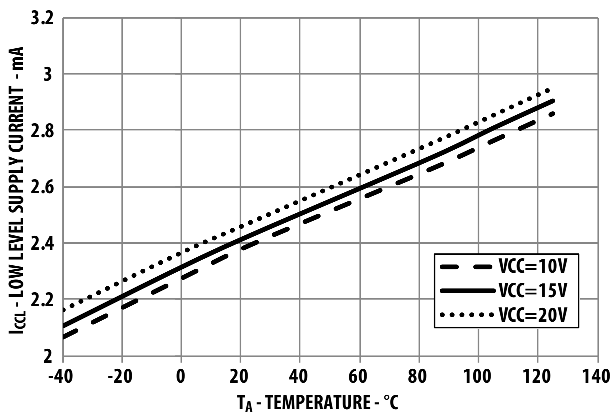


Figure 8: V_F vs. Temperature

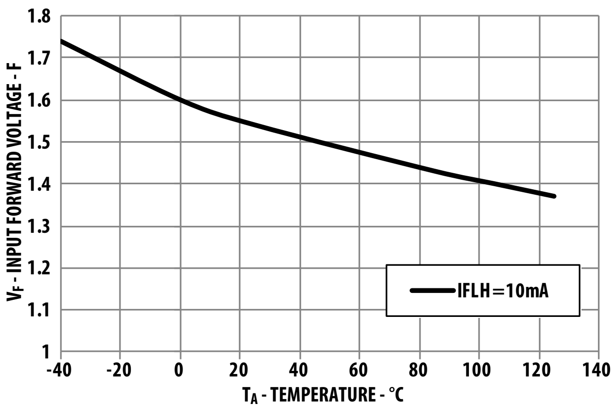


Figure 9: I_F vs. V_F

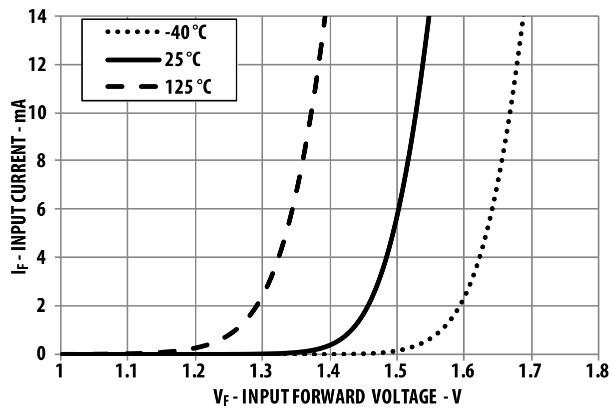


Figure 10: t_{PLH} vs. Temperature

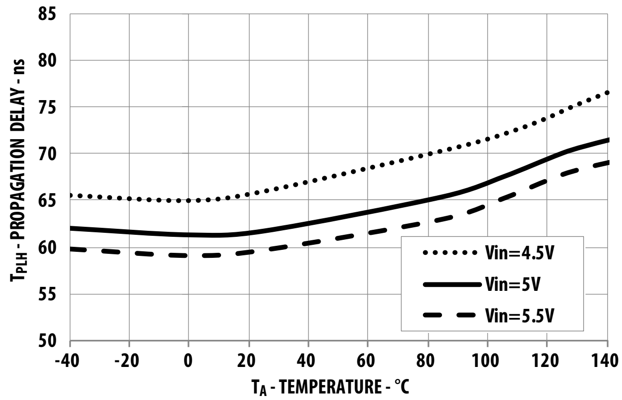


Figure 11: t_{PHL} vs. Temperature

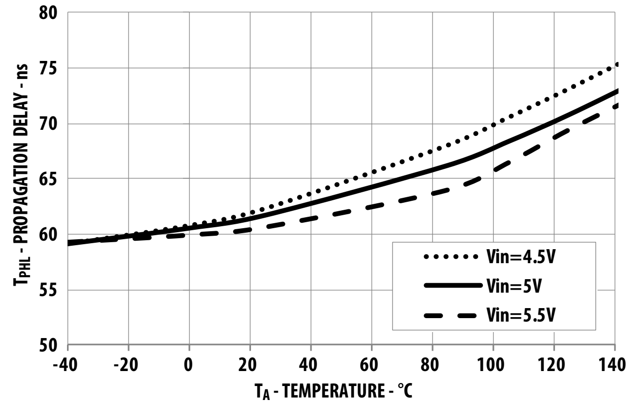


Figure 12: PWD vs. Temperature

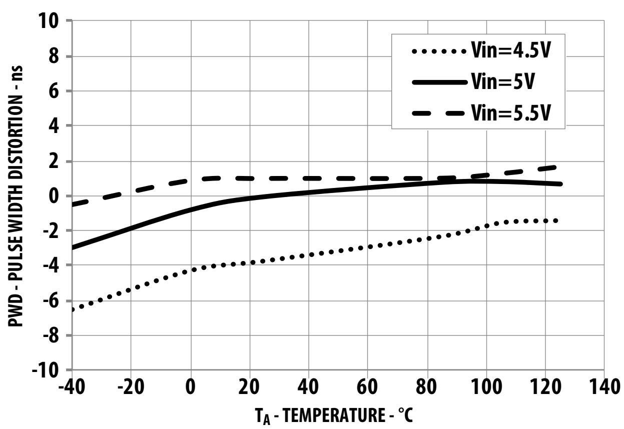


Figure 13: t_{PLH} and t_{PHL} Test Circuit

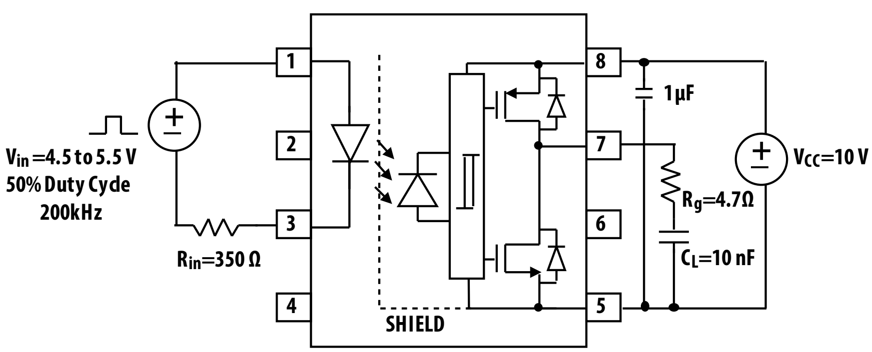


Figure 14: t_r and t_f Test Circuit

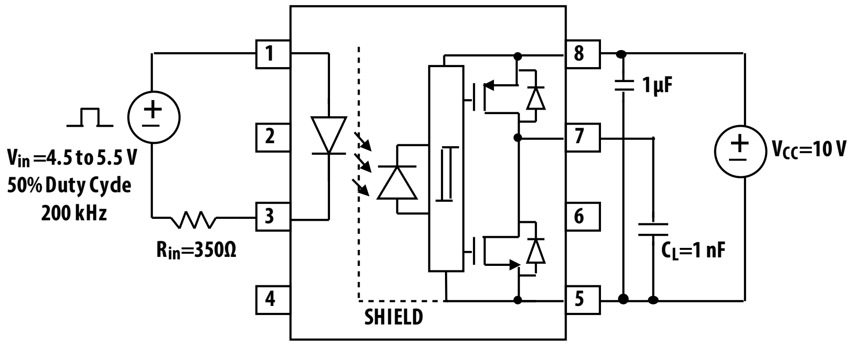


Figure 15: t_{PLH}, t_{PHL}, t_r and t_f Reference Waveforms

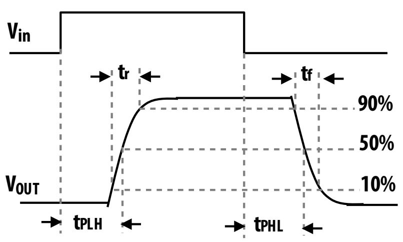
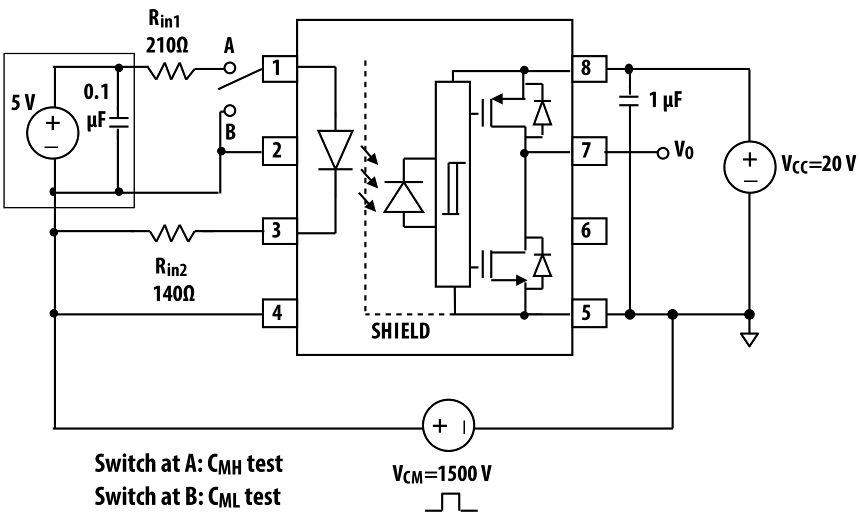


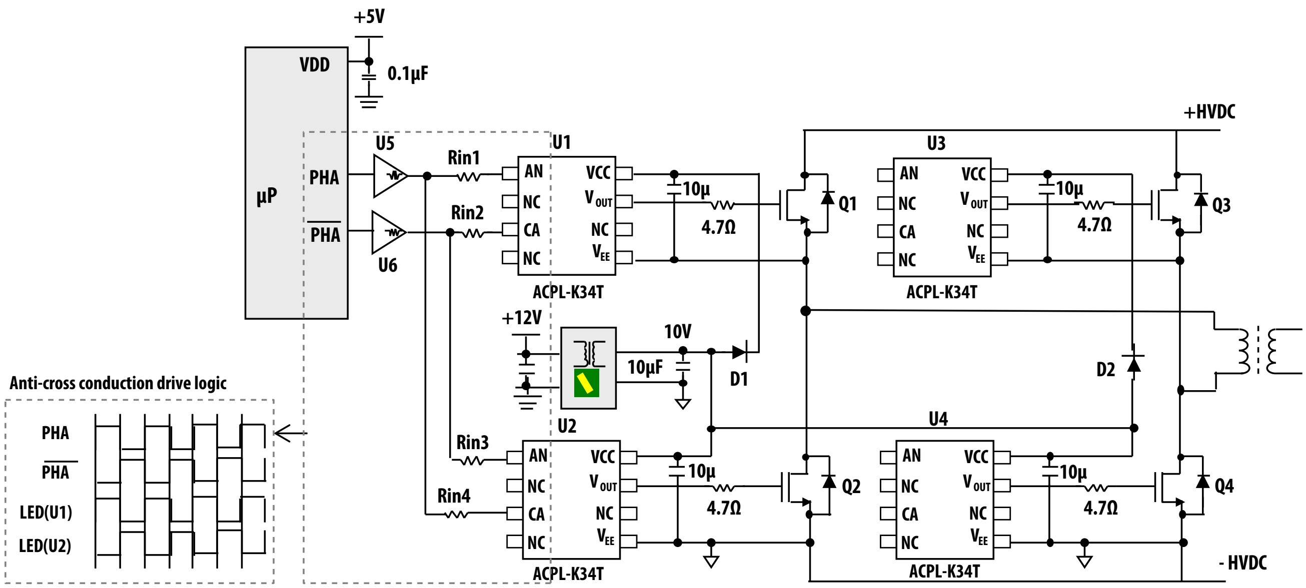
Figure 16: CMR Test Circuit



Application Information

Typical High-Speed MOSFET Gate Drive Circuit

Figure 17: Typical High-Speed MOSFET Gate Drive Circuit



Anti-Cross Conduction Drive

One of the many benefits of using ACPL-K34T is the ease to implement anti-cross conduction drive between the high-side and low-side gate drivers to prevent a shoot-through event. This safety interlock drive can be realized by interlocking the output of buffer U5 and U6 to both high-side and low-side gate drivers, as shown in Figure 17. However, due to the propagation delay difference between optocouplers, a certain amount of dead time must be added to ensure sufficient dead time at MOSFET gate. Refer to Dead Time Distortion and Propagation Delay for more details.

Recommended LED Drive Circuits

Common mode noise exists whenever there is a difference in the ground level of the optocoupler's input control circuitry and output control circuitry. Figure 18 and Figure 19 show the recommended LED drive circuits for high common mode rejection (CMR) performance of the optocoupler gate driver. Split-limiting resistors are used to balance the impedance at both anode and cathode of the input LED for high common mode noise rejection (see Figure 16).

Open drain and open collector drive circuits showed in Figure 20 are not recommended. During the off state of the MOSFET/transistor, cathode of the input LED sees high impedance and becomes sensitive to noise. In any cases, if the designer still prefers to use single a MOSFET/transistor drive over the recommended CMOS buffer drive shown in Figure 18 and Figure 19, the designer can choose alternative circuits shown in Figure 22 and Figure 23; however, the M1/Q1 drive circuits in Figure 22 and Figure 23 will shunt current during LED off state, which will result in more power consumption.

Drive Power

If a CMOS buffer is used to drive the LED, it is recommended to connect the CMOS buffer at the LED cathode. This is because the sinking capability of the NMOS is usually more than the driving capability of the PMOS in a CMOS buffer.

Drive Logic

The designer can configure the LED drive circuits for non-inverting and inverting logic as recommended in Figure 18 and Figure 19.The external power supply, V_{DD1}, must be connected to the CMOS buffer for the inverting and non-inverting logic to work. If the V_{DD1} supply is lost, the LED will be permanently off and the output will be at low logic.

Bypass and Reservoir Capacitors

Supply bypass capacitors are necessary at the input buffer and the ACPL-K34T output supply pin. A ceramic capacitor with the value of 0.1 µF is recommended at the input buffer to provide high frequency bypass, which also helps to improve the CMR performance. At the output supply pin ($V_{CC} – V_{EE}$), it is recommended to use a 10-µF, low ESR and low ESL capacitor as a charge reservoir to supply instant driving current to the MOSFET at V_{OUT} during switching.

Figure 18: Recommended Non-Inverting Drive Circuit

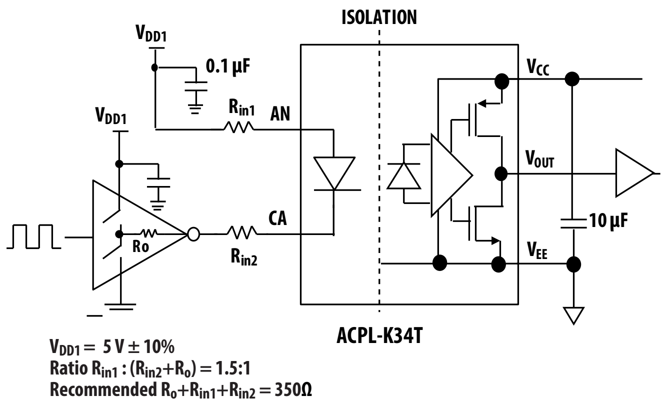


Figure 19: Recommended Inverting Drive Circuit

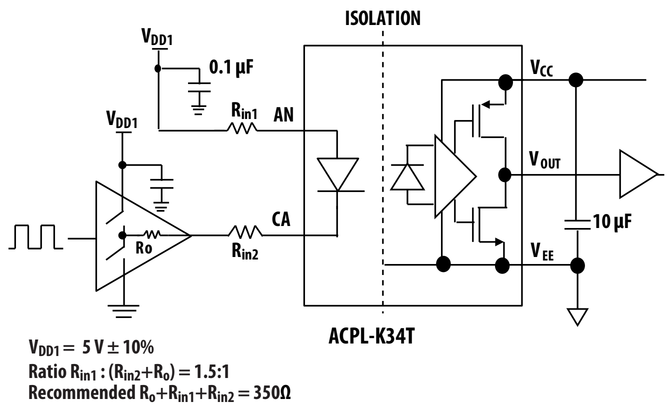


Figure 20: (A) Not Recommended – Open Drain/Open Collector Drive Circuit

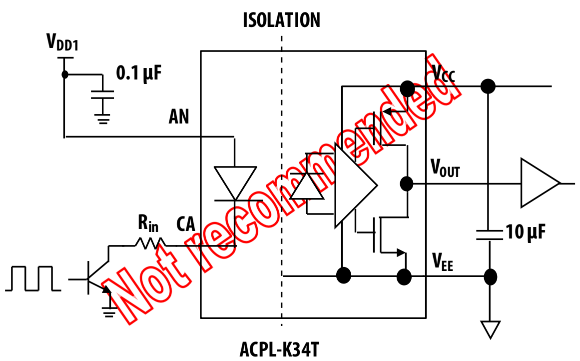


Figure 21: (B) Not Recommended – Open Drain/Open Collector Drive Circuit

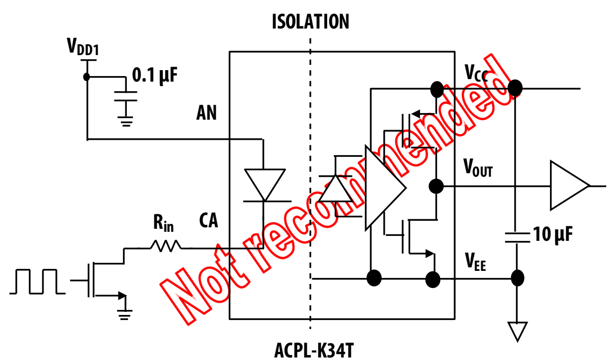


Figure 22: (A) Alternative LED Drive Circuits to Replace Figure 20 and Figure 21

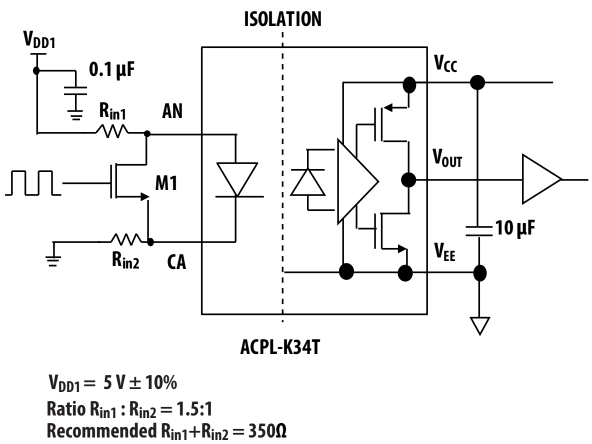
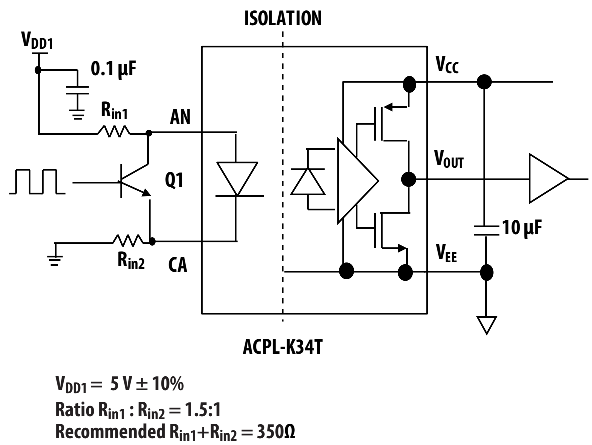


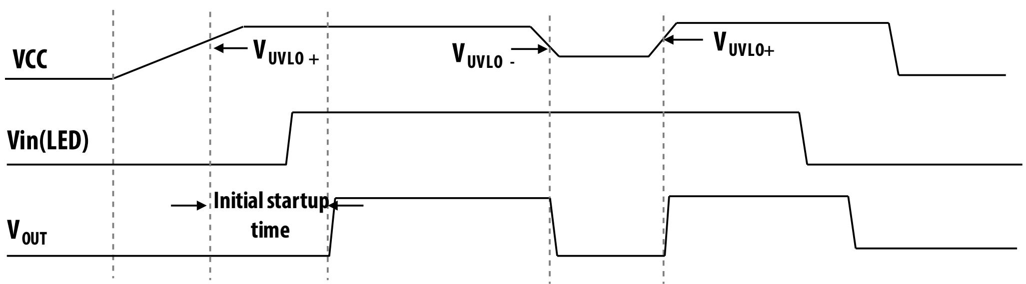
Figure 23: (B) Alternative LED Drive Circuits to Replace Figure 20 and Figure 21



Initial Power-Up and UVLO Operation

Insufficient gate voltage to the MOSFET can increase turn on resistance of the MOSFET, resulting in large power loss and MOSFET damage due to high heat dissipation. The ACPL-K34T monitors the output power supply constantly. During initial power-up, the ACPL-K34T requires a maximum 50 µs of initial startup time for the internal bias and circuitry to get ready. The gate driver output (V_{OUT}) is held at off state during the initial startup time. Thereafter, when the output power supply is lower than the under-voltage lockout (V_{UVLO-}) threshold, the gate driver output will shut off to protect the MOSFET from low voltage bias. When the output power supply is more than the V_{UVLO+} threshold, V_{OUT} is released from low state and it follows the input LED drive signal, as shown in Figure 24.

Figure 24: ACPL-K34T Initial Power-Up and UVLO Operation



Dead Time Distortion and Propagation Delay

Dead time is the period of time during which both high-side and low-side power transistors (shown as Q1 and Q2 in Figure 17) are off. Any overlap in Q1 and Q2 conduction will result in a shoot-through event, and large short circuit current will flow through the power devices between the high-side and low-side power rail.

The ACPL-K34T includes a dead time distortion (DTD) specification intended to help designers optimize dead time in a power inverter design. A negative DTD value will decrease the system dead time, and so a negative DTD must be compensated by adding extra dead time to the design. Figure 25 shows that dead time after optocoupler is reduced by negative DTD. On the other hand, a positive DTD will add to the system original dead time, and so a positive DTD will cause dead time redundancy to the system. Figure 26 shows that dead time after optocoupler is increased by positive DTD.

Figure 25: Dead Time and Propagation Delay Waveforms - Negative DTD Reduces Original DT

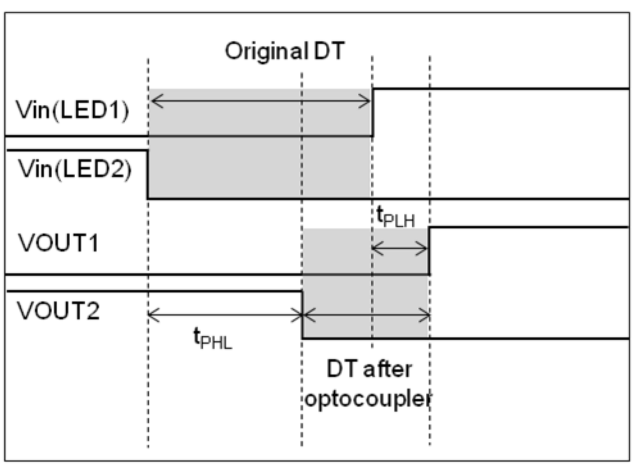
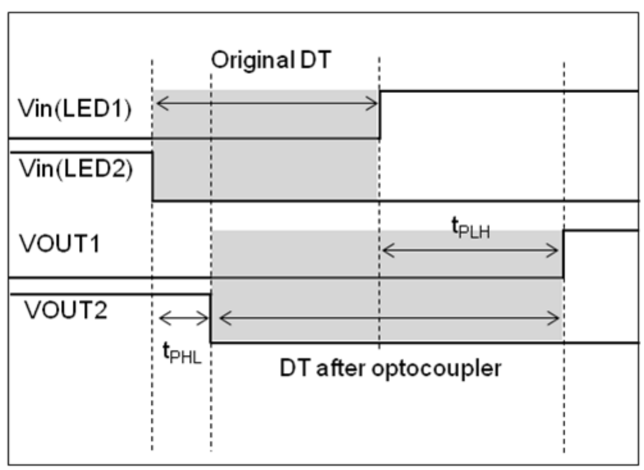


Figure 26: Dead Time and Propagation Delay Waveforms - Positive DTD Increased Original DT



To prevent cross-conduction between high-side and low-side power transistors, minimum dead time (DT MIN) must be introduced to the system. For example, given DTD MIN = –40 ns and DTD MAX = 50 ns, if designers target to have the minimum dead time (DT MIN) of 20 ns after the optocoupler, then the initial dead time (DT) needed for the system can be calculated as:

DT = DT MIN – DTD MIN
= 20 ns – (–40 ns)
= 60 ns

Maximum dead time (DT MAX) after the optocoupler can be calculated as:

DT MAX = DT + DTD MAX
= 60 ns + 50 ns
= 110 ns

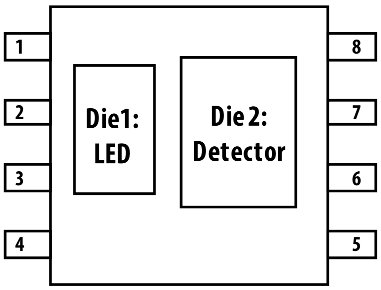
By introducing DT = 60 ns, the overall system dead time can vary from 20 ns to 110 ns due to the optocoupler's DTD.

NOTE: The propagation delays used to calculate dead time distortion (DTD) are taken at equal temperatures and test conditions since the optocouplers used are typically mounted close to each other and are switching the same type of MOSFETs

Thermal Resistance Model for ACPL-K34T

The diagram for measurement is shown in Figure 27. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the second die is heated and all the dice temperatures are recorded. With the known ambient temperature, the die junction temperature, and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 2-by-2 matrix for our case of two heat sources.

Figure 27: Diagram of ACPL-K34T for Measurement



$$\begin{vmatrix} R11 & R12 \\ R21 & R22 \end{vmatrix} \bullet \begin{vmatrix} P1 \\ P2 \end{vmatrix} = \begin{vmatrix} \Delta T1 \\ \Delta T2 \end{vmatrix}$$

Definitions

R11: Thermal Resistance of Die1 due to heating of Die1 (°C/W)
R12: Thermal Resistance of Die1 due to heating of Die2 (°C/W)
R21: Thermal Resistance of Die2 due to heating of Die1 (°C/W)
R22: Thermal Resistance of Die2 due to heating of Die2 (°C/W)

P1: Power dissipation of Die1 (W)
P2: Power dissipation of Die2 (W)

T1: Junction temperature of Die1 due to heat from all dice (°C)
T2: Junction temperature of Die2 due to heat from all dice (°C)
T_A: Ambient temperature (°C)
ΔT1: Temperature difference between Die1 junction and ambient (°C)
ΔT2: Temperature deference between Die2 junction and ambient (°C)

Equation 1:

$T1 = (R11 \times P1 + R12 \times P2) + T_A$

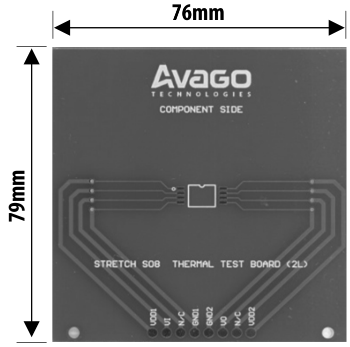
Equation 2:

$T2 = (R21 \times P1 + R22 \times P2) + T_A$

Measurement Data

Measurement is done on both low and high conductivity boards as shown in the following table.

Table 1: Test Board Thermal Conductivity Measurement Data

Layout	Measurement Data	
	Low conductivity board: R11 = 191°C/W R12 = R21 = 68.5°C/W R22 = 77°C/W	High conductivity board: R11 = 155°C/W R12 = R21 = 64°C/W R22 = 41°C/W

Note that the thermal resistance R11, R12, R21, and R22 in Table 1 can be improved by increasing the ground plane/copper area.

Application and environment design for the ACPL-K34T must ensure that the junction temperature of the internal IC and LED within the gate drive optocoupler do not exceed 150°C. Equation 1 and Equation 2 are for the purposes of estimating the junction temperatures.

The following provides an example.

Calculation of LED and Output IC Power Dissipation

LED power dissipation, $P_E = I_{F(LED)}$ (Recommended Max.) × $V_{F(LED)}$ (at 125°C) × Duty Cycle

$= 13\text{ mA} \times 1.25\text{V} \times 50\%$

$= 8.125\text{ mW}$

Output IC power dissipation, $P_O = V_{CC}$ (Recommended Max.) × $I_{CC(MAX)} + P_{HS} + P_{LS}$

$= 20\text{V} \times 4\text{ mA} + 53.3\text{ mW} + 32\text{ mW}$

$= 165.3\text{ mW}$

where:

P_{HS} = High-side switching power dissipation

$= (V_{CC} \times Q_G \times f_{PWM}) \times R_{DS,OH(MAX)} / (R_{DS,OH(MAX)} + R_{GH}) /2$

$= (20\text{V} \times 80\text{ nC} \times 200\text{ kHz}) \times 4\Omega/(4\Omega + 8\Omega)/2$

$= 53.3\text{ mW}$

P_{LS} = Low-side switching power dissipation

$= (V_{CC} \times Q_G \times f_{PWM}) \times R_{DS,OL(MAX)} / (R_{DS,OL(MAX)} + R_{GL}) /2$

$= (20\text{V} \times 80\text{ nC} \times 200\text{ kHz}) \times 2\Omega/(2\Omega + 8\Omega)/2$

$= 32\text{ mW}$

Q_G = Gate charge at supply voltage

f_{PWM} = LED switching frequency
R_{GH} = Gate charging resistance
R_{GL} = Gate discharging resistance

Calculation of LED junction temperature and output IC junction temperature at T_A = 125°C:

LED junction temperature:

$T1 = (R11 \times P_E + R12 \times P_O) + T_A$
$= (191°C/W \times 8.125\ mW + 68.5°C/W \times 165.3\ mW) + 125°C$
$= 138°C < T_{J(absolute\ max)}$ of 150°C

Output IC junction temperature:

$T2 = (R21 \times P_E + R22 \times P_O) + T_A$
$= (68.5°C/W \times 8.125\ mW + 77°C/W \times 165.3\ mW) + 125°C$
$= 138°C < T_{J(absolute\ max)}$ of 150°C

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