

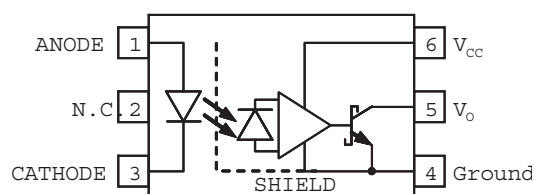
## ACPL-P456 and ACPL-W456

### High-CMR Intelligent Power Module and Gate Drive Interface Optocoupler

#### Description

The ACPL-P456 and ACPL-W456 contain a GaAsP LED that is optically coupled to an integrated high-gain photodetector. A minimized propagation delay difference between devices makes these optocouplers excellent solutions for improving inverter efficiency through reduced switching dead time. Specifications and performance plots are given for typical Intelligent Power Module (IPM) applications.

#### Functional Diagram



**NOTE:** A 0.1- $\mu$ F bypass capacitor must be connected between pins 4 and 6.

#### Truth Table (Positive Logic)

| LED | V <sub>O</sub> |
|-----|----------------|
| ON  | LOW            |
| OFF | HIGH           |

#### Applications

- IPM isolation
- Isolated IGBT/MOSFET gate drives
- AC and brushless DC motor drives
- Industrial inverters

#### Features

- Performance specified for common IPM applications over the industrial temperature range
- Short maximum propagation delays
- Minimized pulse width distortion (PWD)
- Very high common mode rejection (CMR)
- High current transfer ratio (CTR)
- Available in a stretched SO-6 package with 7 mm or 8 mm of creepage and clearance
- Safety approval:
  - UL recognized with 5000V<sub>RMS</sub> for 1 minute per UL1577
  - CSA approved
  - IEC/EN/DIN EN 60747-5-5 approved with V<sub>IORM</sub> = 1140V<sub>peak</sub> (ACPL-W456) and V<sub>IORM</sub> = 891V<sub>peak</sub> (ACPL-P456) for Option 060

#### Specifications

- Wide operating temperature range: –40°C to 100°C
- Maximum propagation delay t<sub>PHL</sub> = 400 ns, t<sub>PLH</sub> = 490 ns
- Maximum PWD = 450 ns
- 15-kV/ $\mu$ s minimum CMR at V<sub>CM</sub> = 1500V
- CTR > 44% at I<sub>F</sub> = 10 mA

**CAUTION!** Take normal static precautions in the handling and assembly of this component to prevent damage and/or degradation that can be induced by ESD.

## Ordering Information

The ACPL-P456 and ACPL-W456 are UL recognized with 5000V<sub>RMS</sub> for 1 minute per UL1577 and are approved under CSA Component Acceptance Notice #5, File CA 88324.

| Part Number            | Option         | Package           | Surface Mount | Tape and Reel | IEC/EN/DIN EN 60747-5-5 | Quantity      |
|------------------------|----------------|-------------------|---------------|---------------|-------------------------|---------------|
|                        | RoHS Compliant |                   |               |               |                         |               |
| ACPL-P456<br>ACPL-W456 | -000E          | Stretched<br>SO-6 | X             |               |                         | 100 per tube  |
|                        | -500E          |                   | X             | X             |                         | 1000 per tube |
|                        | -060E          |                   | X             |               | X                       | 100 per tube  |
|                        | -560E          |                   | X             | X             | X                       | 1000 per tube |

To form an ordering part number, choose a part number from the Part Number column, and combine it with the desired option from the Option column.

Example 1: Use ACPL-P456-560E to order the product in a stretched SO-6 package in tape and reel packaging with IEC/EN/DIN EN 60747-5-5 safety approval and RoHS compliance.

Example 2: Use ACPL-P456-000E to order the product in a stretched SO-6 package in tube packaging and RoHS compliance.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

## Solder Reflow Profile

The recommended reflow profile is per JEDEC standard J-STD-020 (latest revision). Nonhalide flux should be used.

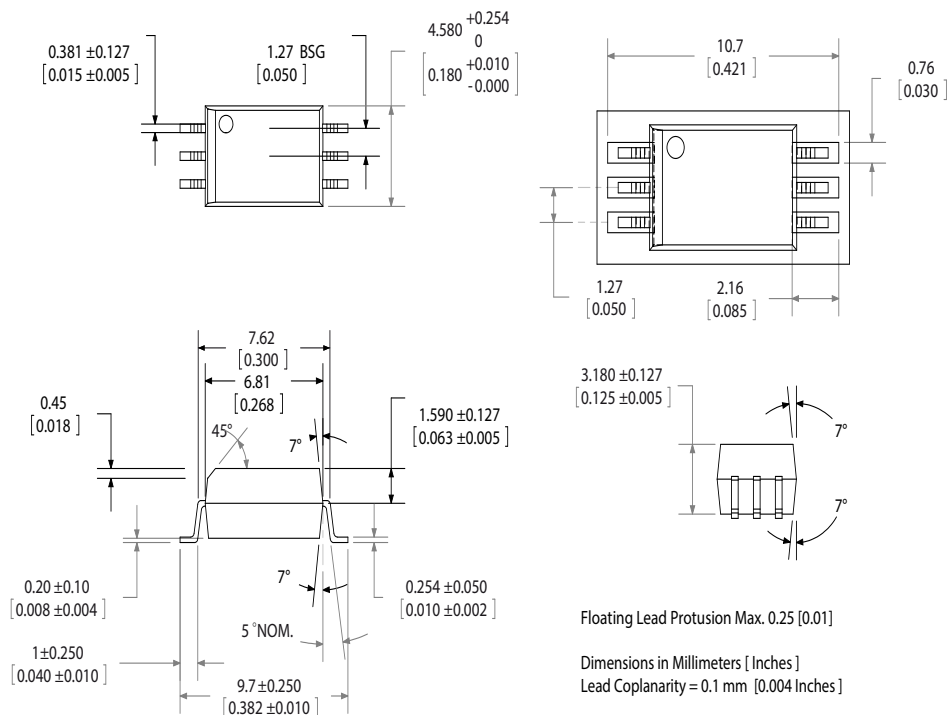
## Regulatory Information

The ACPL-P456 and ACPL-W456 are approved by the following organizations:

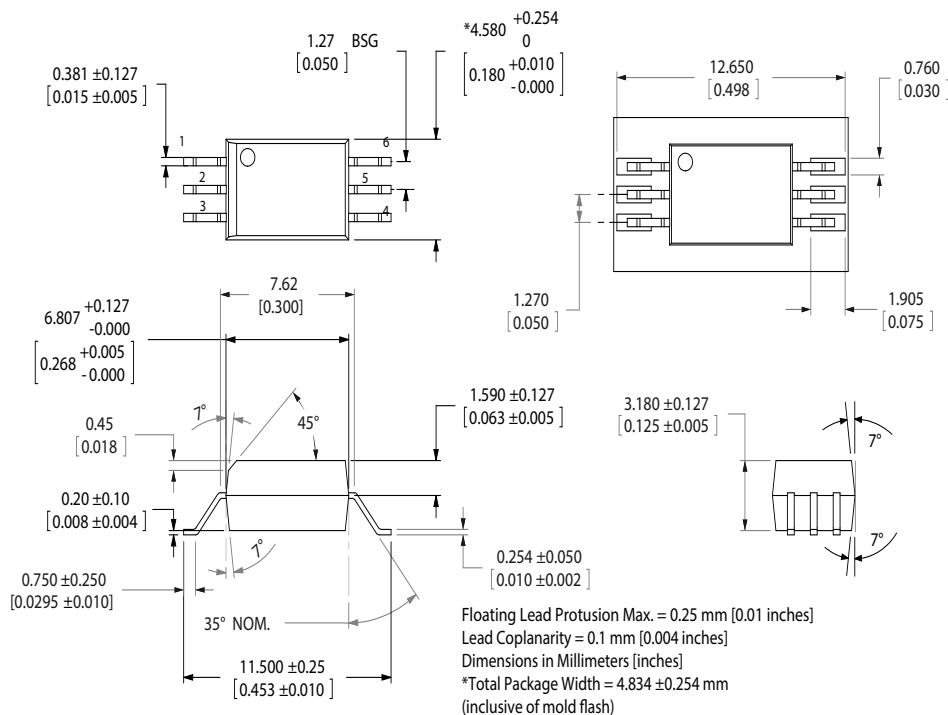
- IEC/EN/DIN EN 60747-5-5 (Option 060 only): Approved with maximum working insulation voltage  $V_{IORM} = 1140V_{peak}$  (ACPL-W456) and  $V_{IORM} = 891V_{peak}$  (ACPL-P456).
- UL: Approval under UL 1577, component recognition program up to  $V_{ISO} = 5000V_{RMS}$ , File E55361.
- CSA: Approval under CSA Component Acceptance Notice #5, File CA 88324.

## Package Outline Drawings

### ACPL-P456 Stretched SO-6 Package (7 mm of Clearance)



### ACPL-W456 Stretched SO-6 Package (8 mm of Clearance)



## IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (Option 060)

| Description                                                                                                                                                                                                                                                                                  | Symbol          | ACPL-P456                              | ACPL-W456                                       | Unit       |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|----------------------------------------|-------------------------------------------------|------------|
| Installation Classification per DIN VDE 0110/1.89, Table 1<br>For rated mains voltage $\leq 150V_{RMS}$<br>For rated mains voltage $\leq 300V_{RMS}$<br>For rated mains voltage $\leq 450V_{RMS}$<br>For rated mains voltage $\leq 600V_{RMS}$<br>For rated mains voltage $\leq 1000V_{RMS}$ | —               | I – IV<br>I – IV<br>I – III<br>I – III | I – IV<br>I – IV<br>I – IV<br>I – IV<br>I – III | —          |
| Climatic Classification                                                                                                                                                                                                                                                                      | 55/100/21       |                                        |                                                 |            |
| Pollution Degree (DIN VDE 0110/39)                                                                                                                                                                                                                                                           | 2               |                                        |                                                 |            |
| Maximum Working Insulation Voltage                                                                                                                                                                                                                                                           | $V_{IORM}$      | 891                                    | 1140                                            | $V_{peak}$ |
| Input to Output Test Voltage, Method b <sup>a</sup><br>$V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ second,<br>Partial Discharge $< 5$ pC                                                                                                                          | $V_{PR}$        | 1671                                   | 2138                                            | $V_{peak}$ |
| Input to Output Test Voltage, Method a <sup>a</sup><br>$V_{IORM} \times 1.5 = V_{PR}$ , Type and Sample Test, $t_m = 10$ seconds,<br>Partial Discharge $< 5$ pC                                                                                                                              | $V_{PR}$        | 1425                                   | 1824                                            | $V_{peak}$ |
| Highest Allowable Overvoltage<br>(Transient Overvoltage $t_{ini} = 60$ seconds)                                                                                                                                                                                                              | $V_{IOTM}$      | 6000                                   | 8000                                            | $V_{peak}$ |
| Safety-Limiting Values – maximum values allowed in the event of a failure                                                                                                                                                                                                                    |                 |                                        |                                                 |            |
| Case Temperature                                                                                                                                                                                                                                                                             | $T_S$           | 175                                    |                                                 | °C         |
| Input Current                                                                                                                                                                                                                                                                                | $I_{S, INPUT}$  | 230                                    |                                                 | mA         |
| Output Power                                                                                                                                                                                                                                                                                 | $P_{S, OUTPUT}$ | 600                                    |                                                 | mW         |
| Insulation Resistance at $T_S$ , $V_{IO} = 500V$                                                                                                                                                                                                                                             | $R_S$           | $>10^9$                                |                                                 | $\Omega$   |

a. Refer to the optocoupler section of the *Isolation and Control Components Designer's Catalog*, under the Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5), for a detailed description of the Method a and Method b partial discharge test profiles.

## Insulation and Safety Related Specifications

| Parameter                                            | Symbol | ACPL-P456 | ACPL-W456 | Unit | Conditions                                                                                                                             |
|------------------------------------------------------|--------|-----------|-----------|------|----------------------------------------------------------------------------------------------------------------------------------------|
| Minimum External Air Gap<br>(External Clearance)     | L(101) | 7.0       | 8.0       | mm   | Measured from input terminals to output terminals, shortest distance through the air.                                                  |
| Minimum External Tracking<br>(External Creepage)     | L(102) | 8.0       | 8.0       | mm   | Measured from input terminals to output terminals, shortest distance path along the body.                                              |
| Minimum Internal Plastic Gap<br>(Internal Clearance) | —      | 0.08      |           | mm   | Through insulation distance conductor to conductor, usually the straight-line distance thickness between the emitter and the detector. |
| Minimum Internal Tracking<br>(Internal Creepage)     | —      | N/A       |           | mm   | Measured from input terminals to output terminals, along the internal cavity.                                                          |
| Tracking Resistance<br>(Comparative Tracking Index)  | CTI    | $>175$    |           | V    | DIN IEC 112/VDE 0303 Part 1.                                                                                                           |
| Isolation Group                                      | —      | IIIa      |           | —    | Material Group (DIN VDE 0110, 1/89, Table 1).                                                                                          |

## Absolute Maximum Ratings

| Parameter                                                    | Symbol                         | Min. | Max. | Unit | Note |
|--------------------------------------------------------------|--------------------------------|------|------|------|------|
| Storage Temperature                                          | $T_S$                          | –55  | +125 | °C   |      |
| Operating Temperature                                        | $T_A$                          | –40  | +100 | °C   |      |
| Average Input Current                                        | $I_{F(AVG)}$                   | —    | 25   | mA   | a    |
| Peak Input Current<br>(50% duty cycle, <1-ms pulse width)    | $I_{F(PEAK)}$                  | —    | 50   | mA   | b    |
| Peak Transient Input Current<br>(<1-ms pulse width, 300 pps) | $I_{F(TRAN)}$                  | —    | 1.0  | A    |      |
| Reverse Input Voltage (Pins 3–1)                             | $V_R$                          | —    | 5    | V    |      |
| Average Output Current (Pin 5)                               | $I_{O(AVG)}$                   | —    | 25   | mA   |      |
| Output Voltage (Pins 5–4)                                    | $V_O$                          | –0.5 | +30  | V    |      |
| Supply Voltage (Pins 6–4)                                    | $V_{CC}$                       | –0.5 | +30  | V    |      |
| Output Power Dissipation                                     | $P_O$                          | —    | —    | mW   | c    |
| Total Power Dissipation                                      | $P_T$                          | —    | 210  | mW   | d    |
| Infrared and Vapor Phase Reflow Temperature                  | See the reflow thermal profile |      |      |      |      |

a. Derate linearly above 90°C free-air temperature at a rate of 0.8 mA/°C.

b. Derate linearly above 90°C free-air temperature at a rate of 1.6 mA/°C.

c. Derate linearly above 90°C free-air temperature at a rate of 3.0 mW/°C.

d. Derate linearly above 90°C free-air temperature at a rate of 4.2 mW/°C.

## Recommended Operating Conditions

| Parameter             | Symbol       | Min. | Max. | Unit |
|-----------------------|--------------|------|------|------|
| Power Supply Voltage  | $V_{CC}$     | 4.5  | 30   | V    |
| Output Voltage        | $V_O$        | 0    | 30   | V    |
| Input Current (ON)    | $I_{F(ON)}$  | 10   | 20   | mA   |
| Input Voltage (OFF)   | $V_{F(OFF)}$ | –5   | 0.8  | V    |
| Operating Temperature | $T_A$        | –40  | +100 | °C   |

## Electrical Specifications

Over recommended operating conditions unless otherwise specified:  $T_A = -40^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ ,  $V_{CC} = 4.5\text{V}$  to  $30\text{V}$ ,  $I_{F(\text{ON})} = 10\text{ mA}$  to  $20\text{ mA}$ ,  $V_{F(\text{OFF})} = -5\text{V}$  to  $+0.8\text{V}$ .

| Parameter                                  | Symbol                    | Min. | Typ. | Max. | Unit                         | Test Conditions                              | Figure | Note |
|--------------------------------------------|---------------------------|------|------|------|------------------------------|----------------------------------------------|--------|------|
| Current Transfer Ratio                     | CTR                       | 44   | 90   | —    | %                            | $I_F = 10\text{ mA}$ , $V_O = 0.6\text{V}$   |        | a    |
| Low Level Output Current                   | $I_{OL}$                  | 4.4  | 9.0  | —    | mA                           | $I_F = 10\text{ mA}$ , $V_O = 0.6\text{V}$   | 1, 2   |      |
| Low Level Output Voltage                   | $V_{OL}$                  | —    | 0.3  | 0.6  | V                            | $I_O = 2.4\text{ mA}$                        |        |      |
| Input Threshold Current                    | $I_{TH}$                  | —    | 1.5  | 5.0  | mA                           | $V_O = 0.8\text{V}$ , $I_O = 0.75\text{ mA}$ | 1      | b    |
| High Level Output Current                  | $I_{OH}$                  | —    | 5    | 50   | $\mu\text{A}$                | $V_F = 0.8\text{V}$                          | 3      |      |
| High Level Supply Current                  | $I_{CCH}$                 | —    | 0.6  | 1.3  | mA                           | $V_F = 0.8\text{V}$ , $V_O = \text{Open}$    |        | b    |
| Low Level Supply Current                   | $I_{CCL}$                 | —    | 0.6  | 1.3  | mA                           | $I_F = 10\text{ mA}$ , $V_O = \text{Open}$   |        | b    |
| Input Forward Voltage                      | $V_F$                     | —    | 1.5  | 1.8  | V                            | $I_F = 10\text{ mA}$                         | 4      |      |
| Temperature Coefficient of Forward Voltage | $\Delta V_F / \Delta T_A$ | —    | -1.6 | —    | $\text{mV}/^{\circ}\text{C}$ | $I_F = 10\text{ mA}$                         |        |      |
| Input Reverse Breakdown Voltage            | $V_{BR}$                  | 5    | —    | —    | V                            | $I_R = 10\text{ }\mu\text{A}$                |        |      |
| Input Capacitance                          | $C_{IN}$                  | —    | 60   | —    | pF                           | $f = 1\text{ MHz}$ , $V_F = 0\text{V}$       |        |      |

a. Current transfer ratio in percent is defined as the ratio of output collector current ( $I_O$ ) to the forward LED input current ( $I_F$ ) multiplied by 100.

b. Use of a 0.1- $\mu\text{F}$  bypass capacitor connected between pins 4 and 6 can improve performance by filtering power supply line noise.

## Switching Specifications ( $R_L = 20\text{ k}\Omega$ )

Over recommended operating conditions unless otherwise specified.  $T_A = -40^\circ\text{C}$  to  $+100^\circ\text{C}$ ,  $V_{CC} = +4.5\text{V}$  to  $30\text{V}$ ,  $I_{F(ON)} = 10\text{ mA}$  to  $20\text{ mA}$ ,  $V_{F(OFF)} = -5\text{V}$  to  $0.8\text{V}$ .

| Parameter                                          | Symbol              | Min. | Typ. | Max. | Unit              | Test Conditions                               | Fig.               | Note |
|----------------------------------------------------|---------------------|------|------|------|-------------------|-----------------------------------------------|--------------------|------|
| Propagation Delay Time to Logic Low Output Level   | $t_{PHL}$           | 30   | 200  | 400  | ns                | $C_L = 100\text{ pF}$                         | 5, 7, 8, 9, 10, 11 | a, b |
|                                                    |                     | —    | 100  | —    | —                 | $C_L = 10\text{ pF}$                          |                    |      |
| Propagation Delay Time to Logic High Output Level  | $t_{PLH}$           | 270  | 400  | 550  | ns                | $C_L = 100\text{ pF}$                         |                    |      |
|                                                    |                     | —    | 130  | —    | —                 | $C_L = 10\text{ pF}$                          |                    |      |
| Pulse Width Distortion                             | PWD                 | —    | 200  | 450  | ns                | $C_L = 100\text{ pF}$                         |                    | c    |
| Propagation Delay Difference Between Any Two Parts | $t_{PLH} - t_{PHL}$ | -150 | +200 | +450 | ns                | —                                             |                    | d    |
| Output High Level Common Mode Transient Immunity   | $ CM_H $            | 15   | 30   | —    | kV/ $\mu\text{s}$ | $I_F = 0\text{ mA}$ ,<br>$V_O > 3.0\text{V}$  | 6                  | e    |
| Output Low Level Common Mode Transient Immunity    | $ CM_L $            | 15   | 30   | —    | kV/ $\mu\text{s}$ | $I_F = 10\text{ mA}$ ,<br>$V_O < 1.0\text{V}$ |                    | f    |

- a. Pulse:  $f = 20\text{ kHz}$ , duty cycle = 10%.
- b. Use of a  $0.1\text{-}\mu\text{F}$  bypass capacitor connected between pins 4 and 6 can improve performance by filtering power supply line noise.
- c. Pulse width distortion (PWD) is defined as  $|t_{PHL} - t_{PLH}|$  for any given device.
- d. The difference between  $t_{PLH}$  and  $t_{PHL}$  between any two parts under the same test condition. (See [IPM Dead Time and Propagation Delay Specifications](#).)
- e. Common mode transient immunity at a logic high level is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to ensure that the output will remain in a logic high state (that is,  $V_O > 3.0\text{V}$ ).
- f. Common mode transient immunity at a logic low level is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to ensure that the output will remain in a logic low state (that is,  $V_O < 1.0\text{V}$ ).

## Package Characteristics

| Parameter                                             | Symbol    | Min. | Typ.      | Max. | Unit      | Test Conditions                                                 | Note    |
|-------------------------------------------------------|-----------|------|-----------|------|-----------|-----------------------------------------------------------------|---------|
| Input-Output Momentary Withstand Voltage <sup>a</sup> | $V_{ISO}$ | 5000 | —         | —    | $V_{RMS}$ | $RH < 50\%$ , $t = 1\text{ minute}$<br>$T_A = 25^\circ\text{C}$ | b, c, d |
| Input-Output Resistance                               | $R_{I-O}$ | —    | $10^{12}$ | —    | $\Omega$  | $V_{I-O} = 500V_{DC}$                                           | c       |
| Input-Output Capacitance                              | $C_{I-O}$ | —    | 0.6       | —    | pF        | $f = 1\text{ MHz}$                                              | c       |

- a. The input-output momentary withstand voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, see the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics table (if applicable).
- b. For ACPL-W456 and ACPL-P456.
- c. The device is considered a two-terminal device: Pins 1 and 3 are shorted together, and Pins 4, 5, and 6 are shorted together.
- d. In accordance with UL1577, each optocoupler is proof-tested by applying an insulation test voltage of  $6000V_{RMS}$  for 1 second (leakage detection current limit,  $I_{I-O} \leq 5\text{ }\mu\text{A}$ ).

Figure 1: Typical Transfer Characteristics

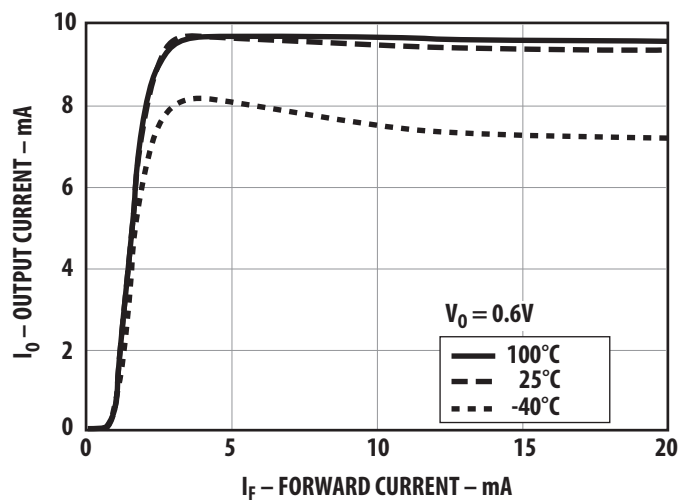


Figure 2: Normalized Output Current vs. Temperature

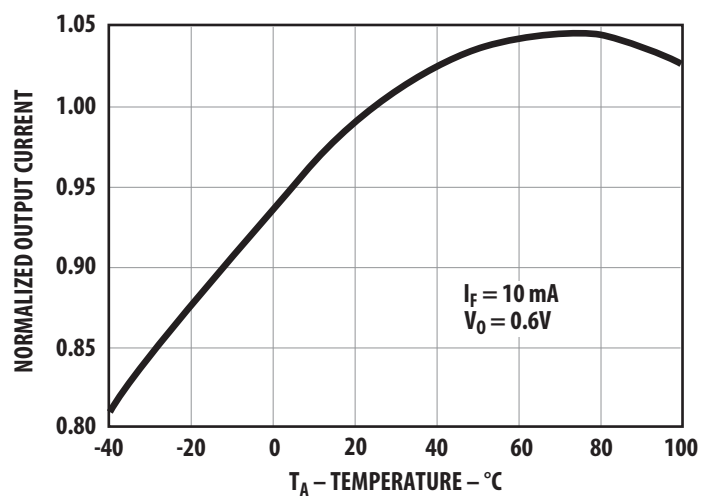


Figure 3: High Level Output Current vs. Temperature

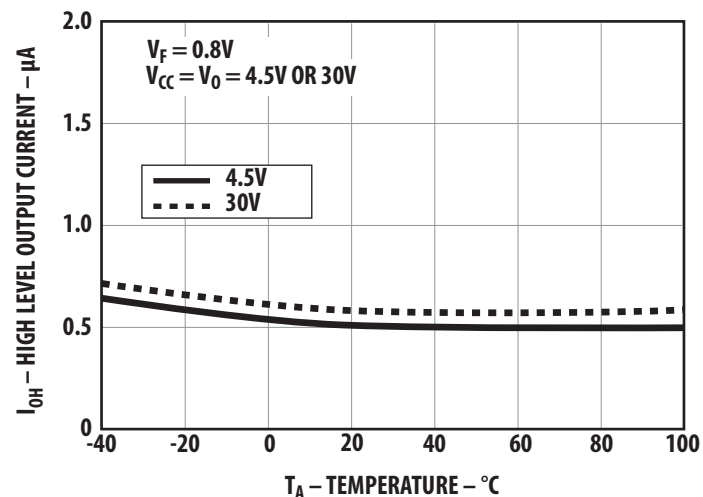


Figure 4: Input Current vs. Forward Voltage

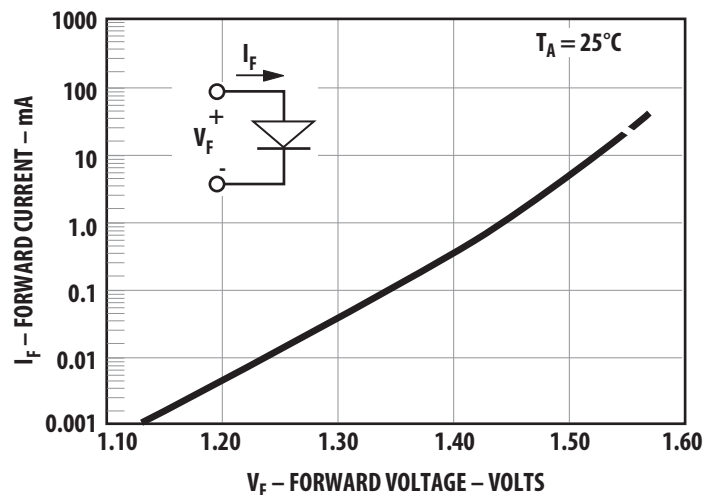
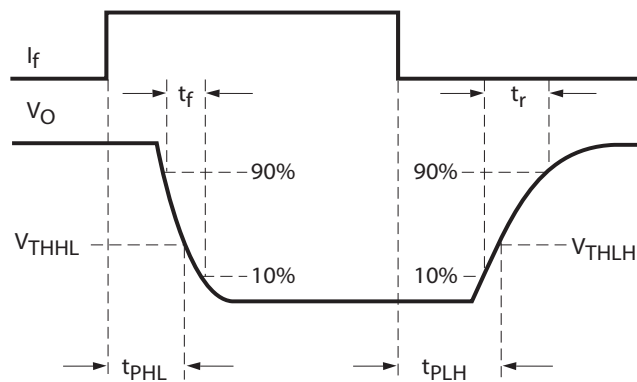
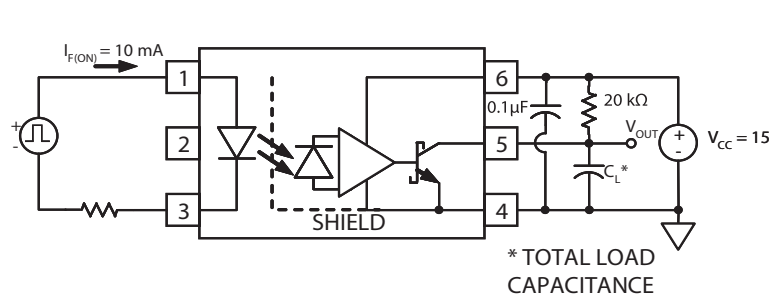


Figure 5: Propagation Delay Test Circuit



### Figure 6: CMR Test Circuit and Waveforms

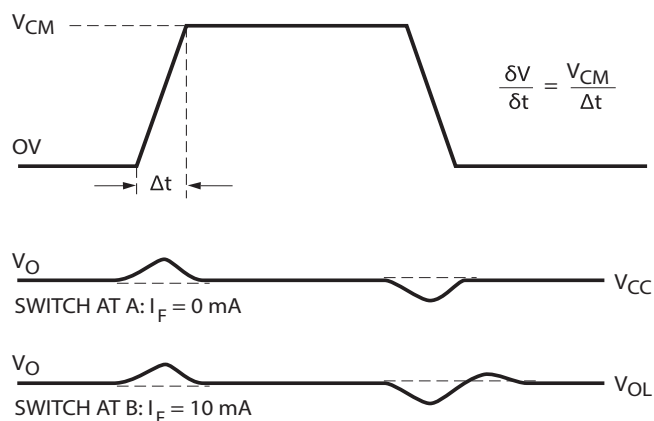
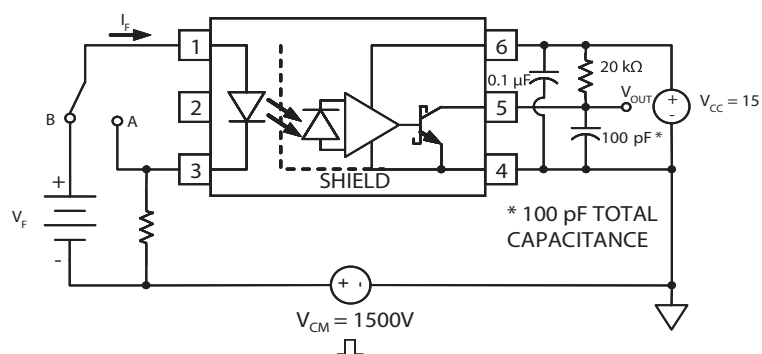
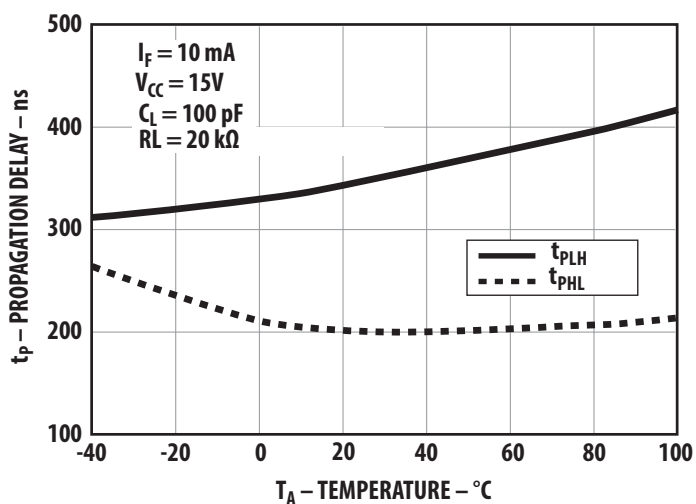
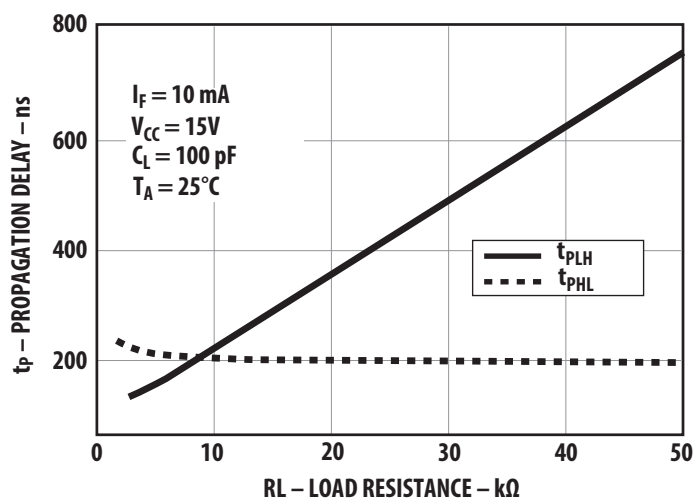


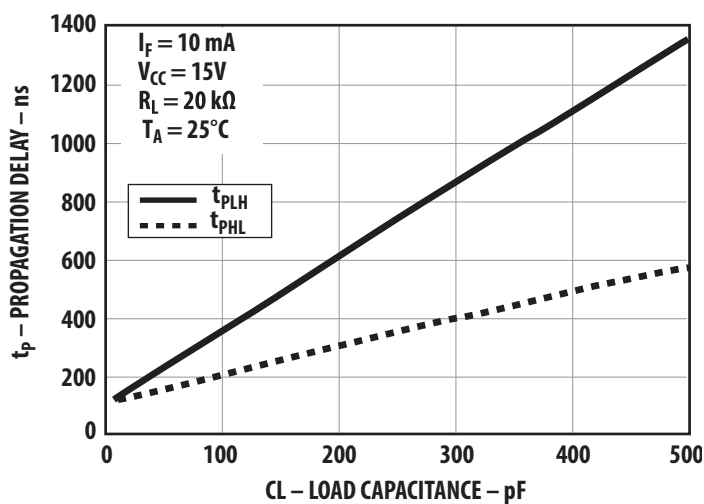
**Figure 7: Propagation Delay with External 20-k $\Omega$  R<sub>L</sub> vs. Temp.**



### Figure 8: Propagation Delay vs. Load Resistance



### Figure 9: Propagation Delay vs. Load Capacitance



### Figure 10: Propagation Delay vs. Supply Voltage

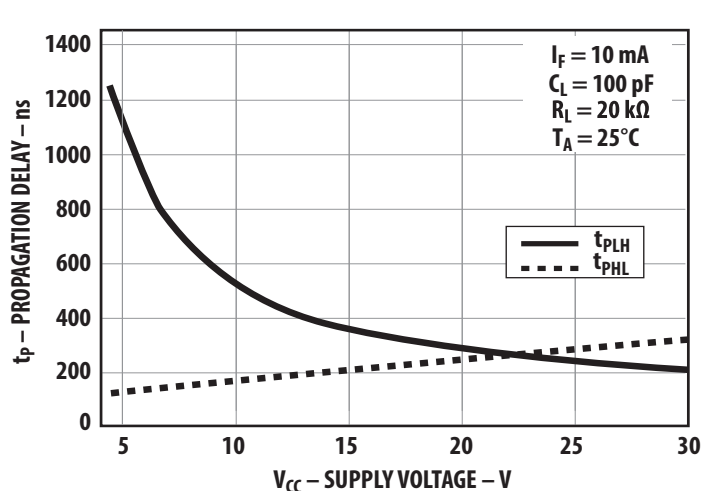
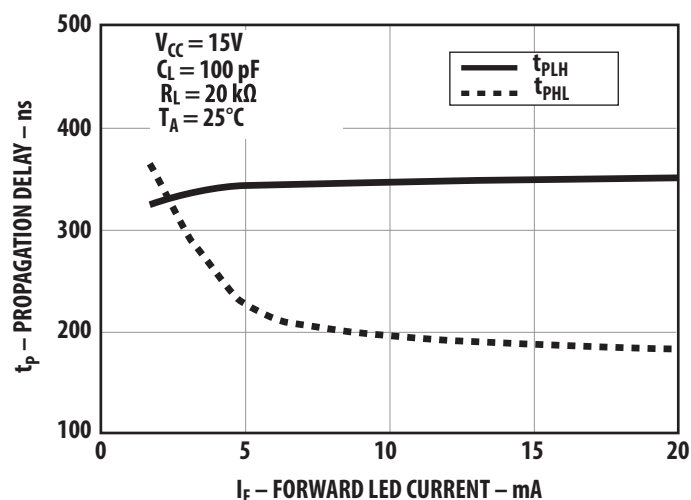


Figure 11: Propagation Delay vs. Input Current



## Applications Information

### LED Drive Circuit Considerations for Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 13. The ACPL-P456/W456 improve CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and the optocoupler output pin and output ground as shown in Figure 14. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high-CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 12) can achieve a 15-kV/ $\mu\text{s}$  CMR while minimizing component complexity. Note that a CMOS gate is recommended in Figure 12 to keep the LED off when the gate is in the high state.

Figure 12: Recommended LED Drive Circuit

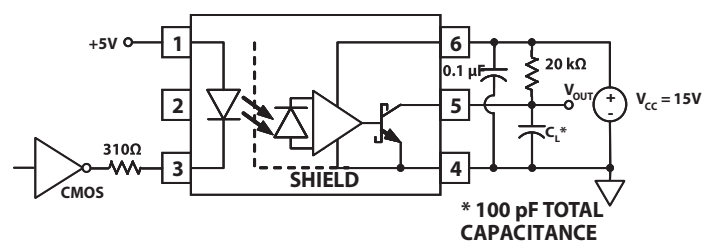
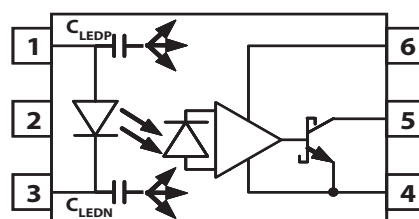
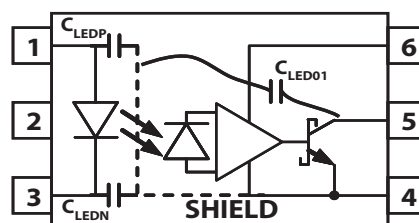


Figure 13: Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers



Another cause of CMR failure for a shielded optocoupler is direct coupling to the optocoupler output pins through  $C_{LED01}$  in Figure 14. Many factors influence the effect and magnitude of the direct coupling including the position of the LED current setting resistor and the value of the capacitor at the optocoupler output ( $C_L$ ).

Figure 14: Optocoupler Input to Output Capacitance Model for Shielded Optocouplers



## CMR with the LED On (CMRL)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. The recommended minimum LED current of 10 mA provides adequate margin over the maximum  $I_{TH}$  of 4.0 mA (see Figure 1) to achieve a 15-kV/ $\mu$ s CMR.

The placement of the LED current setting resistor affects the ability of the drive circuit to keep the LED on during transients and interacts with the direct coupling to the optocoupler output. For example, the LED resistor in Figure 15 is connected to the anode. Figure 16 shows the AC equivalent circuit for Figure 15 during common mode transients. During a  $+dV_{CM}/dt$  in Figure 16, the current available at the LED anode ( $I_{TOTAL}$ ) is limited by the series resistor. The LED current ( $I_F$ ) is reduced from its DC value by an amount equal to the current that flows through  $C_{LEDP}$  and  $C_{LEDO1}$ . The situation is made worse because the current through  $C_{LEDO1}$  has the effect of trying to pull the output high (toward a CMR failure) at the same time the LED current is being reduced. For this reason, the recommended LED drive circuit (Figure 12) places the current setting resistor in series with the LED cathode. Figure 17 is the AC equivalent circuit for Figure 12 during common mode transients. In this case, the LED current is not reduced during a  $+dV_{CM}/dt$  transient because the current flowing through the package capacitance is supplied by the power supply. During a  $-dV_{CM}/dt$  transient, however, the LED current is reduced by the amount of current flowing through  $C_{LEDN}$ . But, better CMR performance is achieved since the current flowing in  $C_{LEDO1}$  during a negative transient acts to keep the output low.

**Figure 15: LED Drive Circuit with Resistor Connected to LED Anode (Not Recommended)**

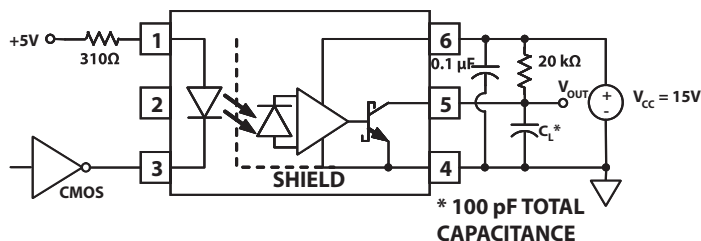


**Figure 16: AC Equivalent Circuit for Figure 15 During Common Mode Transients**

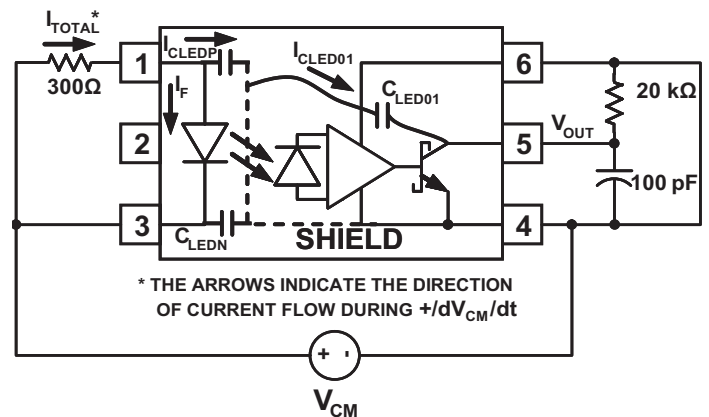
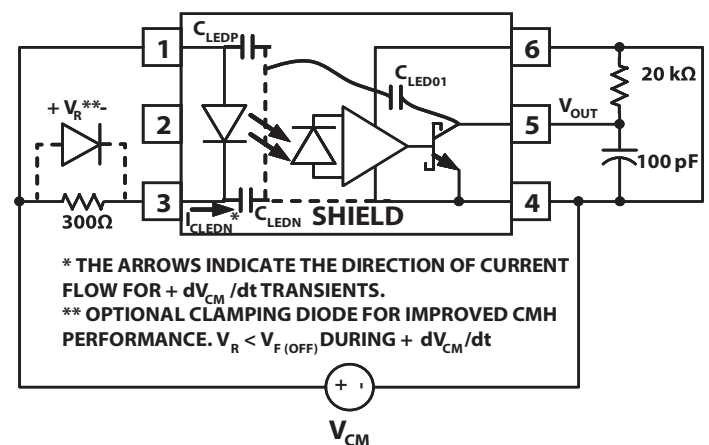


**Figure 17: AC Equivalent Circuit for Figure 12 During Common Mode Transients**



## CMR with the LED Off (CMRH)

A high CMR LED drive circuit must keep the LED off ( $V_F \leq V_{F(OFF)}$ ) during common mode transients. For example, during a  $+dV_{CM}/dt$  transient as shown in Figure 17, the current flowing through  $C_{LEDN}$  is supplied by the parallel combination of the LED and series resistor. As long as the voltage developed across the resistor is less than  $V_{F(OFF)}$ , the LED will remain off and no common mode failure will occur. Even if the LED momentarily turns on, the 100-pF capacitor from pins 5–4 will keep the output from dipping below the threshold. The recommended LED drive circuit (Figure 12) provides about 10V of margin between the lowest optocoupler output voltage and a 3V IPM threshold during a 15-kV/ $\mu$ s transient with  $V_{CM} = 1500V$ . Additional margin can be obtained by adding a diode in parallel with the resistor, as shown by the dashed line connection in Figure 17, to clamp the voltage across the LED below  $V_{F(OFF)}$ .

Because the open collector drive circuit, shown in Figure 18, cannot keep the LED off during a  $+dV_{CM}/dt$  transient, it is not desirable for applications requiring ultra high CMRH performance. Figure 19 is the AC equivalent circuit for Figure 18 during common mode transients. Essentially all the current flowing through  $C_{LEDN}$  during a  $+dV_{CM}/dt$  transient must be supplied by the LED. CMRH failures can occur at  $dv/dt$  rates where the current through the LED and  $C_{LEDN}$  exceeds the input threshold. Figure 20 shows an alternative drive circuit that does achieve ultra high CMR performance by shunting the LED in the off state.

**Figure 18: Not Recommended Open Collector LED Drive Circuit**

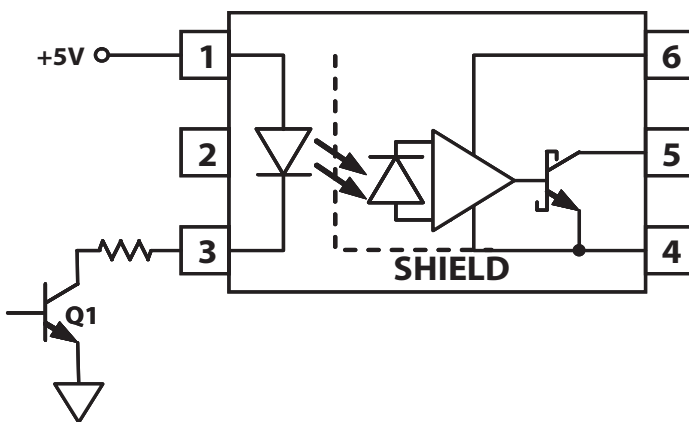


**Figure 19: AC Equivalent Circuit for Figure 18 During Common Mode Transients**

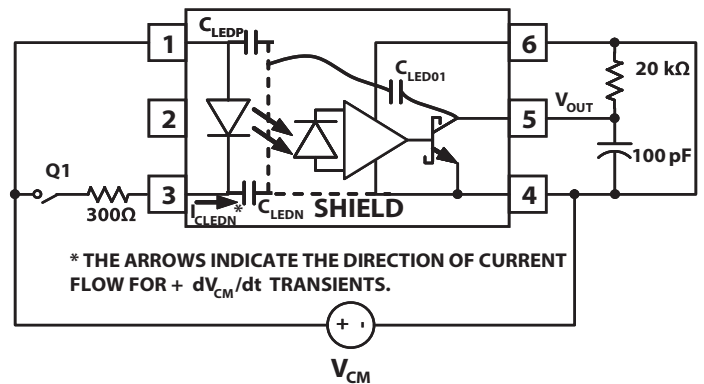
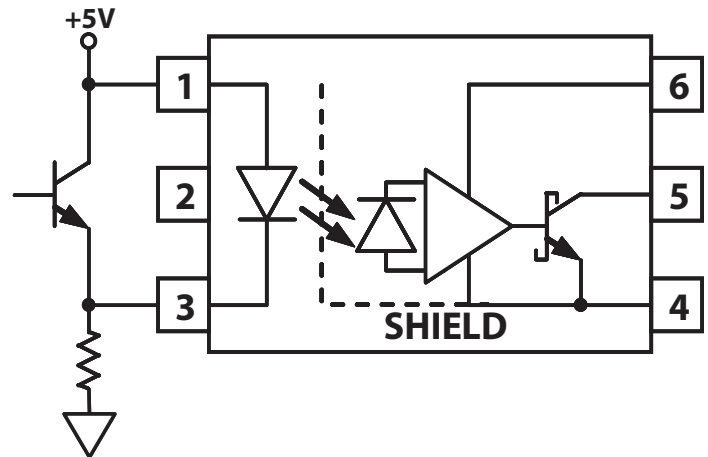


**Figure 20: Recommended LED Drive Circuit for Ultra High CMR**



## IPM Dead Time and Propagation Delay Specifications

The ACPL-P456/W456 includes a Propagation Delay Difference specification intended to help designers minimize “dead time” in their power inverter designs. Dead time is the time period during which both the high- and low-side power transistors (Q1 and Q2 in Figure 21) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices between the high- and low-voltage motor rails.

To minimize dead time, the designer must consider the propagation delay characteristics of the optocoupler as well as the characteristics of the IPM IGBT gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the IPM IGBT gate drive circuit can be analyzed in the same way), it is important to know the minimum and maximum turn-on ( $t_{PHL}$ ) and turn-off ( $t_{PLH}$ ) propagation delay specifications, preferably over the desired operating temperature range.

The limiting case of zero dead time occurs when the input to Q1 turns off at the same time that the input to Q2 turns on. This case determines the minimum delay between LED1 turn-off and LED2 turn-on, which is related to the worst-case optocoupler propagation delay waveforms, as shown in Figure 22. A minimum dead time of zero is achieved in

Figure 22 when the signal to turn on LED2 is delayed by ( $t_{PLH} \text{ max.} - t_{PHL} \text{ min.}$ ) from the LED1 turn-off. Note that the propagation delays used to calculate PDD are taken at equal temperatures since the optocouplers under consideration are typically mounted in close proximity to each other. (Specifically, previous equations are not the same as the  $t_{PLH} \text{ max.}$  and  $t_{PHL} \text{ min.}$ , over the full operating temperature range, specified in the data sheet.) This delay is the maximum value for the propagation delay difference specification, which is specified at 450 ns for the ACPL-P456/W456 over an operating temperature range of  $-40^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ .

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time occurs in the highly unlikely case where one optocoupler with the fastest  $t_{PLH}$  and another with the slowest  $t_{PHL}$  are in the same inverter leg. The maximum dead time in this case becomes the sum of the spread in the  $t_{PLH}$  and  $t_{PHL}$  propagation delays as shown in Figure 23. The maximum dead time is also equivalent to the difference between the maximum and minimum propagation delay difference specifications. The maximum dead time (due to the optocouplers) for the ACPL-P456/W456 is 600 ns ( $= 450 \text{ ns} - (-150 \text{ ns})$ ) over an operating temperature range of  $-40^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ .

Figure 21: Typical Application Circuit

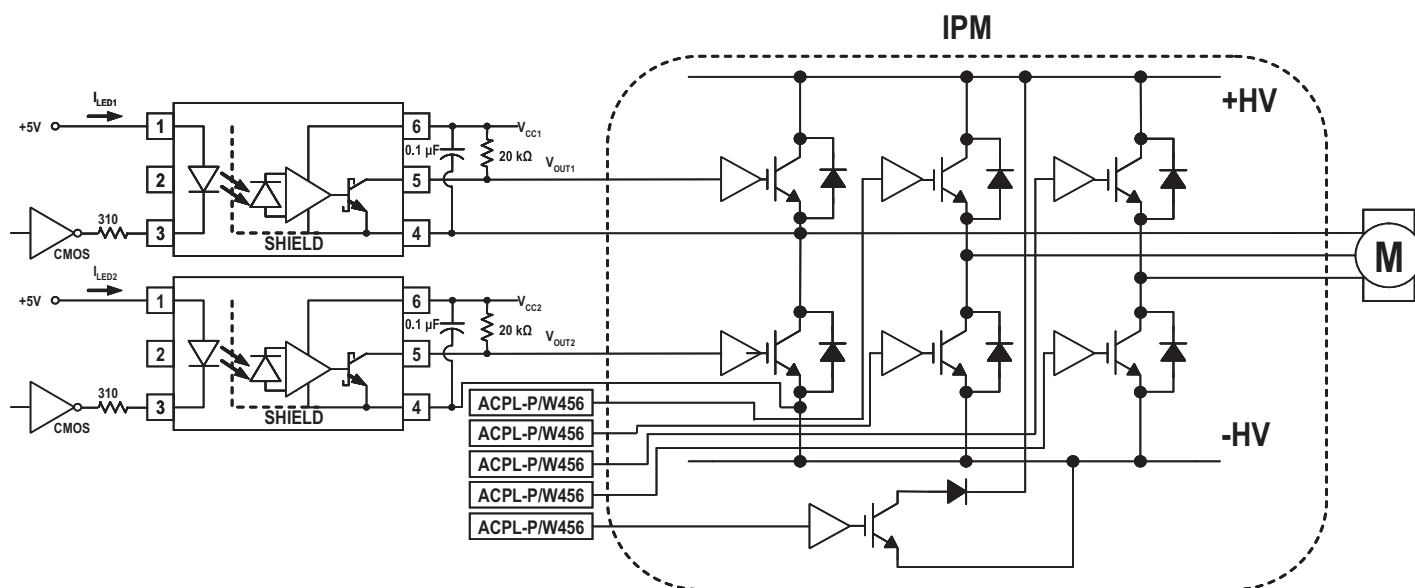
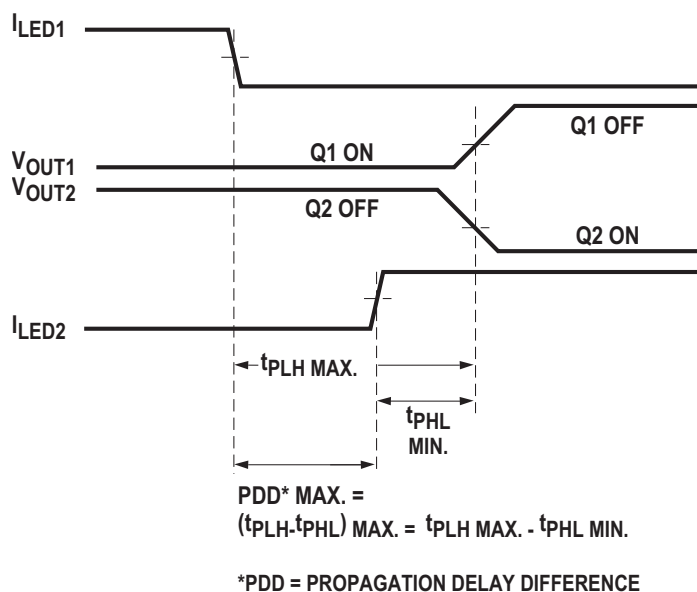
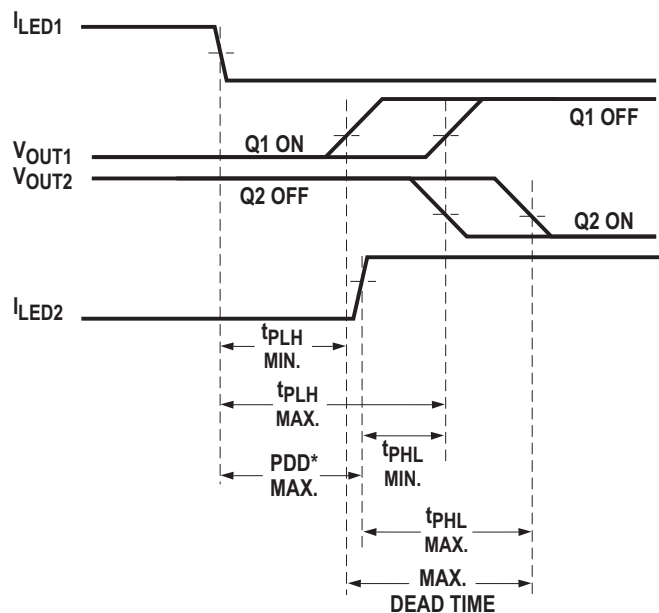


Figure 22: Minimum LED Skew for Zero Dead Time



NOTE: THE PROPAGATION DELAYS USED TO CALCULATE PDD ARE TAKEN AT EQUAL TEMPERATURES.

Figure 23: Waveforms for the Dead Time Calculation



MAXIMUM DEAD TIME (DUE TO OPTOCOUPLER)

$$\begin{aligned}
 &= (t_{PLH\ MAX.} - t_{PLH\ MIN.}) + (t_{PHL\ MAX.} - t_{PHL\ MIN.}) \\
 &= (t_{PLH\ MAX.} - t_{PHL\ MIN.}) - (t_{PLH\ MIN.} - t_{PHL\ MAX.}) \\
 &= PDD^*\ MAX. - PDD^*\ MIN.
 \end{aligned}$$

\*PDD = PROPAGATION DELAY DIFFERENCE

NOTE: THE PROPAGATION DELAYS USED TO CALCULATE THE MAXIMUM DEAD TIME ARE TAKEN AT EQUAL TEMPERATURES.

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