

AEDR-9930EA

Three-Channel Reflective Incremental Rotary Encoder Digital Output (397 LPI)



Description

The Broadcom® AEDR-9930EA is a three-channel reflective optical encoder. The selectable and programmable options available are three-channel digital differential A, B, and I outputs.

The AEDR-9930EA digital encoder mode offers two-channel (AB) quadrature digital outputs and a third channel digital index output. Being TTL compatible, the outputs of the AEDR-9930EA encoder can be interfaced with most signal processing circuitry. Therefore, the encoder provides easy integration and flexible design-in into existing systems.

The AEDR-9930EA encoder is designed to operate over a temperature range of -40°C to $+125^{\circ}\text{C}$ and is suitable for commercial, industrial, and automotive end applications.

The encoder houses an LED light source and photodetecting circuitry in a single package. The small size of 5.00 mm (L) \times 5.00 mm (W) \times 1.05 mm (H) allows the encoder to be used in a wide range of miniature commercial applications where size and space are primary concerns.

Features

- Digital output option: three-channel differential or TTL compatible; two-channel quadrature (AB) digital outputs for direction sensing and a third channel, index digital output
- Wide-selection built-in interpolator with 1x to 10x, 12x, 14x, 15x, 16x, 18x, 20x, 25x, 32x, 50x, 64x, 80x, 100x, 128x, 160x, 256x to 512x, and other user-programmable interpolation factors
- SPI programmable interpolator from 1x to 1024x
- Surface-mount leadless package: 5.0 mm (L) \times 5.0 mm (W) \times 1.05 mm (H)
- Operating voltage of 3.3V and 5.0V supply
- Built-in LED current regulation
- Wide operating temperature range from -40°C to $+125^{\circ}\text{C}$
- High encoding resolution: 397 LPI (lines per in.) or 15.63 LPmm (lines per mm)
- Qualified automotive standard AEC-Q100 Grade 1

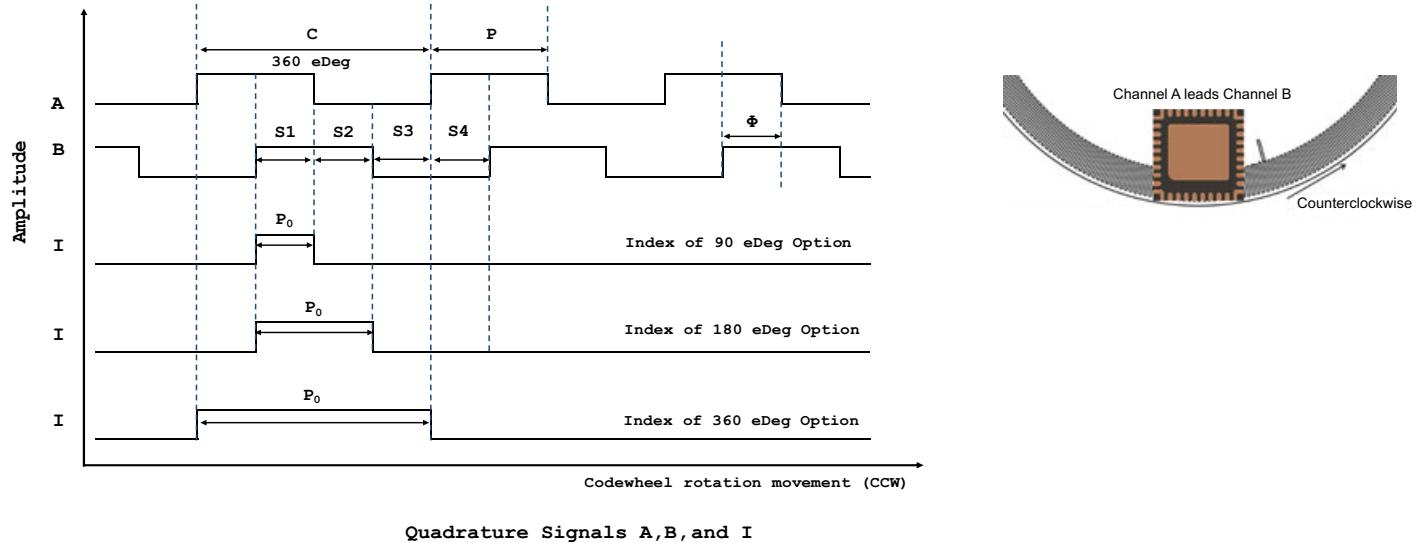
Applications

- Closed-loop stepper motors
- Small motors, actuators
- Industrial printers
- Robotics
- Card readers
- Pan-tilt-zoom (PTZ) cameras
- Portable medical equipment
- Optometric equipment
- Linear stages

Disclaimer: Except as expressly indicated in writing, the component is not designed or warranted to be suitable for use in safety-related applications where its failure or malfunction can reasonably be expected to result in injury, death, or severe equipment damage. Customers are solely responsible for determining the suitability of this product for its intended application and are solely liable for all loss, damage, expense, or liability in connection with such use.

Output Waveform

Figure 1: Sample Output Waveforms



Digital Parameter Definitions

Test	Parameter	Definition
Count	N	The number of bar and window pairs or counts per revolution (CPR) of the code wheel.
Cycle	C	360 electrical degrees ('e), 1 bar and window pair. One shaft rotation: 360 mechanical degrees, N cycles.
Cycle Error	ΔC	An indication of cycle uniformity. The difference between an observed shaft angle that gives rise to one electrical cycle and the nominal angular increment of $1/N$ of a revolution.
Pulse Width (Duty) Error	ΔP	The deviation, in electrical degrees, of the pulse width from its ideal value of $180^\circ e$.
State	S	The number of electrical degrees between a transition in the output of channel A and the neighboring transition in the output of channel B. There are four states per cycle, each nominally $90^\circ e$.
Phase	Φ	The number of electrical degrees between the center of the high state of channel A and the center of the high state of channel B. This value is nominally $90^\circ e$ for quadrature output.
Optical Radius	R_{OP}	The distance from the code wheel's center of rotation to the optical center (O.C.) of the encoder module.
Index Pulse Width	P_0	The number of electrical degrees that an index is high during one full shaft rotation.

Absolute Maximum Ratings

Parameter	Symbol	Value
Storage Temperature	T_S	−40°C to 150°C
Operating Temperature	T_A	−40°C to 125°C
Supply Voltage	V_{CC}	7V

NOTE:

1. Proper operation of the encoder cannot be guaranteed if the maximum ratings are exceeded.
2. Exposure to extreme light intensity (such as from flashbulbs or spotlights) can cause permanent damage to the device.
3. Remove Kapton tape only after the SMT reflow process and just before the final assembly. Take precautions to keep the encoder ASIC clean at all times.
4. Some particles might be present on the encoder ASIC surface. The presence of these particles does not degrade the performance of the encoder.

CAUTION! Take antistatic discharge precautions when handling the encoder to avoid damage, degradation, or both, induced by ESD.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Temperature	T_A	−40	25	125	°C	
Supply Voltage	V_{CC}	3.0	3.3	3.6	V	Ripple < 100 mV _{p-p}
		4.5	5	5.5		
Current	I_{CC}	—	70	125	mA	Dependent on the spatial position and rotation speed
Pin Current (All I/O Outputs)	I	−20	—	20	mA	
Maximum Output Frequency (External Pin Selectable)	F	—	—	0.2	MHz	At 1x interpolation
		—	—	0.4	MHz	At 2x interpolation
		—	—	0.8	MHz	At 4x interpolation
		—	—	1.6	MHz	At 8x interpolation
		—	—	3.2	MHz	At 16x interpolation
		—	—	4.0	MHz	At 32x interpolation
		—	—	4.0	MHz	At 64x interpolation
		—	—	4.0	MHz	At 128x interpolation
		—	—	4.0	MHz	At > 256x interpolation
Maximum Output Frequency (SPI Programmable)	F	—	—	4.0	MHz	At ≥ 20 x interpolation
Tangential Misalignment	E_T	—	—	± 0.5	mm	
Radial Misalignment (R_{OP} Dependent)	E_R	—	—	± 0.3	mm	Based on R_{OP} 5.21 mm 512 CPR = ± 0.30 mm 256 CPR = ± 0.20 mm 1000 CPR = ± 0.50 mm
Code Wheel Gap	G	0.45	0.75	1.05	mm	For ≥ 512 CPR
Specular Reflectance	R_f	60%	—	—	—	Reflective area
		—	—	5%	—	Nonreflective area

Power-Up Behavior

When the AEDR-9930EA is powered on, the A, B, and I digital outputs are invalid until after the initial first toggle state of either the Channel A or Channel B signal.

Encoder Pinout

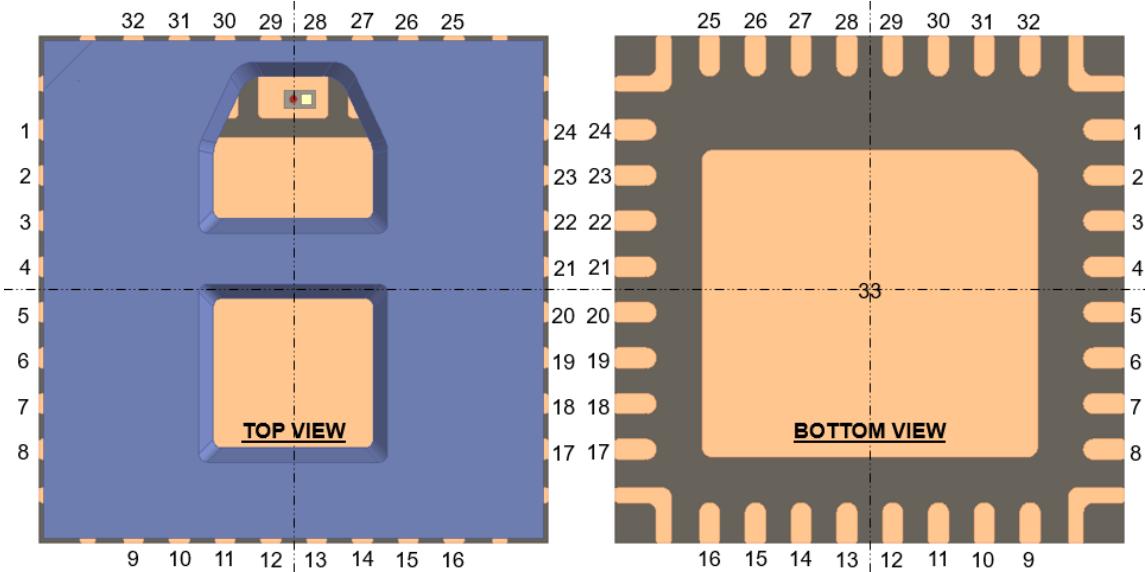


Table 1: AEDR-9930EA Pinout

Pin	Name ^a	Function
1	CH_A+	Digital A+
2	CH_A- / SPI_DIN	Digital A- / SPI Data In
3	VDD 5V	Digital Supply Voltage
4	VSSD	Digital Ground
5	CH_B+	Digital B+
6	CH_B- / SPI_CLK	Digital B- / SPI Clock
7	CH_I+ / SPI_DOUT	Digital I+ / SPI Data Out
8	CH_I- / CLK100K	Digital I- / CLK 100k
9	CAL_STAT	Calibration Status
10	N.C.	—
11	N.C.	—
12	N.C.	—
13	N.C.	—
14	N.C.	—
15	N.C.	—
16	N.C.	—
17	CAL	Autocalibration

a. N.C. = No connect.

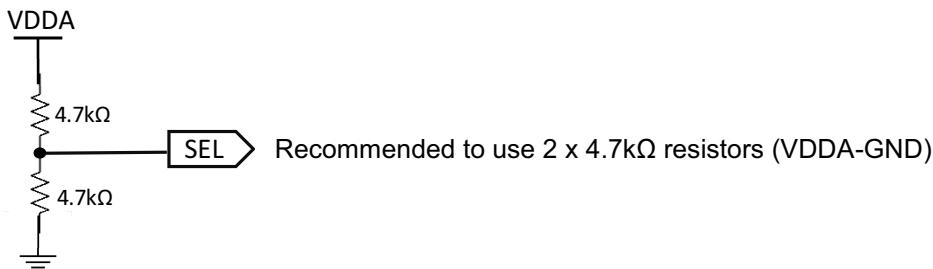
Pin	Name ^a	Function
18	INDEX_SEL	Index Selection
19	SEL1	Mode Selection 1
20	SEL2	Mode Selection 2
21	SEL3	Mode Selection 3
22	VSSA	Analog Ground
23	VDDA	Analog Supply Voltage
24	LED REG	LED Regulation
25	OP_STAT	Operation Status
26	N.C.	—
27	LED CATHODE	LED Cathode
28	LED ANODE	LED Anode
29	LED ANODE	LED Anode
30	N.C.	—
31	VSSA	Analog Ground
32	ERR_STAT	Error Status
33	VSSA	Analog Ground

Select Options – AEDR-9930EA Built-in Interpolation

No.	SEL1 ^a	SEL2 ^a	SEL3 ^a	Interpolation Factor	IND_SEL	Index
1	Low	Low	Low	1X	Low	Interpolation 1X - Index Gated 90°
					High	Interpolation 1X - Index Gated 180°
					Open	Interpolation 1X - Index Raw (Ungated)
2	High	Low	Low	2X	Low	Interpolation 2X - Index Gated 90°
					High	Interpolation 2X - Index Gated 180°
					Open	Interpolation 2X - Index Gated 360°
3	Open	Low	Low	3X	Low	Interpolation 3X - Index Gated 90°
					High	Interpolation 3X - Index Gated 180°
					Open	Interpolation 3X - Index Gated 360°
4	Low	High	Low	4X	Low	Interpolation 4X - Index Gated 90°
					High	Interpolation 4X - Index Gated 180°
					Open	Interpolation 4X - Index Gated 360°
5	High	High	Low	5X	Low	Interpolation 5X - Index Gated 90°
					High	Interpolation 5X - Index Gated 180°
					Open	Interpolation 5X - Index Gated 360°
6	Open	High	Low	6X	Low	Interpolation 6X - Index Gated 90°
					High	Interpolation 6X - Index Gated 180°
					Open	Interpolation 6X - Index Gated 360°
7	Low	Open	Low	7X	Low	Interpolation 7X - Index Gated 90°
					High	Interpolation 7X - Index Gated 180°
					Open	Interpolation 7X - Index Gated 360°
8	High	Open	Low	8X	Low	Interpolation 8X - Index Gated 90°
					High	Interpolation 8X - Index Gated 180°
					Open	Interpolation 8X - Index Gated 360°
9	Open	Open	Low	9X	Low	Interpolation 9X - Index Gated 90°
					High	Interpolation 9X - Index Gated 180°
					Open	Interpolation 9X - Index Gated 360°
10	Low	Low	High	10X	Low	Interpolation 10X - Index Gated 90°
					High	Interpolation 10X - Index Gated 180°
					Open	Interpolation 10X - Index Gated 360°
11	High	Low	High	12X	Low	Interpolation 12X - Index Gated 90°
					High	Interpolation 12X - Index Gated 180°
					Open	Interpolation 12X - Index Gated 360°
12	Open	Low	High	14X	Low	Interpolation 14X - Index Gated 90°
					High	Interpolation 14X - Index Gated 180°
					Open	Interpolation 14X - Index Gated 360°
13	Low	High	High	15X	Low	Interpolation 15X - Index Gated 90°
					High	Interpolation 15X - Index Gated 180°
					Open	Interpolation 15X - Index Gated 360°

No.	SEL1 ^a	SEL2 ^a	SEL3 ^a	Interpolation Factor	IND_SEL	Index
14	High	High	High	16X	Low	Interpolation 16X - Index Gated 90°
					High	Interpolation 16X - Index Gated 180°
					Open	Interpolation 16X - Index Gated 360°
15	Open	High	High	18X	Low	Interpolation 18X - Index Gated 90°
					High	Interpolation 18X - Index Gated 180°
					Open	Interpolation 18X - Index Gated 360°
16	Low	Open	High	20X	Low	Interpolation 20X - Index Gated 90°
					High	Interpolation 20X - Index Gated 180°
					Open	Interpolation 20X - Index Gated 360°
17	High	Open	High	25X	Low	Interpolation 25X - Index Gated 90°
					High	Interpolation 25X - Index Gated 180°
					Open	Interpolation 25X - Index Gated 360°
18	Open	Open	High	32X	Low	Interpolation 32X - Index Gated 90°
					High	Interpolation 32X - Index Gated 180°
					Open	Interpolation 32X - Index Gated 360°
19	Low	Low	Open	50X	Low	Interpolation 50X - Index Gated 90°
					High	Interpolation 50X - Index Gated 180°
					Open	Interpolation 50X - Index Gated 360°
20	High	Low	Open	64X	Low	Interpolation 64X - Index Gated 90°
					High	Interpolation 64X - Index Gated 180°
					Open	Interpolation 64X - Index Gated 360°
21	Open	Low	Open	80X	Low	Interpolation 80X - Index Gated 90°
					High	Interpolation 80X - Index Gated 180°
					Open	Interpolation 80X - Index Gated 360°
22	Low	High	Open	100X	Low	Interpolation 100X - Index Gated 90°
					High	Interpolation 100X - Index Gated 180°
					Open	Interpolation 100X - Index Gated 360°
23	High	High	Open	128X	Low	Interpolation 128X - Index Gated 90°
					High	Interpolation 128X - Index Gated 180°
					Open	Interpolation 128X - Index Gated 360°
24	Open	High	Open	160X	Low	Interpolation 160X - Index Gated 90°
					High	Interpolation 160X - Index Gated 180°
					Open	Interpolation 160X - Index Gated 360°
25	Low	Open	Open	256X	Low	Interpolation 256X - Index Gated 90°
					High	Interpolation 256X - Index Gated 180°
					Open	Interpolation 256X - Index Gated 360°
26	High	Open	Open	512X	Low	Interpolation 512X - Index Gated 90°
					High	Interpolation 512X - Index Gated 180°
					Open	Interpolation 512X - Index Gated 360°
27	Open	Open	Open	SPI Mode	Low	SPI Mode: Program Selection
					High	SPI Mode: Output Enabled

a. Open selection must be connected to the middle of a voltage divider circuit (see [Figure 2](#)).

Figure 2: Example of Voltage Divider Circuit

The preceding digital interpolation factor is used with the following equations to cater to various rotational speed (RPM) and count per revolution (CPR).

$$\text{RPM} = (\text{Count Frequency} \times 60) / \text{CPR}$$

The CPR (at 1X interpolation) is based on the following equation, which is dependent on the radius of operation (R_{OP}).

$$\text{CPR} = \text{LPI} \times 2\pi \times R_{OP} \text{ (in.)} \text{ or } \text{CPR} = \text{LPmm} \times 2\pi \times R_{OP} \text{ (mm)}$$

NOTE: $\text{LPmm} = \text{LPI} / 25.4$

Programmable Select Options

The AEDR-9930EA digital encoder is programmable via the SPI with an interpolation factor from 1x to 1024x.

1. Configure external selection to SPI Mode: Program Selection.
2. For signals output after configuration, set external selection to SPI Mode: Output Enabled.

SPI Communication Pinout (for Interpolation and Index Width Selection)

Table 2: Encoder Calibration Related Pinout

Pin	Name	Function
7	SPI DOUT	SPI Data Output
2	SPI DIN	SPI Data Input
6	SPI CLK	SPI Clock

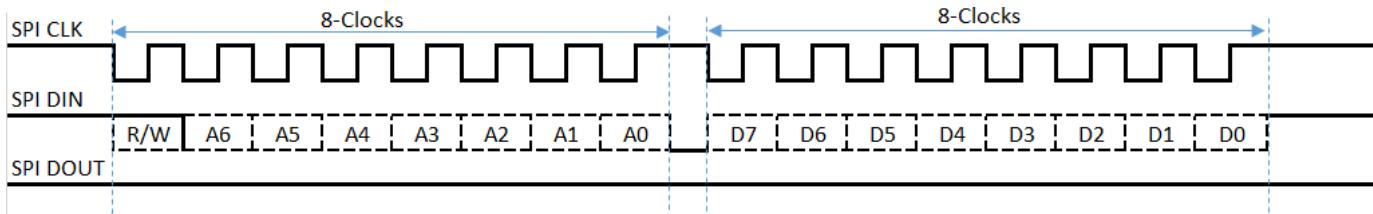
SPI Read and Write Timing Diagram (Maximum Clock Frequency: 1 MHz)

Table 3: SPI Read and Write Memory Map

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	Address[6:0]										Data[7:0]				
Write	1	Address[6:0]										Data[7:0]				

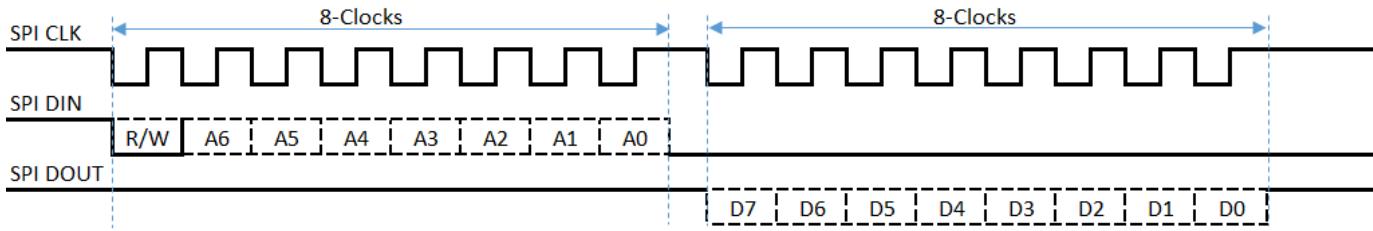
SPI Write: <Write Command = 1><7bits address><8bits data>

Figure 3: SPI Write Timing Diagram



SPI Read: <Read Command = 0><7bits address>

Figure 4: SPI Read Timing Diagram



Unlock Sequence

1. Write to SPI address 0x10 with the value AB (hex) to unlock Level 1.
2. Write to SPI address 0x14 with the value 00 (hex) to go to Page 0.

Program Memory

1. Write to SPI address 0x11 with the value A1 (hex) to program memory.

Interpolation Settings and Programming

1. Write to SPI address 0x0B and 0x0C with the value shown in the following tables.
2. After finalizing the CPR settings, write to SPI address 0x11 (hex) with the value A1 (hex) before proceeding to program the AEDR-9930EA.

Table 4: List of Available Interpolation and Index Values in the AEDR-9930EA

Byte Address [Hex]	Page	Bit								Note
		7	6	5	4	3	2	1	0	
0x0B				lwidth_digital[1:0]					INT[10:8]	
0x0C					INT[7:0]					INT: 0-1024

Interpolation INT	0x0B (Hex)	0x0C (Hex)
1	Bit 0 = 0	01
2	.	02
.	.	.
.	.	.
10	.	0A
11	.	0B
.	.	.
.	.	.
255	Bit 0 = 0	FF
256	Bit 0 = 1	00
257	Bit 0 = 1	01
.	.	.
.	.	.
512	Bit 1 = 1	00
.	.	.
.	.	.
1024	Bit 2 = 1	00

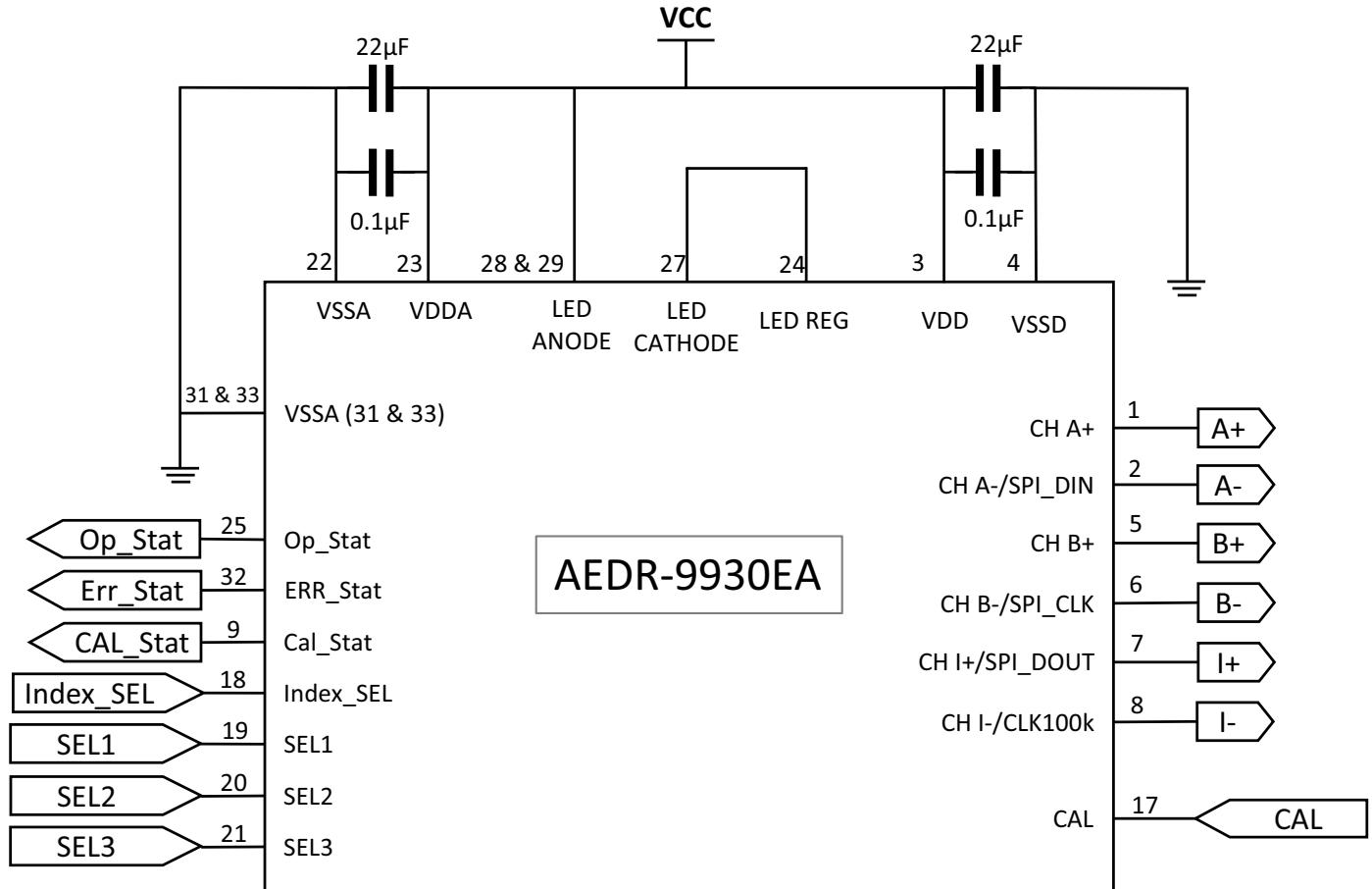
lwidth_Digital	IndexWidth
00	90°
01	180°
10	N/A
11	360°

Recommended Setup for the Power Supply Pins and General Routing

VDDA, VDD, and the respective grounds (VSSA and VSSD) are to be connected separately as shown in [Figure 5](#). Be sure to follow these schematic design rules:

- Use a pair of 22- μ F and 0.1- μ F capacitors as a bypass on VDD and VDDA. Place them in parallel as close as possible to the encoder ASIC package, in between the power and ground pins.
- Design separate VDD and VDDA traces.
- Minimize trace or cable length where possible.

Figure 5: Reference Schematic Diagram for AEDR-9930EA



NOTE:

1. Pin 33 is the center pad of the package and is labeled VSSA.
2. See the [Select Options – AEDR-9930EA Built-in Interpolation](#) table for SEL1, SEL2, SEL3, and IND_SEL configurations.
3. VDDA and VDD must be the same voltage level.
4. VSSA and VSSD must be connected together.
5. Op_Stat, Err_Stat, and Cal_Stat are encoder status outputs. Do not use the outputs to directly drive an LED. Do not connect the pins if they will not be used.
6. Place a weak pull-low onto the CAL pin.

Autocalibration Process

The AEDR-9930EA has a built-in autocalibration process that can be triggered on power-up by shorting the CAL pad to VDDA or VDD. The purpose of the calibration process is to align the center of the Index signal to the center of the Channel B signal. The misalignment of the Index signal is due to potential spatial misalignment of the encoder ASIC to the code wheel after assembly.

Perform the autocalibration process even if the A, B, and I signals appear normal at the first power-on after the encoder assembly. The autocalibration process helps to optimize the internal encoder ASIC settings, which enhances reliability and performance.

Autocalibration steps are as follows:

1. Spin the motor at a rotation speed between 500 rpm to 1500 rpm.
2. Short the CAL pad to the VDDA or VDD line. Use a high-value resistor such as 4.7 kΩ or 5.6 kΩ to do the shorting.
3. Turn on the power to the encoder. This will trigger the ASIC to start the autocalibration process.
4. Wait for at least 5 seconds. The Ch B+ state will change to high if the autocalibration is successful. Both the Ch A+ state and the Ch B+ state will change to high if the autocalibration process is unsuccessful. If the autocalibration is unsuccessful, check the spatial alignment between the encoder ASIC (PCB) and the code wheel and repeat Step 1 to 4.
5. Remove the short between CAL (pin 17) to VDDA or VDD. Perform a power cycle, and the encoder ASIC will function as normal.

Table 5: Encoder Autocalibration Status Based on Pad State

Pad	CAL (Pin 17)	A+	B+	I+	Status
Pad State	H	L	L	L	Autocalibrating
	H	H	L	L	Incremental autocalibration complete
	H	L	H	L	Incremental and index autocalibration complete
	H	H	H	L	Autocalibration error

Table 6: LED Status (LED Pins)

Pad	Op_Stat	CAL_Stat	ERR_Stat	Status
Pad State	L	Pulsing (500 ms)	L	Autocalibrating
	L	H	L	Autocalibration complete
	L	L	L	Autocalibration incomplete or error

Status Pin States (LED Indicators)

Pin	Power-Up from t = 0	Encoder Ready	Autocalibrating	Autocalibration Done	Autocalibration Error	LED_ERROR ^a	LED_ERROR ^b
Op_Stat	L	H	L	L	L	L	L
Cal_Stat	L	L	Pulsing (500 ms)	H	L	L	L
Err_Stat	L	L	L	L	L	H	Pulsing (500 ms)

a. No pulsing signal indicates a maximum LED current state (off-scale/no window bar).

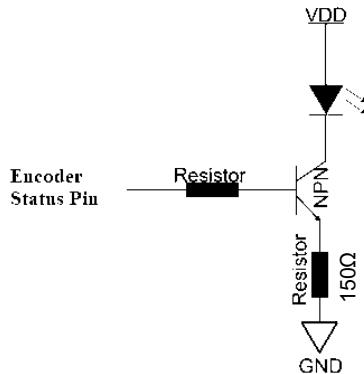
b. Early warning on high LED current but signal is normal.

NOTE:

1. The status pin serves as an output signal and is *not* intended to drive or sink current.
2. The ABI signal state when LED_ERROR is triggered (off-scale/no window bar) is as follows:

I/O	A+	A-	B+	B-	I+	I-
Pad State	H	L	H	L	L	H

Figure 6: Status Pin Diagram



NOTE:

1. H = High (VDD)
2. L = Low (GND)

Digital Signal Characteristics (Code Wheel of R_{OP} at 5.21 mm, 512 CPR)

Table 7: Typical Channel A and Channel B Signal Dynamic Performance over Different Interpolation Values

Parameter	Symbol	Dynamic Performance ^a								Unit
		Typical ^b								
Interpolation Factor		1X	2X	4X	8X	16X	32X	64X	128X	
Cycle Error	ΔC	± 7	± 8	± 9	± 9	± 11	± 13	± 16	± 19	$^{\circ}\text{e}$
Pulse Width (Duty) Error	ΔP	± 4	± 4	± 5	± 5	± 8	± 11	± 13	± 15	$^{\circ}\text{e}$
Phase Error	$\Delta\phi$	± 1	± 2	± 2	± 3	± 4	± 6	± 8	± 9	$^{\circ}\text{e}$
State Error	ΔS	± 2	± 2	± 3	± 4	± 5	± 10	± 13	± 13	$^{\circ}\text{e}$
Index Pulse Width (Gated 90°)	P_O	90								$^{\circ}\text{e}$
Index Pulse Width (Gated 180°)	P_O	180								$^{\circ}\text{e}$
Index Pulse Width (Gated 360°)	P_O	N/A	360							$^{\circ}\text{e}$
Index Pulse Width (Raw Ungated)	P_O	330	N/A							$^{\circ}\text{e}$

a. The optimal performance of the encoder depends on the motor and system setup condition of the individual customer.

b. Typical values represent the average value of the encoder performance based on the factory setup conditions at 2-MHz frequency for ≥ 16 interpolations.

Electrical Characteristics

Characteristics over recommended operating conditions at 25°C.

Table 8: Typical Channel A and Channel B Signal Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
High Level Output Voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -20 \text{ mA}$
Low Level Output Voltage	V_{OL}	—	—	0.4	V	$I_{OH} = +20 \text{ mA}$
Output Current per Channel, I_{out}	I_O	—	—	20	mA	
Rise Time	t_r	—	< 50	—	ns	$CL \leq 50 \text{ pF}$
Fall Time	t_f	—	< 50	—	ns	

Code Wheel Characteristics

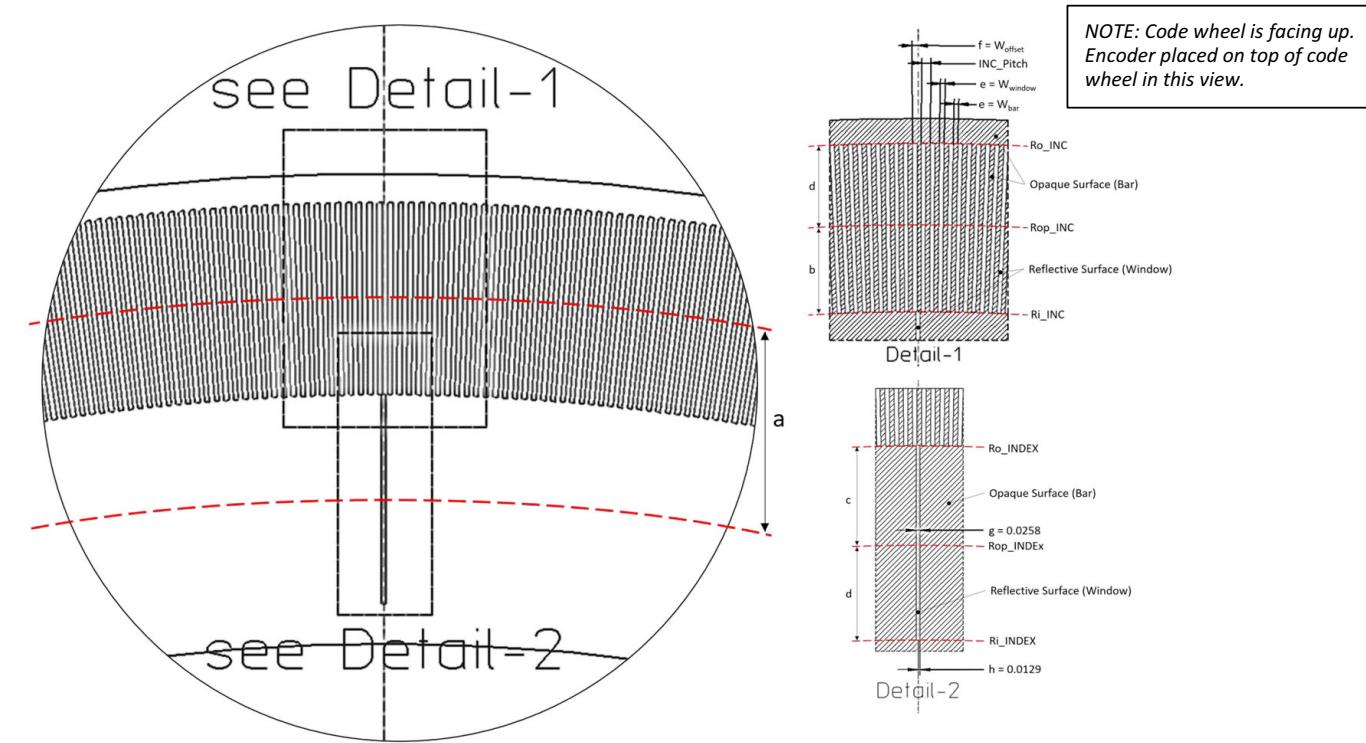
Characteristics are based on a Broadcom-qualified code wheel supplier. Contact Broadcom for information regarding qualified reflective code wheel suppliers.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Specular Reflectance	R_f	60%	—	—	—	Reflective area
		—	—	5%	—	Nonreflective area
LED Peak Wavelength	λ_p	—	853	—	nm	

Code Wheel Design Guidelines

- The window tracks are reflective surfaces.
- The bar tracks are opaque surfaces.
- The incremental window and bar tracks are trapezoidal.
- The number of incremental window and bar tracks depends on the CPR.
- The incremental window and bar tracks have the same width value.
- There is an offset between the incremental window tracks and the index window track.
- There is only one index window track.
- The index window track is rectangular.
- The width of the index window track is 0.0258 mm.

Figure 7: Code Wheel Design



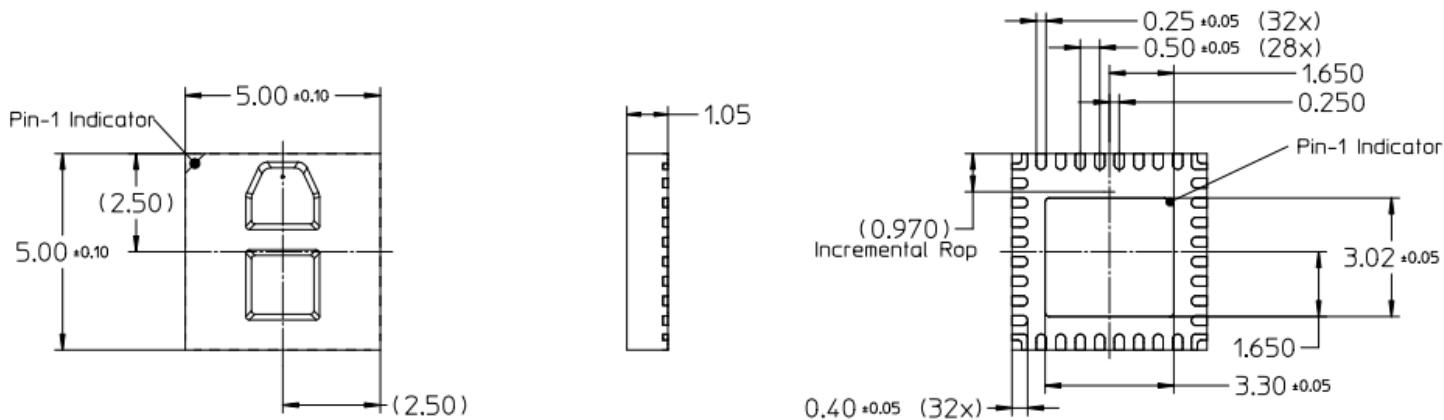
Dimension	Formula	397 LPI
a (mm)	$R_{OP_INC} - R_{OP_INDEX}$	1.2625
b (mm)	$R_{OP_INC} - R_{I_INC}$	0.5788
c (mm)	$R_{O_INDEX} - R_{OP_INDEX}$	0.6837
d (mm)	$R_{O_INC} - R_{OP_INC}$ or $R_{OP_INDEX} - R_{I_INDEX}$	0.6500
e (°)	$(360/CPR)/2$	—
f (°)	$1.25 \times e$	—
g (mm)	—	0.0258
h (mm)	—	0.0129

Code Wheel Design Example

The following demonstrates a code wheel design for 397 LPI at 1250 CPR.

Determine R_{OP_INC} : $(25.4/396.875) \times (1250/2\pi) \approx 12.7324$ mm
 Determine R_{OP_INDEX} : $12.7324 - 1.2625 = 11.4699$ mm
 Determine R_{O_INC} : $12.7324 + 0.65 = 13.3824$ mm
 Determine R_{I_INC} : $12.7324 - (0.5788) = 12.1536$ mm
 Determine R_{O_INDEX} : $11.4699 + (1.2625 - 0.5788) = 12.1536$ mm
 Determine R_{I_INDEX} : $11.4699 - 0.65 = 10.8199$ mm
 Determine W_{window} and W_{bar} : $(360/1250) / 2 = 0.144^\circ$
 Determine W_{offset} : $1.25 \times 0.144 = 0.180^\circ$

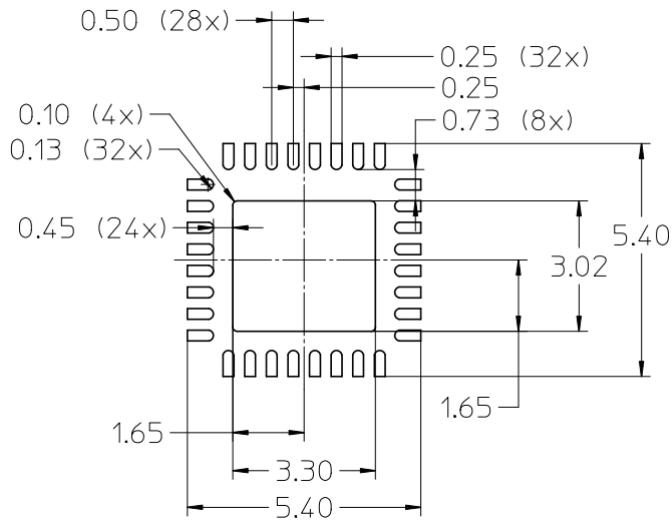
Package Outline Drawing



NOTE:

1. All dimensions are in millimeters (mm).
2. Unless otherwise specified, tolerance is $x.x \pm 0.15$ mm.

Recommended PCB Land Pattern



NOTE:

1. All dimensions are in millimeters (mm).
2. Unless otherwise specified, tolerance is $x.x \pm 0.05$ mm.

Encoder Placement Orientation, Position, and Direction of Movement

The AEDR-9930EA is designed with both the emitter and detector die placed in parallel to the code wheel window/bar orientation. The encoder package is mounted on top facing down onto the code wheel. When properly aligned, the detector side will be closer to the center of the code wheel than the emitter.

The optical center of the encoder package must be aligned tangential to the code wheel's R_{OP} . The optimal gap setting recommended is 0.75 mm, with the range of 0.45 mm to 1.05 mm, based on 512 CPR.

Channel A leads Channel B when the code wheel rotates counterclockwise, and Channel B leads Channel A when the code wheel rotates clockwise.

Figure 8: Top-Down View of AEDR-9930EA with Respect to Code Wheel Positioning

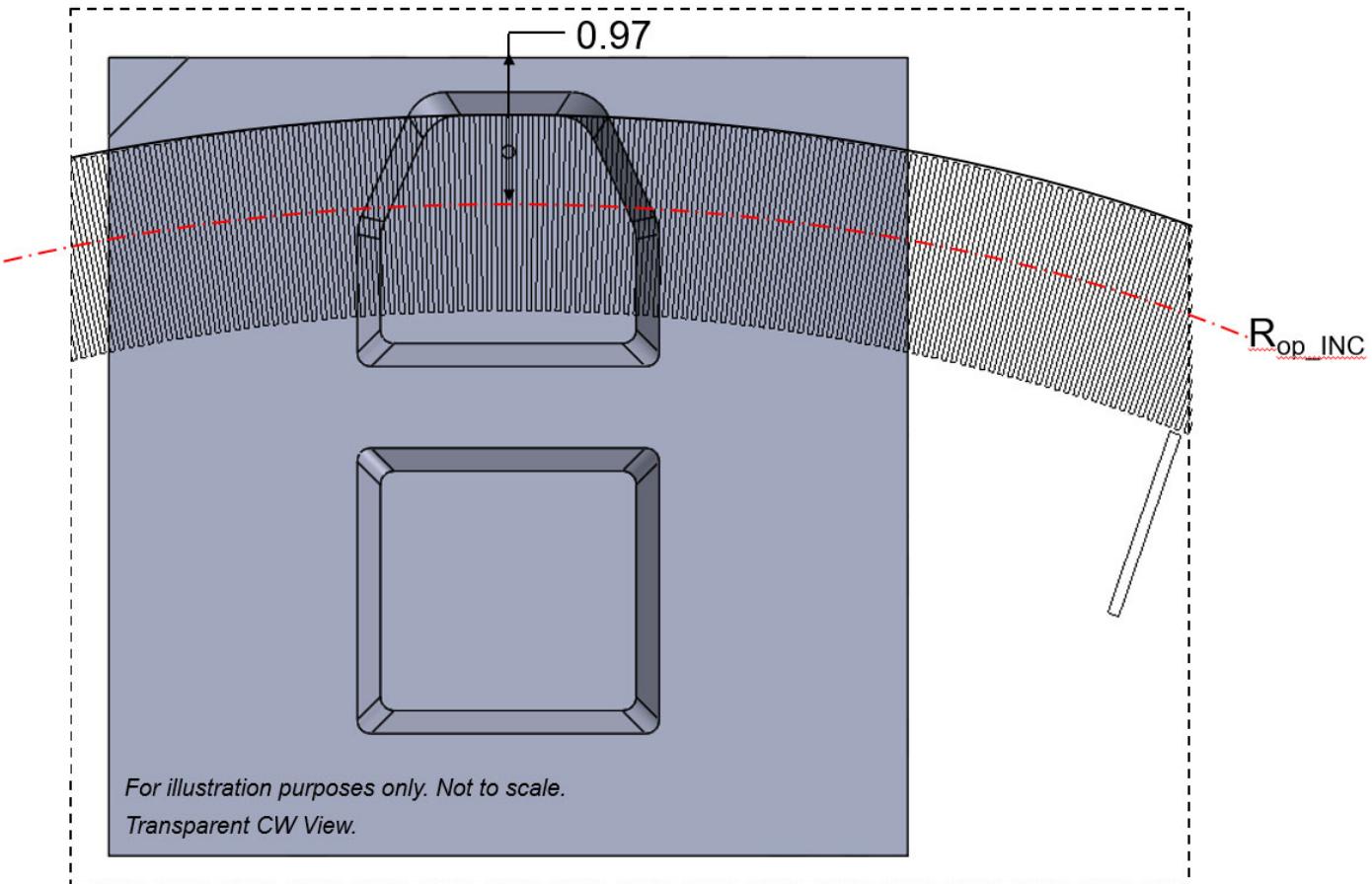
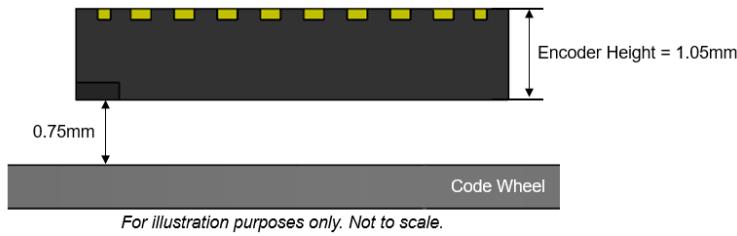
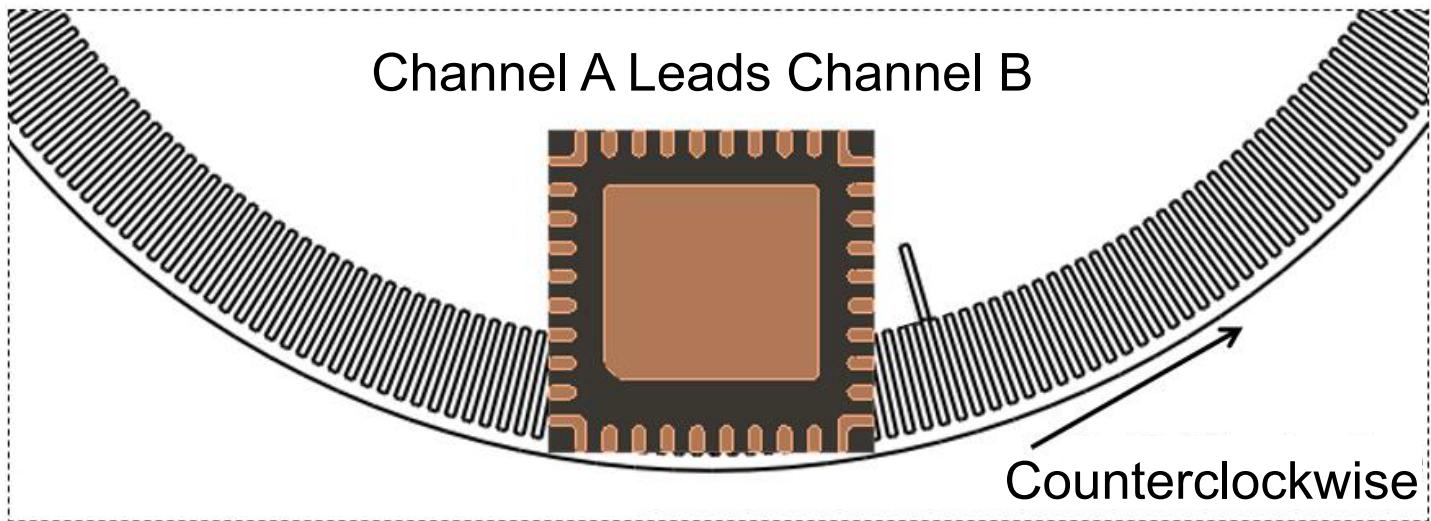
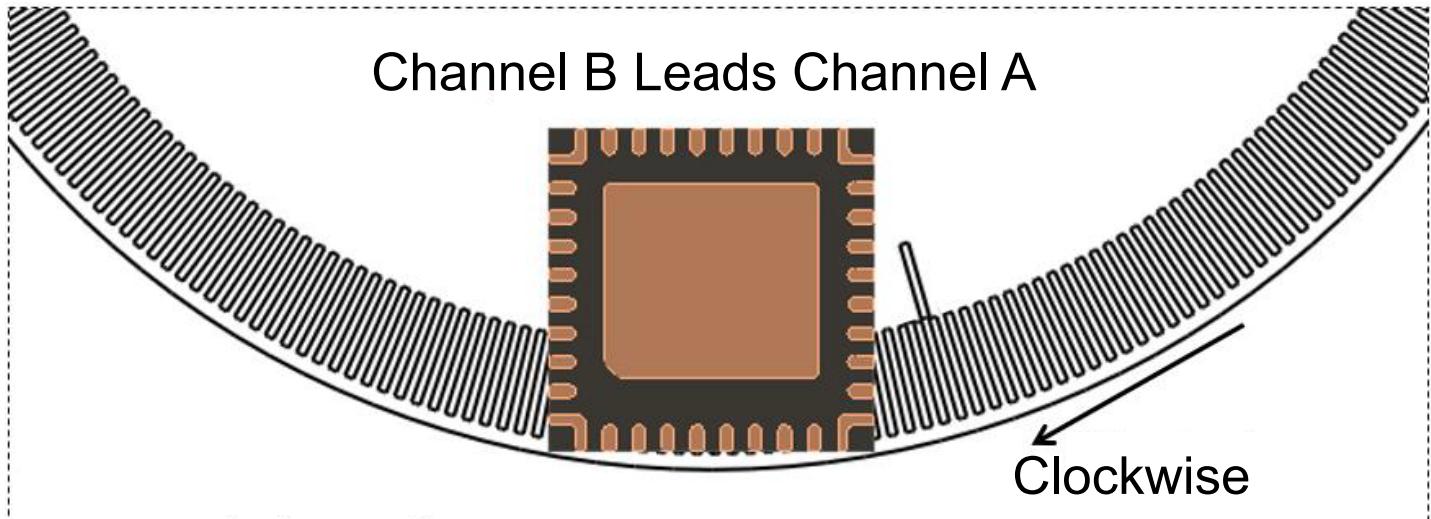


Figure 9: Channel A and Channel B Signal Output Sequence with Respect to Code Wheel Rotational Direction



NOTE: Drawings are for illustration purposes only and are not to scale.

Moisture Sensitivity Level

The AEDR-9930EA package is qualified to moisture sensitive level 3 (MSL 3). Precaution is required to handle this moisture sensitive product to ensure the reliability of the product.

Storage before use:

- An unopened moisture barrier bag (MBB) can be stored at $< 40^{\circ}\text{C}/90\% \text{ RH}$ for 12 months.
- Open the MBB just prior to assembly.

Control after opening the MBB:

- The encoder that will be subjected to reflow solder must be mounted within 168 hours of exposure to factory conditions of $< 30^{\circ}\text{C}/60\% \text{ RH}$.

Control for unfinished reel:

- Store a sealed MBB with desiccant or desiccators at $< 5\% \text{ RH}$.

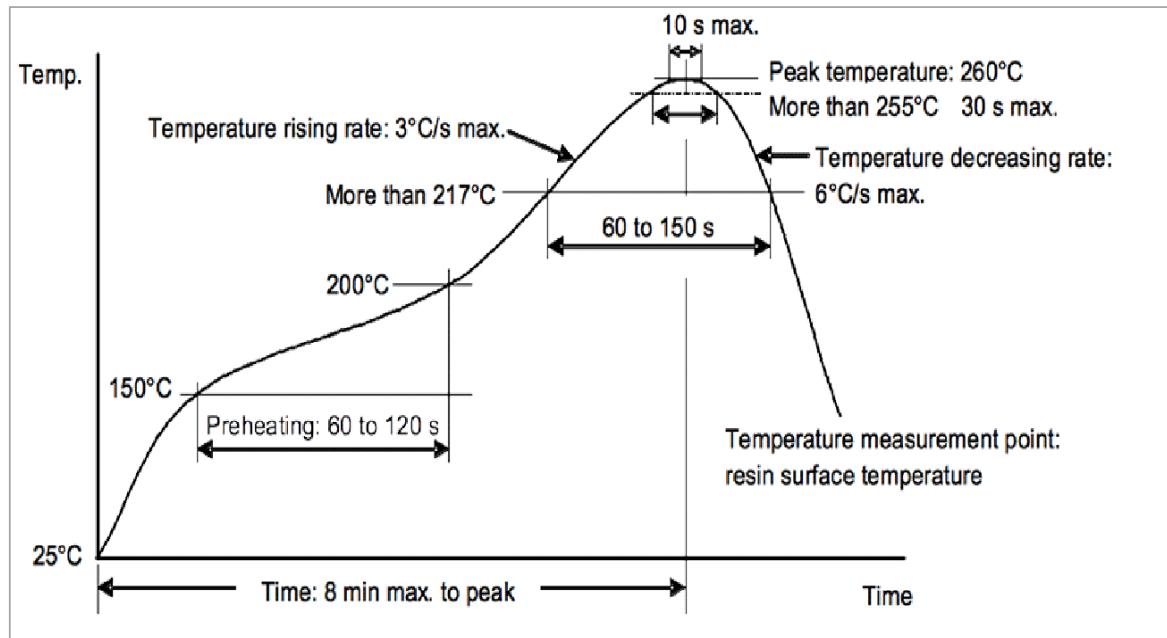
Baking is required if the following conditions exist:

- The humidity indicator card (HIC) is $> 10\%$ when read at $23^{\circ}\text{C} \pm 5^{\circ}\text{C}$.
- The encoder floor life exceeds 168 hours after opening the moisture barrier bag.

Recommended baking condition:

- $60^{\circ}\text{C} \pm 5^{\circ}\text{C}$ for 20 hours (tape and reel) or $125^{\circ}\text{C} \pm 5^{\circ}\text{C}$ for 8 hours (loose units).

Figure 10: Typical Lead-Free Solder Reflow Profile



CAUTION! Use care when handling the encoder ASIC because it is a sensitive optical device. Remove the protective Kapton tape only after the reflow process and just before the final assembly.

Tape and Reel Information

Figure 11: AEDR-9930EA Carrier Tape Dimensions

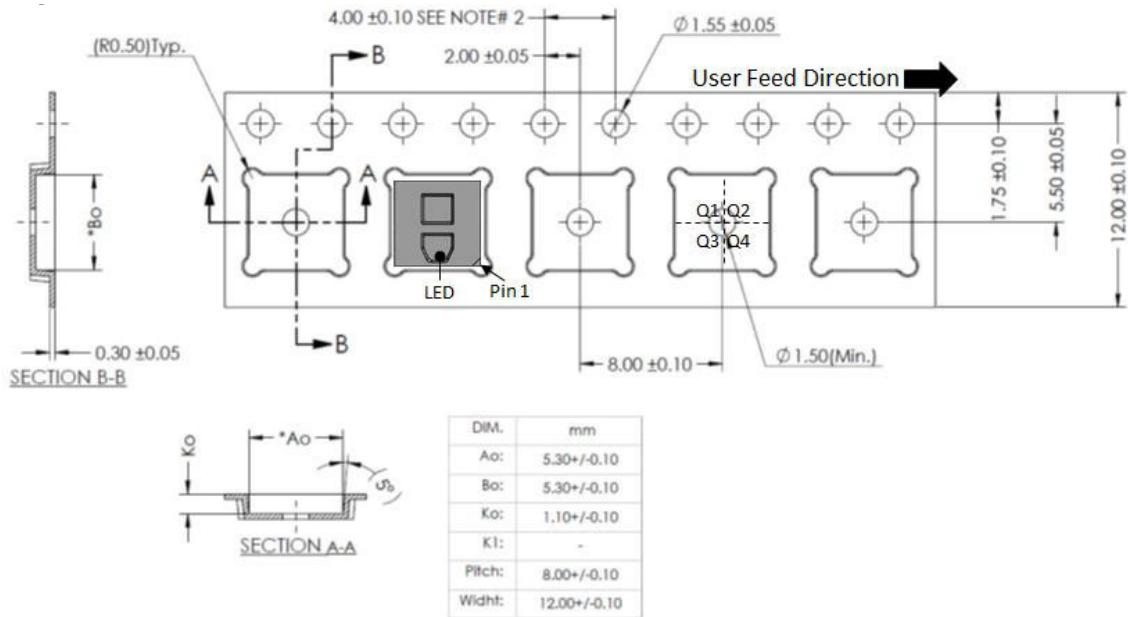
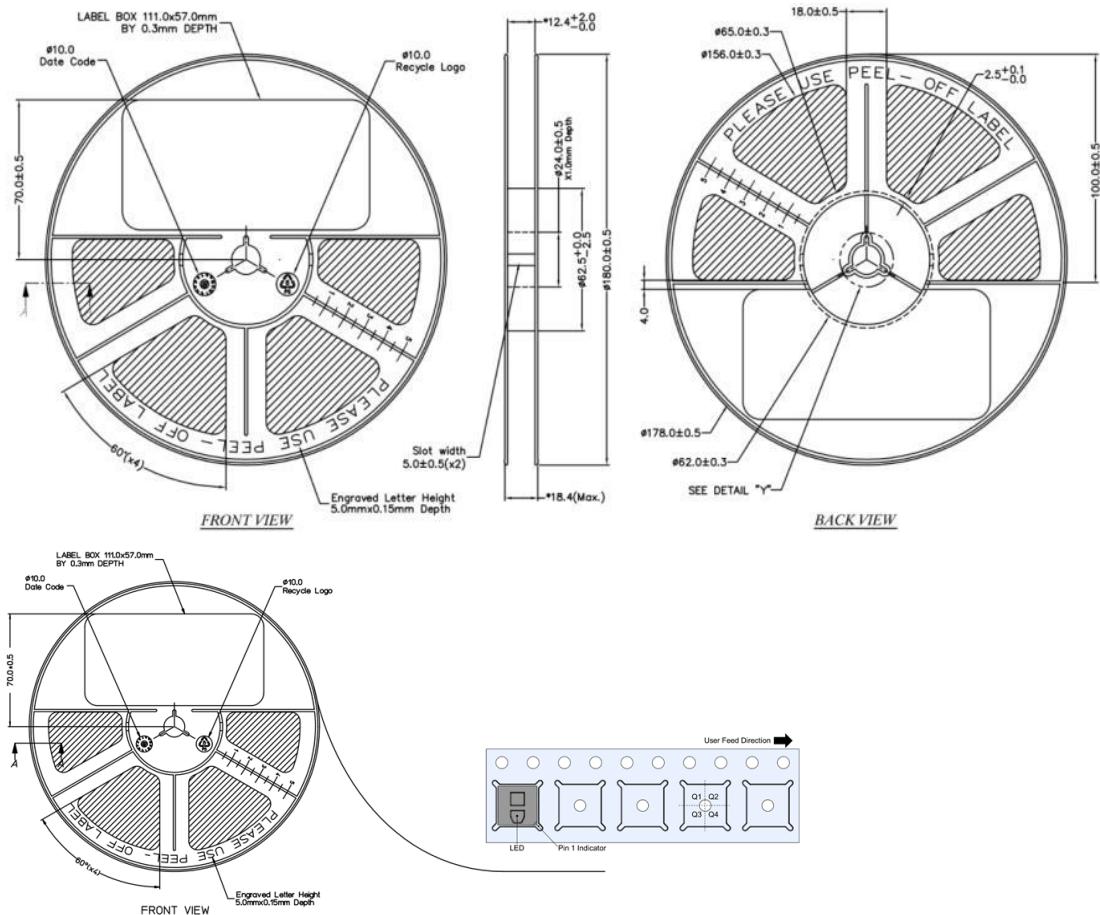


Figure 12: AEDR-9930EA Reel Dimensions and Orientation



Ordering Information

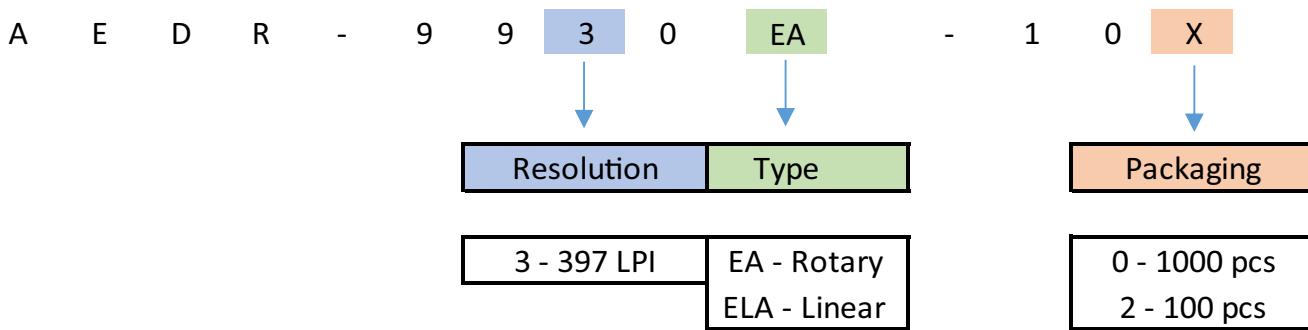


Table 9: Relevant Part Numbers and Ordering Information

Ordering Information	Type
AEDR-9930EA-100	AEDR-9930EA, 397 LPI Incremental Rotary Encoder, Tape and Reel, 1000 pieces
AEDR-9930EA-102	AEDR-9930EA, 397 LPI Incremental Rotary Encoder, Tape and Reel, 100 pieces

NOTE: For applications that require a linear encoder or off-scale-to-on-scale autocalibration, refer to the AEDR-9930ELA data sheet.

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