USER GUIDE

UG532: Skyworks Saturn Evaluation Platform

Features

- Supported products:
  - SKY69101
  - SKY69002/01
  - SKY63103/02/01
- All products feature a 64-LGA package with similar pinouts
- Skyworks ClockBuilder® Pro software for Windows® makes configuration easy
- USB cable and 5 V dc adapter are provided in the kit
- Flexible power tree allows user to configure power to the device
- On-board power monitors to evaluate total power draw of the clock configuration
- On-board ambient temperature sensor
- NetSync™ devices only: On-board OCXO/TCXO reference to meet holdover requirements
- Access to all clock device GPIOs
- 3-wire SPI, 4-wire SPI, and I^2C all supported via header for direct serial communication with the device
- Host interface connector header for easy evaluation of AccuTime™-enabled timing solution

Description

The Saturn Evaluation Platform is used for evaluating a broad family of both NetSync and jitter attenuator devices.

These supported clock devices are built on 6th-generation DSPLL® and MultiSynth™ technology. All devices supported by this evaluation board (EVB) feature an on-chip crystal oscillator (XO) and an on-chip BAW oscillator (BOSC) that act in tandem as a high-frequency dual reference to provide the lowest phase noise floor for sub-10 kHz (close-in phase noise) and across the rest of the integration band. NetSync devices come with many features to support IEEE 1588/PTP applications. They can be used in conjunction with AccuTime software, which runs on a separate host processor, to provide a complete IEEE 1588/PTP timing solution.

The Saturn EVB is designed to be configured by ClockBuilder Pro software, which offers a GUI for easy evaluation of the clock device. With ClockBuilder Pro EVB GUI, all that is needed is a USB connection to any Windows PC and an external 5 V supply.

1. Functional Block Diagram

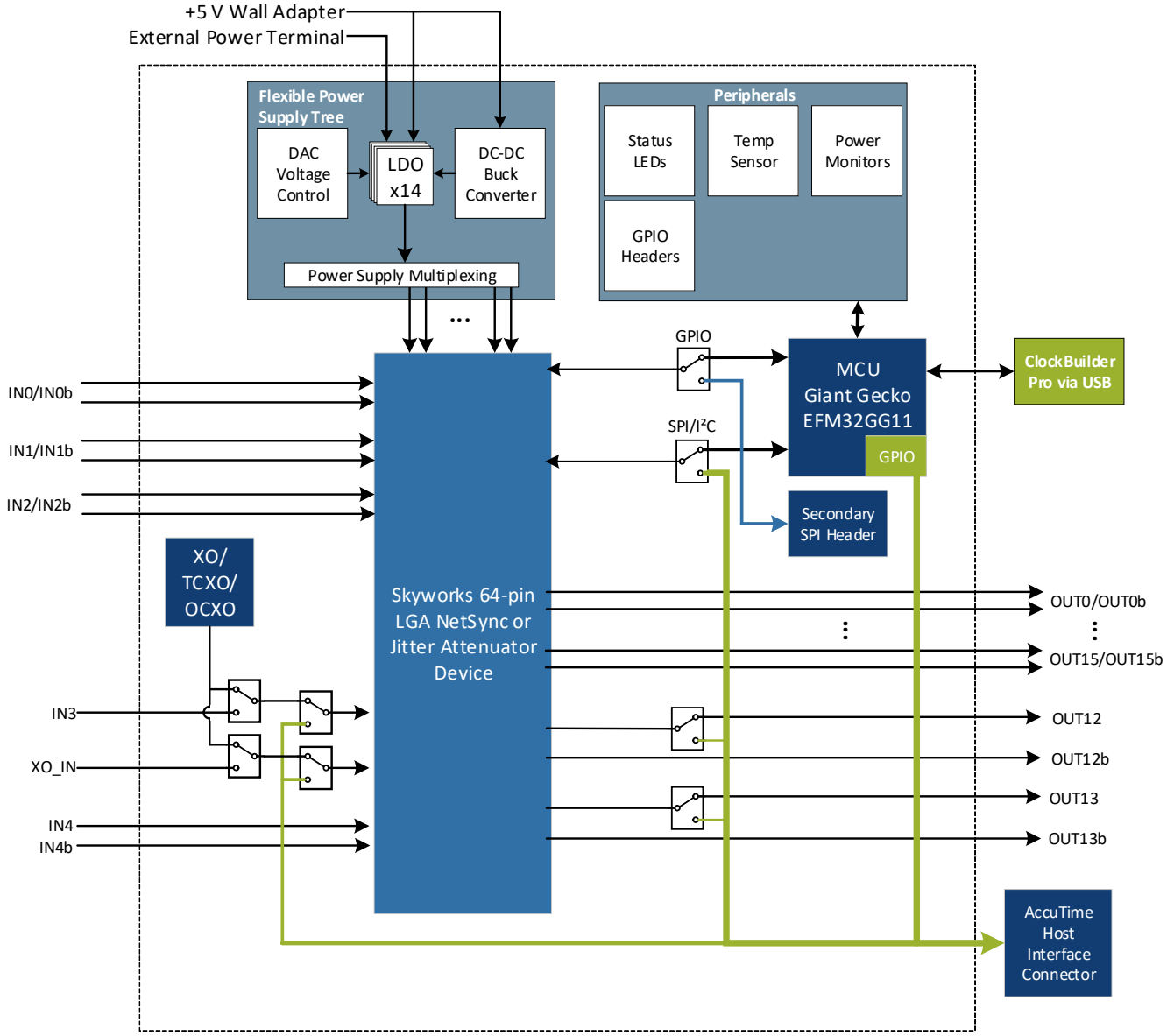

Figure 1. Evaluation Board Block Diagram

2. Quick Start Guide

When first receiving the EVB, confirm that the jumper settings match Figure 2 to ensure that the DUT receives power and serial communications.

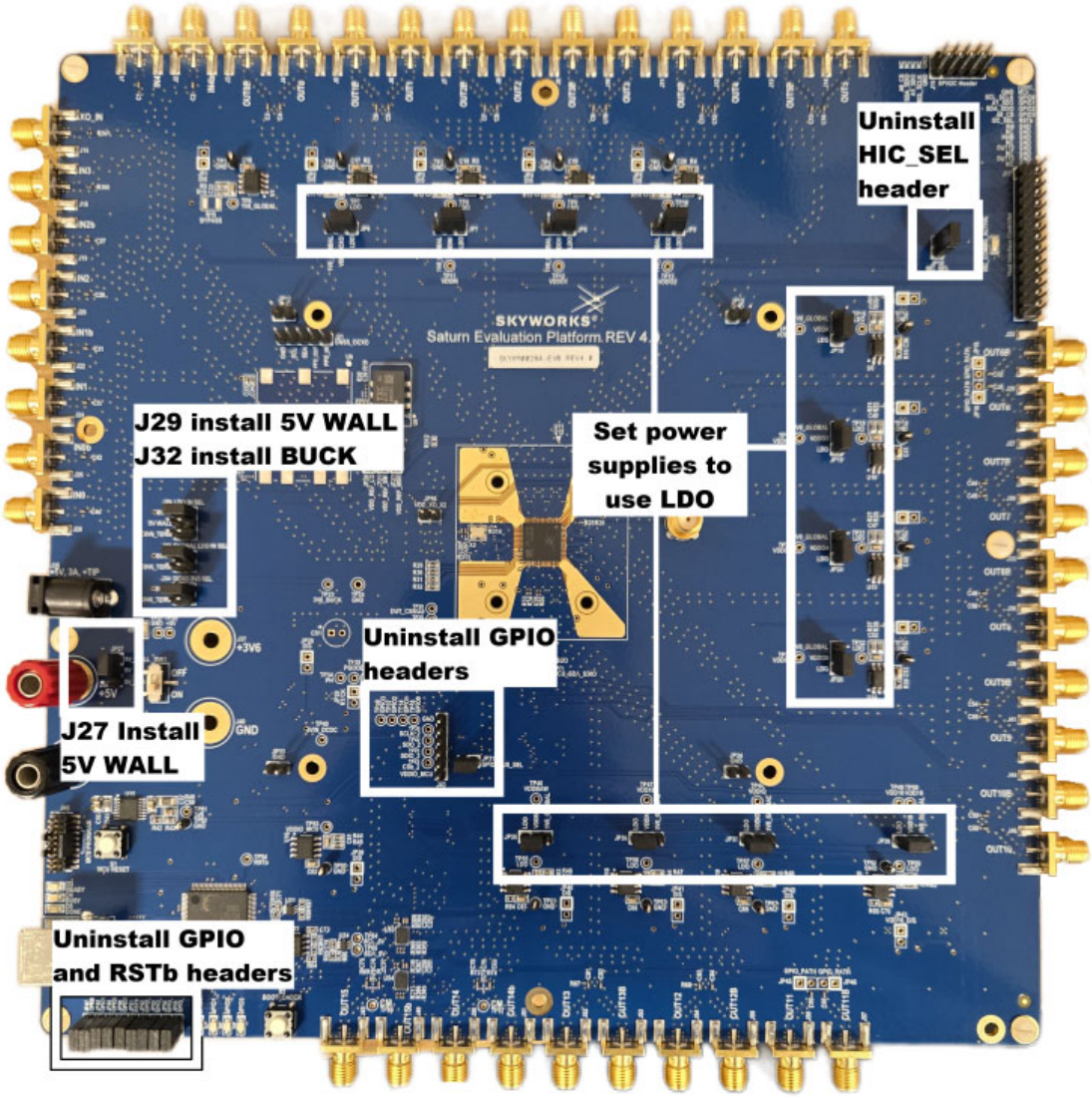

Figure 2. Evaluation Board Quick Start Jumper Settings

After the jumpers are installed as shown above, plug the 5 V dc adapter included in the EVB kit into the J35 barrel plug. Then, plug in the included USB cable. All voltage regulators are set to 3.3 V, except for VDD18 which is set to 1.8 V.

After using the power switch (down-right from the power barrel jack) to turn the board on, a frequency plan may be written to the DUT. The next section briefly covers using ClockBuilder Pro with the EVB as a quick start guide. For more guidance on using ClockBuilder Pro and creating a frequency plan, see the reference manual.

3. Using ClockBuilder® Pro with the EVB

The EVB is designed to work alongside ClockBuilder Pro to streamline the development process. To get started with a sample frequency plan, open ClockBuilder Pro, locate the EVB, and select “Open Sample Project.”

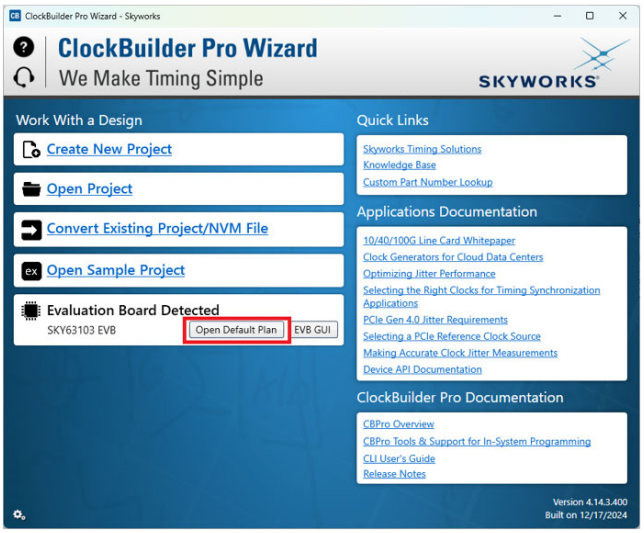

Figure 3. Opening a Sample Project in ClockBuilder® Pro

Inside the frequency plan, the EVB appears under “Evaluation Board Detected.” The opened frequency plan can then be written to flash memory by clicking **Flash DUT.** This retains the configuration even when the DUT is unpowered. Clicking **Write DUT Volatily** writes the plan to the DUT RAM, but the configuration is lost when the DUT is power cycled.

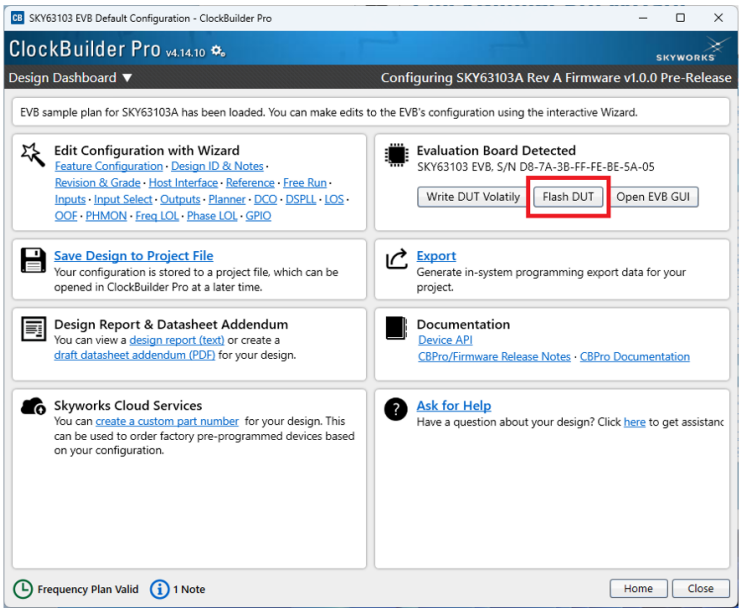

Figure 4. Writing a Frequency Plan to the EVB in ClockBuilder Pro

4. EVB Overview

Figure 5 shows an overhead picture of the EVB highlighting the main areas the user may reconfigure to meet application needs. The EVB supports a socket for internal Skyworks use only.

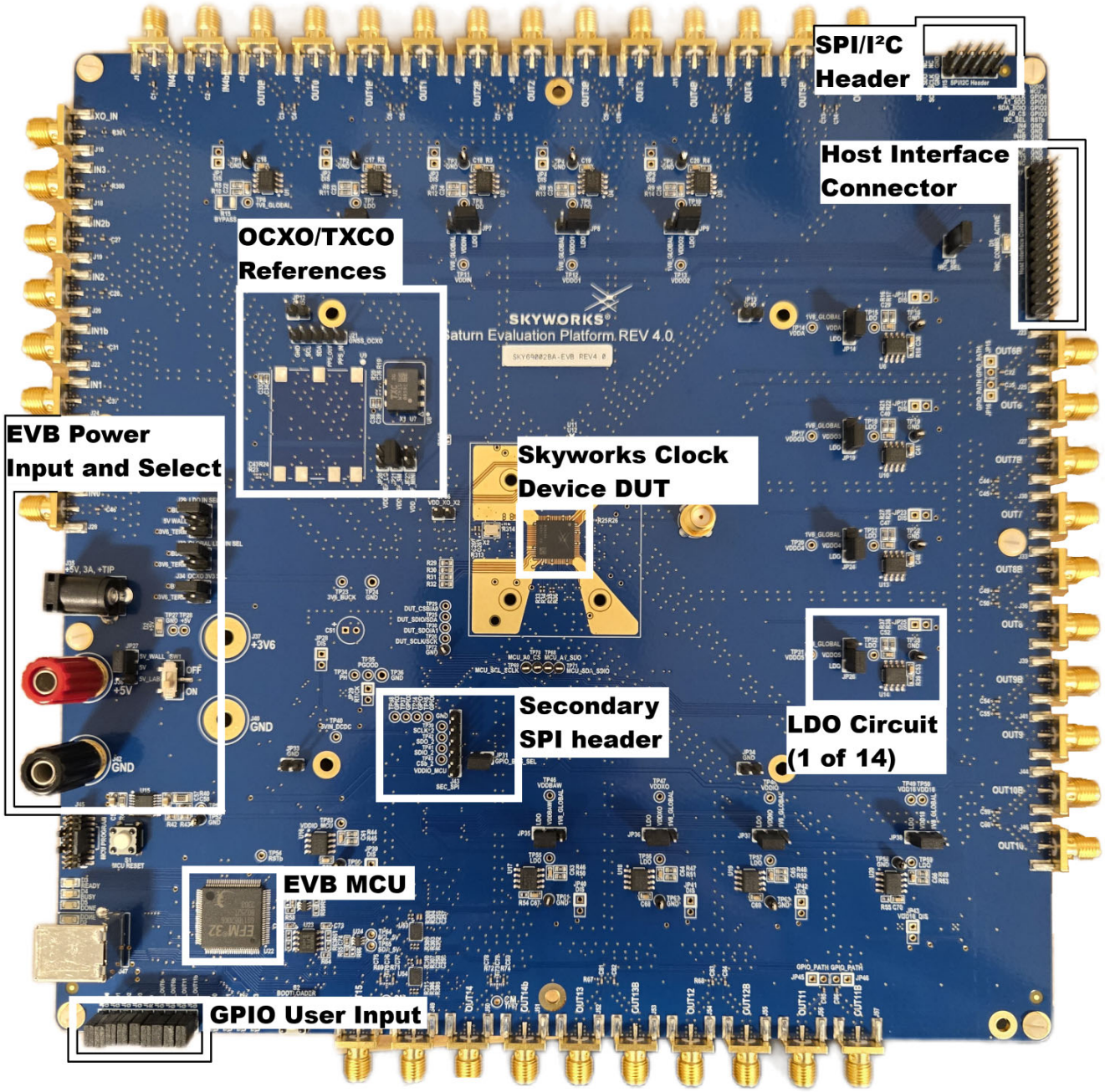

Figure 5. Evaluation Board Overview

5. Flexible Power Supply Tree

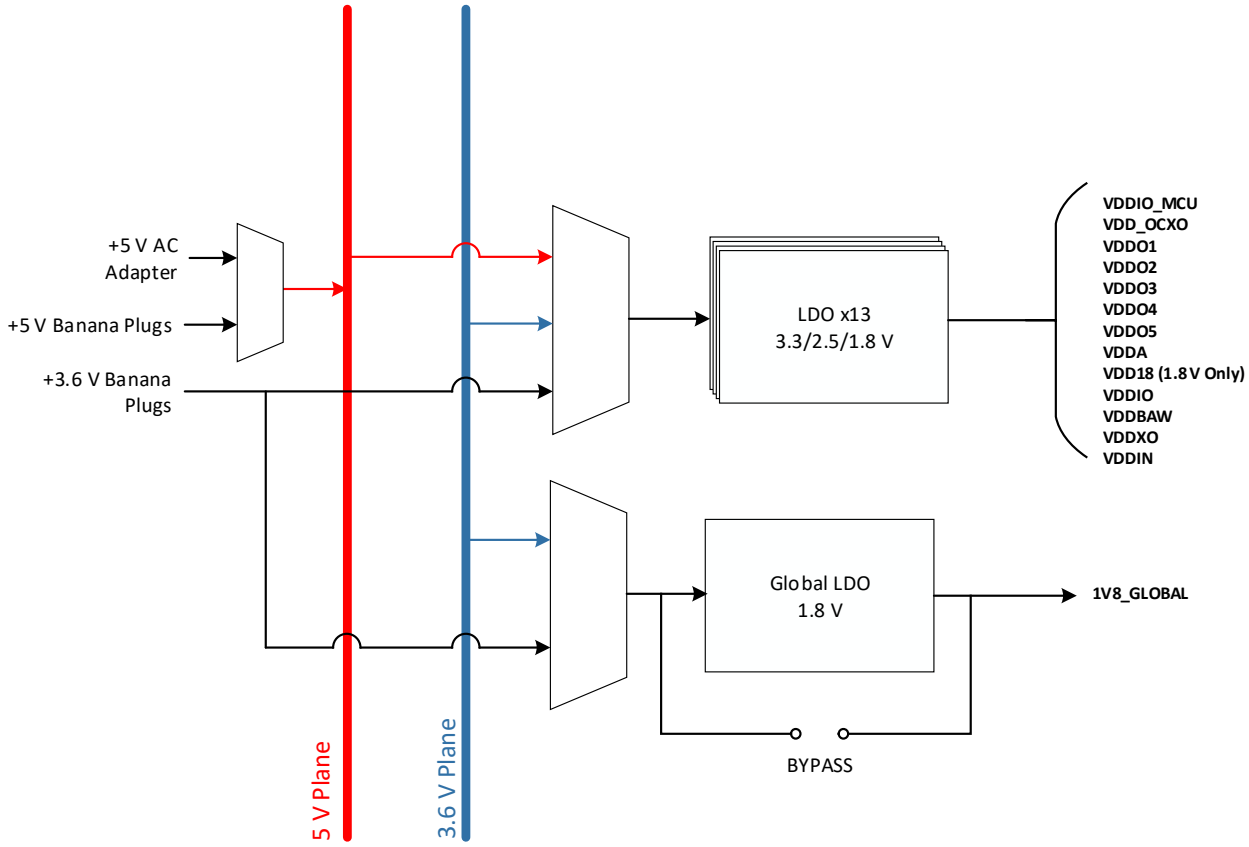

Figure 6. Flexible Power Supply Tree Block Diagram

The EVB is designed to allow different power configurations to match user needs. The clock device can receive power from either individual LDOs for each power pin or from the global 1.8 V LDO. Figure 6 shows all the possible routes for power to the DUT. The user sets the muxes in Figure 6 via headers on the EVB. Please refer to Figure 6 throughout this section.

5.1. Configurable 3.3/2.5/1.8 V LDOs

With the exception of VDD18, all individual LDOs can be independently configured to an output voltage of 1.8 V, 2.5 V, or 3.3 V through the ClockBuilder Pro EVB GUI. After an output voltage is set, it remains at the programmed output voltage upon reset.

Each of the 14 LDOs has a dedicated power monitor to sense both current and voltage to each power pin on the device. All LDOs can be enabled or disabled via the EVB GUI. Each circuit has a test point with silkscreen displaying which power pin on the device the LDO circuit is connected to, as well as a header with a jumper showing which LDO is connected to the power pin. Set the jumper to the “LDO” position to connect the power pin to the individually programmable LDO as shown in Figure 7, which also shows VDDREF receiving power from its individually programmable LDO.

The 1V8_Global option is covered in the section “5.2. Global 1.8 V LDO” on page 8.

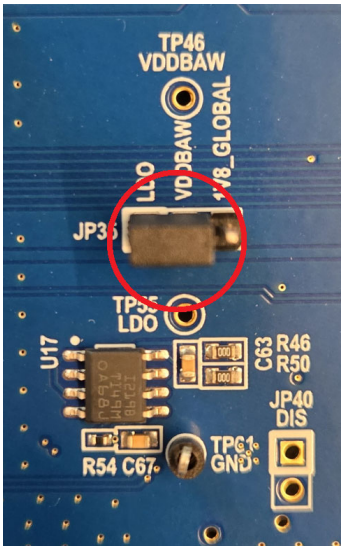

Figure 7. Individual LDO with Programmable Output Voltage

The 11 power supplies to the clock device are described below:

- **VDDO[1:5]** – Clock device output drivers.
- **VDDA** – Core analog supply voltage.
- **VDD18** – Core supply voltage for 1.8 V. Cannot be configured to a different voltage.
- **VDDIO** – I/O clock supply voltage. This determines logic levels for serial communications and GPIO.
- **VDDREF** – Supply voltage for the integrated BOSC reference.
- **VDDRXO** – Supply voltage for the integrated XO reference.
- **VDDIN** – Supply voltage for input supply buffers. This determines input swing levels required for CMOS input clocks.

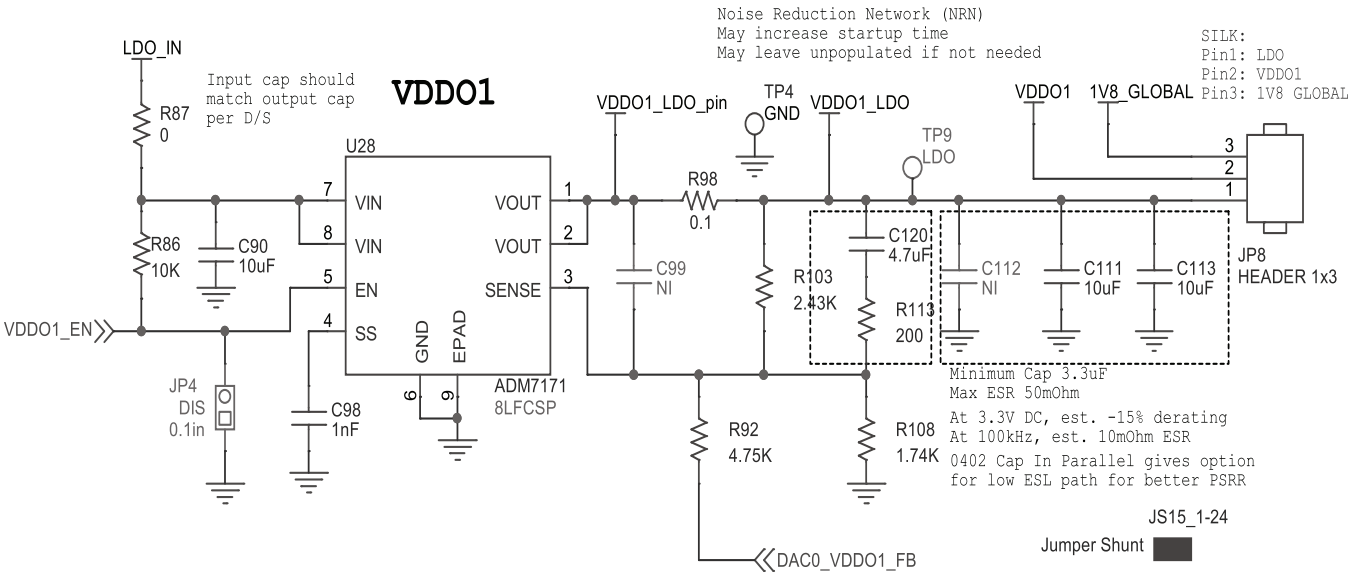

Figure 8. Programmable LDO Circuit Schematic Example

5.2. Global 1.8 V LDO

A global LDO is provided to evaluate a simpler power configuration where a single LDO powers the entire clock device. The global LDO voltage is 1.8 V, providing the lowest power configuration for the DUT. The global LDO also has a power monitor for voltage and current sense, displayed in the ClockBuilder Pro EVB GUI. To configure the device for the global LDO, the user must connect each power pin to the global LDO. Figure 9 shows an example LDO configuration header where JP35 is set so VDDBAW receives power from its individual LDO. For power from the global LDO, change the jumper setting to 1V8_GLOBAL.

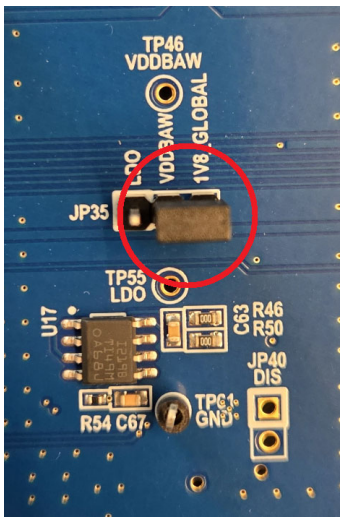

Figure 9. VDDBAW Set to Global 1.8 V Supply

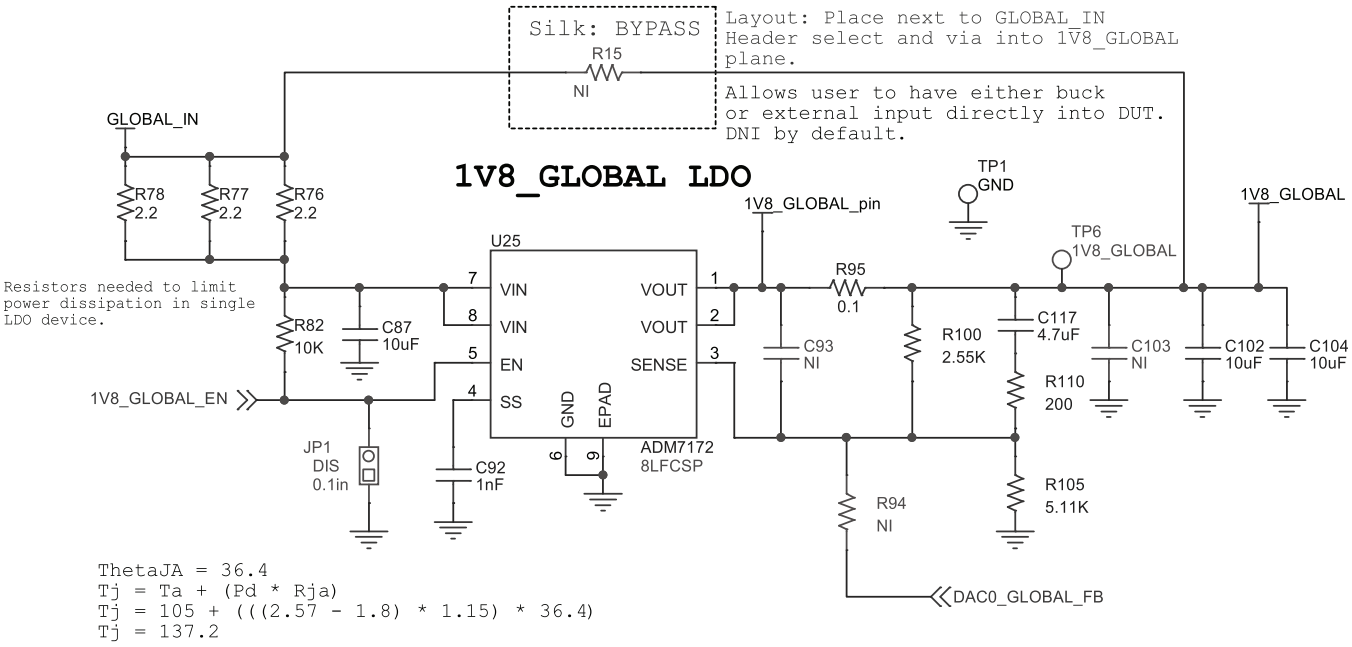

Figure 10. Global LDO Schematic

5.3. VDDIO_MCU and VDD_OCXO

VDDIO_MCU is not electrically connected to VDDIO and powers most of the EVB peripherals that are not part of the DUT. This isolates the power to the clock device and gives the user the most accurate measurement of power consumed for a user-defined configuration. VDDIO_MCU is set to a constant 3.3 V.

For NetSync devices, an on-board OCXO/TCXO is provided to meet holdover requirements. VDD_OCXO is not needed when an OCXO/TCXO is not in use.

5.4. 5 V Plane Input

Figure 11 shows the 5 V input in its default state connected to the 5 V dc adapter. The 5 V plane input can either be the dc adapter provided with the EVB kit that connects to the barrel jack J35, or a lab supply connected to the banana jacks J38 and J42. The three-pin header JP27 is used to select the power source of the 5 V plane, accomplished by connecting the center 5V pin to either the 5V_WALL or 5V_LAB pin. After an input to the onboard 5 V plane is selected, SW1 can be used to power cycle the board.

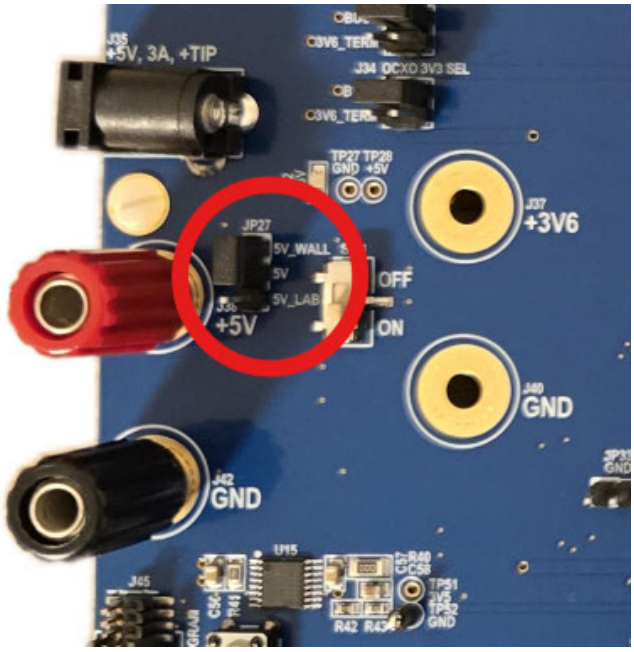

Figure 11. 5 V Plane Input Configuration

5.5. LDO Input Selection

LDO inputs are user-selectable to help create a power tree to mimic an end application. The LDO inputs are determined by the J29 and J32 headers located near the banana jacks. LDO_IN is the shared input for the individual LDOs and can accept input power directly from the 5 V plane, the on-board dc-dc buck converter, or the lower voltage 3.6 V banana jacks. GLOBAL_LDO_IN is the input for the global 1.8 V LDO and can select its input from the dc-dc buck converter or the external supply via the 3.6 V banana jacks. Five V input to the 1.8 V global LDO is not available.

Figure 12 shows an example configuration where LDO_IN gets power from the dc adapter and global LDO gets power from the buck converter.

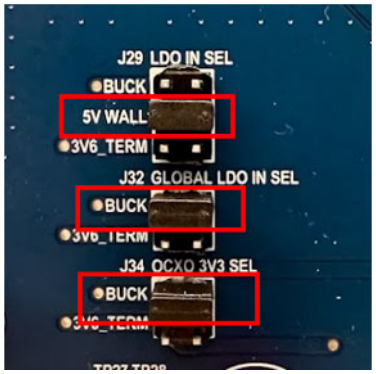

Figure 12. LDO Input Selection Configuration Example

By default, the input to the VDD_OCXO LDO comes directly from the 5 V plane; this configuration is acceptable for most OCXO/TCXO references. A few modifications must be made for specific applications requiring high current (> 1 A dc).

Figure 13 shows the changes needed to connect other voltage supplies to VDD_OCXO. The modifications shown in Figure 13 connect the input of the OCXO to either the on-board buck converter or the external 3.6 V terminal. This selection is made via J34, shown in Figure 12. The resistors that need to be modified can be found near the VDD_OCXO header on the bottom of the board.

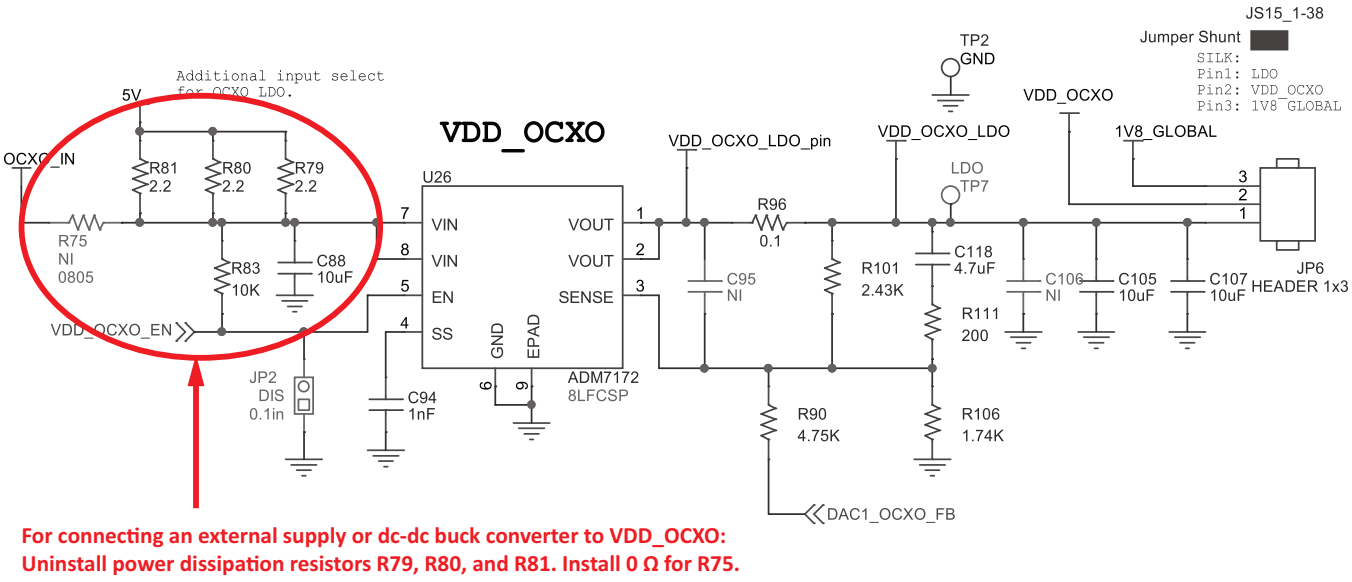

Figure 13. VDD_OCXO Configuration for Buck Converter or External Power Use

5.6. Bypassing LDOs to Supply DUT Power

A few modifications need to be made if a user wants to supply DUT power using the on-board buck converter or an external supply. To bypass the on-board LDOs, install a bypass resistor R15 shown in Figure 14, and then switch the desired supplies to the 1V8_GLOBAL setting as shown in “5.2. Global 1.8 V LDO” on page 8.

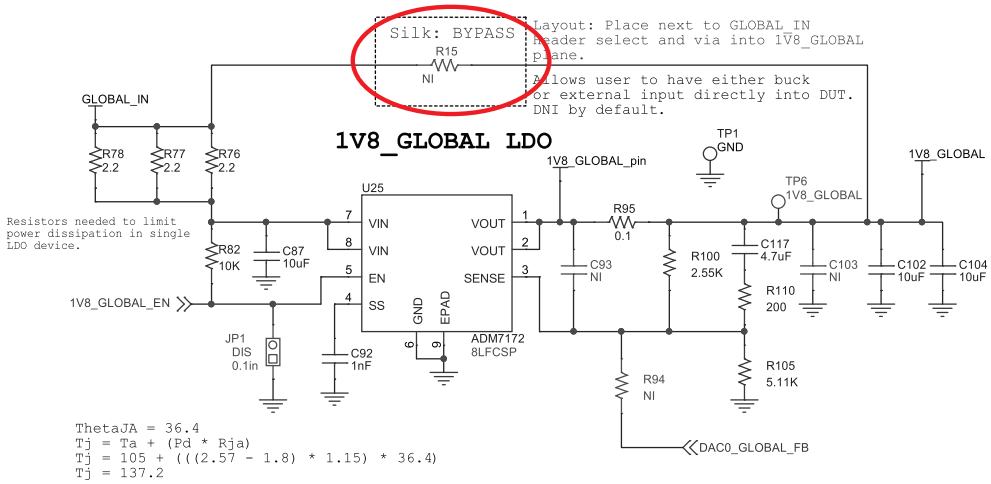

Figure 14. Bypass Resistor

6. On-board Reference Oscillators

6.1. XO Reference

Revision 4.0 or higher Saturn EVBs include a TXC 7X54070001 (54 MHz XO) for use as a phase reference. Because all Saturn EVBs feature DUTs with an internal XTAL, this XO is unpowered and disconnected from the DUT by default. To evaluate the performance of a DUT using an external XO reference, connect the VDD_XO_X2 jumper to power the XO, then install R314 to connect the XO output to the XO_IN pin of the DUT.

If using an external XO, ensure that no other signal goes into the XO_IN pin of the DUT. This can be accomplished by uninstalling R147 (XO_IN SMA connector to XO_IN pin) and R148 (OCXO/TCXO to XO_IN pin) as shown in Figure 15. R147, R148, and R314 all connect to XO_IN. Only one should be installed at a time.

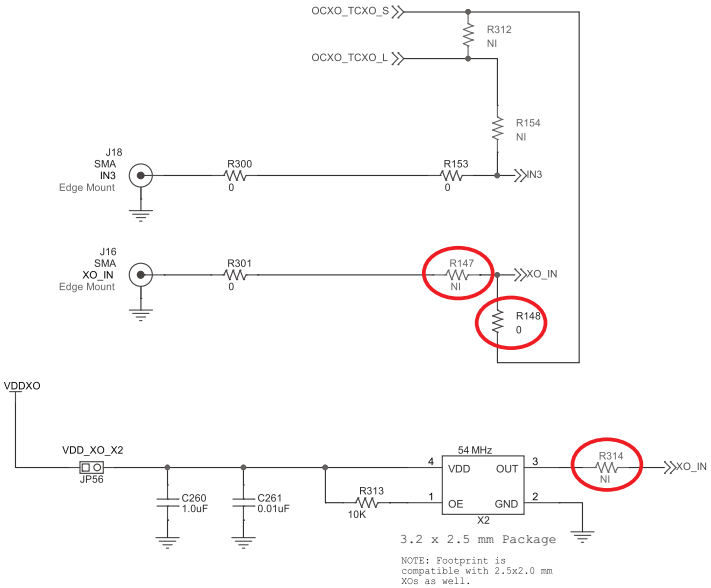

Figure 15. Uninstalling R147 and R148

6.2. TCXO/OCXO References

NetSync applications typically require a TCXO or OCXO for best MTIE/TDEV performance. A TCXO is typically used in applications supporting Synchronous Ethernet (SyncE) and in Full Timing Support (FTS) networks. These applications allow the SyncE signal to provide additional timing stability so that the lower-cost TCXO can be used. In applications without SyncE, or when time holdover is required, an OCXO provides greater stability than a TCXO.

For more information on selecting a holdover reference for your application, see Recommended XTAL, XO, VCXO, TCXO, and OCXO References for Fifth and Sixth Generation DSPLL® Devices. EVBs for NetSync Devices (SKY69001, SKY69002, and SKY69101) have pre-populated holdover references, which are detailed in Table 1.

The Saturn evaluation platform supports various package sizes to accommodate a user-selected reference. Only CMOS output references are supported. Footprints supported are:

- 22 x 25 mm (U2)
- 14 x 9 mm (U4)
- 9 x 7 mm (U3)
- 7 x 5 mm (X1)
- 5.5 x 3.7 mm (U5)
- 3.2 x 2.5, 2.5 x 2.0 mm (X2)

Table 1. Reference Oscillators

Part Number	Supported Skyworks Clock Device	Clock Device Family	Included Reference Oscillators	Reference Oscillator Frequency	Clock Device Input Pin
SKY69002BA-EVB	SKY69001/002	Wireless NetSync	TXC OG48070101 (OCXO)	48 MHz	XO_IN
			TXC 7X54070001 (XO)	54 MHz	Disconnected (XO_IN)
SKY69101BA-EVB	SKY69101	Wireline NetSync	TXC OG48070101 (OCXO)	48 MHz	XO_IN
			Rakon STP3608LF (OCXO)	38.88 MHz	IN3
			TXC 7X54070001 (XO)	54 MHz	Disconnected (XO_IN)
SKY63103AA-EVB	SKY63103	Jitter attenuator	TXC 7X54070001 (XO)	54 MHz	Disconnected (XO_IN)
SKY63102AA-EVB	SKY63102	Jitter attenuator	TXC 7X54070001 (XO)	54 MHz	Disconnected (XO_IN)
SKY63101AA-EVB	SKY63101	Jitter attenuator	TXC 7X54070001 (XO)	54 MHz	Disconnected (XO_IN)

JP20, JP21, and JP22 control power to the references, and only one should be connected at a time. To use the smaller 5.5 x 3.7 mm package, R127 must be populated. When not using the smallest package, it is still advised not to power more than one VDD jumper (and therefore more than one reference) to ensure VDD_OCXO LDO does not reach thermal shutdown.

Connecting an OCXO/TCXO reference to the DUT input requires adding one or more 0 Ω resistors to the board. Figure 18 shows the schematic connection of the XO reference output to the input of the clock device. To attach a small footprint reference to XO_IN, install R148 (uninstalling R147 to remove the unnecessary trace to the SMA connector is recommended). To attach a large footprint reference to IN3, install R154 (uninstalling R153 is recommended).

The user can connect the large reference to XO_IN OR the small reference to IN3, but these options are mutually exclusive. To do so, install R312 and either R154 (for IN3) or R148 (for XO_IN). Install a jumper on JP14 for the U27 OCXO power supply.

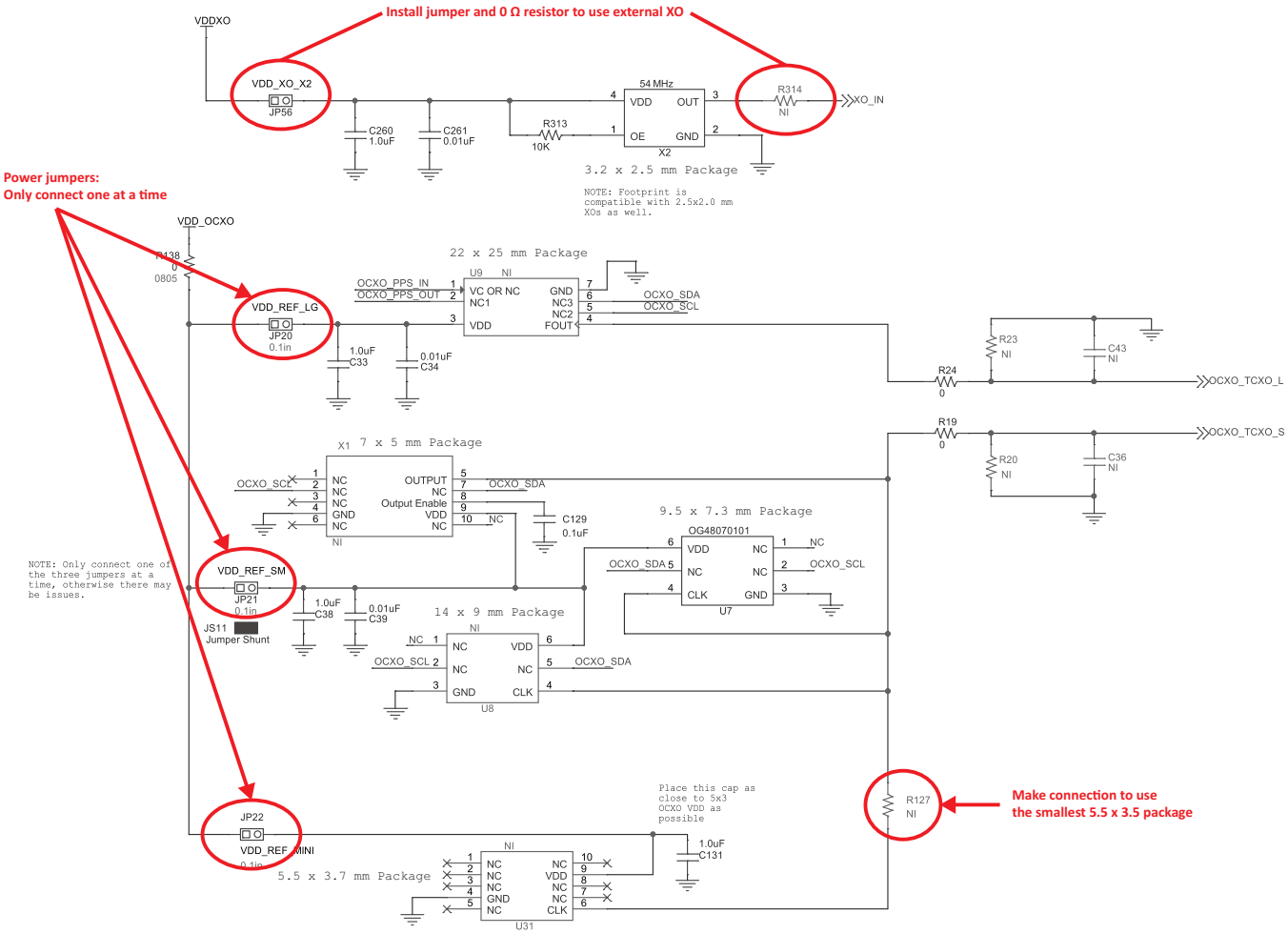

Figure 16. Schematic for External OCXO/TCXO Reference

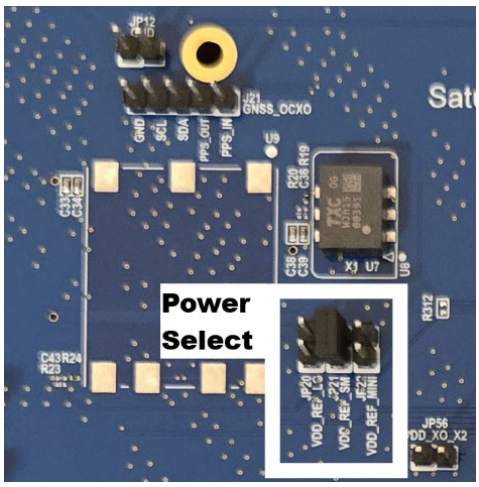

Figure 17. Jumper Configuration for OCXO/TCXO Reference

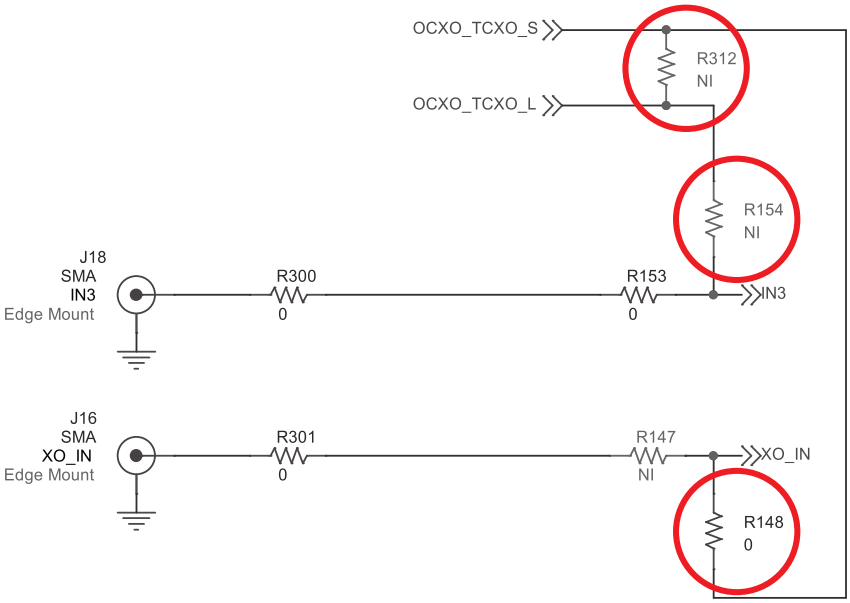

Figure 18. NetSync Reference Input Resistor Configuration

7. Clock I/O

Clock inputs and outputs follow the schematic and layout rules in the device reference manual to ensure the input and output clocks maintain the best signal integrity and phase noise performance for evaluation. IN0 to IN2 have the standard input termination and are configured for differential input clock signals by default. The ac-coupling capacitors can be found directly next to their matching SMA connectors on the edge of the board. The 50 Ω terminations can be found on the bottom side of the board underneath the DUT.

See Figure 19 for reconfiguring the standard input termination to accept CMOS input clocks. IN3 and IN4 differ from the standard input clock termination to accommodate peripheral functions of the EVB as described in "9. EVB Peripherals" on page 19.

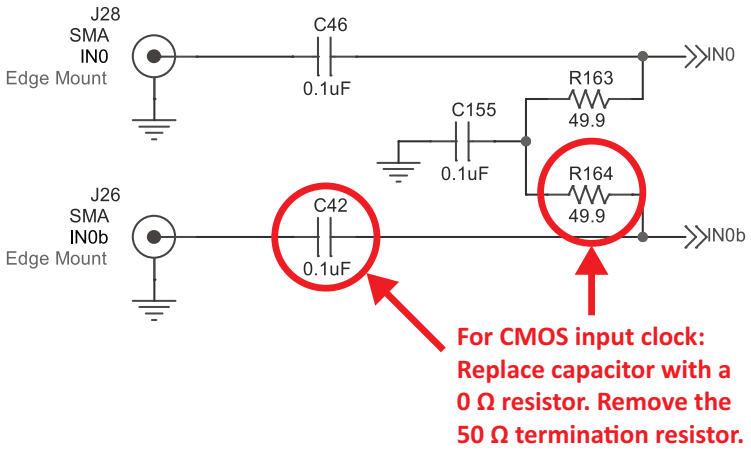

Figure 19. Input Termination Schematic

OUT0 to OUT13 features the standard output termination, which is configured for differential output clock signals such as ac-coupled LVPECL, LVDS, CML, and custom differential output. The output termination can be found directly next to the respective SMA connector on the edge of the board. Figure 20 shows the reconfiguration of the standard output termination for CMOS output clocks.

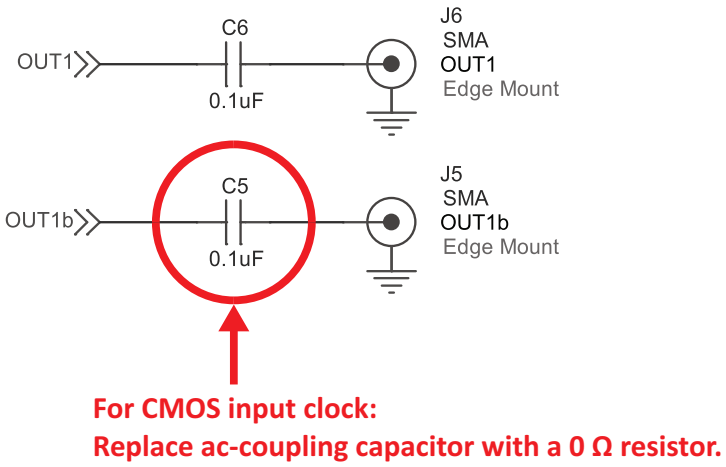

Figure 20. Output Termination Schematic

OUT14 to 15 feature additional termination options to accommodate special user needs. By default, these terminations are set up like the standard termination and are configured for output differential clocks. All termination components are found directly next to their respective SMA connector on the edge of the board. A test point is included to provide an output common mode voltage. If an output common mode voltage is applied, be sure the ac-coupling capacitors are installed to prevent damage to the output drivers of the DUT.

Additional resistors allow the user to output a CMOS clock at a custom-defined logic level by creating a resistor divider after the output driver. See the device reference manual for resistor divider suggested values for output CMOS clocks. Figure 21 shows the output terminations for OUT14 and OUT15.

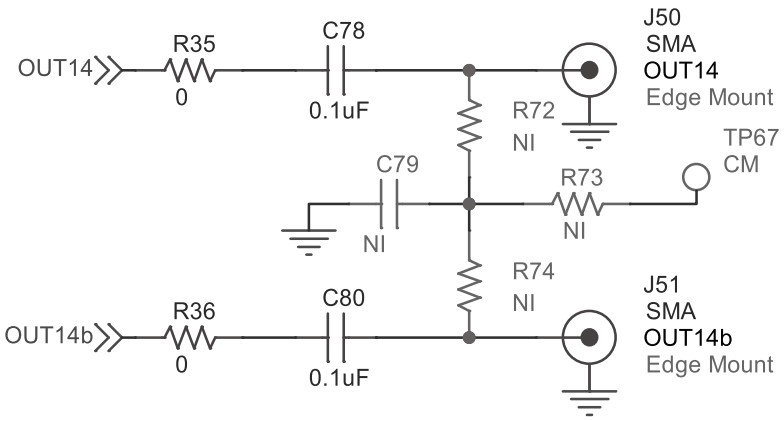

Figure 21. Output Termination Schematic for OUT14 and OUT15

8. Serial Communications

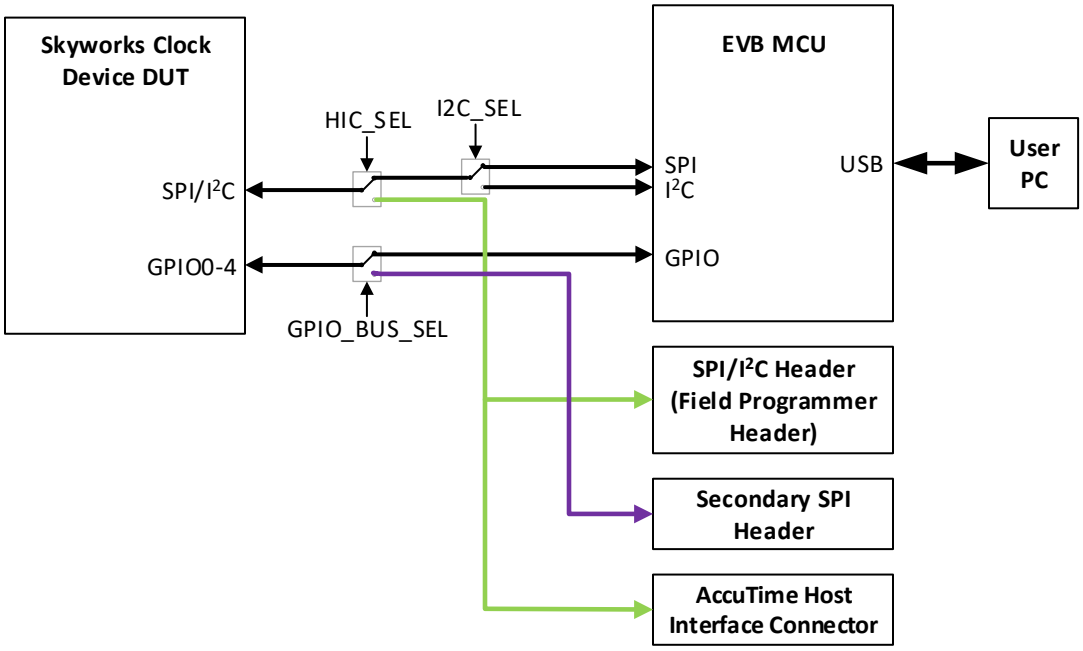

Figure 22. Serial Interface Path Block Diagram

The EVB offers users many different options for communicating with the DUT via serial interface. Figure 22 shows the options available, with the current switch settings in the diagram shown in their default positions. Each switch can be flipped in the ClockBuilder Pro EVB GUI. HIC_SEL and GPIO_BUS_SEL are physically present on the board. They both have a pulldown resistor keeping the switch in the default position. I2C_SEL can only be controlled through software.

8.1. Field Programmer and External Serial Controller

The SPI/I²C header near the host interface connector allows for connection to the Skyworks field programmer, allowing the user to program an in-system device using ClockBuilder Pro. The EVB MCU is already compatible with ClockBuilder Pro, so this is not needed when using the EVB. This header also provides a direct serial link with the device if the user wishes to communicate with the device API without using ClockBuilder Pro. The EVB GUI is not being used in this configuration, so the HIC_SEL header will need a jumper installed to use the SPI/I²C header to communicate with the DUT. Note that this shares the bus with the host interface connector. The host interface connector is discussed in “10. AccuTime™ Host Interface Connector” on page 21.

8.2. Secondary SPI

All Skyworks clock devices supported by the EVB have a secondary SPI port assignable to the GPIO pins of the clock device. The secondary SPI is compatible with both 4-wire and 3-wire SPI and cannot be used to program the DUT. The secondary SPI can be used at the same time as the primary SPI port and has access to the device API, but is mainly intended for status monitoring and phase readback.

See the device data sheet and reference manual for more information on using the secondary SPI port. To use the secondary SPI port on the EVB, populate the jumper on the GPIO_BUS_SEL pin header. J43 is a 6-pin header for the user interface with the secondary SPI port and is not populated on the EVB by default. Figure 23 shows the schematic for the secondary SPI header.

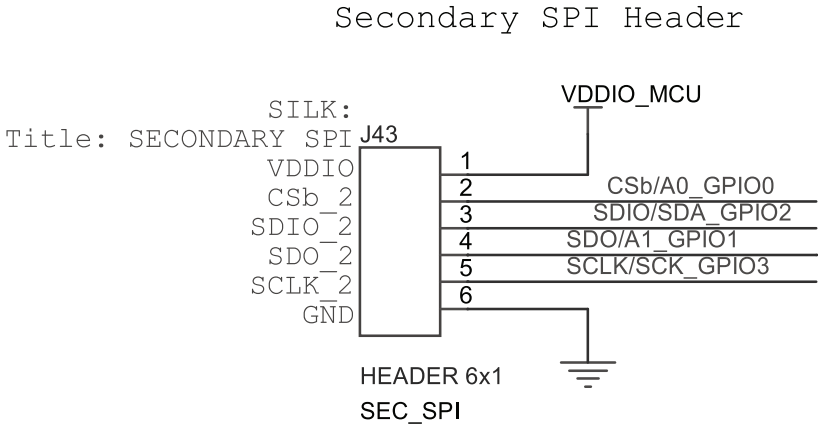

Figure 23. Secondary SPI Header Schematic

9. EVB Peripherals

9.1. GPIO, Reset, and Status LEDs

Skyworks clock devices supported by the EVB all have four dedicated GPIO pins, with some devices having the possibility of using OUT6 and OUT6B, as well as OUT11 and OUT11B, as additional GPIO input-only pins. All possible GPIO pins to the device have a pin header to operate as a user input, and the four dedicated GPIO pins also have status LEDs. All GPIO pin headers and their status LEDs can be found on the edge of the board next to the MCU. GPIO headers are pulled-up to VDDIO when disconnected, and installing the jumper asserts a 0 V signal.

The GPIO pin headers and the GPIO on the clock device are not directly connected; the MCU handles all logic to and from the GPIO on the clock device. The GPIO pin headers on the board serve as user inputs only. Asserted user input from the pin header always takes priority over input from the EVB GUI. If the DUT GPIO is programmed as an output, or if the user wants ClockBuilder Pro EVB GUI to have complete control, leave the jumpers on the GPIO pin headers uninstalled.

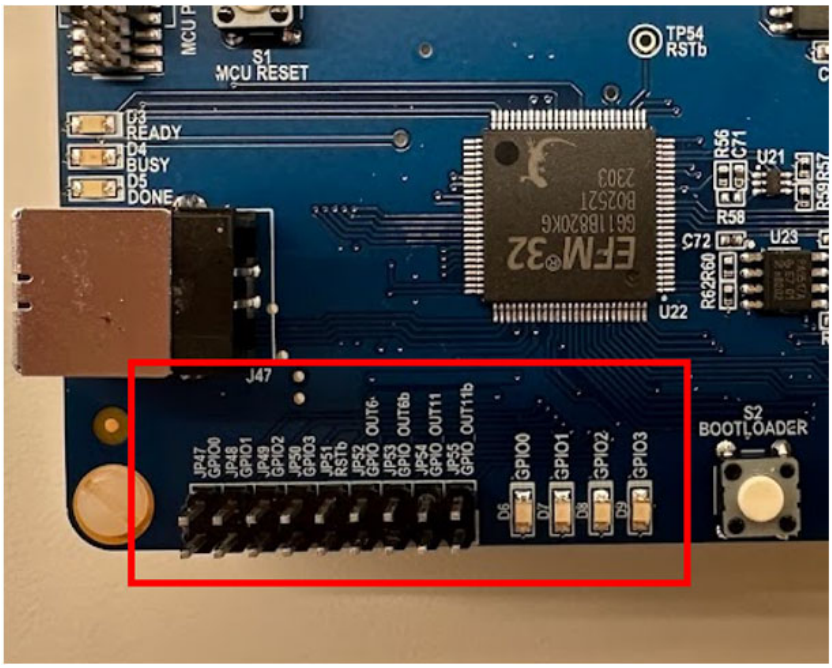

Figure 24. GPIO User Input Headers, GPIO Not Asserted

ClockBuilder Pro can program the GPIO on the clock device as either active-high or active-low when configuring the device frequency plan. For configurations expecting active-high GPIO at the DUT, the user-asserted input on the pin header is converted to an active-high signal for the DUT. For active-low configurations in ClockBuilder Pro, the user-asserted input on the pin header is converted to an active-low signal for the DUT.

The status LEDs follow the DUT-side GPIO voltage blindly. In an active-high DUT configuration, the LEDs turn on when the user asserts a signal on the GPIO pin headers. In active-low configurations, the LEDs turn off when the user asserts input on the pin header.

RSTb is used to place the device into hard reset, and a user-asserted low signal on the pin header takes priority over the EVB GUI. For more information on the device reset behavior on the EVB, refer to the device data sheet and reference manual.

Figure 25 demonstrates how to configure OUT6 and OUT6B, and OUT11 and OUT11B as GPIO inputs. The uninstalled pin headers can be found directly next to the respective output on the edge of the board. Note that when configured as a GPIO input, OUT6 and OUT6B, and OUT11 and OUT11B use VDDO3 and VDDO4, respectively, as their reference for logic level, not VDDIO like the other GPIO inputs.

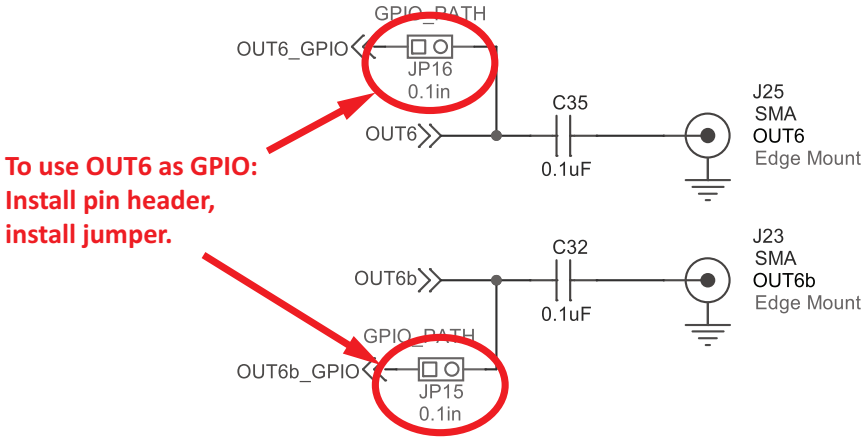

Figure 25. OUT6/OUT6B Configured as GPIO Inputs

9.2. OSYNC (SKY69002)

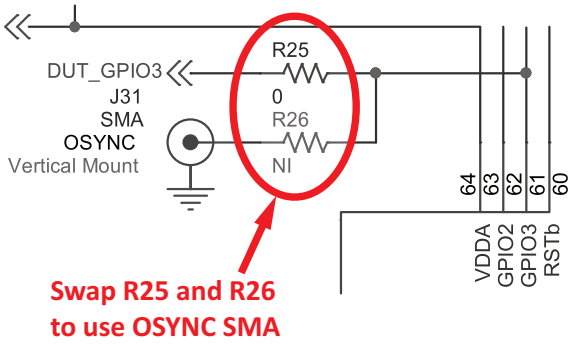

Figure 26. OSYNC SMA Schematic Diagram

The SKY69002 is the only device supported by the EVB that supports the OSYNC feature. OSYNC is important for modern radio network applications such as massive-MIMO. GPIO2 or GPIO3 can be programmed for OSYNC, but on the EVB the OSYNC SMA is connected to GPIO3. The OSYNC SMA is disconnected by default. Figure 26 demonstrates OSYNC SMA activation.

9.3. Power Monitors and Temperature Sensor

Each LDO on board has its own independent power monitor to sense both voltage and current out of the LDO. Individual LDOs are isolated from the power pins on the DUT so the user can get an accurate power measurement for their clock configuration. A temperature sensor is included to measure ambient temperature on the board.

Note: *The temperature sensor is not meant for sensing the DUT temperature. All telemetry readings are displayed in the EVB GUI.*

10. AccuTime™ Host Interface Connector

The AccuTime host interface connector allows easy evaluation of a timing solution using AccuTime and a NetSync clock device supported by the EVB. The host interface connector provides external platform access to two CMOS input clocks, two CMOS output clocks, the serial bus, all DUT GPIO, and RSTb.

IN4 and IN4b are used for the external input clocks and are configured as shown in Figure 27. In order to use external host via the host interface connector, R141 must be swapped with R143 and R142 must be swapped with R144. Resistors that need to be swapped can all be found on the bottom of the board underneath the DUT.

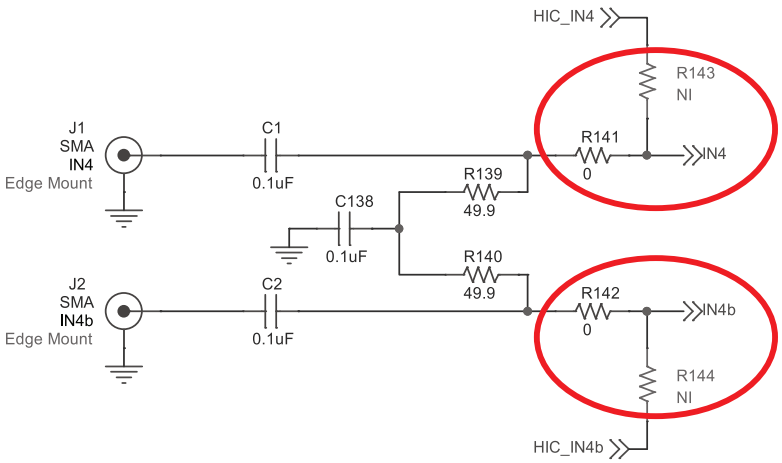

Figure 27. Host Interface Connection Changes

OUT12 and OUT13 are used for the external output clocks. Figure 28 shows OUT12 configured for the host interface connector. Repeat the same process for OUT13. The capacitor and resistor that need to be swapped can be found directly adjacent to their respective SMA connectors on the edge of the board.

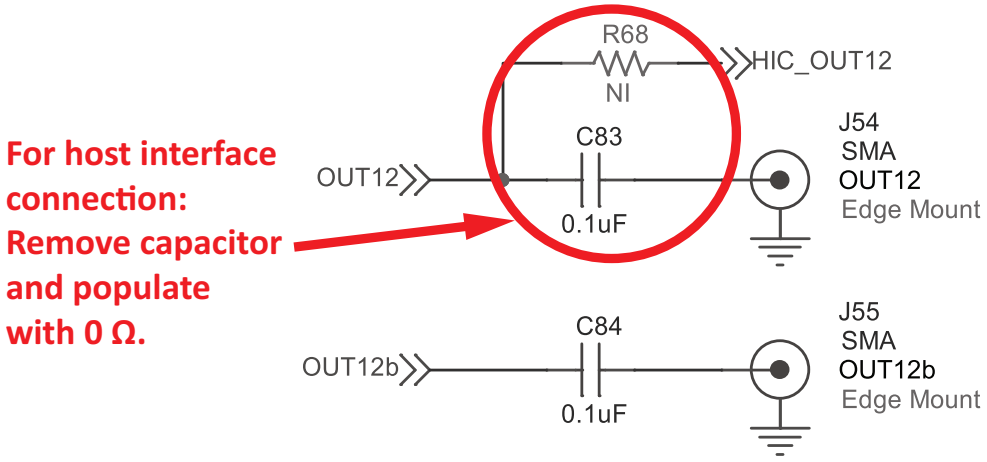

Figure 28. Host Interface Connector Configuration for External Output Clock

To connect the serial bus for communication with the external host, install the jumper to the HIC_SEL pin header JP10 as shown in Figure 29.

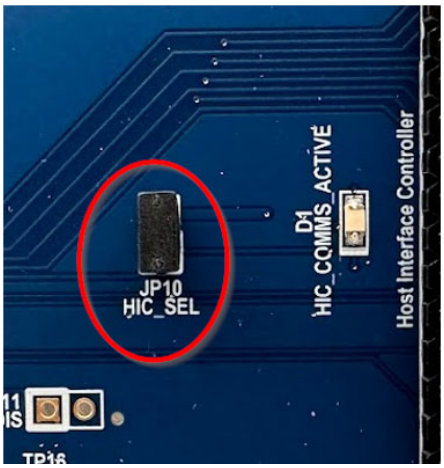

Figure 29. HIC_SEL Header with Jumper Installed

GPIO and RSTb do not need to be configured to connect with an external host because the MCU handles all GPIO logic in and out of the DUT. Configure the GPIO from the external host interfaces with the DUT similarly to the EVB GUI, where the user-input GPIO pin headers on the EVB take priority.

11. Best Practices for Taking Measurements

11.1. Phase Noise Measurements and Baluns

A balun is used when the DUT clock output is a differential signal, but the phase noise analyzer input port is single-ended. A balun converts balanced signals to unbalanced signals and vice versa. A balun board is included in the evaluation kit. Connect differential clocks to the balanced end of the balun using phase-matched cables.

While it is possible to connect only one leg of a differential clock to the phase noise analyzer, it is generally not recommended because the measurement of interest is the clock differential phase noise, not the single-ended phase noise.

Single-ended LVCMOS clocks can be connected to the phase noise analyzer without a balun. Typically, ac-coupling is required to protect the instrument's input buffer, but that may depend on the model of the phase noise analyzer being used.

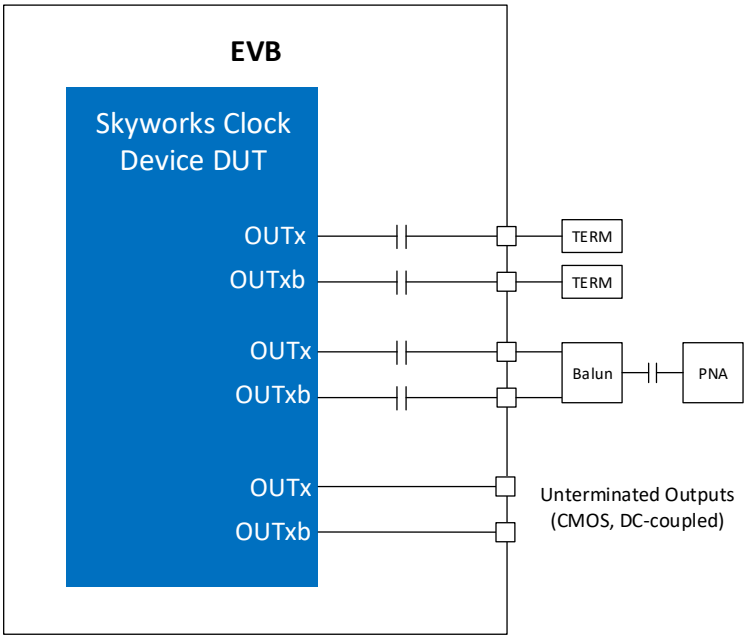

Figure 30. PNA Measurement Diagram

11.2. Zero Delay Mode

Zero Delay Mode (ZDM) externalizes the feedback path of the DSPLL to eliminate delay in all dividers and drivers outside of the PLL loop. A typical application may be when using the PPS PLL available in some NetSync devices. Refer to the DUT reference manual for further information on ZDM.

Typically, the ZDM external feedback path is implemented using a very short trace from the output pin to the input pin in applications designed to achieve the smallest I/O delay possible. Two pairs of phase-matched cables can be used to evaluate the ZDM performance of the DUT (shown in green and orange in Figure 31).

The PLL tries to match the phase of INx and IN_ZDM by adjusting the edge of OUT_ZDM. If the feedback path has the same propagation delay as the path to INx from the clock generator, the OUT_ZDM edge (and therefore OUTx edge) should be completely in phase with the clock edge at the clock generator output, assuming both outputs from the clock generator are in phase to begin with. If the remaining cable pair is also phase-matched, then the edge difference between the two clocks seen on the oscilloscope should ideally be 0, but, realistically, this reflects the ZDM performance of the DUT. All clock pair traces on the EVB are phase-matched.

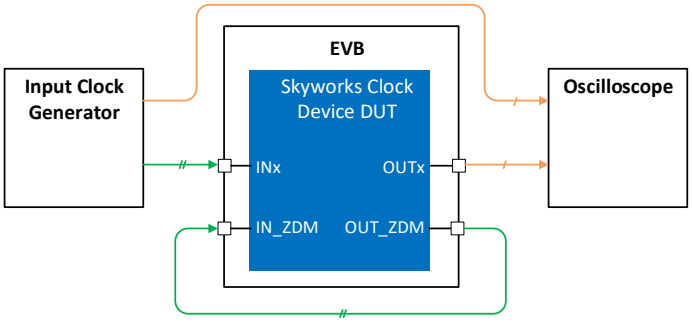

Figure 31. Measurement for DUT ZDM Performance

11.3. Time Domain Measurement of Output Clocks

When taking measurements on one leg of an output clock (e.g., oscilloscope measurements), it is essential to terminate the other leg properly. Because both legs of the output driver operate as a differential pair, one unterminated leg may lead to distortion in both legs of the clock signal. For differential formats, if one leg of the output clock is being measured, its inverse leg should be terminated with a 50 Ω SMA terminator with ac-coupling capacitors installed.

When measuring the clock output waveform, it is essential to use an oscilloscope and probe with sufficient bandwidth to capture the clock rise and fall time. The data sheet specs describe the DUT in isolation and do not take into account PCB effects. Therefore, the output clock rise and fall times may be slightly slower than specified in the data sheet due to the high-frequency losses in the PCB and SMA connectors.

LVCMOS outputs require an external source resistance to match the total source resistance to the trace impedance. See the DUT reference manual for more information on the recommended CMOS termination. OUT14 and OUT15 contain an in-line source resistor found next to the DUT that can be used for source resistance termination. See Figure 32.

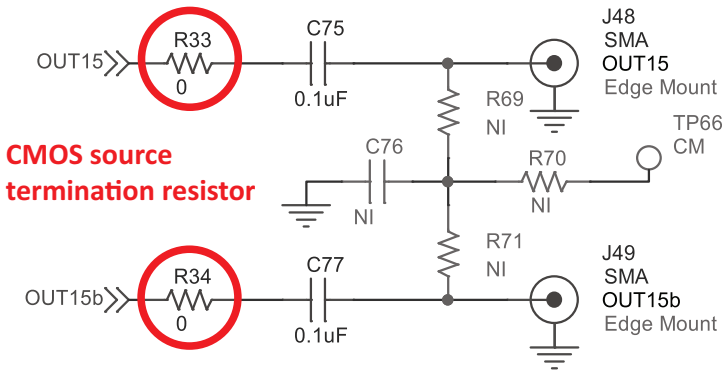

Figure 32. CMOS Source Termination Resistor Schematic Diagram

11.4. Output Clock Skew Measurement

Measuring phase between clock outputs may be important in some applications. Frequency counters may be used if they have time interval measurement capability. However, an oscilloscope is the preferred instrument because the entire clock waveform can be examined. In both cases, the zero-crossing voltage should be equal to the midpoint of the clock waveform period. For ac-coupled clocks, this is at 0 V. Phase-matched cables should be used, and oscilloscope channel-to-channel skew should be calibrated out prior to taking the measurement in order to minimize errors due to instrumentation. Sufficient oscilloscope bandwidth is also critical to getting an accurate skew measurement on high-speed clock edges.

12. Appendix

12.1. EVB Jumper Settings

Table 2 lists every pin header input on the board with a brief description. Installing a jumper asserts the connection state in the description.

Table 2. EVB Jumper Input

Reference Designator	Silkscreen Label	Description
JP27	5V	Connect the 5 V plane on the board to either the DC adapter or banana jacks
J29	LDO_IN SEL	Selects the input to the individual LDOs to the DUT power pins. Only connect one input at a time.
J32	GLOBAL_LDO IN SEL	Selects the input to the global LDO. Only connect one input at a time.
J34	OCXO_3V3 SEL	Selects input to the OCXO/TCXO when not configured for 5 V. See “LDO Input Selection”. Connect only one input at a time.
JP20	VDD_U2_OCXO	Connects power to U2, the 22 x 25 mm OCXO.
JP21	VDD_X1_TCXO	Connects power to X1, U3, and U4. OCXO/TCXO footprints for 7 x 5 mm, 9 x 7 mm, and 14 x 9 mm.
JP22	VDD_U5	Connects power to U5, OCXO/TCXO 5.5 x 3.7 mm package.
JP6, JP7, JP8, JP9, JP14, JP19, JP24, JP26, JP35, JP36, JP37, JP38	See middle pin of each header to find the supply name.	Selects either global LDO or individual LDO as the input to the labeled supply voltage.
JP10	HIC_SEL	Control input to connect the serial bus to the host interface connector and SPI/I^2C header.
JP31	GPIO_BUS_SEL	Connects DUT GPIO to the secondary SPI header. Disconnects MCU GPIO from DUT.
JP15, JP16, JP45, JP46	GPIO_PATH	Connects the respective output (OUT6/OUT6B, OUT11/OUT11B) to MCU GPIO for control via ClockBuilder Pro EVB GUI. Jumpers are uninstalled by default.
JP47, JP48, JP49, JP50, JP51, JP52, JP53, JP54, JP55	User input headers, input labeled next to each header	Install jumper to assert active-low signal to the GPIO. See “9.1. GPIO, Reset, and Status LEDs” on page 19 for a complete description of user input behavior.
JP28	DIS	Disables the dc-dc buck converter on board. Jumper is uninstalled by default.
JP43	VDD18_DIS	Install jumper to disable VDD18.
JP1, JP2, JP3, JP4, JP5, JP11, JP17, JP23, JP25, JP39, JP40, JP41, JP42	DIS	Disables the LDO adjacent to the header. Find the middle pin of the local 3-pin select header to determine which LDO is being controlled. The jumper is uninstalled by default.

13. Ordering Information

Table 3. Ordering Options

Part Number	Supported Skyworks Clock Device	Clock Device Family	OCXO/TCXO Included on EVB
SKY69002BA-EVB	SKY69001/002	Wireless NetSync	Yes
SKY69101BA-EVB	SKY69101	Wireline NetSync	Yes
SKY63103AA-EVB	SKY63103	Wireline jitter attenuator	No
SKY63102AA-EVB	SKY63102	Wireline jitter attenuator	No
SKY63101AA-EVB	SKY63101	Wireline jitter attenuator	No

14. Revision History

Revision	Date	Description
B	December, 2025	Updated for Saturn CEVB Rev. 4
A	January, 2025	Initial release